ACC 3203
PS/2 Model 50/60 Floppy Disk Formatter/Controller

- Compatible with IBM* PS/2* Model 50/60 disk drive systems
- Supports 720K/1.2M/1.44M formats
- Supports up to four 3.5" or 5.25" floppy disk drives
- Emulates the NEC765A in an IBM PC environment
- Built-in handshaking signals to operate in either DMA or non-DMA mode
- Built-in address mark detection circuitry to simplify read electronics
- IBM PS/2 Model 50/60 system address decoder
- On-chip digital data separator eliminates critical analog adjustments
- Diagnostic read back registers compatible with PS/2 Model 50/60
- Data rates of 250 and 500 Kbits
- Programmable data record length, 256, 512 or 1024 bytes/sector
- Multisector and multitrack transfer capability
- Flexible data scan capability, single sector or the entire track
- 16-bit half cell divide algorithm reduces soft error rates
- Direct high current drive output
- Single 24 MHz crystal input
- 1.5 micron high performance CMOS technology
- 68-L PLCC package

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General Description

The ACC 3203 is a high performance CMOS single-chip floppy disk controller. With the ACC 3203, designers can build an IBM PS/2 Model 50/60 compatible Floppy Disk Drive with fast access time, high reliability and low cost per bit capability.

The ACC 3203 integrates the functions of a standard floppy disk drive controller.

Data separator
Write precompensation circuit
Decode logic
Data rate selection
Clock generation
Drive interface drivers and receivers.

This integration greatly reduces the number of components required to interface floppy disk drives to a microprocessor system.

ACC Microelectronics Corporation · 3295 Scott Blvd. · Santa Clara, CA 95054
Phone: 408-980-0622 FAX: 408-980-0626

The ACC 3203 supports up to four floppy disk drives. It is compatible with IBM System 34 double density format (MFM), and Sony EMCA format.

The ACC 3203 contains the decode logic for the internal registers, the write logic and the read logic. The system address decoder is compatible with IBM PS/2 Model 50/60 systems.

Handshaking signals are provided to make DMA operation easy to incorporate with the aid of an external DMA control chip. The ACC 3203 operates in either DMA or Non-DMA modes. In the Non-DMA mode, the ACC 3203 generates interrupts to the processor each time a data byte is available. In DMA mode, the processor only needs to load the command into the ACC 3203 which will control all data transfers.

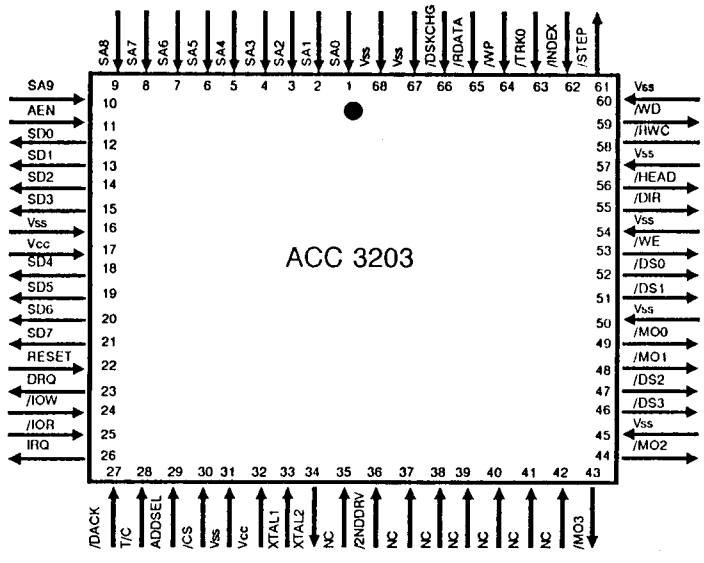
The Data Separator in the ACC 3203 minimizes read error rates for high performance floppy disk drives. The on-chip phase loop adjusts the clock used during data read to keep it in phase with the data signal. Write precompensation is included in addition to the formatting, encoding/decoding, stepper motor control, and status sensing functions. All inputs are TTL compatible, and outputs to the floppy drive are high current, open drain allowing direct drive interface.

Using a single 24 MHz crystal input, the ACC 3203's internal Clock Generation circuit provides all timing signals for the sampling clock, write clock, and master clock. It generates 8 and 4 MHz to handle standard data rates of 500 and 250 Kb/s.

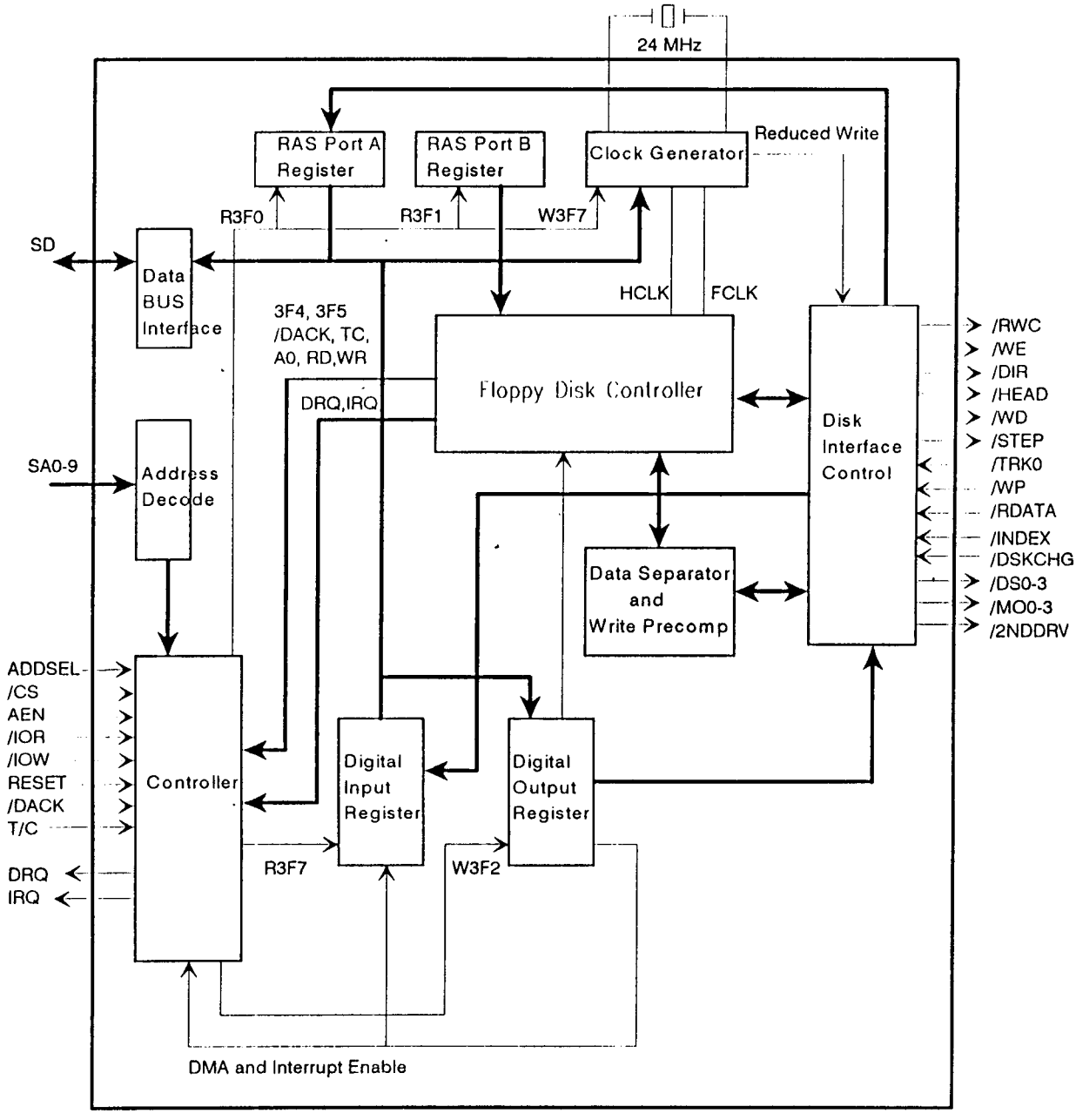
The ACC 3203 executes the following fifteen commands from the microprocessor.

- Read Data
- Read Deleted Data
- Read a Track
- Read ID
- Write Data
- Write Deleted Data
- Format a Track
- Scan Equal
- Scan Low or Equal
- Scan High or Equal
- Recalibrate
- Sense Interrupt Status
- Specify
- Sense Drive Status
- Seek

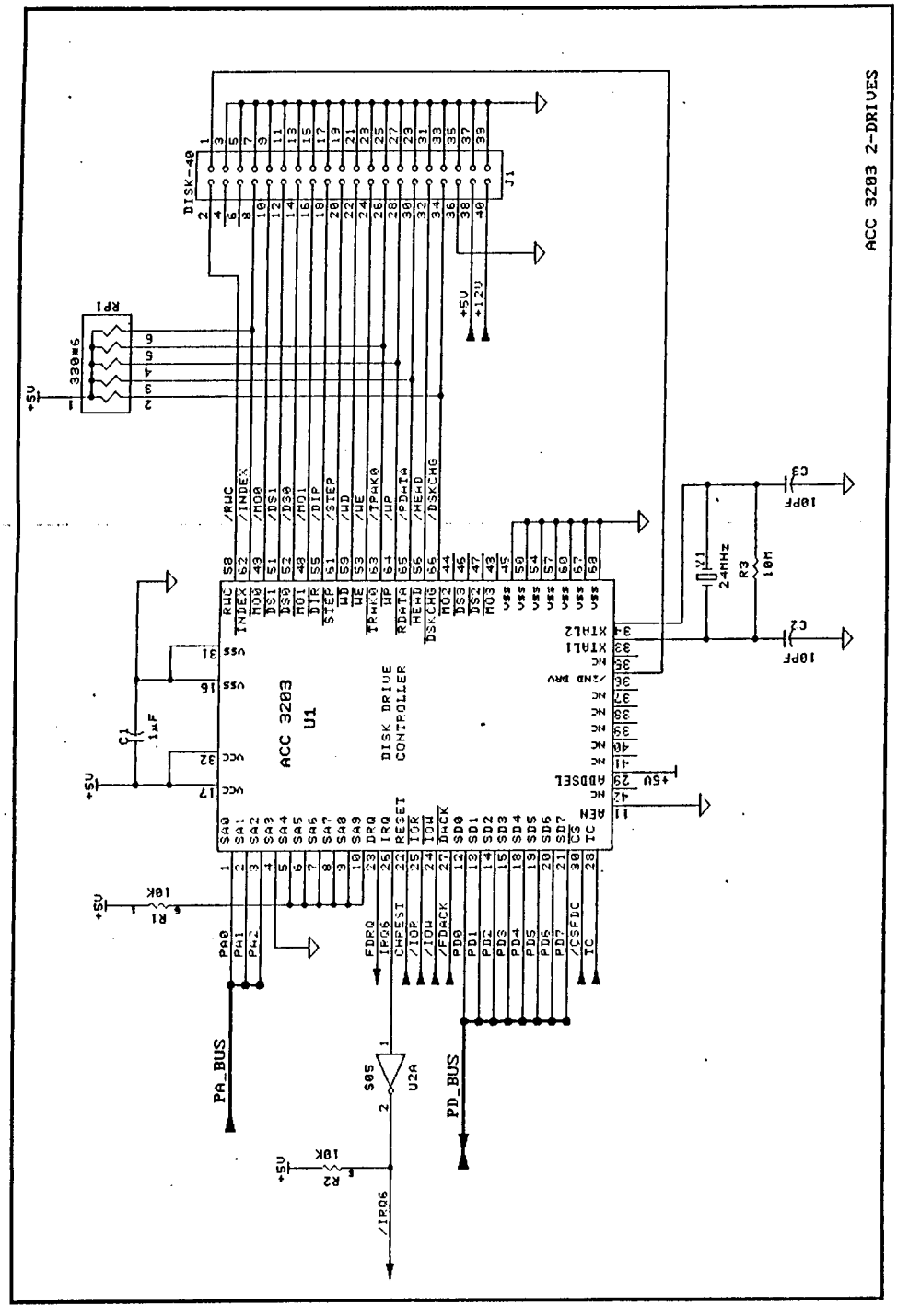
Pin Diagram



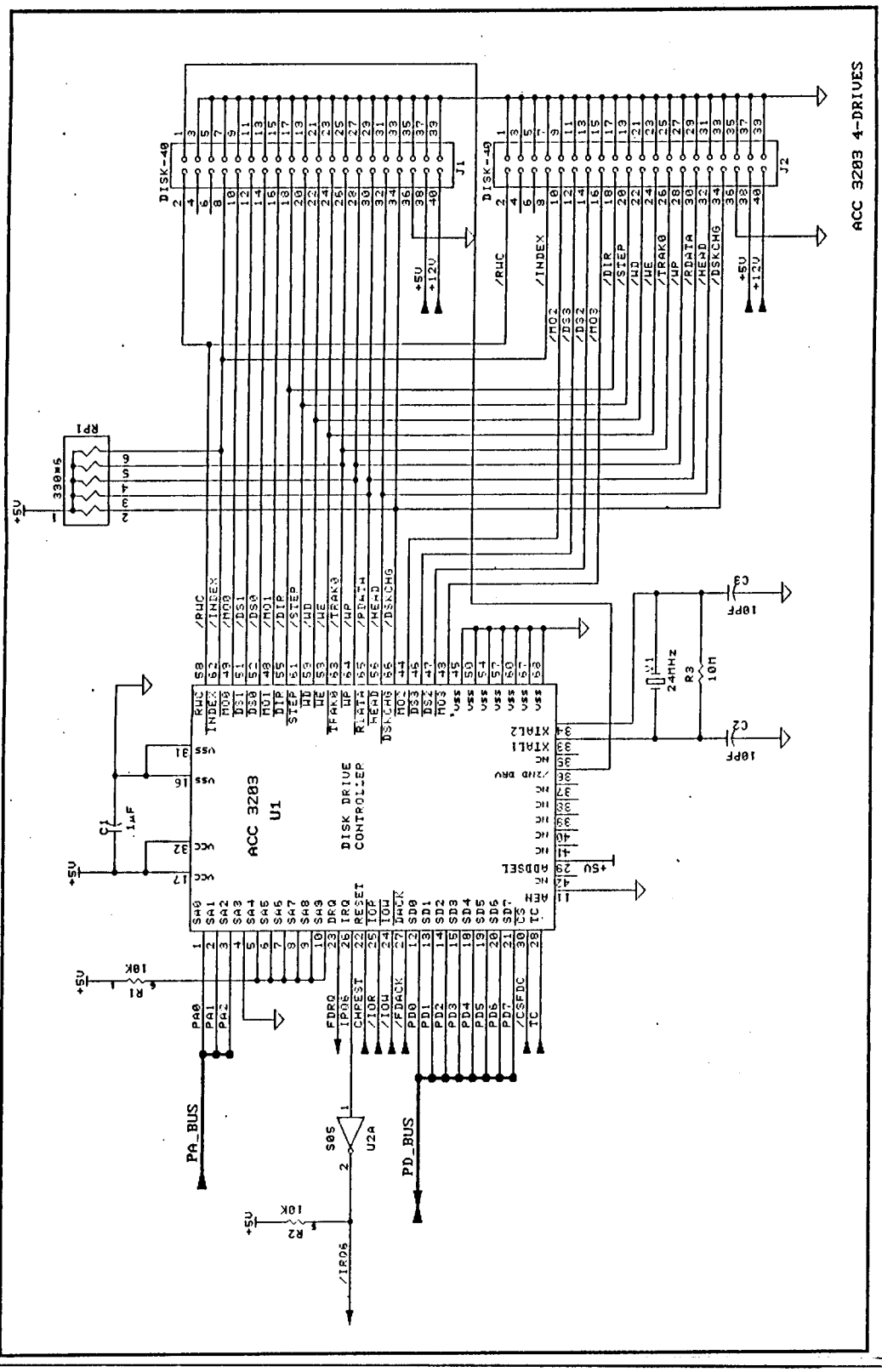
Block Diagram



Typical Application (2 Drives)



Typical Application (4 Drives)



Pin Descriptions

Symbol	Pin	I/O	Pin Description
SA0	1	I	Address bus.
SA1	2		
SA2	3		
SA3	4		
SA4	5		
SA5	6		
SA6	7		
SA7	8		
SA8	9		
SA9	10		
AEN	11	I	Address enable. Input from DMA controller. When this line is active, the DMA controller has control of the address bus.
SD0	12	I/O	Data bus.
SD1	13		
SD2	14		
SD3	15		
SD4	18		
SD5	19		
SD6	20		
SD7	21		
RESET	22	I	Active high input that resets the controller to the idle state. Resets all the output lines to floppy disk drive to their disabled states.
DRQ	23	O	DMA request by FDC when DRQ=1.
/IOW	24	I	Command from the processor to transfer data from the SD bus to the FDC,
/IOR	25	I	Command from the processor to transfer data from the chip to the SD bus.
IRQ	26	O	Interrupt request generated when IRQ=1.
/DACK	27	I	When set to 0, a DMA cycle is active and the controller performs a DMA transfer.
TC	28	I	When set to 1, terminates data transfer during Read/ Write/Scan commands in DMA or interrupt mode.
ADDSEL	29	I	Address select. When set to 1, SA=3FX. When set to 0, SA=37X

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/CS	30	I	Chip Select. When set to 0, FDC is selected,
XTAL1	33	I	XTAL oscillator input.
XTAL2	34	O	XTAL oscillator drive output.
/2NDDRV	36	I	Pulled low to indicate a second floppy drive is present in the system. A built-in pullup resister keeps the pin high if it is left floating.
/MO3 /MO2 /MO1 /MO0	43 44 48 49	O	When set to 0, the MOTOR ON enables disk drive 3. This is an open drain output.
/DS3 /DS2 /DS1 /DS0	46 47 51 52	O	When set to 0, the drive select enables disk drive 3. This signal is an open drain output.
/WE	53	O	Write Enable. When set to 0, causesa write from the microprocessor to the FDD. An open drain output.
/DIR	55	O	Direction of the head stepper motor. An OD output. Logic 1 = outward motion. Logic 0 = inward motion.
/HEAD	56	O	Head select. Open drain output. Determines which disk drive head is active. Logic 1 = Side 0. Logic 0 = Side 1.
/RWC	58	O	Reduced write current. This signal can be used on two-speed disk drives to select the transfer rate. Logic 0 = 250KB/s. Logic 1 = 500KB/s. An OD output.
/WD	59	O	Write Data. Logic low open drain. Writes precompensated serial data to the selected floppy disk drive. An OD output.
/STEP	61	O	STEP output pulses. Active low open drain output. Produces a pulse at a programmable rate to move the head to another cylinder.
/INDEX	62	I	Active low Schmitt input from the disk drive. Senses the head positioning over the beginning of a track marked by an index hole.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/TRK0	63	I	Track 00. Active low schmitt input from the disk drive. Signals that the head is positioned over the outermost track.
/WP	64	I	Write Protected. Active low schmitt input from the disk drive indicates that the diskette is write protected.
/RDATA	65	I	Read data input. Signals a read from the FDD to the microprocessor.
/DSKCHG	66	I	Diskette change. This signal is active low at power-on and when the diskette is removed. It remains active until a /step pulse is received with the diskette in place.
VCC	17, 32		+5 volt supply
VSS	16, 31, 45, 50, 54, 57, 60, 67, 68		Ground
n.c	35, 37, 38, 39, 40, 41, 42		

Register Descriptions

There are seven registers in the ACC 3202, two registers to control specific interface signals, three registers for the status of signals used in diskette operations, and two controller registers. The I/O addresses of these registers are described in the tables below.

Address		Registers	
Primary (ADDSEL=1)	**Secondary (ADDSEL=0)**	**Read**	**Write**
3F0	370	RAS Port A register	
3F1	371	RAS Port B register	
3F2	372		Digital output register
3F4	374	Main status register	
3F5	375	Data register	Data register
3F7	377	Digital input register	Diskette control register

RAS Port A Register
(HEX 3F0) (8-bits) (R)

The RAS Port A Register shows the status of corresponding signals.

Bit	Function
7	IRQ 6 (IRQ)
6	/Second Drive (/2DNDDRV)
5	Step (latched)
4	/Track 0 (/TRK0)
3	Head 1 Select (HEAD)
2	/Index (/INDEX)
1	/Write Protect (/WP)
0	Direction (DIR)

RAS Port B Register
(HEX 3F1) (8-bits) (R)

The RAS Port B Register shows the status of signals between the diskette drive and the controller.

Bit	Function
7	Reserved
6	Reserved
5	Drive Select (1 = drive 1)
4	Write Data (latched)
3	Read Data (latched)
2	Write Enable (latched)
1	Motor On 1 (MO1)
0	Motor On 0 (MO0)

Digital Output Register
(HEX 3F2) (8-bits) (W)

The Digital Output Register controls drive motors, drive selection, and feature enable. All bits are cleared by the I/O reset line.

Bit	Function
7	Motor Enable 3
6	Motor Enable 2
5	Motor Enable 1
4	Motor Enable 0
3	DMA and Interrupt Enable
2	/Floppy Disk Controller reset
1,0	Drive Select 0 through 3 00 selects drive 0 01 selects drive 1 10 selects drive 2 11 selects drive 3

Digital Input Register
(HEX 3F7) (R)

The digital input register is for diagnostics.

Bit	Function
7	/Diskette Change (/DSKCHG)
6-1	Reserved
0	250 Rate Select

Diskette Control Register
(HEX 3F7) (W)

The diskette control register set the transfer rate and selects write precompenation.

Bit	Function
7-2	Reserved
1-0	Transfer Rates Select and Reduced Wtire Current Control 00 500 Kb/s /RWC=0 01 250 Kb/s /RWC=1 10 250 Kb/s /RWC=1 11 Reserved

Main Status Register
(HEX 3F4) (8) (R)

The main status register controls data flow between the microprocessor and the controller.

Bit	Function
7	Request for Master 1 Data Register ready for transfer
6	Data Input/Output 1 Data transfer from Controller 0 Data transfer from the SD BUS
5	Execution Mode (Non-DMA mode) 1 Execution
4	Controller Busy 1 Controller busy
3	Drive 3 Busy 1 Diskette 3 in seek mode Drive 3 busy
2	Drive 2 busy 1 Diskette 2 in seek mode Drive 2 busy
1	Drive 1 Busy 1 Diskette 1 in seek mode Drive 1 busy
0	Drive 0 Busy 1 Diskette 0 in seek mode Drive 0 busy

Data Register
(HEX 3F5) (8) (R/W)

The Data Register consists of four status registers in a stack. Only one register is presented to the data bus at a time. It stores data, commands and parameters, and provides diskette/drive status information. Data bytes are passed through the data register to program or obtain results after a command.

Status Register 0 (ST0)

Bit	Function
7-6	IC (Interrupt Code) 00 Normal termination of command 01 Abnormal termination of command 10 Invalid command issue 11 Abnormal termination because the ready signal from FDD changed state during command execution
5	SE, seek end 1 seek end
4	EC (Equipment Check) 1 When a fault signal is received from the FDD, or the track 0 signal fails to occur after 77 step pulses 0 No error
3	NR (Not Ready) 1 Drive is not ready 0 Drive is ready
2	HD (Head address) 1 Head 1 select 0 Head 0 select
1-0	US1,US0. Drive select 00 Drive 0 select 01 Drive 1 select 10 Drive 2 select 11 Drive 3 select

Status Register 1 (ST1)

Bit	Function
7	EN (End of Cylinder) 1 When the FDC tries to access a sector beyond the final sector of a cylinder.
6	Not used. This bit is always 0.
5	DE (Data Error) 1 When the FDC detects a CRC error in either the ID field or data field.
4	OR (Over Run) 1 IF the FDC is not serviced by the host system during data transfer within a set time interval
3	Not used. This bit is always 0.
2	ND (No Data) 1 During execution of Read Data
1	NW (Not Writable) 1 During execution of Wrtie Data
0	Missing Address Mark 1 When the FDC cannot detect the data address mark or deleted data address mark

Status Register 2 (ST2)

Bit	Function
7	Not used. This bit is always 0
6	CM (Control Mark) 1 During execution of the Read Data or Scan command.
5	DD (Data Error in Data Field) 1 If the FDC detects a CRC error in the data field.
4	WC (Wrong Cylinder) 1 Wrong Cylinder
3	SH (Scan Equal Hit) 1 During execution of the Scan command, if the condition "equal" is satisfied.
2	SN (Scan Not Satisfied) 1 During execution of the Scan command if FDC cannot find a sector.
1	BC (Bad Cylinder) 1 Bad Cylinder
0	MD (Missing Address Mark in Data Field) 1 When data is read from the medium, if the FDC cannot find a data address mark or deleted data address mark.

Status Register 3 (ST3)

Bit	Function
7	FT, Fault
6	WP, Write Protected
5	RY, Ready
4	T0, Track 0
3	TS, Two-Side
2	HD, Head Address
1	US1, Unit Select 1
0	US0, Unit Select 0

Commands

The ACC 3202 diskette controller is capable of performing fifteen commands. Each command is initiated by a multi-byte transfer from the microprocessor. The result can also be a multi-byte transfer back to the microprocessor. Each command consists of three phases: Command, Execution, and Result.

Command

The microprocessor issuses all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After completing the operation, status information and other housekeeping information are made available to the microprocessor.

Command Symbol Descriptions

A0 Address Line 0
A0 controls the selection of main status register (A0=0) or data register (A0=1).

C Cylinder Number
Current or selected cylinder (track), numbers 0 through 76.

D Data
Data pattern to be written into a sector.

D_7-D_0 Data Bus
8 bit data bus, where D_7 stand for the most significant bit, and D_0 stands for the least significant bit.

DTL Data Length
The value of this byte is normally ignored by the controller. However a byte must be written at this location.

EOT End of Track
The final sector number on a cylinder.

GPL Gap Length
The length of gap 3. During Read/ Write commands this value determines the number of bytes that VCO sync keeps low after two CRC bytes. During Format command it determines the size of gap 3.

H Head Address
Head number 0 or 1, as specified in the ID field.

HD Head
Selected head number 0 or 1. (H=HD in all commands)

HLT Head Load Time
The head load time in the selected FDD (2 to 254 ms in 2 ms increments.)

HUT Head Unload Time
Time after a Read or Write operation. (16 to 240 ms in 16 ms increments).

MF FM or MFM Mode
Must be 1 to select MFM mode.

MT Multitrack
If MT is high, a multitrack operation is performed. If MT=1 after finishing a read/write operation on side 0, FDC automatically starts searching for sector 1 on side 1.

N Number
The number of data bytes written in a sector.

NCN New Cylinder Number
New cylinder number reached as a result of the seek operation; desired position of head.

ND Non-DMA Mode

PCN Present Cylinder Number
Cylinder number at the completion of the Sense Interrupt Status command, current position of the head.

R Record
The sector number to be read or written.

R/W Read/Write
Either a Read or Write signal.

SC Sector
Number of sectors per cylinder.

SK Skip
Skip deleted data address mark.

SRT Stepping Rate
These bits indicate the stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (FH=1ms, EH=2 ms, etc.).

ST0-ST3
Status 0-Status 3
One of the four registers that store status information after a command has been executed. This information is available during the result phase after command execution. These registers must not be confused with the main status register (selected by A0=0). ST0-ST3 are read only after a command has been executed and only if they contains information relevant to the command.

STP Scan Test
If STP=1 during a scan operation, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA). If STP=2, alternate sectors are read and compared.

US0-1 Unit Select
Selected drive number 0 or 1.

COMMAND FORMAT

The following commands can be issued to the controller. An "x" indicates a "don't care" condition.

READ DATA

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	0	0	1	1	0
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Cylinder Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End of Track							
Byte 7	Gap Length							
Byte 8	Data Length							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

READ DELETED DATA

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	0	1	1	0	0
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Cylinder Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End of Track							
Byte 7	Gap Length							
Byte 8	Data Length							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

READ A TRACK

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	MF	SK	0	0	0	1	0
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Cylinder Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End of Track							
Byte 7	Gap Length							
Byte 8	Data Length							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

READ ID

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	MF	0	0	1	0	1	0
Byte 1	x	x	x	x	x	HD	US1	US0

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

WRITE DATA

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	0	0	0	1	1	1
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Cylinder Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End of Track							
Byte 7	Gap Length							
Byte 8	Data Length							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

WRITE DELETED DATA

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	0	0	0	1	0	1
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Cylinder Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End of Track							
Byte 7	Gap Length							
Byte 8	Data Length							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

FORMAT A TRACK

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	MF	0	0	1	1	0	0
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Number of Data Bytes in Sector							
Byte 3	Sectors per Cylinder							
Byte 4	Gap Length							
Byte 5	Data							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

SCAN EQUAL

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	1	0	0	0	1
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Cylinder Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End of Track							
Byte 7	Gap Length							
Byte 8	Scan Test							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

SCAN LOW OR EQUAL

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	1	1	0	0	1
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Cylinder Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End of Track							
Byte 7	Gap Length							
Byte 8	Scan Test							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

SCAN HIGH OR EQUAL

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	1	1	1	0	1
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Cylinder Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End of Track							
Byte 7	Gap Length							
Byte 8	Scan Test							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

RECALIBRATE

Command Phase
(This command has no result phase.)

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	1	1
Byte 1	x	x	x	x	x	0	US1	US0

SENSE INTERRUPT STATUS

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	0	0

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Present Cylinder Number							

SPECIFY

Command Phase
(This command has no result phase.)

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	1	1
Byte 1	SRT				HUT			
Byte 2	HLT							ND

SENSE DRIVE STATUS

Command phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	1	0
Byte 1	x	x	x	x	x	HD	US1	US0

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status 3 Register							

SEEK

Command Phase
(This command has no result phase.)

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	1	1
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	New Cylinder Number for Seek							

INVALID

Result Phase

The following status byte is returned to the microprocessor when an invalid command is received.

	7	6	5	4	3	2	1	0
Byte 0	Status 0 Register							

Electrical Characteristics

Absolute Maximum Ratings*

Parameter	Min	Max	Unit
Operating Temperature	-10°	+70°	C
Storage Temperature	-55°	+150°	C
All Output Voltages	-0.5	+7	Volts
All Input Voltages	-0.5	+7	Volts
Supply Voltage Vcc	-0.5	+7	Volts
Power Dissipation		1	Watt

Note: Stress above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC Characteristics

Ta = 0° C to +70° C; VCC = +5 V +/- 5% unless otherwise specified

SA0-9, AEN, RESET, /IOW, /IOR, /DACK, T/C, /CS

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}		0.8	V	
Input High Voltage	V_{IH}	2.0		V	
Input Leakage Current	I_{LIH}		1.0	uA	V_{IN} = VCC
Input Leakage Current	I_{LIL}		1.0	uA	V_{IN} = 0V

SD0-7, DRQ, IRQ

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}		0.8	V	
Input High Voltage	V_{IH}	2.0		V	
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4	Vcc	V	I_{OH} = -16 mA
Leakage Current	I_{LOB}	-10	10	uA	

/WP, /INDEX, /TRK0, /RDATA, /DSKCHG

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Leakage Current	I_{IL}	-64	-250	uA	
Negative-going Threshold	V_{t-}	0.2VCC		V	
Positive-going Threshold	V_{t+}		0.8VCC	V	
Input Hysteresis	V_H	1.0		V	

/MO0-3, /DS0-3, /RWC, /DIR, /STEP, /WD, /WE, /HEAD

Parameter	Symbol	Min	Max	Unit	Test Conditions
Output Low Voltage	V_{OLD}		0.4	V	I_{OL}=40mA
Output High Leakage	I_{LOH}		10	uA	V_{OUT} = Vcc

ADDSEL

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}		0.8	V	
Input High Voltage	V_{IH}	2.0		V	
Input Low Current	I_{IL}	-64	-250	uA	

XTAL1

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}		1.0	V	
Input High Voltage	V_{IH}	4.0		V	
Input Low Current	I_{IL}		-1.0	uA	
Input high Current	I_{IH}		1.0	uA	

XTAL2

Parameter	Symbol	Min	Max	Unit	Test Conditions
Output Low Voltage	V_{OL}		0.4	V	I_{OL}=0.28 mA
Output High Voltage	V_{OH}	2.4			I_{OH}=-1.4 mA

AC Characteristics

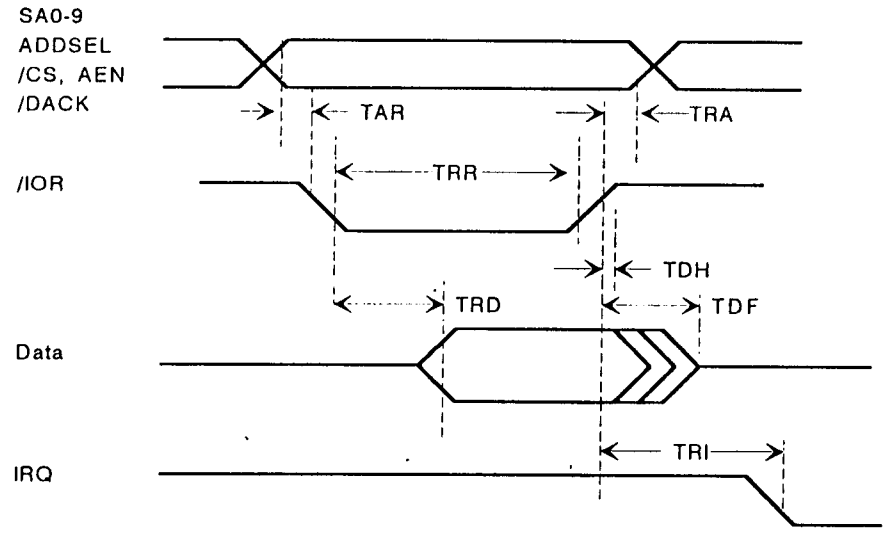
Data rate = 500/250 Kb/sec

Parameter	Symbol	Min	Typ(2)	Max	Unit	Test Conditions
SA9-0, ADDSEL, AEN, /DACK, /CS setup time to /IOR falling edge	TAR	25			ns	
SA9-0, ADDSEL, AEN, /DACK, /CS hold time from /IOR rissing edge	TRA	0			ns	
/IOR width	TRR	80			ns	
Data access time from /IOR falling edge	TRD			80	ns	CL = 100pf
Data hold from /IOR rising edge	TDH	10			ns	CL = 100pf
SD to float from /IOR rising edge	TDF	10		50	ns	CL = 100pf
IRQ delay from /IOR rising edge	TRI			360/675	ns	
SA9-0, ADDSEL, AEN, /DACK, /CS setup time to /IOW falling edge	TAW	25			ns	
SA9-0, ADDSEL, AEN, /DACK, /CS hold time from /IOW rising edge	TWA	0			ns	
/IOW width	TWW	60			ns	
Data setup time to /IOW rising edge	TDW	60			ns	
Data hold time from /IOW rising edge	TWD	0			ns	
IRQ delay from /IOW rising edge	TWI			360/675	ns	

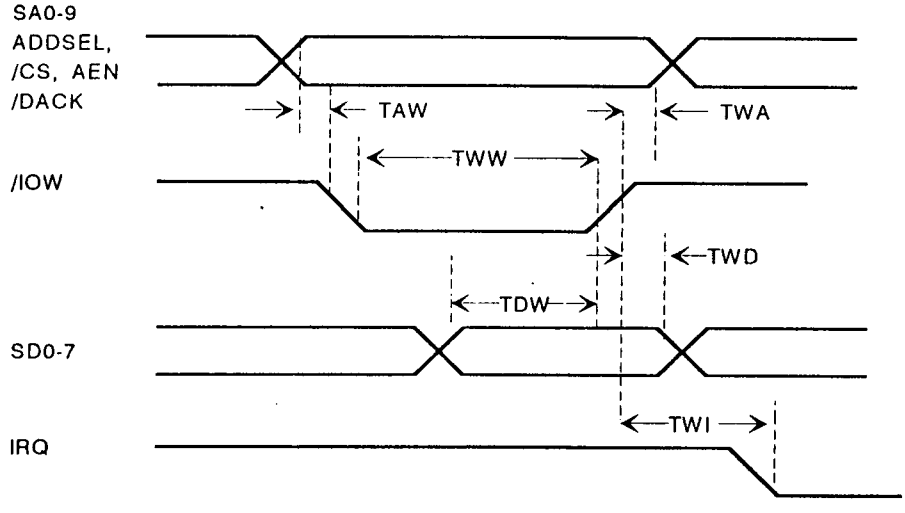
Parameter	Symbol	Min	Typ(2)	Max	Unit	Test Conditions
DRQ cycle time	TMCY	27			us	
DRQ delay time from /DACK	TAM			50	ns	
DRQ to /DACK delay falling edge	TMA	0			ns	
/DACK width	TAA	260/510			ns	
/IOR delay from /DRQ	TMR	0			ns	
/IOW delay from /DRQ	TMW	0			ns	
/IOW or /IOR response time from DRQ	TMRW			12/24	us	
TC Width	TTC	135/260			ns	
RESET Width	TRST	1.8/3.5			us	
/INDEX Width	TIDX	0.5/1.0			us	
/DIR setup time to /STEP	TDST	1.0/2.0			us	
/DIR hold time from /STEP	TSTD	24/48.0			us	
/STEP pulse width	TSTP	6.8/13.8	7/14	7.2/14.2	us	
/STEP cycle time	TSC	(3)	(3)	(3)	us	
/WD pulse width	TWDD	100	125	150	ns	
Write Precompensation time		100	125	150	ns	

(2) Typical values for T = 25° C and nominal supply voltage.
(3) Programmable from 2ms through 32ms in 2ms increments.

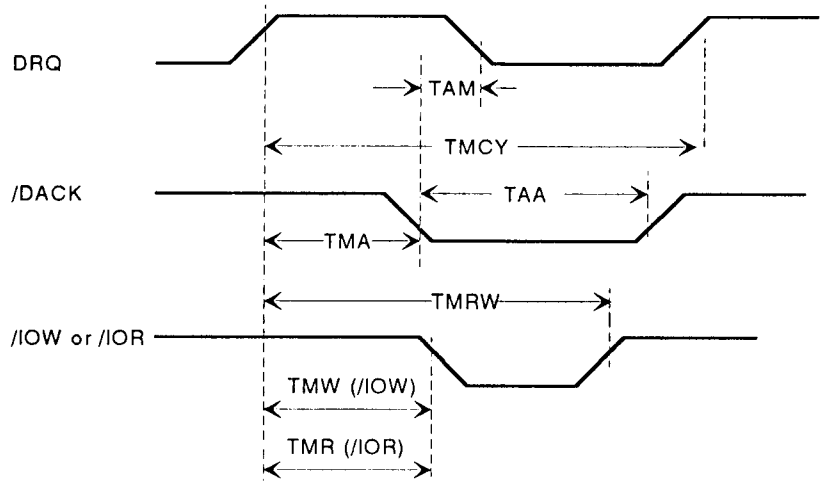
Processor Read Operation



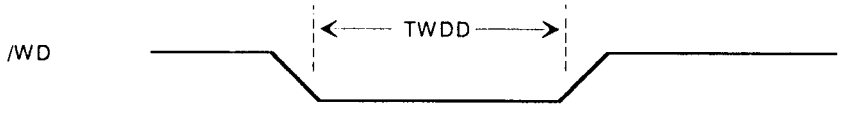
Processor Write Operation



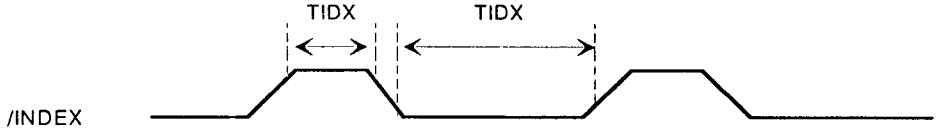
DMA Operation



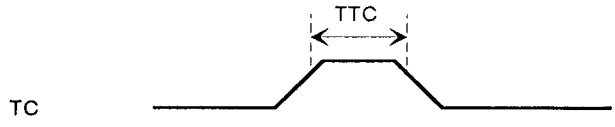
Write Data



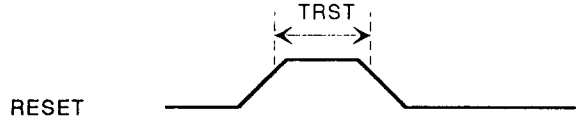
Index



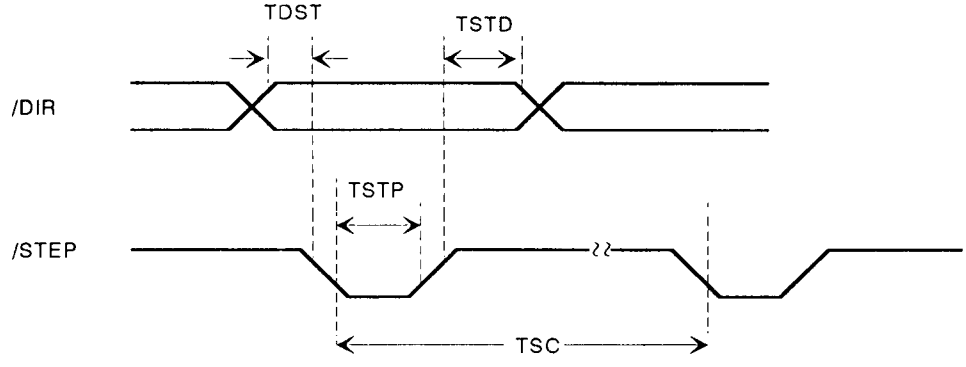
Terminal Count



Reset



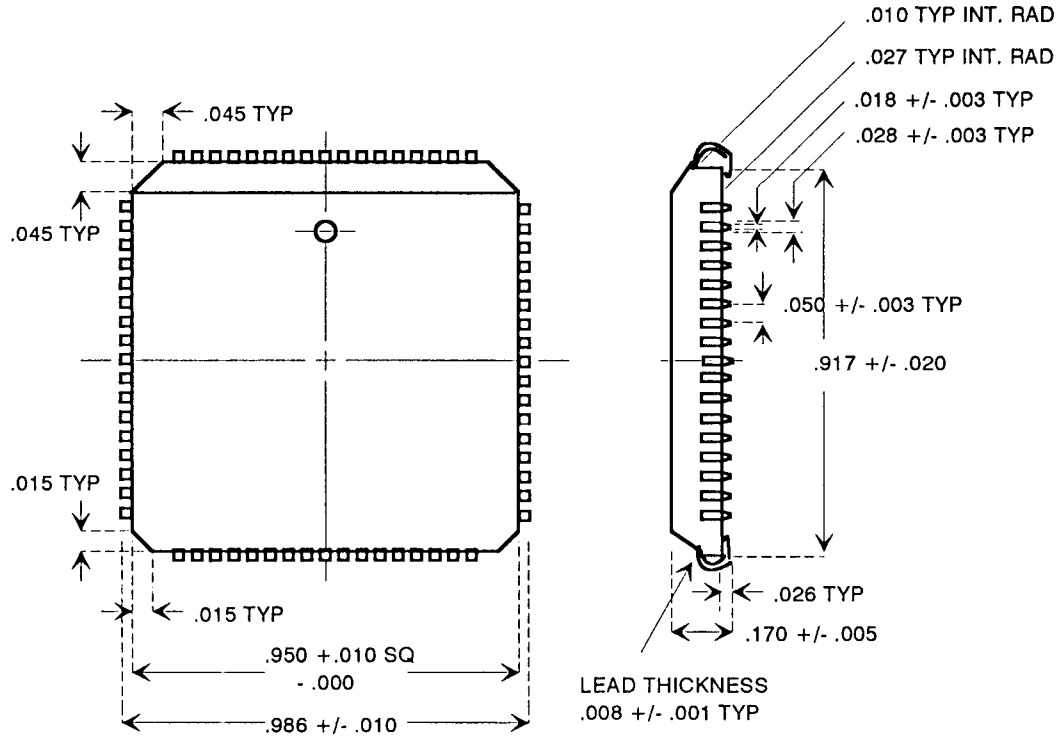
Drive Seek Operation



Production Package Specification

Package: 68-pin PLCC
Unit: inches

Chip: ACC 3203



ACC
Microelectronics Corporation

3295 Scott Blvd.
Santa Clara, CA 95054
Phone: 408-980-0622 FAX: 408-980-0626

P/N 520018 Rev. 1 10/20/88