ACC 85000A
Model 50/60 Chip Set

The ACC 85000 is a four-device CMOS chip set designed to provide OEMs with 100% PS/2* Model 50/60 compatibility and greater flexibility to build a distinctive high performance Model 50/60 compatible system. Only 29 external TTLs are required along with this highly integrated chip set to build a Model 50/60 compatible turbo system.

Features

- 100% hardware and software compatible with IBM* PS/2 Model 50/60
- 100% compatible with IBM PS/2 Model 50/60 Micro Channel* implementation
- Supports 10, 12.5, and 16 MHz 80286 and 80386SX processors
- DMA and Micro Channel operate at the ultimate Micro Channel bus performance
- Software switching for turbo speed
- Compatible with commercially available VGA chips
- Supports up to 16 MB of on-board DRAM
- Supports 256K x 1, 256K x 4, 1M x 1, and 1M x 4 DRAMs
- Supports shadow RAM
- Supports EMS 4.0

The ACC 85000 chip set includes the ACC 5000 DMA and Micro Channel Controller, the ACC 5100 Peripheral Interface Controller, the ACC 5200 Data Buffer Logic and the ACC 5300 Memory Controller and Buffers.

The ACC 5000 DMA and Micro Channel Controller integrates DMA control and Micro Channel control logic into a single chip.

The ACC 5100 integrates a level-sensitive interrupt sharing controller, Programmable Option Select Logic, an 8254 compatible timer and glue logic.

The ACC 5200 integrates data buffers and latches.

The ACC 5300 integrates the memory controller, and memory buffers and latches.

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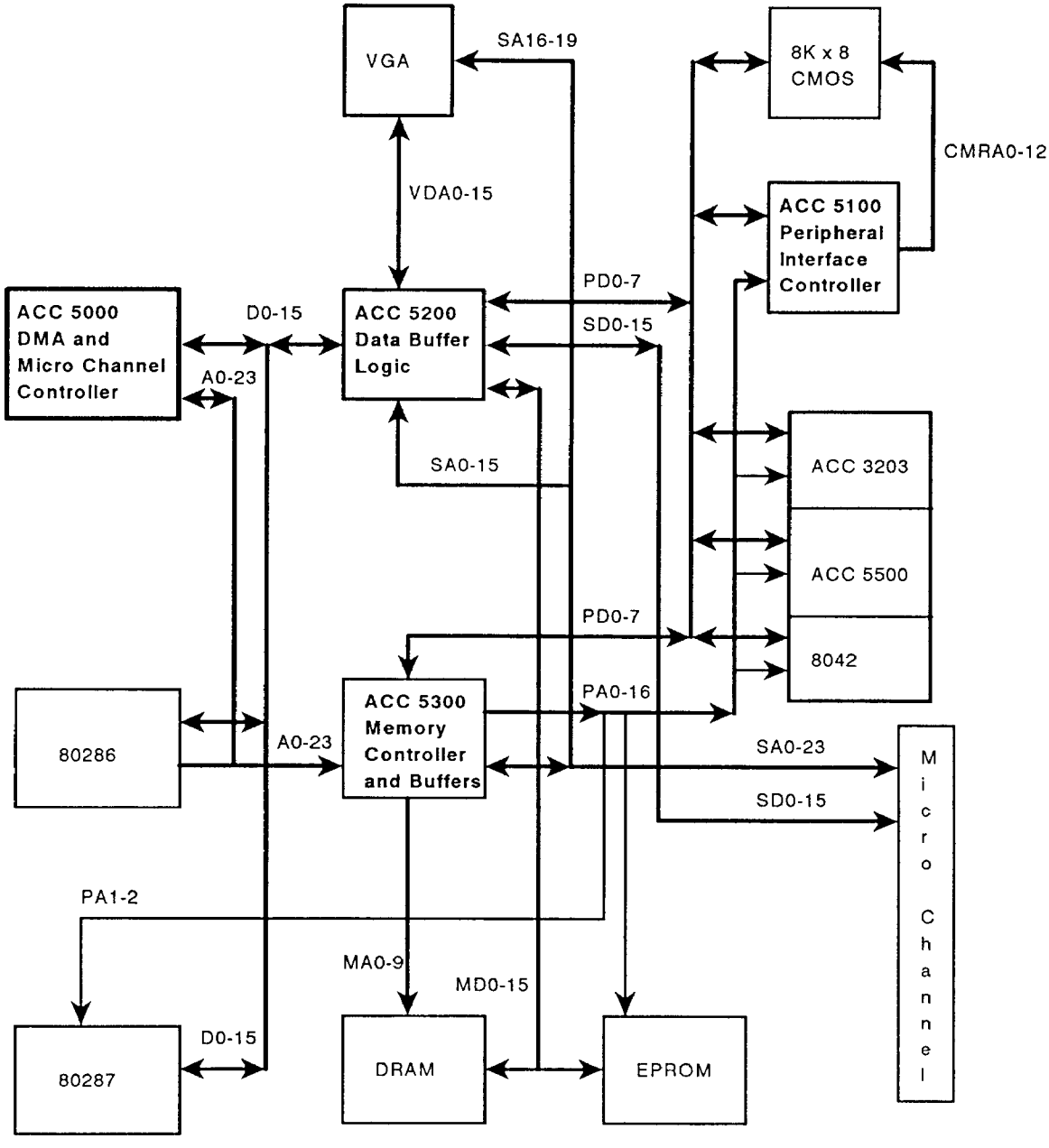
ACC 85000 System Block Diagram



ACC 5000
DMA & Micro Channel Controller

The ACC 5000 is a high performance CMOS device that integrates the DMA control and Micro Channel* control logic of an IBM PS/2* Model 50/60 into a single 144-pin flat pack. Both the DMA and Micro Channel operate at IBM standard clock rate to reach 100% IBM compatibility. The ACC 5000 supports turbo speed switch making the CPU speed switchable between turbo mode (12.5/16 MHz) and normal mode (10 MHz) on the fly.

Features

- 100% IBM PS/2 compatible Model 50/60 DMA controller implementation
- 100% IBM PS/2 compatible Model 50/60 Micro Channel implementation
- Supports 10, 12.5, and 16 MHz 80286 and 80386SX processors
- 200 ns cycle for DMA and Micro Channel provides the ultimate Micro Channel BUS performance
- Turbo speed change accomplished through software switching on the fly
- Equivalent performance of two 8237 DMA controllers with support for Extended mode
- 16 MB memory address capability and 64 KB I/O address capability
- Eight independent DMA channels for extended mode
- Executes central arbitration control point functions
- Regulates and controls the duration of arbitration cycles
- Monitors the Micro Channel for time-out conditions
- Clock and reset logic
- 1.5 micron high performance CMOS technology
- 144-pin PFP package

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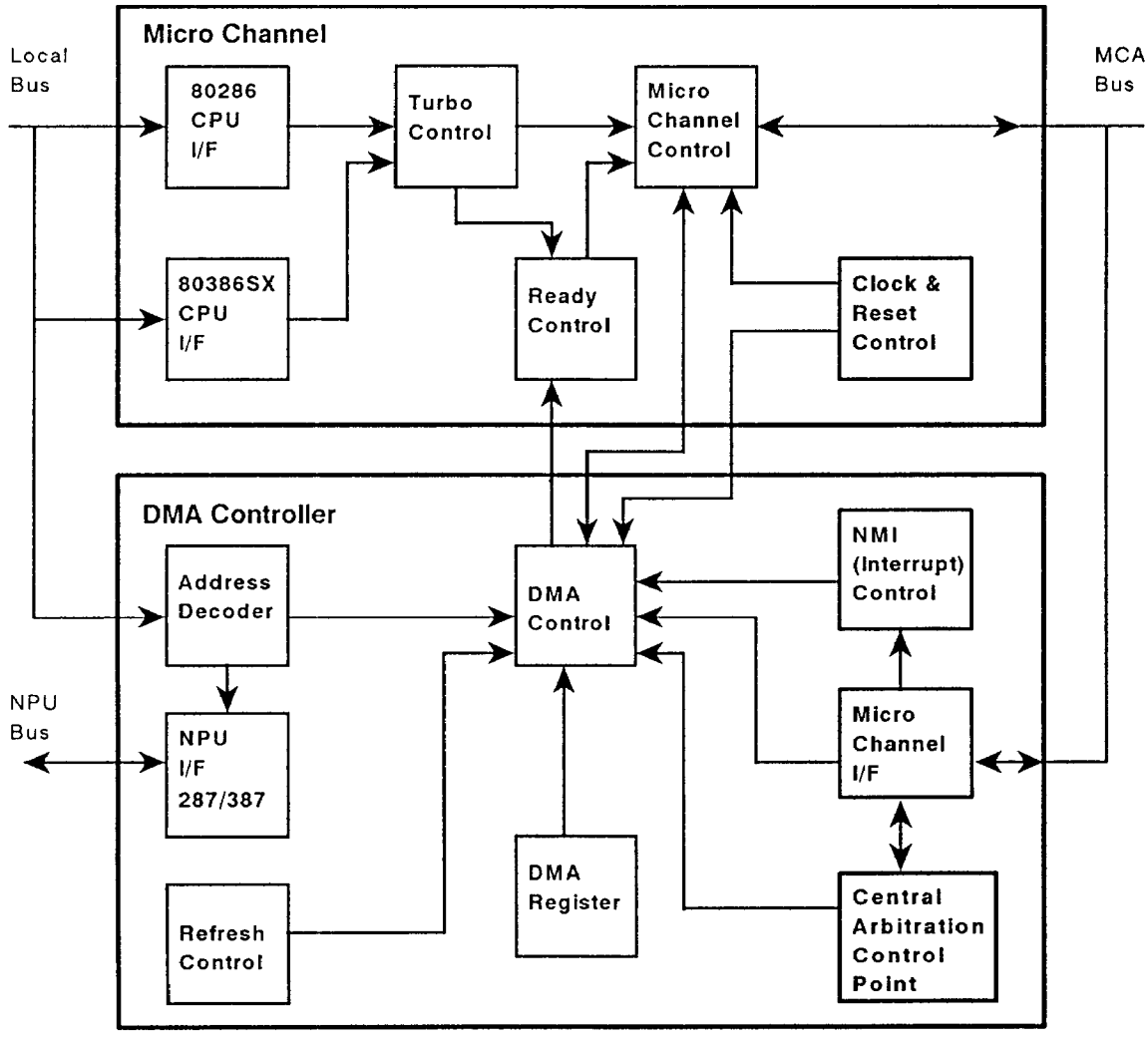
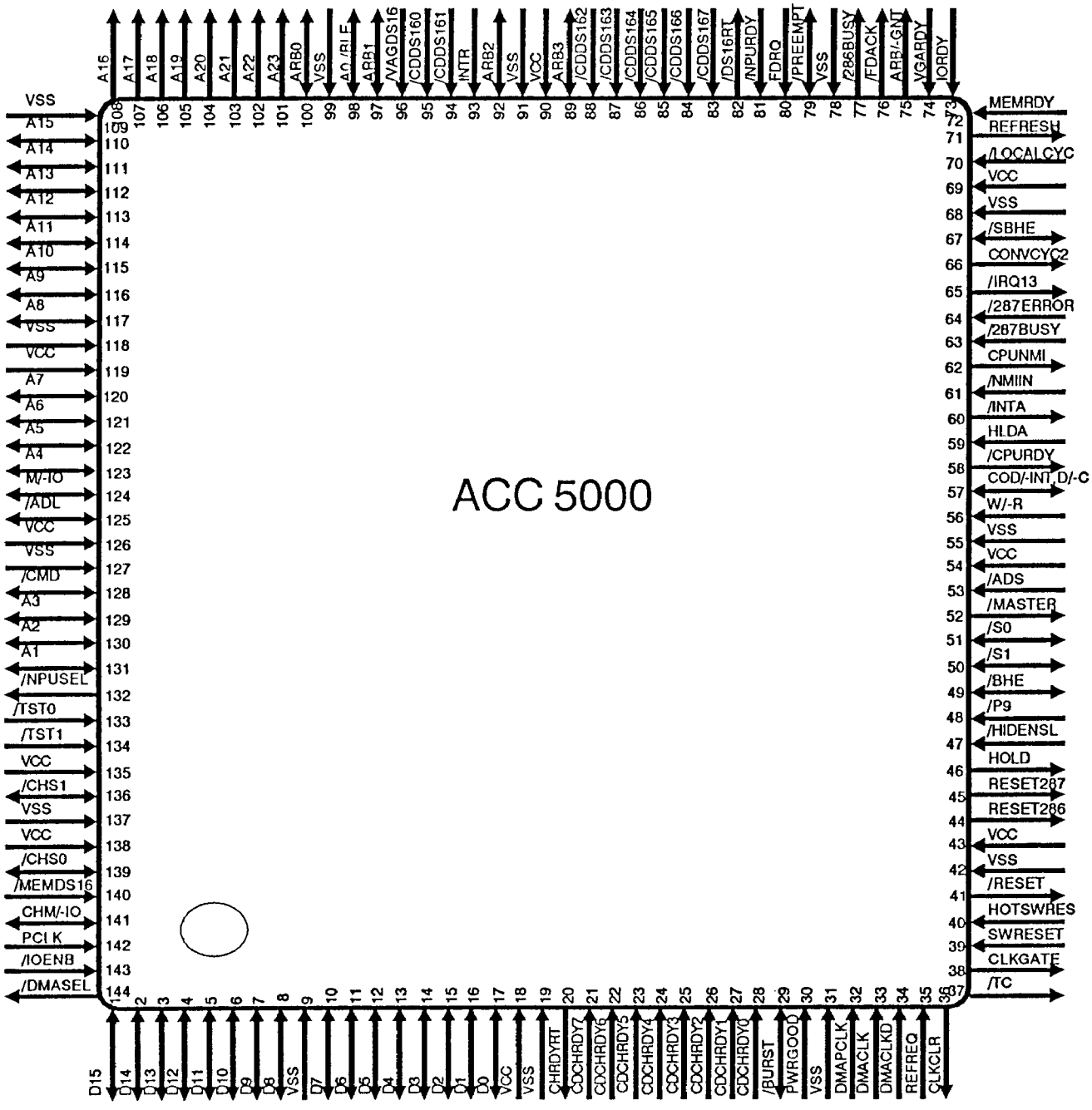
ACC 5000 System Block Diagram



Pin Diagram


ACC 5000
VSS
A15
A14
A13
A12
A11
A10
A9
A8
VSS
VCC
A7
A6
A5
A4
M/-IO
/ADL
VCC
VSS
/CMD
A3
A2
A1
/NPUSEL
/TST0
/TST1
VCC
/CHS1
VSS
VCC
/CHS0
/MEMDS16
CHM/-IO
PCLK
/IOENB
/DMASEL
A16
A17
A18
A19
A20
A21
A22
A23
ARB0
VSS
A0 /BLE
ARB1
/VAGDS16
/CDDS160
/CDDS161
INTR
ARB2
VSS
VCC
ARB3
/CDDS162
/CDDS163
/CDDS164
/CDDS165
/CDDS166
/CDDS167
/DS16RT
/NPURDY
FDRQ
/PREEMPT
VSS
/286BUSY
/FDACK
ARB/-GNT
VGARDY
IORDY
MEMRDY
REFRESH
/LOCALCYC
VCC
VSS
/SBHE
CONVCYC2
/IRQ13
/287ERROR
/287BUSY
CPUNMI
/NMIIN
/INTA
HLDA
/CPURDY
COD/-INT
D/-C
W/-R
VSS
VCC
/ADS
/MASTER
/S0
/S1
/BHE
/P9
/HIDENSL
HOLD
RESET287
RESET286
VCC
VSS
/RESET
HOTSWRES
SWRESET
CLKGATE
/TC
D15
D14
D13
D12
D11
D10
D9
D8
VSS
D7
D6
D5
D4
D3
D2
D1
D0
VCC
VSS
CHRDYRT
CDCHRDY7
CDCHRDY6
CDCHRDY5
CDCHRDY4
CDCHRDY3
CDCHRDY2
CDCHRDY1
CDCHRDY0
/BURST
PWRGOOD
VSS
DMAPCLK
DMACLK
DMACLKD
REFREQ
CLKCLR

Pin Descriptions

Symbol	Pin	I/O	Pin Description
D15	1	I/O	CPU/DMA data bus.
D14	2		
D13	3		
D12	4		
D11	5		
D10	6		
D9	7		
D8	8		
D7	10		
D6	11		
D5	12		
D4	13		
D3	14		
D2	15		
D1	16		
D0	17		
CHRDYRT	20	O	Channel ready return signal to bus.
CDCHRDY7	21	I	Channel ready signal from adapter slot.
CDCHRDY6	22		
CDCHRDY5	23		
CDCHRDY4	24		
CDCHRDY3	25		
CDCHRDY2	26		
CDCHRDY1	27		
CDCHRDY0	28		
/BURST	29	I/O	Signal from Micro Channel, indicates that the present master will make multiple transfers. (24 ma sink)
PWRGOOD	30	I	Power good indication from power supply. Generates power-up reset.
DMAPCLK	32	I	DMA version of PCLK, constant 10 MHz. (50% duty cycle)
DMACLK	33	I	20MHz clock input for DMA and Micro Channel. (40-50% duty cycle)
DMACLKD	34	I	Delayed 20MHz clock input for DMA and Micro Channel, generates internal non-overlapping clocks.
REFREQ	35	I	Refresh request from ACC 5100.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
CLKCLR	36	O	Signal clears external CPU clock divider.
/TC	37	O	Signal indicating the last DMA transfer for the present DMA channel (terminal count). (24 ma sink)
CLKGATE	38	O	Signal gates DMACLK into CPU clock when Micro Channel is accessed.
SWRESET	39	I	CPU software reset signal from 8042 chip.
HOTSWRES	40	I	Alternate "hot" CPU reset from ACC 5100 (faster than SWRESET).
/RESET	41	O	Reset signal for all motherboard logic except 80286 and 80287.
RESET286	44	O	Reset for 80286.
HOLD	45	O	Reset for 80287.
RESET287	46	O	CPU Hold request signal.
/HIDENSL	47	I	High density floppy disk select.
/P9	48	I	Input selects 80386SX processor when pulled low, otherwise 286 is selected by default because of built-in pullup resistor.
/BHE	49	I/O	Enable for high byte.
/S1 /S0	50 51	I/O	Cycle status signals for CPU/DMA. For the 80386SX processor, these signals are derived from other signals by the ACC 5000.
/MASTER	52	O	Signal indicates that another master (besides CPU or DMA) has control of the Micro Channel.
/ADS	53	I	Address strobe from 80386SX processor.
W/-R	56	I	80386SX processor write/read signal.
COD/-INTA	57	I/O	For 286: Additional status signal.
D/-C	57	I/O	For 80386SX processor: Additional status signal.
/CPURDY	58	O	CPU ready signal.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
HLDA	59	I	Hold acknowledge signal from CPU.
/INTA	60	O	Interrupt Acknowledge signal for ACC 5100.
/NMIIN	61	I	Non-maskable interrupt from ACC 5100.
CPUNMI	62	O	Non-maskable interrupt to CPU.
/287BUSY	63	I	Busy signal from numeric processor.
/287ERROR	64	I	Error signal from numeric processor.
/IRQ13	65	O	Numeric processor interrupt to ACC 5100.
CONVCYC2	66	O	Signal indicates to ACC 5200 and ACC 5300 that the second part of a byte/word conversion cycle is in progess.
/SBHE	67	I/O	Micro Channel byte high enable. (24 ma sink)
/LOCALCYC	70	I	Signal from ACC 5300 indicates that the current cycle is local and does not involve the Micro Channel.
REFRESH	71	O	Signals the Micro Channel that this is a memory refresh cycle. (24 ma sink)
MEMRDY	72	I	Ready signal from ACC 5300 (for DRAM or EPROM).
IORDY	73	I	Ready signal from ACC 5100 (for on-board I/O).
VGARDY	74	I	Ready signal from VGA subsystem.
ARB/-GNT	75	O	Signal indicates Arbitrate vs Bus Grant state on the Micro Channel. (24 ma sink)
/FDACK	76	O	DMA acknowledge to ACC 3203 FDC.
/286BUSY	77	O	Numeric processor busy to CPU.
/PREEMPT	79	I/O	Requests the Micro Channel. (24 ma sink)
FDRQ	80	I	DMA request from ACC 3203 FDC.
/NPURDY	81	I	Ready input from 80376SX NPU (P9 only). Pullup resister is built in.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/DS16RT	82	O	Data size 16 return to bus. (24 ma sink)
/CDDS16(7) /CDDS16(6) /CDDS16(5) /CDDS16(4) /CDDS16(3) /CDDS16(2) /CDDS16(1) /CDDS16(0)	83 84 85 86 87 88 94 95	I	Input signal from each of 8 adapter slots. Indicates that the adapter allows 16-bit I/O.
ARB3 ARB2 ARB1 ARB0	89 92 97 100	I/O	Micro Channel arbitration priority level signal. (24 ma sink)
INTR	93	I	CPU interrupt signal from the ACC 5100.
/VGADS16	96	I	Signal from VGA subsystem for 16-bit I/O.
A0	98	I/O	For 286: CPU/DMA address Bit 0.
/BLE	98	I/O	For 80386SXX processor: Enable for lower byte (pin works the same way, only the name is changed).
M/-IO	124	I/O	Signal indicates Memory or I/O operation.
/ADL	125	I/O	Micro Channel Address Latch signal. (24 ma sink)
/CMD	128	I/O	Micro Channel Command Strobe. (24 ma sink)
/NPUSEL	132	O	Chip select for 80287 NPU.
/CHS1 /CHS0	136 139	I/O	MicroChannel /S1 signal. (24 ma sink)
/MEMDS16	140	I	Input from ACC 5300. Indicates that the on-board memory selected can handle 16-bit transfers.
CHM/-IO	141	I/O	Micro Channel version of M/-IO. (24 ma sink)
PCLK	142	I	Peripheral clock, half speed of CPUCLK.
/IOENB	143	I	Qualifies I/O decoding inside the ACC 5000.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/DMASEL	144	O	Selects DMA or NPU registers. When low, indicates that the DMA is accessed by the CPU.
A23	101	O	CPU/DMA address bus.
A22	102		
A21	103		
A20	104		
A19	105		
A18	106		
A17	107		
A16	108		
A15	110		
A14	111		
A13	112		
A12	113		
A11	114		
A10	115		
A9	116		
A8	117		
A7	120		
A6	121		
A5	122		
A4	123		
A3	129		
A2	130		
A1	131		
/TST0 /TST1	133 134	I	Reserved. Tied to pullup register in system. **Test Pin Input**
VCC	18, 43, 54, 69, 90 119, 126, 135, 138		+5 volt supply
VSS	9, 19, 31, 42, 55 68, 78, 91, 99, 109, 118, 127, 137		Ground

TST0	TST1	Function
0	0	reserved
0	1	MCA Mode
1	0	DMA Mode
1	1	Normal Mode

Functional Description

CPU Interface (80286/80386SX)

The Micro Channel Controller subsystem converts control signals from either the 80286 or 80386SX CPU to signals compatible with the Micro Channel bus. In the case of the 80386SX CPU, an extra translation takes place. The 80386SX CPU is assumed to be pipelined (/NA connected to ground) and its control lines are decoded to create /S1 and /S0 signals which imitate those of the 80286. See Table 1 below.

TURBO Control

The ACC 5000 chip can switch dynamically between two operating speeds, 10Mhz (for IBM compatibility) and a selected higher (turbo) speed for faster CPU DRAM accesses. The ACC 85000 chip set is characterized for four turbo speeds: 10 Mhz, 12.5 Mhz, 16 Mhz and 20 Mhz. However, with a properly designed external clock generator, any speed between 10Mhz and 20Mhz can be used.

All programmable options of the ACC 85000 chip set are controlled by software accesses to configuration registers which are present inside individual chips. All chips in the ACC 85000 chip set have these configuration registers except for the ACC 5200.

Registers are accessed through I/O ports 22H and 23H. The procedure is to write a register number to 22H, then read or write the actual register data at port 23H. Address space for 64 configuration registers has been provided, with the addresses allocated between the chips as indicated below.

Chip	Register numbers allocated
ACC 5000	00H - 0FH
ACC 5100	10H - 1FH
ACC 5300	20H - 3FH

Not all of the allocated registers are actually used. Register 00H is the only one in the ACC 5000. It is used by the Turbo and Ready Control logic blocks.

Table 1 80386SX to 80286 Conversion

(80386SX inputs) D/-C	M/-IO	W/-R	Cycle Type	(80286 equivalent status) /S1	/S0
0	0	0	Interrupt Acknowledge	0	0
0	0	1	Reserved		
0	1	0	Code Read	0	1
0	1	1	Halt/shutdown	0	0
1	0	0	I/O Read	0	1
1	0	1	I/O Write	1	0
1	1	0	Data Read	0	1
1	1	1	Data Write	1	0

NOTE: The 80386SX D/-C pin is connected to pin COD/-INTA on the ACC 5000.

The format for Register 00H is shown below.

00H

7 6 5 4 3	2	1	0
reserved	TEN MEG	ENB DEF	TURBO

All these bits are cleared to zero by a CPU reset.

TURBO

When TURBO is 0, the CPU runs at a fixed 10 Mhz frequency. All DRAM accesses are directed through the Micro Channel. In this mode, the system timing is 100% compatible with the IBM PS/2 Model 50/50Z/60.

When TURBO is 1, the CPU switches between 10 Mhz for Micro Channel cycles and a higher turbo rate for all cycles not involving the Micro Channel. In this mode, the CPU accesses the DRAM directly, bypassing the Micro Channel.

ENB DEF

This bit, when set, enables the "default" Micro Channel cycle used in the PS/2 Model 50Z. When ENB DEF is zero, one wait state is inserted into all Micro Channel cycles for 100% compatibility with the IBM PS/2 Model 50/60.

TEN MEG

Turbo mode usually indicates switching to a higher CPU speed. However the turbo mode in the ACC 85000 chip set is advantageous even for a 10 Mhz turbo speed. At 10 MHz, although the CPU clock is the same speed, the paged and page/ interleaved DRAM access modes can be used in the ACC 5300. With these modes, the system can use slower DRAMS for near zero wait state performance. When turbo mode is selected for a CPU speed of 10Mhz, the TEN MEG bit must be set to one so the ACC 5000 can optimize its turbo control logic for that speed. TEN MEG has no effect when TURBO is zero.

When the ACC 5000 is in turbo mode, the signal /LOCALCYC is checked at the beginning of each CPU cycle (as indicated by /S1 and /S0) to determine if the Micro Channel is required. If /LOCALCYC is high, the clock is switched down to 10 Mhz, and a Micro Channel cycle is initiated. At the end of the cycle, the clock is switched back to turbo speed, as long as the TURBO bit is high.

This Turbo Control logic requires that both the normal and turbo clocks be synchronous to each other. Because of the stringent speed and accuracy requirements of this clock switching, the actual clock generator is implemented outside of the ACC 5000 in TTL circuitry. The ACC 5000 provides the control signals for the clock generator. ACC has designed TTL clock generators for 10Mhz, 12.5 Mhz, 16 Mhz and 20 Mhz CPUs. These clock generators require, in the worst case, two 16L8D PAL chips. If another CPU speed is required, contact ACC for design assistance with this clock generator.

Micro Channel Control/Ready Control

The Micro Channel Control/Ready Control logic generates IBM Micro Channel compatible strobes using status signals from the CPU. All Micro Channel output signals can sink 24ma for direct connection to the bus. All I/O operations on the motherboard are initiated by the Micro Channel, except for the 80387SX NPU for 80386SX systems. This includes CPU accesses to the DMA slave registers inside the ACC 5000.

One Micro Channel cycle is usually generated for each CPU cycle. However, there is one case in which a CPU cycle can cause two Micro Channel cycles. This occurs when the CPU accesses 16 bits of data from an 8-bit peripheral, or 8-bit memory. The Micro Channel Control block detects this condition and handles it by making two separate Micro Channel cycles while the CPU waits. In this case, the signal /CONVCYC2 indicates to the ACC 5200 and ACC 5300 that the second of the two cycles is taking place.

CPU Ready control logic is built into the Micro Channel bus state machine. /CPURDY becomes active only after all incoming ready signals are high, including CDCHRDY(0) through CDCHRDY(7), VGARDY, DMARDY, MEMRDY and IORDY. DMARDY is generated inside the ACC 5000 by the DMA subsystem. During non-Micro Channel cycles, /CPURDY is generated from MEMRDY and /NPURDY and INTRDY. INTRDY is generated internally in response to Interrupt Acknowledge, Halt and Shutdown cycles.

Interrupt and Reset Control

The ACC 5000 receives three reset inputs: PWRGOOD, SWRESET and HOTSWRES. PWRGOOD is the power good signal from the power supply. When PWRGOOD is low, both /RESET and RESET286 signals are activated for a system power-up reset.

RESET286 is valid for at least 16 CPUCLK cycles and is synchronized with respect to CPUCLK. Both edges of RESET286 are timed to set the 80286 or 80386SX CPU's internal PCLK to a known state.

/RESET performs system reset for all other chips on the motherboard, except the 80287 or 80387SX NPU. The NPU interface block controls this.

SWRESET and HOTSWRES are software reset signals for the CPU only. SWRESET is generated by the 8042 keyboard controller. HOTSWRES is an alternate CPU reset from the ACC 5100 which is several microseconds faster than SWRESET.

Several special CPU conditions are monitored in this logic. In response to a "shutdown" cycle received from the CPU, a RESET286 pulse is generated. "Halt" cycles are ignored, except for generating /CPURDY, and an "interrupt acknowledge" cycle results in a 200ns /INTA pulse.

DMA Control

The DMA controller is software compatible with two Intel 8237 chips and includes the extended functions added by IBM for the P/S 2 Model 50/60. There are eight programmable DMA channels along with the Micro Channel central arbitration control point (CACP). Six of the DMA channels are assigned fixed priorities, and two have programmable priorities. An 11-bit memory refresh counter, numeric processor interface and other logic are also included.

The DMA controller is a serial transfer device requiring a minimum of two cycles with a cycle time of 200 ns to transfer a word or byte for either I/O or memory access. During a DMA cycle, data is first read from a source device and held in a temporary register for writing to a destination device in the second cycle. DMA cycles on the Micro Channel can be extended in the same manner as CPU-initiated Micro Channel cycles. All DMA data transfers are between an I/O and a memory device. Memory to memory transfer is not supported.

Two DMA operating modes are supported, Compatible and Extended. Each of these modes is discussed in detail below.

Compatible Mode

In the 8237 compatible mode, DMA I/O devices are addressed only by priority number on the

Micro Channel, no I/O address is available. DMA channels 1-3 and 5-7 are assigned to a fixed priority level, according to their channel numbers. Channels 0 and 4 have programmable priority, using any level from 00H through 0EH. The user must be sure that the priorities assigned to these channels do not conflict with any other active DMA channels.

A local arbiter (typically on a Micro Channel Adapter card) uses a DMA channel by assuming its priority level on the Micro Channel. When the arbiter requires DMA, it must participate in an arbitration cycle and be granted control by the Micro Channel. If the DMA channel is enabled, the ACC 5000 assumes control and performs the DMA transfer after HLDA is received from the CPU. Priority levels for DMA channels 0 and 4 are controlled by two Arbus registers, which are written to by the CPU.

DMA Slave Cycles

The DMA controller is ordinarily in slave mode. In this mode, its internal registers can be accessed by the CPU. All registers in the DMA controller are 8 bits wide, no word transfers are possible.

DMA Master Cycles

In master mode, the DMA controller emulates the timing of an Intel 80286 processor consisting of three states similar to the 80286 processor: idle state, status state, and command state.

Idle State

The DMA controller is in idle state after reset or if no DMA requests are received.

Status State

When the DMA controller receives a DMA request from an unmasked channel, it asserts a HOLD signal to the CPU. After receiving an HLDA signal from the CPU, it starts a DMA cycle by asserting status lines to perform data transfer between memory and I/O devices. This can be a single data transfer, burst data transfer, or verify data transfer from memory depending on the setup of the mode register.

Command State

In the command state, the DMA controller either reads the data from the source device to the temporary holding register or transfers data to the target device.

In the compatible mode, channels 4-7 can perform either byte or word transfers. Channels 0-3 can only perform byte transfers. In the extended mode, all channels can be either byte or word data transfers depending on the mode register set-up. Each data transfer cycle is terminated by /CPURDY which is asserted by the Micro Channel controller.

The ACC 5000 also supports multiple-byte data transfers. To request this feature, the winning local arbiter must activate the /BURST signal. Once /BURST is activated, the data transfer continues until /BURST goes inactive, or until the transfer count goes to zero. The ACC 5000 indicates this condition to the local arbiter by activating the /TC (terminal count) signal.

Byte Pointer

An internal byte pointer allows 16 and 24-bit registers to be accessed through a byte wide port. After each byte has been accessed, the byte pointer is changed to allow the next byte to be accessed next time. The pointer always starts out pointing to the least significant byte, then to each more significant byte in order. Table 2 lists DMA registers.

Memory Address Register

The Memory Address Register consists of two parts, Base and Current. A CPU write to the

Memory Address Register updates both the base and current internal registers. The base register remains unchanged during the DMA operation, while the current register is updated to indicate the next Memory Address to be accessed. A CPU read always returns the contents of the current register.

If auto-initialize is enabled, the current register reloads at the end of process (EOP) with the value stored in the base register. EOP is generated when the DMA controller reaches a terminal count condition and the /TC signal is asserted.

Transfer Count Register

The Transfer Count Register also consists of Base and Current parts. A CPU write updates both base and current. The base register remains unchanged during the DMA operation, while the current register is decremented. This register determines the number of word or byte DMA transfers which take place. The number of transfers is one plus the register contents. Writing zero to the Transfer Count Register results in one DMA transfer. /TC is activated as the current Transfer Count Register goes from 0000H to FFFFH.

If auto-initialize is enabled, this register reloads at the end of process (EOP) with the value stored in the base register.

Current I/O Address Register

The Current I/O Address Register is initialized by the CPU in Extended mode only. The DMA I/O address is determined by this register while Bit 0 of the Extended Mode Register is 1. Otherwise, the DMA I/O address is always zero. Refer to Table 3 for an I/O map of DMA registers in compatible mode.

Table 2 DMA Registers

Register Name	Number of Registers	Size (bits)	Allocation
Memory address	8	24	1 per channel
I/O address	8	16	1 per channel
Transfer count	8	16	1 per channel
Temporary holding	1	16	All channels
Mask	2	4	1 per 4-channel group
Arbus	2	4	1 per 4-channel group
Mode	8	8	1 per channel
Status	2	8	1 per 4-channel group
Function	1	8	All channels
Refresh	1	11	Independent of DMA

Table 3 DMA Registers - I/O Map for Compatible Mode

I/O Address	Bits	Description	Byte Pointer
0000H	16	Ch 0 Memory address register (R/W)	Yes
0001H	16	Ch 0 Transfer count register (R/W)	Yes
0002H	16	Ch 1 Memory address register (R/W)	Yes
0003H	16	Ch 1 Transfer count register (R/W)	Yes
0004H	16	Ch 2 Memory address register (R/W)	Yes
0005H	16	Ch 2 Transfer count register (R/W)	Yes
0006H	16	Ch 3 Memory address register (R/W)	Yes
0007H	16	Ch 3 Transfer count register (R/W)	Yes
0008H	8	Ch 0-3 Status register	
000AH	3	Ch 0-3 Mask register (Set/Rst)(W)	
000BH	8	Ch 0-3 Mode register (W)	
000CH	-	Ch 0-3 Clear byte pointer (W)	
000DH	-	Ch 0-3 Master clear (W)	
000EH	-	Ch 0-3 Clear mask register (W)	
000FH	4	Ch 0-3 Write mask register (W)	
0081H	8	Ch 2 Page register (R/W)*	
0082H	8	Ch 3 Page register (R/W)*	
0083H	8	Ch 1 Page register (R/W)*	
0087H	8	Ch 0 Page register (R/W)*	
0089H	8	Ch 6 Page register (R/W)*	
008AH	8	Ch 7 Page register (R/W)*	
008BH	8	Ch 5 Page register (R/W)*	
008FH	8	Ch 4 Page register (R/W)*	
00C0H	16	Ch 4 Memory address register (R/W)	Yes
00C2H	16	Ch 4 Transfer count register (R/W)	Yes
00C4H	16	Ch 5 Memory address register (R/W)	Yes
00C6H	16	Ch 5 Transfer count register (R/W)	Yes
00C8H	16	Ch 6 Memory address register (R/W)	Yes
00CAH	16	Ch 6 Transfer count register (R/W)	Yes
00CCH	16	Ch 7 Memory address register (R/W)	Yes
00CEH	16	Ch 7 Transfer count register (R/W)	Yes
00D0H	8	Ch 4-7 Status register	
00D4H	3	Ch 4-7 Mask register (Set/Rst)(W)	
00D6H	8	Ch 4-7 Mode register (W)	
00D8H	-	Ch 4-7 Clear byte pointer (W)	
00DAH	-	Ch 4-7 Master clear (W)	
00DCH	-	Ch 4-7 Clear mask register	
00DEH	4	Ch 4-7 Write mask register (W)	

* Upper bytes of Memory Address Register

Mode register

The operating mode of the DMA controller can be programmed when HLDA is inactive through the Mode register. Mode register format is described below. The 8237 originally supported four operating modes. The ACC 5000 (identical to PS/2 Model 50/60) only supports "demand" mode. In this mode, the length of each burst of data transfers is controlled by the /BURST signal.

If /BURST is not activated, each burst is limited to a single byte or word transfer. If /BURST is activated during one transfer, another transfer occurs, until /BURST is deactivated, or the transfer count is expired. Once this takes place (EOP condition), /TC goes active and the channel is masked until the CPU reinitializes it.

End Conditions

In compatible mode, only the lower 16 bits of the Memory Address Register are updated while a DMA operation is taking place. An increment or decrement past a 64K page boundary results in address wraparound. Despite the wraparound, the DMA operation continues until the transfer count goes to FFFFH. Be sure that this does not result in altering unintended memory locations.

The Transfer count register decrements to FFFFH and stops. If the register is set to FFFFH initially, the counter decrements until it encounters FFFFH again.

If Auto-initialize is selected, the channel's associated mask register bit is NOT set at EOP. (EOP masks the channel.)

Tables 4 and 5 are the mode register formats for the Compatible and Extended modes respectively.

Table 4 Mode Register Format for Compatible Mode

7 6	5	4	3 2	1 0
0 0	DIR	AUTO	TYPE	CHAN

DIR Address direction
1 = decrement,
0 = increment

AUTO Auto-initialize feature 1 = on

TYPE Transfer type

0	0	Verify
0	1	Write Memory
1	0	Read Memory
1	1	Reserved

CHAN Channel Select

0	0	Channel 0 or 4
0	1	Channel 1 or 5
1	0	Channel 2 or 6
1	1	Channel 3 or 7

Table 5 Mode Register Format for Extended Mode

7	6	5	4	3	2	1	0
0	WID	0	0	W/R	DATA	0	I/O

WID Data width
1 = 16-bit transfer,
0 = 8-bit transfer

W/R Write/Read
1 = Write,
0 = Read

DATA Data/Verify
1 = Data transfer,
0 = Verify

I/O I/O Address
1 = programmable,
0 = I/O address 0000H

Arbus Registers

There are two Arbus registers, one for DMA channel 0 and one for DMA channel 4. These registers provide an arbitration level that is assigned by software. The lower 4 bits of each register contains the programmed arbitration level for its DMA channel. Level 0FH cannot be used. That level is dedicated to the system CPU.

Status Register

In Compatible mode, I/O address 0008H is reserved for channels 0-3 of the status register. I/O address 00D0H is reserved for channels 4-7 of the status register. In Extended mode, a status read provides the status of channels 0-3 and a second read provides the status of channels 4-7. The byte pointer is cleared when an access to the extended command register is made. Table 6 contains the format for the Status register. All the bits in the status register are set to zero during initialization.

Table 6 Status Register Format

7	6	5	4	3	2	1	0
CRQ				TC			
3	2	1	0	3	2	1	0

CRQ3	ChanRQ 3 or 7
CRQ2	ChanRQ 2 or 6
CRQ1	ChanRQ 1 or 5
CRQ0	ChanRQ 0 or 4
TC3	TC 3 or TC 7
TC2	TC 2 or TC 6
TC1	TC 1 or TC 5
TC0	TC 0 or TC 4

Mask Register

Each DMA channel has an associated mask bit. These bits are used to prevent external DMA requests from generating transfer cycles. Each mask bit can be programmed to be set or cleared. After a reset, all mask bits are set. A clear mask register command clears all mask bits.

In compatible mode, the I/O address for channels 0-3 is 000AH. For channels 4-7, the I/O address is 00D4H. Table 7 contains mask register formats.

Table 7 Mask Register Format

7	6	5	4	3	2	1 0
0	0	0	0	0	MASK	CHAN

MASK Mask bit
1 = set mask,
0 = clear mask

CHAN Channel Select

0	0	0 or 4
0	1	1 or 5
1	0	2 or 6
1	1	3 or 7

In Extended mode, each channel mask bit can be set by setting Bits 7-4 of the extended function register (0018H) to a hexadecimal value 9(H). It can also be reset by setting bits 7-4 of the extended function register to a hexadecimal value, A(H). Refer to the description of extended functions below for details.

Write Mask Register

The DMA controller can be masked by setting or resetting all the mask bits in the write mask register. The I/O address for channels 0-3 is 000FH. The I/O address for channels 4-7 is 00DEH. Table 8 contains the format for the Write mask register.

Table 8 Write Mask Register Format

7	6	5	4	3	2	1	0
0	0	0	0	CM3	CM2	CM1	CM0

CM3 Channel 3 or 7 Mask
CM2 Channel 2 or 6 Mask
CM1 Channel 1 or 5 Mask
CM0 Channel 0 or 4 Mask

Clear Mask Register

A write command issued to I/O address 000EH unmasks channels 0-3. A write command issued to I/O address 00DCH unmasks channels 4-7.

Clear Byte Pointer (Write only)

The Clear Byte Pointer command is usually executed before reading or writing to the address or word count registers. This command initializes the flip-flop to point to the low byte of the register.

In Compatible mode, I/O address 000CH is for channels 0-3, I/O address 00D8H is for channels 4-7. In Extended mode, the byte pointer is cleared each time the extended function register is accessed.

Extended Mode

The extended mode uses two byte locations, the Extended Function Register (EFR) (0018H) and the Extended Function Execute register (EFE) (001AH), to program all DMA and CACP registers.

Programming in extended mode requires first writing to the EFR, then possibly accessing one or more bytes in the EFE. Commands that do not require EFE access are called "Direct." Table 9 contains the format of the extended function register.

Central Arbitration Control Point (CACP)

The central arbitration control point controls and monitors the Micro Channel and CPU local bus arbitration functions. The bit settings in the Arbitration register (0090H) configure the CACP. Table 10 shows the format of the Arbitration register. This format is different for read and write. Default condition at power up is zero.

An arbitration cycle is defined as the transition of an ARB/-GNT signal from low to high and back low again. During ARB, all competing local arbiters can drive their priority level on ARB0-3 to determine the new bus owner. Refresh cycles are executed during ARB high time and extend the arbitration cycle. Arbitration cycles can be initiated by the following six internal conditions:

- Refresh Request
- Bus Timeout
- Competing Bus Master
- Competing DMA Slave
- NMI
- Bus Idle

A Bus Idle condition exists if a bus master or DMA slave is granted the bus, the transfer is complete, and none of the bus control signals (/S0, /S1, /CMD, /BURST) are active.

Bus cycles originating from a DMA slave, a channel bus master, or refresh requests, require that the CPU relinquish the local bus. The CACP accomplishes this task.

In a special case, if level 0 is detected on the ARB0-3 bus, arbitration can be truncated to a minimum of 100 ns.

Arbitration time can be extended by an NMI or Refresh cycle. NMI sets Bit 6 to one. To continue arbitration, the CPU must clear Bit 6 to zero. A Refresh cycle extends arbitration time by the length of the refresh cycle.

Table 9 Extended Address Register

7 6 5 4	3	2 1 0
FUNC	0	CHAN

FUNC	Extended function code
0 0 0 0	Read/Write I/O Address Register (16 bits)
0 0 0 1	Reserved
0 0 1 0	Write Memory Address Register (24 bits)
0 0 1 1	Read Memory Address Register (24 bits)
0 1 0 0	Write Transfer Count Register (16 bits)
0 1 0 1	Read Transfer Count Register (16 bits)
0 1 1 0	Read Status Register
0 1 1 1	Read/Write Extended Mode Register
1 0 0 0	Read/Write Arbus Register
1 0 0 1	Set Mask Register bit (Direct)
1 0 1 0	Clear Mask Register bit (Direct)
1 0 1 1	Reserved
1 1 0 0	Reserved
1 1 0 1	Master Clear (Direct)
1 1 1 0	Reserved
1 1 1 1	Reserved

CHAN Selected DMA Channel (0 - 7)

Table 10 Arbitration Register Format

Write format

7	6	5	4 3 2 1 0
CPU	MASK	EXT	0 0 0 0 0

Read format

7	6	5	4	3 2 1 0
CPU	MASK	TIMO	0	LEVEL

CPU Enable System CPU cycles during arbitration.

MASK Arbitration Mask, forces ARB/-GNT pin high. NMI interrupts set this bit.

EXT Enable extended 600ns arbitration cycle.

TIMO Bus timeout has occurred. Clearing MASK also clears this bit.

LEVEL Arbitration level on Micro Channel during most recent grant state.

The built-in 15 microsecond refresh timer is used to detect a Micro Channel bus timeout condition. If a refresh request is pending, and is still not serviced by the time another refresh is requested, a bus timeout condition occurs. because memory refresh has the highest priority on the Micro Channel, the existence of this bus timeout implies that a burst DMA cycle was taking place, and did not respond to the /PREEMPT signal.

When a bus timeout occurs, the CACP identifies the arbitration level of the device. It generates an NMI, initializes the DMA controller, Micro Channel control logic, and ready logic so the CPU can begin error recovery. After a bus timeout, DMA registers must be reprogrammed to restart any DMA operation. The bus timeout error condition exists until the CPU sets the MASK bit to 0.

The CACP acts as a local arbiter for the on-board floppy disk controller, converting its DMA requests into appropriate Micro Channel signals. The interface returns /DACK to the floppy disk controller after bus control is obtained.

Arbitration States

Arbitration control has six major states and two primary outputs. The outputs are the ARB/-GNT and CPU HOLD signals.

1. System/Dispatcher State

   In the System/Dispatcher State, the system CPU can execute error recovery programs, diagnostics or other system level programs. Normal applications do not usually execute when the arbiter is in this state.

2. CPU State

   In the CPU State, normal application programs are executed. Error recovery or supervisory programs can also be executed when the arbiter is in this state.

3. ARB State

   The ARB State is a transition state between a request for the CPU to yield the bus to a higher priority and the release. When the CPU releases the bus, a refresh cycle or bus master can use the bus.

4. Refresh State

   The Refresh State is a transition state when a single refresh cycle is generated. This state is relinquished when the cycle is finished.

5. Grant State

   Arbitration control is in Grant State when a bus master or DMA slave has won the bus.

6. Wait State

   The Wait State is a transition state for the DMA controller to finish both bus cycles of a transfer before relinquishing the bus.

The ACC 5000 generates a /PREEMPT signal under the following conditions:

1. When the floppy disk controller issues DRQ and the DMA controller channel 2 is not masked.
2. When a refresh request occurs.
3. When the ARB/-GNT line is low and NMI occurs while ARB0-3 not equal to 0FH. In this case, the MASK bit is set.

Rating Specifications

Absolute Maximum Ratings*

Parameter	Symbol	Min	Max	Units
Power supply voltage	VCC	-0.3	7.0	V
Power dissipation (@5.25 V)	Wd		TBD	W
Current (@5.25 V)	IDD		TBD	mA
DC Input voltage	VI	-0.3	7.0	V
Storage temperature	Tstg	-40	125	°C

* Exposing the device to stress above these can cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
DC supply voltage	VCC	4.75	5.25	V
Ambient temperature	Ta	0	70	°C

Capacitance Limits

TA = +25° C, VCC = 5 V

Parameter	Symbol	Min	Max	Unit	Test Condition
Input capacitance	CI		10	pF	fc = 1 MHz unmeasured pins at GND
I/O capacitance	CIO		15	pF	

DC Specifications

TA = 0° C to +70° C, VCC = +5 V +/- 5% ambient termperature

Group 1 INPUT

Pins CDCHRDY0-7, DMAPCLK, DMACLK, DMACLKD, REFREQ, SWRESET, HLDA, HOTSWRES, /HIDENSL, /NMIIN, /287BUSY, /287ERROR, /LOCALCYC, MEMRDY, IORDY, VGARDY, FDRQ, /NPURDY, /CDDS160-7, INTR, /VGADS16, /TST0, /TST1

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.25 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.25 V
Input low current	IIL	-10	10	uA	VIN = 0.0V
Input high current	IIH	-10	10	uA	VIN = VCC

Group 2 INPUT WITH PULLUP RESISTORS

Pins /P9, /ADS, W/-R

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.25 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.25 V
Input low current	IIL	-200	-10	uA	VIN = 0.0V
Input high current	IIH	-10	10	uA	VIN = VCC

Group 3 OUTPUT (3mA)

Pins RESET287, /IRQ13, /286BUSY, A16-20

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 3mA
Output high voltage	VOH	2.4		V	IOH = -3mA

Group 4 OUTPUT (6 mA)

Pins CLKCLR, CLKGATE, RESET286

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 6mA
Output high voltage	VOH	2.4		V	IOH = -6mA

Group 5 OUTPUT (9 mA)

Pins CONVCYC2, /FDACK

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 9mA
Output high voltage	VOH	2.4		V	IOH = -9mA

Group 6 OUTPUT (24 mA)

Pins /TC, HOLD, /SBHE, REFRESH, ARB/-GNT, /FDACK, /DS15RT, /ADL, CHM/-IO

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 24mA
Output high voltage	VOH	2.4		V	IOH = -24mA

Group 7 I/O (1.5 mA)

Pins PWRGOOD

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.25 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.25 V
Input low current	IIL	-10	10	uA	VIN = 0.0V
Input high current	IIH	-10	10	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 1.5mA
Output high voltage	VOH	2.4		V	IOH = -1.5mA

Group 8 I/O WITH PULLUP RESISTORS (3 mA)

Pins D0-15, CPUNMI, /PREEMPT, /DMASEL, A1-15, A21-23

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.25 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.25 V
Input low current	IIL	-200	-10	uA	VIN = 0.0V
Input high current	IIH	-10	10	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 3mA
Output high voltage	VOH	2.4		V	IOH = -3mA

Group 9 I/O WITH PULLUP RESISTORS (6 mA)

Pins /MASTER, M/-IO

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.25 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.25 V
Input low current	IIL	-200	-10	uA	VIN = 0.0V
Input high current	IIH	-10	10	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 6mA
Output high voltage	VOH	2.4		V	IOH = -6mA

Group 12 I/O WITH OPEN DRAIN OUTPUT (24 mA)

Pins /BURST, ARB0-3

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.25 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.25 V
Input low current	IIL	-200	-10	uA	VIN = 0.0V
Input high current	IIH	-10	10	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL =24mA
Output high voltage	VOH	n/a	n/a	V	n/a

Group 13 I/O WITH PULLUP RESISTORS (24 mA)

Pins /CMD, /CHS0, /CHS1

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.25 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.25 V
Input low current	IIL	-200	-10	uA	VIN = 0.0V
Input high current	IIH	-10	10	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL =24mA
Output high voltage	VOH	2.4		V	IOH = -24mA

ACC 5100
Peripheral Interface Controller

The ACC 5100 is a high performance CMOS device that integrates a level-sensitive interrupt sharing controller, Programmable Option Select Logic, an IBM compatible timer, and glue logic into a single 144-pin flat pack. The ACC 5100 is one of four devices in the ACC 85000 chip set designed to provide 100% PS/2* Model 50/60 compatibility and greater flexibility in building a distinctive high performance Model 50/60 compatible system.

Features

- 100% hardware and software compatible with IBM PS/2 Model 50/60
- 100% implementation of Programmable Option Select (POS) logic
- 100% implementation of Model 50/60 compatible system control registers
- Two IBM compatible interrupt controllers
- IBM compatible system timer
- Watchdog timer logic
- System board I/O decode logic
- Peripheral device control logic
- NMI generator
- Clock generation logic for the 80287 and 8042 keyboard controller
- Supports external CMOS RAM for configuration registers
- Built-in 74LS245 compatible video buffers
- 1.5 micron high performance CMOS technology
- 144-pin PFP package

* Trademarks of International Business Machines

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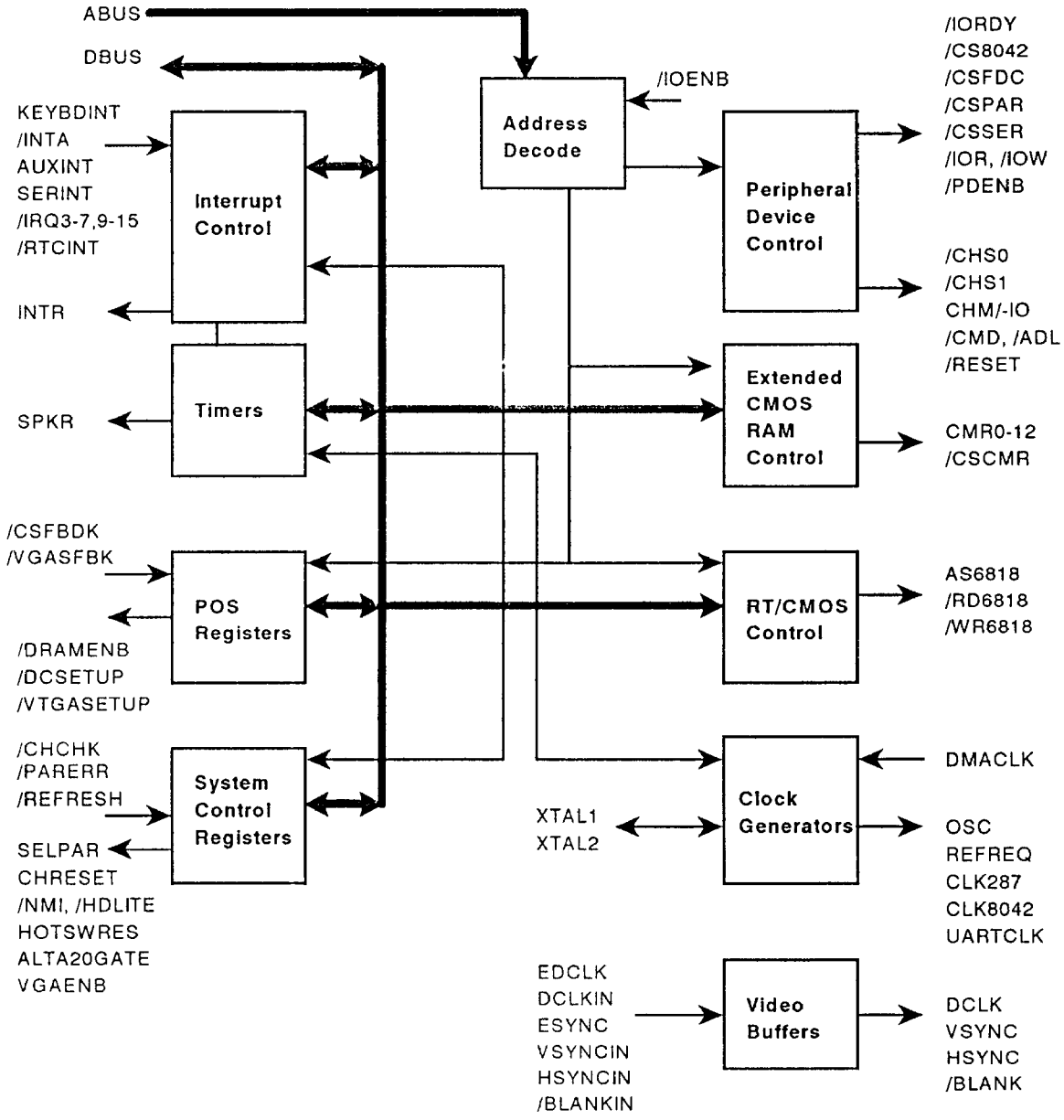
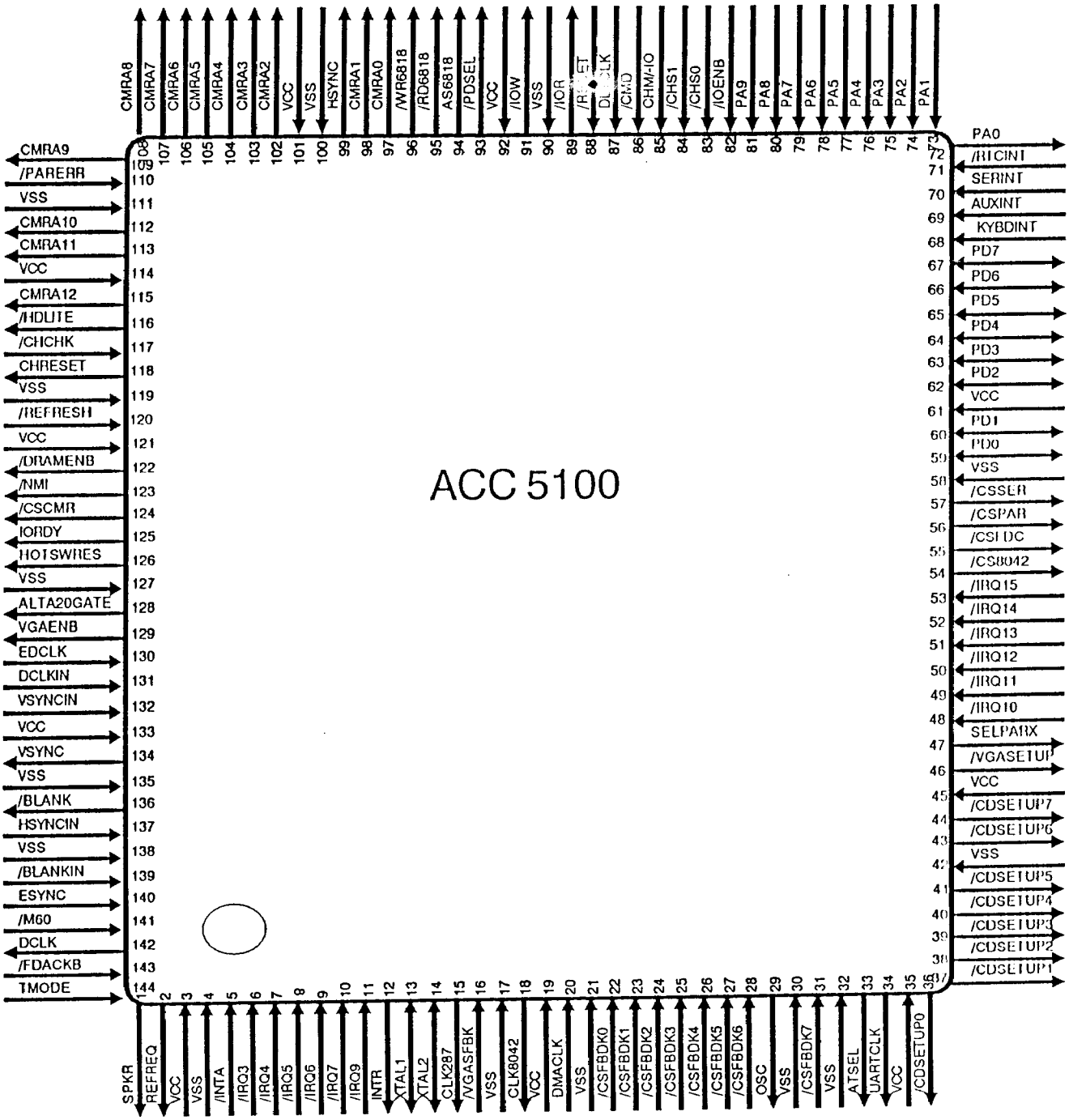
ACC 5100 Block Diagram



Pin Diagram


ACC 5100
CMRA8 107
CMRA7 106
CMRA6 105
CMRA5 104
CMRA4 103
CMRA3 102
CMRA2 101
VCC 100
VSS 99
HSYNC 98
CMRA1 97
CMRA0 96
/WR6818 95
/RD6818 94
AS6818 93
/PDSEL 92
VCC 91
/IOW 90
VSS 89
/IOR 88
/RESET 87
DCLK 86
/CMD 85
CHM-IO 84
/CHS1 83
/CHS0 82
/IOENB 81
PA9 80
PA8 79
PA7 78
PA6 77
PA5 76
PA4 75
PA3 74
PA2 73
PA1 72
CMRA9 109
/PARERR 110
VSS 111
CMRA10 112
CMRA11 113
VCC 114
CMRA12 115
/HDLITE 116
/CHCHK 117
CHRESET 118
VSS 119
/REFRESH 120
VCC 121
/DRAMENB 122
/NMI 123
/CSCMR 124
IORDY 125
HOTSWRES 126
VSS 127
ALTA20GATE 128
VGAENB 129
EDCLK 130
DCLKIN 131
VSYNCIN 132
VCC 133
VSYNC 134
VSS 135
/BLANK 136
HSYNCIN 137
VSS 138
/BLANKIN 139
ESYNC 140
/M60 141
DCLK 142
/FDACKB 143
TMODE 144
SPKR 1
REFREQ 2
VCC 3
VSS 4
/INTA 5
/IRQ3 6
/IRQ4 7
/IRQ5 8
/IRQ6 9
/IRQ7 10
/IRQ9 11
INTR 12
XTAL1 13
XTAL2 14
CLK287 15
/VGASFBK 16
VSS 17
CLK8042 18
VCC 19
DMACLK 20
VSS 21
/CSFBDK0 22
/CSFBDK1 23
/CSFBDK2 24
/CSFBDK3 25
/CSFBDK4 26
/CSFBDK5 27
/CSFBDK6 28
OSC 29
VSS 30
/CSFBDK7 31
VSS 32
ATSEL 33
UARTCLK 34
VCC 35
/CDSETUP0 36
PA0 73
/RICINT 72
SERINT 71
AUXINT 70
KYBDINT 69
PD7 68
PD6 67
PD5 66
PD4 65
PD3 64
PD2 63
VCC 62
PD1 61
PD0 60
VSS 59
/CSSER 58
/CSPAR 57
/CSIDC 56
/CS8042 55
/IRQ15 54
/IRQ14 53
/IRQ13 52
/IRQ12 51
/IRQ11 50
/IRQ10 49
SELPARX 48
/VGASETUP 47
VCC 46
/CDSETUP7 45
/CDSETUP6 44
VSS 43
/CDSETUP5 42
/CDSETUP4 41
/CDSETUP3 40
/CDSETUP2 39
/CDSETUP1 38

Pin Descriptions

Symbol	Pin	I/O	Pin Description
SPKR	1	O	Speaker output.
REFREQ	2	O	Refresh request output.
/INTA	5	I	Interrupt Acknowledge from ACC 5000.
/IRQ3 /IRQ4 /IRQ5 /IRQ6 /IRQ7 /IRQ9 /IRQ10 /IRQ11 /IRQ12 /IRQ13 /IRQ14 /IRQ15	6 7 8 9 10 11 48 49 50 51 52 53	I	Interrupt.
INTR	12	O	Interrupt output for 80286.
XTAL1 XTAL2	13 14	I/O	14MHz Crystal Oscillator.
CLK287	15	O	9.54 MHz clock output for 80287.
/VGASFBK	16	I	Selected feedback for VGA subsystem.
CLK8042	18	O	9.54 MHz clock output for 8042 (different duty cycle than CLK287).
DMACLK	20	I	20MHz clock input, 50/50 duty cycle.
/CSFBDK0 /CSFBDK1 /CSFBDK2 /CSFBDK3 /CSFBDK4 /CSFBDK5 /CSFBDK6 /CSFBDK7	22 23 24 25 26 27 28 31	I	Card selected feedbacks for Micro Channel slot.
OSC	29	O	14MHz buffered output for I/O cards. (24ma sink)
ATSEL	33	O	AT bus select.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
UARTCLK	34	O	1.8432MHz output derived from 14Mhz Crystal.
/CDSETUP0	36	O	Card setup output for I/O card.
/CDSETUP1	37		
/CDSETUP2	38		
/CDSETUP3	39		
/CDSETUP4	40		
/CDSETUP5	41		
/CDSETUP6	43		
/CDSETUP7	44		
/VGASETUP	46	O	Puts VGA chip in setup mode.
SELPARX	47	O	Selects parallel port extended mode.
/CS8042	54	O	Selects 8042 chip.
/CSFDC	55	O	Selects 3203 FDC chip.
/CSPAR	56	O	Select Parallel I/O Port.
/CSSER	57	O	Selects Serial I/O Port.
PD0	59	I/O	Data bus.
PD1	60		
PD2	62		
PD3	63		
PD4	64		
PD5	65		
PD6	66		
PD7	67		
KYBDINT	68	I	Keyboard interrupt from 8042.
AUXINT	69	I	Auxiliary interrupt from 8042.
SERINT	70	I	Serial Interrupt.
/RTCINT	71	I	Interrupt from Real Time Clock.
/IOENB	82	I	Input enables I/O decode on ACC 5100.
/CHS0	83	I	Channel Status input.
/CHS1	84		

Pin Descriptions

Symbol	I/O	Pin Description
PA0	72	I	Address bus input.
PA1	73	
PA2	74	
PA3	75	
PA4	76	
PA5	77	
PA6	78	
PA7	79	
PA8	80	
PA9	81	
CHM/-IO	85	I	Channel Memory /IO input.
/CMD	86	I	Command signal from Micro Channel.
DLYCLK	87	I	20 MHz clock delay, 15 ns.
/RESET	88	I	Reset input.
/IOR	89	O	I/O Read strobe output.
/IOW	91	O	I/O Write strobe output.
/PDSEL	93	O	Peripheral Bus selected output.
AS6818	94	O	Control line for 6818 RTC.
/RD6818	95	O	Control line for 6818 RTC.
/WR6818	96	O	Control line for 6818 RTC.
CMRA0	97	O	Address line for 8K x 8 CMOS RAM.
CMRA1	98	
CMRA2	102	
CMRA3	103	
CMRA4	104	
CMRA5	105	
CMRA6	106	
CMRA7	107	
CMRA8	108	
CMRA9	109	
CMRA10	112	
CMRA11	113	
CMRA12	115	
HSYNC	99	O	Horizontal sink to VGA.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/PARERR	110	I	Parity error input.
/HDLITE	116	O	Hard Disk activity light output.
/CHCHK	117	I	Micro Channel check input.
CHRESET	118	O	Micro Channel reset output. (24ma sink).
/REFRESH	120	I	Micro Channel refresh input.
/DRAMENB	122	O	DRAM enable output for ACC 5300.
/NMI	123	O	Non-maskable interrupt.
/CSCMR	124	O	Chip select for 8K x 8 CMOS RAM.
IORDY	125	O	I/O Ready output. Indicates that the perhipheral controlled by the ACC 5100 is ready.
HOTSWRES	126	O	Alternate "hot" CPU reset.
ALTA20GATE	128	O	Alternate A20 gate signal.
VGAENB	129	O	Enables on-board VGA operation. Derived from port 3C3H.
EDCLK	130	I	Enables on-board VGA to drive DCLK. Pin has built-in pullup resistor.
DCLKIN	131	I	DCLK from on-board VGA.
VSYNCIN	132	I	Sync signal from on-board VGA.
VSYNC	134	O	Vertical sync to VGA.
/BLANK	136	O	Blank signal to VGA.
HSYNCIN	137	I	Sync signal from on-board VGA.
/BLANKIN	139	I	Sync signal from on-board VGA.
ESYNC	140	I	Enables on-board VGA to drive sync signals on Micro Channel. Pin has built-in pullup resistor.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/M60	141	I	Model 50/60 strap. Pin grounded for Model 60, or no connect for Model 50. Model 50 does not require CMOS RAM.
DCLK	142	O	DCLK to Micro Channel.
/FDACK	143	I	DMA acknowledge for FDC.
TMODE	144	I	Test mode, must be pulled low.
VCC	3, 19, 35, 45, 61, 92, 101, 114, 121, 133		+5 volt supply
VSS	4, 17, 21, 30, 32, 42,58, 90, 100, 111, 119, 127, 135, 138		Ground

Functional Description

Interrupt Controller

The ACC 5100 provides 16 levels of independently maskable interrupts. These are functionally equivalent to two Intel 8259A interrupt controllers cascaded together.

Interrupt controller 1 is the master controller. It is accessed through I/O addresses 0020H and 0021H. Interrupt controller 2 is the slave controller. It is accessed through I/O addresses 00A0H and 00A1H. Table 1 lists all interrupts by priority level, name, and functional assignment.

Figure 1 is a block diagram of the ACC 5100 interrupt controller. Each functional block is described in detail.

Table 1 **Interrupt Level Assignments**

Level	Name	Function
1	NMI	Parity, watchdog timer, arbitration time-out, channel check
2	IRQ0	Timer
3	KYBDINT	Keyboard
	IRQ2	Cascade interrupt control
4	IRQ8	Real time clock
5	IRQ9	Redirect cascade
6	IRQ10	Reserved
7	IRQ11	Reserved
8	IRQ12	Mouse
9	IRQ13	Math coprocessor exception
10	IRQ14	Fixed disk
11	IRQ15	Reserved
12	IRQ3	Serial 2
13	IRQ4	Serial 1
14	IRQ5	Reserved
15	IRQ6	Floppy disk
16	IRQ7	Parallel port

IRQ8 through IRQ 15 are cascaded through IRQ2

Note: The AUXINT signal is internally ORed with IRQ12.

SERINT drives IRQ4 if Serial 1 is selected by POS and IRQ3 if Serial 2 is selected.

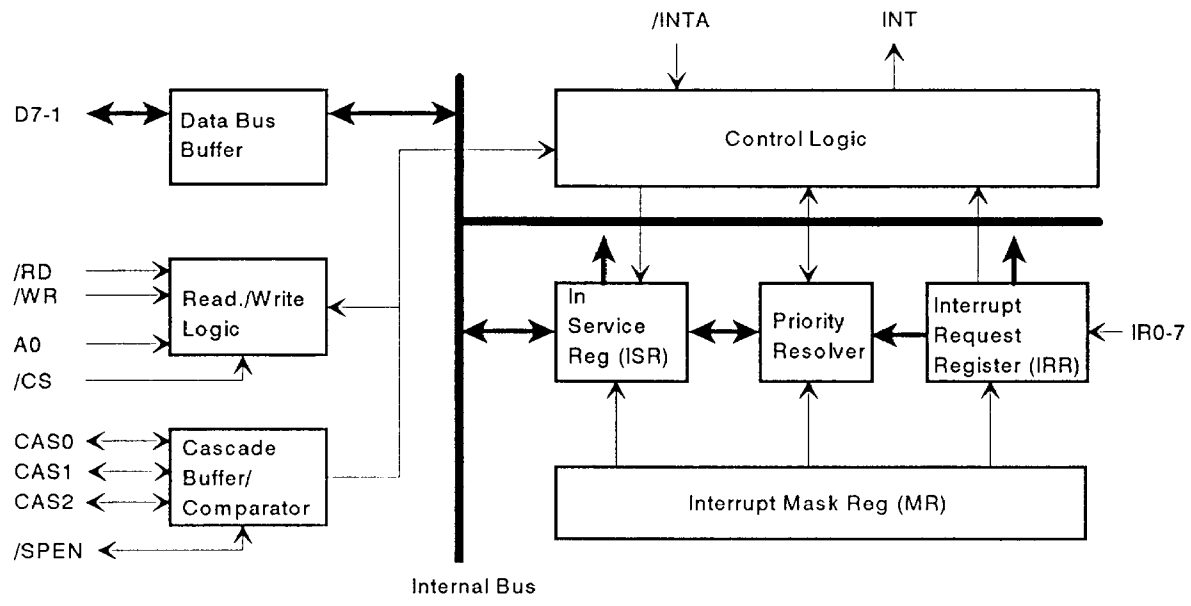


Figure 1 ACC 5100 Interrupt Controller

Interrupt Request Register (IRR) and In-service Register (ISR)

The interrupts at the IR input lines are controlled by the Interrupt Request Register (IRR) and In Service Register (ISR) register in cascade. The IRR stores all the interrupt levels requesting service. The ISR stores all the interrupt levels being serviced.

Priority Resolver

The priority resolver determines the priorities of the bits set in the IRR. This logic selects the highest priority and strobes it into the corresponding bit of the ISR during an /INTA pulse.

Interrupt Mask Register (IMR)

The Interrupt Mask Register (IMR) stores the bits that mask the interrupt lines to be masked. The IMR operates on the IRR. If a higher priority input is masked, the interrupt request lines of a lower priority are not affected.

Interrupt Acknowledge (/INTA signal)

/INTA pulses cause the 8259A to release vectoring data to the data bus.

Read/Write Control Logic

Read/write control logic accepts output commands from the CPU. This logic contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store various control formats for the device to operate. This logic also allows the status of the 8259A to be transferred to the Data bus.

Cascade Buffer/Comparator

The Cascade Buffer/Comparator stores and compares the IDs of each interrupt controller in the system. Master CAS0-2 pins are output pins. Slave CAS0-2 pins are input pins. The master sends the ID of the interrupting slave device (fixed at 2) onto the CAS0-2 lines. The slave sends its preprogrammed subroutine address to the Data bus during the next one or two consecutive /INTA pulses.

Interrupt Sequence

The normal sequence of events during an interrupt is listed below.

1. One or more of the interrupt request lines (/IR7-0) are activated, setting the corresponding IRR bit(s).

2. The interrupt controller evaluates the requests and sends an INT to the CPU if appropriate.

3. The CPU acknowledges the INT and sends two /INTA pulses.

4. After receiving the first /INTA pulse from the CPU, the highest priority ISR bit is set and the corresponding IRR bit is reset. The interrupt controller does not drive the Data bus during this cycle.

   During the second /INTA pulse, the interrupt controller releases an 8-bit pointer to the Data bus to be read by the CPU.

5. The interrupt cycle is complete at this point. In the AEOI mode, the ISR bit is reset at the end of the second /INTA pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

End of Interrupt (EOI) Command

The In-service (IS) bit can be reset two ways.

1. Automatically after the the trailing edge of the last in-sequence /INTA pulse (when AEOI bit in ICW1 is set).

2. By a command word issued to the interrupt controller before returning from a service routine (EOI command). An EOI command must be issued twice if in Cascade mode, once for the master and once for the corresponding slave.

There are two forms of the EOI command: specific and non-specific. When the interrupt controller is in a mode which preserves the fully-nested structure, it can determine which IS bit to reset on EOI. When a non-specific EOI command is issued, the 8259A automatically resets the highest IS bit set because in the fully-nested mode, the highest IS level has to be the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI=1, SL=0, R=0).

When the interrupt controller is in a mode which can interfere with the fully-nested structure, it might not be able to identify the last level acknowledged. In this case, a specific EOI command must be issued which includes the IS level to be reset. A specific EOI can be issued with OCW2 (EOI=1, SL=1, R=0, and L0-2 is the binary level of the IS bit to be reset).

Note that an IS bit masked by an IMR bit is not cleared by a non-specific EOI if the interrupt controller is in Special Mask mode.

Modes of Operation

The ACC 5100 interrupt controller has six modes of operation.

- Fully-nested Mode
- Special Fully-nested Mode
- Automatic Rotation Mode
- Specific Rotation Mode
- Poll Mode
- Special Mask Mode

Fully-nested Mode

The interrupt controller enters the Fully-nested mode after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 7-0. Zero is the

highest. When an interrupt is acknowledged, the highest priority request is determined and its vector is put on the Data bus. One of the interrupt service register (IS0-7) bits is set and remains set until the microprocessor issues an EOI command immediately before returning from the service routine, or until the trailing edge of the last INTA, if the AEOI (Automatic End of Interrupt) bit is set. All further interrupts of the same or lower priority are inhibited if the IS bit is set, while higher levels generate an interrupt. The interrupts generated by higher levels are acknowledged only if the microprocessor internal Interrupt enable flip-flop has been re-enabled by software.

After the initialization sequence, IR0 has the highest priority and IR7, the lowest. Priorities can be altered in the Rotation mode.

Special Fully-nested Mode

The Fully-nested mode is programmed into the master (using ICW4). Note that the ACC 5100 has only one configuration, one master and one slave.

This mode is similar to the Fully-nested mode with the following exceptions:

1. When an interrupt request from the slave is in service, the slave is not locked out from the master's priority logic. Additional interrupt requests from higher priority IRs within the slave are recognized by the master and initiate interrupts to the processor. (In Fully-nested mode, the slave is masked out when its request is in service and higher requests from the slave cannot be serviced.)

2. When exiting the interrupt service routine, the software must check if the interrupt serviced was the only one from the slave by sending a non-specific EOI command to the slave, reading its In-service register, and checking for zero. If the In-service register is empty, a non-specific EOI can be sent to the master. If the In-service register is not empty, an EOI must not be sent.

Automatic Rotation Mode

In applications with several interrupt devices with equal priority, Automatic Rotation mode takes effect. A device, after being serviced, receives the lowest priority. Therefore, a device requesting an interrupt must wait, worst case, until each of seven other devices are serviced at most once. For example, Figure 2 lists the priority and in-service (IS) status if IR4 has the highest priority.

Before rotation

IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
0	1	0	1	0	0	0	0

IS status

lowest priority							highest priority
7	6	5	4	3	2	1	0

Priority status

After rotation

IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
0	1	0	0	0	0	0	0

IS status

highest priority							lowest priority
7	6	5	4	3	2	1	0

Priority status

Figure 2 Priority Changes with Rotation

There are two ways to use OCW2 to perform automatic rotation.

1. Rotation on the Non-specific EOI command.
   R=1, SL= 0, EOI=1

2. Rotation in the Automatic EOI mode.
   To set, R=1, SL=0, EOI=0
   To clear, R=0, SL=0, EOI=0

Specific Rotation Mode

Priorities can be changed by programming the lowest priority and therefore fixing all other priorities. For example, if IR5 is programmed as the bottom priority device, IR6 will have the highest priority.

The SET PRIORITY command is issued in OCW2 when R=1, SL=1, and L0-2 is the binary priority level code of the bottom priority device.

Internal status is updated by software control during OCW2 in this mode. However, it is independent of the EOI command (also executed by OWC2). Priority changes can be executed during an EOI command by using the Rotate on specific EOI command in OCW2, (R=1, SL=1, EOI=1 and L0-2 = IR level to receive bottom priority).

Poll Mode

In Poll mode, INT output is not used, thus preventing the microprocessor internal interrupt enable flip-flop from being reset and disabling its interrupt input. Service to devices is accomplished through software with a Poll command.

The Poll command is issued by setting P=1 in OCW3. The interrupt controller considers the next /RD pulse to the interrupt controller (/RD=0, /CS=1) as an interrupt acknowledge, sets the appropriate IS bit if there is a request and reads the priority level. Interrupt is frozen from /WR to /RD. Table 2 shows a word enabled on the Data bus during /RD.

Table 2 Word Enabled on the Data Bus during /RD

D7	D6	D5	D4	D3	D2	D1	D0
I	-	-	-	-	W2	W1	W0

W0-2: Binary code of the highest priority level requesting service.

I: Equal to 1 if there is an interrupt.

Poll mode is used if there is a routine command common to several levels and the /INTA sequence is not necessary.

Special Mask Mode

Some applications require an interrupt service routine that alters the system priority structure dynamically during execution.For example, a software routine can inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty in this case is that if an interrupt request is acknowledged and EOI command did not reset the IS bit (while executing a service routine), the interrupt controller inhibits all lower priority requests with no simple method for the routine to enable them. However, in Special Mask mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level and enables interrupts from all other levels that are not masked (lower and higher levels). Thus, any interrupts can be selectively enabled by loading the mask register.

The Special Mask mode is set by OWC3 when ESMM=1 and SMM=1. It is cleared when ESMM=1 and SMM=0.

Level Sensitive Mode

The interrupt controller cannot be put in an edge-triggered mode, it operates in level sensitive mode only. In the Level sensitive mode, interrupt requests are recognized by a high level on the interrupt request input. This conditions requires that interrupt requests be removed before the EOI command is issued.

Interrupt Acknowledge

The CPU issues two interrupt acknowledge cycles. The interrupt controller uses the first interrupt acknowledge cycle to freeze the state of the interrupts internally for priority resolution. On the second interrupt acknowledge cycle, the master sends a byte of data to the processor with the acknowledged interrupt code.

Programming the Interrupt Controller

The interrupt controller accepts two types of command words from the CPU.

1. Initialization Control Words (ICWs)

   Before normal operation can begin, each interrupt controller must be brought to a starting point using a sequence of two to four bytes timed by /WR pulses.

2. Operation Control Words (OCWs)

   These control words instruct the interrupt controller to operate in the following interrupt modes:

   Fully-nested Mode
   Rotation Mode
   Special Mask Mode
   Polled Mode

OCWs can be written into the interrupt controller any time after initialization. Table 3 is a map of the interrupt controller functions.

Table 3 Interrupt Controller Function Map

Interrupt	Controller	Address Function	Read/Write
1	020	ICW1	Write
1	021	ICW2	Write
1	021	ICW3	Write
1	021	ICW4	Write
1	021	OCW1	Write
1	020	OCW2	Write
1	020	OCW3	Write
1	020	IRR	Read
1	020	ISR	Read
1	021	IMR	Read
2	0A0	ICW1	Write
2	0A1	ICW2	Write
2	0A1	ICW3	Write
2	0A1	ICW4	Write
2	0A1	OCW1	Write
2	0A0	OCW2	Write
2	0A0	OCW3	Write
2	0A0	IRR	Read
2	0A0	ISR	Read
2	0A1	IMR	Read

Initialization Control Words (ICWs)

When a command is issued with A0=0 and D4=1, it is interpreted as Initialization Control Word 1 (ICW1). ICW1 begins the following automatic initialization sequence.

1. The Interrupt mask register is cleared.
2. IR7 input is assigned priority 7.
3. Slave mode address is set to 7.
4. Special mask mode is cleared and status read is set to IRR.
5. If IC4=0, all functions selected in ICW4 are set to zero. Master/slave in ICW4 is only used in the buffered mode. In non-buffered mode, there is no AEOI.

Initialization Control Word 1 and 2 (ICW1, ICW2)

The interrupt controller inserts A15-11 in the five most significant bits of the vectoring byte and sets the three least significant bits according to the interrupt level. A10-5 are ignored. The Address Interval (ADI) has no effect. Table 4 contains ICW1 format with mandatory codes. Table 5 is the ICW2 format and Table 6 contains vector coding information.

Table 4 ICW1 Format

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	0	1

Table 5 ICW2 Format

D7	D6	D5	D4	D3	D2	D1	D0
T7	T6	T5	T4	T3	A10	A9	A8

Table 6 Coding for an Interrupt Vector Byte

Master	Slave	D7	D6	D5	D4	D3	D2	D1	D0
IR7	IR8	T7	T6	T5	T4	T3	1	1	1
IR6	IR9	T7	T6	T5	T4	T3	1	1	0
IR5	IR10	T7	T6	T5	T4	T3	1	0	1
IR4	IR11	T7	T6	T5	T4	T3	1	0	0
IR3	IR12	T7	T6	T5	T4	T3	0	1	1
IR2	IR13	T7	T6	T5	T4	T3	0	1	0
IR1	IR14	T7	T6	T5	T4	T3	0	0	1
IR0	IR15	T7	T6	T5	T4	T3	0	0	0

Initialization Control Word 3 (ICW3)

The interrupt controller loads the 8-bit slave register with the following two functions.

1. In master mode when SP=1 or in buffered mode when M/S=1 in ICW4, a 1 is set for each slave in the system. The master releases byte 1 of the call sequence and enables the corresponding slave to release byte 2 through the cascade lines. All bits must be programmed according to Table 7, the ICW3 format is as a master device.

Table 7 ICW3 Format (Master Device)

D7	D6	D5	D4	D3	D2	D1	D0
S7	S6	S5	S4	S3	S2	S1	S0
0	0	0	0	0	1	0	0

2. In slave mode when /SP=0 or if BUF=1 and M/S=0 in ICW4, bits 2-0 identify the slave. The slave compares its cascade input with these bits, and if equal, byte 2 of the call sequence is released on the Data bus. The slave device must be programmed according to Table 8.

Table 8 ICW3 Format (Slave Device)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	ID2	ID1	ID0
0	0	0	0	0	0	1	0

Initialization Control Word 4 (ICW4)

Table 9 is the ICW4 format.

Table 9 ICW4 Format

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	SFNM	BUF	M/S	AEOI	uPM
0	0	0	*	0	0	*	1

* programmable

SFNM Setting this bit to 1 programs the Special fully-nested mode.

AEOI Automatic end of interrupt
1 = ON
0 = OFF

Figure 3 is a flow chart of the initialization sequence.

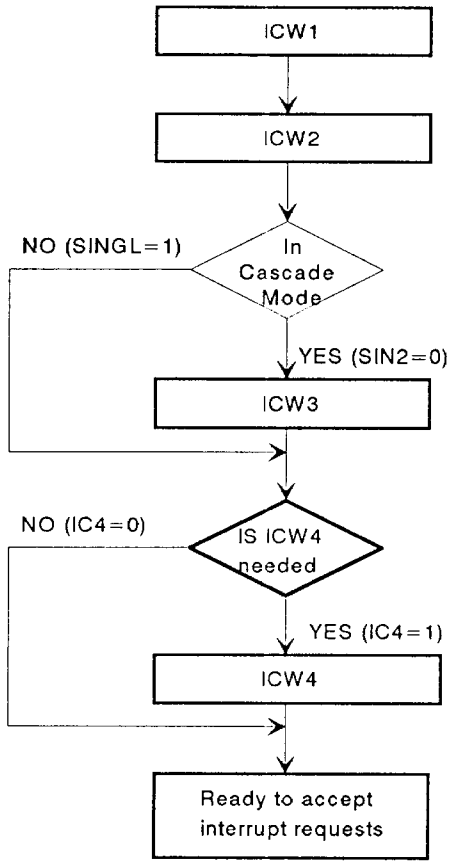


Figure 3 Initialization Sequence

Operation Control Words (OCWs)

After initialization control words (ICWs) are programmed into the interrupt controller, the chip can accept interrupt requests on its input lines. During the interrupt controller operation, Operation Control Words (OCWs) can cause the interrupt controller to operate in various modes.

Operation Control Word 1 (OCW1)

OCW1 sets and clear the mask bits in the Interrupt mask register (IMR). M7-M0 are the the eight mask bits. When M=1, the channel is masked. When M=0, the channel is enabled. Table 10 contains the format of the OCW1 control word.

Table 10 Operation Control Word 1 Format

D7	D6	D5	D4	D3	D2	D1	D0
M7	M6	M5	M4	M3	M2	M1	M0

Operation Control Word 2 (OCW2)

Table 11 contains the format of the OCW2 control word.

Table 11 Operation Control Word 2 Format

D7	D6	D5	D4	D3	D2	D1	D0
R	SL	EOI	0	0	L2	L1	L0

R, SI, EOI

These bits control the rotate and end of interrupt modes and combinations of these two modes.

R	SL	EOI	Command
0	0	0	Reserved
0	0	1	Non-specific EOI command
0	1	0	No operation
0	1	1	Specific EOI command*
1	0	1	Rotate on non-specific EOI command
1	0	1	Rotate on non-specific EOI command
1	1	0	Set priority command
1	1	1	Rotate on specific EOI command**

* Bits 0,1and 2 are the binary level of the in-service bit to be reset

** Bits 0, 1, and 2 are the binary level of the lowest priority device

L2-L0 When the SL bit is active, these bits determine the interrupt level affected.

L2	L1	L0	Level affected
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Operation Control Word 3 (OCW3)

Table 12 contains the format of the OCW3 control word.

Table 12 Operation Control Word 3 Format

D7	D6	D5	D4	D3	D2	D1	D0
0	ESMM	SMM	0	1	P	RR	RIS

ESMM Enable special mask mode. When this bit is set to 1, the SMM bit is enabled to set or reset the Special mask mode. When ESMM is set to 0, the SMM bit becomes a "don't care" bit.

SMM Special mask mode. If ESMM=1 and SMM=1, the interrupt controller enters Special mask mode. If ESMM=1 and SMM=0, the interrupt controller reverts to normal mask mode. When ESMM=0, SMM has no effect.

ESMM	SMM	Result
0	0	No action
0	1	No action
1	0	Reset special mask
1	1	Set special mask

Poll command.
1 = enabled
0 = disabled

RR, RIS
Read register command bits.

RR	RIS	Result
0	0	No action
0	1	No action
1	0	Read IR register on next /RD pulse
1	1	Read IS register on next /RD pulse

System Timers

The ACC 5100 contains three programmable timers. Channel 0 is a general purpose system timer. Channel 2 is primarily used as a tone generator. Channel 3 is a watchdog timer used for error detection. These timers are compatible with the Intel 8254. Figure 4 is a block diagram of a system timer.

Control word register

Each counter has an associated control word register which is programmed to define the mode and parameters of counter operation. The counter (counting element) is a 16-bit synchronous down counter that can be preset.

The output latches OL_M and OL_L (most-significant-bit and least-significant-bit) are 8-bit latches. Both latches usually follow the counter, but if an appropriate counter latch command is sent to the Control word register, the present count is latched until read by the CPU, then the latches follow the counter again. The counter's control logic enabled one latch at a time to drive the internal bus. Note that the counter itself is not read, it is the output latch that is being read.

The count registers CR_M and CR_L (most-significant-bit and least-significant-bit) are 8-bit registers. When a new count is written to the counter, the count registers store the count

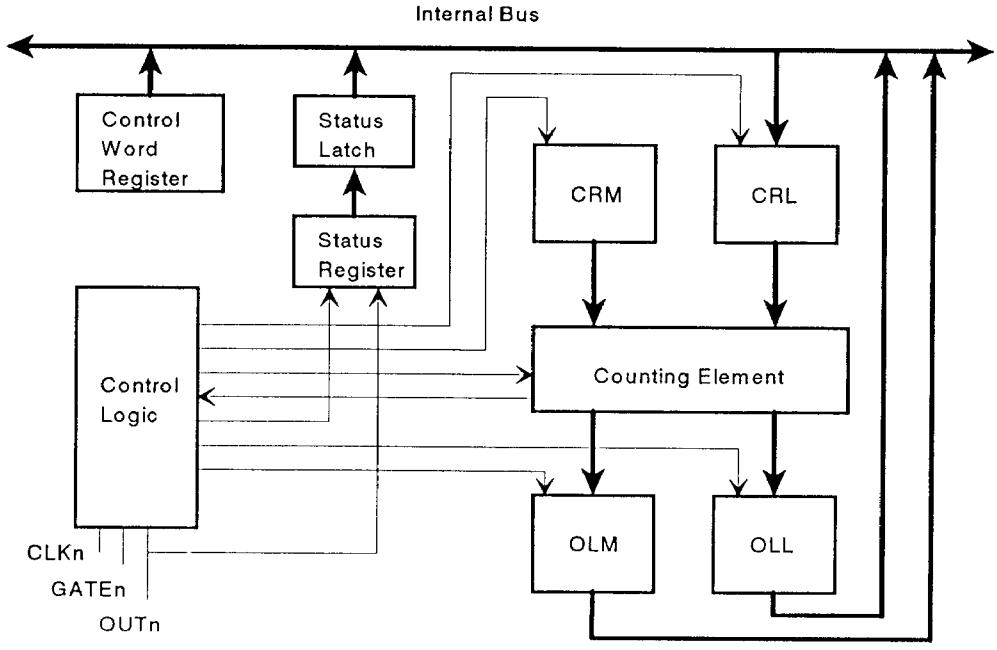


Figure 4 System Timers

and transfer the count to the counter. One register at a time is loaded from the internal bus (controlled by the control logic). Both bytes are transferred to the counter simultaneously. The count registers are cleared when the counter is programmed. If the counter has been programmed for one byte counts, the other byte will be zero. Counts are always written to the count registers, not the counter.

Channel 0

GATE0	Always enabled
CLKIN0	Driven by 1.193 MHz
CLKOUT0	Drives IRQ0 latch

A latch set by the rising edge of the CLKOUT0 drives IRQ0. The latch can be cleared by a system rest, an interrupt acknowledge cycle with a hex 08 vector, or an I/O write to hex 0061 (System control port B) setting bit 7 to 1.

Channel 2

GATE2	Controlled by port hex 0061 bit 0
CLKIN2	Driven by 1.193 MHz
CLKOUT2	Two connections, one is to port, hex 0061 bit 5. The other connection is a logical AND to hex 0061 bit 1 (speaker data enable). The output of the AND gate drives the SPKR signal.

Note that the SPKR output must be enabled by setting Bit 1 of system control port B (hex 61) to 1 to drive the output from Channel 2.

Channel 3

GATE3	Driven by IRQ0
CLKIN3	Tied to CLKOUT0 inverted
CLKOUT3	Drives NMI active when high

Channel 3 operates only in Mode 0 and counts in 8-bit binary. Channel 3 operation is defined

only when Channel 0 is programmed in Mode 2 or Mode 3.

This timer detects when IRQ0 is active for more than one period of CLKOUT0. The count decrements if IRQ0 is active when a rising edge of CLKOUT0 occurs. When the count decrements to 0, an NMI is generated. Channel 3 can be used to detect when IRQ0 is not being serviced and can therefore be useful in detecting error conditions.

When Channel 3 times out, an NMI is generated and System control port A (hex 0090) bit 4 is set to 1.

When Channel 3 is enabled, and IRQ0 is pending for more than one period of CLKOUT0, any data written to Channels 0 or 3 is ignored. If Channel 3 is disabled, the inhibit signal is never active.

There are three timers: 0, 2 and 3. Each timer is independent. Timers 0 and 2 are 16-bit binary or BCD down counters. Timer 3 is an 8-bit down counter that only counts in binary. All counters can be preset.

System timers are treated as five external I/O ports when programmed. Three ports are treated as count registers and two are control registers for programming timer modes. Counters are programmed by writing a control word followed by an initial count. Control words are sent to Control word registers. Counters 0 and 2 are located at address 0043. Timer 3 is located at address 0047. Initial counts are written into Count registers, then transferred to the counting element depending on mode. The control word specifies the format of the initial count.

A new initial count can be written to the counters without affecting the programmed mode of the counter. The new count must follow the format of the programmed count.

The count is read by issuing a Counter latch command which locks the current value into the output latch until read. If the counter is programmed for 2-byte counts, two bytes must be read. They do not have to be read consecutively; read, write or programming operations of other counters can be inserted between the two bytes.

However, if the counters are programmed to read or write 2-byte counts, the program cannot transfer control between writing the first and second byte to another routine that reads or writes to the same counter without causing a bad count.

Table 13 contains system timer/counter register data.

Table 13 System Timer/Counter Registers

I/O	Address Register
0040	Count register, Channel 0 (R/W)
0042	Count register, Channel 2 (R/W)
0043	Control byte register, Channel 0 or 3 (W)
0044	Count register, Channel 3 (R/W)
0047	control byte register, Channel 3 (W)

Count register, Channel 0 (Hex 0040)

The control byte is written to port hex 0043 to establish the format of the count (LSB only, MSB only, or LSB followed by MSB). The control byte must be written before writing the count to port hex 0040.

Count register, Channel 2 (Hex 0042)

The control byte is written to port hex 0043 to establish the format of the count (LSB only, MSB only, or LSB followed by MSB). The control byte must be written before writing the count to port hex 0042.

Control word register, Channel 0 or 2 (Hex 0043)

The format of the control byte (port hex 0043) for counter 0 and 2 is defined by this write only register.

7 6	5 4	3 2 1	0
Counter Select	W/R	Mode Select	Count Method

Counter Select

These bits select Counter 0 or 2.

7	6	Function
0	0	Select counter 0
0	1	Unused
1	0	Select counter 2
1	1	Unused

R/W Counter Bits

These bits specify a Counter latch command of a Control byte. If a control byte is selected, the method for reading or writing the bytes is also determined.

5	4	Function
0	0	Counter latch command
0	1	Read/Write counter bits 0-7 only
1	0	Read/Write counter bits 8-15 only
1	1	Read/Write counter bits 0-7 first, then bits 8-15

Mode Select

3	2	1	Function
0	0	0	Mode 0 Interrupt on terminal count
0	0	1	Mode 1 Hardware retriggerable one shot
0	1	0	Mode 2 Rate generator
0	1	1	Mode 3 Square wave
1	0	0	Mode 4 Software retriggerable strobe
1	0	1	Mode 5 Hardware retriggerable strobe

Count Method

This bit selects the counting method for the control register.

Bit 0 = 1 Binary coded decimal
Bit 0 = 0 16-bit binary

Control Word Register, Channel 3 (Hex 0047)

The format of the control byte (port hex 0047) for counter 3 is defined by this write only register.

Count register, Channel 3 (Hex 0044)

The control byte is written to port hex 0047 to decide the count format. This must be written to before writing the count to port hex 0044.

7 6	5 4	3 2 1 0
Counter Select	W/R	Unused

Counter Select

These bits select counter 3.

7	6	Function
0	0	Select counter 3
0	1	Unused
1	0	Unused
1	1	Unused

W/R Counter

These bits decide a counter latch command or a control byte.

5	4	Function
0	0	Counter latch command select counter 0
0	1	R/W counter bits 0-7 only
1	0	Unused
1	1	Unused

Bits 3-0 are unused and must be written to 0.

Counter Latch Command

The Counter latch command is written to the control byte register. Bits 5 and 4 distinguish the counter latch command from a control byte. See above.

When the Counter latch command is received, the count is latched into the selected counter's output latch. This count is held in the latch until read by the CPU or until the counter is reprogrammed. After the count is read, it is automatically unlatched. The output latch resumes following the counting element. Counter latch commands do not affect the mode of the counter. All latch commands issued to a counter before the count is read are ignored. A read cycle to the counter latched returns the value latched by the first Counter latch command.

Timer Modes

There are six system timer modes.

Mode 0	Interrupt on Terminal Count
Mode 1	Hardware Retriggerable One-shot
Mode 2	Rate Generator
Mode 3	Square Wave
Mode 4	Software Triggered Strobe
Mode 5	Hardware Triggered Strobe (retriggerable)

Term definitions follow: a "CLK pulse" is a rising, then falling edge on the counter CLK input, a "trigger" is a rising edge on a counter's GATE input, and a "counter load" is the transfer of a count from the counter register to the counting element.

Table 14 lists the minimum and maximum initial counts for Counters 0 and 2.

Mode 0 Interrupt on Terminal Count

Event counting is performed using Mode 0. After the Control word is written, OUT is initially low, and remains low until the counter reaches zero. OUT then goes high and remains high until a new count or a new Control word for Mode 0 is received by the counter.

GATE = 1 enables counting
GATE = 0 disables counting

GATE has no effect on OUT.

After the Control word and initial count are written to a counter, the initial count is loaded on the next CLK pulse. The CLK pulse does not decrement the count. For an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

Table 14 Minimum and Maximum Initial Counts for Counters 0 and 2

Minimum Mode	Maximum Count	Count
0	1	$0=2^{16}$ (binary counting) or 10^4 (BCD counting)
1	1	$0=2^{16}$ (binary counting) or 10^4 (BCD counting)
2	2	$0=2^{16}$ (binary counting) or 10^4 (BCD counting)
3	2	$0=2^{16}$ (binary counting) or 10^4 (BCD counting)
4	1	$0=2^{16}$ (binary counting) or 10^4 (BCD counting)
5	1	$0=2^{16}$ (binary counting) or 10^4 (BCD counting)

Counter 3 can only use Mode 0. It has a minimum initial count of 1 and a maximum of hex FF.

When a new count is written to the counter, it is loaded on the next CLK pulse and counting continues from the new count. If a 2-byte count is written, the first byte disables counting, out is set low (no clock pulse required); the second byte allows the new count to be loaded on the next CLK pulse. The counting sequence is synchronized by software. OUT does not go high until N + 1 CLK pulses after the new count N is written.

If an initial count is written while GATE = 0, it is loaded on the next CLK pulse. When GATE goes high, OUT goes high N CLK pulses later. No CLK pulse is required to load the counter (this has already been accomplished).

Mode 1 Hardware Retriggerable One-shot

OUT is initially high and goes low on the CLK pulse following a trigger to begin the one-shot pulse. OUT remains low until the counter reaches zero. OUT goes high and remains high until the CLK pulse after the next trigger.

The counter is armed after the Control word and initial count are written. A trigger loads the counter and sets OUT low on the next CLK pulse which starts the one-shot pulse. An initial count of N results in a one-shot pulse lasting N CLK cycles. The one-shot is retriggerable; therefore OUT remains low for N CLK pulses after any trigger. The one-shot pulse can be repeated without reloading the count into the counter. GATE does not affect OUT.

If a new count is written during a one-shot pulse, the current one-shot is not affected unless the counter is retriggered. If the counter is retriggered, the counter is loaded with the new count and the one-shot pulse continues until the new count is finished.

Mode 2 Rate Generator

Mode 2 functions like a divide-by-N counter. OUT is initially high. When the initial count decrements to 1, OUT goes low for one CLK pulse, then goes high again. The counter reloads the initial count and the process repeats. The same sequence repeats indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE =1 enables counting
GATE =0 disables counting

If GATE goes low during an output pulse, OUT is set high. When triggered, the counter is reloaded with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Therefore, the counter can be synchronized by the GATE input.

After a Control word and initial count are written, the counter is loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. The counter can also be synchronized by software in this manner.

If a new count is written while counting, the current counting sequence is not affected. If a trigger is received after writing a new count but not before the end of the current period, the counter is loaded with the new count on the next CLK pulse. Counting continues from the new count. Otherwise the count is loaded at the end of the current counting cycle. A count of 1 is illegal in Mode 2.

Mode 3 Square Wave

Mode 3 is similar to Mode 2 except for the OUT duty cycle. OUT is initially high. When half the initial count has expired, OUT goes low for the rest of the count. This sequence is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycle.

GATE =1 enables counting
GATE =0 disables counting

If GATE goes low while OUT is low, OUT goes high. No clock pulse is required. Triggering reloads the counter with the initial count on the

next CLK pulse. Therefore, the counter can be synchronized by the GATE input.

If a Control word and initial count are written, the counter is loaded on the next CLK pulse. The counter can also be synchronized by software in this manner.

If a new count is written while counting, the current counting sequence is not affected. If a trigger is received after writing a new count but before the end or the current half-cycle of the square wave, the counter is loaded with the new count on the next CLK pulse. Counting continues from the new count. Otherwise, the new count is loaded at the end of the current half-cycle.

Implementing Even Counts

OUT is initially high. The initial count is loaded on one CLK pulse, then decremented by two on succeeding CLK pulses. When the count expires, OUT changes value. The counter is reloaded with the initial count. This sequence is repeated indefinitely.

Implementing Odd Counts

OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse, then decremented by two on succeeding CLK pulses. OUT goes low one clock pulse after the count expires. The counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the counter is reloaded with the initial count minus one. This is repeated indefinitely. For odd counts, OUT is high for (N + 1)/2 counts and low for (N - 1)/2 counts.

Mode 4 Software Triggered Strobe

OUT is initially high. When the initial count expires, OUT goes low for one CLK pulse and then goes high again. Writing the initial count triggers the counting sequence.

GATE = 1 enables counting
GATE = 0 disables counting

GATE does not affect OUT.

After a Control word and initial count are written, the counter is loaded on the next CLK pulse. The CLK pulse does not decrement the count. For an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written while counting, the new count is loaded on the next CLK pulse. Counting continues from the new count. If a 2-byte count is written, the first byte has no effect on the counting, the second byte causes the new count to be loaded on the next CLK pulse.

The sequence can be retriggered by software in this manner. OUT strobes low N + 1 CLK pulses after the new count of N is written.

Mode 5 Hardware Triggered Strobe (Retriggerable)

OUT is initially high. A rising edge of GATE triggers counting. When the initial count has expired, OUT goes low for one CLK pulse and then goes high again.

After the Control word and initial count are written, the count is not loaded until the CLK pulse after a trigger. The CLK pulse does not decrement the count. For an initial count of N, OUT does not strobe low until N + 1 CLK pulses after a trigger.

A trigger causes the counter to be loaded with the initial count on the next CLK pulse. The

counting sequence can be retriggered. OUT does not strobe low for N + 1 CLK pulses after any trigger. OUT is not affected by GATE.

If a new count is written while counting, the current sequence is not affected. If a trigger occurs after the new count is written but before the current count expires, the counter is loaded with the new count on the next CLK pulse. Counting continues.

Operations Common to All Modes

1. All control logic is immediately reset when a Control word is written to a counter. OUT goes to a known initial state; no CLK pulses are required.

2. GATE input is always sampled on the rising edge of CLK. For Modes 0, 2, 3 and 4, GATE input is level sensitive and the logic level is sampled on the rising edge of CLK.

   For Modes 1, 2, 3 and 5, GATE input is rising-edge sensitive. A rising edge of GATE (trigger) sets a flip-flop in the counter that is edge sensitive. The flip-flop is sampled on the next rising edge of CLK and reset immediately after the sampling. A trigger is therefore detected whenever it occurs. A high logic level is not required until the next rising edge of CLK.

3. New counts are loaded and counters are decremented on the falling edge of CLK.

   The counter does not stop when the count reaches zero. In Modes 0, 1, 4 and 5, the counters wraps to the highest count and continues counting. In Modes 2 and 3, the counter reloads itself with the initial count and continues counting.

Programmable Option Select (POS)

The programmable option select (POS) architecture provides an effective means to handle system configuration. This architecture uses programmable registers which can be set by the Power On Self Test (POST) to provide configuration data for the system board and the adapters. POS allows up to eight registers on each adapter to be used for configuration (0100H to 0107H). POS is controlled by two registers in the ACC 5100: the System board enable/setup register (0094H) and the Adapter enable/setup register (0096H). In addition, the ACC 5100 contains POS registers 0100H through 0103H of the system board. Table 15 summarizes the POS registers in the ACC 5100 and the functions of each of these registers is described below. POS control circuitry is also implemented in the ACC 5100.

Table 15 ACC 5100 POS Registers

POS Control Registers	
Address	**Function**
0094	System board setup enable register
0096	Adapter setup enable register

System Board POS Registers	
Address	**Function**
0100	POS Register 0 - system board identification (low byte)
0101	POS Register 1 - system board identification (high byte)
0102	POS Register 2 - system board configuration
0103	POS Register 3 - system board configuration

Procedural guides to set up the POS registers

Setup functions respond to I/O addresses hex 0100 through 0107 only if the unique setup signal is active. The following precautions must be exercised before setting individual bits in the POS
registers.

1. System Board Video Subsystem Setup

   Set Bit 5 in the System Board Enable/ Setup Register (hex 0094) to 0 to put the system board video into the setup mode.

   Set Bit 3 in the Adapter Enable/Setup Register (hex 0096) to 0 to avoid driving a 'setup' signal to an adapter.

   Set Bit 7 in the System Board Enable/ Setup Register (hex 0094) to 1 to avoid driving a 'setup' signal to the system board functions.

2. Adapter Setup

   Set Bit 3 in the Adapter Enable/Setup Register (hex 0096) to 1 to permit adapter setup.

   Set Bit 5 in the System Board Enable/ Setup Register (hex 0094) to 1 to avoid driving a 'setup' signal to the Video Subsystem.

   Set Bit 7 in the System Board Enable/ Setup Register (hex 0094) to 1 to avoid driving a 'setup' signal to a system board function.

3. System Board Setup

   Set Bit 7 in the System Board Enable/ Setup Register (hex 0094) to 0 to permit setup of system board functions.

   Set Bit 3 in the Adapter Enable/Setup Register (hex 0096) to 0 to avoid driving a'setup' signal to an adapter.

   Set Bit 5 in the System Board Enable/ Setup Register (hex 0094) to 1 to avoid driving a 'setup' signal to the Video Subsystem.

After setup operations are complete, the Adapter Enable/Setup Register (hex 0096) must be set to hex 00, and the System Board Enable/Setup Register (hex 0094) must be set to hex FF.

Card Selected Feedback

After an adapter is addressed, it sets the card selected feedback signal (/CDSFDBK) to active. This signal is latched inside the ACC 5100 and can be read through the Card Selected Feedback Register at address hex 0091. Diagnostic programs and automatic configuration programs use this signal to verify an adapter's performance at a given address or DMA port. This signal must be inactive during a setup cycle.

Card Selected Feedback Register (hex 0091)

The Card Selected Feedback Register (hex 0091) is a read only register. Refer to Table 16. Programs can monitor /CDSFDBK through this register and determine if the video subsystem, system board I/O, or an adapter is addressed and functioning.

Table 16 Card Selected Feedback Register (Hex 0091)

Bit	Function
7-1	Unused
0	Card Selected Feedback

Bit 0 When /CDSFDBK was active on a previous cycle, or when the system board I/O functions (diskette drive, serial, or parallel interfaces) are accessed by an I/O cycle, this bit is set to 1. It resets to 0 after a read to the register.

System Board Setup Enable Register

Because the POS registers use the same address locations (0100H to 0107H) to access the system board and each adapter, each adapter must be independently enabled. The System Board Setup-Enable Register provides this function for the system board and the video system.

Table 17 contains the bit definitions for the System Board Setup Enable Register (hex 0094).

Table 17 System Board Setup-Enable Register (Hex 0094)

Bit	Function
7	System board setup-enable
6	Unused
5	Video system setup-enable
4-0	Unused

Bit 7 This bit is active low. When set to 0, it enables the system board setup mode and permits access to system board POS registers (0100H to 0103H). When set to 1, the system board setup mode is disabled. This bit defaults to 1 at system reset.

Bit 5 This bit is active low. When set to 0, it enables the video system setup mode and permits access to video system POS registers. When set to 1, the video system setup mode is disabled. This bit defaults to 1 at system reset.

System Board POS Register 0 (Hex 100)

This register contains system board identification (low byte). When the system board is in setup mode, reading this register returns a value of FF. This is a read only register.

System Board POS Register 1 (Hex 101)

This register contains system board identification (high byte). When the system board is in setup mode, the System Board POS Register 1 (hex 101) identifies the system as either Model 50 or Model 60. FB is returned for Model 50; F7 is returned for Model 60. This is a read-only register.

System Board POS Register 2 (Hex 0102)

When the system board setup mode is enabled, this register can be accessed for system board configuration. It controls the serial and parallel ports, and the floppy disk drive. Refer to Table 18 for bit definitions.

Table 18 System Board POS Register 2 (Hex 0102)

Bit	Function
7	Select parallel port extended mode
6,5	Parallel port select
4	Parallel port enable
3	Serial port select
2	Serial port enable
1	Floppy drive interface enable
0	System board enable

Bit 7 This bit is active low. When set to 0, the parallel port is enabled as a bidirectional interface. When set to 1, the bidirectional mode is disabled. This bit is set to 0 by system reset, then POST sets it to 1.

Bits 6,5

These bits configure the system board parallel port.

Bits 6	5	Select	Hex Address
0	0	Parallel 1	03BC-03BF
0	1	Parallel 2	0378-037B
1	0	Parallel 3	0278-027B
1	1	Unused	

Bit 4 When set to 1, the system board parallel port is enabled. Note that the system board enable (Bit 0) must also be enabled.

Bit 3 This bit configures the system board serial port.

	Select	Hex Address	Active Interrupt
1	Serial 1	03C8-03CC	4
0	Serial 2	02F8-02FF	3

Bit 2 When set to 1, the system board serial port is enabled. Note that the system board enable (Bit 0) must also be enabled.

Bit 1 When set to 1, the floppy disk drive controller is enabled. Note that the system board enable (Bit 0) must also be enabled.

Bit 0 When set to 1, the system board is enabled. This activates the independent enable bits for the serial and parallel ports, and the floppy disk drive (Bits 4,2,1). When set to 0, these devices are disabled regardless of the state of their independent enables.

System Board POS Register 3 (Hex 0103)

When the system board setup mode is enabled, this register can be accessed to enable/disable the system board RAM. Refer to Table 19 for bit definitions.

Table 19 System Board POS Register 3 (Hex 0103)

Bit	Function
7-1	Unused
0	When set to 1, the system board RAM is enabled. When set to 0, the RAM is disabled.

Adapter-Setup Enable Register (0096H)

Because the POS system uses the same address locations (0100H to 0107H) to access the system board, each adapter must be independently enabled. The Adapter-Setup Enable Register (0096H) provides this function for each of the eight available adapters. Refer to Table 20 for bit definitions.

Table 20 Adapter-Setup Enable Register (Hex0096)

Bit	Function
7	Channel reset
6-4	Unused
3	Card setup enable
2-0	Channel/adapter select 2-0

Bit 7 When set to 1, the channel reset signal to all adapters is activated

Bit 3 When set to 1, the card setup signal selected by bits 2 through 0 is enabled.

Bits 2-0

These bits select which of the eight card setup signals (CDSETUP0-7) are activated by card setup enable (Bit 3).

Bits	Channel Selected	Card Setup Signal
2 1 0	Channel 1	CDSETUP0
0 0 0	Channel 2	CDSETUP1
0 0 1	Channel 3	CDSETUP2
0 1 1	Channel 4	CDSETUP3
1 0 0	Channel 5	CDSETUP3
1 0 1	Channel 6	CDSETUP4
1 1 0	Channel 7	CDSETUP6
1 1 1	Channel 8	CDSETUP7

Table 21 contains bit definitions for the video system enable register (Hex 03C3H).

Table 21 Video System Enable Register (Hex 03C3H)

Bit	Function
7-1	Unused
0	Video system enable

Bit 0 When set to 1, the video system is enabled. When set to 0, the video system is disabled.

System Control Registers

The ACC 5100 has two system control registers: Register A (0092H) and Register B (0061H). These registers control a variety of system functions described in Tables 22 and 23.

Table 22 Register A (Hex 0092)

Bit	Function
7,6	Hard disk activity light.
5	Unused
4	Watchdog timer status
3	Security lock latch
2	Unused
1	Alternate A20
0	Hot software reset

Bit 7,6 Hard disk activity light

0 0	Light is OFF
0 1	Light is ON
1 0	Light is ON

Bit 4 Watchdog timer status. A read-only bit which is set to 1 when Timer 3 times out.

Bit 3 Security lock latch. Used to secure eight bytes of RAM space in the Real Time Clock/CMOS RAM (RT/CMOS). Once this bit is set to 1, no further access to RT/CMOS RAM addresses 38-3F is permitted. Once set, this bit can only be cleared by a system reset.

Bit 1 Alternate A20. Enables the address signal A20 when the microprocessor is in the Real address mode. When this bit is set to 0, A20 cannot be used in Real mode addressing. This bit is set to 0 by system reset.

Bit 0 Hot software reset. When this bit is set to 1, the hot software reset pin (HOTSWRES) is pulsed high for a duration of 100 to 125 ns after a delay of 6.72 us.

Table 23 Register B (Hex 0061)

Bit	Function
7	Parity check status (read) Reset IRQ0 (write)
6	Channel check status
5	Timer 2 status
4	Toggle with each refresh request
3	Channel check enable
2	Parity check enable
1	Speaker data enable
0	Timer 2 gate enable

Bit 7 This bit performs two functions depending on whether it is being read or written. When read, it returns parity check status, a 1 indicates that a parity error has occured. When this bit is written to a 1, IRQ0 is reset. Writing a 0 to this bit has no effect.

Bit 6 Channel check status. This bit is read-only. When read, this bit returns channel check status. A 1 indicates a channel check error.

Bit 5 This bit is read-only. When read, it returns a Timer 2 staus. A 1 indicates that Timer 2 has timed out.

Bit 4 This bit is read-only. The state of this bit toggles with each refresh request.

Bit 3 Channel check enable. This bit is active low. When set to 0, it enables channel checking. This bit is set to 1 by a system reset.

Bit 2 Parity check enable. This bit is active low. When set to 0, it enables parity checking. This bit is set to 1 by a system reset.

Bit 1 When this bit is set to 1, it enables speaker data by connecting the Timer 2 output to the SPKR output pin. When this bit is set to 0, speaker data is disabled forcing the SPKR pin to 0 until the bit is enabled again.

Bit 0 This bit controls the Timer 2 gate. When set to 1, counting is enabled on Timer 2. When set to 0, counting is disabled.

Peripheral Device Control

The ACC 5100 provides chip selects to enable several peripheral devices: the floppy disk controller (/CSFDC), the 8042 keyboard controller (/CS8042), the parallel I/O port (/CSPAR), and the serial I/P port (/CSSER).

The ACC 5100 provides several control signals for peripheral devices. These are the IOR and IOW signals which are decoded from CPU status and control signals and then sent to the peripheral devices. The ACC 5100 also provides a control output (/PDSEL) for the ACC 5200 data buffer circuit.

The ATSEL output signal is used to identify the presence of an AT adapter. When a Micro Channel adapter is addressed for setup, it responds with its card selected feedback output. If no response is received, the ACC 5100 assumes that the adapter is an AT type and activates the ATSEL output.

Extended CMOS RAM

The ACC 5100 supports up to 8K x 8 bits of extended CMOS RAM via two address registers at I/O ports hex 74 (low byte) and hex 75 (high byte), and a CMOS RAM chip select which is active for data transfers at I/O port hex 76. The two address registers drive thirteen CMOS RAM address outputs (CMRA0-12). Tables 24 and 25 contain bit definitions for address registers hex 74 and 75.

Table 24 Extended CMOS RAM Low Byte Address Register (Hex 74)

Bit	Function
7	CMRA7
6	CMRA6
5	CMRA5
4	CMRA4
3	CMRA3
2	CMRA2
1	CMRA1

Bits 7-0
These bits drive the corresponding CMOS RAM address outputs.

Table 25 Extended CMOS RAM High Byte Address Register (Hex 75)

Bit	Function
7-5	Unused
4	CMRA12
3	CMRA11
2	CMRA10
1	CMRA9
0	CMRA8

Bits 4-0
These bits drive the corresponding CMOS RAM address outputs.

Real Time Clock/CMOS RAM

The ACC 5100 provides control logic to support the Motorola 146818A real time clock/CMOS RAM circuit (RT/CMOS). When the RT/CMOS address and data registers (hex 0070 and hex 0071) are accessed, the ACC 5100 provides the appropriate Read, Write, and Address strobe signals to the RT/CMOS. A brief description of the RT/CMOS registers and I/O operations follows.

The ACC 5100 provides an NMI mask which can disable the NMI. The NMI mask register is combined with the RT/CMOS address register at address hex 0070. The NMI mask bit Q7 is located inside the ACC 5100.

The RT/CMOS address register and NMI mask (hex 0070) is used in conjunction with the port at hex 0071 to read and write RT/CMOS RAM bytes. Refer to Tables 26 and 27 below.

Table 26 RT/CMOS Address Register and NMI Mask (Hex 0070)

Bit	Function
7	NMI mask. When set to 1, the NMI is masked off (disabled). Bit 7 is set to 1 by a power-on reset and is write-only.
6	Reserved
5-0	Select RT/CMOS RAM addresses

Table 27 RT/CMOS Data Register (Hex 0071)

Bit	Function
7-0	RT/CMOS Data

Warning: the operation following a write to hex 0070 must access port hex 0071 to avoid intermittent malfunctions and faulty operation of the RT/CMOS RAM.

During I/O operations to the RT/CMOS RAM addresses, interrupts must be masked to prevent other interrupt service routines from changing the CMOS address register before reading or writing data.

To perform I/O R/W operations to and from the RT/CMOS RAM addresses, write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register first. Then write or read data to or from address hex 0071.

Keyboard Password

The ACC 5100 supports the Intel 8042 keyboard controller's password security mechanism by providing a "Security lock latch." The security lock latch reserves eight bytes of the RT/CMOS RAM space (address 38-3F) for password storage. After the password is loaded into the security space, it can be locked to prevent further access by setting the security lock latch (Bit 3, system control port A, hex 0092). Once set, the only way to clear this latch is with a hardware reset.

Clock Generators

The ACC 5100 provides clock generation for three system devices: the 80287 math coprocessor (CLK287), the 8042 keyboard controller (CLK8042), and the system serial port (UARTCLK).

Video Tristate Buffers

The ACC 5100 incorporates four video tristate buffers, which are equivalent to a 74LS125, to minimize the number of TTL components required. These buffers are used to disable the on-board video system when an alternate video system is used.

RATING SPECIFICATIONS

Absolute Maximum Ratings*

Parameter	Symbol	Min	Max	Units
Power supply voltage	VCC	-0.5	7.0	V
Power dissipation (@5.25 V)	Wd		TBD	W
Current (@5.25 V)	IDD	TBD	TBD	mA
DC Input voltage	VI	-0.5	7.0	V
Storage temperature	Tstg	-65	150	°C

* Exposing the device to stress above these can cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
DC supply voltage	VCC	4.5	5.5	V
Ambient temperature	Ta	-40	85	°C

Capacitance Limits

TA = +25° C, VCC = 5 V

Parameter	Symbol	Min	Max	Unit	Test Condition
Input capacitance	CI		10	pF	fc = 1 MHz unmeasured pins at GND
I/O capacitance	CIO		15	pF	

DC Specifications

TA = 0° C to +70° C, VCC = +5 V +/- 10%

Input Pins /IOENB, /CHS0, /CHS1, CHM/-IO, /CMD, DLYCLK, /RESET, /INTA, /M60, /IRQ3-15, KYBDINT, AUXINT, /VGASFBK, DMACLK, /CSFBDK0-7, SERINT, /RTCINT, PA0-9, /PARERR, /CHCHK, /REFRESH, EDCLK, DCLKIN, VSYNCIN, HSYNCIN, /BLANKIN, ESYNC, /FDACK, TMODE

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.5 V
Input low current	IIL		-1.0	uA	VIN = 0.0V
Input high current	IIH		1.0	uA	VIN = VCC

I/O Pins PD0-7

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.5 V
Input low current	IIL		-1.0	uA	VIN = 0.0V
Input high current	IIH		1.0	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 4mA
Output high voltage	VOH	2.4		V	IOH = -4mA

I/O Pins XTAL1, XYTAL2

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.5 V
Input low current	IIL		-1.0	uA	VIN = 0.0V
Input high current	IIH		1.0	uA	VIN = VCC
Output low voltage	VOL		0.5	V	IOL = 3.2mA
Output high voltage	VOH	2.4		V	IOH = -3.2mA

Output Pins SPKR, REFREQ, INTR, CLK287, CLK8042, ATSEL, UARTCLK, /IOR, /CDSETUP0-7, /VGASETUP, SELPARX, /CS8042, /CSFDC, /CSPAR, /CSSER, /IOW, /PDSEL, AS6818, /RD6818, WR6818, CMRA0-12, /HDLITE, /CHCHK, /DRAMENB, /NMI, /CSCMR, IORDY, HOTSWRES, ALTA20GATE, VGAENB, /BLANK, DCLK

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 4mA
Output high voltage	VOH	2.4		V	IOH = -4mA

Output Pins HSYNC, VSYNC

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 12mA
Output high voltage	VOH	2.4		V	IOH = -12mA

Output Pins OSC, CHRESET

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 24mA
Output high voltage	VOH	2.4		V	IOH = -24mA

ACC 5200
Data Buffer Logic

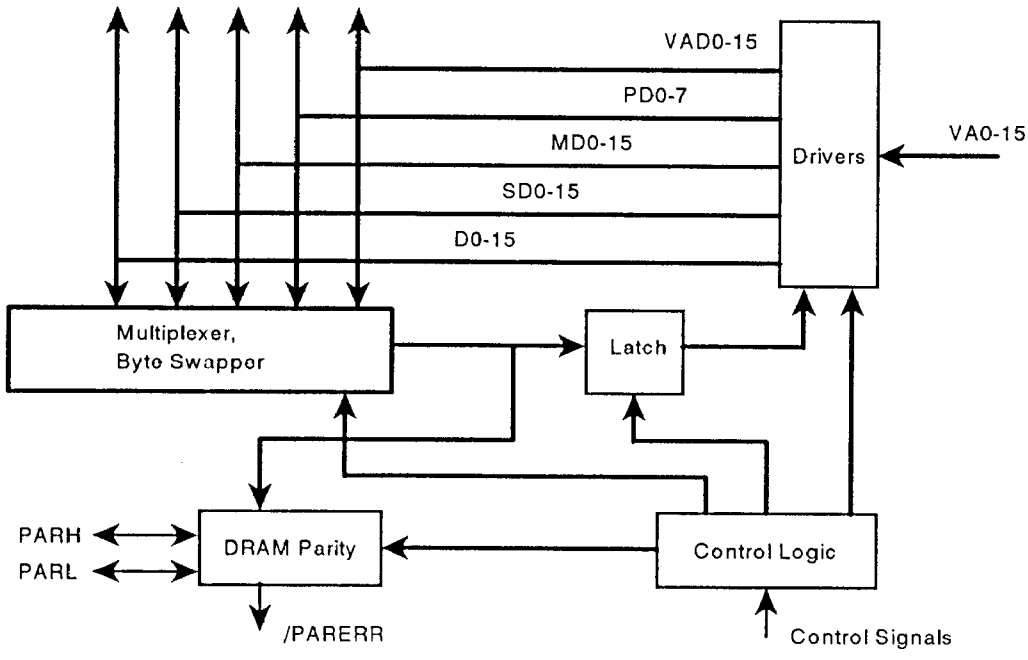
The ACC 5200 is a high performance CMOS device that integrates the data buffers and latches, and glue logic of a Model 50/60 compatible system into a 144-pin flat pack. The ACC 5200 is one of four devices in the ACC 85000 chip set designed to provide 100% PS/2* Model 50/60 compatibility and greater flexibility in building a distinctive high performance Model 50/60 compatible system.

Features

- 100% hardware and software compatible with IBM* PS/2 Model 50/60
- CPU clock rates up to 20 MHz
- Micro Channel* data buffers and latches
- 24 milliamp output drive capability on SD0-15 bus outputs
- Memory parity generation and detection
- Compatible with commericially available VGA interface
- Local bus data latches
- 1.5 micron high performance CMOS technology
- 144-pin PFP package

* Trademarks of International Business Machines

Block Diagram



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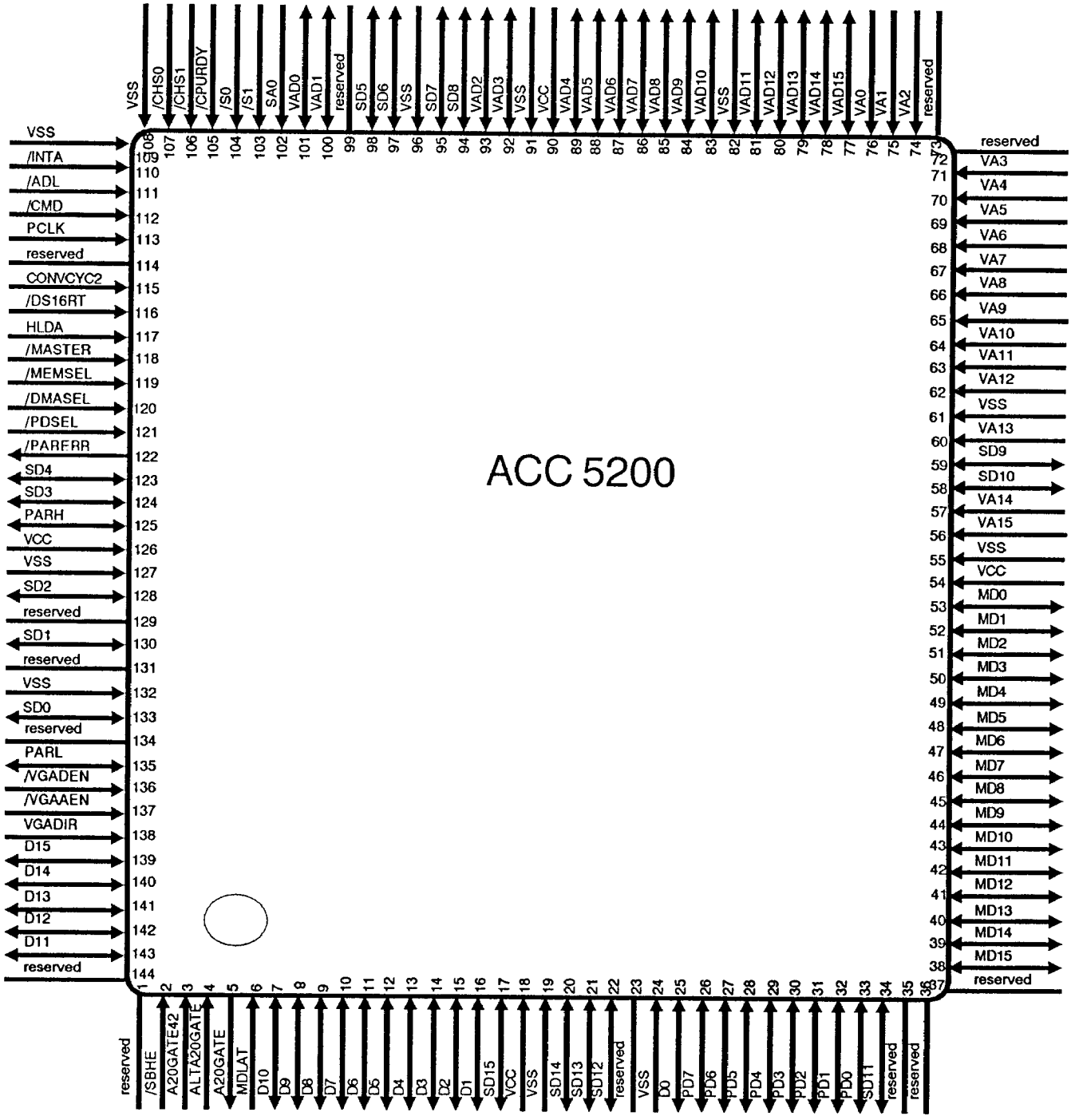
Pin Diagram


ACC 5200
VSS
/CHS0
/CHS1
/CPURDY
/S0
/S1
SA0
VAD0
VAD1
reserved
SD5
SD6
VSS
SD7
SD8
VAD2
VAD3
VSS
VCC
VAD4
VAD5
VAD6
VAD7
VAD8
VAD9
VAD10
VSS
VAD11
VAD12
VAD13
VAD14
VAD15
VA0
VA1
VA2
reserved
VSS
/INTA
/ADL
/CMD
PCLK
reserved
CONVCYC2
/DS16RT
HLDA
/MASTER
/MEMSEL
/DMASEL
/PDSEL
/PARERR
SD4
SD3
PARH
VCC
VSS
SD2
reserved
SD1
reserved
VSS
SD0
reserved
PARL
/VGADEN
/VGAAEN
VGADIR
D15
D14
D13
D12
D11
reserved
reserved
VA3
VA4
VA5
VA6
VA7
VA8
VA9
VA10
VA11
VA12
VSS
VA13
SD9
SD10
VA14
VA15
VSS
VCC
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MD8
MD9
MD10
MD11
MD12
MD13
MD14
MD15
reserved
reserved
/SBHE
A20GATE42
ALTA20GATE
A20GATE
MDLAT
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
SD15
VCC
VSS
SD14
SD13
SD12
reserved
VSS
D0
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0
SD11
reserved
reserved

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/SBHE	2	I	Micro Channel high byte enable.
A20GATE42	3	I	A20 gate signal from 8042.
ALTA20GATE	4	I	Fast A20 gate from the ACC 5100.
A20GATE	5	O	Logical OR of HLDA, A20GATE42 and ALTA20GATE.
MDLAT	6	I	Reserved
D15	139	I/O	CPU Data Bus.
D14	140		
D13	141		
D12	142		
D11	143		
D10	7		
D9	8		
D8	9		
D7	10		
D6	11		
D5	12		
D4	13		
D3	14		
D2	15		
D1	16		
D0	25		
SD15	17	I/O	Micro Channel Data Bus.
SD14	20		
SD13	21		
SD12	22		
SD11	34		
SD10	58		
SD9	59		
SD8	94		
SD7	95		
SD6	97		
SD5	98		
SD4	123		
SD3	124		
SD2	128		
SD1	130		
SD0	133		

Pin Descriptions

Symbol	Pin	I/O	Pin Description
PD7	26	I/O	Peripheral Data Bus.
PD6	27		
PD5	28		
PD4	29		
PD3	30		
PD2	31		
PD1	32		
PD0	33		
MD15	38	I/O	Memory Data Bus.
MD14	39		
MD13	40		
MD12	41		
MD11	42		
MD10	43		
MD9	44		
MD8	45		
MD7	46		
MD6	47		
MD5	48		
MD4	49		
MD3	50		
MD2	51		
MD1	52		
MD0	53		
VA15	56	I	Video Address Bus (normally connected to SA0-15).
VA14	57		
VA13	60		
VA12	62		
VA11	63		
VA10	64		
VA9	65		
VA8	66		
VA7	67		
VA6	68		
VA5	69		
VA4	70		
VA3	71		
VA2	74		
VA1	75		
VA0	76		
SA0	102	I	Micro Channel address Bit 0.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/S1	103	I	Status bit from CPU or ACC 5000.
/S0	104		
VAD15	77	I/O	Address/Data Bus for VGA chip.
VAD14	78		
VAD13	79		
VAD12	80		
VAD11	81		
VAD10	83		
VAD9	84		
VAD8	85		
VAD7	86		
VAD6	87		
VAD5	88		
VAD4	89		
VAD3	92		
VAD2	93		
VAD1	100		
VAD0	101		
/CPURDY	105	I	Processor ready signal.
/CHS1	106	I	Micro Channel status bit.
/CHS0	107		
/INTA	110	I	Interrupt acknowledge input from ACC 5000.
/ADL	111	I	Micro Channel address latch signal.
/CMD	112	I	Micro Channel command strobe.
PCLK	113	I	Processor cycle clock.
CONVCYC2	115	I	Signal from ACC 5000 indicates second byte of two-byte conversion cycle.
/DS16RT	116	I	Data size 16-bit return from bus.
HLDA	117	I	Hold Acknowledge from CPU. Indicates that the Micro Channel is being driven by DMA or another master.
/MASTER	118	I	Signals that an off-board master is controlling the Micro Channel.
/MEMSEL	119	I	Active when on-board DRAM or EPROM is selected.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/DMASEL	120	I	Signal from ACC 5000, indicates that data on the PD bus is selected.
/PDSEL	121	I	Signal from ACC 5100, indicates that DMA or NPU (including 387SX) is selected.
/PARERR	122	O	Memory parity error output.
PARH	125	I/O	Memory Parity Data.
PARL	135	I/O	Memory Parity Data.
/VGADEN	136	I	Data enable for VAD0-15 bus.
/VGAAEN	137	I	Address enable for VAD0-15 bus.
VGADIR	138	I	Direction indication for VAD0-15. VGADIR high indicates a data read from the VGA chip.
VCC	18, 54, 90, 126		+5 volt supply
VSS	19, 24, 55, 61, 82, 91, 96, 108, 109, 127, 132		Ground
reserved	1, 23, 35, 36, 37, 72, 73, 99, 114, 129, 131, 134, 144		

Functional Description

The ACC 5200 data buffer controls the data flow between all the bus lines on the system board.

- CPU Bus (D BUS)
- Micro Channel Bus (SD BUS)
- Memory Bus (MD BUS)
- Peripheral Bus (PD BUS)
- Video Bus (VAD BUS)

Control Logic

The direction of data flow is controlled by the control logic. The video address bus is also connected to the video bus through this logic.

Multiplexer, Byte Swapper

The byte swapper logic transfers data between 16-bit and 8-bit bus lines. When data is written from a 16-bit bus to an 8-bit bus, two consecutive 8-bit write operations are performed. When data is read from an 8-bit bus to a 16-bit bus, the lower 8-bit data is latched first and read at the same time the higher 8-bit is transferred.

DRAM Parity

The parity generation and checking scheme for data integrity is an ODD parity scheme. If the number of "ones" in the combined data and parity is even, a parity error occurs.

Latch

Latch input comes from the multiplexer which has selected one of the data buses for input. Latch output is sent back to the bus selected by the control logic.

Drivers

Drivers provide interface to external bus lines.

Rating Specifications

Absolute Maximum Ratings*

Parameter	Symbol	Min	Max	Units
Power supply voltage	VCC	-0.3	7.0	V
Power dissipation (@5.25 V)	Wd		TBD	W
Current (@5.25 V)	IDD	TBD	TBD	mA
DC Input voltage	VI	-0.3	7.0	V
Storage temperature	Tstg	-40	125	°C

* Exposing the device to stress above these can cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
DC supply voltage	VCC	4.75	5.25	V
Ambient temperature	Ta	0	70	°C

Capacitance Limits

TA = +25° C, VCC = 5 V

Parameter	Symbol	Min	Max	Unit	Test Condition
Input capacitance	CI		10	pF	fc = 1 MHz unmeasured pins at GND
I/O capacitance	CIO		15	pF	

DC Specifications

TA = 0° C to +70° C, VCC = +5 V +/- 5%

Pins A20GATE42, ALTA20GATE, MDLAT, VA0-15, SA0, /S0, /S1, /CHS0, /CHS1, /INTA, /ADL, /CMD, PCLK, CONVCYC2, /DS16RT, HLDA, /MASTER, /MEMSEL, /DMASEL, /PDSEL, /VGADEN, /VGAAEN, VGADIR

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.25 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.25 V
Input low current	IIL	-10	10	uA	VIN = 0.0V
Input high current	IIH	-10	10	uA	VIN = VCC

Pins D0-15, PD0-7, MD0-15, VAD0-15, PARH, PARL

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.25 V
Input high voltage	VIH	2.0	-	V	VCC = 5 +/- 0.25 V
Input low current	IIL	-10	10	uA	VIN = 0.0V
Input high current	IIH	-10	10	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 6mA
Output high voltage	VOH	2.4		V	IOH = -6mA

Pins SD0-15

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.25 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.25 V
Input low current	IIL	-10	10	uA	VIN = 0.0V
Input high current	IIH	-10	10	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 24mA
Output high voltage	VOH	2.4		V	IOH = -24mA

Pins A20GATE, /PARERR

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 6mA
Output high voltage	VOH	2.4		V	IOH = -6mA

ACC 5300
Memory Controller and Buffers

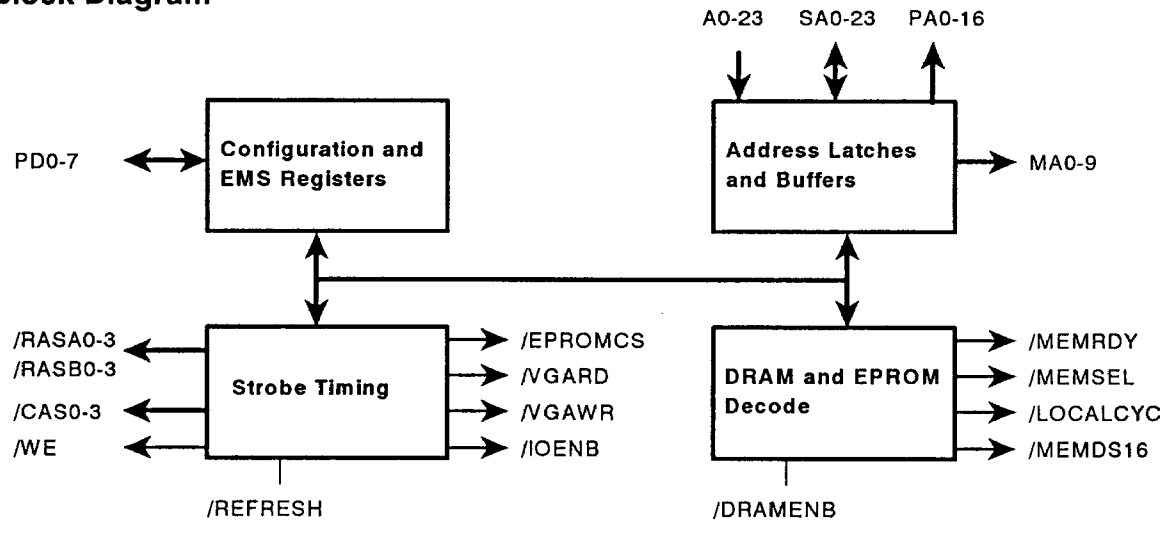
The ACC 5300 is a high performance CMOS device that integrates the memory controller and memory buffers and latches of a Model 50/60 compatible system into a 144-pin flat pack. The ACC 5200 is one of four devices in the ACC 85000 chip set designed to provide 100% PS/2* Model 50/60 compatibility and greater flexibility in building a distinctive high performance Model 50/60 compatible system.

Features

- 100% hardware and software compatible with the IBM* PS/2 Model 50/60
- Micro Channel* address buffers and control latches
- EPROM and DRAM control logic
- Refresh logic
- Supports 256K x 1, 256K x 4, 1M x 1, and 1M x 4
- Supports up to 16 MB of on-board RAM
- Supports shadow RAM
- Supports EMS 4.0
- 1.5 micron high performance CMOS technology
- 144-pin PFP package

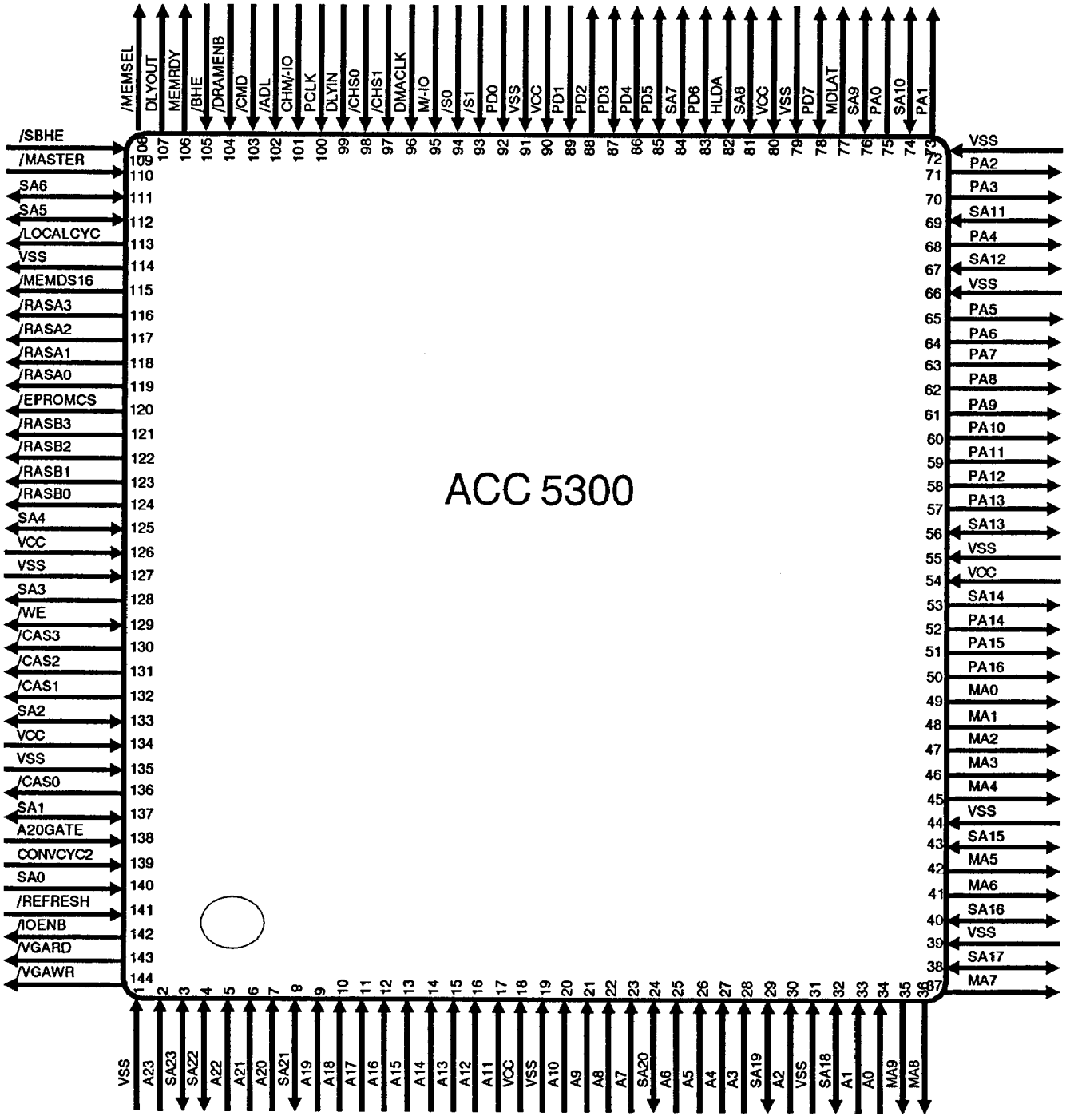
* Trademarks of International Business Machines

Block Diagram



ACC Microelectronics Corporation · 3295 Scott Blvd. · Santa Clara, CA 95054
Phone: 408-980-0622 FAX: 408-980-0626

Pin Diagram


ACC 5300
/SBHE
/MASTER
SA6
SA5
/LOCALCYC
VSS
/MEMDS16
/RASA3
/RASA2
/RASA1
/RASA0
/EPROMCS
/RASB3
/RASB2
/RASB1
/RASB0
SA4
VCC
VSS
SA3
/WE
/CAS3
/CAS2
/CAS1
SA2
VCC
VSS
/CAS0
SA1
A20GATE
CONVCYC2
SA0
/REFRESH
/IOENB
/VGARD
/VGAWR
/MEMSEL
DLYOUT
MEMRDY
/BHE
/DRAMENB
/CMD
/ADL
CHM/-IO
PCLK
DLYIN
/CHS0
/CHS1
DMACLK
M/-IO
/S0
/S1
PD0
VSS
VCC
PD1
PD2
PD3
PD4
PD5
SA7
PD6
HLDA
SA8
VCC
VSS
PD7
MDLAT
SA9
PA0
SA10
PA1
VSS
PA2
PA3
SA11
PA4
SA12
VSS
PA5
PA6
PA7
PA8
PA9
PA10
PA11
PA12
PA13
SA13
VSS
VCC
SA14
PA14
PA15
PA16
MA0
MA1
MA2
MA3
MA4
VSS
SA15
MA5
MA6
SA16
VSS
SA17
MA7
VSS
A23
SA23
SA22
A22
A21
A20
SA21
A19
A18
A17
A16
A15
A14
A13
A12
A11
VCC
VSS
A10
A9
A8
A7
SA20
A6
A5
A4
A3
SA19
A2
VSS
SA18
A1
A0
MA9
MA8

Pin Descriptions

Symbol	Pin	I/O	Pin Description
A23	2	I	CPU Address Bus.
A22	5		
A21	6		
A20	7		
A19	9		
A18	10		
A17	11		
A16	12		
A15	13		
A14	14		
A13	15		
A12	16		
A11	17		
A10	20		
A9	21		
A8	22		
A7	23		
A6	25		
A5	26		
A4	27		
A3	28		
A2	30		
A1	33		
A0	34		
PA16	50	O	Latched peripheral address bus for peripherals and EPROM.
PA15	51		
PA14	52		
PA13	57		
PA12	58		
PA11	59		
PA10	60		
PA9	61		
PA8	62		
PA7	63		
PA6	64		
PA5	65		
PA4	68		
PA3	70		
PA2	71		
PA1	73		
PA0	75		

Pin Descriptions

Symbol	Pin	I/O	Pin Description
MA9	35	O	Multiplexed address line for DRAM.
MA8	36		
MA7	37		
MA6	41		
MA5	42		
MA4	45		
MA3	46		
MA2	47		
MA1	48		
MA0	49		
SA23	3	I/O	Micro Channel Address Bus (24ma sink).
SA22	4		
SA21	8		
SA20	24		
SA19	29		
SA18	32		
SA17	38		
SA16	40		
SA15	43		
SA14	53		
SA13	56		
SA12	67		
SA11	69		
SA10	74		
SA9	76		
SA8	81		
SA7	84		
SA6	111		
SA5	112		
SA4	125		
SA3	128		
SA2	133		
SA1	137		
SA0	140		
MDLAT	77	O	Reserved.
PD7	78	I/O	Data bus used to access configuration registers inside the ACC 5300.
PD6	83		
PD5	85		
PD4	86		
PD3	87		
PD2	88		
PD1	89		
PD0	92		

Pin Descriptions

Symbol	Pin	I/O	Pin Description
HLDA	82	I	Hold acknowledge from CPU. Indicates that the Micro Channel is being driven by DMA or other master.
/S1 /S0	93 94	I	CPU or DMA status signal.
M/-IO	95	I	Indicates Memory or I/O selected.
DMACLK	96	I	DMA/Micro Channel 20 MHz clock.
/CHS1 /CHS0	97 98	I	Micro Channel status signal.
DLYIN	99	I	Input from delay line.
PCLK	100	I	Processor clock input.
CHM/-IO	101	I	Micro Channel memory/IO select signal.
/ADL	102	I	Micro Channel address latch signal.
/CMD	103	I	Micro Channel command strobe.
/DRAMENB	104	I	Input enables ACC 5300 control of on-board DRAM.
/BHE	105	I	Byte high enable.
MEMRDY	106	O	Ready signal for DRAM and EPROM access.
DLYOUT	107	O	Output drives two-tapped delay line.
/MEMSEL	108	O	Indicates that DRAM or EPROM is selected.
/SBHE	109	I	Micro Channel high byte enable.
/MASTER	110	I	Signal indicates that the Micro Channel is controlled by an adapter card.
/LOCALCYC	113	O	Signals that current CPU cycle does not require the Micro Channel.
/MEMDS16	115	O	Signal indicates that the DRAM or EPROM is selected and is capable of a 16-bit transfer. Always true for the EPROM, and is true for DRAM unless only one module is plugged in.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/RASA3 /RASA2 /RASA1 /RASA0	116 117 118 119	O	DRAM /RAS signal.
/EPROMCS	120	O	Output enable for 27512 EPROMs.
/RASB3 /RASB2 /RASB1 /RASB0	121 122 123 124	O	DRAM /RAS signal.
/WE	129	O	DRAM write enable.
/CAS3 /CAS2 /CAS1 /CAS0	130 131 132 136	O	DRAM /CAS signal.
A20GATE	138	I	Signal from 8042 enables A20.
CONVCYC2	139	I	Signal goes active during the second byte of a word/byte conversion cycle.
/REFRESH	141	I	Indicates the current Micro Channel cycle is DRAM refresh.
/IOENB	142	O	Enables I/O decoding on motherboard. When /MASTER is active, /IOENB does not go active for any I/O address below 100H.
/VGARD	143	O	Read strobe for VGA chip.
/VGAWR	144	O	Write strobe for VGA chip.
VCC	18, 54, 80, 90, 126, 134,		+5 volt supply
VSS	1, 19, 31, 39, 44, 55, 66, 72, 79, 91, 114, 127, 135		Ground

Functional Description

Configuration and EMS Registers

All programmable options of the ACC 85000 chip set are controlled by software accesses to configuration registers present inside the individual chips. All chips in the ACC 85000 chip set have these configuration registers except for the ACC 5200.

Registers are accessed through I/O ports 22H and 23H. The procedure is to write a register number to 22H, then read or write the actual register data at port 23H. Address space has been provided for 64 configuration registers. Address allocation between the chips is indicated below.

Chip	Register Numbers Allocated
ACC 5000	00H - 0FH
ACC 5100	10H - 1FH
ACC 5300	20H - 3FH

Not all of the allocated registers are actually used. The registers used in the ACC 5300 are shown in Figure 1. All unused register bits must be considered as reserved. When writing, write them to zero.

	7	6	5	4	3	2	1	0
20H		MAP ENB	SHAD RD	SHAD WR	1 MEG	DRAM SIZE		
21H	ECHSP				DCHSP	DTIM OPT	DRAM MODE	
22H							EMS ENB	VGA IO
23H	EMS REG 3 8, 9		EMS REG 2 8, 9		EMS REG 1 8, 9		EMS REG 0 8, 9	
24H	EMS REG 0 0-7							
25H	EMS REG 1 0-7							
26H	EMS REG 2 0-7							
27H	EMS REG 3 0-7							

Figure 1 Configuration Registers

Configuration Register Descriptions

DRAM SIZE

			Number of 9-bit DRAM modules installed
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	12
1	0	1	16
1	1	X	Reserved

ONE MEG

Bit = 1 indicates 1 Megabit DRAM chips are used.
Bit = 0 indicates 256Kbit DRAM chips.

For 1 Megabit chips, a maximum of 16 megabytes can be addressed. For 256k bit chips, 4 megabytes is the maximum.

SHAD WR
SHAD RD

Bits work together to control the Shadow RAM feature. Initially, both bits are set to zero for normal EPROM operation. To activate the Shadow RAM feature, set SHADOW WR to 1. In this mode the EPROM can be copied into RAM using a block move instruction. After copying is finished, make SHADOW WR = 0 and SHADOW RD = 1 to enable the Shadow RAM in read-only mode.

MAP ENB

When this bit is 1, the upper 384K of the first megabyte of DRAM is remapped contiguously above the highest non-mapped DRAM. If Shadow RAM is enabled, only 256K of DRAM is available for re-mapping. If MAP ENB = 0, this DRAM is not used.

DRAM MODE

Chooses one of three possible modes for CPU DRAM accesses. Micro Channel and DMA RAM accesses are not affected by these bits.

0 0	Direct access. No paging, no wait states.
0 1	Paged access. No wait states for page hit, one wait state for page miss.
1 0	Page/interleaved access. No wait states for page hit, one wait state for interleaved miss, two wait states for non-interleaved miss.

Refer to the table below for the DRAM speed required for all possible combinations of DRAM MODE and CPU speed.

	10	12.5	16	20MHz
Direct	100ns	80ns	--	--
Paged	120ns	100ns*	80ns	--
Pg/Inter.	150ns	150ns	120ns	80ns

* 100ns fast page or 85ns

DTIM OPT

This bit must be set to 1 if Paged access is selected for 16 MHz operation with 80ns DRAM. In this case, the leading edge of /RAS starts earlier to meet the DRAM tRAC specification. This bit has no effect in any other access mode.

DCHSP

This bit controls DRAM timing for Micro Channel and DMA operations. DCHSP must be 0 for no wait state operation, and 1 for one wait state. For no wait state operation, the DRAM chips must be either 85ns, or 100ns fast page types.

ECHSP

Bit controls EPROM timing. ECHSP is set to 0 for one wait state operation, or set to 1 for two wait states. For one wait state, the EPROM or ROM chips must have 170ns or less access time. For two wait states, EPROM or ROM chips as slow as 250ns can be used.

VGA IO

This bit is set to a 1 if the on-board VGA chip uses a common set of /RD and /WR strobes for VGA I/O and Memory access. In this case, /VGARD and /VGAWR are connected directly to the VGA chip's /RD and /WR pins. VGA IO is set to 0 for VGA chips which have separate strobes for Memory and I/O accesses. In that case, /VGARD and /VGAWR connect to the VGA chip's /MEMR and /MEMW pins.

EMS ENB

Bit enables EMS address translation when it equals 1.

EMS REG

Configuration registers 23H through 27H are EMS translation page registers. Four 10-bit page registers are mapped into five 8-bit registers on the ACC 5300. When addresses D0000 through DFFFF are accessed and EMS ENB is one, address bits 14 through 23 are replaced with the contents of one of these page registers.

EMS Register	Address Range
0	D0000 - D3FFF
1	D4000 - D7FFF
2	D8000 - DBFFF
3	DC000 - DFFFF

In addition to the configuration registers described above, the ACC 5300 maintains a copy of Register 0 bit 0, which indicates when the ACC 85000 system is in turbo mode. Register 0 bit 0 is updated in the ACC 5300 every time the CPU writes to the same register in the ACC 5000. If turbo mode is not selected, all DRAM accesses are performed through the Micro Channel and bypass the DRAM MODE selected.

Address Latches and Buffers

The A0-A23 signals from the 80286 CPU or ACC 5000 are buffered and latched in the ACC 5300 to generate the Micro Channel SA0-SA23 signals. These outputs sink 24 ma for direct connection to the Micro Channel. Latch timing assures that SA0-SA23 do not change sooner than 50ns before the end of /CMD. The ACC 5300 tri-states the SA0-SA23 outputs when /MASTER is active so another master can drive the Micro Channel.

EMS address translation is performed between A0-A23 and SA0-SA23. This means that the EMS translation in the ACC 5300 can be used with non-EMS memory extension boards on the Micro Channel.

SA0-SA16 are latched further in the ACC 5300 to form PA0-PA16 signals which are used by peripheral chips and EPROMs in the ACC 85000 system. These signals follow SA0-SA16 when /ADL is active.

MA0-MA9 are the multiplexed address lines for the DRAM chips. Multiplexer timing is compatible with the ACC 5300's /RAS and /CAS output strobes. In the case of DRAM remapping, MA0-MA9 outputs are modified to reflect the address translation. In DRAM systems consisting of four modules or less, these signals can be connected directly without external buffering. Larger systems require TTL buffering.

DRAM Strobe Timing

The ACC 5300 provides eight /RAS and four /CAS output signals. For the maximum DRAM configuration, this provides one /RAS for each two modules and one /CAS for each four modules. Figure 2 shows how these signals are connected. In this configuration, external TTL buffers are required for the /RAS and /CAS lines.

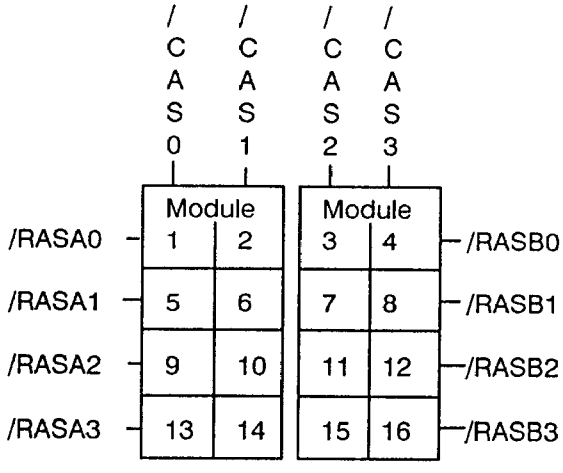


Figure 2 Connection for up to 16 DRAM Modules

If 1, 2 or 4 DRAM modules are configured, they are connected differently. Refer to Figure 3 below.

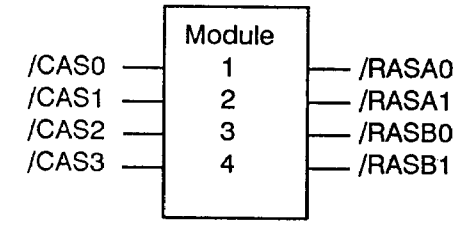


Figure 3 Connection for 4 DRAM Modules

No TTL buffering is required for the configuration in Figure 3. If on-board DRAM is expandable to more than four DRAM modules, use the connection scheme shown in Figure 1.

Staggered refresh is supported for any configuration with more than four DRAM modules. The staggered refresh operation uses 2 wait states, and the /RAS strobes are broken up into 4 groups, separated from each other by 25ns. Only 1 wait state is required for a standard refresh operation.

DRAM and EPROM Decode

DRAM and EPROM decode logic (based on information in the configuration registers) determines when DRAM or EPROM is being accessed on the motherboard. The major output signals are /EPROMCS, /LOCALCYC, /MEMSEL and /MEMDS16.

/EPROMCS goes active in response to a read from addresses 0E0000 - 0F0000 or FE0000 - FFFFFF. If SHAD RD is 1, /EPROMCS is disabled, and DRAM is read from instead.

/LOCALCYC is active for any cycle that does not require the Micro Channel. This situation only occurs for on-board DRAM accesses in turbo mode, and for accesses to an 80387SX NPU. If only one DRAM module is configured,

all DRAM accesses are performed through the Micro Channel. This procedure allows the built in Micro Channel byte swap and cycle conversion logic to make 8-bit DRAM look like 16-bit DRAM to the 80286 CPU. In another special case, when SHAD WR is 1 and SHAD RD is 0, Shadow RAM write is performed throuugh the Micro Channel. /LOCALCYC is also forced off for DMA cycles or non-turbo mode cycles.

/MEMSEL is active for EPROM or DRAM accesses. /MEMDS16 is also active, except when one DRAM module is installed. In that case, /MEMDS16 does not go active for any DRAM cycle.

Rating Specifications

Absolute Maximum Ratings*

Parameter	Symbol	Min	Max	Units
Power supply voltage	VCC	-0.3	7.0	V
Power dissipation (@5.25 V)	Wd		TBD	W
Current (@5.25 V)	IDD	TBD	TBD	mA
DC Input voltage	VI	-0.3	7.0	V
Storage temperature	Tstg	-40	125	°C

* Exposing the device to stress above these can cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
DC supply voltage	VCC	4.75	5.25	V
Ambient temperature	Ta	0	70	°C

Capacitance Limits

TA = +25° C, VCC = 5 V

Parameter	Symbol	Min	Max	Unit	Test Condition
Input capacitance	CI		10	pF	fc = 1 MHz unmeasured pins at GND
I/O capacitance	CIO		15	pF	

DC Specifications

TA = 0° C to +70° C, VCC = +5 V +/- 5%

Pins A0-23, HLDA, /S0, /S1, M/-IO, /CHS0, /CHS1, DLYIN, CHM/-IO, /ADL, /CMD, /DRAMENB, /BHE, /SBHE, /MASTER, A20GATE, CONVCYC2, /REFRESH

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.25 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.25 V
Input low current	IIL	-10	10	uA	VIN = 0.0V
Input high current	IIH	-10	10	uA	VIN = VCC

Pins PD0-7. DLYOUT

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.25 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.25 V
Input low current	IIL	-200	-10	uA	VIN = 0.0V
Input high current	IIH	-10	10	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 3mA
Output high voltage	VOH	2.4		V	IOH = -3mA

Pins SA0-SA23

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.5 V
Input low current	IIL	-200	10	uA	VIN = 0.0V
Input high current	IIH	-10	10	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 24mA
Output high voltage	VOH	2.4		V	IOH = -24mA

Pins MA0-9, PA0-16, MDLAT, MEMRDY, /MEMSEL, /LOCALCYC, /MEMDS16, /WE, /RASA0-3, /EPROMCS, /RASB0-3, /CAS0-3, /IOENB, /VGARD, /VGAWR

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 3mA
Output high voltage	VOH	2.4		V	IOH = -3mA