ACC 83000
Model 30 Integrated Chip Set

The ACC 83000 chip set is designed for system designers to build 100% compatible IBM PS/2 Model 30* systems. The ACC 83000 contains two VLSI chips.

The ACC 3100 provides system control signals, and the ACC 3000 is the I/O controller.

The ACC 83000 supports a local CPU bus, a system memory bus, and compatible Model 30 buses. The system clock generates 24, 8 and 1.84 MHz clock timing. Up to eight I/O channel interrupts with sharing capability are available with variable wait states.

Features

- 100% IBM PS/2 Model 30 system support gate array pin to pin compatible
- 100% IBM PS/2 Model 30 I/O support gate array pin to pin compatible
- Bus and memory controllers
- Supports up to 8 channel interrupts with sharing capability
- Wait state generator
- System clock
- Built-in mouse and keyboard interface
- Decoder and data bus controller
- NMI control and peripheral logic
- Parallel port control
- 1.5 micron high performance CMOS technology
- 84-L PLCC package

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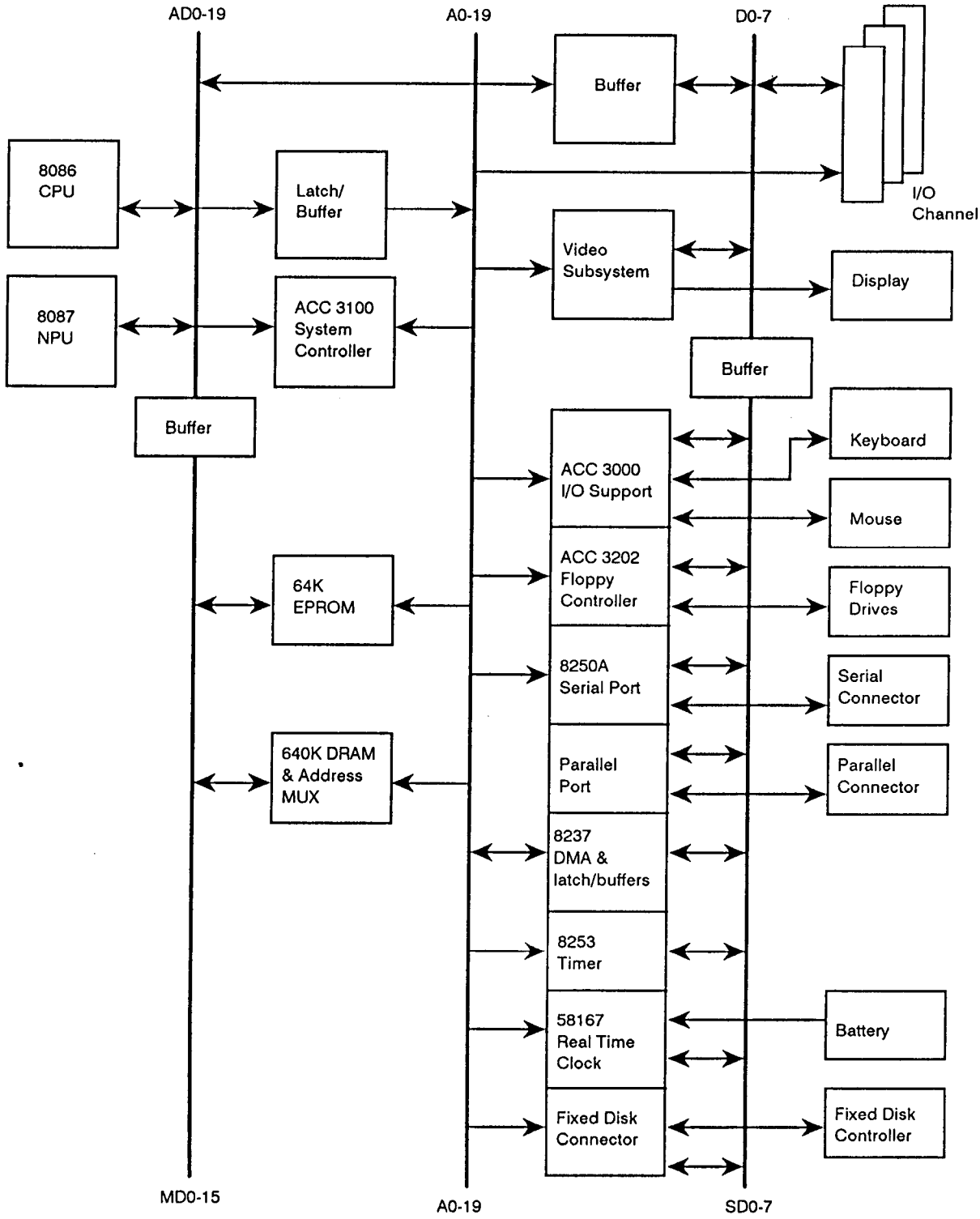
ACC 83000 System Block Diagram



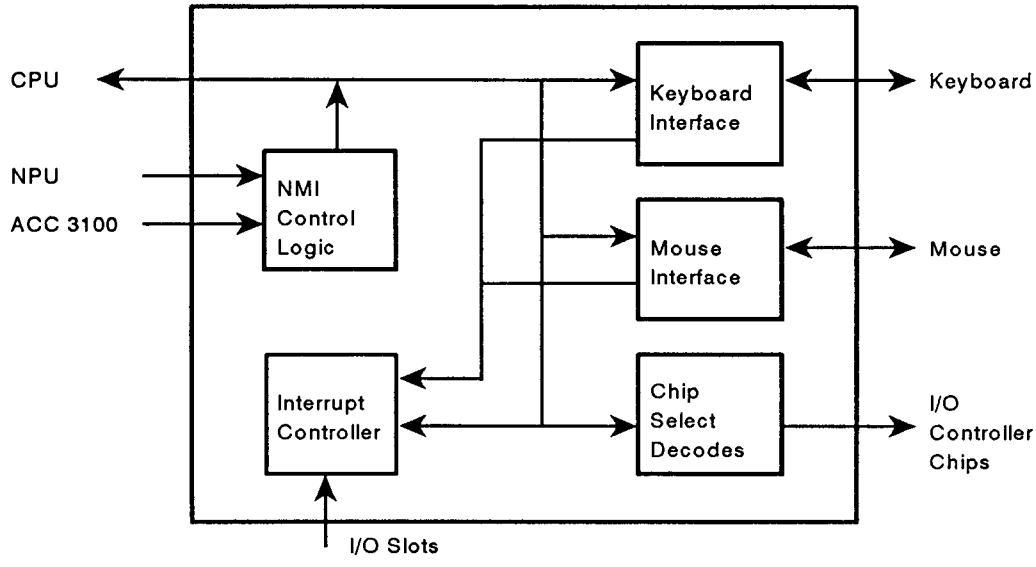
ACC 3000
Model 30 I/O Controller

The ACC 3000 is a VLSI device that emulates the I/O Support Gate Array of the IBM PS/2 Model 30. This chip is designed to help system designers build a Model 30 compatible machine at a lower cost with a faster design cycle.

Features

- 100% IBM Model 30 I/O support gate array pin-to-pin compatible
- Controls the following chip select signals:
  - Serial port
  - Diskette controller
  - Video controller
  - Parallel port
  - Fixed disk controller
  - Real-time clock
- NMI control logic
- Peripheral sense logic and control
- Built-in Model 30 keyboard and pointing device interface
- Supports up to 8 channel interrupts with sharing capability
- Provides parallel port control signals
- Decoder & Data Bus controller
- 1.5 micron high performance CMOS technology
- 84-L PLCC package

Block Diagram



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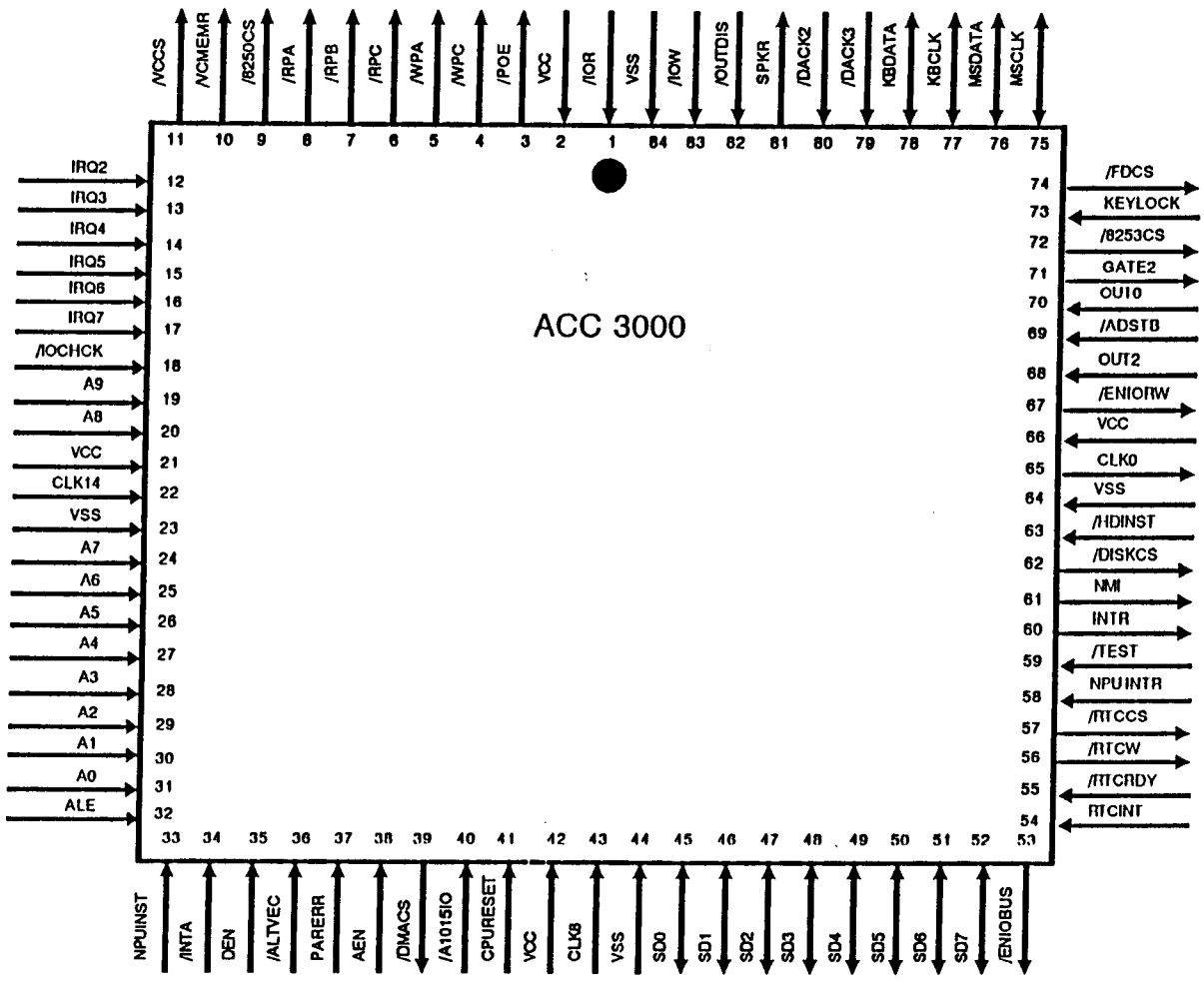
Pin Diagram


ACC 3000
/VCCS 11
/VCMEMR 10
/8250CS 9
/RPA 8
/RPB 7
/RPC 6
/WPA 5
/WPC 4
/POE 3
VCC 2
/IOR 1
VSS 84
/IOW 83
/OUTDIS 82
SPKR 81
/DACK2 80
/DACK3 79
KBDATA 78
KBCLK 77
MSDATA 76
MSCLK 75
IRQ2 12
IRQ3 13
IRQ4 14
IRQ5 15
IRQ6 16
IRQ7 17
/IOCHCK 18
A9 19
A8 20
VCC 21
CLK14 22
VSS 23
A7 24
A6 25
A5 26
A4 27
A3 28
A2 29
A1 30
A0 31
ALE 32
/FDCS 74
KEYLOCK 73
/8253CS 72
GATE2 71
OUT0 70
/ADSTB 69
OUT2 68
/ENIORW 67
VCC 66
CLK0 65
VSS 64
/HDINST 63
/DISKCS 62
NMI 61
INTR 60
/TEST 59
NPUINTR 58
/RTCCS 57
/RTCW 56
/RTCRDY 55
RTCINT 54
NPUINST 33
/INTA 34
DEN 35
/ALTVEC 36
PARERR 37
AEN 38
/DMACS 39
/A1015IO 40
CPURESET 41
VCC 42
CLK8 43
VSS 44
SD0 45
SD1 46
SD2 47
SD3 48
SD4 49
SD5 50
SD6 51
SD7 52
/ENIOBUS 53

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/IOR	1	I	I/O Read from 8288 bus controller
/POE	3	O	Parallel Port Enable
/WPC	4	O	Write to Parallel Port C
/WPA	5	O	Write to Parallel Port A
/RPC	6	O	Read Parallel Port C
/RPB	7	O	Read Parallel Port B
/RPA	8	O	Read Parallel Port A
/8250CS	9	O	Chip Select for 8250
/VCMEMR	10	O	Video Controller Memory Read/Write Enable
/VCCS	11	O	Video Controller Chip Select
IRQ2	12	I	Interrupt Request
IRQ3	13	I	
IRQ4	14	I	
IRQ5	15	I	
IRQ6	16	I	
IRQ7	17	I	
/IOCHCK	18	I	I/O Channel Check
A9	19	I	Address Bus bit
A8	20		
A7	24		
A6	25		
A5	26		
A4	27		
A3	28		
A2	29		
A1	30		
A0	31		
CLK14	22	I	14.318 MHz Clock Input. This signal is divided by twelve internally and is used as the timing reference for the keyboard and mouse.
ALE	32	I	Address Latch Enable

Pin Description

Symbol	Pin I/O	Pin Description
NPUINST	33	I	Numerical Processor Unit Installation
/INTA	34	I	Interrupt Acknowledge
DEN	35	I	Data Enable
/ALTVEC	36	I	When this pin is low, the interrupt vector for IRQ1 changes from 71H to 70H. This pin has a built-in resistor. There is no connection to the Model 30 board.
PARERR	37	I	Parity Error
AEN	38	I	Address Enable
/DMACS	39	O	DMA Chip Select
/A1015IO	40	I	Memory I/O Indication
CPURESET	41	I	CPU-Reset
CLK8	43	I	8 MHz Clock Input (System Clock)
SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7	45 46 47 48 49 50 51 52	I/O	System Data BUS bit.
/ENIOBUS	53	O	Enable I/O Bus
RTCINT	54	I	Real Time Clock Interrupt
/RTCRDY	55	I	Real Time Clock Ready
/RTCW	56	O	Real Time Clock Write
/RTCCS	57	O	Real Time Clock Chip Select
NPUINTR	58	I	Numerical Processor Unit Interrupt
/TEST	59	I	Numerical Processor Installed when set to 0
INTR	60	O	Interrupt Request To CPU

Pin Descriptions

Symbol	Pin	I/O	Pin Description
NMI	61	O	Non Maskable Interrupt to CPU
/DISKCS	62	O	Hard Disk Chip Select
/HDINST	63	I	Hard Disk Installation
CLK0	65	O	1.19 MHz Output Timer Clock. (Resulting output from Pin 22 after the signal has been divided by twelve internally)
/ENIORW	67	O	Enable I/O Read Write
OUT0	70	I	8253 Channel 0
OUT2	68	I	8253 Channel 2
/ADSTB	69	I	Address Strobe
GATE2	71	O	8253 Gate 2
/8253CS	72	O	8253 Chip Select
KEYLOCK	73	I	Keylock
/FDCS	74	O	Floppy Disk Chip Select
MSCLK	75	I/O	Mouse Port Clock Input/Output
MSDATA	76	I/O	Mouse Port Data Input/Output
KBCLK	77	I/O	Keyboard Port Clock Input/Output
KBDATA	78	I/O	Keyboard Port Data Input/Output
/DACK2	80	I	DMA Acknowledge 2
/DACK3	79	I	DMA Acknowledge 3
SPKR	81	O	Speaker output.
/OUTDIS	82	I	When low, all output pins are disabled to facilitate on-board chip testing. The pin has a built-in pullup resistor. There is no connection on the Model 30 board.
/IOW	83	I	I/O Write from 8288 bus controller
VCC	2, 21, 42, 66		+5 volt supply
VSS	23, 44, 64 84		Ground

Functional Description

Interrupt Controller

The interrupt controller has eight interrupt channels. Interrupt 1 is shared for three sources, the keyboard, mouse and real time clock. The BIOS controls the allocation.

The interrupt controller is a subset of the 8259A. It supports the following features in the 8086 mode:

- Automatic End of Interrupt

  Performs automatic reset after the second interrupt acknowledge

- Specific EOI

  Specifies the channel to reset

- Nonspecific EOI

  Resets the channel with the highest priority

The interrupt controller resolves priorities and stores interrupt request information in the IRR (interrupt request register). The ISR (interrupt service register) contains data identifying the channel in service.

Refer to the ACC 3000 timing diagram.

Mouse and Keyboard Interface

Two sets of circuitry control the interface for the mouse and keyboard respectively. They support a parallel to serial conversion when the CPU transmits data, and a serial to parallel conversion when the CPU receives data.

Interface protocol has the following sequence:

Start bit
Data bits (8 bits; start from LSB)
Parity bit
4 stop bits

Decoder and Data Bus Controller

The decoder decodes I/O addresses and sends chip select signals to respective peripheral chips. It enables a chip select when the corresponding peripheral bit in the planar register is set to one. The decoder also controls a bidirectional parallel port.

Refer to the following I/O Address Map.

Hex Range	Device
0000 to 001F	DMA Controller, 8237A-5
0020 to 003F	Interrupt controller
0040 to 005F	Timer
0060 to 0062	I/O ports
0063 to 006F	System board/Control and status
0080 to 008F	DMA page registers
00A0 to 00AF	Interrupt controller extension
00B0 to 00BF	Real time clock command/ status
00E0 to 00EF	Real time clock counter/ RAM
0320 to 032F	Hard disk
0378 to 037F	Parallel port
03C0 to 03DF	Video subsystem
03F0 to 03F7	Floppy disk
03F8 to 03FF	Serial port

Note: I/O addresses, Hex 000 to 0FF, are reserved for the system board I/O.

The NMI mask can be set and reset by system software with the following procedures:

Write Hex 80 to I/O address Hex A0
(enable NMI)
Write Hex 00 to I/O address Hex A0
(disable NMI)

The data bus controller in the ACC 3000 is a multiplexer to control data flow.

Peripheral Sense Logic

The peripheral sense logic recognizes the presence of the NPU (numeric processing unit) chip on the motherboard. If the NPU is present, the NPU install signal goes high.

The peripheral sense logic provides an interface between the CPU and the /HDINST install signal to determine if a hard disk is present.

NMI Control Logic

NMI control logic receives /IOCHCK, NPUINST, and parity error signals to generate an NMI (non-maskable interrupt) signal to the CPU for error checking.

Data Bus Interface

The data bus interface transmits and receives data between logic blocks and the CPU.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Power supply voltage	VCC	Ta=25 C	3.0	+7	V
Power dissipation (@ 5.25 V)	Wd			1	W
Current (@ 5.25 V)	IDD		20	50	mA
Input voltage	VI		0.0	VCC+0.5	V
Output voltage	VO		0.0	VCC+0.5	V
Operating temperature	Top		0	70	C
Storage temperature	Tstg		-50	150	C

Capacitance

Parameter	Symbol	Min	Max	Unit	Test Condition
Input capacitance	CI		10	pF	fc = 1 MHz unmeasured points at ground
I/O capacitance	CIO		15	pF	

DC Specifications

GROUP 1 INPUT

/IOR, IRQ2, IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, /IOCHCK, A9-A0, ALE, CLK14, /INTA, DEN, PARERR, AEN, /A1015IO, CPURESET, CLK8, RTCINT, /RTCRDY, NPUINTR, /TEST, /HDINST, OUT2, /ADSTB, OUT0, KEYLOCK, /DACK3, /DACK2, /IOW, /ALTVEC, /OUTDIS

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 +/- 0.5V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 +/- 0.5V
Input low current	IIL	n/a	-1.0	uA	VIN = 0.0V
Input high current	IIH	n/a	1.0	uA	VIN = VCC

GROUP 2 INPUT/OUTPUT

SD0, SD1, SD2, SD3, SD4, SD5, SD6, SD7, MSCLK, MSDATA, KBCLK, KBDATA

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 +/- 0.5V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 +/- 0.5V
Input low current	IIL		-10.0	uA	VIN = 0.0V
Input high current	IIH		10.0	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 8.0mA
Output high voltage	VOH	2.4		V	IOH = -8.0mA
Output high impedance current	IOZ	-10.0	10.0	uA	0V < VOUT < VCC

GROUP 3 TRISTATE OUTPUT

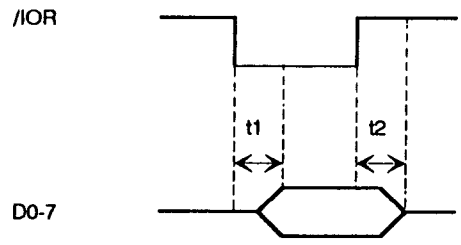
/POE, /WPC, /WPA, /RPC, /RPB, /RPA, /RTCW, /RTCCS, /8250CS, /VCMEMR, /VCCS, NPUINST, /DMACS, /ENIOBUS, INTR, NMI, /DISKCS, CLK0, /ENIORW, GATE2, /8253CS, /FDCS, SPKR

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 4.0mA
Output high voltage	VOH	2.4		V	IOH = -4.0mA
Output leakage tristate	IOZ	-10.0	10.0	uA	

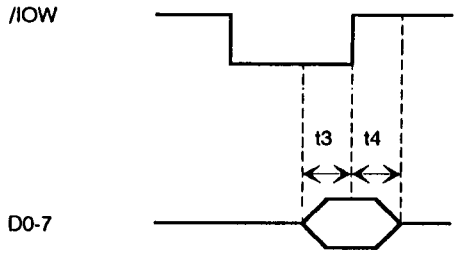
AC Specifications

Symbol	Description	Min	Max	Units
t1	Data valid from /IOR	21	30	ns
t2	Data float after /IOR	22	30	ns
t3	Data setup to /IOW	10		ns
t4	Data hold after /IOW	0		ns
t5	Data valid from /INTA	25	35	ns
t6	Data float after /INTA	25	35	ns
t7	Interrupt output delay	200		ns
t8	Interrupt output inactive delay	40		ns
t9	Mouse/keyboard CLK IN width low	500		ns
t10	Mouse/keyboard CLK IN width high	500		ns
t11	Mouse/keyboard DATA IN setup time	150		ns
t12	Mouse/keyboard DATA IN hold time	10		ns
t13	/RPA, /RPB, /RPC active delay after /IOR	20	35	ns
t14	/RPA, /RPB, /RPC inactive delay after /IOR	15	25	ns
t15	/WPA, /WPC active delay after /IOW	15	25	ns
t16	/WPA, /WPC inactive delay after /IOW	10	20	ns
t17	/CS active delay after ALE	20	35	ns
t18	/CS inactive delay after ALE	10	25	ns
t19	/ENIOBUS active delay after /CS	10		ns
t20	/ENIOBUS inactive delay after /CS	10		ns
t21	T_{LH} of OUT0 after CLK14	15		ns
t22	T_{HL} of OUT0 after CLK14	15		ns

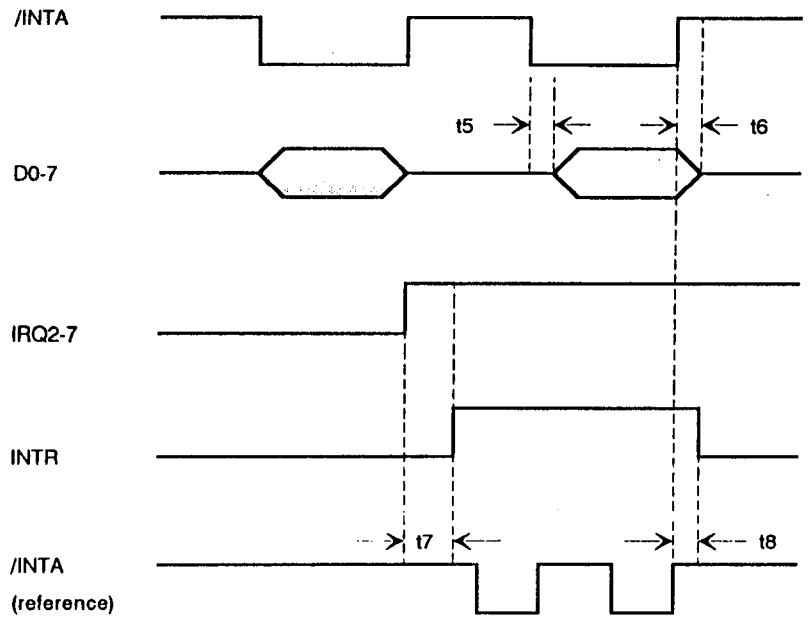
Read Cycle Timing



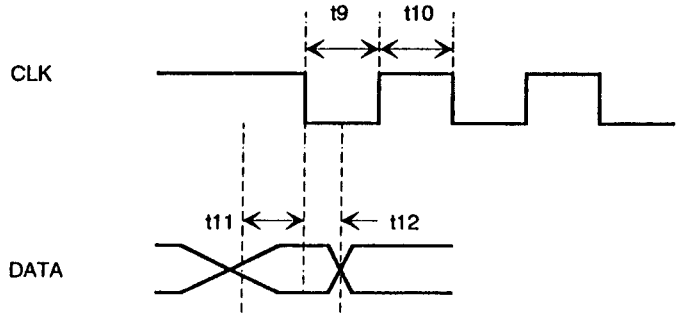
Write Cycle Timing



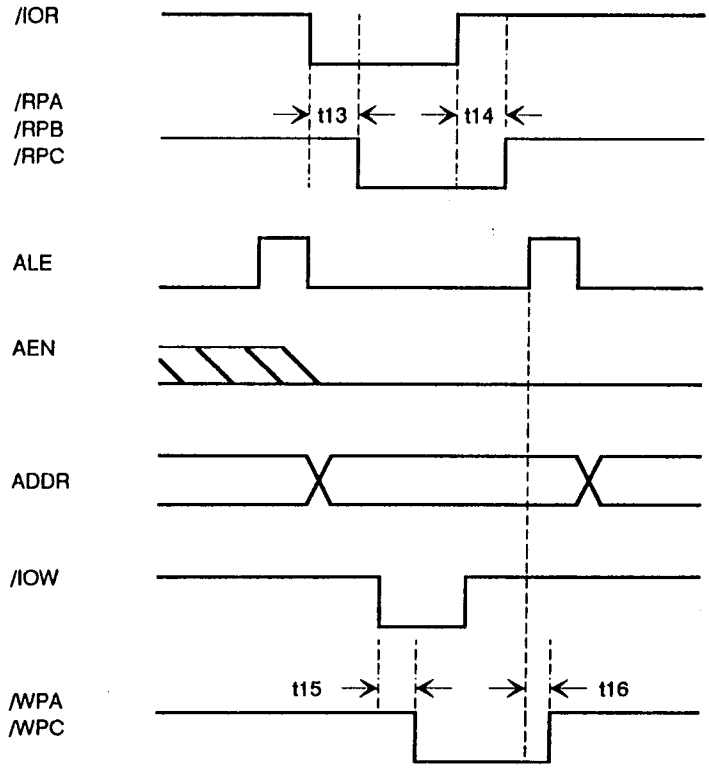
Interrupt Controller Timing



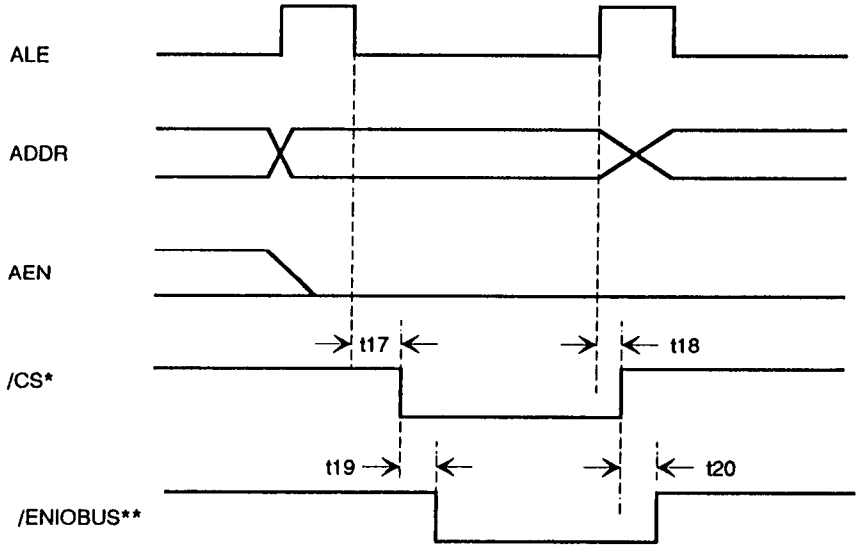
Mouse/Keyboard Timing



Parallel Port Timing



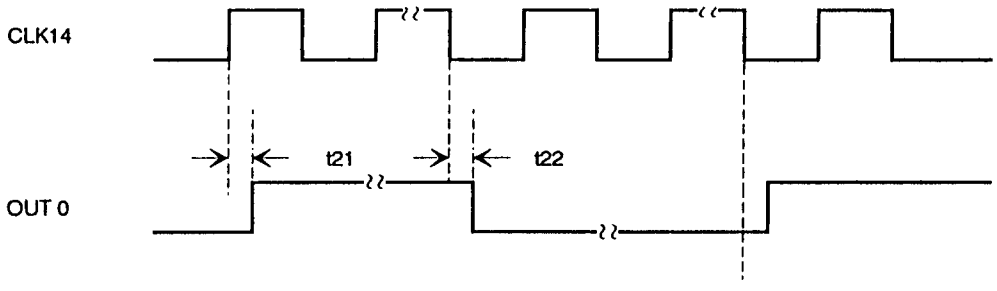
Chip Select Timing



* Active only when the respective enable bit is set to one and ADDR is stable before ALE.

** Active only when 8237, 765, I/O registers inside, I/O support gate array, parallel port, 82367, 58167, hard disk or 8250 is selected.

Other Timing



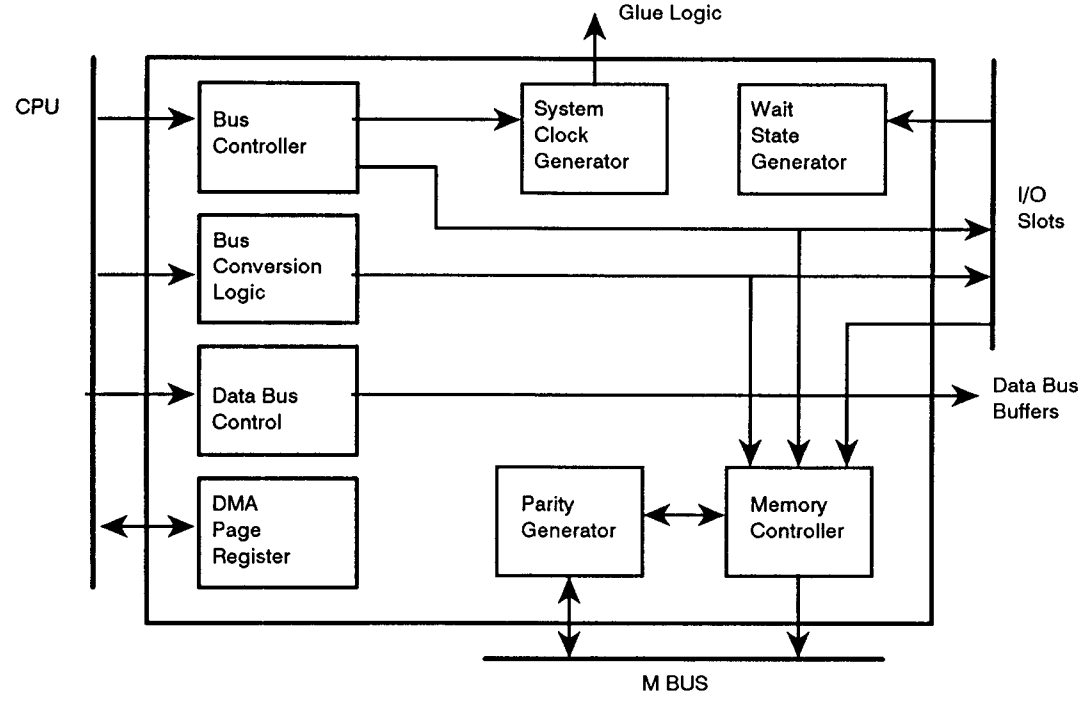
ACC 3100
Model 30 System Controller

The ACC 3100 is a VLSI device that emulates the System Support Gate Array of the IBM PS/2 Model 30. This chip is designed to help system designers build a machine compatible with the Model 30 at a lower cost and with a faster design cycle.

Features

- 100% IBM Model 30 system support gate array pin-to-pin compatible
- Bus controller
- Memory controller
- Parity checker
- Bus conversion logic
- Wait state generator
- System clock generator
- DMA page registers and support logic
- 1.5 micron high performance CMOS technology
- 84-L PLCC package

Block Diagram



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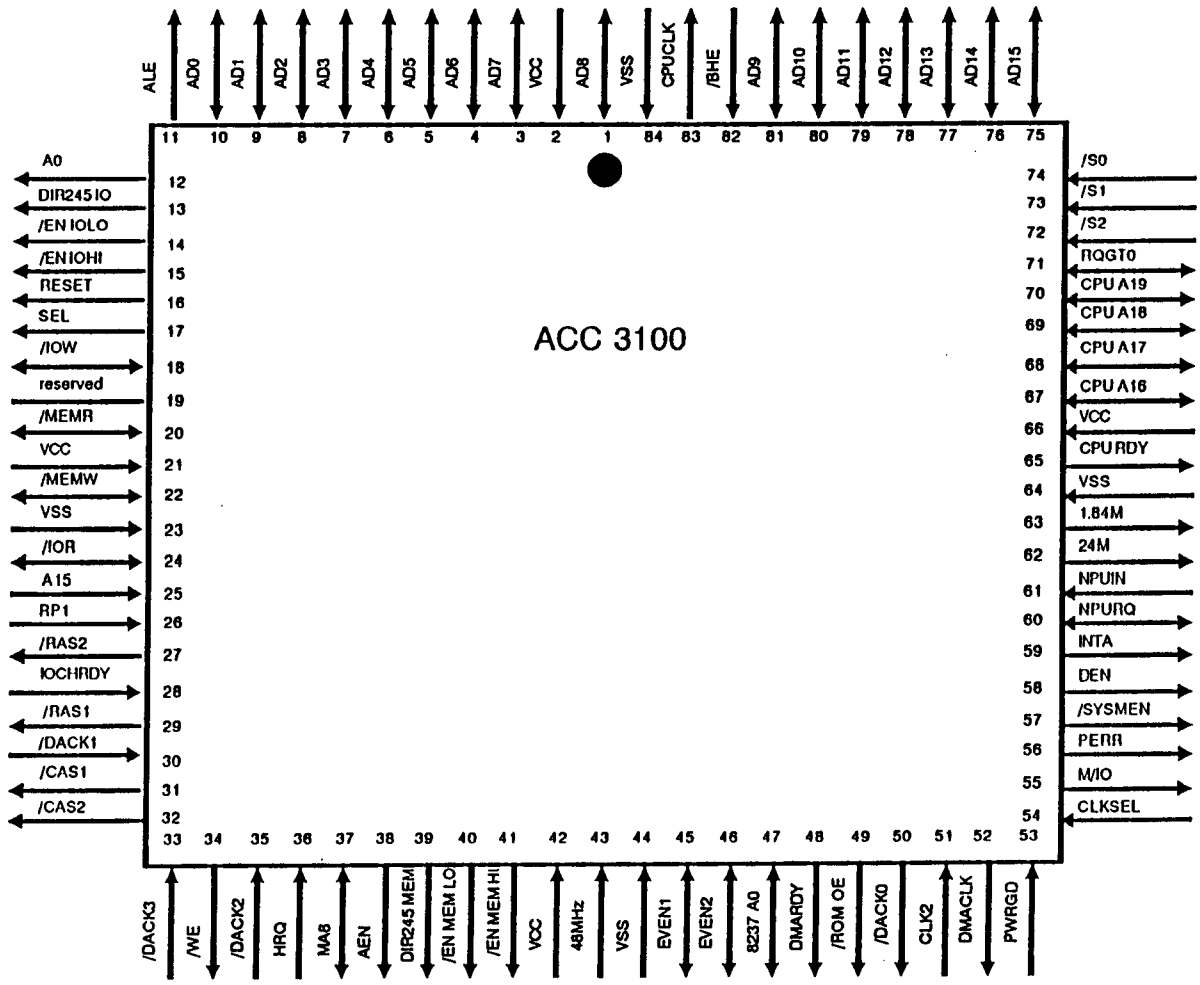
Pin Diagram


ACC 3100
ALE
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
VCC
AD8
VSS
CPUCLK
/BHE
AD9
AD10
AD11
AD12
AD13
AD14
AD15
A0
DIR245IO
/ENIOLO
/ENIOHI
RESET
SEL
/IOW
reserved
/MEMR
VCC
/MEMW
VSS
/IOR
A15
RP1
/RAS2
IOCHRDY
/RAS1
/DACK1
/CAS1
/CAS2
/S0
/S1
/S2
RQGT0
CPU A19
CPU A18
CPU A17
CPU A16
VCC
CPURDY
VSS
1.84M
24M
NPUIN
NPURQ
INTA
DEN
/SYSMEN
PERR
M/IO
CLKSEL
/DACK3
/WE
/DACK2
HRQ
MA8
AEN
DIR245 MEM
/EN MEM LO
/EN MEM HI
VCC
48MHz
VSS
EVEN1
EVEN2
8237 A0
DMARDY
/ROM OE
/DACK0
CLK2
DMACLK
PWRGD

Pin Descriptions

Symbol	Pin	I/O	Pin Description
AD15	75	I/O	CPU Local Address/Data Bus bit.
AD14	76		
AD13	77		
AD12	78		
AD11	79		
AD10	80		
AD9	81		
AD8	1		
AD7	3		
AD6	4		
AD5	5		
AD4	6		
AD3	7		
AD2	8		
AD1	9		
AD0	10		
ALE	11	O	CPU Address Latch Strobe
A0	12	O	Address Bit 0
A15	25	I	CPU Address 15
DIR245IO	13	O	Direction of I/O Data Buffer
/ENIOLO	14	O	Low Byte I/O Data Buffer Enable
/ENIOHI	15	O	High Byte I/O Date Buffer Enable
RESET	16	O	CPU Reset Input
SEL	17	O	DRAM Row/Column Address Select
/IOW	18	I/O	I/O Write Command
/MEMR	20	I/O	Memory Read Command
/MEMW	22	I/O	Memory Write Command
/IOR	24	I/O	I/O Read Command
RP1	26	I	Pull Up Resistor input
/RAS1	29	O	Row Address Strobe for DRAM Bank 1
/RAS2	27	O	Row Address Strobe for DRAM Bank 2

Pin Descriptions

Symbol	Pin	I/O	Pin Description
IOCHRDY	28	I	I/O Channel Ready Input
/DACK0	50	O	DMA Acknowledge
/DACK1 /DACK2 /DACK3	30 35 33	I	DMA Acknowledge
/CAS1 /CAS2	31 32	O O	Column Address Strobe for DRAM Low Byte Bank Column Address Strobe for DRAM High Byte Bank
/WE	34	O	Write Enable For DRAM
HRQ	36	I	Hold Request
MA8	37	I/O	DRAM Address Bus Bit 8
AEN	38	O	DMA Address Enable
DIR245MEM	39	O	Direction of Memory Data Buffer
/ENMEMLO	40	O	Low Byte Memory Data Buffer Enable
/ENMEMHI	41	O	High Byte Memory Data Buffer Enable
48MHz	43	I	48 MHz Clock Input
EVEN1 EVEN2	45 46	I/O I/O	High Byte Data Parity Check Low Byte Data Parity Check
8237A0	47	I/O	DMA Address 0
DMARDY	48	O	DMA Ready
/ROMOE	49	O	ROM Output Enable
CLK2	51	I	Alternate Clock Input (24 MHz)
DMACLK	52	O	DMA Clock Output
PWRGD	53	I	Power Good Input From Power Supply
CLKSEL	54	I	CLK2 Select
M/IO	55	O	Memory/IO Operation

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/PERR	56	O	Parity Error Output
/SYSMEN	57	O	System memory access enable.
DEN	58	O	Video Data Enable
INTA	59	O	Interrupt to CPU
NPURQ	60	I/O	8087 Request/Grant
NPUINST	61	I	8087 Installed
24M	62	O	24 MHz Clock Output For FDC
1.84M	63	O	1.84 MHz Clock Output For UART
CPURDY	65	O	CPU Ready
CPUA16 CPUA17 CPUA18 CPUA19	67 68 69 70	I/O	CPU Address
RQGT0	71	I/O	Bus Request/Grant
/S2 /S1 /S0	72 73 74	I	CPU Local Bus Status Bit
/BHE	82	I	Byte High Enable
CPUCLK	83	O	CPU Clock Input
VCC	2, 21, 42,66		+5 volt supply
VSS	23, 44, 64, 84		Ground
Reserved	19	I	

Functional Description

Bus Controller

The ACC 3100 bus controller is compatible with Intel's 8288. It decodes status from three CPU pins to generate I/O read, I/O write, memory read/write, and ALE commands. The /S0, /S1, and /S2 signals are decoded to define the following bus cycles:

/S2	/S1	/S0	
0 (low)	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1 (high)	0	0	Code address
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive

The bus controller accepts the Hold Request (HRQ) signal from the DMA controller.

The ACC 3100 has three modes of operation:

- CPU
- DMA
- Refresh

CPU Mode

During normal operation, the HRQ is inactive, decoding is from the status line.

DMA Mode

The HRQ signal is active to indicate a request from the DMA controller, the CPU receives a signal to release the bus, and bus control signals become inactive (float).

Refresh Mode

When the DRAM requires a refresh, the bus controller checks all 256 rows of addresses within 4 milliseconds.

Wait State Generator

The wait state generator inserts wait states to the CPU and controls bus conversion logic.

The wait state generator checks the A0 address line and /BHE to determine if byte-word conversion is required. Four wait states are inserted for the I/O if there is no byte-word conversion. Twelve wait states are inserted for byte-word conversion. There are no wait states on the motherboard RAM or ROM.

The IOCHRDY pin on the I/O card is pulled low when a device requires more time than the default wait states or when the CPU must wait for signals.

Memory Controller

The memory controller generates row address strobes and column address strobes for the DRAM.

/RAS1 apply to the first 128 Kbytes, with a range of 0 to 1FFFFH. /RAS2 apply to the next 512 Kbytes with a range of 20000H to 9FFFFH. /WE and SEL are common to both banks. SEL doesn't go to the DRAM directly, but is used as a DRAM address multiplexer.

The bus conversion logic converts the 16-bit data write to two 8-bit data writes, and converts two 8-bit data reads to a 16-bit data read.

System Clock Generator

The system clock generator receives 48 MHz input from an external oscillator and divides it into 24 MHz for the floppy disk controller. The 24 MHz is divided by three into 8 MHz with a

duty cycle of 33% for the 8086 to clock inputs. This signal is called the CPUCLK. The CPUCLK is divided into 4 MHz which is used as the DMA clock.

The 24 MHz frequency is also divided by 13 to generate 1.84 MHz for UART clock input.

The CPURESET, generated to reset the CPU, is active for 64 milliseconds after the PWRGD goes high.

Two additional pins, CLK2 and CLKSEL can be used for test purposes.

Decoder

The decoder decodes from CPUA19 to CPUA16 for the CPU to access ROM, DRAM, or video RAM. Address ranges follow.

ROM:	F0000H	to	FFFFFH
DRAM:	00000H	to	9FFFFH
Video RAM:	A0000H	to	AFFFFH
or	B8000H	to	BFFFFH

The DRAM range can be disabled by programming the 6BH I/O port. Refer to the following table.

Bit	Function
7	Parity check pointer 1 = lower 128K failed 0 = upper 512K failed
6	Disable RAM, 90000-9FFFF
5	Disable RAM, 80000-8FFFF
4	Disable RAM, 70000-7FFFF
3	Disable RAM, 60000-6FFFF
2	Disable RAM, 50000-5FFFF
1	Disable RAM, 40000-4FFFF
0	Remap low memory

DMA Page Registers

The DMA supplies 16 of the 20 address lines in the Model 30. The page register, a small 4 X 4 memory, drives the additional four address lines. When the DMA controls the bus, the DMA drives A0 to A15, the page register drives A16 to A19. The register addresses are listed in the following table.

HEX Address	DMA Register Address
081	Channel 2
082	Channel 3
083	Channel 1
087	Channel 0

Parity Generator

The parity generator is for error detection only and is dedicated to the DRAM. The parity generator is active during DRAM read and write. If a parity error occurs during read, an NMI is generated.

Rating Specifications

Parameter	Symbol	Condition	Min	Max	Unit
Power supply voltage	VCC	Ta=25 C	3.0	+7	V
Power dissipation (@ 5.25 V)	Wd			1	W
Current (@ 5.25 V)	IDD		20	50	mA
Input voltage	VI		0.0	VCC+0.5	V
Output voltage	VO		0.0	VCC+0.5	V
Operating temperature	Top		0	70	C
Storage temperature	Tstg		-50	150	C

Capacitance

Parameter	Symbol	Min	Max	Unit	Test Condition
Input capacitance	CI		10	pF	fc = 1 MHz unmeasured points at ground
I/O capacitance	CIO		15	pF	

DC Specifications

GROUP 1 INPUT

HRQ, /DACK1, /DACK2, /DACK3, IOCHRDY, RP1, A15, Reserved, /BHE, NPUINST, 48MHZ

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V +/- 0.5 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 V +/- 0.5 V
Input low current	IIL	n/a	-1.0	uA	VIN = 0.0V
Input high current	IIH	n/a	1.0	uA	VIN = VCC

GROUP 2 INPUT WITH PULLUP

PWRGD, CLK2, /S0, /S1, /S2, CLKSEL

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V +/- 0.5 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 V +/- 0.5 V
Input low current	IIL	-64.0	250.0	uA	VIN = 0.0V
Input high current	IIH	n/a	n/a	uA	n/a

GROUP 3 TRISTATE OUTPUT

/CAS1, /CAS2, /WE, M/IO, /PERR, /SYSMEN, DEN, INTA, 1.84M, A0, DIR245IO, /ENIOLO, /ENIOHI, CPURESET, SEL, DIR245MEM, /ENMEMLO, /ENMEMHI, DMARDY, /ROMOE, /DACK0, DMACLK, ALE, CPURDY, /RAS1, /RAS2, AEN

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 4.0mA
Output high voltage	VOH	2.4		V	IOH = -4.0mA
Output high Impedance current	IOZ	-10.0	10.0	uA	

MA8, CPUCLK, 24M

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 8.0mA
Output high voltage	VOH	2.4		V	IOH = -8.0mA
Output high Impedance current	IOZ	-10.0	10.0	uA	

GROUP 4 INPUT/OUTPUT

AD0-AD15, CPUA16-A19, 8237A0, EVEN1, EVEN2, RQGT0, NPURQ

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V +/- 0.5V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 V +/- 0.5V
Input low current	IIL		-10.0	uA	VIN = 0.0V
Input high current	IIH		10.0	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 8.0mA
Output high voltage	VOH	2.4		V	IOH = -8.0mA
Output high impedance current	IOZ	-10.0	10.0	uA	0V < VOUT < VCC

GROUP 5 INPUT/OUTPUT WITH PULLUP

/MEMW, /MEMR

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V +/- 0.5V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 V +/- 0.5V
Output low voltage	VOL		0.4	V	IOL = 4.0mA
Output high voltage	VOH	2.4		V	IOH = -4.0mA
Output high impedance current	IOZ	-64.0	-260.0	uA	VCC = 5.5V

/IOW, /IOR

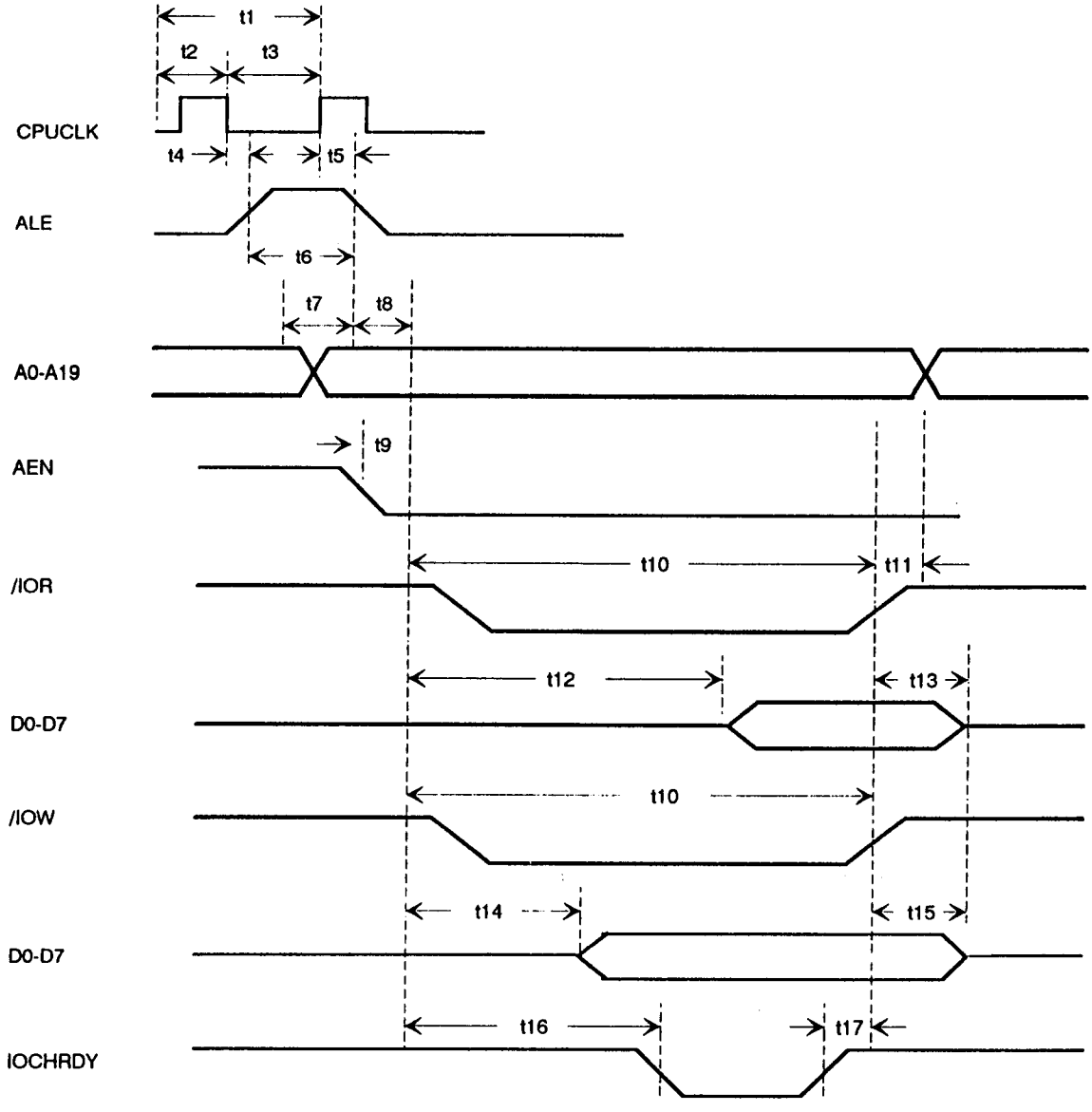
Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V +/- 0.5V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 V +/- 0.5V
Output low voltage	VOL		0.4	V	IOL = 8.0mA
Output high voltage	VOH	2.4		V	IOH = -8.0mA
Output high impedance current	IOZ	-64.0	-260.0	uA	VCC = 5.5V

AC Specifications

8 Bit I/O Bus Cycles

Symbol	Description	Min	Max	Units
t1	CLK cycle time	125		ns
t2	CLK high time	44		ns
t3	CLK low time	68		ns
t4	ALE active delay		50	ns
t5	ALE inactive delay		55	ns
t6	ALE width	58		ns
t7	Address valid to ALE inactive	20		ns
t8	ALE inactive to command active	60		ns
t9	Command active from AEN inactive	95		ns
t10	Command pulse width	605		ns
t11	Address hold from command inactive	45		ns
t12	Data valid from read active		540	ns
t13	Data hold from read inactive	0		ns
t14	Data valid from write active		120	ns
t15	Data hold from write inactive	25		ns
t16	IOCHRDY inactive from command active		325	ns
t17	Command inactive from IOCHRDY active	160		ns

8 Bit I/O Bus Cycles

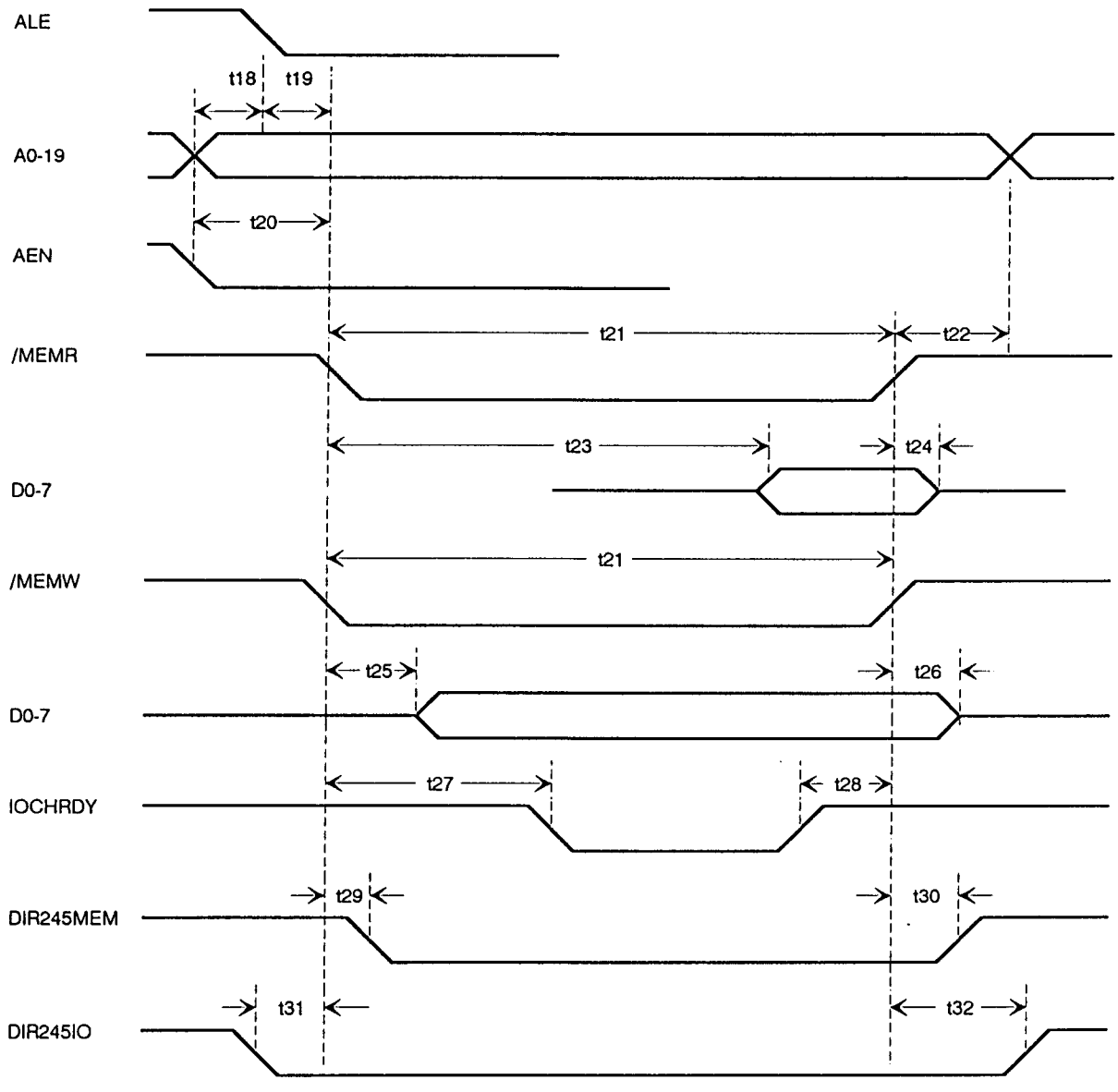


AC Specifications

8 Bit Memory Bus Cycles

Symbol	Description	Min	Max	Units
t18	Address valid to ALE inactive	20		ns
t19	ALE inactive to command acttive	60		ns
t20	Command active from AEN inactive	95		ns
t21	Command pulse width	395		ns
t22	Address hold from command inactive	45		ns
t23	Data valid from Read active		315	ns
t24	Data hold from Read inactive	0		ns
t25	Data valid from Write active		120	ns
t26	Data hold from Write inactive	25		ns
t27	IOCHRDY inactive from command active		115	ns
t28	Command inactive from IOCHRDY active	160		ns
t29	DIR245MEM active from command active		0	ns
t30	DIR245MEM inactive from command inactive		20	ns
t31	DIR245IO active from command active		40	ns
t32	DIR245IO inactive from command inactive		80	ns

8 Bit Memory Bus Cycles

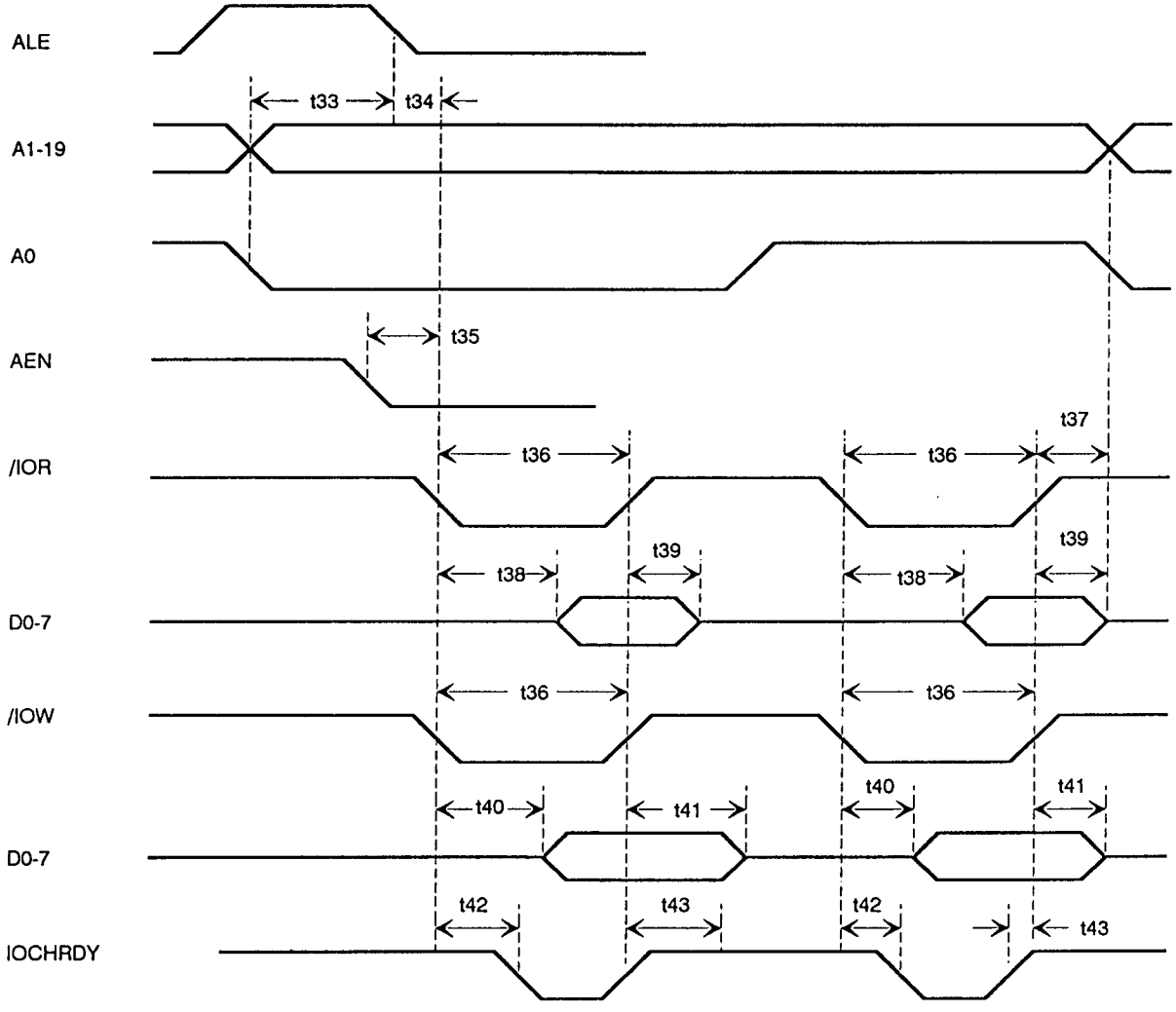


AC Specifications

16 Bit I/O Bus Cycles

Symbol	Description	Min	Max	Units
t33	Address valid to ALE inactive	20		ns
t34	ALE inactive to command active	60		ns
t35	Command active from AEN inactive	95		ns
t36	Command pulse width	605		ns
t37	Address hold from command inactive	45		ns
t38	Data valid from read active		540	ns
t39	Data hold from read inactive	0		ns
t40	Data valid from write active		120	ns
t41	Data hold from write inactive	25		ns
t42	IOCHRDY inactive from command active		325	ns
t43	Command inactive from IOCHRDY active	160		ns

16 Bit I/O Bus Cycles

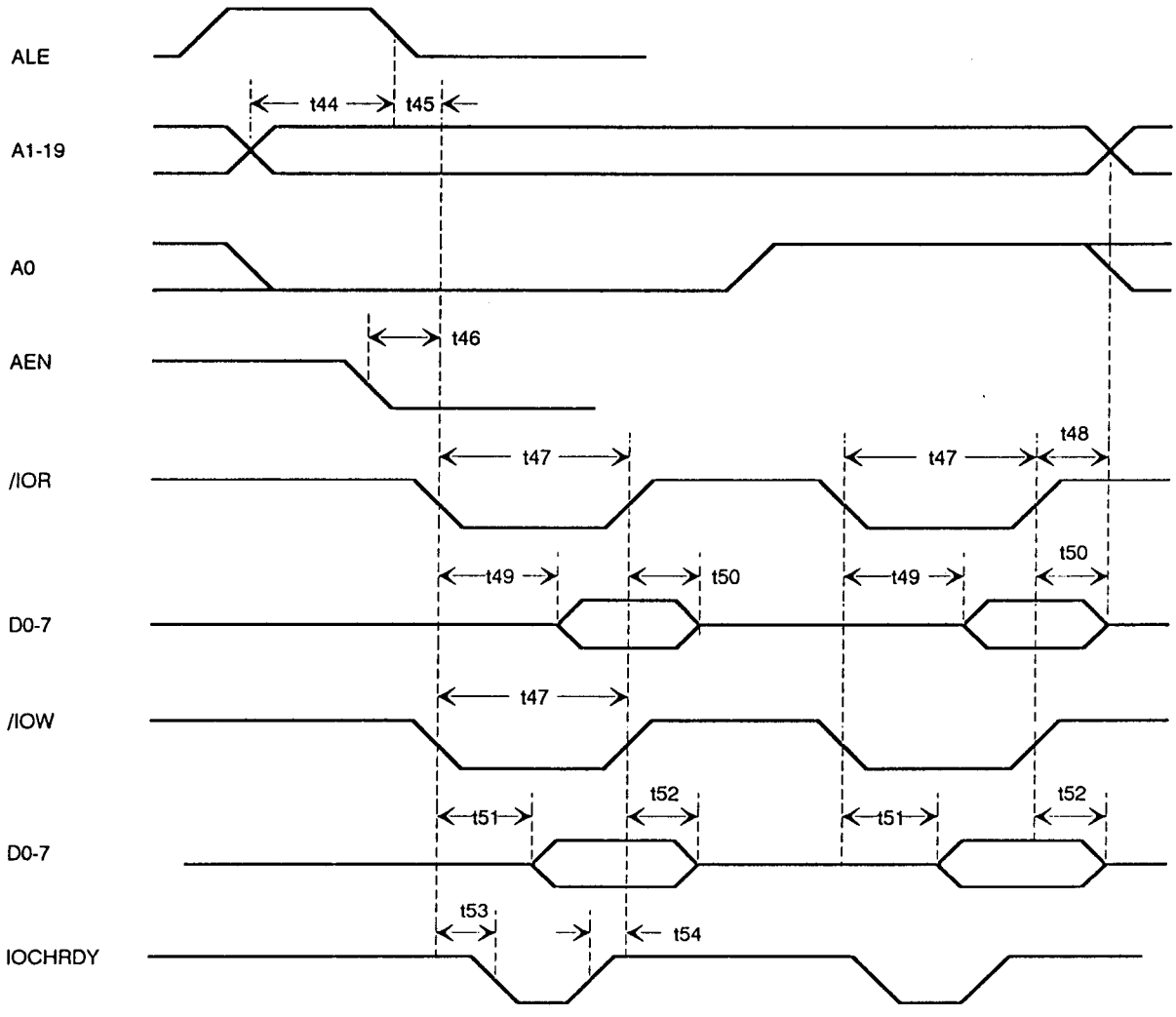


AC Specifications

16 Bit Memory Bus Cycles

Symbol	Description	Min	Max	Units
t44	Addrress valid to ALE inactive	20		ns
t45	ALE inactive to command active	60		ns
t46	Command active from AEN inactive	95		ns
t47	Command pulse width	395		ns
t48	Address hold from command inactive	45		ns
t49	Data valid from read active		315	ns
t50	Data hold from read inactive	0		ns
t51	Data valid from write active		120	ns
t52	Data hold from write inactive	25		ns
t53	IOCHRDY inactive from command active		115	ns
t54	Command inactive from IOCHRDY active	160		ns

16 Bit Memory Bus Cycles

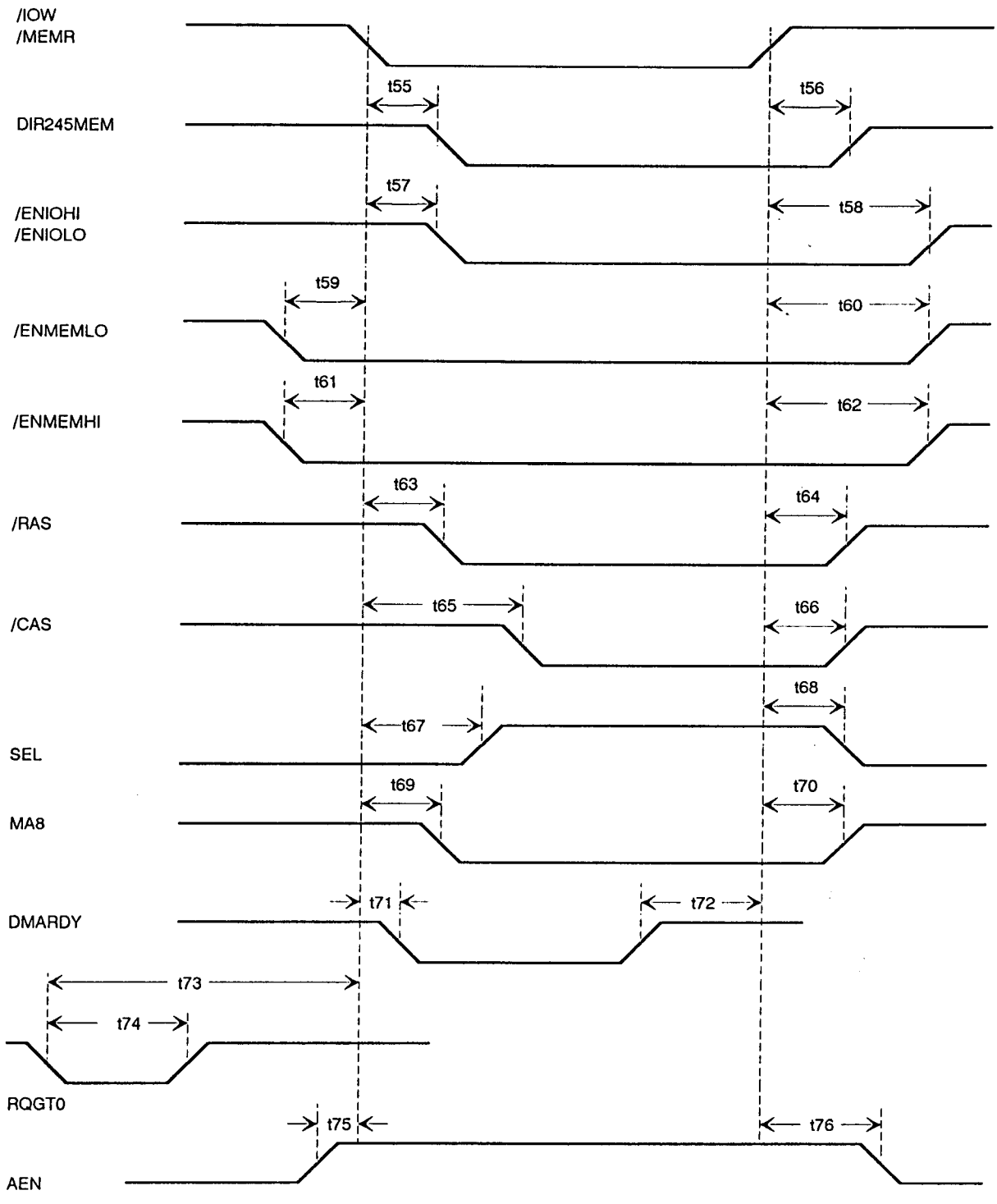


AC Specifications

DMA

Symbol	Description	Min	Max	Units
t55	DIR245MEM active from command active		24	ns
t56	DIR245MEM inactive from comand inactive		60	ns
t57	/ENIOHI and /ENIOLO active from command active		24	ns
t58	/ENIOHI and /ENIOLO inactive from command inactive		261	ns
t59	/ENMEMLO active to command active	320		ns
t60	/ENMEMLO inactive from command inactive		275	ns
t61	/ENMEMHI active to command active	340		ns
t62	/ENMEMHI inactive from command inactive		275	ns
t63	/RAS active from command active		24	ns
t64	/RAS inactive from command inactive		40	ns
t65	/CAS active from command active		110	ns
t66	/CAS inactive from command inactive		45	ns
t67	SEL active from command active		79	ns
t68	SEL inactive from command inactive		35	ns
t69	MA8 active from command active		74	ns
t70	MA8 inactive from command inactive		41	ns
t71	DMARDY active from command active		20	ns
t72	DMARDY inactive from command inactive		80	ns
t73	RQGT0 active from command active	724		ns
t74	RQGT0 inactive from command inactive	650		ns
t75	AEN active to command active	351		ns
t76	AEN inactive from command inactive		240	ns

DMA

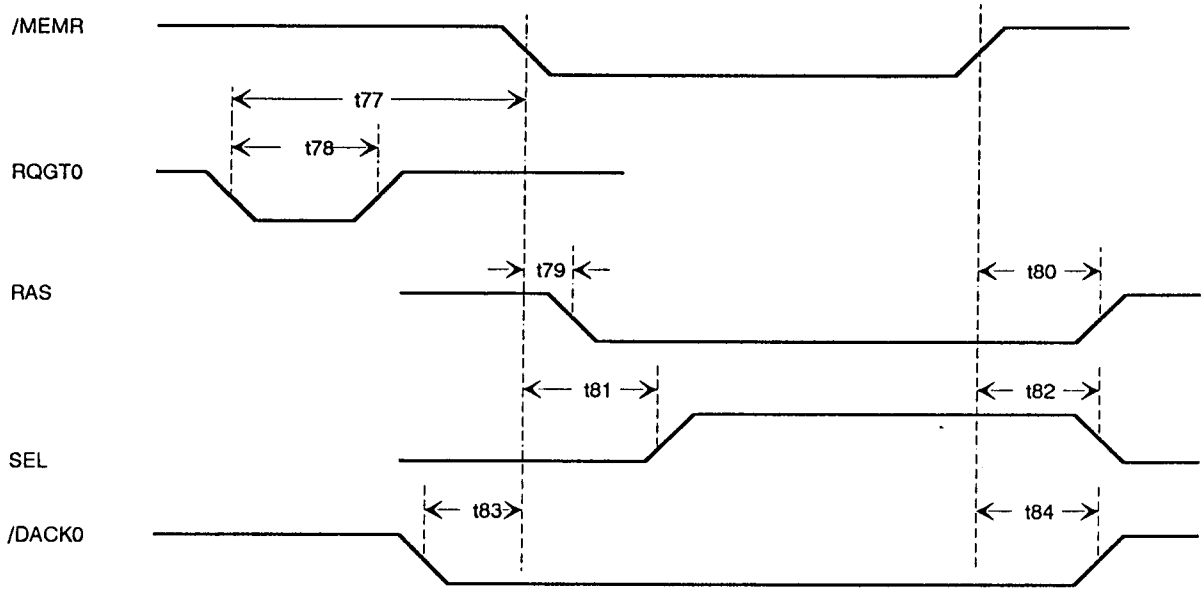

/IOW
/MEMR
t55
t56
DIR245MEM
t57
t58
/ENIOHI
/ENIOLO
t59
t60
/ENMEMLO
t61
t62
/ENMEMHI
t63
t64
/RAS
t65
t66
/CAS
t68
t67
SEL
t69
t70
MA8
t71
t72
DMARDY
t73
t74
RQGT0
t75
t76
AEN

AC Specifications

Refresh

Symbol	Description	Min	Max	Units
t77	Refresh RQGT0 active to command active	566		ns
t78	Refresh RQGT0 inactive to command inactive	491		ns
t79	/RAS active from command active		1	ns
t80	/RAS inactive from command inactive		36	ns
t81	SEL active from command active		78	ns
t82	SEL inactive from command inactive		32	ns
t83	/DACK0 active to command active	205		ns
t84	/DACK0 inactive from command inactive		50	ns

Refresh

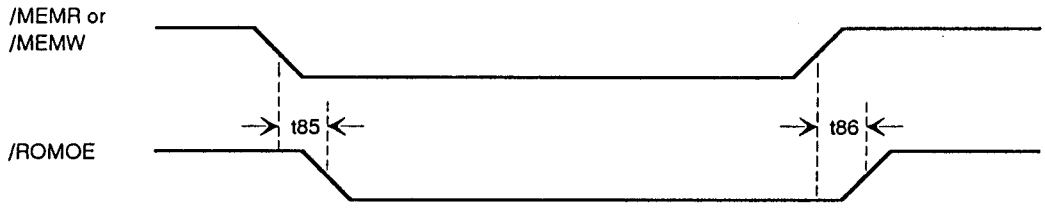


AC Specifications

ROM Access

Symbol	Description	Min	Max	Units
t85	/ROMOE active from command active		0	ns
t86	/ROMOE inactive from command inactive		3	ns

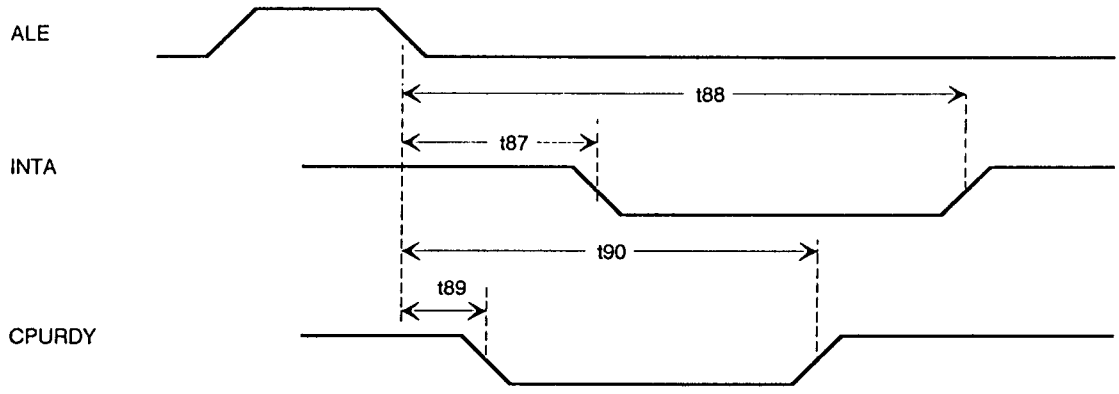
ROM Access



AC Specifications

Interrupt

Symbol	Description	Min	Max	Units
t87	INTA active from ALE inactive		200	ns
t88	INTA inactive from ALE inactive		840	ns
t89	CPURDY active from ALE inactive		100	ns
t90	CPURDY inactive from ALE inactive		720	ns



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