ACC 82300
386 AT Chip Set

The ACC 82300 chip set is designed for system designers to build a high performance 20/25 MHz 386 systems. The ACC 82300 contains three VLSI chips that can implement a 100% compatible IBM PC/AT system.

The ACC 2500 provides system control signals, the ACC2300 is a page interleaved memory controller, and the ACC 2000 is the integrated peripherals controller.

The ACC 82300 chip set supports a local CPU bus, a system memory bus, and compatible AT buses. The AT bus clock is fixed at 8 MHz and is totally asynchonous to the CPU clock to support compatible AT bus timing.

The ACC 82300 chip set operates up to 20/25 MHz with zero wait state memory access by using 80 ns DRAMs.

Features

- 100% IBM PC/AT compatible
- Supports up to 16 MB on-board memory
- Operates with Page interleaved DRAM accessing
- Supports 1, 2 and 4 memory banks with 256K x 1 and 256K x 4, or 1M x 1 DRAMs
- Supports 80387 coprocessors
- Supports EMS 4.0
- Supports shadow RAM for efficient BIOS execution
- Independent AT bus clock
- Flexible architecture to design customized 386 systems
- Supports 20/25 MHz zero wait state operation

General Description

The 82300 chip set is designed for 80386 based IBM PC/AT compatible systems. The 82300 supports four buses as illustrated in the system block diagram. CPU local bus (A and D) is the bus between the 80386, and address and data buffers. DRAM is accessed through the system memory bus (MA and ID) and controlled by the ACC 2300. The I/O channel bus (SA and SD) is compatible with the IBM PC/AT bus and can support both 8-bit and 16-bit devices. The peripheral bus (PA and PD) interfaces the on-board DMA controller, timer, and interrupt controller. The local data bus and system memory data bus has a 32-bit data width. The I/O data bus supports up to 16 bits and the peripheral data bus supports 8-bit peripherals.

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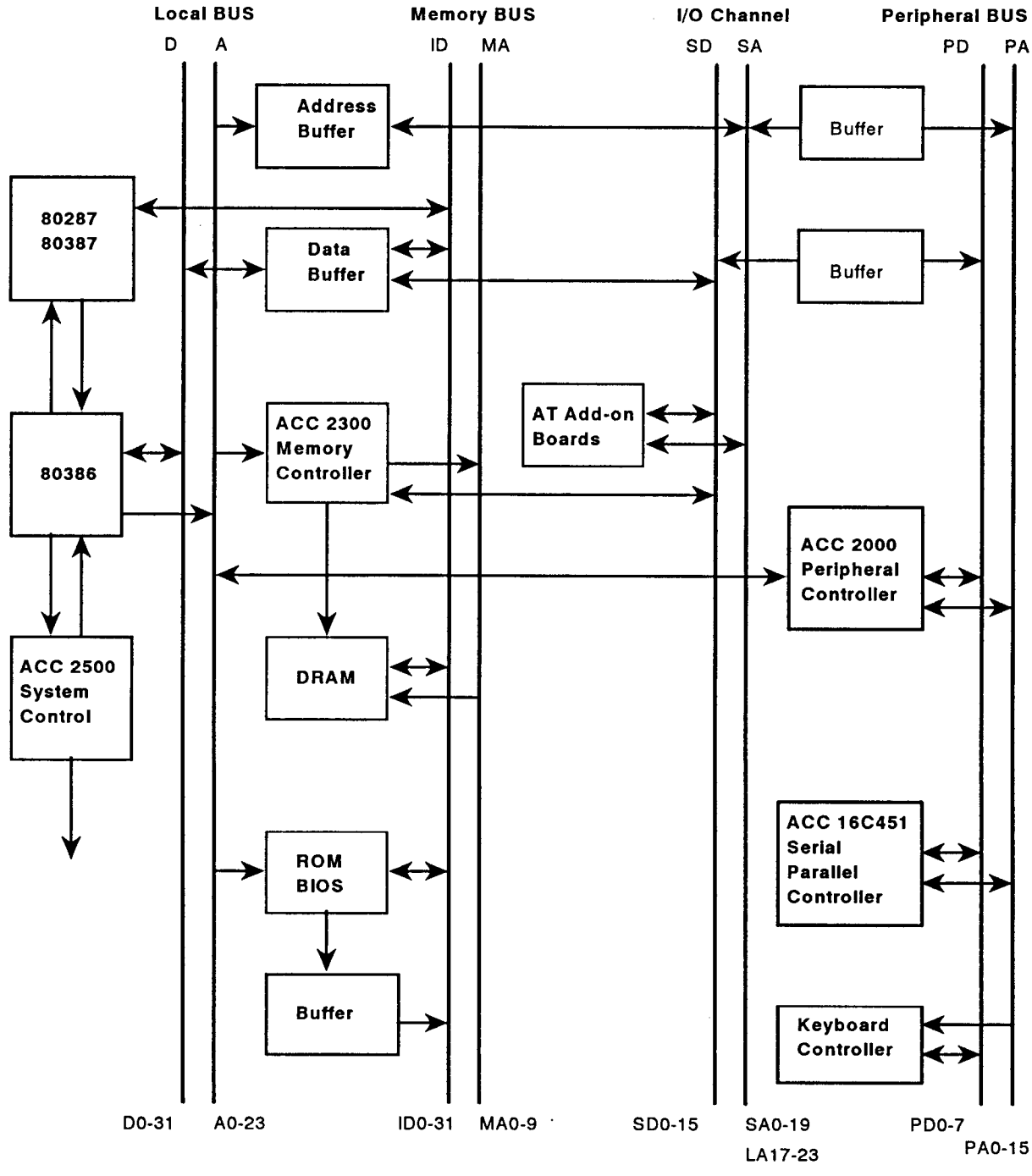
ACC 82300 AT System Block Diagram



ACC 2000
PC/AT Integrated Bus & Peripheral Controller

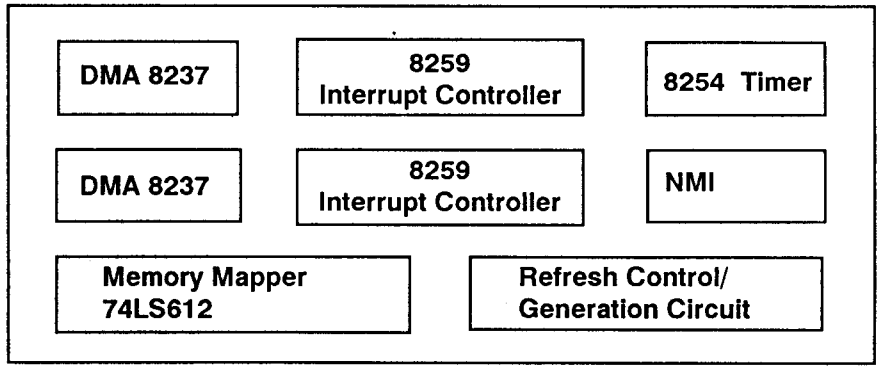
The ACC 2000 is an integrated high performance CMOS PC/AT* peripheral controller that incorporates several TTL, SSI, and MSI including two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, and one 74LS612 memory mapper. The ACC 2000 is a high performance VLSI that offers a single chip solution for all the peripherals attached to the X BUS (peripheral bus) in IBM PC/AT compatible systems.

Features

- 100% hardware and software compatible with the IBM* PC/AT
- Fully compatible to Intel's

  8237 DMA controller
  8254 Timer/Counter
  8259 Interrupt controller
- Fully compatible to TI's 74LS612 memory mapper
- Supports 7 DMA channels, 3 timer/counter channels and 14 interrupt request channels
- 100 % compatible with the IBM AT I/O BUS
- Supports up to 8 MHz DMA clock
- Supports 16 MB DMA address space
- Built-in refresh control circuit
- TTL compatible
- Speed switching through hardware or software
- 1.5 micron high performance CMOS technology
- 84-L PLCC package

Block Diagram



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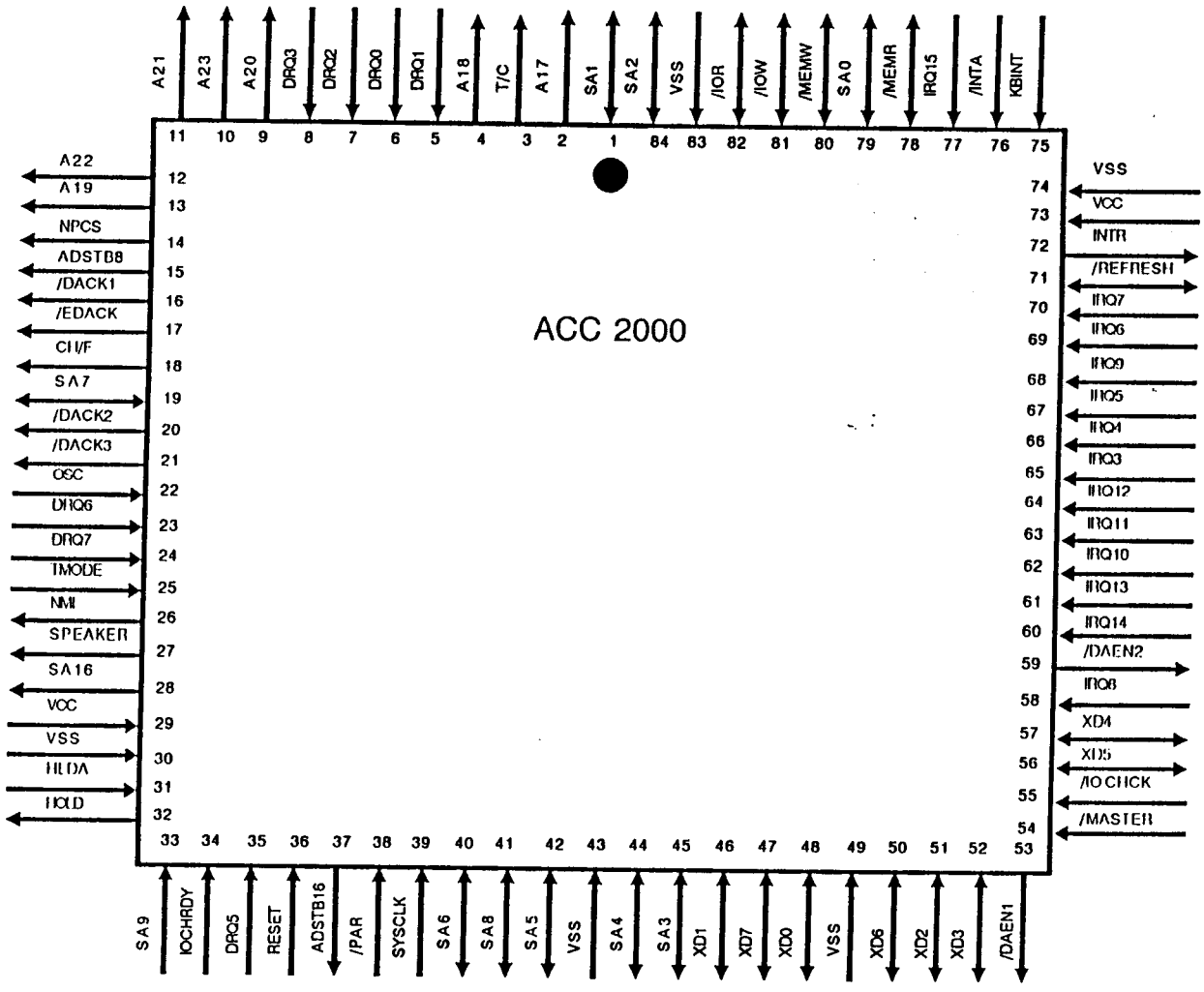
Pin Diagram


ACC 2000
A21 11
A23 10
A20 9
DRQ3 8
DRQ2 7
DRQ0 6
DRQ1 5
A18 4
T/C 3
A17 2
SA1 1
SA2 84
VSS 83
/IOR 82
/IOW 81
/MEMW 80
SA0 79
/MEMR 78
IRQ15 77
/INTA 76
KBINT 75
A22 12
A19 13
NPCS 14
ADSTB8 15
/DACK1 16
/EDACK 17
CH/F 18
SA7 19
/DACK2 20
/DACK3 21
OSC 22
DRQ6 23
DRQ7 24
TMODE 25
NMI 26
SPEAKER 27
SA16 28
VCC 29
VSS 30
HLDA 31
HOLD 32
VSS 74
VCC 73
INTR 72
/REFRESH 71
IRQ7 70
IRQ6 69
IRQ9 68
IRQ5 67
IRQ4 66
IRQ3 65
IRQ12 64
IRQ11 63
IRQ10 62
IRQ13 61
IRQ14 60
/DAEN2 59
IRQ8 58
XD4 57
XD5 56
/IOCHCK 55
/MASTER 54
SA9 33
IOCHRDY 34
DRQ5 35
RESET 36
ADSTB16 37
/PAR 38
SYSCLK 39
SA6 40
SA8 41
SA5 42
VSS 43
SA4 44
SA3 45
XD1 46
XD7 47
XD0 48
VSS 49
XD6 50
XD2 51
XD3 52
/DAEN1 53

Pin Descriptions

Symbol	Pin	Type	Description
SA0	79	I/O	System address bus bit.
SA1	1		
SA2	84		
SA3	45		
SA4	44		
SA5	42		
SA6	40		
SA7	19		
SA8	41		
SA9	33	I	System address bus bit.
SA16	28	O	System address bus Bit 16.
A17	2	O	Address bus bit.
A18	4		
A19	13		
A20	9		
A21	11		
A22	12		
A23	10		
T/C	3	O	Terminal count pulsing. When the terminal count for DMA channel is reached.
DRQ0	6	I	DMA Request Line. Active high.
DRQ1	5		
DRQ2	7		
DRQ3	8		
DRQ5	35		
DRQ6	23		
DRQ7	24		
NPCS	14	O	Chip select for numeric processor 80287.
ADSTB8	15	O	Address strobe for 8 bit DMA transfers.
/DACK1	16	O	Encoded DMA acknowledge bit.
/DACK2	20		
/DACK3	21		
/EDACK	17	O	Enable DMA acknowledge decoder. Active low .
CH/F	18	O	Change operation speed with software, I/O port 3C5H Bit 0.

Pin Descriptions

Symbol	Pin	Type	Description
OSC	22	I	14.31818 MHz clock input.
TMODE	25	I	Test pin.
NMI	26	O	Non-maskable interrupt to 80286 CPU. Active high; NMI generated by the math processor, memory parity error, or error from bus /IOCHCK.
SPEAKER	27	O	Data to speaker.
HLDA	31	I	Hold acknowledge from CPU.
HOLD	32	O	Hold request to CPU. Active high.
IOCHRDY	34	I	I/O channel ready from expansion bus.
RESET	36	I	System reset.
ADSTB16	37	O	Address strobe for 16 bit DMA transfers.
/PAR	38	I	Parity error output from Data buffer. Active low.
SYSCLK	39	I	System clock.
XD0 XD1 XD2 XD3 XD4 XD5 XD6 XD7	48 46 51 52 57 56 50 47	I/O	Peripheral data bus Bit 0.
/DAEN1	53	O	DMA address enable for 8 bit data transfer. Active low.
/MASTER	54	I	CPU I/O control for address, data, and control lines.
/IOCHCK	55	I	Error expansion bus. Active low.
/DAEN2	59	O	DMA address enable for 16 bit data transfer. Active low.

Pin Descriptions

Symbol	Pin	Type	Description
IRQ3	65	I	Interrupt request input. Active high.
IRQ4	66	I	
IRQ5	67	I	
IRQ6	69	I	
IRQ7	70	I	
IRQ8	58	I	
IRQ9	68	I	
IRQ10	62	I	
IRQ11	63	I	
IRQ12	64	I	
IRQ13	61	I	
IRQ14	60	I	
IRQ15	77	I	
/REFRESH	71	I/O	Refresh cycle. Active low.
INTR	72	O	Interrupt to CPU. Active high.
KBINT	75	I	Keyboard interrupt to 8259.
/INTA	76	I	Interrupt acknowledge. Active low.
/MEMR	78	I/O	Memory read. Active low.
/MEMW	80	I/O	Memory write. Active low.
/IOW	81	I/O	I/O write. Active low.
/IOR	82	I/O	I/O read. Active low.
VCC	29, 73		+5 volt supply
VSS	30, 43, 49, 74, 83		Ground

Functional Description

Interrupt Controller

Two programmable interrupt controllers in the ACC 2000 function as a system wide interrupt manager for an IBM PC/AT system, compatible with the Intel 8259 interrupt controller. The interrupt controller efficiently determines when and which I/O device is serviced by the microcomputer.

The two cascaded interrupt controllers in the ACC 2000 provide a total of 15 possible interrupt sources. One of these interrupt request lines is used internally, providing a total of 14 possible external interrupt sources. The internal line connects to the 8254 Counter 0 output.

Mode Controller

The system clock can be switched by either software or hardware.

With software switching, users can program Bit 0 in I/O port 3C5H to select the frequency of the system clock. When Bit 0 is programmed HIGH, it operates in "turbo" mode.

Hardware switching is with a button key or a jumper connecting to the CH/F pin to select the appropriate mode. If the CH/F signal is a rising edge trigger, it is set to "turbo" mode, and if a falling edge, it is set to "normal" mode.

Each switching scheme is independent of the other. The system is always set by the latest selection, hardware or software.

DMA

There are two 8237 equivalent DMA controllers cascaded together in the ACC 2000 chip. During a DMA cycle, one of the two external 8-bit latches hold the middle range address bits while the 74LS612 generates the upper range address bits. Once the hold request has been acknowledged, the DMA controller drives 24 address bits for a total addressing capability of 16 Megabytes. The middle address bits of the 24-bit address range are held in two sets of 8-bit registers, one register for each DMA controller. The DMA controller drives the value to be loaded onto the data bus, and then issues an address strobe signal to latch the data bus value into these registers.

The two 8237 compatible DMA controllers in the ACC 2000 provide a total of seven external DMA channels. Each channel has a 24-bit address output to access data throughout the entire 16 megabyte system address space. Channel 0 through channel 3 support 8-bit peripherals and an 8 or 16-bit memory. Each channel can transfer data in 64 Kbyte pages.

Channel 4 is used for cascading and is not available externally. Channel 5 through channel 7 support 16-bit I/O adapters to transfer data between 16-bit I/O adapters and 16-bit system memory. Each channel can transfer data in 128 Kbyte pages. The DMA function improves the computer system by allowing external devices to transfer information directly from and to the system memory.

Features include

- Address increment or decrement.
- Seven independent DMA channels with independent auto initialization for each channel.
- Each DMA request can be controlled individually to enable or disable.
- Software DMA request.

Timer/Counter

The Timer/Counter is the functional equivalent of an 8254 timer. It has three internal counters and clock inputs. The three clock inputs are tied to a clock of 1.19 MHz. The output of Counter 0 is connected to the IRQ input of interrupt controller one. Counter one output initiates a refresh cycle and Counter two output generates sound waveforms for speaker circuitry.

Features:

- Three independent 16-bit counters
- Count binary or BCD

Memory Mapper

The ACC 2000 has the equivalent of a 74LS612 to generate the upper address bits during a DMA cycle.

Source Memory Mapper	8237
(for DMA Channels 0 - 3)	
Address A23 <--> A16	A15 <--> A0
(for DMA Channels 5 - 7)	
Address A23 <--> A17	A16 <--> A1

PIO

The PIO is the system configuration to control the timer channel speaker ports. It also has circuitry to detect refresh. This condition can be read back as Bit 4.

Refresh Generation Logic

Refresh circuitry contains an 8-bit counter for address SA0-7 during a refresh.

Refresh/DMA Abitration Logic

ACC 2000 contains circuitry to control a refresh cycle. A 74LS590 equivalent 8-bit counter outputs the refresh addresses onto the memory bus when the refresh signal is pulled low.

There are two possible sources for a hold request to the CPU. Either the DMA controller issues a hold request or the output of Counter 1 in the 8254 makes a low to high transition. The HOLD line is active when either source is requesting a hold. The hold request from the DMA controller is sampled on the rising edge of the DMA clock and the request from the timer is sampled on the falling edge of the DMA clock.

If the DMA controller's hold wins the arbitration, the HOLD is asserted, and it waits for a signal back from the CPU. When the DMA controller is finished, it negates its hold request signal to the arbiter. The arbitration then switches to a REFRESH cycle if there is a pending hold from the Counter/Timer, otherwise the arbiter inactivates the HOLD line and returns control to the CPU.

If a refresh cycle wins the arbitration, the HOLD is asserted and the ACC 2000 pulls the /REFRESH pin low. /REFRESH remains low for four SYSCLK rising edges. On the fourth rising edge of SYSCLK, the HOLD line is inactivated. However, if there is a pending hold request from the DMA controller on the fourth rising edge of SYSCLK, the REFRESH cycle is extended for one more SYSCLK cycle. The Hold request arbiter then acknowledges the hold request from the DMA controller.

NMI and Port B Logic

The ACC 2000 contains non-maskable interrupt (NMI) signal generation logic. An NMI can be caused by an I/O error or by a parity error. Port B indentifies the source of the error. At power up, the NMI signal is masked off. NMI is enabled by writing to I/O address 070 hex with Bit 7 low; NMI is disabled by writing to I/O addresss 070 hex with Bit 7 high.

Rating Specifications

Absolute Maximum Ratings*

TA = 25° C

Parameter	Symbol	Min	Max	Unit
Power supply voltage	V_{CC}	-0.5	7.0	V
Power dissipation (@5.25 V)	W_d		1	W
Current (@5.25 V)	I_{DD}	20	50	mA
Input voltage	V_I	-0.5	VCC+0.5	V
Output voltage	V_O	-0.5	VCC+0.5	V
Operating temperature	T_{op}	0	70	°C
Storage temperature	T_{stg}	-50	150	°C

* Exposing the device to stress above these limits can cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Capacitance Limits

TA = +25° C, VCC = 5 V

Parameter	Symbol	Min	Max	Unit	Test Condition
Input capacitance	C_I		10	pF	fc = 1 MHz unmeasured pins at GND
I/O capacitance	C_{IO}		15	pF	

DC Characteristics

TA = 0° C to +70° C, VCC = +5 V +/- 10%

DRQ0-3, DRQ5-7, TMODE, HLDA, SA9, IOCHRDY, RESET, /PAR, SYSCLK, /MASTER, /IOCHCK, IRQ3-15, KBINT, /INTA, OSC

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 +/- 0.5 V
Input low current	IIL		-10	uA	VIN > VSS
Input high current	IIH		-10	uA	VIN < VCC

XD0-7

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.2VCC - 0.1 V		VCC = 5 +/- 0.5 V
Input high voltage	VIH	0.2VCC + 0.9	VCC	V	VCC = 5 +/- 0.5 V
Input low current	IIL		-10	uA	VIN > 0.0V
Input high current	IIH		10	uA	VIN < VCC
Output low voltage	VOL		0.45	V	IOL = 3.2mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA
Tristate leakage current	IOZ	-10	10	uA	0 V < VOUT < VCC

SA0-6, SA8, /REFRESH, /MEMR, /MEMW, /IOW, /IOR

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.2VCC - 0.1	V	VCC = 5V +/- 5%
Input high voltage	VIH	0.7VCC	VCC	V	VCC = 5V +/- 5%
Input low current	IIL		-10.0	uA	VIN > VSS
Input high current	IIH		10.0	uA	VIN < VCC
Output low voltage	VOL		0.45	V	IOL = 9.6mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA
Tristate leakage current	IOZ	-10.0	10.0	uV	0V < VOUT < VCC

NPCS, ADSTB8, /DACK1-3, /EDACK, CH/F, NMI, SPEAKER, HOLD, ADSTB16, /DAEN1-2, INTR

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 3.2mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA

T/C

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 9.6mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA

A17-23

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 3.2mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA
Tristate leakage current	IOZ	-10.0	10.0	uA	0V < VOUT < VCC

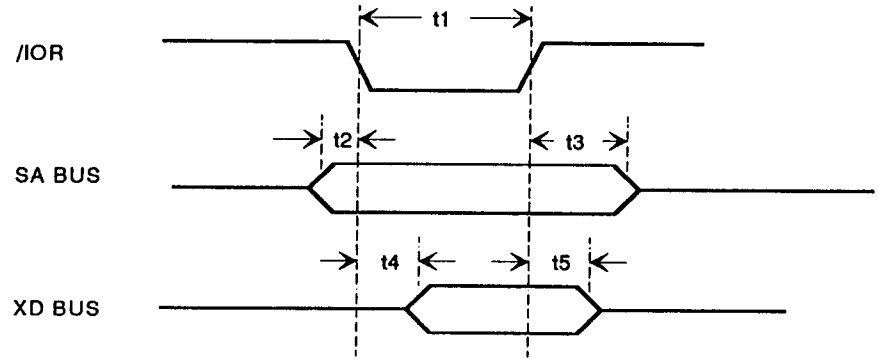
SA16

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 9.6mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA
Tristate leakage current	IOZ	-10.0	10.0	uA	0V < VOUT < VCC

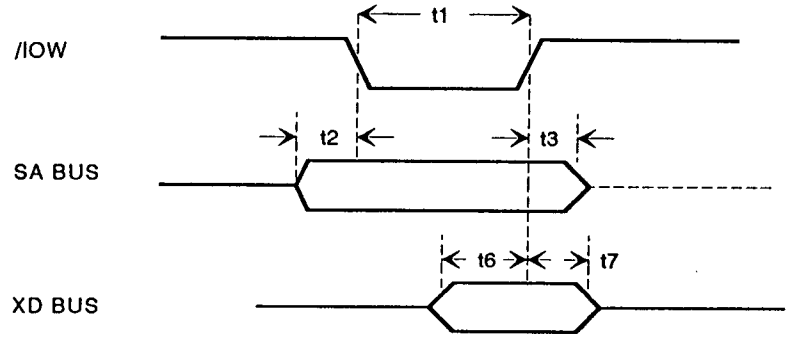
AC Specifications

Symbol	Parameter	Min	Max	Units
t1	/IOR or /IOW pulse width	110		ns
t2	SA address valid to /IOR /IOW low setup time	25		ns
t3	SA address hold time from /IOR /IOW high	13		ns
t4	XD data valid delay from /IOR low		110	ns
t5	XD data float delay from /IOR high	0	90	ns
t6	XD data valid to /IOW high setup time	70		ns
t7	XD data hold time from /IOW high	15		ns
t8	RESET high pulse width	250		ns
t9	RESET inactive to first /IOR or /IOW command	4		SYSCLK Cycle
t10	Command recovery time between successive /IOR or /IOW pulses	125		ns
t11	CH/F valid from /IOW high delay		60	ns
t12	NPCS valid from address delay		51	ns
t13	NMI output delay		68	ns

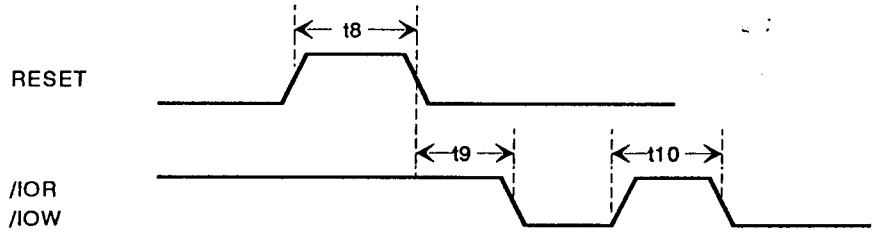
Peripheral Read Timing



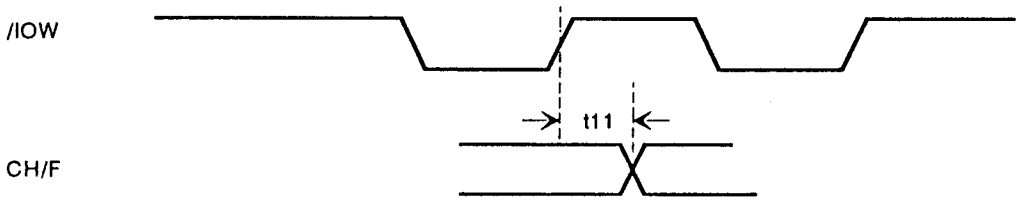
Peripheral Write Timing

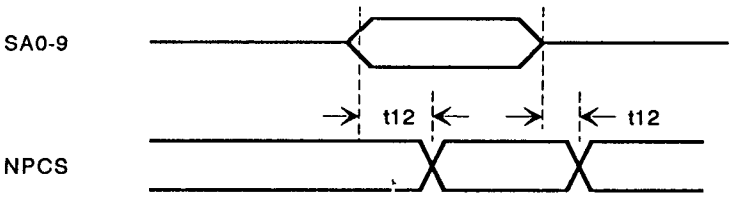


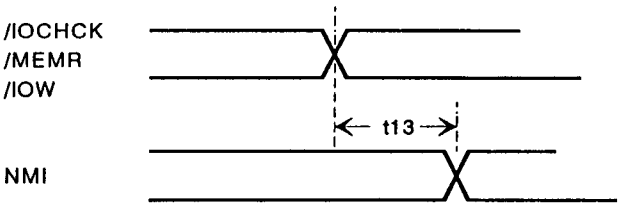
Command and Reset Timing



Other Timing Waveforms



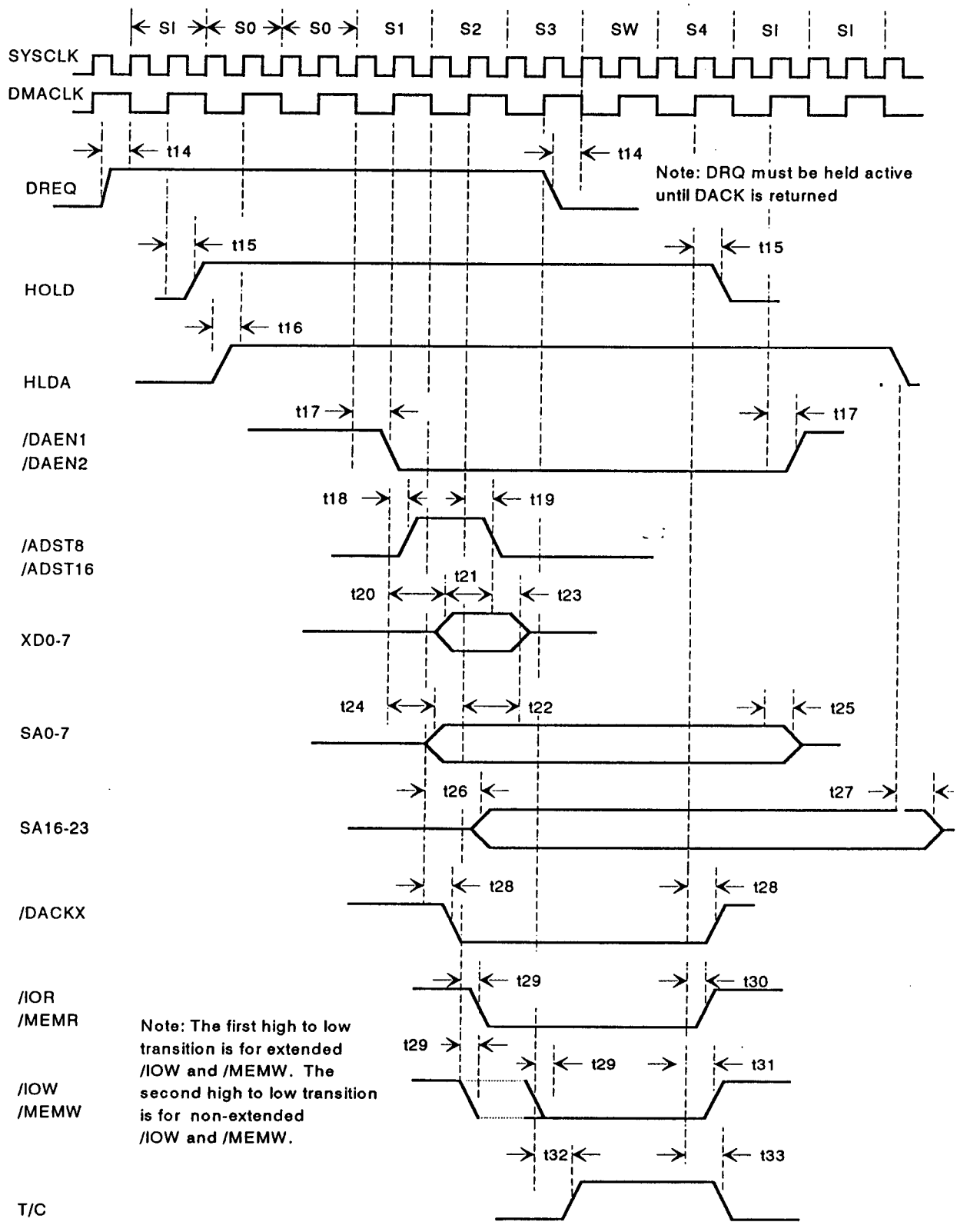




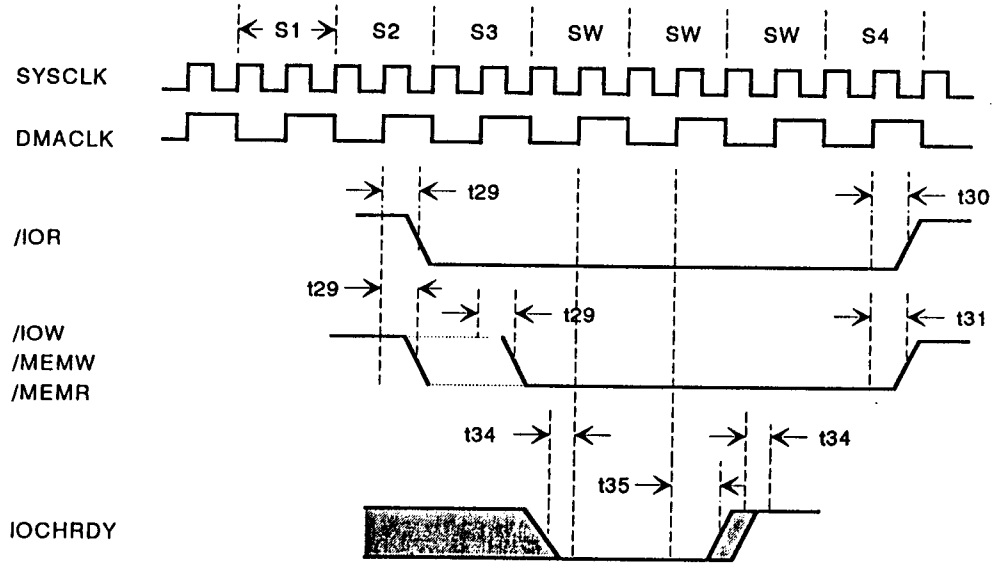
AC Specifications

Symbol	Parameter	Min	Max	Units
t14	DRQ to SYSCLK high setup time	0		ns
t15	HOLD valid from SYSCLK high delay time		50	ns
t16	HLDA to SYSCLK high setup time	25		ns
t17	/DAEN1 valid from SYSCLK high delay time		77	ns
t18	ADSTB8 or ADSTB16 high from SYSCLK high		72	ns
t19	ADSTB8 or ADSTB16 low from SYSCLK high delay time		76	ns
t20	Data float to active delay from SYSCLK high		93	ns
t21	Data to ADSTB8 or ADSTB16 low set up time	70		ns
t22	Data active to float delay from SYSCLK high		92	ns
t23	Data from ADSTB8 or ADSTB16 low HOLD time	8		ns
t24	low byte ADDR float to active from SYSCLK high		180	ns
t25	low byte ADDR active to float delay from SYSCLK high		70	ns
t26	high byte ADDR float to active delay from SYSCLK high		123	ns
t27	high byte add active to float from HLDA low		35	ns
t28	/DACK valid from SYSCK high delay time		83	ns
t29	/IOR, /IOW, /MEMR, /MEMW active from SYSCLK high delay time		53	ns
t30	/IOR and /MEMR inactive from SYSCLK high delay time		97	ns
t31	/IOW and /MEMW inactive from SYSCLK high delay time		80	ns
t32	T/C active from SYSCLK high delay time		82	ns
t33	T/C inactive from SYSCLK high delay time		82	ns
t34	IOCHRDY input setup time to SYSCLK high	26		ns
t35	IOCHRDY input hold time from SYSCLK high	15		ns

DMA Timing


SI
S0
S0
S1
S2
S3
SW
S4
SI
SI
SYSCLK
DMACLK
t14
t14
DREQ
Note: DRQ must be held active until DACK is returned
t15
t15
HOLD
t16
HLDA
t17
t17
/DAEN1
/DAEN2
t18
t19
/ADST8
/ADST16
t21
t20
t23
XD0-7
t24
t22
t25
SA0-7
t26
t27
SA16-23
t28
t28
/DACKX
t29
t30
/IOR
/MEMR
t29
t29
t31
/IOW
/MEMW
t32
t33
T/C
Note: The first high to low transition is for extended /IOW and /MEMW. The second high to low transition is for non-extended /IOW and /MEMW.

IOCHRDY Timing

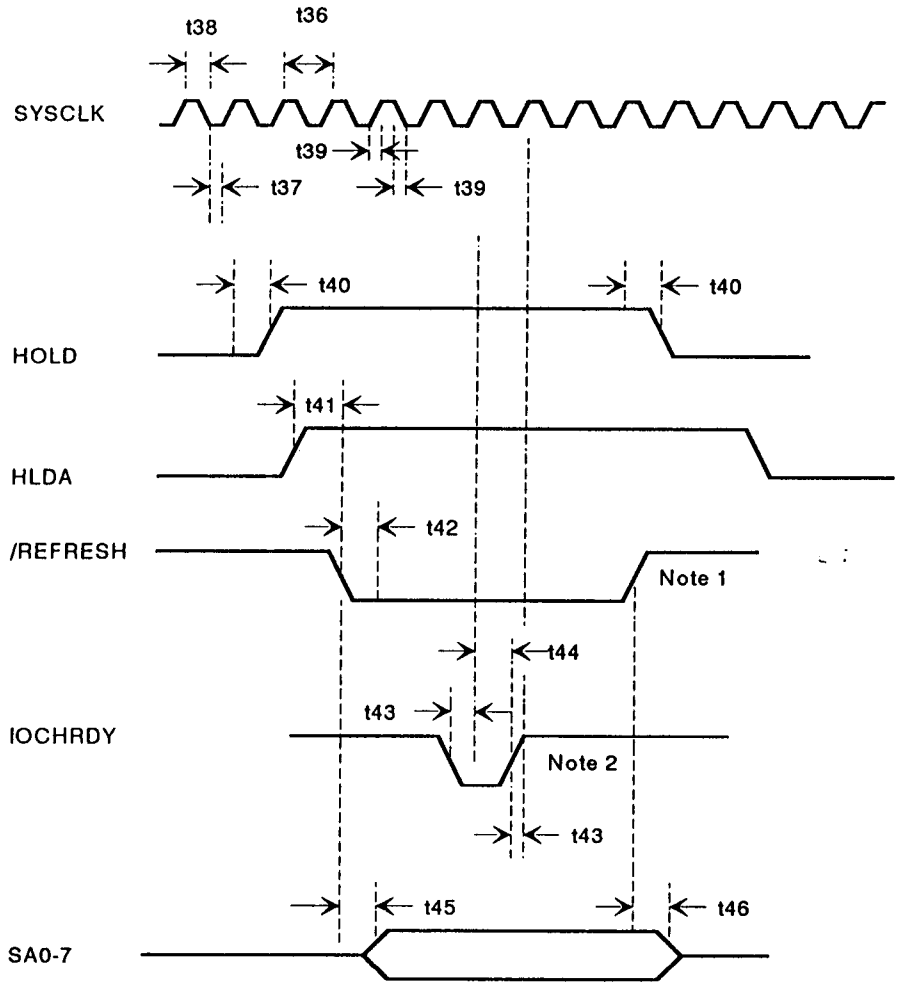


The first wait state is inserted by the internal circuitry of the ACC 2000 for all DMA cycles. Additional wait states must be inserted using IOCHRDY.

AC Specifications

Symbol	Parameter	Min	Max	Units
t36	SYSCLK cycle time	62		ns
t37	SYSCLK pulse width low	25		ns
t38	SYSCLK pulse width high	25		ns
t39	SYSCLK rise/fall time	10		ns
t40	HOLD valid from SYSCLK high delay time		50	ns
t41	/REFRESH low delay from HLDA		40	ns
t42	/REFRESH low to SYSCLK high setup time		20	ns
t43	IOCHRDY input setup time to SYSCLK high	26		ns
t44	IOCHRDY input hold time from SYSCLK high	15		ns
t45	REFRESH address valid delay from /REFRESH		92	ns
t46	Refresh address hold time from /REFRESH inactive		88	ns

Refresh Timing



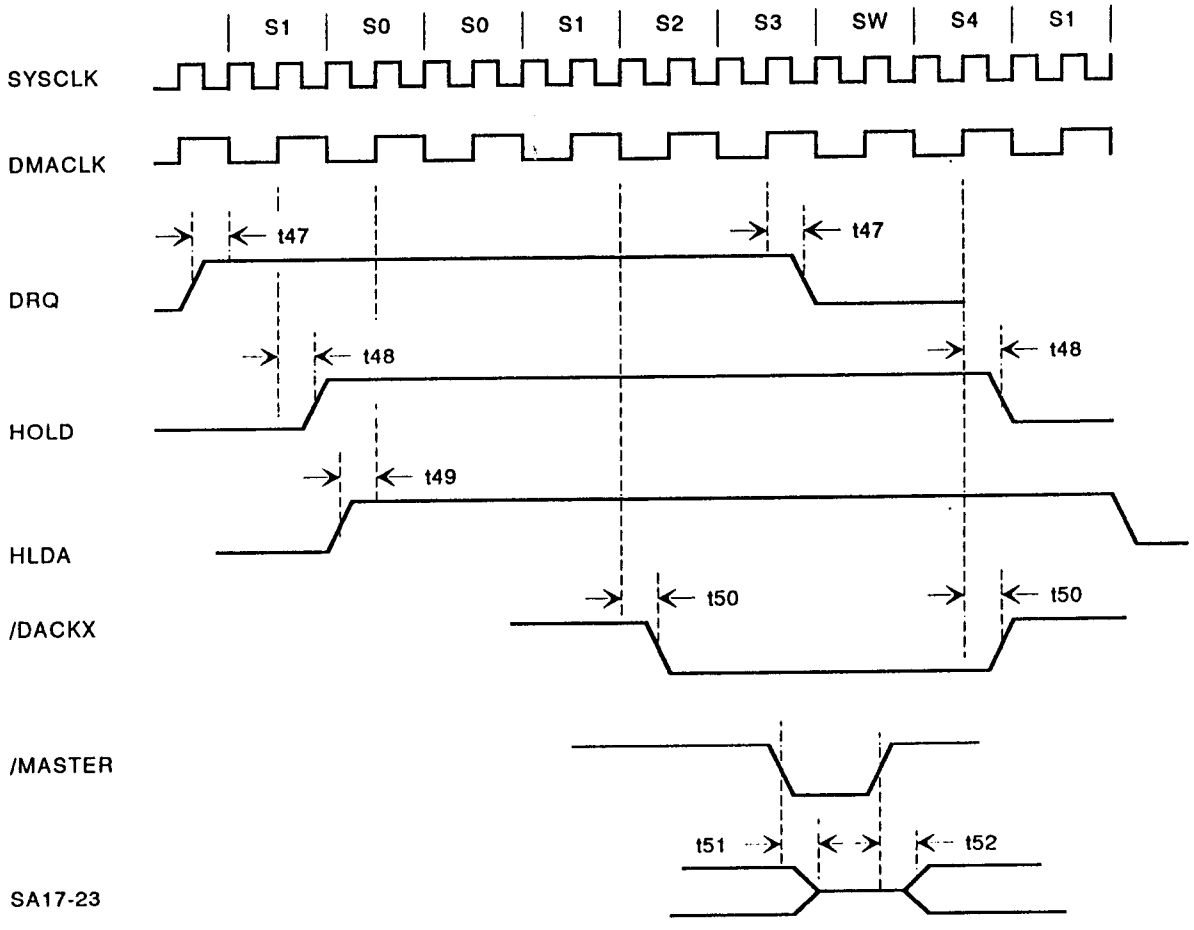
Notes

1 A /REFRESH pulse is normally four SYSCLK cycles long.
2 /REFRESH cycles can be extended by inserting wait states using IOCHRDY.

AC Specifications

Symbol	Parameter	Min	Max	Units
t47	DRQ to SYSCLK high setup time	0		ns
t48	HOLD valid from SYSCLK high delay time		50	ns
t49	HLDA to SYSCLK high set up time	25		ns
t50	/DACK valid from SYSCLK high delay time		83	ns
t51	SA17-SA23 float from /MASTER low delay time	11	36	ns
t52	SA17-SA23 active from /MASTER high delay time	11	36	ns

/MASTER Timing

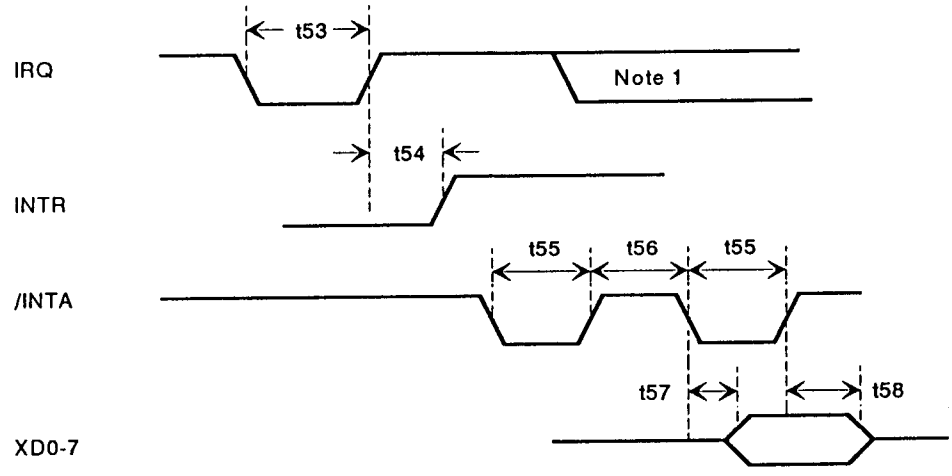


Note: A new bus master must be programmed in Cascade mode.
The new master must not pull /MASTER low until it has received the corresponding /DACK signal.

AC Specifications

Symbol	Parameter	Min	Max	Units
t53	Interrupt request pulse width low	60		ns
t54	Interrupt output delay		63	ns
t55	/INTA pulse width low	80		ns
t56	/INTA to next /INTA within an INTA sequence only	120		ns
t57	XD data valid delay from /INTA low		109	ns
t58	XD data float delay from /INTA high	22	69	ns

Interrupt Timing

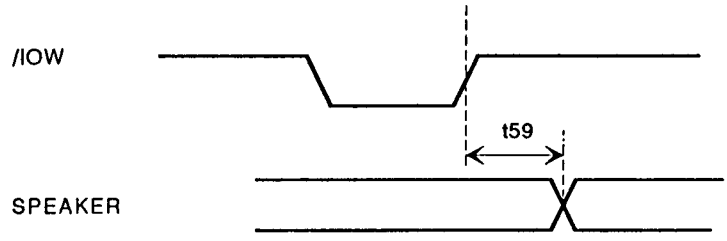


Note 1 IRQ must remain active until the first /INTA pulse.

AC Specifications

Symbol	Parameter	Min	Max	Units
t59	SPEAKER valid from /IOW high delay time		100	ns

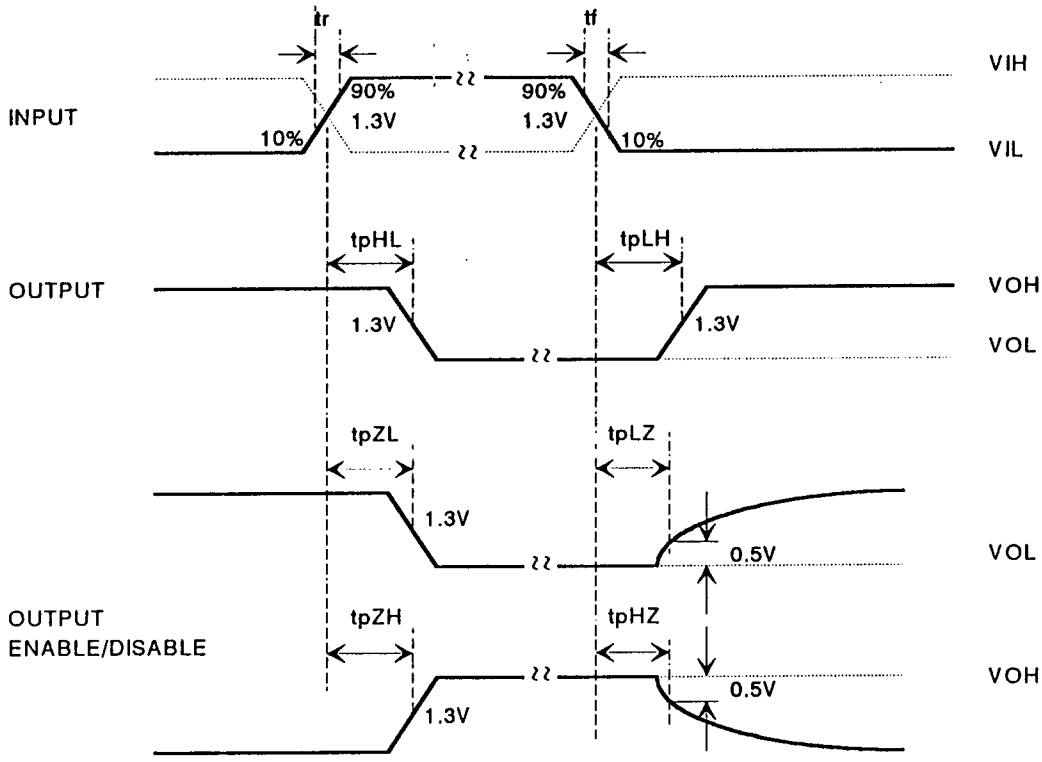
8254 Timing



Load Circuit and AC Characteristics Measurement

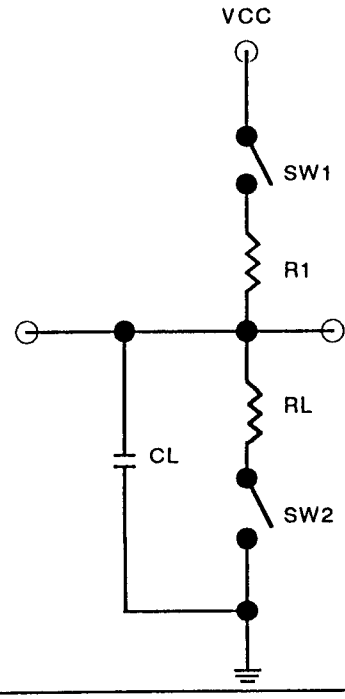
Parameter	Output Type	Symbol	CL(pF)	R1	RL	SW1	SW2
Propagation	Totem pole						
Delay	3-state	tPLH	50		1.0K	off	on
		tPHL	50		1.0K	off	on
Time	Bidirectional						
Propagation	Open drain or	tPLH	50	0.5K		on	off
Delay time	Open collection	tPHL	50	0.5K		on	off
Disable time	3-state	tPLZ	5	0.5K	1.0K	on	on
	Bidirectional	tPHZ	5	0.5K	1.0K	off	on
Enable time	3-state	tPZL	50	0.5K	1.0K	on	on
	Bidirectional	tPZH	50	0.5K	1.0K	off	on

AC Characteristics Measurement



VIH = 3 V, VIL = 0, tr ≤ 10 ns, tf ≤ 5 ns

Load Circuit



ACC 2300
Page/Page Interleaved Memory Controller

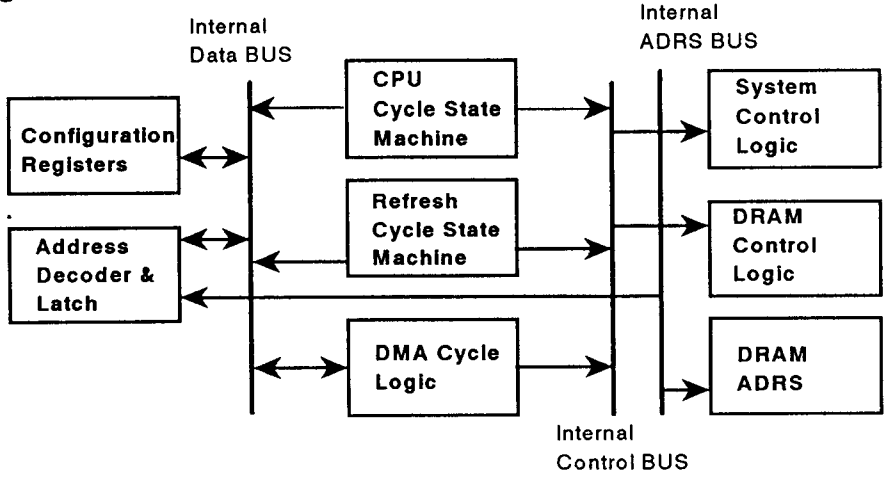
The ACC 2300 is an integrated high performance CMOS Memory Controller for an 80386 based system. The ACC 2300 performs in two modes: the Page/Page Interleaved mode, or the Direct Access mode. The memory configurations in either mode can be one bank (non-interleaved) or multiple banks (2 or 4) interleaved. This flexible configuration supports up to 16 MB of DRAMs with 1 Mbit DRAMs. With the ACC 2500 and the ACC 2000, the complete 386 chip set offers a 100% PC/AT* compatible integrated solution for designers to build a powerful 20/25 MHz 386 workstation.

Features

- High performance Page interleaved or Direct DRAM accessing
- Flexible memory configurations of 1, 2, and 4 banks by using either 256K x 1 and 256K x 4, or 1M x 1 DRAMs
- Automatic remapping of the RAM in 512K (640K) to 1 MB address space
- Staggered refresh to reduce power supply noise
- Shadow RAM for efficient BIOS execution
- Supports up to 16 MB on-board memory
- Supports 20 MHz zero wait state by using 80 ns 286K x 1 or 100 ns 256K x 4 or 100 ns 1M x 1 Fast Page mode DRAMs in Page mode
- Supports 25 MHz zero wait state by using 80 ns 256 x 4 or 1M x 1 DRAMS in Page interleaved mode
- 100-pin PFP package

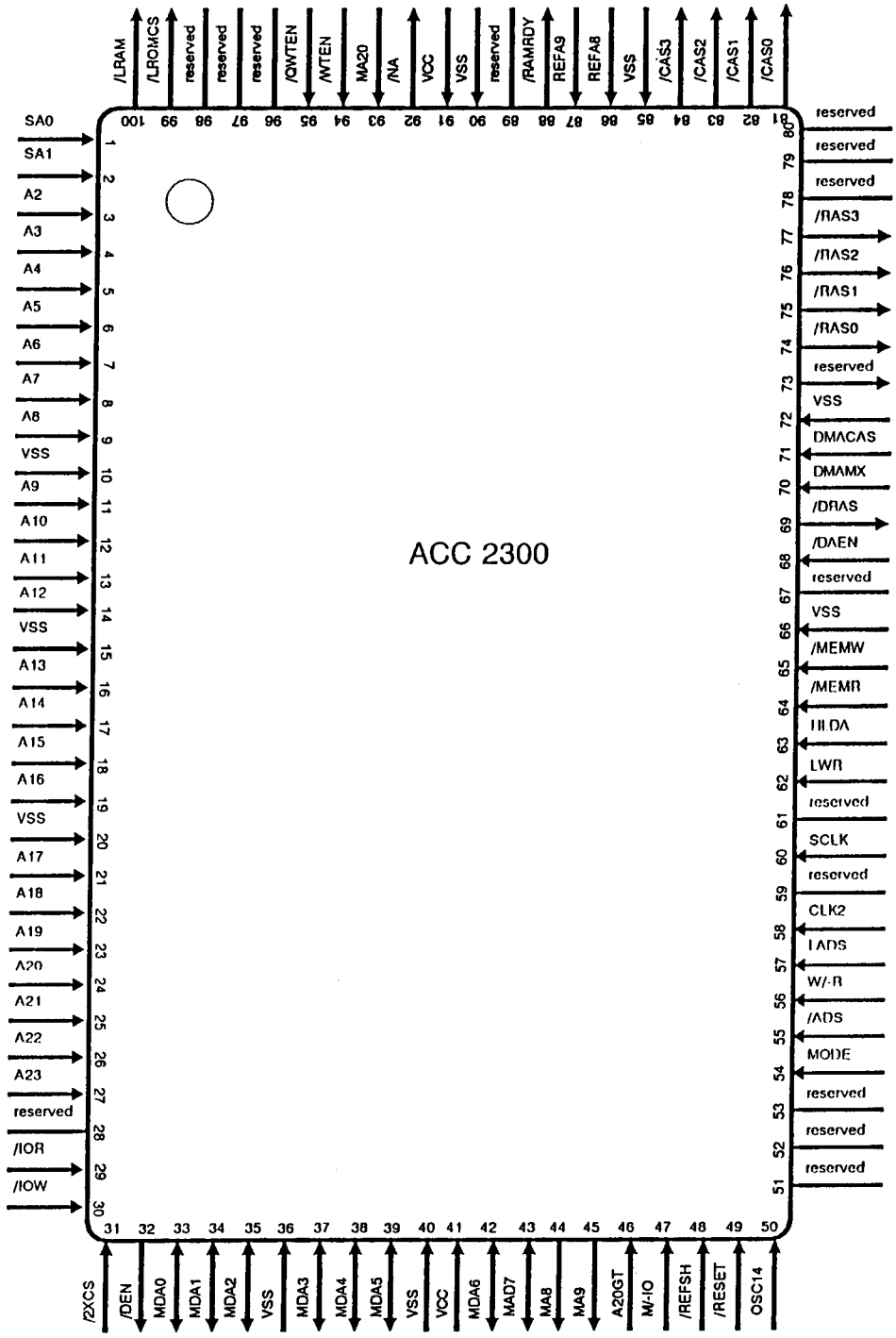
* Trademarks of International Business Machines

Block Diagram



ACC Microelectronics Corporation · 3295 Scott Blvd. · Santa Clara, CA 95054
Phone: 408-980-0622 FAX: 408-980-0626

Pin Diagram


ACC 2300
SA0
SA1
A2
A3
A4
A5
A6
A7
A8
VSS
A9
A10
A11
A12
VSS
A13
A14
A15
A16
VSS
A17
A18
A19
A20
A21
A22
A23
reserved
/IOR
/IOW
/LRAM
/LROMCS
reserved
reserved
reserved
/CWTEN
/WTEN
MA20
/NA
VCC
VSS
reserved
/RAMRDY
REFA9
REFA8
VSS
/CAS3
/CAS2
/CAS1
/CAS0
reserved
reserved
reserved
/RAS3
/RAS2
/RAS1
/RAS0
reserved
VSS
DMACAS
DMAMX
/DRAS
/DAEN
reserved
VSS
/MEMW
/MEMR
HLDA
LWR
reserved
SCLK
reserved
CLK2
LADS
W/-R
/ADS
MODE
reserved
reserved
reserved
/2XCS
/DEN
MDA0
MDA1
MDA2
VSS
MDA3
MDA4
MDA5
VSS
VCC
MDA6
MAD7
MA8
MA9
A20GT
M-IO
/REFSH
/RESET
OSC14

Pin Descriptions

Symbol	Pin	I/O	Pin Description
SA0	1	I	System address bit.
SA1	2	I	
A2	3	I	Local address bit.
A3	4	I	
A4	5	I	
A5	6	I	
A6	7	I	
A7	8	I	
A8	9	I	
A9	11	I	
A10	12	I	
A11	13	I	
A12	14	I	
A13	16	I	
A14	17	I	
A15	18	I	
A16	19	I	
A17	21	I	
A18	22	I	
A19	23	I	
A20	24	I	
A21	25	I	
A22	26	I	
A23	27	I	
reserved	28		
/IOR	29	I	I/O read command for I/O ports 22 and 23.
/IOW	30	I	I/O write command for I/O ports 22 and 23.
/2XCS	31	I	I/O ports 22 and 23 chip select.
/DEN	32	O	I/O cycle bus buffer enable for I/O ports 22 and 23.
MDA0	33	I/O	Multiplexed data and address bit. It is a data I/O pin when used to program a configuration register and functions as an address output pin under normal conditions.
MDA1	34	I/O	
MDA2	35	I/O	
MDA3	37	I/O	
MDA4	38	I/O	
MDA5	39	I/O	
MDA6	42	I/O	
MDA7	43	I/O	

Pin Descriptions

Symbol	Pin	I/O	Pin Description
MA8	44	O	DRAM address bit
MA9	45	O	
A20GT	46	I	A20GATE input
M/-IO	47	I	Bus cycle status for memory or I/O
/REFSH	48	I	Refresh cycle
/RESET	49	I	System reset
OSC14	50	I	14 MHz clock input
MODE	54	I	Selects between Page Mode and Direct Access Mode
/ADS	55	I	Address data strobe from 80386
W/-R	56	I	Write/read from 80386
LADS	57	I	Latched ADS signal
CLK2	58	I	Processor clock input
SCLK	60	I	Reference clock for CLK2
LWR	62	I	Latched write/read signal
HLDA	63	I	Hold acknowledge input
/MEMR	64	I	AT bus cycle memory read command
/MEMW	65	I	AT bus cycle memory write command
/DAEN	68	I	DMA cycle address enable
/DRAS	69	O	DMA cycle RAS output
DMAMX	70	I	DMA cycle MUX input
DMACAS	71	I	DMA cycle CAS input
/RAS0	74	O	Bank 0, row address strobe
/RAS1	75	O	Bank 1, row address strobe
/RAS2	76	O	Bank 2, row address strobe

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/RAS3	77	O	Bank 3, row address strobe
/CAS0	81	O	Bank 0, column address strobe
/CAS1	82	O	Bank 1, column address strobe
/CAS2	83	O	Bank 2, colunm address strobe
/CAS3	84	O	Bank 3, column address strobe
REFA8 REFA9	86 87	I I	Refresh address bit.
/RAMRDY	88	O	RAM ready output
/NA	92	O	Next address request output to 80386
MA20	93	I	A20 input
/WTEN	94	I	Write enable signal input
/QWTEN	95	O	Qualified RAM write enable control
/LROMCS	99	O	ROM BIOS cycle chip select
/LRAM	100	O	Local RAM cycle
VCC	41, 91		+5 volt supply
VSS	10, 15, 20, 36 40, 66, 72, 85, 90		Ground
Reserved	51, 52, 53, 59, 61, 67, 73, 78, 79, 80, 89, 96, 97, 98		

Functional Description

Configuration Registers

There are two configuration registers in the ACC 2300. They are accessed through I/O ports 22H and 23H by writing the index of the desired register into Port 22H, then accessing 23H for the data.

The ACC 2300 configuration registers have the following features:

- Define the base address as 512K or 640K, and can remap the remaining 512K or 384K to the address range just below 16MB.
- Define the relocation of 128K RAM space normally reserved for BIOS. Relocation can start at FE0000, or start at 0E0000 and use the space as a shadow RAM. The 128K can be read only or read/write.
- Select Direct Access mode when the MODE pin is set to zero. Selects Page mode or page interleaved mode when the MODE pin is set to one.
- Control the RAS timeout to accommodate RAMs with 10 us RAS pulse widths.
- Enable Banks 2 and 3 to get four banks of RAM.
- Control RAS precharge time to compensate for no Fast Page mode RAM

Table 1 defines the configuration registers.

Address Decoder and Latch

The addresss decoder identifies the address range available based on options specified in the configuration registers.

Input addresses are latched internally to maintain the current addresses until the end of the cycle.

When Page interleaved mode is selected with two banks, the page numbers are incremented so that the even-numbered bank contains the even-numbered pages and the odd-numbered bank contains the odd-numbered pages.

When four banks are used in Page interleaved mode, Banks 2 and 3 are incremented with odd pages in Bank 3, and even pages in Bank 2.

Table 2 lists the memory sizes available with the memory options.

Row and column address definitions are specific to the mode selected. Table 3 lists the definitions for Page interleaved mode.

State Machines

The ACC 2300 has three state machines to control CPU access, DMA, and refresh cycle access. The /REF and HLDA input signals control which state machine is activated.

There is a CPU state machine for each of the two modes supported by the ACC 2300. The CPU state machine generates all timing control signals for DRAM Banks 0-3 according to the configuration register set-up.

The DMA cycle state machine generates control signals to the RAM during a DMA cycle.

The refresh cycle state machine generates control signals for RAM refresh. The refresh method is a staggered refresh to reduce power noise.

Table 1 ACC 2300 Configuration Registers

Bit	State	Function
Index 00H		
7		DRAM Type
	0	256K x 1 (default)
	1	1M x 1
6		DRAM RAS Timeout
	0	RAS timeout enable (default)
	1	RAS timeout disable
5		Banks 2 and 3 Enable
	0	Disable banks 2 and 3(default)
	1	Enable banks 2 and 3
4		128K DRAM Relocation
	0	128K DRAM is addressed starting at FE0000 (default)
	1	128K DRAM is addressed starting at 0E0000
3		128K Read/Write Control
	0	Read/write (default)
	1	Read only
2		Map Control
	0	Map disable (default)
	1	Map enable
1		Base Address Select
	0	512KB based (default)
	1	640KB based
0		Single Bank/Interleave Select *
	0	Disable interleave (default)
	1	Enable interleave

Bit	State	Function
Index 01H		
7		reserved
6		reserved
5		reserved
4		reserved
3		Banks 2 and 3 RAS Precharge
	0	6 CLK2 precharge time (default)
	1	4 CLK2 precharge time
2		Banks 2 and 3 Read Cycle Wait
	0	One wait state (default)
	1	Zero wait state
1		Banks 0 and 1 RAS Precharge
	0	6 CLK2 precharge time (default)
	1	4 CLK2 precharge time
0		Banks 0 and 1 Read Cycle Wait
	0	One wait state (default)
	1	Zero wait state

* When interleaving is selected, the Read cycle must be zero wait state. This includes both Bank 0, 1 and Bank 2, 3.

Table 2 Memory Size Selection

	Page Mode	Memory Size	Pages
Bank 0	256K x 1	1M	512
	1M x 1	4M	2048
	Page Interleaved	**Memory Size**	**Pages**
Bank 0 & 1	256K x 1	2M	1024
	1M x 1	8M	4096
Bank 0 - 3	256K x 1	4M	2048
	1M x 1	16M	8192

Table 3 Page Mode Row and Column Address Definitions

Bank 0	Bank 1	Bank 2	Bank 3	RAM Type	Row	Column
X				256K x 1	A<18:11>	A<10:2>
X				1M x 1	A<21:12>	A<11:2>
X	X			256K x 1	A<20:12>	A<10:2>
X	X			1M x 1	A<21:12>	A<22>, A<10:2>
X	X	X	X	256K x 1	A<20:12>	A<10:2>
X	X	X	X	1M x 1	A<21:12>	A<22>, A<10:2>

DRAM Control Logic

DRAM control logic generates RAS and CAS and write enable signals for all system DRAM.

DRAM Address

MDA0 through MDA7, MA8 and MA9 are the RAM addresses for the CPU, DMA, and refresh cycles. MDA0 through MDA7 are also used as data I/O when accessing internal configuration registers.

System Control Logic

The system control logic generates a /DEN signal to control the data buffer during the configuration I/O cycle.

The X BUS is equal to the P BUS.

Rating Specifications

Absolute Maximum Ratings*

Parameter	Symbol	Condition	Min	Max	Unit
Power supply voltage	VCC	Ta=25° C	-0.3	7.0	V
Input voltage	VI	VSS=0	-0.3	VCC+0.3	V
Output voltage	VO		-0.3	VCC+0.3	V
Operating temperature	Top		-25	85	C
Storage temperature	Tstg		-40	125	C

* Exposing the device to stress above these limits can cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operations sections of this specifiction. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	VCC		4.75	5.25	V
Ambient temperature	TA		0	70	C

DC Specifications

TA =0°C to 70°C, VCC = +5V +/- 5%

Group 1 INPUT

A20GT, M/-IO, /REFSH, /RESET, OSC14, MODE, /ADS, W/-R, LADS, CLK2, SCLK, LWR, HLDA, /DAEN, DMAMX, DMACAS, REFA8, REFA9, MA20, /WTEN,

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V +/- 0.25 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 V +/- 0.25 V
Input low current	IIL	-10	10	uA	VIN = 0.0 V
Input high current	IIH	-10	10	uA	VIN = VCC

Group 2 INPUT WITH PULLUP

SA0, SA1, A2-A23, /IOR, /IOW, /2XCS, /MEMR, /MEMW,

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V +/- 0.25 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 V +/- 0.25 V
Input low current	IIL	-200	-10	uA	VIN = 0.0 V
Input high current	IIH	10	200	uA	VIN=VCC

Group 3 OUTPUT

/DRAS, /NA, /DEN, /QWTEN, /RAMRDY

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 4.0 mA
Output high voltage	VOH	2.4		V	IOH = -4.0 mA

/RAS0, /RAS1, /RAS2, /RAS3, /CAS0, /CAS1, /CAS2, /CAS3, /LROMCS, /LRAM

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 8.0 mA
Output high voltage	VOH	2.4		V	IOH = -8.0 mA

Group 4 TRISTATE OUTPUT

MA8, MA9

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 8.0 mA
Output high voltage	VOH	2.4		V	IOH = -8.0 mA
Tristate leakage current	IOZ	-10.0	10.0	uA	0V < VOUT < VCC

Group 5 INPUT/OUTPUT WITH PULLUP

MDA0-MDA7

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V +/- 0.25 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 V +/- 0.25 V
Output low voltage	VOL		0.4	V	IOL = 8.0 mA
Output high voltage	VOH	2.4		V	IOH = -8.0 mA
Tristate leakage current	IOZ	-200	-10	uA	0V < VOUT < VCC

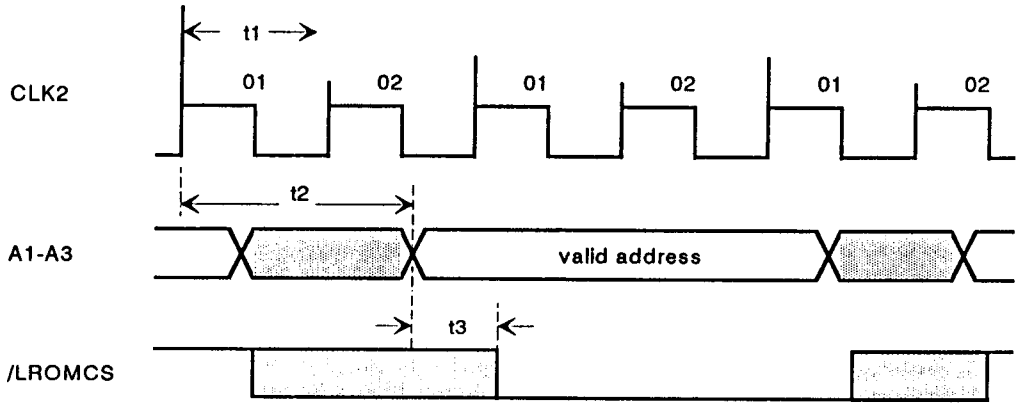
AC Specifications

50 pf load output

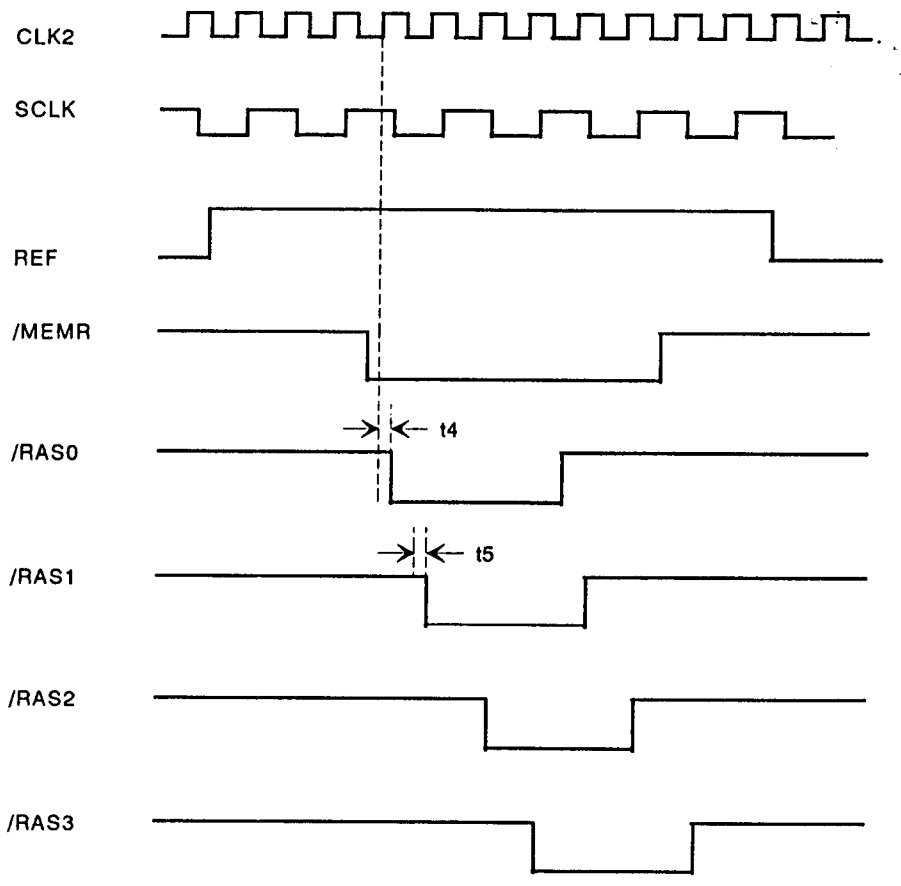
Symbol	Description	Min	Typ	Max	Units
t1	CLK2 period	25			ns
t2	A2-A31 valid delay			32	ns
t3	/LROMCS active delay from valid address		15		ns
t4	/RAS0 active delay from CLK2 in refresh cycle		6.5		ns
t5	/RAS1-/RAS3 active delay from CLK2 in refresh cycle		7.5		ns
t8	/RAS active delay from /MEMR or /MEMW active in DMA cycle		7		ns
t9	/MUX delay from /RAS active in DMA cycle			40	ns
t10	/CAS delay from /RAS active in DMA cycle			80	ns
t11	Row address setup time to /RAS active in DMA cycle	200			ns
t12	Row address hold time to /RAS active in DMA cycle	40			ns
t13	Column address setup time to /CAS active in DMA cycle	35			ns
t14	/WTEN active delay from CLK2 in DMA cycle		11		ns
t15	/2XCS setup time to IO command active	55			ns
t16	XA0 setup time to IO command active	60			ns
t17	/DEN active delay from active IO command		5.5		ns
t18	/LRAM active delay from valid address		16		ns
t19	/NA active delay from CLK2 in local RAM cycle		6		ns
t20	/CAS active delay from CLK2 in local RAM cycle		6		ns

Symbol	Description	Min	Typ	Max	Units
t21	/RAMRDY active delay from CLK2 in local RAM cycle		6.5		ns
t22	LWR active delay from CLK2 in local RAM cycle		15		ns
t23	Column valid address delay from valid address input in local RAM cycle		6		ns
t24	/RAS active delay from CLK2 in local RAM cycle		6		ns
t25	Row address setup time to /RAS active in local RAM cycle	15			ns
t26	Column address setup time to /CAS active in local RAM cycle	15			ns
t27	/WTEN active delay from CLK2 in local RAM cycle		16		ns

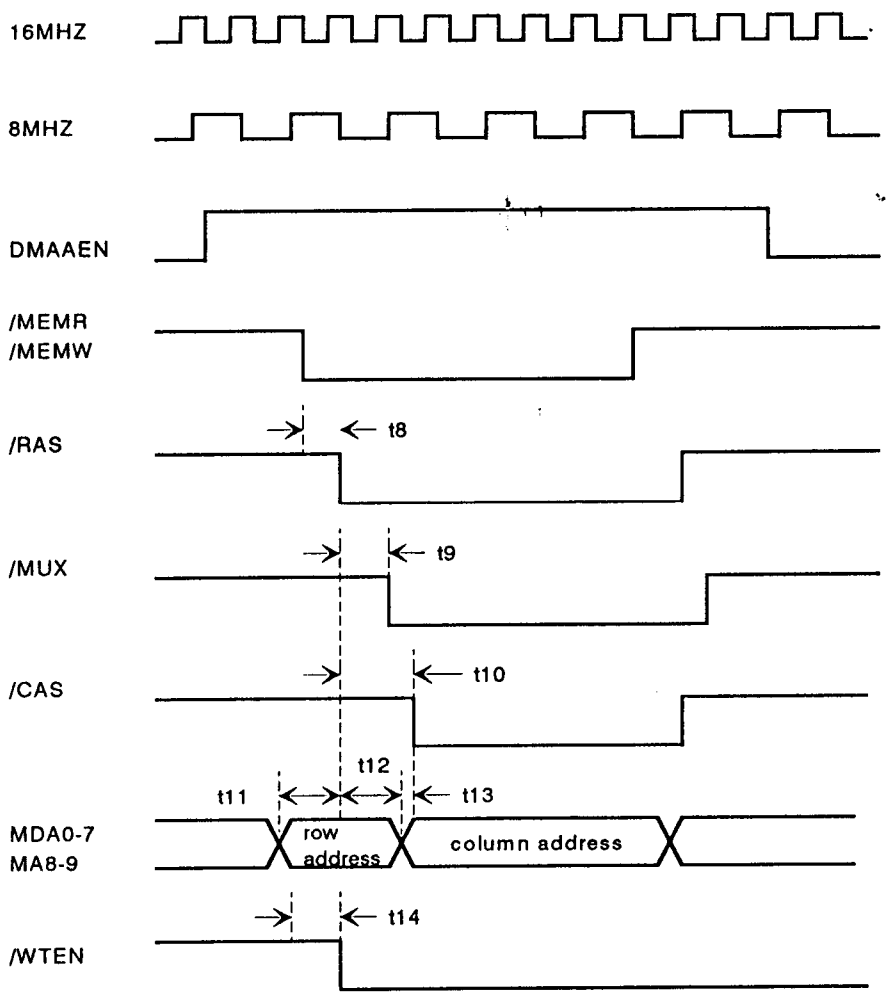
ROM Read Cycle



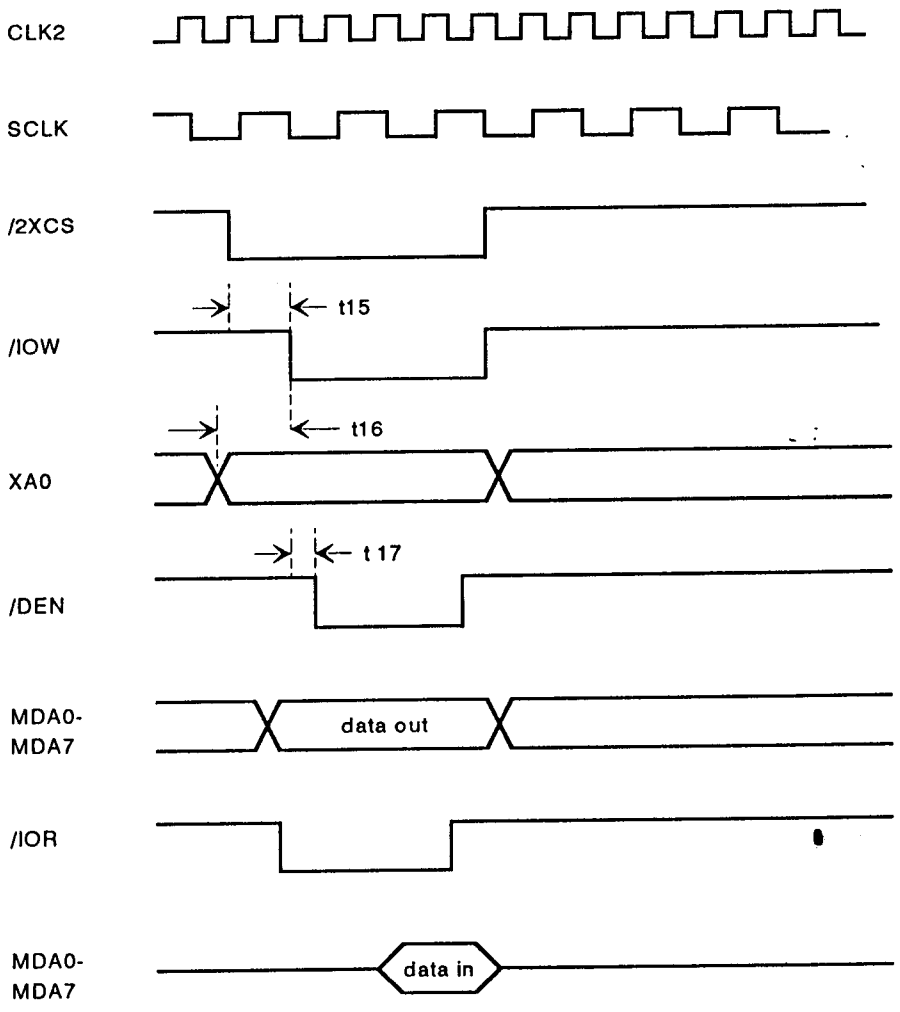
Refresh Cycle



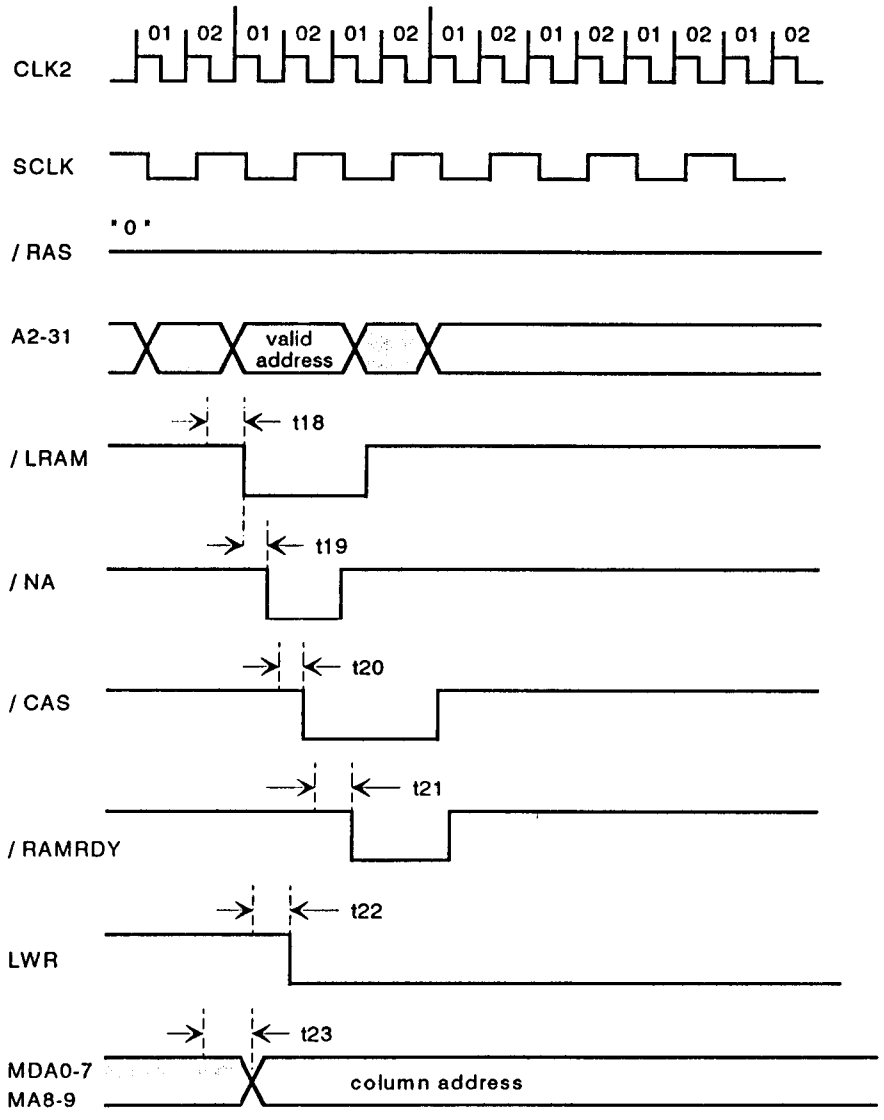
DMA Cycles


16MHZ
8MHZ
DMAAEN
/MEMR
/MEMW
/RAS
t8
/MUX
t9
/CAS
t10
t12
t11
t13
MDA0-7
MA8-9
row address
column address
t14
/WTEN

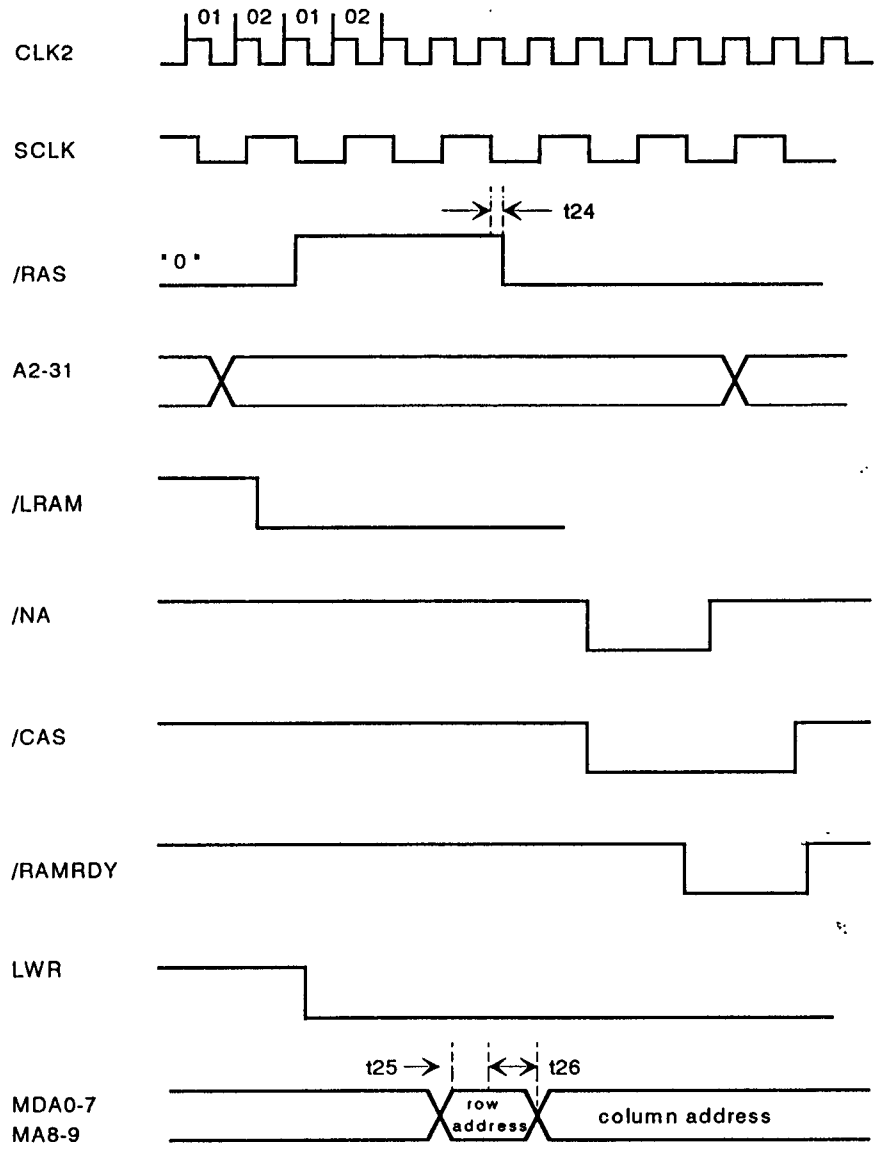
I/O Read/Write Cycle



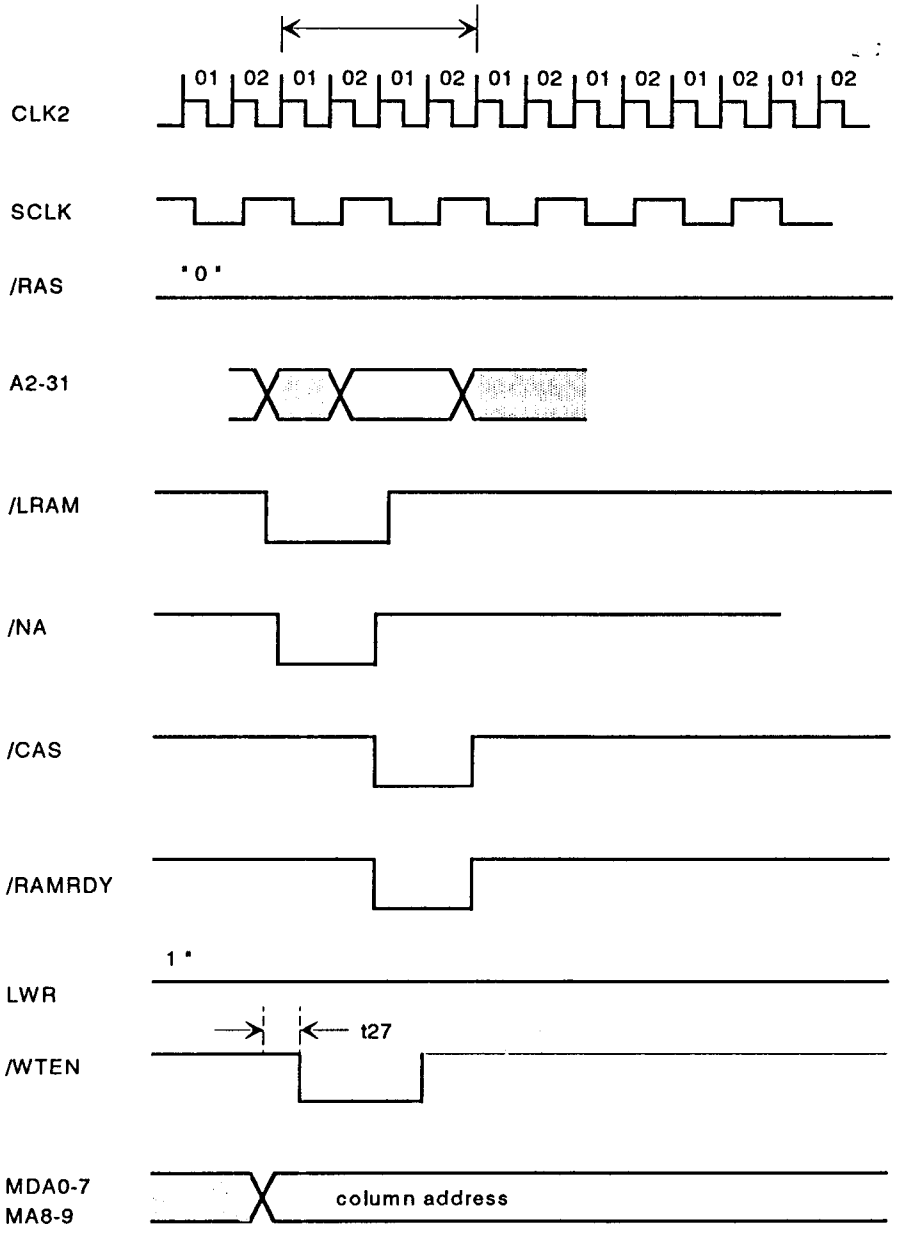
Local RAM Cycle, Read Hit 0WS, RAS Active



Local RAM Cycle, Read Miss, RAS Active



Local RAM Cycle, Write 0 WS, RAS Active



ACC 2500
System Controller

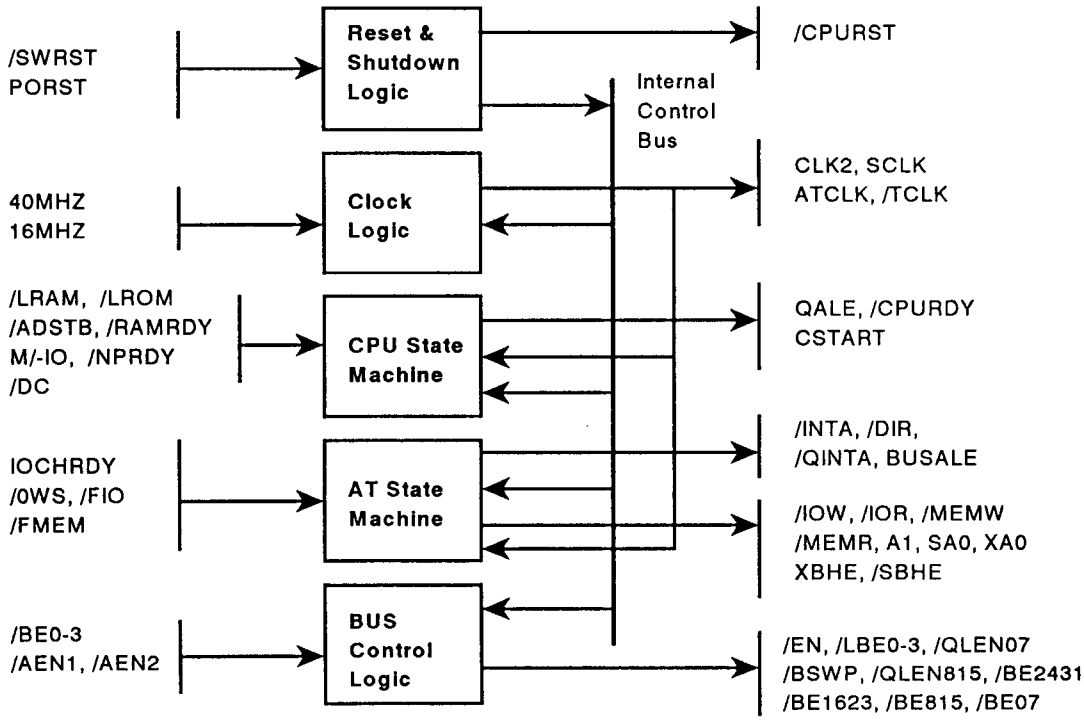
The ACC 2500 is an integrated high performance CMOS System Controller for an 80386 based computer. The ACC 2500 provides the state machines that control all bus accesses and produces the control signals to interface with the 80386. The ACC 2500 has clock switching capability to run the processor at full speed or at an optional speed to accommodate application software. AT* bus state machines control AT bus command timing for 100% compatibility with an IBM* PC/AT. With the ACC 2300 and the ACC 2000, the complete 386 chip set offers a 100% PC/AT compatible integrated solution, and allows designers to build a powerful 20/25 MHz 386 work station.

Features

- Independent 8 MHz AT Bus Clock
- 20/25 MHz or 8 MHz processor clock selection
- CPU interface and BUS control
- AT Bus timing emulation
- Reset and shut down logic
- 100-pin PFP package

* Trademarks of International Business Machines

Block Diagram



ACC Microelectronics Corporation · 3295 Scott Blvd. · Santa Clara, CA 95054
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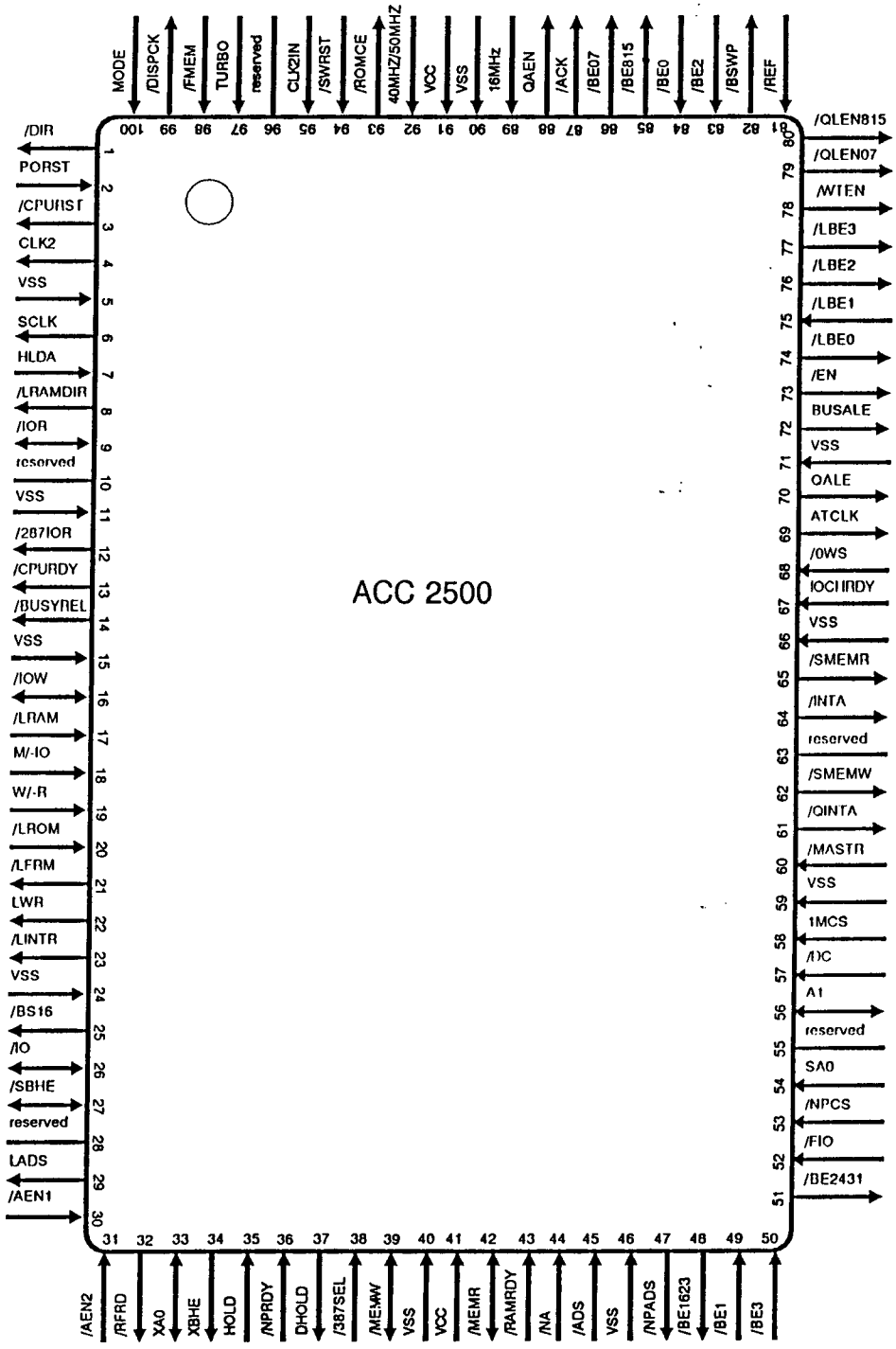
Pin Diagram


ACC 2500
MODE
/DISPCK
/FMEM
TURBO
reserved
CLK2IN
/SWRST
/ROMCE
40MHZ/50MHZ
VCC
VSS
16MHz
QAEN
/ACK
/BE07
/BE815
/BE0
/BE2
/BSWP
/REF
/DIR
PORST
/CPURST
CLK2
VSS
SCLK
HLDA
/LRAMDIR
/IOR
reserved
VSS
/287IOR
/CPURDY
/BUSYREL
VSS
/IOW
/LRAM
M/-IO
W/-R
/LROM
/LFRM
LWR
/LINTR
VSS
/BS16
/IO
/SBHE
reserved
LADS
/AEN1
/QLEN815
/QLEN07
/WTEN
/LBE3
/LBE2
/LBE1
/LBE0
/EN
BUSALE
VSS
OALE
ATCLK
/0WS
IOCHRDY
VSS
/SMEMR
/INTA
reserved
/SMEMW
/QINTA
/MASTR
VSS
1MCS
/IOC
A1
reserved
SA0
/NPCS
/FIO
/BE2431
/AEN2
/RFRD
XA0
XBHE
HOLD
/NPRDY
DHOLD
/387SEL
/MEMW
VSS
VCC
/MEMR
/RAMRDY
/NA
/ADS
VSS
/NPADS
/BE1623
/BE1
/BE3

Pin Descriptions

Pin	Symbol	I/O	Pin Description
/DIR	1	O	System data bus direction control
PORST	2	I	Power on reset
/CPURST	3	O	80386 reset
CLK2	4	O	Clock to 80386 & 80387
SCLK	6	O	Reference clock to CLK2
HLDA	7	I	Hold acknowledge from 80386
/LRAMDIR	8	O	Local data bus direction control
/IOR	9	I/O	AT bus IO read
/287IOR	12	O	287 IO read control
/CPURDY	13	O	Ready signal to 80386
/BUSYREL	14	O	Coprocessor busy clear signal
/IOW	16	I/O	AT bus IO write
/LRAM	17	I	Local RAM cycle
M/-IO	18	I	MIO from 80386
W/-R	19	I	WR from 80386
/LROM	20	I	Local ROM cycle
/LFRM	21	O	Latched local RAM select
LWR	22	O	Latched write control signal
/LINTR	23	O	Latched interrupt request signal
/BS16	25	O	BS16 to 80386
/IO	26	I/O	IO cycle
/SBHE	27	I/O	System bus high byte enable
LADS	29	O	Latched ADS signal

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/AEN1	30	I	DMA transfer 8-bit enable
/AEN2	31	I	DMA transfer 16-bit enable
/RFRD	32	O	Refresh read command
XA0	33	I/O	X address bus bit 0
XBHE	34	O	X address bus high byte enable
HOLD	35	I	Hold request signal
/NPRDY	36	I	Coprocessor ready
DHOLD	37	O	80386 hold request signal
/387SEL	38	I	Coprocessor 80387 select
/MEMW	39	I/O	AT bus memory write
/MEMR	42	I/O	AT bus memory read
/RAMRDY	43	I	RAM ready
/NA	44	I	Next address request
/ADS	45	I	ADS signal from 80386
/NPADS	47	O	80387 ADS control signal
/BE1623	48	O	System byte 2 enable
/BE1	49	I	Byte enable 1 from 80386
/BE3	50	I	Byte enable 3 from 80386
/BE2431	51	O	System byte 3 enable
/FIO	52	I	16-bit IO cycle
/NPCS	53	I	Accessing a coprocessor cycle
SA0	54	I/O	System address bus bit 0
A1	56	I/O	Address bus bit 1
/DC	57	I	DC from 80386

Pin Descriptions

Symbol	Pin	I/O	Pin Description
1MCS	58	I	Address range lower than 1MB
/MASTR	60	I	AT bus master input
/QINTA	61	O	Turns on buffer during interrupt acknowledge cycle
/SMEMW	62	O	System bus memory write
/INTA	64	O	Interrupt acknowledge cycle.
/SMEMR	65	O	System bus memory read
IOCHRDY	67	I	IO channel ready from AT bus
/0WS	68	I	Zero wait state control signal from AT bus
ATCLK	69	O	AT system clock
QALE	70	O	System address latch enable
BUSALE	72	O	AT address bus latch enable
/EN	73	O	Local data buffer enable
/LBE0 /LBE1 /LBE2 /LBE3	74 75 76 77	O	Latched byte enable
/WTEN	78	O	RAM Write enable
/QLEN07	79	O	System byte 0 latch enable
/QLEN815	80	O	System byte 1 latch enable
/REF	81	I	Refresh cycle
/BSWP	82	O	System low/high byte swap enable
/BE0 /BE2	84 83	I I	Byte enable from 80386 Byte enable from 80386
/BE815	85	O	System byte 1 enable
/BE07	86	O	System byte 0 enable

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/ACK	87	O	AEN1 or AEN2 has been asserted
QAEN	88	O	X address buffer direction control
16MHZ	89	I	16 MHz clock input
40MHZ/50MHZ	92	I	40/50 MHz clock input
/ROMCE	93	O	BIOS ROM output enable
/SWRST	94	I	Software reset from 8742
CLK2IN	95	I	CPU clock input
TURBO	97	I	Turbo speed control
/FMEM	98	I	AT bus 16-bit memory access cycle
/DISPCK	99	O	Parity disable
MODE	100	I	Page or Two-way interleaved mode select
VCC	41, 91		+5 volts
VSS	5, 11, 15, 24, 40, 46, 59, 66, 71, 90		Ground
Reserved	10, 28, 55, 63, 96		

Functional Description

The ACC 2500 implements three internal state machines to interface with the 80386 and provides control signals for all bus accesses.

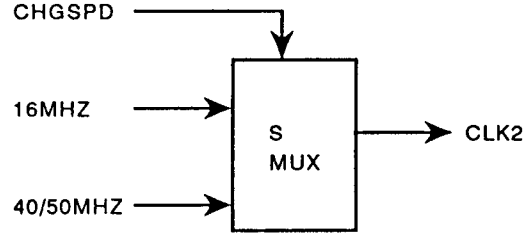
Two independent clock oscillators provide processor clock selection. A 20/25 MHz frequency runs the processor at full speed and a 8 MHz frequency is for application software that is timing dependent. AT bus command timing, controlled by a state machine, synchronizes with an 8 MHz clock which is independent of the processor clock. 32-bit local RAM access is through the ACC 2300. I/O accesses can support both 8-bit and 16-bit devices.

The ACC 2500 has the following functional blocks:

- Reset and shutdown logic
- Clock switching logic
- CPU state machine
- AT bus state machine
- Bus control logic

Reset and Shutdown Logic

The power on reset generated from the power supply resets both the system and the 80386. A software reset can be generated either by programming the 8042 keyboard controller or when a shutdown condition occurs. The software reset influences only the 80386, the system remains unchanged.



Clock Switching Logic

The clock switching logic selects between 40/50 or 16 MHz for the processor clock. The TURBO signal controls the clock selection. The processor clock is 40/50 MHz when TURBO is high and 16 MHz when TURBO is low. The AT bus clock is 8 MHz asynchronous to the processor clock. The system clock (SCLK) is inverted and half the processor clock and is used as a reference clock to generate CPU control signals.

Clock switching is performed dynamically through the keyboard. ACC 2500 logic guarantees a clean switch between high and low frequencies without a glitch or timing violation.

CPU State Machine

The CPU state machine controls access to devices on the local bus. The CPU state machine starts at each new cycle. A cycle start signal is also generated to mark the start of the cycle. The CPU state machine generates a ready signal back to the CPU when a cycle is completed. Interface to the 80386 begins when an /ADS is detected and terminates when a synchronized /READY signal is received. If the current cycle is not a local ROM or RAM cycle, control passes to the AT bus cycle and the ALE is generated to mark the start of an AT bus cycle.

AT Bus State Machine

The AT state machine controls the AT bus cycle and generates all bus commands. The AT state machine gains control of the buses when the current cycle is not a local cycle. The AT bus clock is 8 MHz and the state machine performs the synchronization of control and

status signals between the AT bus and the processor. The state machine controls the duration and associated wait states of AT bus commands. Both 8-bit and 16-bit I/O devices are supported on the I/O channel.

An AT bus cycle is initiated by asserting ALE and terminated by asserting /CPURDY. /MEMCS16 and /IOCS16 are sampled to determine if the bus is 8 or 16 bits when the I/O command becomes active. The AT bus state machine provides sequencing and timing controls for status and command of various bus cycles. The command cycle is terminated by an active /0WS or IOCHRDY signal.

Bus Control Logic

The bus control logic generates all buffer control signals for the local bus, system bus, and the peripheral bus. The bus control logic also controls data conversion and data swapping when a 16-bit bus cycle tries to access an 8-bit peripheral.

The ACC 2500 responds to /IOCS16 and /MEMCS16 when determining the amount of data required by the I/O channel. If none of these signals are asserted, 8-bit transfers are assumed and 16-bit access converts to two 8-bit bus accesses.

The AT bus commands, /IOW, /IOR, /MEMR, and /MEMW, have one wait state if the transfer is a 16-bit transfer and four wait states if the transfer is an 8-bit transfer. AT bus command wait states are based on an 8 MHz clock.

Rating Specifications

Absolute Maximum Ratings *

Parameter	Symbol	Condition	Min	Max	Unit
Power supply voltage	VCC	Ta=25 C	-0.3	7.0	V
Input voltage	VI	VSS=0	-0.3	VCC+0.3	V
Output voltage	VO		-0.3	VCC+0.3	V
Operating temperature	Top		-25	85	C
Storage temp	Tstg		-40	125	C

* Exposing the device to stress above these limits can cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specificaiton. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	VCC		4.75	5.25	V
Ambient temperature	TA		0	70	C

DC Specifications

TA = 0°C to 70°C, VCC = +5V +/- 5%

Group 1 INPUT

16MHz, 40MHZ/50MHZ, CLK2IN, PORST, HLDA, /LRAM, /LROM, /AEN1, /AEN2, HOLD, /NPURDY, /387SEL, /NA, /FIO, /NPCS, 1MCS, /MASTR, IOCHRDY, /0WS, /SWRST, TURBO, /FMEM, MODE, /RAMRDY, /REF

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V +/- 0.25 V
Input High voltage	VIH	2.0	VCC	V	VCC = 5 V +/- 0.25 V
Input low current	IIL	-10	10	uA	VIN = 0.0 V
Input high current	IIH	-10	10	uA	VIN =VCC

GROUP 2 INPUT WITH PULLUP

M/-IO, W/-R, /ADS, /BE0, /BE1, /BE2, /BE3, /DC

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V +/- 0.25 V
Input High voltage	VIH	2.0	VCC	V	VCC = 5 V +/- 0.25 V
Input low current	IIL	-200	-10	uA	VIN = 0.0 V
Input high current	IIH	10	200	uA	VIN = VCC

Group 3 OUTPUT

/DIR, /CPURST, /LRAMDIR, /287IOR, /CPURDY, /BUSYREL, LWR, /LFRM, /BS16, /QINTA, /INTA, QALE, /EN, /LINTR, DHOLD, /NPADS, /BE1623, /BE2431, BUSALE, /QLEN07, /QLEN815, /BE815, /BE07, /ROMCE, /DISPCK, /LBE0-3, /RAMWEN, /BSWP, /ACK, QAEN,

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 4.0 mA
Output high voltage	VOL	2.4		V	IOH = -4.0 mA

CLK2, SCLK, LADS, ATCLK

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 8.0 mA
Output high voltage	VOL	2.4		V	IOH = -8.0 mA

Group 4 TRISTATE OUTPUT

/RFRD, /XBHE

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 4.0 mA
Output high voltage	VOL	2.4		V	IOH = -4.0 mA
Tristate leakage current	IOZ	-10.0	10.0	uA	OV < VOUT < VCC

/SMEMW, /SMEMR

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 12.0 mA
Output High voltage	VOL	2.4		V	IOH = -12.0 mA
Tristate leakage current	IOZ	-10.0	10.0	uA	OV < VOUT < VCC

Group 5 INPUT/OUTPUT WITH PULLUP

/IO, XA0

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V =/- 0.25 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 V =/- 0.25 V
Output low voltage	VOL		0.4	V	IOL = 4.0 mA
Output high voltage	VOH	2.4		V	IOH = -4.0 mA
Tristate leakage current	IOZ	-200	-10	uA	0V < VOUT < VCC

A1

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V =/- 0.25 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 V =/- 0.25 V
/Output low voltage	VOL		0.4	V	IOL = 8.0 mA
Output high voltage	VOH	2.4		V	IOH = -8.0 mA
Tristate leakage current	IOZ	-200	-10	uA	0V < VOUT < VCC

/IOR, /IOW, /SBHE, /MEMW, /MEMR, SA0

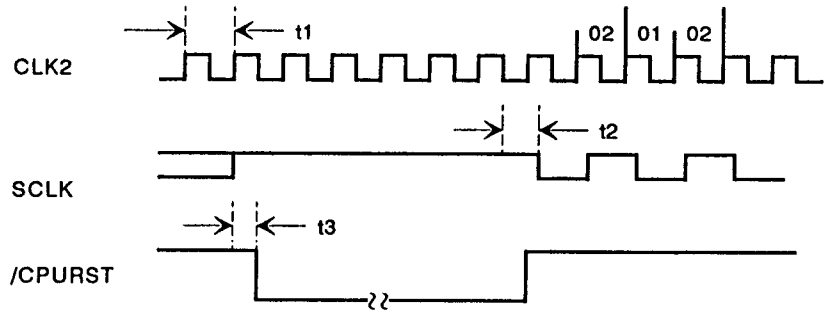
Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V +/- 0.25 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 V +/- 0.25 V
/Output low voltage	VOL		0.4	V	IOL = 12.0 mA
Output high voltage	VOH	2.4		V	IOH = -12.0 mA
Tristate leakage current	IOZ	-200	-10	uA	0V < VOUT < VCC

AC Specifications

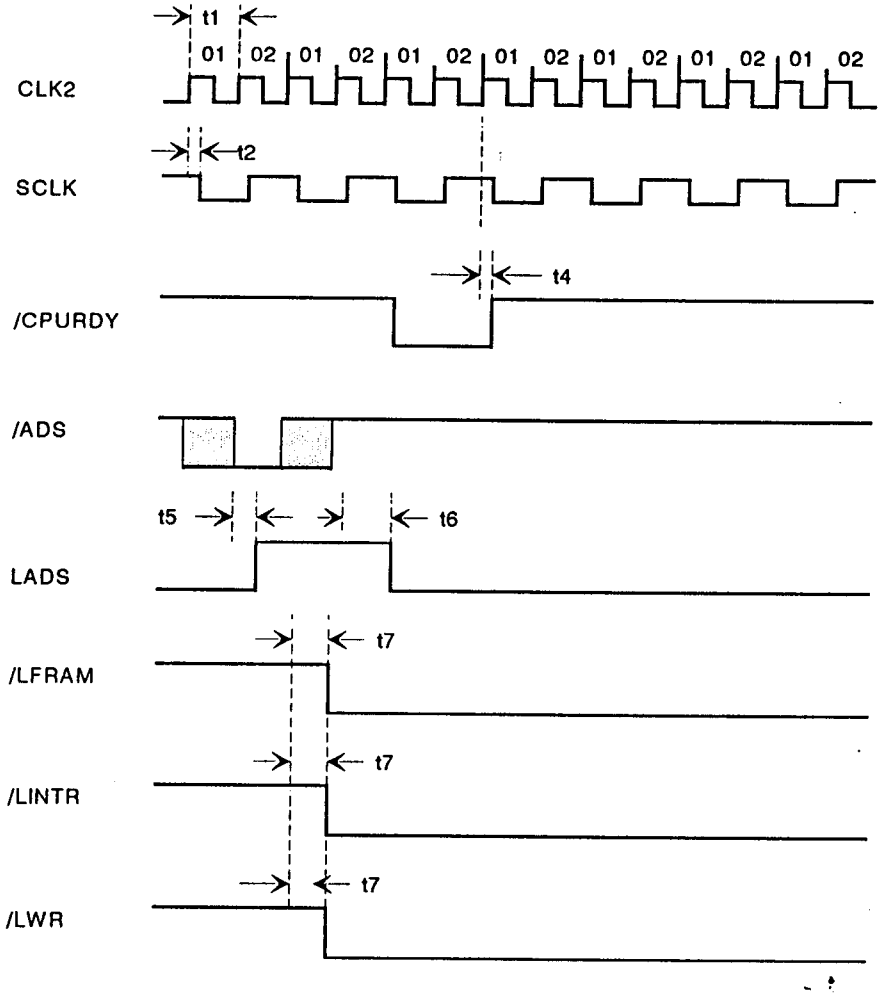
50 pf load output

Symbol	Description	Min	Typ	Max	Units
t1	CLK2 period	25			ns
t2	SCLK delay from CLK2		5		ns
t3	/CPURST delay from CLK2		3.5		ns
t4	/CPURDY active delay from CLK2		6		ns
t5	Latched /ADS active delay form /ADS		5.5		ns
t6	Latched /ADS inactive delay from CLK2		5.5		ns
t7	Latched /LRAM, /LINTR, and /LWR active delay form CLK2		9.5		ns
t8	/INTA active delay from ATCLK		7.5		ns
t9	QALE inactive delay from ATCLK		10		ns
t10	BUSALE active delay from ATCLK		10		ns
t11	DHOLD active delay from CLK2		7.5		ns
t12	/LBE0-/LBE3 active delay from CLK2		16		ns
t13	Buffer enable /EN active delay from CLK2		14		ns
t14	ATCLK active delay from 16MHz		6.5		ns
t15	/MEMR and /MEMW active delay from 8MHz		18		ns
t16	/MEMR and /MEMW, /IOR, and /IOW inactive delay from 16MHz		15		ns
t17	/IOR and /IOW active delay from 16MHz		20.5		ns

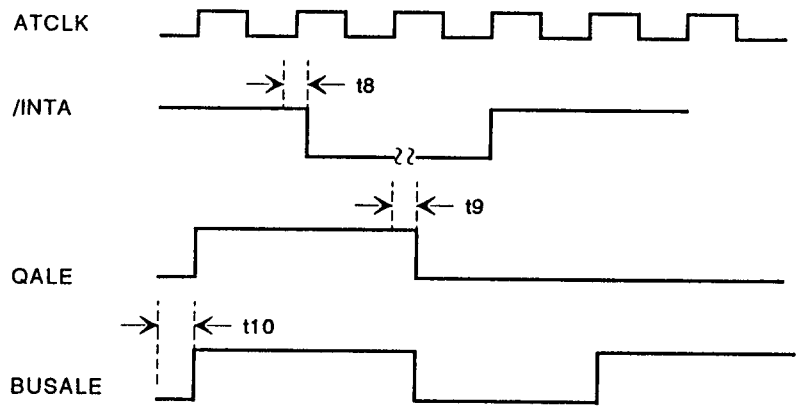
Initial Reset



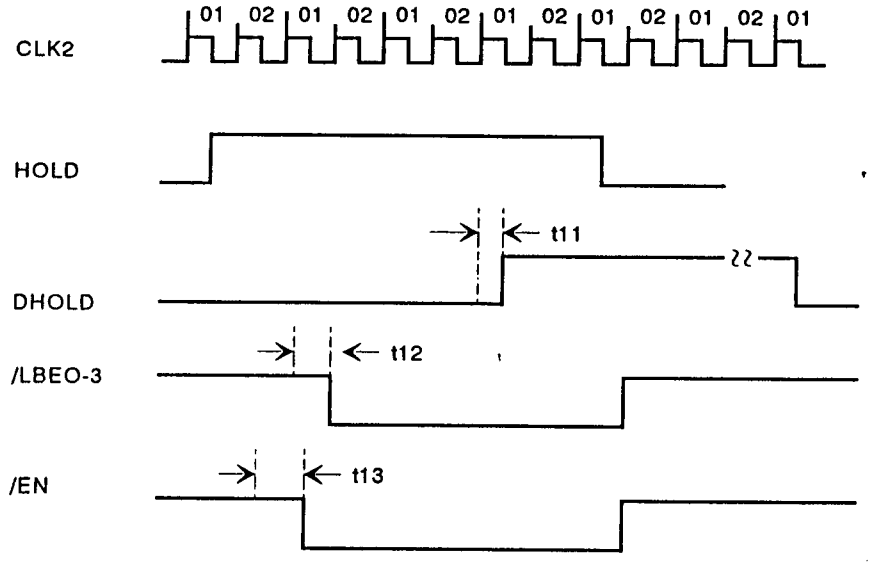
Local RAM Cycle



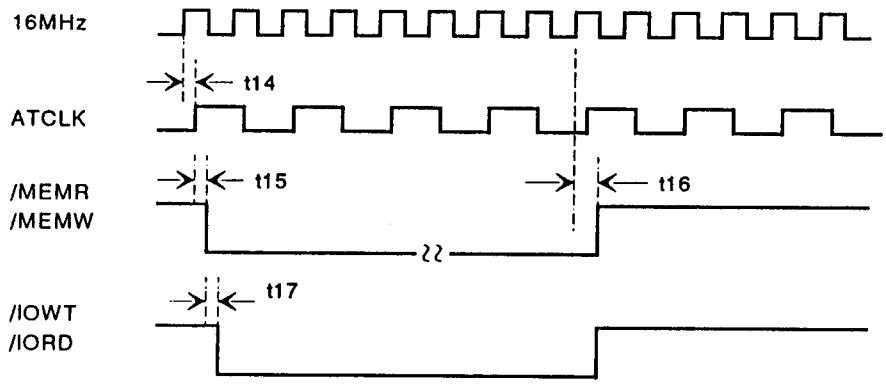
AT BUS Timing



Hold Cycle for DMA



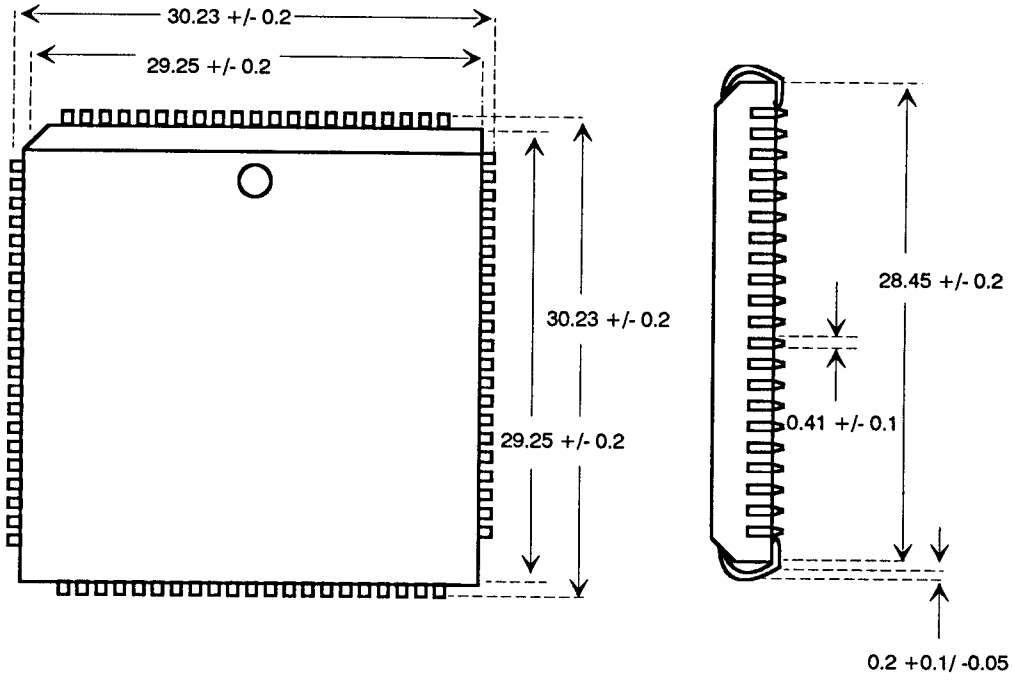
AT BUS Timing

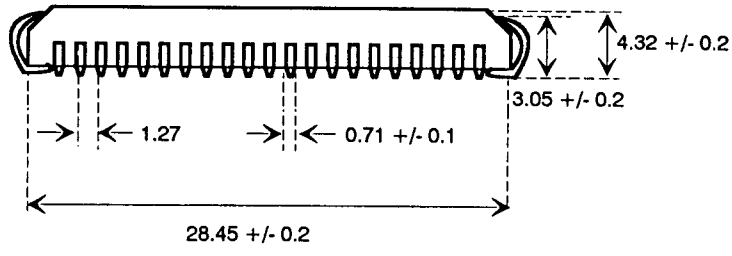


Production Package Specification

Package: 84-pin PLCC
Unit: mm

Chip: ACC 2000

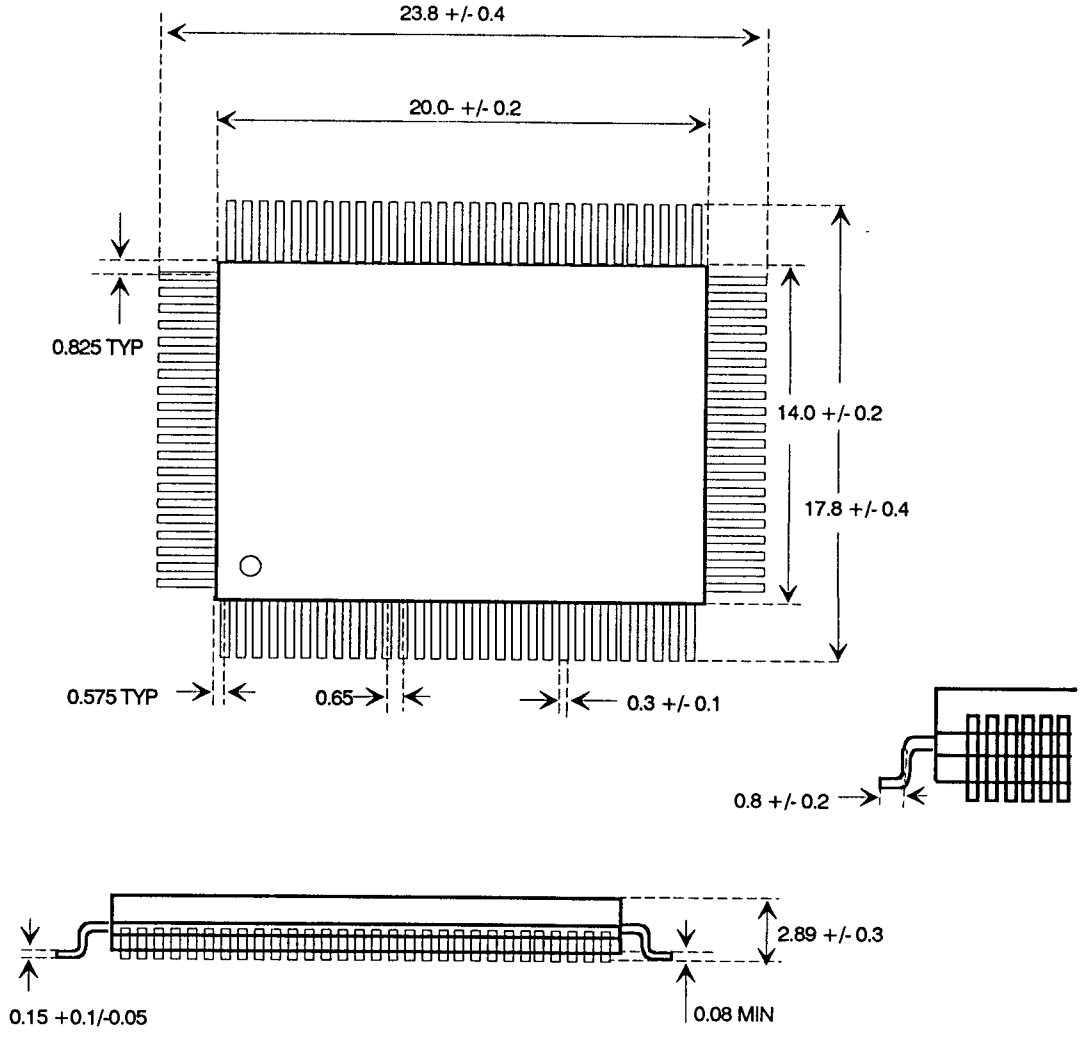




Production Package Specification

Package: 100-pin PFP
Unit: mm

Chip: ACC 2300
ACC 2500



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