T-52-01

82021
Turbo PC/AT Chip Set

- 100% hardware and software compatible with the IBM PC/AT
- Fully compatible with

  Intel 8237 DMA controller
  Intel 8259 interrupt controller
  Intel 8254 timer/counter
  Intel 82284 clock generator
  Intel 82288 bus controller
  TI 74LS612 memory mapper

- Functions include

  7 DMA channels
  3 timer/counter channels
  14 external interrupt channels
  Data buffers
  Address buffers

- Supports Intel 286 and 386SX microprocessors
- Supports Intel 287 and 387SX coprocessors
- Supports chip select for floppy, hard disk, serial/parallel ports
- Optional Direct Memory Access mode
- Supports 64K x 1, 256K x 1, 256K x 4, 1M x 1, 1M x 4, 4M x 1 memory and 16MB on motherboard
- Supports remapping of 640K through 1M memory to above the resident RAM address space
- 4-Way or 2-way page interleaved memory controller
- Supports EMS 4.0
- Built-in staggered memory refresh control
- Supports up to 25 MHz system clock
- I/O (8 MHz) AT BUS compatible
- Quick hardware and software switch from protected mode to real mode for OS/2 optimization
- Shadow RAM for system BIOS and video BIOS

The Turbo PC/AT chip set includes the following three chips:

2000	PC/AT Integrated Bus and Peripheral Controller
2121	System and Memory Controller
2220	Data Buffers or Address Buffers

General Description

The 82021 is an integrated high performance CMOS chip set that replaces most of the MSI/SSI logic used in building an IBM PC/AT compatible system.

The first chip, the 2000, is a peripheral controller that performs the functions of two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, and one

74LS612 memory mapper as well as other standard control logic circuitry.

The second chip, the 2121, is a system controller containing one 82284 clock generator, one 82288 bus controller, and a high performance memory controller providing up to 25 MHz operation as well as the standard AT mode with page interleaved or direct access schemes. To support a 16 MHz page interleaved operation with a 0.7 wait state, 100 ns memory can be used.

The 2220 is a data and address buffer/latch chip that runs in two modes. This chip is used twice, one chip is the data buffer, the other is the address buffer/latch.

The 82021 chip set supports a system clock design up to 25 MHz while maintaining 8 MHz AT bus compatibility. All chips in the 82021 chip set are implemented using advanced CMOS technology. The chip set's high integration reduces total system cost through lower power requirements, increased reliability, and reduced board size.

ACC Micro 82021 System Block Diagram

(where 80386SX and 80387SX can be replaced by 80286 and 80287 respectively)