ACC 82020
Turbo PC/AT Chip Set

- 100% hardware and software compatible with the IBM* PC/AT*
- Fully compatible with

  Intel 8237 DMA controller
  Intel 8259 interrupt controller
  Intel 8254 timer/counter
  Intel 82284 clock generator
  Intel 82288 bus controller
  TI 74LS612 memory mapper

- Functions include

  7 DMA channels
  3 timer/counter channels
  14 external interrupt channels
  Data buffers
  Address buffers

- Supports Intel 286 and 386SX microprocessors
- Supports Intel 287 and 387SX coprocessors
- Supports chip select for mouse, hard disk, serial/parallel ports
- Optional Direct Memory Access mode**
- Supports 64K x 1, 256K x 1, 256K x 4, 1M x 1, 1M x 4, 4M x 1 memory and 16MB on motherboard
- Supports single module of 1M x 9 DRAM**
- Supports remapping of 640K through 1M memory range
- 4-Way or 2-way page interleaved memory controller
- Supports EMS 4.0
- Built-in staggered memory refresh control
- Supports up to 25 MHz system clock
- I/O (8 MHz) AT BUS compatible
- Quick hardware and software switch from protected mode to real mode for OS/2 optimization
- Shadow RAM for BIOS

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** Will be Available fourth quarter 1989

The Turbo PC/AT chip set includes the following three chips:

ACC 2000	Multifunctional Peripheral Controller
ACC 2120	System Bus Controller and Memory Controller
ACC 2220	Data Buffers or Address Buffers

General Description

The ACC 82020 is an integrated high performance CMOS chip set that replaces most of the MSI/SSI logic used in building an IBM PC/AT compatible system.

The first chip, the ACC 2000, is a peripheral controller that performs the functions of two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, and one

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74LS612 memory mapper as well as other standard control logic circuitry.

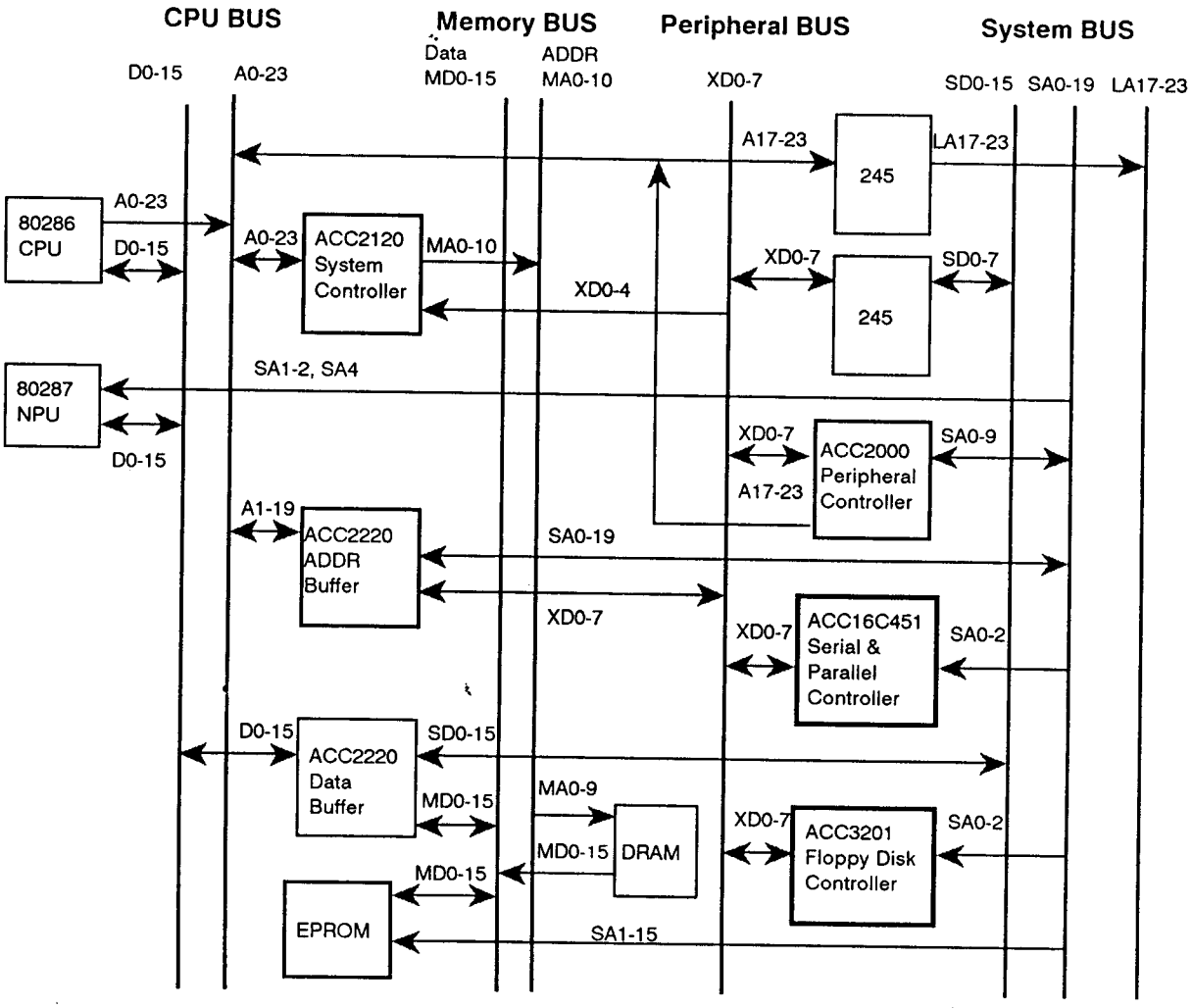
The second chip, the ACC 2120, is a system controller containing one 82284 clock generator, one 82288 bus controller, and a high performance memory controller providing up to 25 MHz operation as well as the standard AT mode with zero and one wait state schemes. To support a 16 MHz page interleaved operation with a 0.7 wait state, 100 ns memory can be used.

The ACC 2220 is a data and address buffer/ latch chip that runs in two modes. This chip is used twice, one chip is the data buffer, the other is the address buffer/latch.

The ACC 82020 chip set supports a system clock design up to 25 MHz while maintaining 8 MHz AT bus compatibility. All chips in the ACC 82020 chip set are implemented using advanced CMOS technology. The chip set's high integration reduces total system cost through lower power requirements, increased reliability, and reduced board size.

ACC 82020 System Block Diagram

(where 80286 and 80287 can be replaced by 80386SX and 80387SX respectively)



ACC 2000
PC/AT Integrated Bus & Peripheral Controller

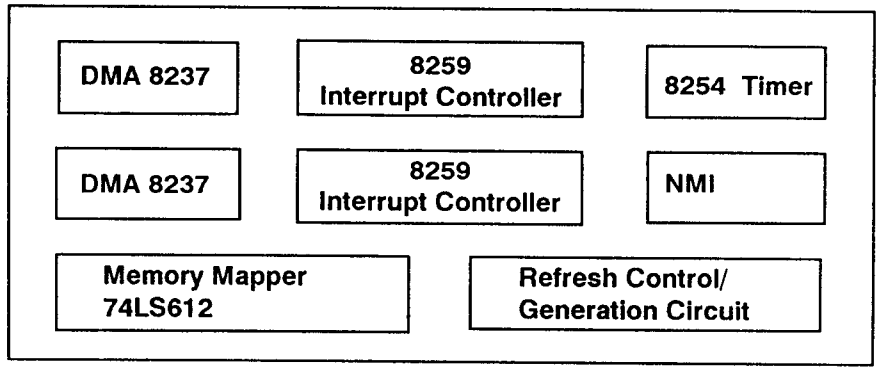
The ACC 2000 is an integrated high performance CMOS PC/AT* peripheral controller that incorporates several TTL, SSI, and MSI including two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, and one 74LS612 memory mapper. The ACC 2000 is a high performance VLSI that offers a single chip solution for all the peripherals attached to the X BUS (peripheral bus) in IBM PC/AT compatible systems.

Features

- 100% hardware and software compatible with the IBM* PC/AT
- Fully compatible to Intel's

  8237 DMA controller
  8254 Timer/Counter
  8259 Interrupt controller
- Fully compatible to TI's 74LS612 memory mapper
- Supports 7 DMA channels, 3 timer/counter channels and 14 interrupt request channels
- 100% compatible with the IBM AT I/O BUS
- Supports up to 8 MHz DMA clock
- Supports 16 MB DMA address space
- Built-in refresh control circuit
- 1.5 micron high performance CMOS technology
- TTL compatible
- 84-L PLCC package

Block Diagram



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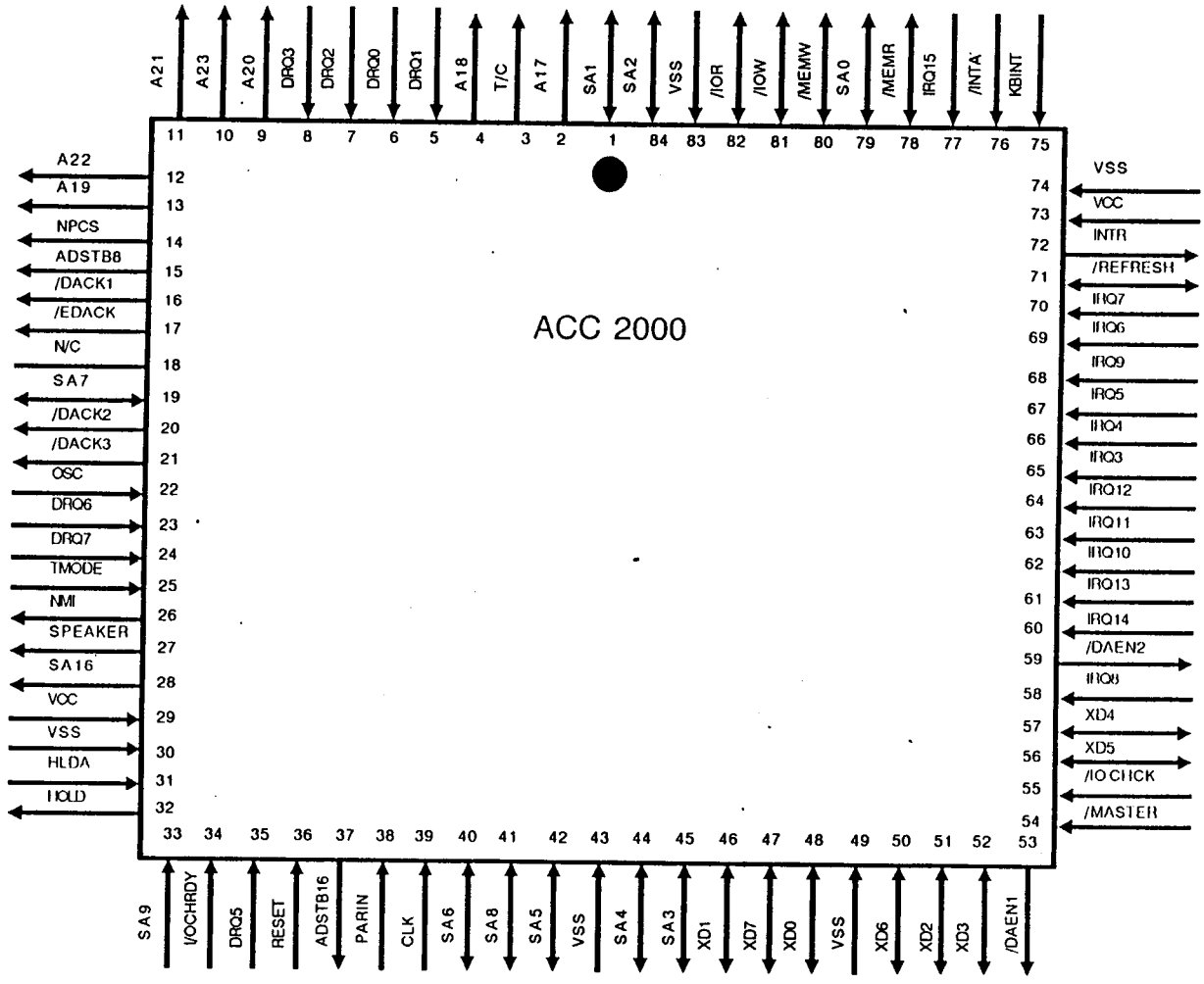
Pin Diagram


ACC 2000
1 A21
2 A23
3 A20
4 DRQ3
5 DRQ2
6 DRQ0
7 DRQ1
8 A18
9 T/C
10 A17
11 SA1
12 SA2
13 VSS
14 /IOR
15 /IOW
16 /MEMW
17 SA0
18 /MEMR
19 IRQ15
20 /INTA
21 KBINT
22 VSS
23 VCC
24 INTR
25 /REFRESH
26 IRQ7
27 IRQ6
28 IRQ9
29 IRQ5
30 IRQ4
31 IRQ3
32 IRQ12
33 IRQ11
34 IRQ10
35 IRQ13
36 IRQ14
37 /DAEN2
38 IRQ8
39 XD4
40 XD5
41 /IOCHCK
42 /MASTER
43 /DAEN1
44 XD3
45 XD2
46 XD6
47 VSS
48 XD0
49 XD7
50 XD1
51 SA3
52 SA4
53 VSS
54 SA5
55 SA8
56 SA6
57 CLK
58 PARIN
59 ADSTB16
60 RESET
61 DRQ5
62 I/OCHRDY
63 SA9
64 HOLD
65 HLDA
66 VSS
67 VCC
68 SA16
69 SPEAKER
70 NMI
71 TMODE
72 DRQ7
73 DRQ6
74 OSC
75 /DACK3
76 /DACK2
77 SA7
78 N/C
79 /EDACK
80 /DACK1
81 ADSTB8
82 NPCS
83 A19
84 A22

Pin Descriptions

Symbol	Pin	Type	Description
SA0	79	I/O	System address bus bit.
SA1	1		
SA2	84		
SA3	45		
SA4	44		
SA5	42		
SA6	40		
SA7	19		
SA8	41		
SA9	33	I	System address bus bit.
SA16	28	O	System address bus Bit 16.
A17	2	O	Address bus bit.
A18	4		
A19	13		
A20	9		
A21	11		
A22	12		
A23	10		
T/C	3	O	Terminal count pulsing. When the terminal count for DMA channel is reached.
DRQ0	6	I	DMA Request Line. Active high.
DRQ1	5		
DRQ2	7		
DRQ3	8		
DRQ5	35		
DRQ6	23		
DRQ7	24		
NPCS	14	O	Chip select for numeric processor 80287.
ADSTB8	15	O	Address strobe for 8 bit DMA transfers.
/DACK1	16	O	Encoded DMA acknowledge bit.
/DACK2	20		
/DACK3	21		
/EDACK	17	O	Enable DMA acknowledge decoder. Active low .
N.C.	18	O	Do not connect.

Pin Descriptions

Symbol	Pin	Type	Description
OSC	22	I	14.31818 MHz clock input.
TMODE	25	I	Test pin.
NMI	26	O	Non-maskable interrupt to 80286 CPU. Active high; NMI generated by the math processor, memory parity error, or error from bus /IOCHCK.
SPEAKER	27	O	Data to speaker.
HLDA	31	I	Hold acknowledge from CPU.
HOLD	32	O	Hold request to CPU. Active high.
IOCHRDY	34	I	I/O channel ready from expansion bus.
RESET	36	I	System reset.
ADSTB16	37	O	Address strobe for 16 bit DMA transfers.
/PAR	38	I	Parity error output from Data buffer. Active low.
SYSCLK	39	I	System clock.
XD0 XD1 XD2 XD3 XD4 XD5 XD6 XD7	48 46 51 52 57 56 50 47	I/O	Peripheral data bus Bit 0.
/DAEN1	53	O	DMA address enable for 8 bit data transfer. Active low.
/MASTER	54	I	CPU I/O control for address, data, and control lines.
/IOCHCK	55	I	Error expansion bus. Active low.
/DAEN2	59	O	DMA address enable for 16 bit data transfer. Active low.

Pin Descriptions

Symbol	Pin	Type	Description
IRQ3	65	I	Interrupt request input. Active high.
IRQ4	66	I	
IRQ5	67	I	
IRQ6	69	I	
IRQ7	70	I	
IRQ8	58	I	
IRQ9	68	I	
IRQ10	62	I	
IRQ11	63	I	
IRQ12	64	I	
IRQ13	61	I	
IRQ14	60	I	
IRQ15	77	I	
/REFRESH	71	I/O	Refresh cycle. Active low.
INTR	72	O	Interrupt to CPU. Active high.
KBINT	75	I	Keyboard interrupt to 8259.
/INTA	76	I	Interrupt acknowledge. Active low.
/MEMR	78	I/O	Memory read. Active low.
/MEMW	80	I/O	Memory write. Active low.
/IOW	81	I/O	I/O write. Active low.
/IOR	82	I/O	I/O read. Active low.
VCC	29, 73		+5 volt supply
VSS	30, 43, 49, 74, 83		Ground

Functional Description

Interrupt Controller

Two programmable interrupt controllers in the ACC 2000 function as a system wide interrupt manager for an IBM PC/AT system, compatible with the Intel 8259 interrupt controller. The interrupt controller efficiently determines when and which I/O device is serviced by the microcomputer.

The two cascaded interrupt controllers in the ACC 2000 provide a total of 15 possible interrupt sources. One of these interrupt request lines is used internally, providing a total of 14 possible external interrupt sources. The internal line connects to the 8254 Counter 0 output.

DMA

There are two 8237 equivalent DMA controllers cascaded together in the ACC 2000 chip. During a DMA cycle, one of the two external 8-bit latches hold the middle range address bits while the 74LS612 generates the upper range address bits. Once the hold request has been acknowledged, the DMA controller drives 24 address bits for a total addressing capability of 16 Megabytes. The middle address bits of the 24-bit address range are held in two sets of 8-bit registers, one register for each DMA controller. The DMA controller drives the value to be loaded onto the data bus, and then issues an address strobe signal to latch the data bus value into these registers.

The two 8237 compatible DMA controllers in the ACC 2000 provide a total of seven external DMA channels. Each channel has a 24-bit address output to access data throughout the entire 16 megabyte system address space. Channel 0 through channel 3 support 8-bit peripherals and an 8 or 16-bit memory. Each channel can transfer data in 64 Kbyte pages.

Channel 4 is used for cascading and is not available externally. Channel 5 through channel 7 support 16-bit I/O adapters to transfer data between 16-bit I/O adapters and 16-bit system memory. Each channel can transfer data in 128 Kbyte pages. The DMA function improves the computer system by allowing external devices to transfer information directly from and to the system memory.

Features include

- Address increment or decrement.
- Seven independent DMA channels with independent auto initialization for each channel.
- Each DMA request can be controlled individually to enable or disable.
- Software DMA request.

Timer/Counter

The Timer/Counter is the functional equivalent of an 8254 timer. It has three internal counters and clock inputs. The three clock inputs are tied to a clock of 1.19 MHz. The output of Counter 0 is connected to the IRQ input of interrupt controller one. Counter one output initiates a refresh cycle and Counter two output generates sound waveforms for speaker circuitry.

Features:

- Three independent 16-bit counters
- Count binary or BCD

Memory Mapper

The ACC 2000 has the equivalent of a 74LS612 to generate the upper address bits during a DMA cycle.

Source Memory Mapper	8237	
(for DMA Channels 0 - 3)		
Address	A23 <--> A16	A15 <--> A0
(for DMA Channels 5 - 7)		
Address	A23 <--> A17	A16 <--> A1

PIO

The PIO is the system configuration to control the timer channel speaker ports. It also has circuitry to detect refresh. This condition can be read back as Bit 4.

Refresh Generation Logic

Refresh circuitry contains an 8-bit counter for address SA0-7 during a refresh.

Refresh/DMA Abitration Logic

ACC 2000 contains circuitry to control a refresh cycle. A 74LS590 equivalent 8-bit counter outputs the refresh addresses onto the memory bus when the refresh signal is pulled low.

There are two possible sources for a hold request to the CPU. Either the DMA controller issues a hold request or the output of Counter 1 in the 8254 makes a low to high transition. The HOLD line is active when either source is requesting a hold. The hold request from the DMA controller is sampled on the rising edge of the DMA clock and the request from the timer is sampled on the falling edge of the DMA clock.

If the DMA controller's hold wins the arbitration, the HOLD is asserted, and it waits for a signal back from the CPU. When the DMA controller is finished, it negates its hold request signal to the arbiter. The arbitration then switches to a REFRESH cycle if there is a pending hold from the Counter/Timer, otherwise the arbiter inactivates the HOLD line and returns control to the CPU.

If a refresh cycle wins the arbitration, the HOLD is asserted and the ACC 2000 pulls the /REFRESH pin low. /REFRESH remains low for four SYSCLK rising edges. On the fourth rising edge of SYSCLK, the HOLD line is inactivated. However, if there is a pending hold request from the DMA controller on the fourth rising edge of SYSCLK, the REFRESH cycle is extended for one more SYSCLK cycle. The Hold request arbiter then acknowledges the hold request from the DMA controller.

NMI and Port B Logic

The ACC 2000 contains non-maskable interrupt (NMI) signal generation logic. An NMI can be caused by an I/O error or by a parity error. Port B indentifies the source of the error. At power up, the NMI signal is masked off. NMI is enabled by writing to I/O address 070 hex with Bit 7 low; NMI is disabled by writing to I/O addresss 070 hex with Bit 7 high.

Rating Specifications

Absolute Maximum Ratings*

TA = 25° C

Parameter	Symbol	Min	Max	Unit
Power supply voltage	V_{CC}	-0.5	7.0	V
Power dissipation (@5.25 V)	W_d		1	W
Current (@5.25 V)	I_{CC}		50	mA
Input voltage	V_I	-0.5	V_{CC}+0.5	V
Output voltage	V_O	-0.5	V_{CC}+0.5	V
Operating temperature	T_{op}	0	70	°C
Storage temperature	T_{stg}	-40	150	°C

* Exposing the device to stress above these limits can cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Capacitance Limits

TA = +25° C, VCC = 5 V

Parameter	Symbol	Min	Max	Unit	Test Condition
Input capacitance	C_I		10	pF	fc = 1 MHz unmeasured pins at GND
I/O capacitance	C_{IO}		15	pF	

DC Characteristics

TA = 0° C to +70° C, VCC = +5 V +/- 10%

DRQ0-3, DRQ5-7, TMODE, HLDA, SA9, IOCHRDY, RESET, /PAR, SYSCLK, /MASTER, /IOCHCK, IRQ3-15, KBINT, /INTA, OSC

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 +/- 0.5 V
Input low current	IIL		-10	uA	VIN > VSS
Input high current	IIH		-10	uA	VIN < VCC

XD0-7

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.2VCC - 0.1 V		VCC = 5 +/- 0.5 V
Input high voltage	VIH	0.2VCC + 0.9	VCC	V	VCC = 5 +/- 0.5 V
Input low current	IIL		-10	uA	VIN > 0.0V
Input high current	IIH		10	uA	VIN < VCC
Output low voltage	VOL		0.45	V	IOL = 3.2mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA
Tristate leakage current	IOZ	-10	10	uA	0 V < VOUT < VCC

SA0-6, SA8, /REFRESH, /MEMR, /MEMW, /IOW, /IOR

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5V +/- 0.5V
Input high voltage	VIH	2.0	VCC	V	VCC = 5V +/- 0.5V
Input low current	IIL		-10.0	uA	VIN > VSS
Input high current	IIH		10.0	uA	VIN < VCC
Output low voltage	VOL		0.45	V	IOL = 9.6mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA
Tristate leakage current	IOZ	-10.0	10.0	uA	0V < VOUT < VCC

NPCS, ADSTB8, /DACK1-3, /EDACK, CH/F, NMI, SPEAKER, HOLD, ADSTB16, /DAEN1-2, INTR

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 3.2mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA

T/C

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 9.6mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA

A17-23

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 3.2mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA
Tristate leakage current	IOZ	-10.0	10.0	uA	0V < VOUT < VCC

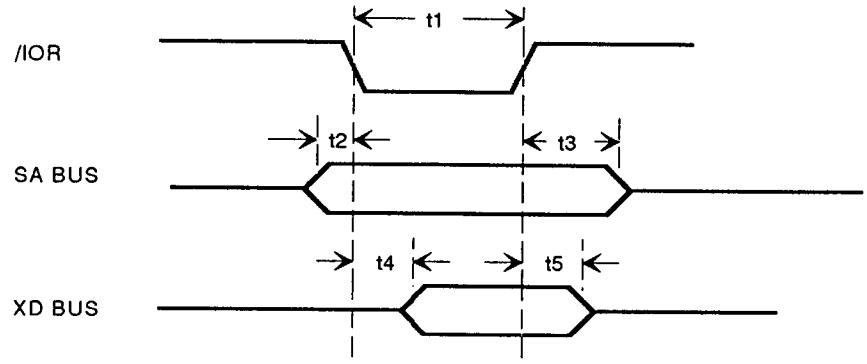
SA16

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 9.6mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA
Tristate leakage current	IOZ	-10.0	10.0	uA	0V < VOUT < VCC

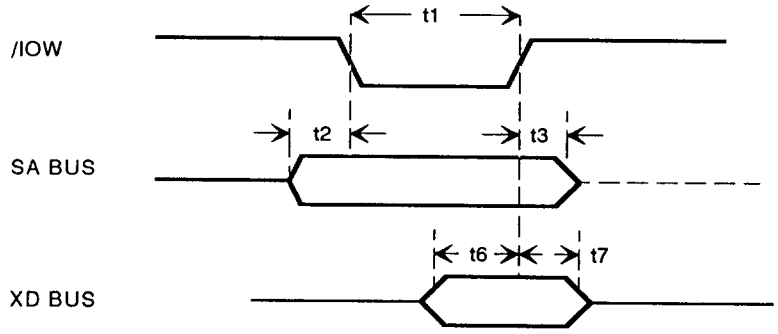
AC Specifications

Symbol	Parameter	Min	Max	Units
t1	/IOR or /IOW pulse width	110		ns
t2	SA address valid to /IOR /IOW low setup time	25		ns
t3	SA address hold time from /IOR /IOW high	13		ns
t4	XD data valid delay from /IOR low		110	ns
t5	XD data float delay from /IOR high	0	90	ns
t6	XD data valid to /IOW high setup time	70		ns
t7	XD data hold time from /IOW high	15		ns
t8	RESET high pulse width	250		ns
t9	RESET inactive to first /IOR or /IOW command	4		SYSCLK Cycle
t10	Command recovery time between successive /IOR or /IOW pulses	125		ns
t11	NPCS valid from address delay		51	ns
t12	NMI output delay		68	ns

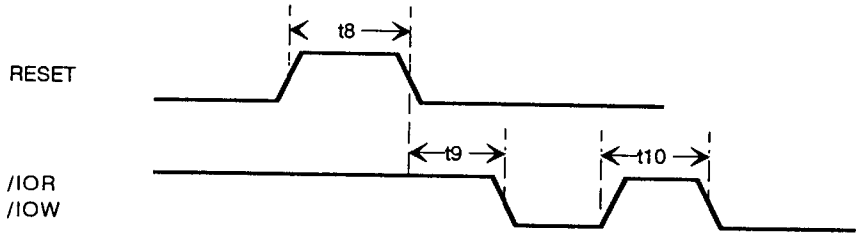
Peripheral Read Timing



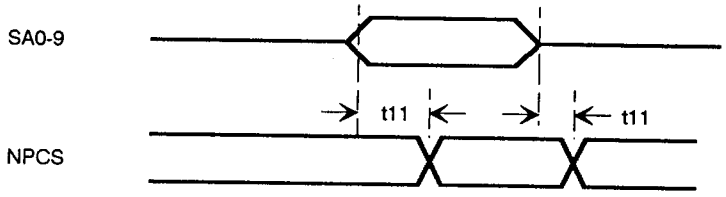
Peripheral Write Timing

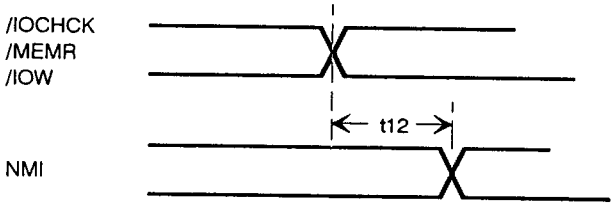


Command and Reset Timing



Other Timing Waveforms

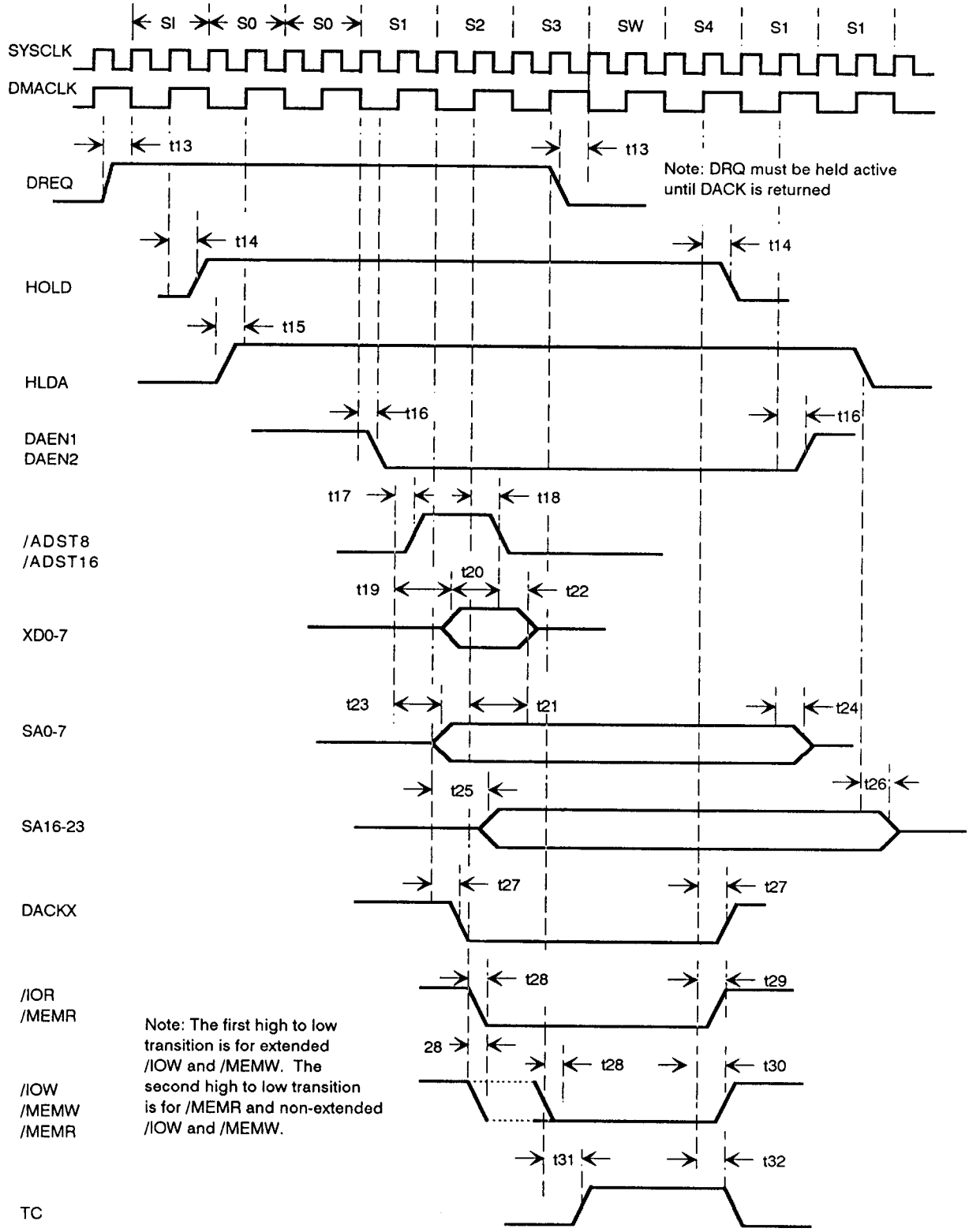




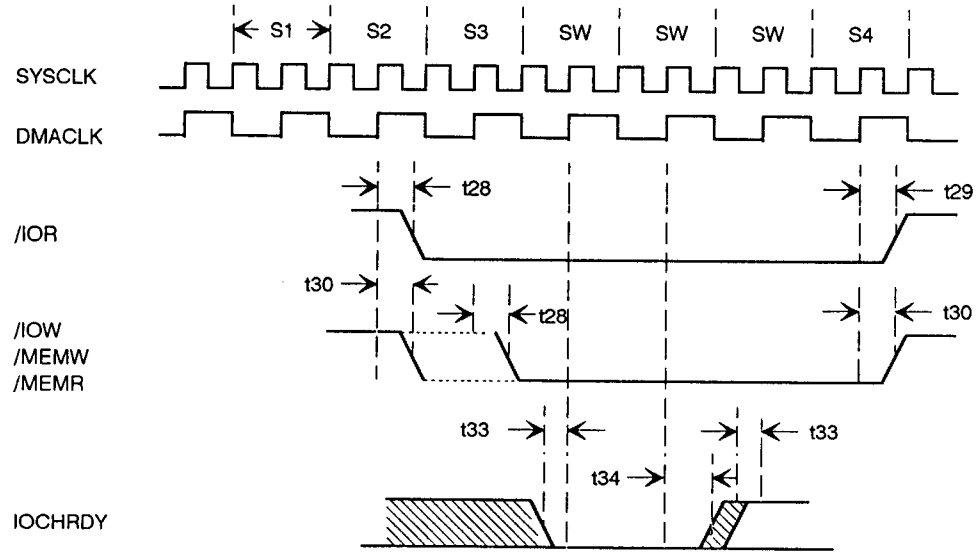
AC Specifications

Symbol	Parameter	Min	Max	Units
t13	DRQ to SYSCLK high setup time	0		ns
t14	HOLD valid from SYSCLK high delay time		50	ns
t15	HLDA to SYSCLK high setup time	25		ns
t16	/DAEN1 valid from SYSCLK high delay time		77	ns
t17	ADSTB8 or ADSTB16 high from SYSCLK high		72	ns
t18	ADSTB8 or ADSTB16 low from SYSCLK high delay time		76	ns
t19	Data float to active delay from SYSCLK high		93	ns
t20	Data to ADSTB8 or ADSTB16 low set up time	70		ns
t21	Data active to float delay from SYSCLK high		92	ns
t22	Data from ADSTB8 or ADSTB16 low HOLD time	8		ns
t23	low byte ADDR float to active from SYSCLK high		180	ns
t24	low byte ADDR active to float delay from SYSCLK high		70	ns
t25	high byte ADDR float to active delay from SYSCLK high		123	ns
t26	high byte add active to float from HLDA low		35	ns
t27	/DACK valid from SYSCK high delay time		83	ns
t28	/IOR, /IOW, /MEMR, /MEMW active from SYSCLK high delay time		53	ns
t29	/IOR and /MEMR inactive from SYSCLK high delay time		97	ns
t30	/IOW and /MEMW inactive from SYSCLK high delay time		80	ns
t31	T/C active from SYSCLK high delay time		82	ns
t32	T/C inactive from SYSCLK high delay time		82	ns
t33	IOCHRDY input setup time to SYSCLK high	26		ns
t34	IOCHRDY input hold time from SYSCLK high	15		ns

DMA Timing


SI
S0
S0
S1
S2
S3
SW
S4
S1
S1
SYSCLK
DMACLK
t13
t13
DREQ
Note: DRQ must be held active until DACK is returned
t14
t14
HOLD
t15
HLDA
t16
t16
DAEN1
DAEN2
t17
t18
/ADST8
/ADST16
t20
t19
t22
XD0-7
t23
t21
t24
SA0-7
t25
t26
SA16-23
t27
t27
DACKX
t28
t29
/IOR
/MEMR
28
t28
t30
/IOW
/MEMW
/MEMR
t31
t32
TC
Note: The first high to low transition is for extended /IOW and /MEMW. The second high to low transition is for /MEMR and non-extended /IOW and /MEMW.

IOCHRDY Timing

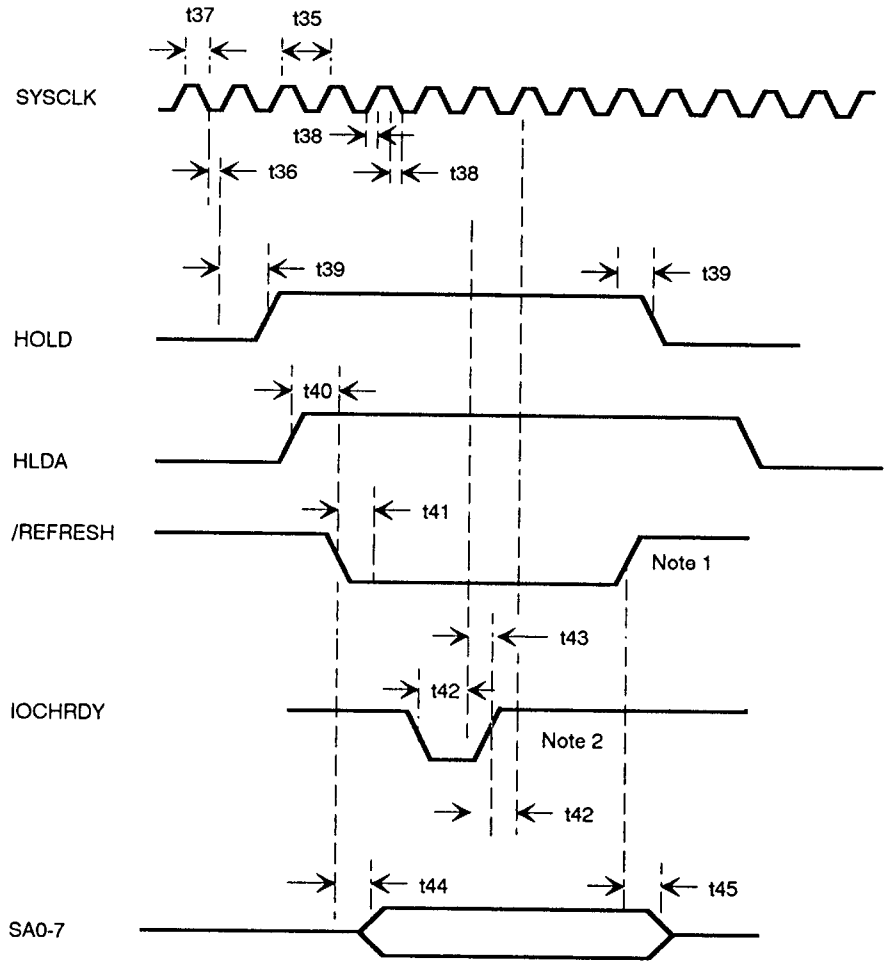


The first wait state is inserted by the internal circuitry of the ACC 2000.
Additional wait states must be inserted using IOCHRDY.

AC Specifications

Symbol	Parameter	Min	Max	Units
t35	SYSCLK cycle time	62		ns
t36	SYSCLK pulse width low	25		ns
t37	SYSCLK pulse width high	25		ns
t38	SYSCLK rise/fall time	10		ns
t39	HOLD valid from SYSCLK high delay time		50	ns
t40	/REFRESH low delay from HLDA		40	ns
t41	/REFRESH low to SYSCLK high setup time		20	ns
t42	IOCHRDY input setup time to SYSCLK high	26		ns
t43	IOCHRDY input hold time from SYSCLK high	15		ns
t44	REFRESH address valid delay from /REFRESH		92	ns
t45	Refresh address hold time from /REFRESH inactive		88	ns

Refresh Timing



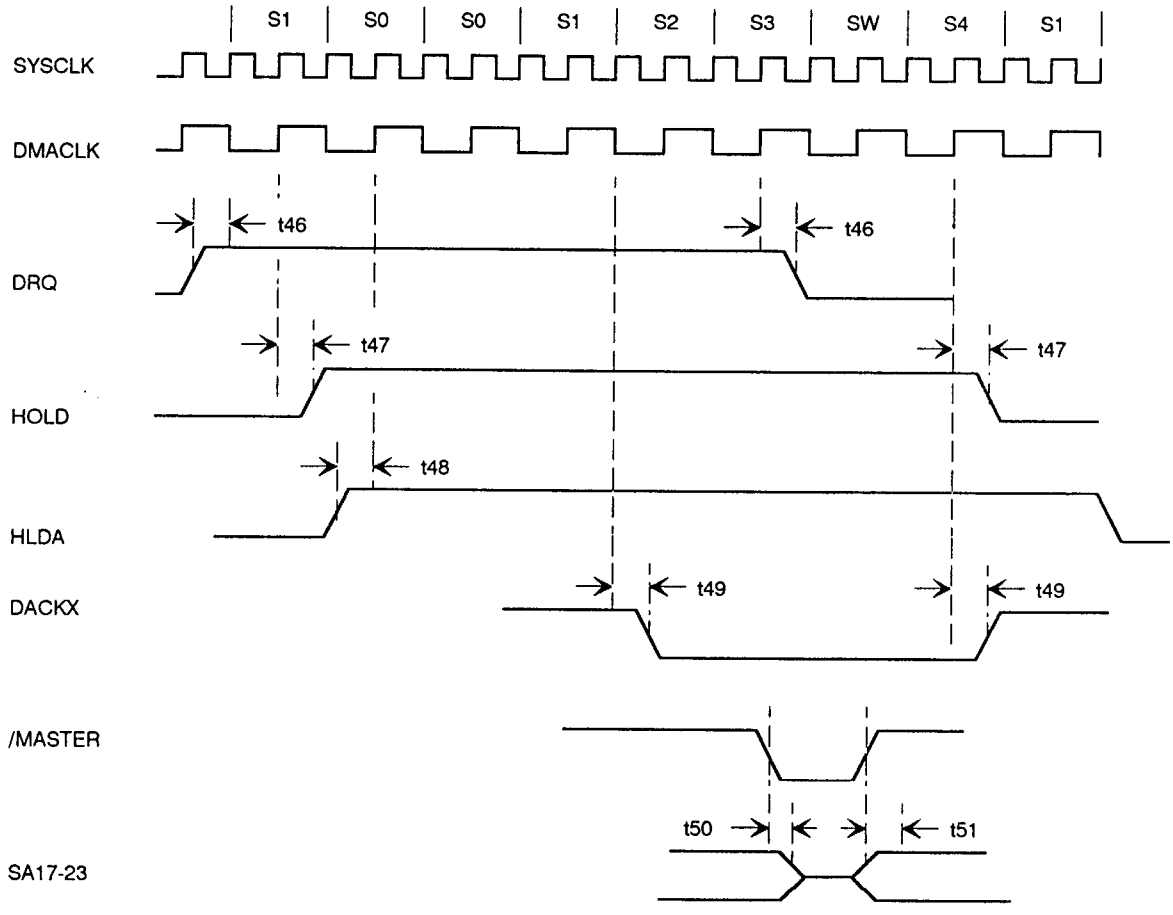
Notes

1 A /REFRESH pulse is normally four SYSCLK cycles long.
2 /REFRESH cycles can be extended by inserting wait states using IOCHRDY.

AC Specifications

Symbol	Parameter	Min	Max	Units
t46	DRQ to SYSCLK high setup time	0		ns
t47	HOLD valid from SYSCLK high delay time		50	ns
t48	HLDA to SYSCLK high set up time	25		ns
t49	/DACK valid from SYSCLK high delay time		83	ns
t50	SA17-SA23 float from /MASTER low delay time	11	36	ns
t51	SA17-SA23 active from /MASTER high delay time	11	36	ns

/MASTER Timing

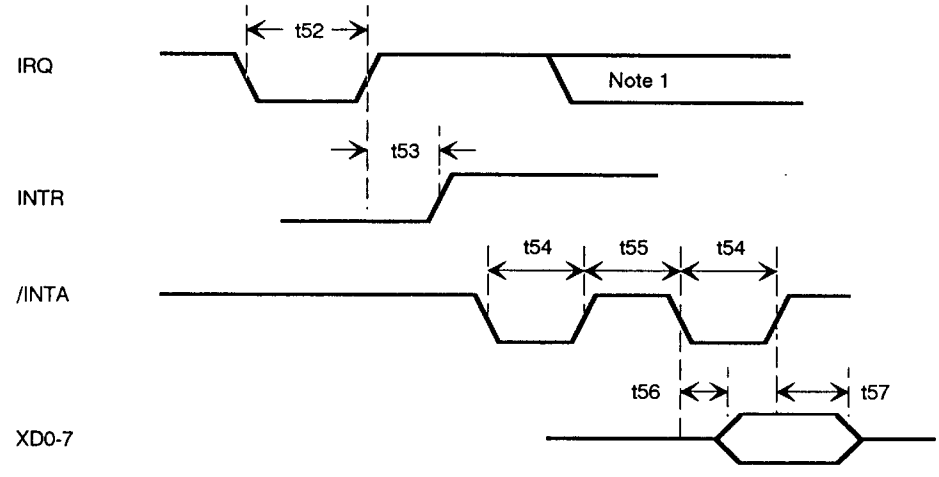


Note: A new bus master must be programmed in Cascade mode.
The new master must not pull /MASTER low until it has received the corresponding /DACK signal.

AC Specifications

Symbol	Parameter	Min	Max	Units
t52	Interrupt request pulse width low	60		ns
t53	Interrupt output delay		63	ns
t54	/INTA pulse width low	80		ns
t55	/INTA to next /INTA within an INTA sequence only	120		ns
t56	XD data valid delay from /INTA low		109	ns
t57	XD data float delay from /INTA high	22	69	ns

Interrupt Timing

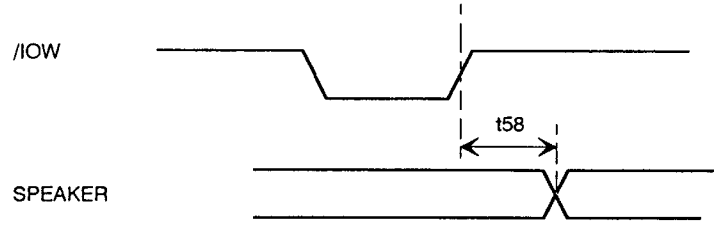


Note 1 IRQ must remain active until the first /INTA pulse.

AC Specifications

Symbol	Parameter	Min	Max	Units
t58	SPEAKER valid from /IOW high delay time		100	ns

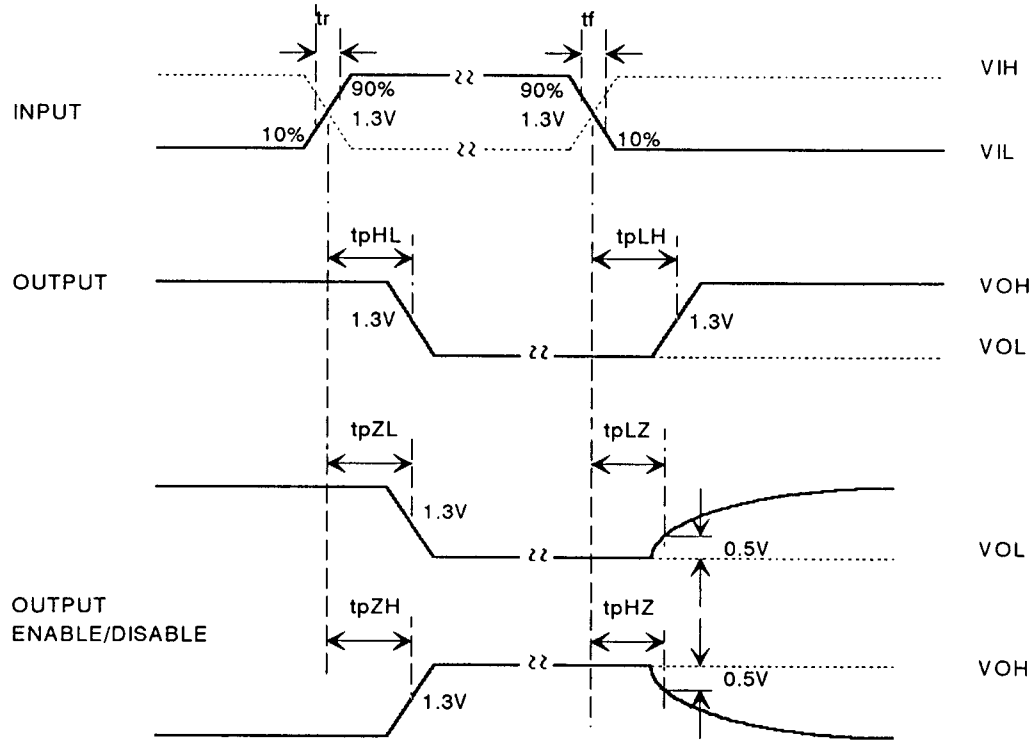
8254 Timing



Load Circuit and AC Characteristics Measurement

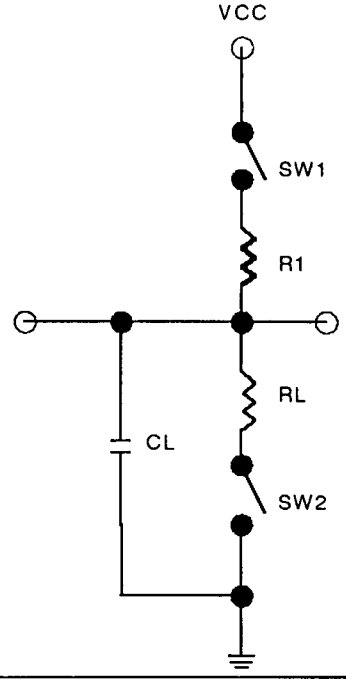
Parameter	Output Type	Symbol	CL(pF)	R1	RL	SW1	SW2
Propagation	Totem pole						
Delay	3-state	tPLH	50		1.0K	off	on
		tPHL	50		1.0K	off	on
Time	Bidirectional						
Propagation	Open drain or	tPLH	50	0.5K		on	off
Delay time	Open collection	tPHL	50	0.5K		on	off
Disable time	3-state	tPLZ	5	0.5K	1.0K	on	on
	Bidirectional	tPHZ	5	0.5K	1.0K	off	on
Enable time	3-state	tPZL	50	0.5K	1.0K	on	on
	Bidirectional	tPZH	50	0.5K	1.0K	off	on

AC Characteristics Measurement



VIH = 3 V, VIL = 0, tr ≤ 10 ns, tf ≤ 5 ns

Load Circuit



ACC 2120
PC/AT Integrated System Controller

The ACC 2120 is an integrated high performance CMOS PC/AT* system controller that integrates the following functions and logic into one single chip: clock generator and selector, bus controller, bus swap logic, coprocessor interface logic, memory decoder, command delay and wait state generation circuits, reset and shut down logic, and ADDR/DATA control logic.

Features

- 100% hardware and software compatible with the IBM* PC/AT
- Supports Intel's 286 and 386SX microprocessors
- Built-in 80287 and 80387SX coprocessor interface logic
- Fully compatible with Intel's 82288 bus controller
- Built-in command delay and wait state generation logic
- Supports CPU operation up to 25 MHz
- Supports 16 MB on board memory
- Turbo speed change performed through hardware or software
- 1-Way, 2-Way or 4-Way page interleaved memory controller
- Optional Direct Access Memory Controller**
- Simultaneous EMS and Shadow RAM **
- Simultaneous extended and EMS expanded memory
- Optional Direct Memory Access mode **
- Supports 64K x 1, 256K x 1, 256K x 4, 1M x 1, 1M x 4, 4 M x 1 memory and 16 MB on motherboard
- 384K Memory mapping above the resident RAM address space
- 512K Memory Mapping above the resident RAM address space **
- Supports shadow RAM for efficient BIOS execution
- Programmable wait states for ROM
- ROM chip select for 27256 or 27512
- Built-in OS/2 optimization circuitry
- Supports EMS 4.0 address translation logic with 4 map registers
- Staggered memory refresh
- 1.2 micron high performance CMOS technology
- 160-pin PFP package

*Trademarks of International Business Machines
**Available fourth quarter 1989

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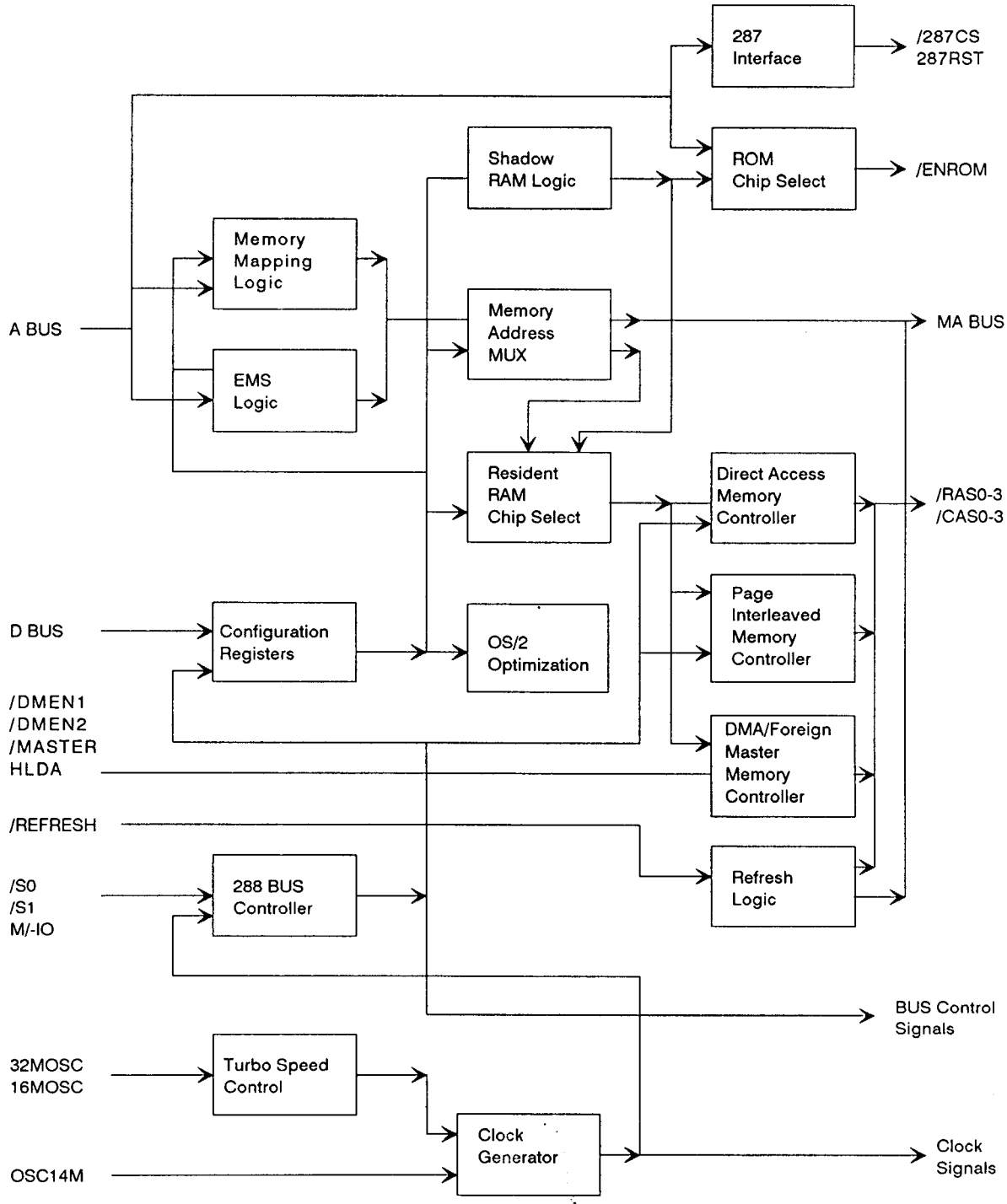
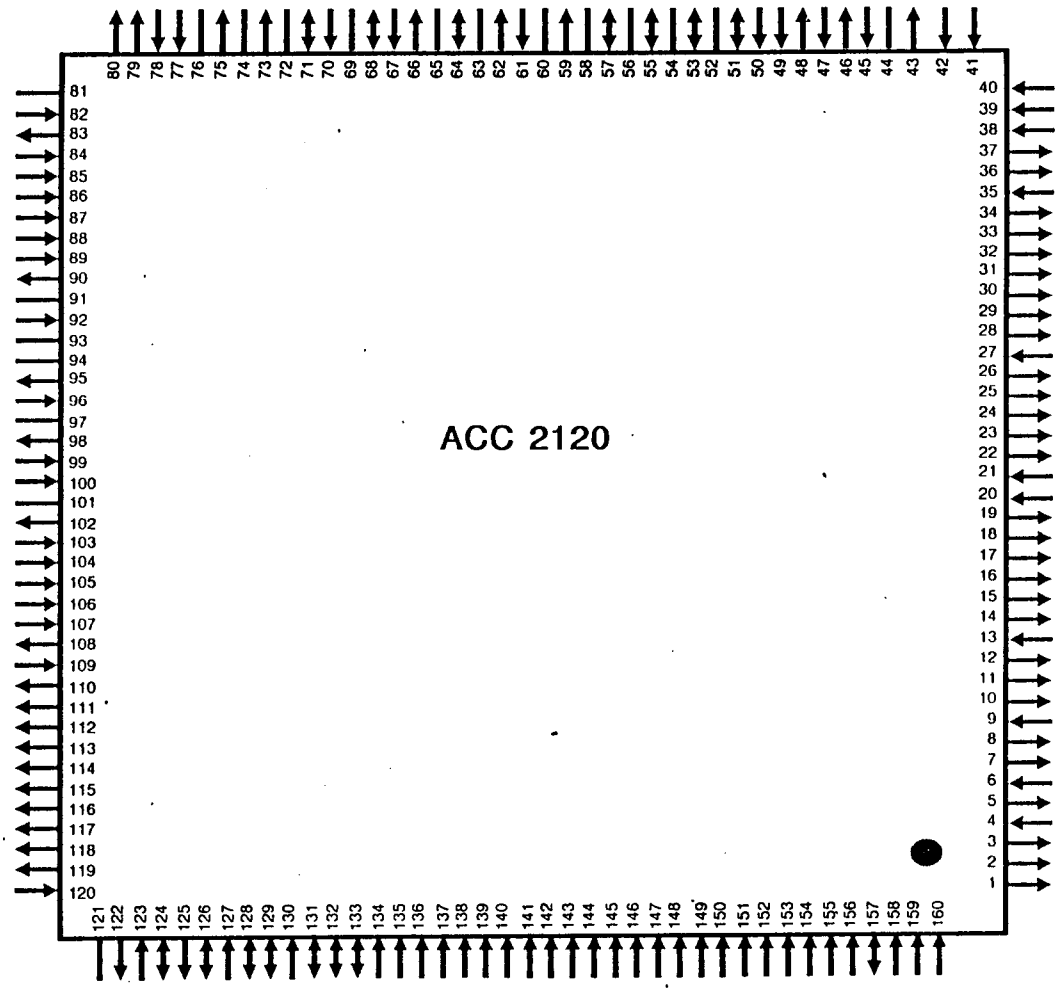
Phone: 408-980-0622 FAX: 408-980-0626

Block Diagram



Pin Diagram



1 /LMEMW	21 VSS	41 /MCS16	61 VSS	81 Reserved	101 Reserved	121 N/C	141 VSS
2 MA0	22 /RAS3	42 /IOCS16	62 PCLK	82 KBLRST	102 /INTA	122 CLK286	142 A6
3 MA1	23 /RAS4	43 RESET	63 N/C	83 CLUART	103 /DMEM1	123 HLDA	143 A7
4 VCC	24 /RAS5	44 N/C	64 /SBHE	84 PWR/GD	104 /DMEM2	124 /SO	144 A8
5 MA2	25 /RAS6	45 /XDEN	65 N/C	85 16MHZ	105 VSS	125 RST286	145 A9
6 VCC	26 /RAS7	46 XDDIR	66 /MDLAT	86 VCC	106 /REFRESH	126 /S1	146 A10
7 MA3	27 VSS	47 /BSY287	67 PWR/MX	87 32MHZ	107 NPCS	127 /BHE	147 A11
8 MA4	28 /CAS0L	48 /BSY286	68 /MEMR	88 VSS	108 IRQ13	128 D0	148 A12
9 VSS	29 /CAS0H	49 VCC	69 N/C	89 HCHF	109 VDD	129 D1	149 A13
10 MA5	30 /CAS1L	50 VSS	70 VSS	90 TURBO	110 L374	130 VSS	150 VSS
11 MA6	31 /CAS1H	51 /IOR	71 /MEMW	91 Reserved	111 CSPCK	131 D2	151 A14
12 MA7	32 /CAS2L	52 N/C	72 N/C	92 /CDINT	112 /ENLBY1	132 D3	152 A15
13 VSS	33 /CAS2H	53 /IOW	73 /SMEMR	93 Reserved	113 /ENLBY2	133 D4	153 A16
14 MA8	34 /CAS3L	54 N/C	74 N/C	94 Reserved	114 /ENHBY	134 M/-IO	154 A17
15 MA9	35 VSS	55 SA0	75 /SMEMW	95 /ENAS	115 DT/-R	135 A0	155 A18
16 MA10	36 /CAS3H	56 N/C	76 N/C	96 GATEA20	116 MDT/-R	136 A1	156 A19
17 /RAS0	37 /ENROM	57 LA20	77 OSC14M	97 KBRST	117 /D245	137 A2	157 A20
18 /RAS1	38 VCC	58 N/C	78 IORDY	98 Reserved	118 /G245	138 A3	158 A21
19 /RAS2	39 /0WS	59 ALE	79 CLK8042	99 /ERROR	119 /READY	139 A4	159 A22
20 VCC	40 /MASTER	60 N/C	80 /RESET	100 VCC	120 VCC	140 A5	160 A23

Pin Descriptions

Symbol	Pin	I/O	Pin Descriptions
Note: All pins are 6 mA drive unless otherwise noted			
/LMEMW	1	O	Resident RAM write enable. 12 mA.
MA0	2	O	Memory address bit. 12 mA.
MA1	3		
MA2	5		
MA3	7		
MA4	8		
MA5	10		
MA6	11		
MA7	12		
MA8	14		
MA9	15		
MA10	16		
/RAS0	17	O	DRAM row address strobe. 12 mA.
/RAS1	18		
/RAS2	19		
/RAS3	22		
/RAS4	23		
/RAS5	24		
/RAS6	25		
/RAS7	26		
/CAS0L	28	O	DRAM column address strobe, low byte. 12 mA.
/CAS1L	30		
/CAS2L	32		
/CAS3L	34		
/CAS0H	29	O	DRAM column address strobe, high byte. 12 mA.
/CAS1H	31		
/CAS2H	33		
/CAS3H	36		
/ENROM	37	O	ROM chip select. Active low.
/0WS (TSTCLR)	39	I	Zero wait state input.
/MASTER	40	I	Signal to gain system control.
/MCS16	41	I	Memory 16-bit chip select.
/IOCS16	42	I	I/O 16-bit chip select.
RESET	43	O	System reset. Active high.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/XDEN	45	I	XD enable input.
XDDIR	46	O	XD direction output.
/BSY287	47	I	Busy math processor input.
/BSY286	48	O	Busy CPU output.
/IOR	51	I/O	I/O read. 24 mA
/IOW	53	I/O	I/O write. 24 mA
SA0	55	I/O	System address bit 0, select low byte. 24 mA
LA20	57	I/O	LA Bus, A20 I/O pin. 24 mA
ALE	59	O	Address latch enable. 24 mA
PCLK	62	O	Peripheral clock. 24 mA
/SBHE	64	I/O	System bus high byte enable. 24 mA
/MDLAT	66	O	Memory data latch.
PWR/MX	67	I	Debounce bypass.
/MEMR	68	I/O	Memory read. 24 mA
/MEMW	71	I/O	Memory write. 24 mA
/SMEMR	73	O	System memory read. 24 mA
/SMEMW	75	O	System memory write. 24 mA
OSC14M	77	I	14.318 MHz oscillator input.
IORDY	78	I	I/O channel ready.
CLK8042	79	O	8042 Clock. 12 mA
/RESET	80	O	System reset. Active low.
Reserved	81		
KBLRST	82	I	Reset switch input.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
CLUART	83	O	UART clock 12 mA
PWR/GD	84	I	Power good.
16MHZ	85	I	16 MHz OSC input.
32MHZ	87	I	System frequency OSC input.
HCHF	89	I	Hardware Turbo mode select.
TURBO	90	O	Turbo mode. 12 mA
Reserved	91		Tied to VCC.
/CDINT	92	I	386SX input
Reserved	93		Tied to VCC.
Reserved	94		Tied to VCC.
/ENAS	95	O	Real time clock address strobe enable.
GATEA20	96	I	Gate A20 enable. Active low.
KBRST	97	I	Keyboard reset.
Reserved	98		Do not connect.
/ERROR	99	I	Error status.
Reserved	101		Do not connect.
/INTA	102	O	Interrupt acknowledge. Active low.
/DMEN1	103	I	DMA address enable for 8-bit data transfer. Active low.
/DMEN2	104	I	DMA address enable for 16-bit data transfer. Active low.
/REFRESH	106	I	Refresh cycle. Active low.
NPCS	107	I	Numeric processor chip select.
IRQ13	108	O	Interrupt request.
L374	110	O	Latch enable for CPU data bus to system data bus conversion.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
CSPCK	111	O	Parity error output enable.
/ENLBY1	112	O	System data bus to local data bus low byte output enable (active low). Used for 8-bit I/O port or extension memory read.
/ENLBY2	113	O	System/Local data bus (CSPCK=0) or Memory/Local data bus (CSPCK=1) low byte transfer enable. Active low.
/ENHBY	114	O	Enable high byte.
DT/-R	115	O	Data transmit/receive.
MDT/-R	116	O	Memory data transmit/receive.
/D245	117	O	Direction control for LS245.
/G245	118	O	Gate input for LS245.
/READY	119	O	Ready signal to CPU. 12 mA
CLK286	122	O	System clock input. 24 mA
A0	135	I	CPU address bit.
A1	136	I	
A2	137	I	
A3	138	I	
A4	139	I	
A5	140	I	
A6	142	I	
A7	143	I	
A8	144	I	
A9	145	I	
A10	146	I	
A11	147	I	
A12	148	I	
A13	149	I	
A14	151	I	
A15	152	I	
A16	153	I	
A17	154	I	
A18	155	I	
A19	156	I	
A20	157	I/O	12mA

Pin Descriptions

Symbol	Pin	I/O	Pin Description
A21	158	I	
A22	159	I	
A23	160	I	
HLDA	123	I	Hold acknowledge from CPU.
/S0	124	I/O	Bus cycle status bit. 12 mA
/S1	126		
RST286	125	O	Reset CPU.
/BHE	127	I	High byte enable from CPU.
D0	128	I/O	CPU data bus. 12 mA
D1	129		
D2	131		
D3	132		
D4	133		
M/-IO	134	I	Memory or I/O select.
VCC	4, 6, 20, 38, 49, 86, 100, 109, 120		+5 volts
VSS	9, 13, 21, 27, 35, 50, 61, 70, 88, 105, 130, 141, 150		Ground
N.C.	44, 52, 54, 56, 58, 60, 63, 65, 69, 72, 74, 76, 121		

Functional Description

Bus Controller and Converter

The ACC 2120 CPU bus controller is functionally equivalent to Intel's 82288 multi-bus adapter, providing CPU bus and signal control for both system and peripheral buses. The /S0, /S1 and M/-IO signals carry data from the CPU, announcing a bus cycle and defining its type. Table 1 lists and defines the different types of bus cycles.

Table 1 ACC 2120 Bus Cycle Definitions

COD, /INTA	M/-IO	/S1	/S0	Bus Cycle Initiated
0 (low)	0	0	0	Interrupt acknowledge
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Not a status cycle
0	1	0	0	If A1=1, then halt; else, shutdown
0	1	0	1	Memory data read
0	1	1	0	Memory data write
0	1	1	1	Not a status cycle
1 (high)	0	0	0	Reserved
1	0	0	1	I/O read
1	0	1	0	I/O write
1	0	1	1	Not a status cycle
1	1	0	0	Reserved
1	1	0	1	Memory instruction read
1	1	1	0	Reserved
1	1	1	1	Not a status cycle

The CPU bus controller has four operation modes.

AT CPU Mode

This mode is active when HLDA is low. The CPU bus controller generates /IOR, /IOW, /INTA, /MR288, /MW288, and DT/-R signals.

DMA Mode

DMA mode is active if HLDA and /DMEN1 or /DMEN2 signals are active. The DMA controller drives the /IOR, /IOW, /MR288, and /MW288 signals.

Refresh Mode

Refresh mode is active when a refresh request is output from the ACC 2000. The /MR288 signal generates the refresh for DRAM memory. /MW288, /IOR, and /IOW signals are in high impedance state.

Master Mode

Master mode is active when HLDA is active and a card in the I/O slot pulls /MASTER low. The card controls system address, data line and control line.

BUS Conversion

The ACC 2120 contains logic to convert between 16-bit and 8-bit data accessing. The /D245 and /G245 signals control this interface logic.

287 Interface Control

Additional circuitry supports the decoding required to select and reset the numeric coprocessor. /287CS is a chip select decoded at addresses 0F8-0FF hex. The RST287 signal resets the math coprocessor. RST287 is activated by a system reset or by performing a write operation to I/O port 0F1 hex. IRQ13 is connected to the ACC 2000 IRQ13 line.

386SX CPU Interface

The 386SX CPU interface provides logic to convert /ADS, W/-R, and D/-C signals to equivalent 286 signals (/S0 and /S1). It also enables a timed reset, ensuring the CPU is synchronized to the system. See figure 1.

386SX CPU timing is incompatible with 286 CPU timing because the 386SX starts its cycle on the rising edge of the clock and the 286 starts its cycle on the falling edge. To correct this problem, the ACC 2120 has logic designed to invert CLK286 automatically.

387SX Interface

The ACC 2120 provides an interface between the 80387SX and the 80386SX by interconnecting /ADS, /WR, M/-IO, A23, A2, RESETIN, and CLK2 signals between the CPU and the 387SX. /READYO is fed back to the ACC 2120 from the 387SX when coprocessor cycles are terminated. A high-speed transfer of opcodes and operands between the 386SX and the 387SX occurs through a communication protocol.

Coprocessor errors are handled with an ACC 2000 request, through a standard ISA scheme from IRQ13.

The 80387SX can run in synchronous or asynchronous mode by connecting CKM to VCC or GND respectively. However, to run in asynchronous mode, the 80387SX requires an independent clock source for NUMCLK2.

Clock Generator

The ACC 2120 Clock Generator provides clock signals to support internal timing requirements. It provides clock outputs for the CPU, the NPU, the DMA, the Keyboard Controller, and the UART. Clock signals are generated from three oscillator inputs, OSC14M, OSC16M, and OSC32M. The OSC14M is driven by a 14.31818 MHz oscillator. This frequency generates output clocks, CL287, CL8042, and CLUART. The other two oscillators are used to

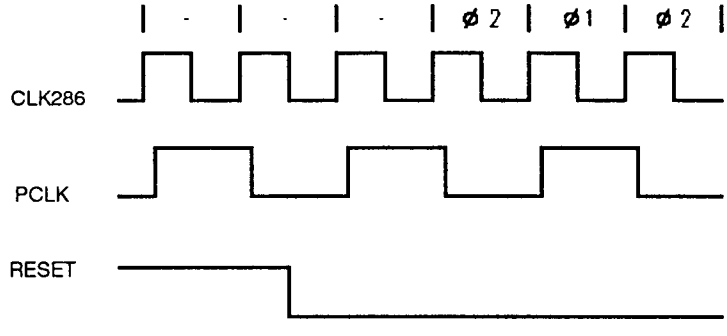


Figure 1 RESET and PCLK Timing for 80386SX CPU

generate CPU and AT Bus clocks. The CPU clock is switched between these two inputs by turbo speed control logic. For normal speed and AT Bus cycles, the CPU clock is switched to OSC16M and driven by a 16 MHz oscillator, obtaining a processing speed of 8 MHz. Processing speed equals half the CPU clock frequencies. For turbo speed, the CPU clock is switched to OSC32M, with variable input frequency. A 32 MHz frequency is used for a turbo processing speed of 16 MHz. A 25 MHz or 20 MHz oscillator is used for 12.5 MHz or 10 MHz processing speed, and a 40 MHz oscillator is used for a 20 MHz processing speed. A 50 MHz oscillator is used for a speed of 25 MHz.

Turbo Speed Control Logic

The system clock is switched between turbo and normal speed by either software or hardware.

If the CHF bit in the configuration register is programmed high or the HCHF signal generates a rising edge trigger, the system clock generator can be set to turbo mode by selecting the higher speed (32 MHz) oscillator. Otherwise, a slower speed oscillator is selected, and the system clock runs at normal speed.

Configuration Registers

The ACC 2120 contains thirteen configuration registers which provide a variety of functions. These functions are concerned with system initialization and software control of advanced memory control features. For system initialization, these configuration registers implement a no-cost, no-space alternative to system board DIP switches. For advanced memory control, these registers provide maximum flexibility and convenience for programming. Configuration registers are selected by the configuration index register at I/O address F2. Table 2 contains a summary of configuration registers.

Configuration registers are programmed with an indirect addressing scheme using I/O addresses F2 and F3. I/O address F2 contains

Table 2 ACC 2120 Configuration Registers

Register	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20	TPI		memory configuration select		
21	CHF	---	---	DA/PI	---
22	---	SH2WR	SH2EN	SH3WR	SH3EN
23	MMEN	EMSEN	---	ROM wait state select	
24	ER0A23	ER0A22	ER0A21	ER0A20	ER0A19
25	ER0A18	ER0A17	ER0A16	ER0A15	ER0A14
26	ER1A23	ER1A22	ER1A21	ER1A20	ER1A19
27	ER1A18	ER1A17	ER1A16	ER1A15	ER1A14
28	ER2A23	ER2A22	ER2A21	ER2A20	ER2A19
29	ER2A18	ER2A17	ER2A16	ER2A15	ER2A14
2A	ER3A23	ER3A22	ER3A21	ER3A20	ER3A19
2B	ER3A18	ER3A17	ER3A16	ER3A15	ER3A14
31				HOTSWR	ENGA20

the write-only configuration index register. F2 selects the corresponding configuration register accessed at I/O address F3. To write a value of "E8" into configuration register 2A, the configuration index register at I/O address F2 must first be written with a value of "2A," then register at I/O address F3 with a value of "E8." Configuration registers are selected by the configuration index register at I/O address F2. Table 2 contains a summary of configuration registers.

The specific functions of each configuration register are detailed below.

Configuration Register 20

Bit	Function
7-5	Unused
4	Turbo Page Interleaved mode
3-0	Memory configuration select

Bit 4 When set to 1, this bit selects the Turbo Page Interleaved mode which provides improved memory performance (approximately 0.4 wait states) but requires faster DRAMs. Default is zero.

Bits 3-0
These bits are encoded to select the type and quantity of system board DRAM. Refer to following table. Default for these bits is 9 hex.

An unused bit is ignored by the system and is always read back as a one.

Note that system board memory is organized in banks consisting of 18 bits of DRAM each (two 8-bit bytes plus two parity bits).

Bits 3 2 1 0	Option	Banks	Type	Total DRAM
0 0 0 0	0	1	256K	
		1	64K	640K*
0 0 0 1	1	1	256K	512K
0 0 1 0	2	2	256K	1M
0 0 1 1	3	4	256K	2M
0 1 0 0	4	6	256K	3M
0 1 0 1	5	8	256K	4M
0 1 1 0	6	1/2	1M	1M
0 1 1 1	7	1	1M	2M
1 0 0 0	8	2	1M	4M
1 0 0 1	9	4	1M	8M
1 0 1 0	10	6	1M	12M
1 0 1 1	11	8	1M	16M
1 1 0 0	12	1	4M	8M
1 1 0 1	13	2	4M	16M

* Option 0 has two different types of memory, one type for each bank, to obtain a total of 640K RAM.

Configuration Register 21

Bit	Function
7-5	Unused
4	Turbo mode select
3-2	Reserved
1	Direct access/Page Interleaved mode select
0	Reserved

Bit 4 When set to 1, this bit selects the Turbo frequency mode. When this bit is set high, the system is placed in Turbo mode. Default is zero.

Bit 1 When set to 1, this bit selects the direct access memory control mode. This mode provides zero wait state performance but requires fast DRAM. When set to 0, this bit selects the Page interleaved memory control mode.

Page interleaved mode reduces performance by only 0.4 to 0.7 wait states, but functions with slower and less expensive DRAMs. Default for Bit 1 is zero.

Note that all reserved bits must be written to zero, even though they can read back as ones. Any readback from reserved bits can be ignored.

Configuration Register 22

Bit	Function
7-5	Unused
4	Reserved
3	Shadow RAM write only mode, Segment 2
2	Shadow RAM enable, Segment 2
1	Shadow RAM write only mode, Segment 3
0	Shadow RAM enable, Segment 3

Bit 3 When set to 1, this bit places the Shadow RAM for Segment 2 (0C0000 to 0DFFFF) into write mode. Refer to the Shadow RAM description. Default is zero.

Bit 2 When set to 1, this bit enables the Shadow RAM at Segment 2 (0C0000 to 0DFFFF). Default is zero.

Bit 1 When set to 1, this bit places the Shadow RAM at Segment 3 (0E0000 to 0FFFFF) into write mode. Default is zero.

Bit 0 When set to 1, this bit enables the Shadow RAM at Segment 3 (0E0000 to 0FFFFF). Default is zero.

Configuration Register 23

Bit	Function
7-5	Unused
4	Memory mapping enable
3	EMS enable
2	Reserved
1,0	ROM wait state select

Bit 4 When set to 1, this bit enables the memory mapping feature. Default is zero.

Bit 3 When set to 1, this bit enables the EMS feature. Default is zero.

Bits 1,0

These bits select the number of wait states that are inserted for all ROM read cycles. These bits default to the 3 wait state select.

Bits 1	Bits 0	Select
0	0	1 wait state
0	1	2 wait states
1	0	3 wait states

Configuration Registers 24-2B

The ACC 2120 supports four EMS registers. Configuration register pairs 24 and 25, 26 and 27, 28 and 29, 2A and 2B, each constitute one EMS register. These pairs are defined as EMS registers 0 through 3. The contents of these pairs provide alternate address bits for A14-23 during EMS accesses. All EMS registers default to zero.

EMS Register 0
Configuration Register 24

The 16 KByte EMS window for EMS register 0 is located at address range 0D0000 to 0D3FFFF.

Bit	Definition
7-5	Unused
4	ER0, A23
3	ER0, A22
2	ER0, A21
1	ER0, A20
0	ER0, A19

Configuration Register 25

Bit	Definition
7-5	Unused
4	ER0, A18
3	ER0, A17
2	ER0, A16
1	ER0, A15
0	ER0, A14

EMS Register 1
Configuration Register 26

The 16 KByte EMS window for EMS register 1 is located at address range 0D4000 to 0D7FFF.

Bit	Definition
7-5	Unused
4	ER1, A23
3	ER1, A22
2	ER1, A21
1	ER1, A20
0	ER1, A19

Configuration Register 27

Bit	Definition
7-5	Unused
4	ER1, A18
3	ER1, A17
2	ER1, A16
1	ER1, A15
0	ER1, A14

EMS Register 2
Configuration Register 28

The 16 KByte EMS window for EMS register 2 is located at address range 0D8000 to 0DBFFF.

Bit	Definition
7-5	Unused
4	ER2, A23
3	ER2, A22
2	ER2, A21
1	ER2, A20
0	ER2, A19

Configuration Register 29

Bit	Definition
7-5	Unused
4	ER2, A18
3	ER2, A17
2	ER2, A16
1	ER2, A15
0	ER2, A14

EMS Register 3
Configuration Register 2A

The 16 KByte EMS window for EMS register 3 is located address range 0DC000 to 0DFFFF.

Bit	Definition
7-5	Unused
4	ER3, A23
3	ER3, A22
2	ER3, A21
1	ER3, A20
0	ER3, A19

Configuration Register 2B

Bit	Definition
7-5	Unused
4	ER3, A18
3	ER3, A17
2	ER3, A16
1	ER3, A15
0	ER3, A14

Configuration Register 31

Bit	Function
7-2	Unused
1	Hot software reset
0	Enable gate A20

Bit 1 This bit triggers a CPU reset when set to 1.

Bit 0 This bit enables address A20 when set to 1.

DRAM Configuration (including single 1M DRAM option)

The ACC 2120 has fourteen memory configuration options which use various sizes and amounts of DRAM to provide up to 16 MB of system board memory. Table 3 lists the memory options available.

Table 3 ACC 2120 Memory Options

Memory Configuration	Number of Banks	Type of Memory	Total Memory
0	1	256K	640K
	1	64K	
1	1	256K	512K
2	2	256K	1M
3	4	256K	2M
4	6	256K	3M
5	8	256K	4M
6	1/2	1M	1M
7	1	1M	2M
8	2	1M	4M
9	4	1M	8M
10	6	1M	12M
11	8	1M	16M
12	1	4M	8M
13	2	4M	16M

Note that all DRAMs must be the same type (e.g., all 256K) on the system board except the 640K option which uses 256K and 64K DRAMs in two banks separately.

The single 1M module option (Option 6) is the only memory option that uses less than one bank of DRAM. This option is economical, using only one memory module. Performance is affected because eight bits must be converted to 16 bits (two memory cycles) for the CPU.

The ACC 2120 supports eight memory banks, each containing 18 bits of DRAM. These 18 bits comprise two 8-bit bytes, plus two parity bits, one for each byte.

Page Interleaved Memory Controller Page Interleaved Mode

The ACC 2120 implements a 4-way, 2-way, and 1-way page interleaved memory controller, providing optimum system performance for high speed CPUs. This option offers near Direct Access performance (approximately 0.4 to 0.7 wait state average), while operating with a slower and less expensive DRAM. The Page Interleaved Memory Controller operates on two principles: Page Mode Memory access, which is much faster than random access, and the sequential and localized patterns it follows.

The Page Interleaved Memory Controller organizes the memory array into interleaved pages by banks, operating up to four banks simultaneously in Page mode. Each bank of memory consists of 18 bits of DRAM (two 8-bit bytes plus two parity bits).

The size of a memory page is determined by the type of DRAM installed. A 256K DRAM provides a page size of 1K bytes (512 column bits per DRAM row times 16 DRAMs per bank), 1M DRAM provides a 2K page size, and 4M DRAM provides a 4K page size. These page sizes are a result of the physical architecture of the DRAM. Once page mode is selected, a row can be kept active (/RAS low) almost indefinitely (up to 10uS), allowing any number of column accesses along that same row. Each row, and any intersecting column access along that same row, is defined as a "Page Hit." This results in a zero wait state access. If any subsequent memory access selects a new row, it is defined as a "Page Miss" and results in a three wait state access.

The organization and operation of the memory array is dependent on the type and quantity of memory installed (See "Configuration Registers" section). Memory performance is improved when a greater number of open pages, up to four, are used. This provides a larger and more flexible "zero wait state" work space. The open page on each bank retains the last row address selected on that particular bank.

The ACC 2120 offers flexible memory bank configurations supporting one bank, two banks, four banks, six banks, and eight banks. When more than four banks of memory are installed, Banks 0 and 4, 1 and 5, 2 and 6, and 3 and 7 are paired so that CAS lines can be shared. This means that only one bank of each pair can be active at any given time. For example, if six banks of memory are installed, Banks 0 and 4, and Banks 1 and 5 share the same CAS lines. Banks 2 and 3 have their own CAS lines. The four simultaneously open pages can reside in either banks 0, 1, 2, 3, banks 0, 5, 2, 3, banks 4, 1, 2, 3, or banks 4, 5, 2, 3 while in the 4-Way Page Interleaved mode.

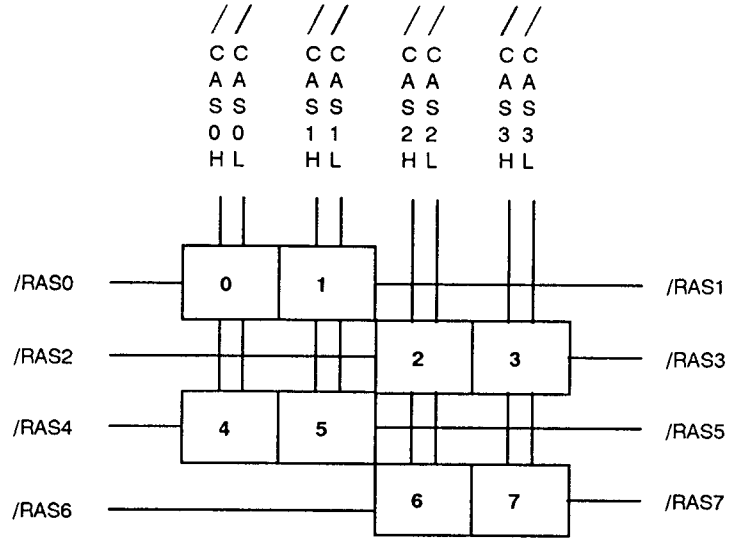


Figure 2 ACC 2120 Memory Bank Configurations

Turbo Page Interleaved Mode

The ACC 2120 Page Interleaved mode provides optimum flexibility in DRAM selection, by utilizing the most available and least expensive DRAMs. With a faster DRAM, the Turbo Page Interleaved mode increases system performance. While in the Turbo Page Interleaved mode, if there is a memory miss, two wait states will be inserted. Overall system performance averages approximately 0.7 wait states for Page Interleaved Mode, and is reduced to approximately 0.4 wait states for Turbo Page Interleaved mode. (See Table 4).

Direct Memory Access Controller**

The Direct Memory Access Controller provides the highest level of system performance for slower systems in the 8, 10, and 12.5 MHz range. Direct Access initiates all CPU cycles to system RAM, with zero wait states. When memory access is under the control of the DMA Controller or AT I/O Bus, process time is slower, but this seldom occurs. Direct Access Control provides the best overall system at any given CPU speed. Direct Access needs high speed DRAM.

**Available fourth quarter 1989

Memory Mapping

Memory Mapping translates system RAM within the 640 KB to 1MB range, which cannot be accessed normally, to an accessible address range, above the physical RAM space.

Memory address space between the 640 KB to 1MB range, which is reserved for system ROM and BIOS application, cannot be used to access physical DRAM. Memory Mapping translates physical RAM space within the 640 KB to 1MB range to memory addresses above the actual installed memory size. For example, if 4 MB of memory are installed, and the memory mapping feature is on, the DRAMs in the 640 KB to 1MB range are mapped to an address above 4 MB.

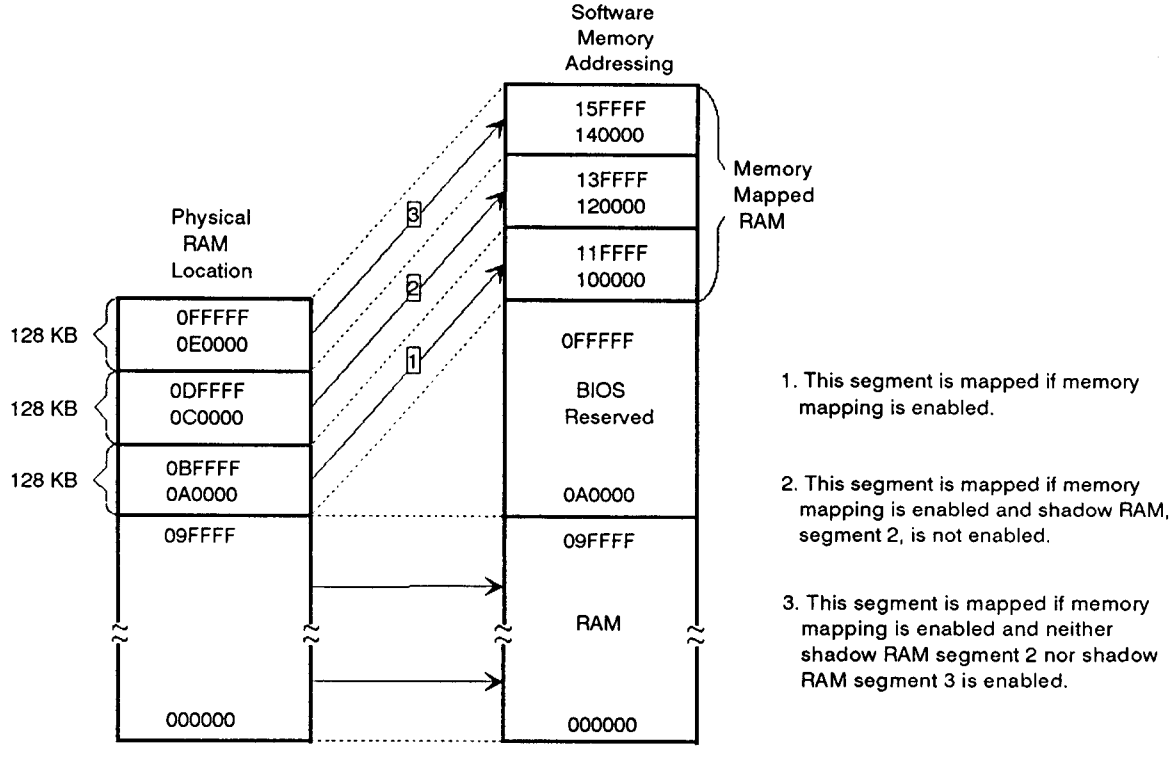


Figure 3 Memory Mapping for a 1 MB System

Memory Mapping is enabled from the configuration register by writing bit 4 of Register 23 to a 1. When Shadow RAM is enabled simultaneously with Memory Mapping, the quantity of RAM available for Memory Mapping is reduced. If Shadow RAM segment 3 is enabled, 256 KB of RAM can be mapped. If Shadow RAM 2 is enabled, only 128 KB of RAM can be mapped. See Figure 3 for the memory mapping involved in a 1MB system and Figure 4 for a 2 MB system.

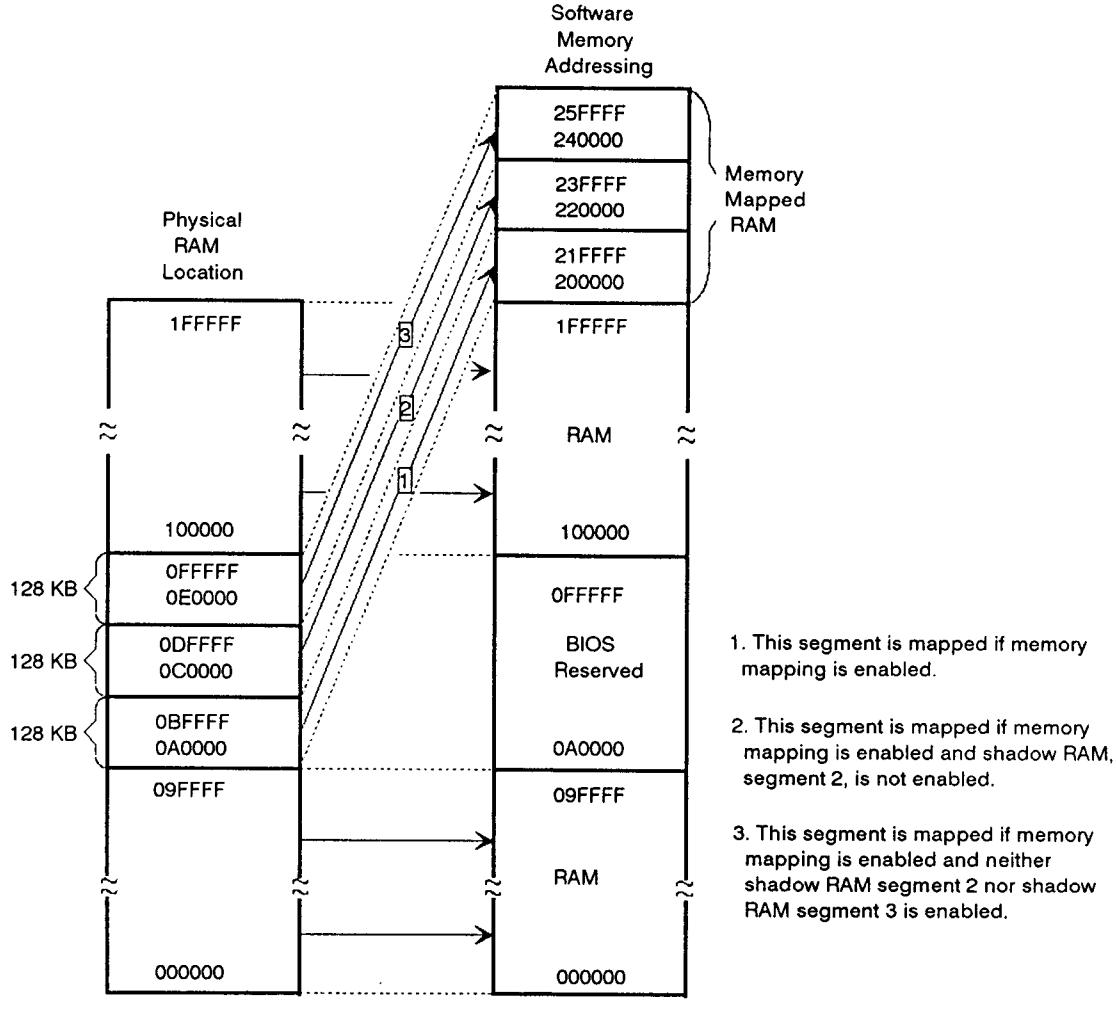


Figure 4 Memory Mapping for a 2 MB System

EMS 4.0

EMS (Extended Memory Specification) is a method of indirectly addressing an extended area of RAM. EMS uses a window in the 384 KB address range dedicated to the system, and indirectly addresses memory through that window. There are four EMS registers in the ACC 2120.

The main application for EMS is in DOS systems whose programs can only access 1MB because the address range has only 20 address bits. (The 8086 had only 20 bits). If a system has more than 1MB of RAM, and DOS can only address 1MB, the remaining memory can only be used by addressing the memory indirectly.

The EMS window (0D0000 to 0DFFFF), is broken into four 16 KB segments. Each of these segments is associated with one of four EMS address registers (See figure 5), where each EMS address register represents ten address bits (A23 to A14). When the EMS window is selected, these bits replace system address bits A23 to A14, giving EMS software the ability to redirect memory addresses from the four EMS windows to anywhere in the resident RAM address range.

EMS is enabled in the Configuration Register by writing Bit 3 of Register 23 to a 1. The four EMS address registers are also programmed within the Configuration Registers.

For example, to access memory at location 230FFF, EMS must be enabled and an address register must be programmed using the upper ten bits of memory address. Address Register 0 is programmed with 0010-0011-00 and the 16 KB block of memory from 230000 to 233FFF is available for Register 0 (located between 0D0000 to 0D3FFF). A memory access to software address 0D0FFF is directed to 230FFF.

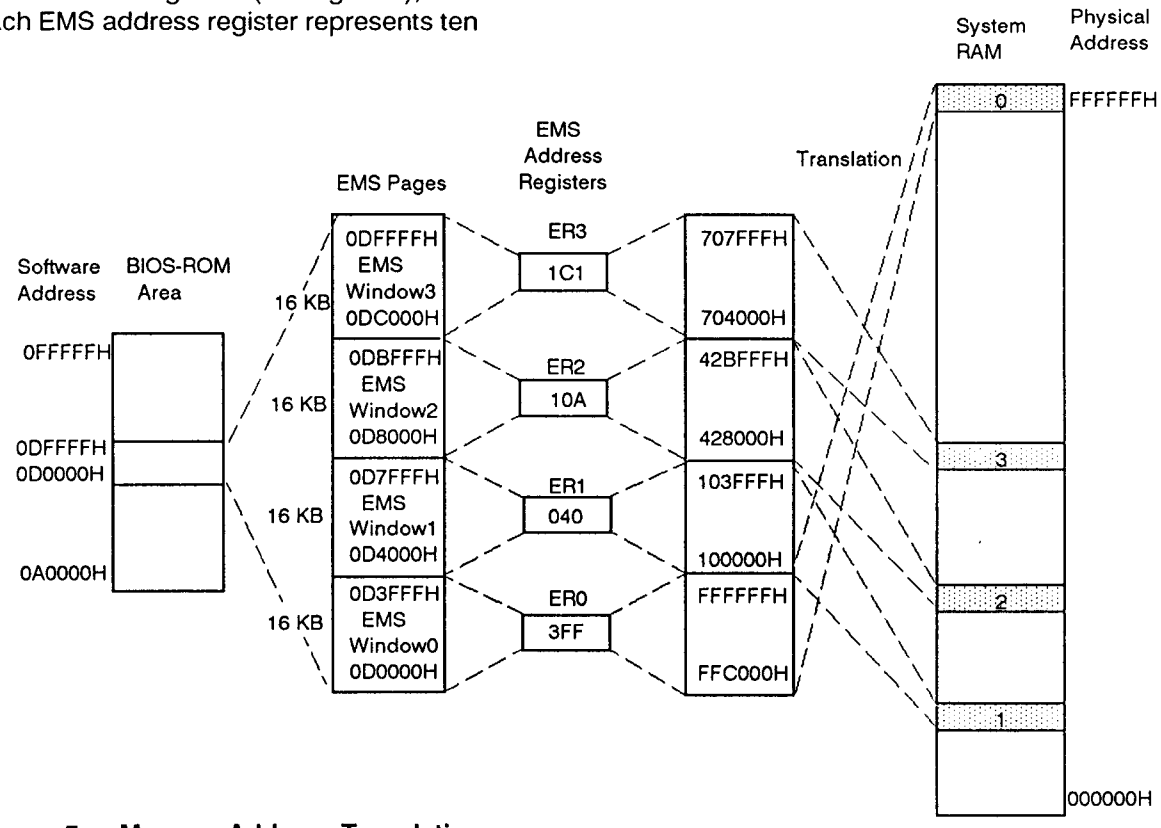


Figure 5 Memory Address Translation

Shadow RAM

Shadow RAM provides an option to transfer BIOS or video-extension BIOS program codes into system RAM. This option provides significant performance improvement for applications requiring intensive BIOS calls.

Shadow RAM implements an alternate BIOS source by copying the complete EPROM program code into system RAM. This is referred to as "shadowing" because the DRAM and EPROM are both located at the same physical address space. This change is transparent to the rest of the system. ROM can be disabled, allowing the RAM to respond in its place. The advantage of this procedure is that DRAM access time is typically much faster than EPROM access time.

The ACC 2120 Shadow RAM is configured in two independent segments. Segment 3 shadows the BIOS ROM at addresses 0E0000

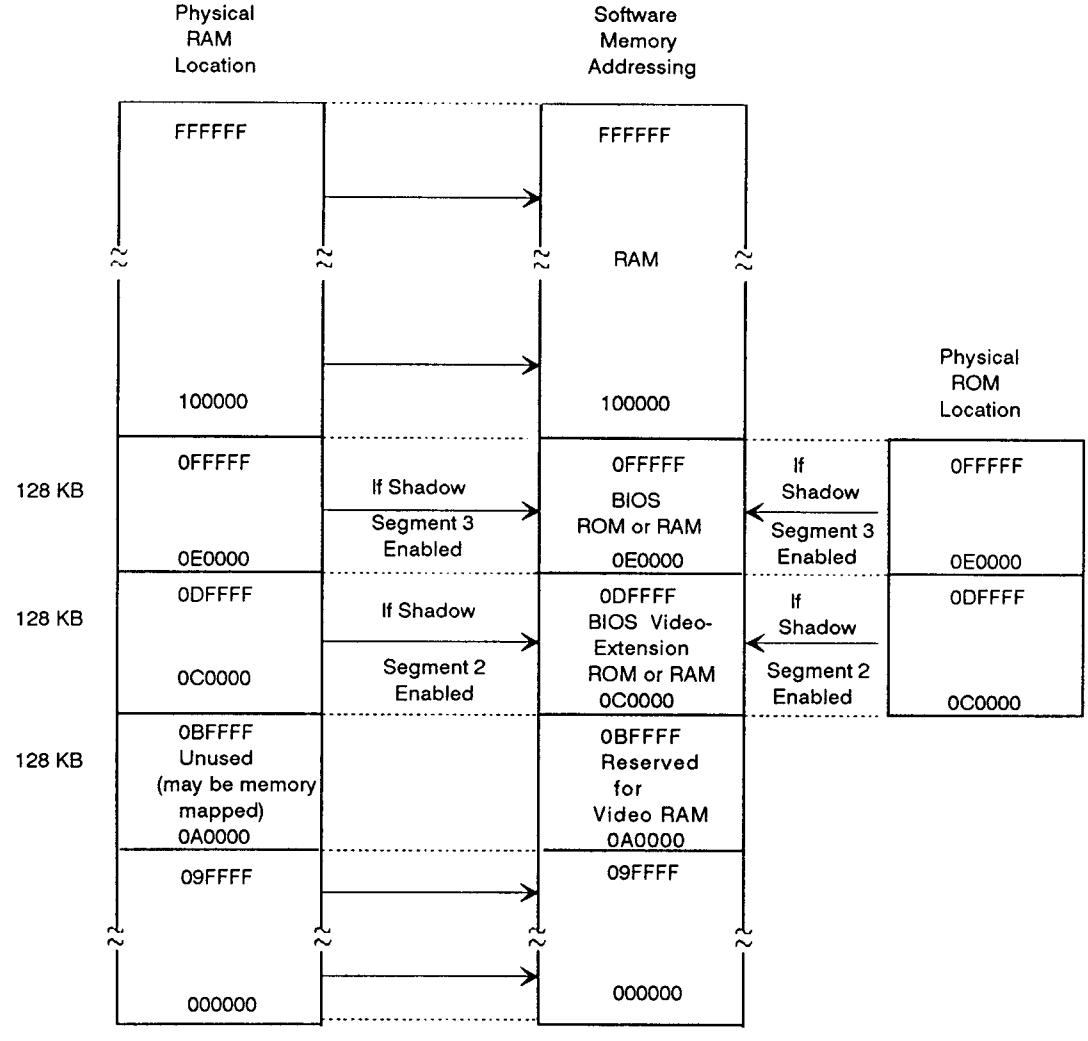


Figure 6 ACC 2120 Shadow RAM Address Map

to 0FFFFF, and Segment 2 shadows the BIOS video-extension ROM at addresses 0C0000 to 0DFFFF. Both Shadow RAM segments are written and enabled using four control bits in Configuration Register 22.

Enabling each Shadow RAM segment requires two steps. The "Shadow RAM Write Mode" for Segment 2 or 3 must be activated to allow the transfer of BIOS program code from EPROM to DRAM. Transfer is made by a read from the EPROM and a write to system DRAM at the same address. The next step activates the "Shadow RAM Enable" of the corresponding Segment, disables the EPROM in that segment, and places the DRAM, in that segment, in read-only mode.

Each Shadow RAM segment is completely independent and can be enabled individually or at the same time. Note that enabling Shadow RAM segments reduces the quantity of memory that can be remapped using the Memory Mapping feature. Figure 6 diagrams Shadow RAM in the ACC 2120.

OS/2 Optimization

The ACC 2120 implements OS/2 optimization, which is a more efficient way to switch back and forth from real to protected mode in an OS/2 environment when frequent DOS calls are made. Conventional methods require the processor to issue two commands to the keyboard controller in switching to protected mode and activating gate A20.

With OS/2 optimization, the ACC 2120 implements a hot software CPU reset by switching Register 31, Bit 1 to 1, and enables gate A20 through switching Register 31, Bit 0 to 1. OS/2 optimization provides substantial performance improvement in an OS/2 environment.

Staggered Refresh Logic

ACC 2120 refresh logic works with the ACC 2000 to perform a periodic refresh for both system DRAM and extended RAM on the AT Bus. The ACC 2000 initiates a refresh cycle by driving its /REFRESH output low, and signaling the ACC 2120 to drive the refresh address onto the MA Bus, simultaneously generating staggered refresh pulses on the eight RAS outputs. The RAS outputs are staggered to reduce the current drain caused by the refresh operation.

During each refresh cycle, the ACC 2000 drives the current refresh address onto the AT address bus. This provides the refresh address for extended memory. The refresh pulse for extended memory is from the ACC 2120 /MR288 signal.

Reset and Shutdown Logic

The reset and shutdown logic contains the circuitry for the RESET and /READY signals. Reset circuitry generates two resets. One is the general system reset with power on and the other is for the CPU, or for taking the 80286 out of protected mode when a warm software reset request is generated by the 8042 keyboard controller.

The PWRGD signal generates a system RESET and is synchronized to CLK286. When the KBRST signal is generated from the 8042 keyboard controller (called a warm reset), RST286 is activated to reset the CPU. RST286 is asserted for at least sixteen CLK286 cycles and then deactivated for proper CPU operation. Special circuitry synchronizes the /READY signal to the CPU.

Rating Specifications

Absolute Maximum Ratings *

Parameter	Symbol	Condition	Min	Max	Unit
Power supply voltage	VCC	Ta=25 C	-0.3	7.0	V
Input voltage	VI	VSS=0	-0.3	VCC+0.3	V
Output voltage	VO		-0.3	VCC+0.3	V
Operating temperature	Top		0	70	C
Storage temp	Tstg		-40	125	C

* Exposing the device to stress above these limits can cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Capacitance Limits

TA = +25o C, VCC = 5V

Parameter	Symbol	Min	Max	Unit	Test Condition
Input capacitance	CI		10	pF	fc = 1 MHz unmeasured pins at GND
I/O capacitance	CIO		15	pF	

DC Specifications

TA = 0°C to 70°C, VCC = +5V +/- 5%

Group 1 INPUT

/0WS, /MASTER, /MCS16, /IOCS16, /XDEN, /BSY287, PWR/MX, OSC14M, IORDY, 16MHZ, 32MHZ, /CDINT, GATEA20, KBRST, /DMEN1, /DMEN2, /REFRESH, NPCS, A0-19, A21-23, HLDA, /BHE, M/-IO

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V +/- 0.25 V
Input High voltage	VIH	2.0	VCC	V	VCC = 5 V +/- 0.25 V
Input low current	IIL	-10	10	uA	VIN = VSS
Input high current	IIH	-10	10	uA	VIN =VCC

HCHF, PWR/GD, KBLRST

Parameter	Symbol	Min	Max	Unit	Test Condition
Schmitt trigger Input low voltage	VIL	VSS	1.0	V	VCC = 5 V +/- 0.25 V
Schmitt trigger Input High voltage	VIH	4.0	VCC	V	VCC = 5 V +/- 0.25 V
Input low current	IIL	-10	10	uA	VIN = VSS
Input high voltage	IIH	-10	10	uA	VIN = VCC

Group 2 OUTPUT

/ENROM, XDDIR, /BSY286, /MDLAT, /RESET, /ENAS, /ERROR, IRQ13,
L374, CSPCK, /ENLBY1, /ENLBY2, /ENHBY, DT/-R, MDT/-R, /D245, /G245, RST286, TURBO

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 6.0 mA
Output high voltage	VOH	2.4		V	IOH = -4.0 mA

/INTA

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 6.0 mA
Output high voltage	VOH	2.4		V	IOH = -4.0 mA
Tristate leakage current	IOZ	-10	10.0	uA	VOUT = VCC or VSS

/LMEMW, MA0-10, /RAS0-7, /CAS0L-3L, /CAS0H-3H, CLK8042, CLUART,
/READY

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 12.0 mA
Output high voltage	VOH	2.4		V	IOH = -8.0 mA

/SMEMW, /SMEMR

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 24.0 mA
Output High voltage	VOH	2.4		V	IOH = -16.0 mA
Tristate leakage current	IOZ	-10.0	10.0	uA	VOUT = VCC or VSS

CLK286, PCLK, ALE

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 24.0 mA
Output High voltage	VOH	2.4		V	IOH = -16.0 mA

Group 3 INPUT/OUTPUT

A20, /S0, /S1, D0, D1, D2, D3, D4

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V +/- 0.25 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 V +/- 0.25 V
Input low current	IIL	-10	10	uA	VIN = VSS
Input high current	IIH	-10	10	uA	VIN = VSS
Output low voltage	VOL		0.4	V	IOL = 12.0 mA
Output high voltage	VOH	2.4		V	IOH = -8.0 mA

/SBHE, LA20

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V +/- 0.25 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 V +/- 0.25 V
Input low current	IIL	-10	10	uA	VIN = VSS
Input high current	IIH	-10	10	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 24.0 mA
Output high voltage	VOH	2.4		V	IOH = -16.0 mA

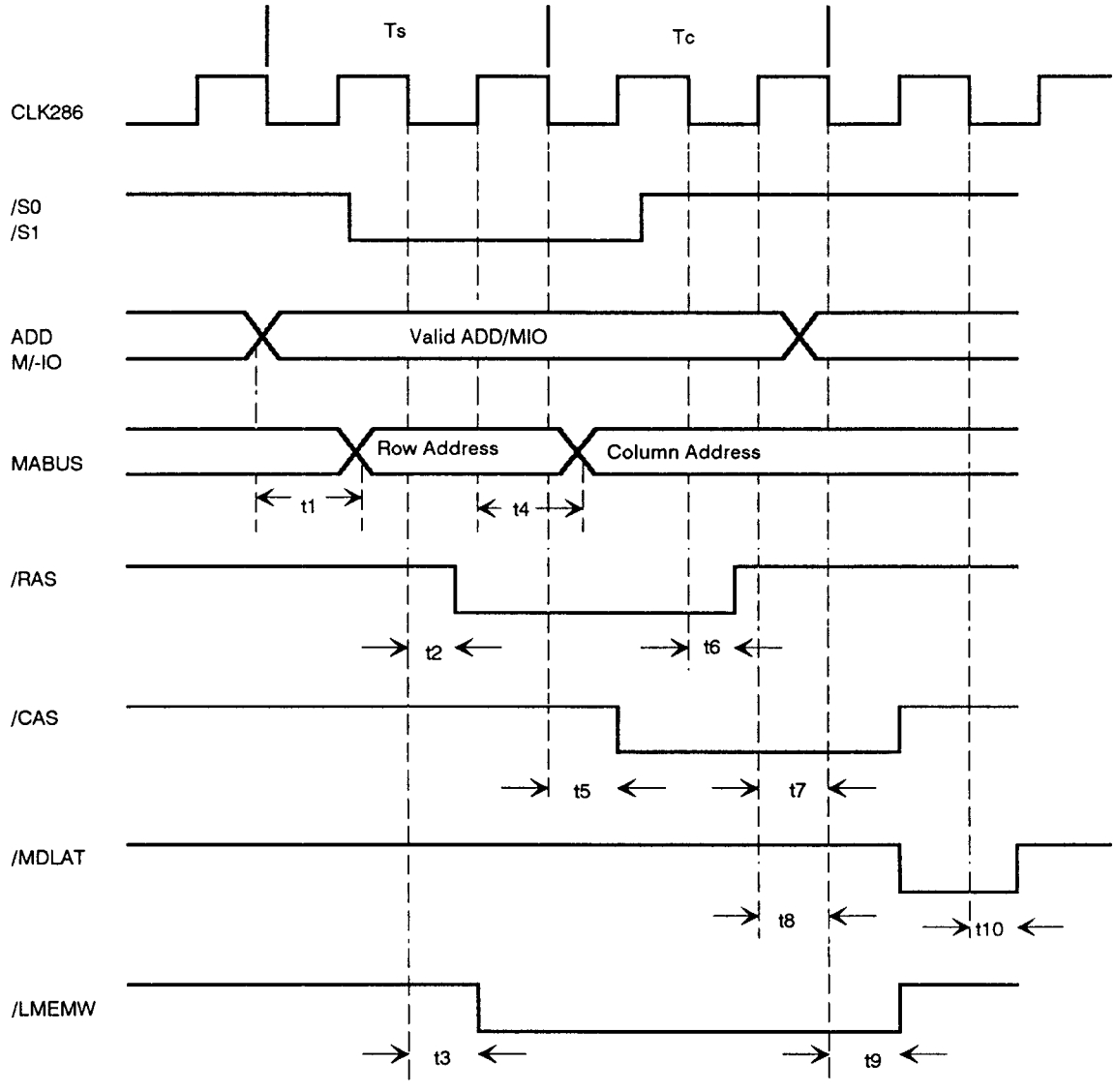
SA0, /MEMR, /MEMW, /IOR, /IOW

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 V +/- 0.25 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 V +/- 0.25 V
Input low current	IIL	-10	10	uA	VIN = VSS
Input high current	IIH	-10	10	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 24.0 mA
Output high voltage	VOH	2.4		V	IOH = -16.0 mA
Tristate leakage current	IOZ	-10.0	10.0	uA	VOUT = VCC or VSS

AC Specifications

Symbol	Description	Min	Max	Units
t1	Row address stable from address	14.5	30.7	ns
t2	/RAS active delay from CLK286 falling edge	6.3	28.6	ns
t3	/LEMW active delay from CLK286 falling edge	5.1	20.2	ns
t4	Column address stable from CLKJ286 rising edge	6.8	26.0	ns
t5	/CAS active delay from CLK286 falling edge	4.6	17.9	ns
t6	/RAS inactive delay from CLK286 falling edge	8.0	30.9	ns
t7	/CAS inactive delay from CLK286 rising edge	6.6	25.4	ns
t8	/MDLAT active delay from CLK286 rising edge	3.5	14.4	ns
t9	/LMEMW inactive delay from CLK286 falling edge	6.1	24.2	ns
t10	/MDLAT inactive delay from CLK286 rising edge	3.3	13.0	ns

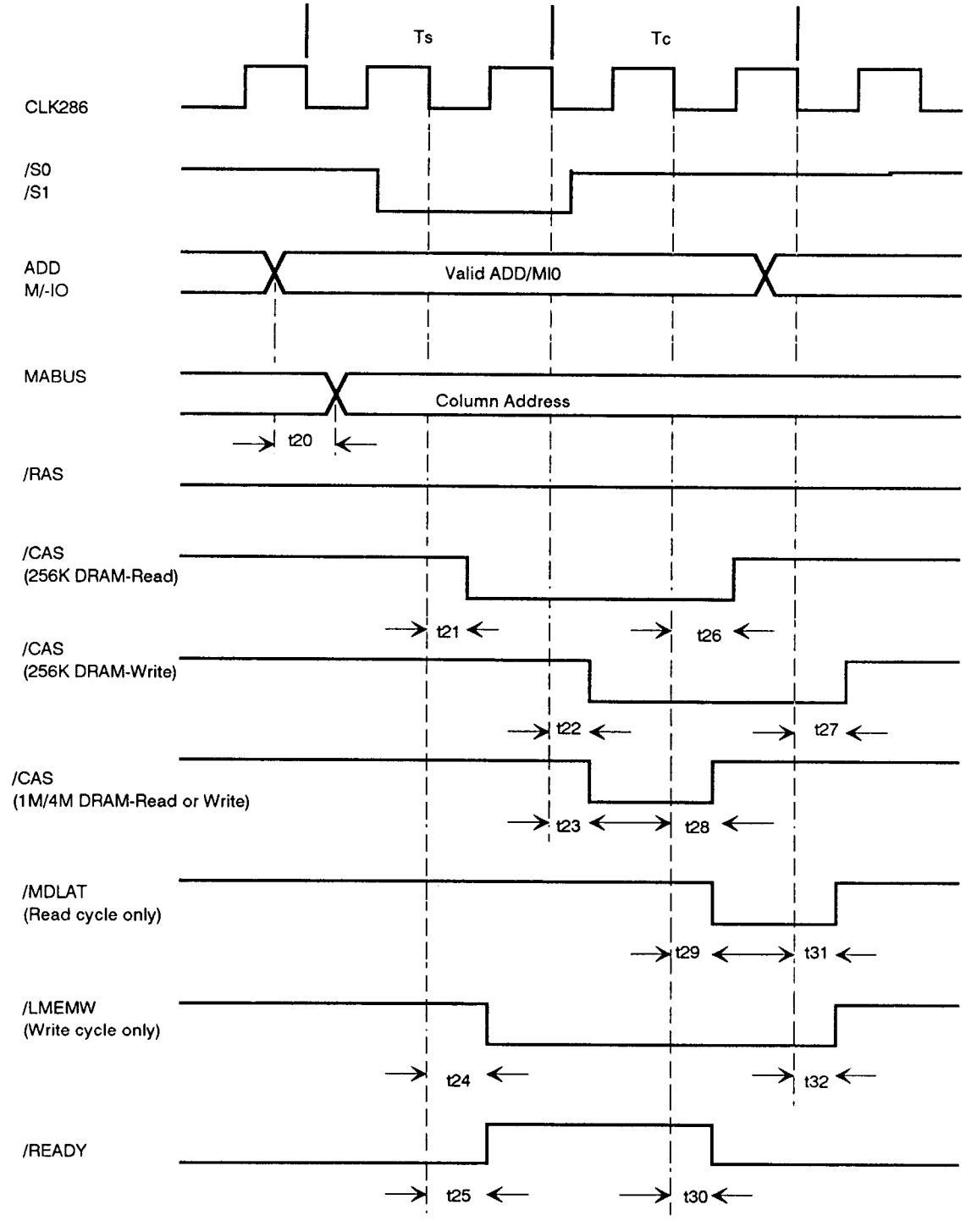
Direct Access Memory Control Timing



AC Specifications

Symbol	Description	Min	Max	Units
t20	Column address stable from valid address	14.5	21.6	ns
/CAS active delay from CLK286 falling edge				
t21	In case of 256K DRAM read cycle	4.6	20.5	ns
t22	In case of 256 DRAM write cycle	4.6	17.9	ns
t23	In case of 1M/4M DRAM	4.6	17.9	ns
t24	/LMEMW active delay from CLK286 falling edge	5.1	20.2	ns
t25	/READY inactive delay from CLK286 falling edge	2.2	17.1	ns
/CAS inactive delay from CLK286 falling edge				
t26	In case of 256K DRAM read cycle	6.6	25.4	ns
t27	In case of 256K DRAM read cycle	6.6	25.4	ns
t28	In case of 1M/4M DRAM	6.6	25.4	ns
t29	/MDLAT active delay from CLK286 falling edge	3.5	14.3	ns
t30	/READY active delay from CLK286 falling edge	3.6	15.2	ns
t31	/MDLAT inactive delay from CLK286 falling edge	3.3	13.0	ns
t32	/LMEMW inactive delay from CLK286 falling edge	6.1	24.2	ns

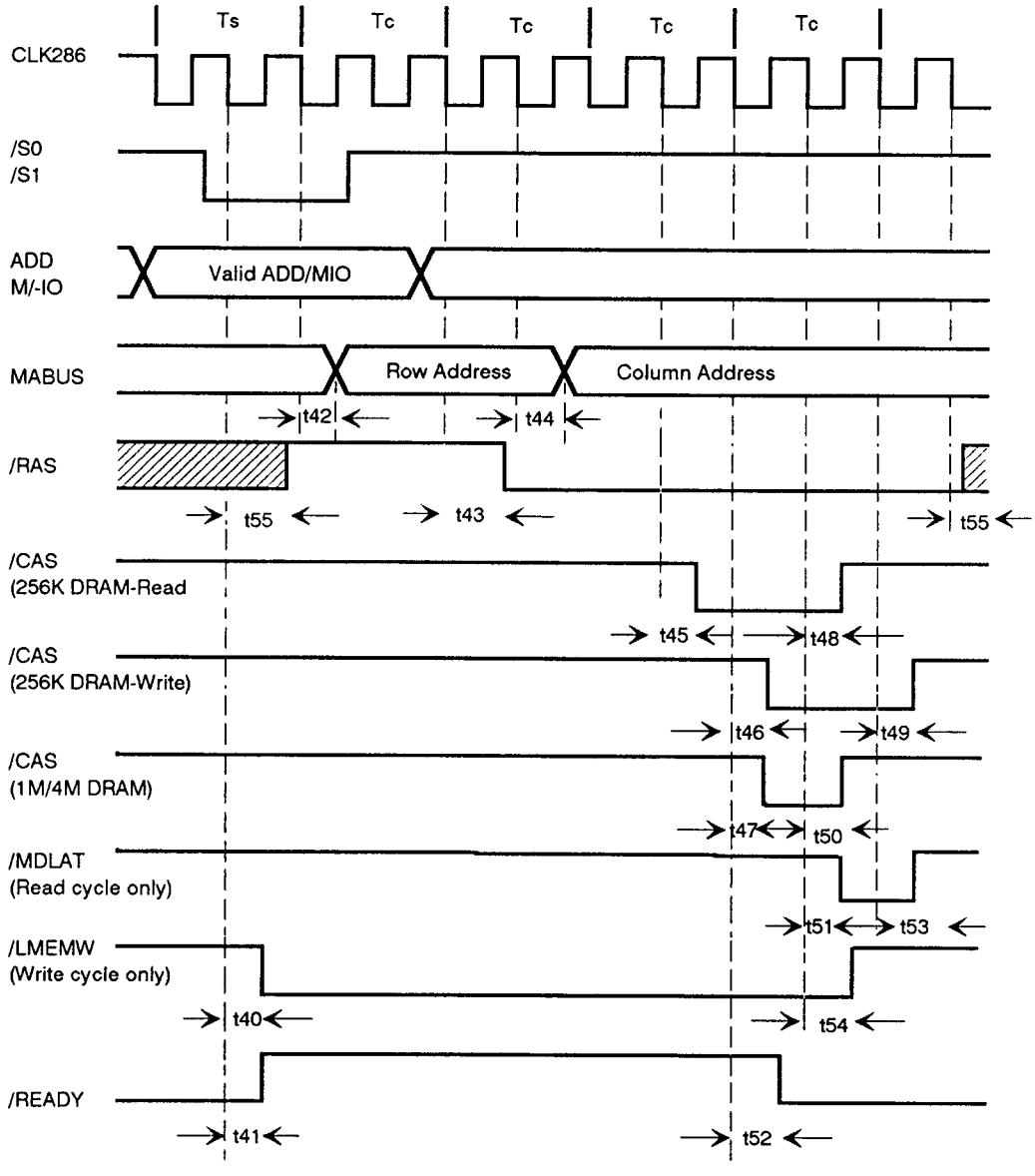
Page Interleaved Memory Control Timing
Page Hit Cycle



AC Specifications

Symbol	Description	Min	Max	Unit
t40	/LMEMW active delay from CLK286 falling edge	5.1	20.2	ns
t41	READY inactive delay from CLK286 falling edge	4.2	17.1	ns
t42	Row address stable from CLK286 falling edge	5.8	23.1	ns
t43	RAS active delay from CLK286 falling edge	22.1	41.7	ns
t44	Column address stable from CLK286 falling edge	21.5	38.6	ns
/CAS active delay from CLK286 falling edge				
t45	256K DRAM - read cycle	4.6	17.9	ns
t46	256K DRAM - write cycle	4.6	17.9	ns
t47	1M/4M DRAM /CAS inactive delay from CLK286 falling edge	4.6	17.9	ns
t48	256K DRAM - read cycle	6.6	25.4	ns
t49	256K DRAM - write cycle	6.6	25.4	ns
t50	1M/4M DRAM	6.6	25.4	ns
t51	/MDLAT active delay from CLK286 falling edge	3.5	14.3	ns
t52	/READY active delay from CLK286 falling edge	21.4	39.1	ns
t53	/MDLAT inactive delay from CLK286	3.3	13.0	ns
t54	/LMEMW inactive delay from CLK286	20.6	35.3	ns
t55	/RAS inactive delay from CLK286	9.4	36.5	ns

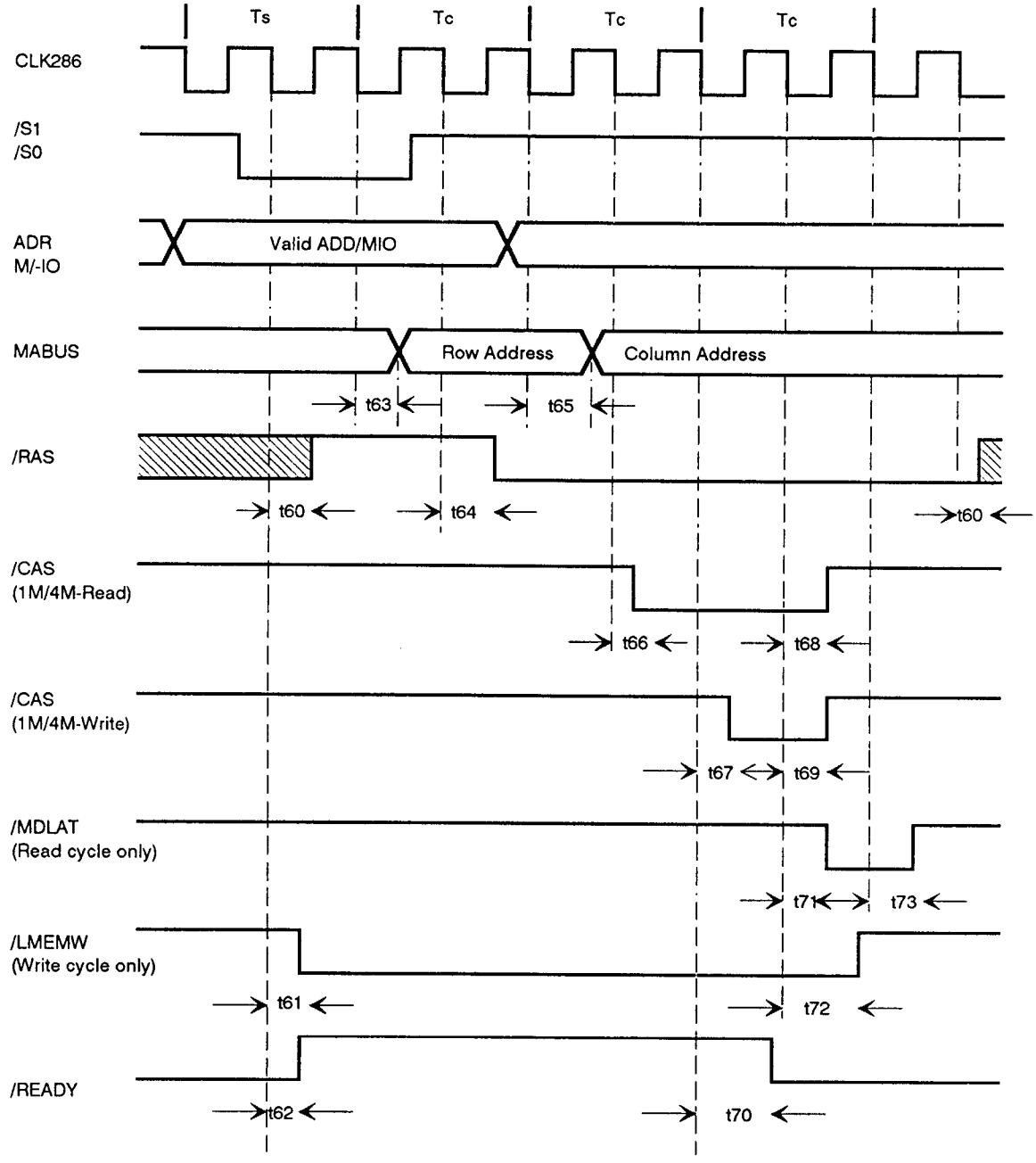
Page Interleaved Memory Control Timing
Page Miss Cycle



AC Specifications

Symbol	Description	Min	Max	Unit
t60	/RAS inactive delay from CLK286 falling edge	7.8	30.3	ns
t61	/LMEMW active delay from CLK286 falling edge	5.1	20.2	ns
t62	/READY inactive delay from CLK286 falling edge	4.2	17.1	ns
t63	Row address stable from CLK286 falling edge	5.8	22.1	ns
t64	/RAS active delay from CLK286 falling edge	22.1	41.7	ns
t65	Column address stable from CLK286 falling edge	21.2	38.6	ns
/CAS active delay from CLK286 falling edge				
t66	In case of 1M/4M read cycle	4.6	17.9	ns
t67	In case of 1M/4M write cycle	4.6	17.9	ns
/CAS inactive delay from CLK286 falling edge				
t68	In case of 1M/4M read cycle	6.6	25.4	ns
t69	In case of 1M/4M write cycle	6.6	25.4	ns
t70	/READY active delay from CLK286	21.4	39.1	ns
t71	/MDLAT active delay from CLK286	3.5	14.3	ns
t72	/LMEMW inactive delay from CLK286	19.6	35.3	ns
t73	/MDLAT inactive delay from CLK286	3.3	13.0	ns

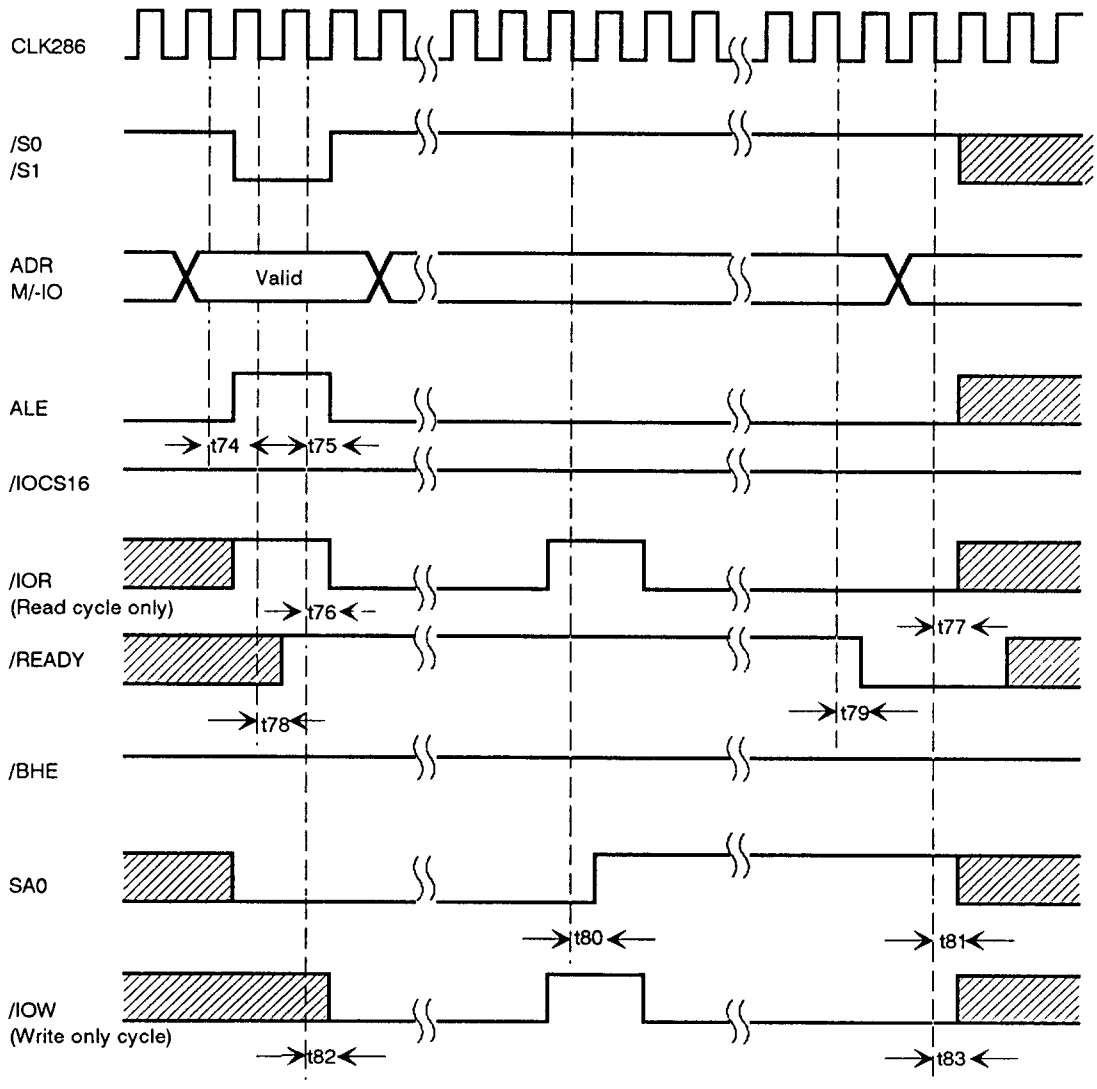
Turbo Page Interleaved Memory Control Timing
Page Miss Cycle



AC Specifications

Symbol	Description	Min	Max	Unit
t74	ALE active delay from CLK286 falling	5.2	13.8	ns
t75	ALE inactive delay from CLK286 falling	5.3	14.6	ns
t76	/IOR active delay from CLK286 falling	7.2	28.2	ns
t77	/IOR inactive delay from CLK286 falling	4.9	19.5	ns
t78	/READY inactive delay from CLK286 falling	3.9	16.3	ns
t79	/READY active delay from CLK286 falling	3.4	14.2	ns
t80	SA0 rising from CLK286 falling	7.2	28.6	ns
t81	SA0 falling from CLK286 falling	8.5	31.1	ns
t82	/IOW active delay from CLK286 falling	5.8	23.1	ns
t83	/IOW inactive delay from CLK286 falling	6.6	25.2	ns

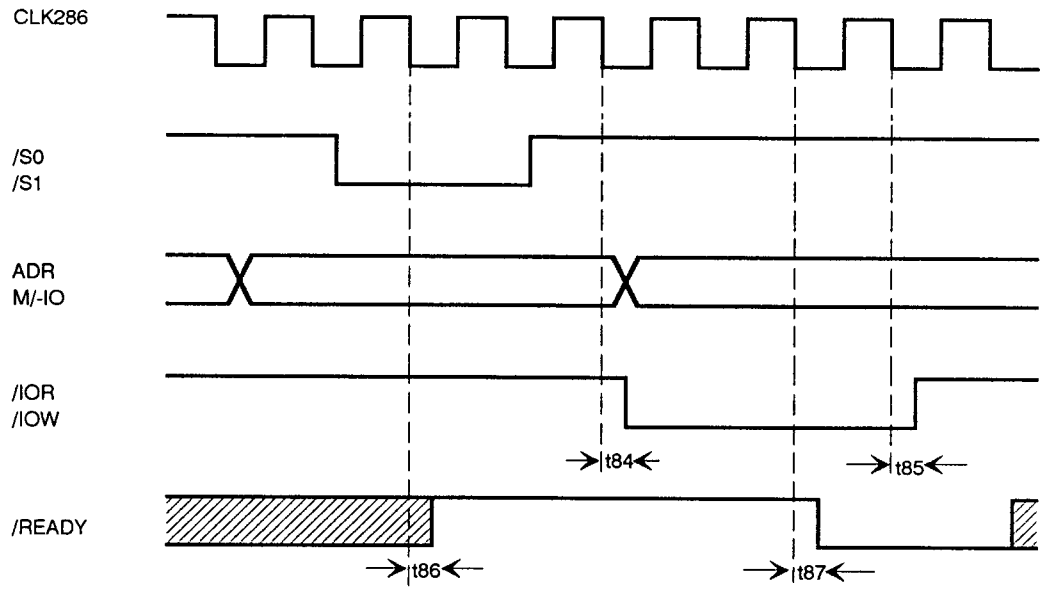
BUS Conversion



AC Specifications

Symbol	Description	Min	Max	Unit
t84	/IOR, /IOW active delay from CLK286 falling	5.8	23.1	ns
t85	/IOR, /IOW inactive delay from CLK286 falling	4.9	19.5	ns
t86	/READY inactive delay from CLK286 falling	3.4	14.2	ns
t87	/READY active delay from CLK286 falling	3.9	16.3	ns

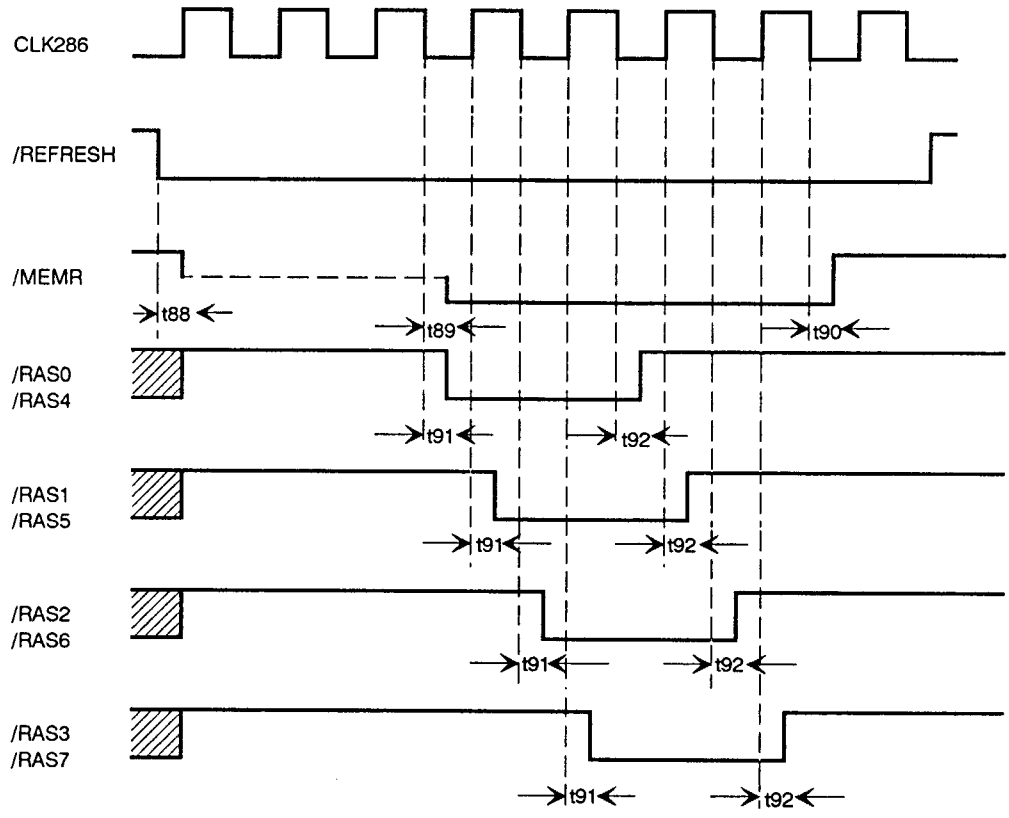
I/O Read/Write



AC Specifications

Symbol	Description	Min	Max	Unit
t88	/MEMR tri-state delay from /REFRESH falling	5.4	21.9	ns
t89	/MEMR active delay from CLK286 falling	7.0	28.3	ns
t90	/MEMR inactive delay from CLK286 falling	6.6	27.8	ns
t91	/RAS active delay from CLK286 falling or CLK286 rising	8.7	34.6	ns
t92	/RAS inactive delay from CLK286 falling or CLK286 rising	7.4	30.0	ns

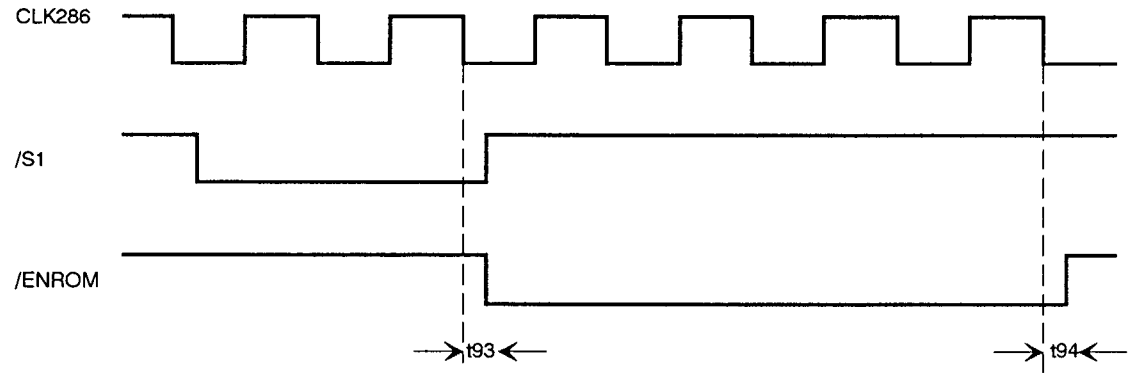
REFRESH


CLK286
/REFRESH
/MEMR
t88
t89
t90
/RAS0
/RAS4
t91
t92
/RAS1
/RAS5
t91
t92
/RAS2
/RAS6
t91
t92
/RAS3
/RAS7
t91
t92

AC Specifications

Symbol	Description	Min	Max	Unit
t93	/ENROM active delay from CLK286 falling	5.6	22.8	ns
t94	/ENROM inactive delay from CLK286 falling	5.2	21.3	ns

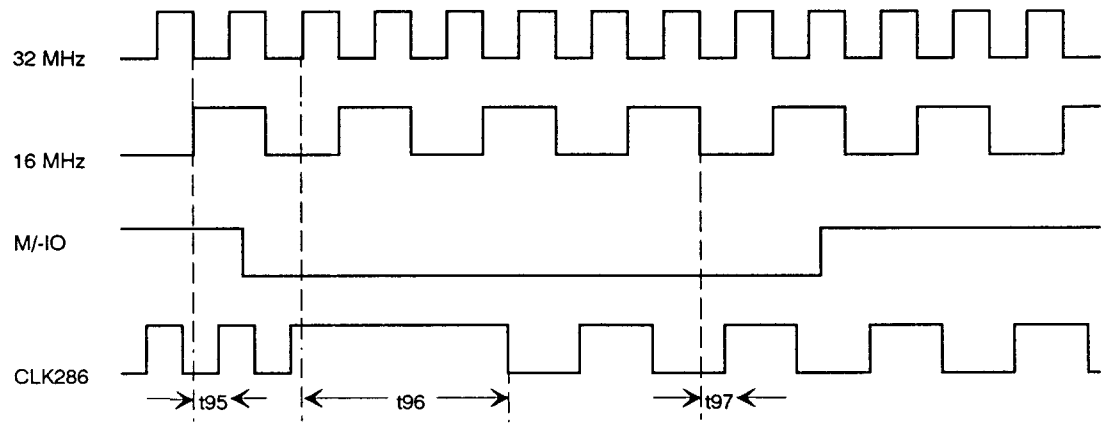
ROM Cycle
1WS



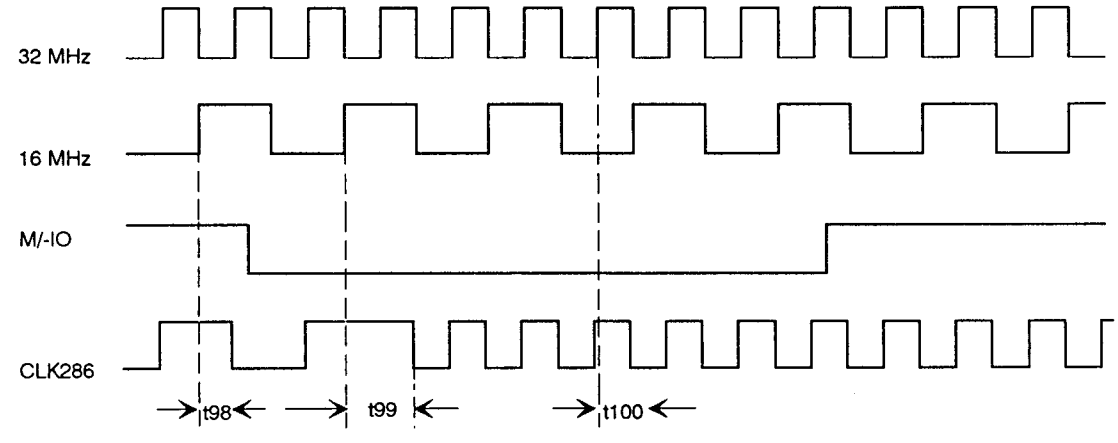
AC Specifications

Symbol	Description	Min	Max	Unit
t95	CLK286 rising delay from 32 MHz falling	3.1	12.6	ns
t96	CLK286 falling switching delay from 32 MHz rising	34.1	89.6	ns
t97	CLK286 rising delay from 16 MHz falling	3.2	12.1	ns
t98	CLK286 falling delay from 16 MHz rising	3.1	12.1	ns
t99	CLK286 falling switching delay from 16 MHz rising	3.1	29.4	ns
t100	CLK286 falling delay from 32 MHz rising	3.1	11.9	ns

Clock Switching from High to Low



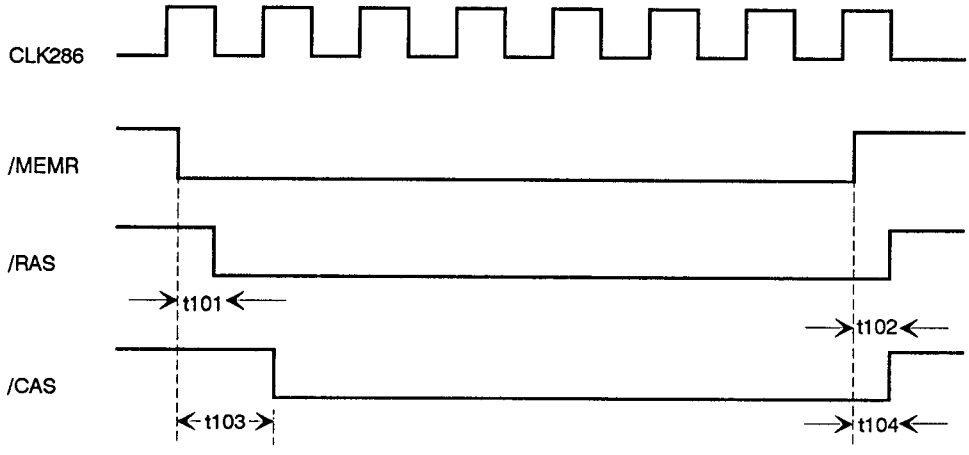
Clock Switching from Low to High



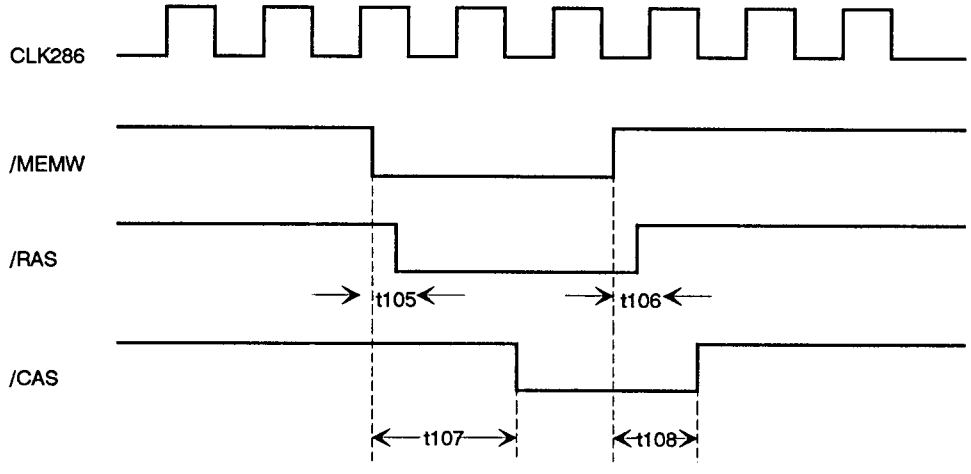
AC Specifications

Symbol	Description	Min	Max	Unit
DMA Memory Read				
t101	/RAS active delay from /MEMR falling	6.4	25.7	ns
t102	/RAS inactive delay from /MEMR rising	6.3	24.1	ns
t103	/CAS active delay from /MEMR falling	90.2	108.4	ns
t104	/CAS inactive delay from /MEMR rising	6.4	24.5	ns
DMA Memory Write				
t105	/RAS active delay from /MEMW falling	6.4	25.9	ns
t106	/RAS inactive delay from /MEMW rising	6.4	24.4	ns
t107	/CAS active delay from /MEMW falling	89.9	107.4	ns
t108	/CAS inactive delay from /MEMW rising	28.9	48.8	ns

DMA
Memory Read



DMA
Memory Write



ACC 2220
PC/AT Integrated Data & Address Buffer

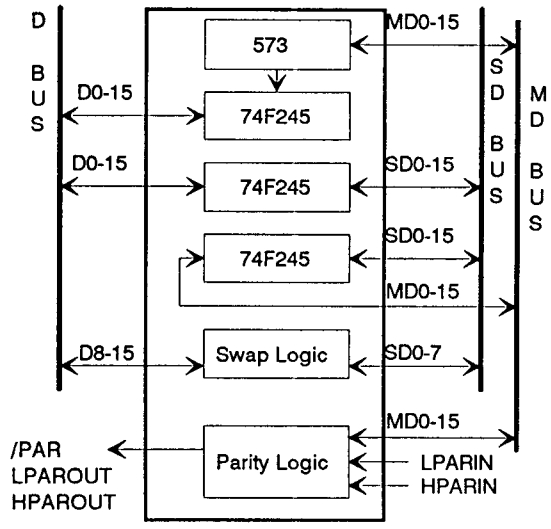
The ACC 2220 is a high performance buffer chip, running in two different modes. It activates data buffers and latches mode when pin 25 is asserted low and address buffers and latches mode when asserted high.

Features

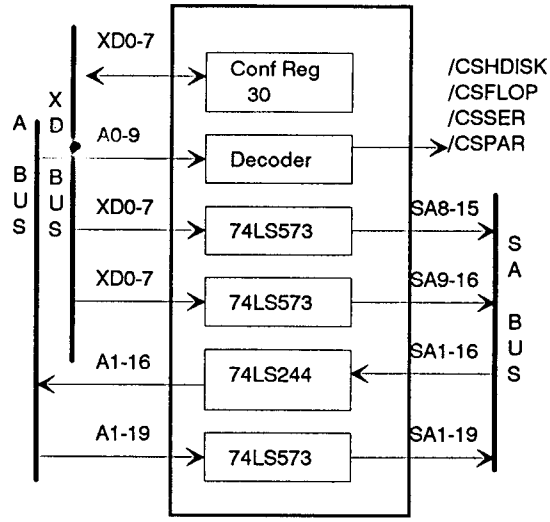
- 100% hardware and software compatible to an IBM PC/AT*
- Data buffers and latches
- Address buffers and latches
- Built-in parity generation/detection logic
- Built-in bus conversion logic for 16-bit to 8-bit transfers
- Generates chip select for hard disk, floppy disk, serial and parallel ports
- Supports direct high drive for expansion slots
- 1.5 micron high performance CMOS technology
- TTL compatible
- 84-L PLCC package

*Trademarks of International Business Machines

Block Diagram



Data Mode



Address Mode

ACC Microelectronics Corporation · 3295 Scott Blvd. · Santa Clara, CA 95054
Phone: 408-980-0622 FAX: 408-980-0626

Pin Diagram

Pin Diagram

ACC 2220 Pin Descriptions (Data Mode)

Symbol	Pin	I/O	Pin Description
SD0	36	I/O	System data bus bit.
SD1	50		
SD2	51		
SD3	75		
SD4	76		
SD5	83		
SD6	84		
SD7	2		
SD8	3		
SD9	10		
SD10	11		
SD11	14		
SD12	15		
SD13	29		
SD14	30		
SD15	34		
MD0	61	I/O	Memory data bus bit.
MD1	62		
MD2	63		
MD3	64		
MD4	65		
MD5	66		
MD6	67		
MD7	28		
MD8	37		
MD9	48		
MD10	58		
MD11	70		
MD12	77		
MD13	82		
MD14	4		
MD15	9		

ACC 2220 Pin Descriptions (Data Mode)

Symbol	Pin	I/O	Pin Description
D0	68	I/O	CPU data bus bit.
D1	69		
D2	78		
D3	79		
D4	80		
D5	81		
D6	5		
D7	6		
D8	7		
D9	8		
D10	19		
D11	20		
D12	21		
D13	22		
D14	23		
D15	24		
LPAROUT	16	O	Low parity bit output.
HPAROUT	17	O	High parity bit output.
A20	18	O	CPU address bus bit.
MODEA/D	25	I	Address (high) / Data mode select (low).
SA0	26	I	System address bus Bit 0.
/SBHE	27	I	System bus high enable. Active low.
/ENLBY1	35	I	System data bus to local data bus low byte output enable (active low). Used for 8-bit I/O port or extension memory read.
HLDA	39	I	Hold acknowledge.
DSMSD	40	I	Memory data / System data bus disable.

ACC 2220 Pin Descriptions (Data Mode)

Symbol	Pin	I/O	Pin Description
PAR	41	O	Memory parity error.
/MASTER	42	I	External master. Active low.
CSPCK	43	I	Parity check enable.
GA20	44	I	Protect mode A20 select. Active high.
A20286	45	I	80286 address bus Bit 20.
/MEMR	46	I	Memory read. Active low.
/ENHBY	47	I	System /Local data bus (CSPCK=0) or Memroy/Local data bus (CSPCK=1) high byte transfer enable. Active low.
ACK	49	O	Bus hold acknowledge. Active high.
/ENLBY2	52	I	System/Local data bus (CSPCK=0) or Memory/Local data bus (CSPCK=1) low byte transfer enable. Active low.
LPARIN	53	I	Low parity bit input.
HPARIN	56	I	High parity bit input.
L374	57	I	Clock input for the system data bus to local data bus low byte latch.
/D245	59	I	System data bus byte swap direction high-to-low (high)/ low-to-high (low).
/G245	60	I	System data bus byte swap enable. Active low.
DT/R	71	I	Local data bus to system data bus transmit (high)/ receive (low).

ACC 2220 Pin Descriptions (Data Mode)

Symbol	Pin	I/O	Pin Description
MDT/R	72	I	System data bus to memory data bus transmit (high) / receive (low).
/MDLAT	38	I	Memory data latch enable. Latches memory data so the CAS can terminate sooner.
VCC	12, 32, 54, 74		+5 volt
VSS	1, 13, 31, 33, 55, 73		Ground

ACC 2220 Pin Descriptions (Address Mode)

Symbol	Pin	I/O	Pin Description
SA0	75	I/O	System address bus bit.
SA1	76		
SA2	83		
SA3	84		
SA4	2		
SA5	3		
SA6	10		
SA7	11		
SA8	14		
SA9	15		
SA10	29		
SA11	30		
SA12	34		
SA13	35		
SA14	52		
SA15	53		
SA16	56		
SA17	57		
SA18	71		
SA19	72		
XDENABLE	9	O	Direction control bit between the CPU data bus (D bus) and the peripheral data bus (XD bus).
/CSHDISK	4	O	Selects the hard disk.
/CSFLOP	82	O	Selects the floppy disk.
/CSSER	77	O	Selects the serial port.
/CSPAR	70	O	Selects the parallel port.
MODEA/D	25	I	Address/data buffer mode select.
ADSTB8	26	I	Byte transfer DMA high address strobe.
ADSTB16	27	I	Word transfer DMA high address strobe.

ACC 2220 Pin Descriptions (Address Mode)

Symbol	Pin	I/O	Pin Description
A1	68	I	CPU address bus bit.
A2	69		
A3	78		
A4	79		
A5	80		
A6	81		
A7	5		
A8	6		
A9	7		
A10	8		
A11	19		
A12	20		
A13	21		
A14	22		
A15	23		
A16	24		
A17	36		
A18	50		
A19	51		
XD0	16	I	Peripheral data bus bit.
XD1	17		
XD2	18		
XD3	38		
XD4	39		
XD5	45		
XD6	59		
XD7	60		
/ENAS	40	I	REAL_TIME_CLOCK address strobe enable. Actve low.
RTCAS	41	O	REAL_TIME_CLOCK multiplexed address strobe. The falling edge causes the address to be latched in 146818.
/IOR	42	I	I/O read. Active low.

ACC 2220 Pin Descriptions (Address Mode)

Symbol	Pin	I/O	Pin Description
/IOW	43	I	I/O write. Active low.
/MASTER	44	I	External master. Active low.
RTCR/W	46	O	REAL_TIME_CLOCK read/write.
RTCDS	47	O	REAL_TIME_CLOCK data strobe or read. Identifies the time period when the REAL_TIME_CLOCK and RAM drive the bus with read data.
/KBCS	49	O	Keyboard chip select. Active low.
ALE	63	I	Address latch enable.
HLDA	64	I	Hold acknowledge.
/DAEN2	65	I	Word transfer DMA address output enable.
/DAEN1	66	I	Byte transfer DMA address output enable.
/REFRESH	67	I	Memory refresh.
/SELPIB	62	I	This pin must be tied low in an ACC 82020 system.
RESET	28	I	System reset.
VCC	12, 32 54, 74		+5 volts
VSS	1, 13, 31, 33, 55, 61, 73		Ground
N.C.	37, 48, 58		

Functional Description

Data Mode

When the MODEA/D pin is set to low, the ACC 2220 operates in DATA Mode. In this mode, the ACC 2220 consists of 48 data bus (D BUS, SD BUS, and MD BUS) drivers, each capable of sinking 6 or 12 mA of current, and two parity generators for high byte and low byte memory data. The parity detection logic generates the parity error signal for the system. The bus conversion logic works in conjunction with the ACC 2120 performing 16-bit to 8-bit transfers.

Data Buffers and Latches

The primary function of the Data Buffer is multiplexing the microprocessor data lines (D0 - D15) to the System Data Bus (SD0 - SD15) and the Memory Data Bus (MD0 -MD15). In the ACC 82020, low byte data is latched when the CPU reads from an 8-bit device, and the memory data is latched by the /MDLAT signal.

Bus Conversion Logic

When the 16-bit CPU reads from or writes to an 8-bit device, the ACC 2120 sends control signals /D245 and /G245 to the ACC 2220. The ACC 2220 then performs the bus conversion.

Parity Generation/Detection Logic

The ACC 2220 provides data parity generator/ checker logic. All data on the Memory Data Bus passes through the parity logic. If an error is detected, the /PAR signal is fed back to the ACC 2000 to generate an NMI to the CPU.

Address Mode

When the MODEA/D pin is set to high, the ACC 2220 operates in ADDRESS Mode. The ACC 2220 consists of 39 address Bus (A BUS and SA BUS) drivers, each capable of sinking 6 or 12 mA of current and the logic to provide control signals to the real time clock.

Address Buffers and Latches

The primary function of the Address Buffer is multiplexing the Microprocessor Address Bus (A1 - A19) to the System Address Bus (SA1 - SA19). The System Address Bus (SA0-SA19) is shared by the coprocessor, ROM, the DMA controller in the ACC 2000 and the expansion slots.

In DMA mode, system address bus bits SA1-16 are transferred to the CPU address bus as bits A1-16.

There is one configuration register in the ACC 2220. Address F2 is the index register and F3 is the address register for configuration register 30.

Configuration register 30 has seven bits. The function of each bit is listed below.

Configuration Register 30

Bit	Function
0	System enable
1	Enable floppy disk interface
2	Enable serial port
3	Serial port select
4	Enable parallel port
5	Parallel port select
6	Hard disk enable

Bit 0: When set to 1, this bit allows bits 4, 2, and 1 to enable or disable their respective devices. When set to 0, it disables the diskette drive interface, and the system board serial and parallel ports. Default is 1.

Bit 1: The diskette drive interface is enabled when this bit and bit 0 are set to 1. Default is 1.

Bit 2: The system board serial port is enabled when this bit and bit 0 are set to 1. Default is 1.

Bit 3: When set to 0, this bit configures the system board serial port to address location 03F8 through 03FF hex. When set to 1, it configures the system board serial port to address location 02F8 through 02FF hex. Default is 0.

Bit 4: The system parallel port is enabled when this bit and bit 0 are set to 1. Default is 1.

Bit 5: When set to 0, this bit configures the system board parallel port to address location 0378 through 037F hex. When set to 1, it configures the system board parallel port to address location 0278 through 027F hex. Default is 0.

Bit 6: The hard disk drive interface is enabled when this bit is set to 1 Default is 1.

Bit 7: Reserved

Combining the bits in register 30 with address input from the CPU, the ACC 2220 generates the following chip select signals:

Parallel port
Serial port
Hard disk
Floppy disk

Real Time Clock Control Signals

The ACC 2220 provides data strobe (RTCDS), read/write (RTCR/W) and address strobe (RTCAS) to 146818.

Rating Specifications

Absolute Maximum Ratings*

Parameter	Symbol	Min	Max	Units
Power supply voltage	VCC	-0.3	7.0	V
Input voltage	VI	-0.3	VCC + 0.3	V
Output voltage	VO	-0.3	VCC + 0.3	V
Operating temperature	Top	0	70	°C
Storage temperature	Tstg	-40	125	°C

* Exposing the device to stress above these can cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Capacitance Limits

TA = +25° C, VCC = 5 V

Parameter	Symbol	Min	Max	Unit	Test Condition
Input capacitance	CI		10	pF	fc = 1 MHz unmeasured pins at GND
I/O capacitance	CIO		15	pF	

DC Specifications

TA = 0° C to +70° C, VCC = +5 V +/- 5%

Pins 25-27, 40, 42-44

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 +/- 0.25 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 +/- 0.25 V
Input low current	IIL	-10	10	uA	VIN = VSS
Input high current	IIH	-10	10	uA	VIN = VCC

Pins 5-8, 16-24, 38-39, 45-47, 59-60, 68, 69, 78-81

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 +/- 0.25 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 +/- 0.25 V
Input low current	IIL	-200	-10	uA	VIN = VSS
Input high current	IIH	-10	10	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 6mA
Output high voltage	VOH	2.4		V	IOH = -4mA
Tristate leakage current	IOZ	-200	-10	uA	VOUT = VCC or VSS

Pins 2, 3, 10, 11, 14, 15, 29, 30, 34-36, 50-53, 56, 57, 61-67, 71, 72, 75, 76, 83, 84

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 +/- 0.25 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 +/- 0.25 V
Input low current	IIL	-200	-10	uA	VIN = VSS
Input high current	IIH	-10	10	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 12mA
Output high voltage	VOH	2.4		V	IOH = -8mA
Tristate leakage current	IOZ	-200	-10	uA	VOUT = VCC or VSS

Pin 41

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 6mA
Output high voltage	VOH	2.4		V	IOH = -4mA

Pin 49

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 12mA
Output high voltage	VOH		2.4	V	IOH = -8mA

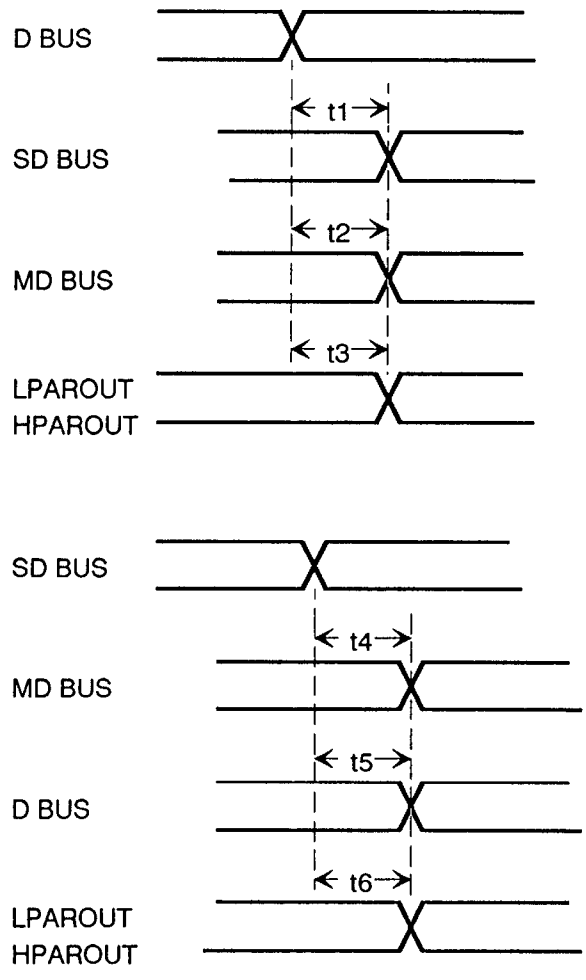
Pins 4, 9, 28, 37, 48, 58, 70, 77, 82

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 +/- 0.25 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 +/- 0.25 V
Input low current	IIL	-10	10	uA	VIN = VSS
Input high current	IIH	-10	10	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 12mA
Output high voltage	VOH	2.4		V	IOH = -8mA
Tristate leakage current	IOZ	-200	-10	uA	VOUT = VCC or VSS

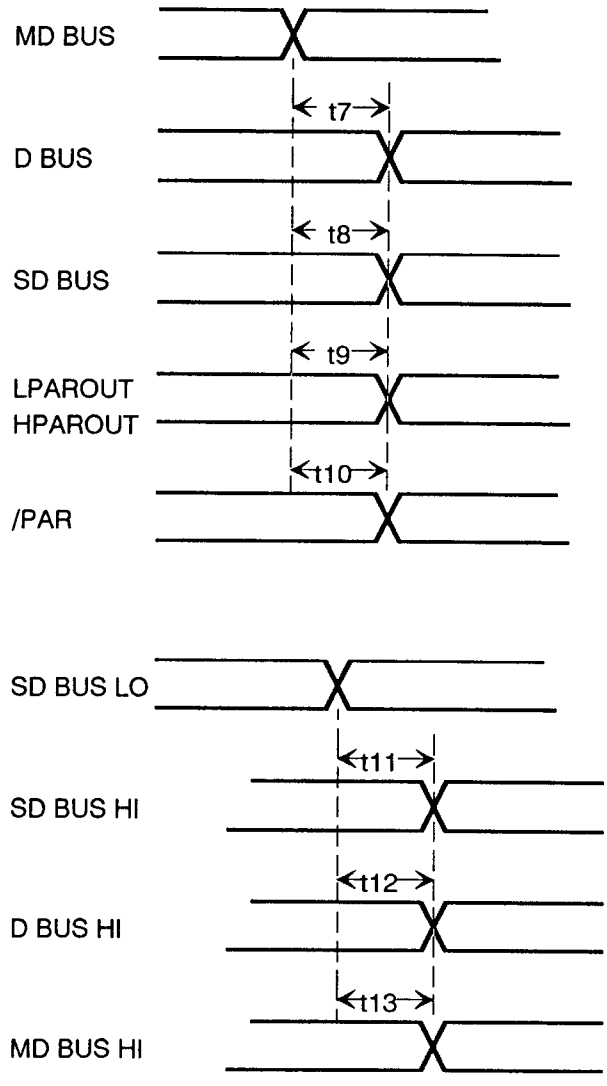
ACC 2220 Data Buffer AC Specifications

Symbol	Description	Min	Typ	Max	Units	Condition
t1	D BUS in to SD BUS out	10	19	36	ns	CL = 200 pF
t2	D BUS in to MD BUS out	5	10	18	ns	CL = 80 pF
t3	D BUS in to LPAROUT or HPAROUT (CPU to memory access)	9	17	31	ns	CL = 80 pF
t4	SD BUS in to MD BUS out	5	10	18	ns	CL = 80 pF
t5	SD BUS in to D BUS out	8	16	30	ns	CL = 80 pF
t6	SD BUS in to LPAROUT or HPAROUT (DMA memory access)	9	17	31	ns	CL = 80 pF
t7	MD BUS in to D BUS out	8	16	30	ns	CL = 80 pF
t8	MD BUS in to SD BUS out	10	20	37	ns	CL = 200 pF
t9	MD BUS in to LPAROUT or HPAROUT	11	22	41	ns	CL = 80 pF
t10	MD BUS in to /PAR	11	22	41	ns	CL = 80 pF
t11	SD BUS low to SD BUS high data out	10	20	38	ns	CL = 200 pF
t12	SD BUS low to D BUS high data out	5	11	20	ns	CL = 80 pF
t13	SD BUS low to MD BUS high data out	7	13	25	ns	CL = 80 pF
t14	LPARIN (or HPARIN) to LPAROUT (or HPAROUT)	10	20	37	ns	CL = 80 pF
t15	A20286 active to GA20 delay	9	18	33	ns	CL = 80 pF
t16	ACK active to HLDA or MASTER	5	10	19	ns	CL = 80 pF

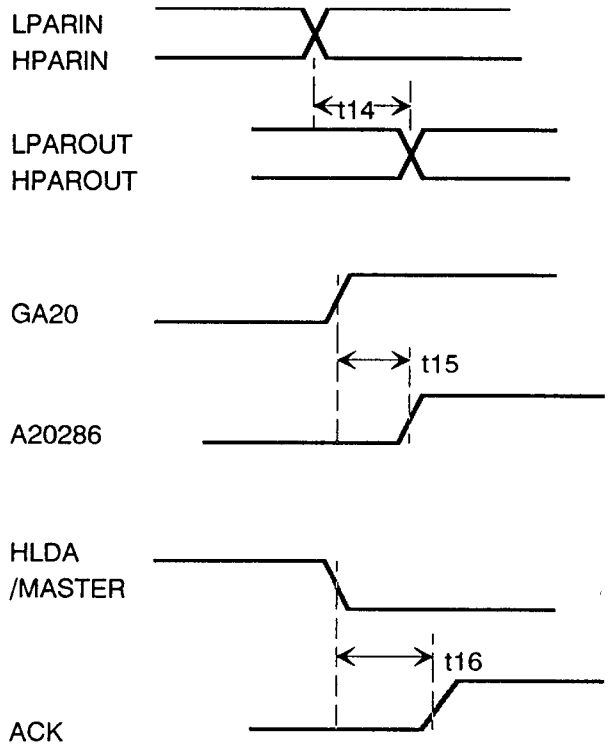
ACC 2220 Data Buffer Timing



ACC 2220 Data Buffer Timing



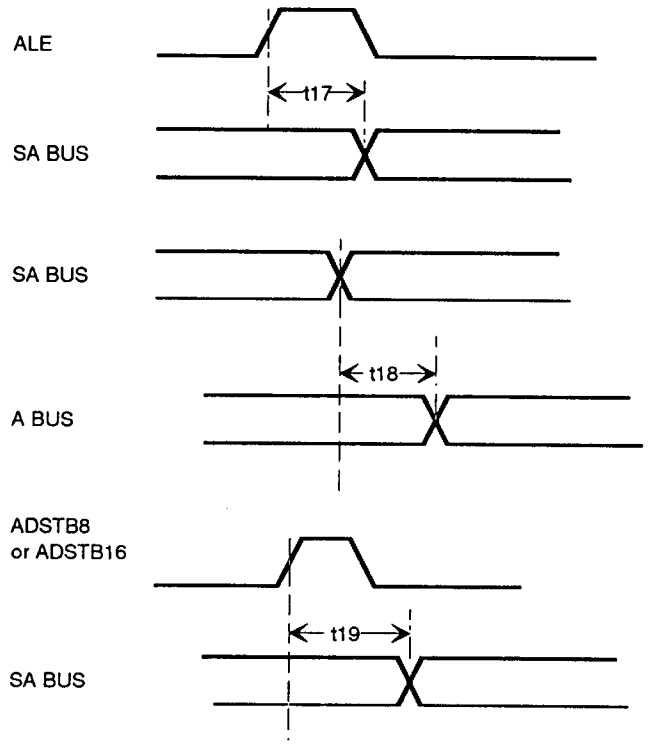
ACC 2220 Data Buffer Timing



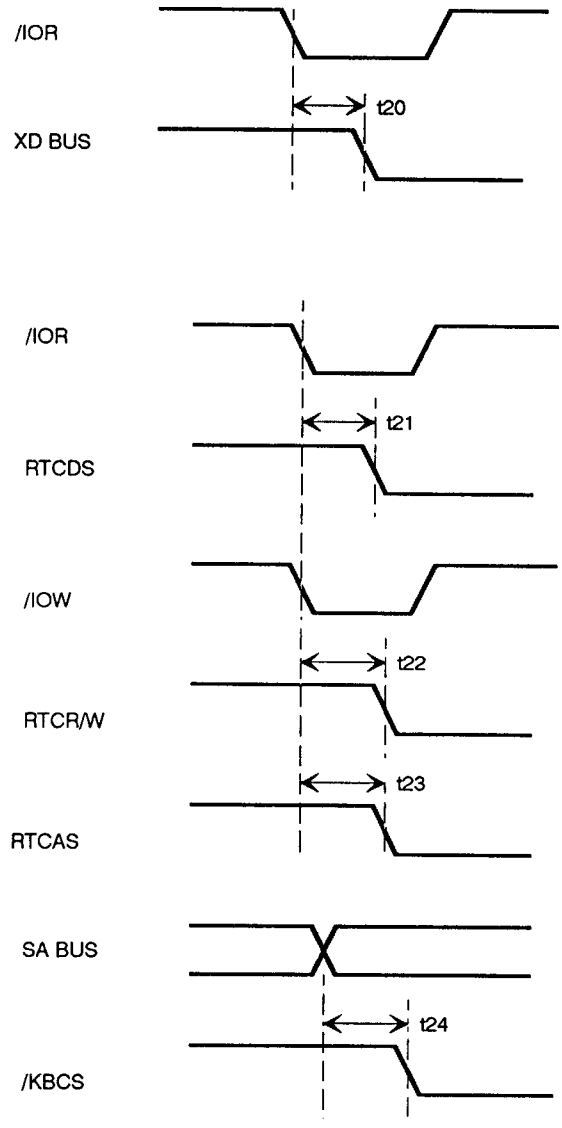
ACC 2220A AC Specifications

Symbol	Description	Min	Typ	Max	Units	Condition
t17	ALE to SA BUS valid address	11	22	40	ns	CL = 200 pF
t18	SA BUS in to A BUS out in master mode	9	17	31	ns	CL = 80 pF
t19	ADSTB8 (or ADSTRB16) to SA BUS valid address	11	21	39	ns	CL = 200 pF
t20	/IOR to XDOUT (Read config Reg 0F3H)	12	23	43	ns	CL = 80 pF
t21	/IOR to RTCDS	8	15	28	ns	CL = 80 pF
t22	/IOW to RTCR/W	8	15	28	ns	CL = 80 pF
t23	/IOW to RTCAS	5	10	18	ns	CL = 80 pF
t24	SA BUS valid address to /KBCS	7	14	26	ns	CL = 80 pF
t25	CPU address valid to chip select output (/CSFLOP, /CSSER, /CSPAR, /CSHDISK) and XDENABLE	9	17	31	ns	CL = 80 pF

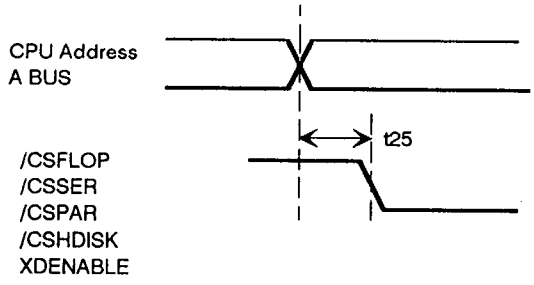
ACC 2220 Address Buffer Timing



ACC 2220 Address Buffer Timing



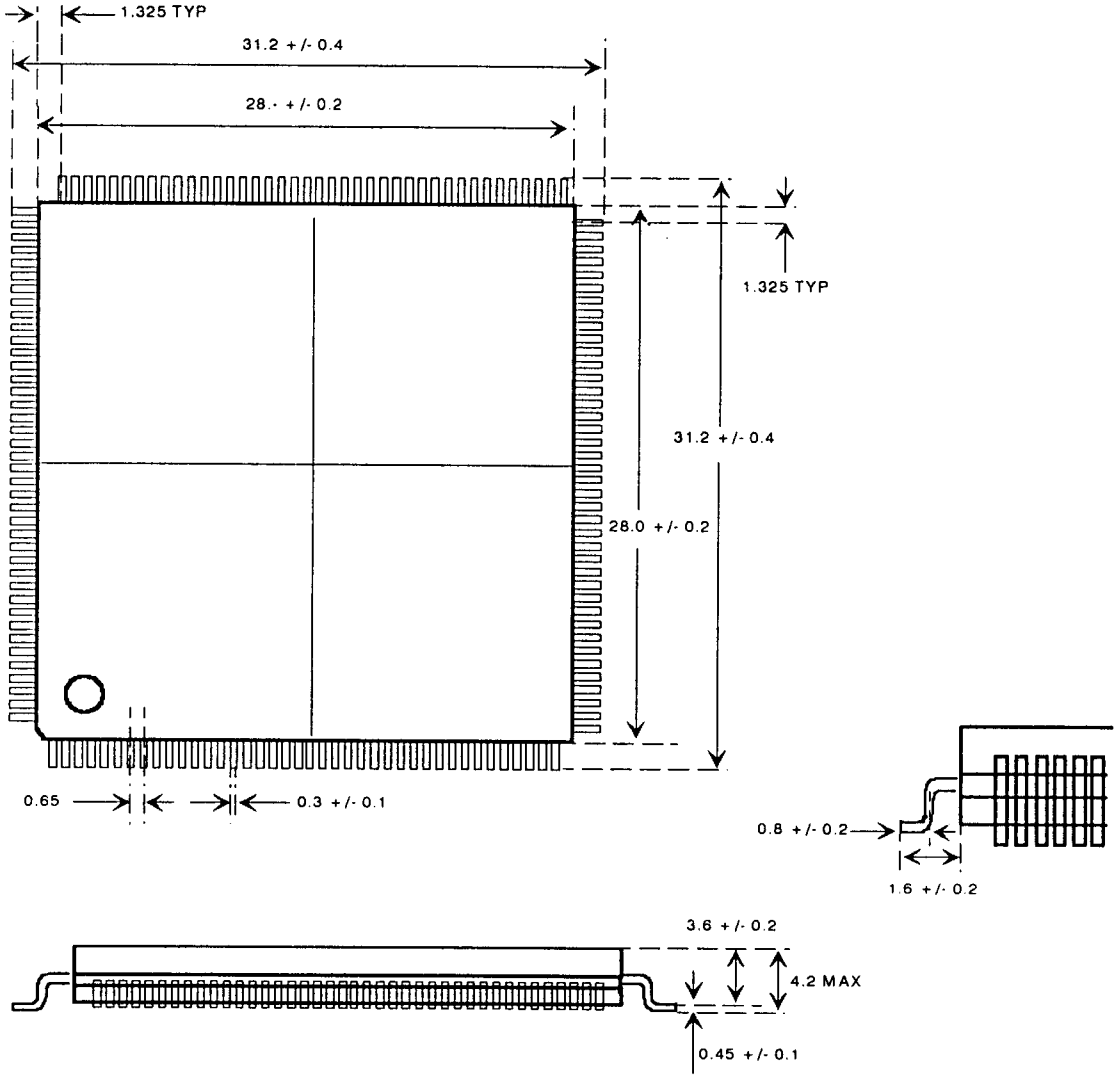
ACC 2220 Address Buffer Timing



Production Package Specification

Package: 160 Pin PFP
Unit: (mm)

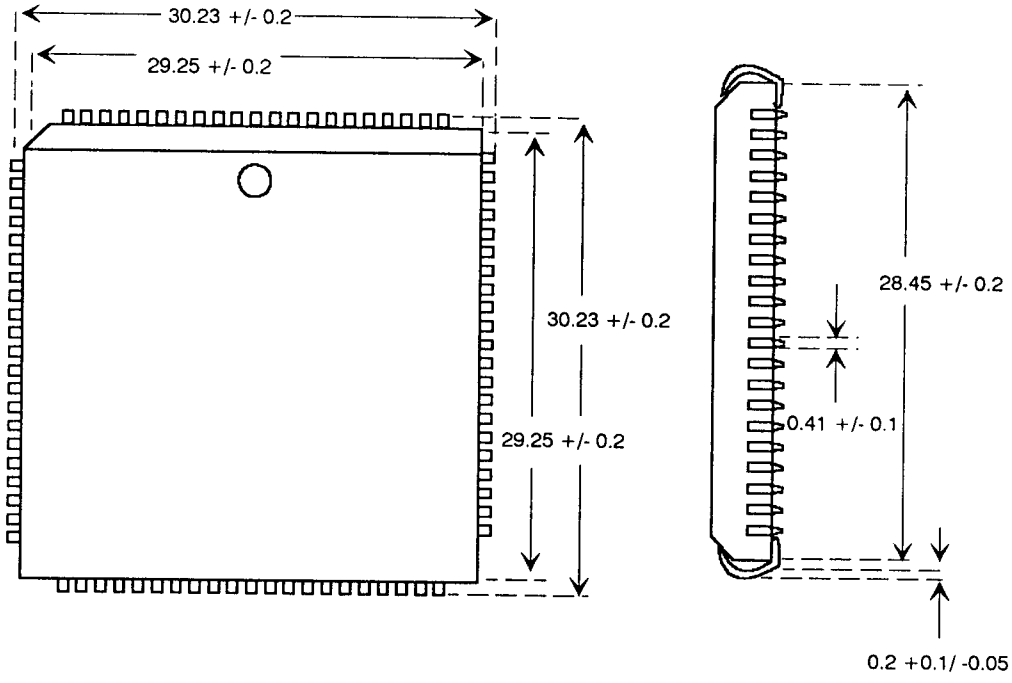
Chips: ACC 2120

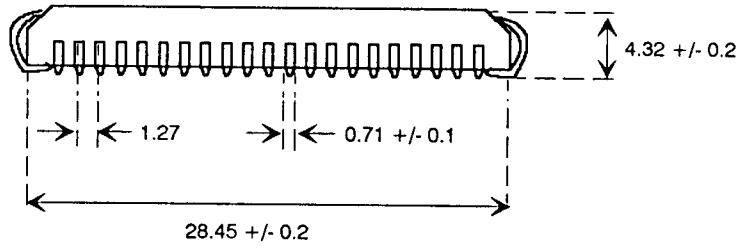


Production Package Specification

Package: 84 Pin PLCC
Unit: (mm)

Chips: ACC 2000
ACC 2220





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