ACC 82010 AT Chip Set

- 100% hardware and software compatible with the IBM PC/AT*
- Fully compatible with

  Intel 8237 DMA controller
  Intel 8259 interrupt controller
  Intel 8254 timer/counter
  Intel 82284 clock generator
  Intel 82288 bus controller
  TI 74LS612 memory mapper

- Functions include

  7 DMA channels
  3 timer/counter channels
  14 external interrupt channels
  Data Buffers
  Address Buffers

- Built in Refresh Control circuit
- Supports up to 12.5 MHz system clock with zero wait state capability
- I/O (8 MHz) AT BUS compatible
- Supports 16 MB DMA address space
- Built-in memory address decoder to support 1MB or 640KB
- Wait state generation
- 1.5 micron high performance CMOS technology
- TTL compatible
- Standard 84-L PLCC package

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The PC/AT chip set includes the following four chips:

ACC 2000	Multifunctional Peripheral Controller
ACC 2100	System Bus Controller
ACC 2220	Data Buffers or Address Buffers

General Description

The ACC 82010 is an integrated high performance CMOS chip set that replaces most of the MSI/SSI The ACC 82010 is an integrated high performance CMOS chip set that replaces most of the MSI/SSI logic used to build IBM PC/AT compatible systems.

The first chip, the ACC 2000, is a peripheral controller that performs the functions of two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, and one 74LS612 memory mapper as well as other standard control logic circuitry.

The second chip, the ACC 2100, is a system controller containing one 82284 clock generator, one 82288 bus controller, and a high performance memory controller providing 12.5 MHz or 16 MHz operation as well as the standard AT mode with zero and one wait state schemes.

The ACC 2220 is a buffer/latch chip that runs in two modes: data mode and address mode.

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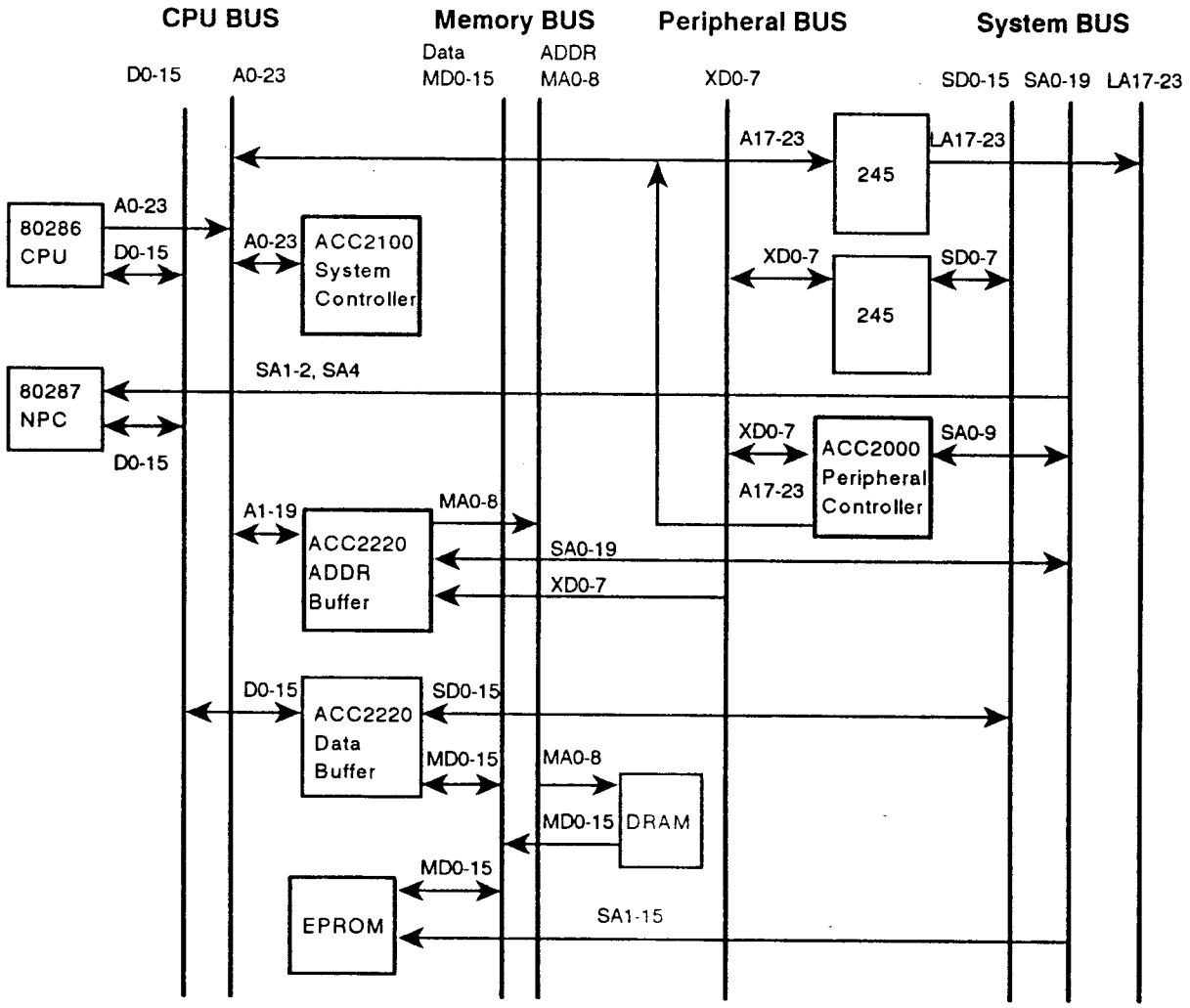
The ACC 82010 chip set can support a 12.5/16 MHz system clock design while maintaining 8 MHz AT bus compatibility. All chips in the ACC 82010 chip set are implemented using advanced CMOS technology and packaged in standard 84-L PLCC packages. The chip set's high integration reduces total system cost through lower power requirements, increased reliability, and reduced board size.

ACC 82010 System Block Diagram



ACC 2000
PC/AT Integrated Bus & Peripheral Controller

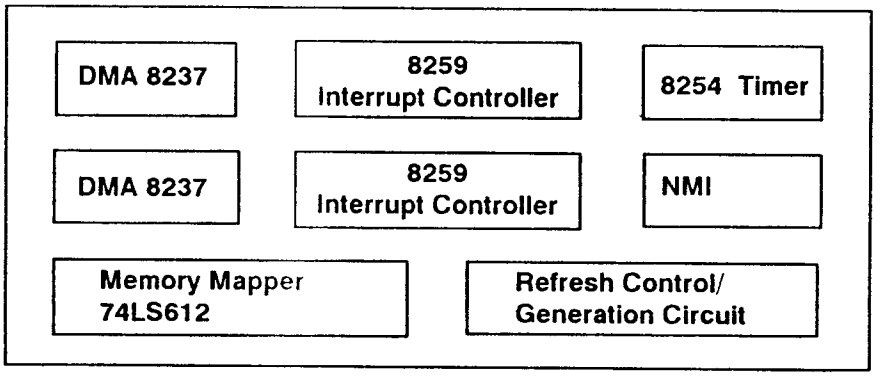
The ACC 2000 is an integrated high performance CMOS PC/AT* peripheral controller that incorporates several TTL, SSI, and MSI including two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, and one 74LS612 memory mapper. The ACC 2000 is a high performance VLSI that offers a single chip solution for all the peripherals attached to the X BUS (peripheral bus) in IBM PC/AT compatible systems.

Features

- 100% hardware and software compatible with the IBM* PC/AT
- Fully compatible to Intel's

  8237 DMA controller
  8254 Timer/Counter
  8259 Interrupt controller
- Fully compatible to TI's 74LS612 memory mapper
- Supports 7 DMA channels, 3 timer/counter channels and 14 interrupt request channels
- 100 % compatible with the IBM AT I/O BUS
- Supports up to 8 MHz DMA clock
- Supports 16 MB DMA address space
- Built-in refresh control circuit
- TTL compatible
- Speed switching through hardware or software
- 1.5 micron high performance CMOS technology
- 84-L PLCC package

Block Diagram



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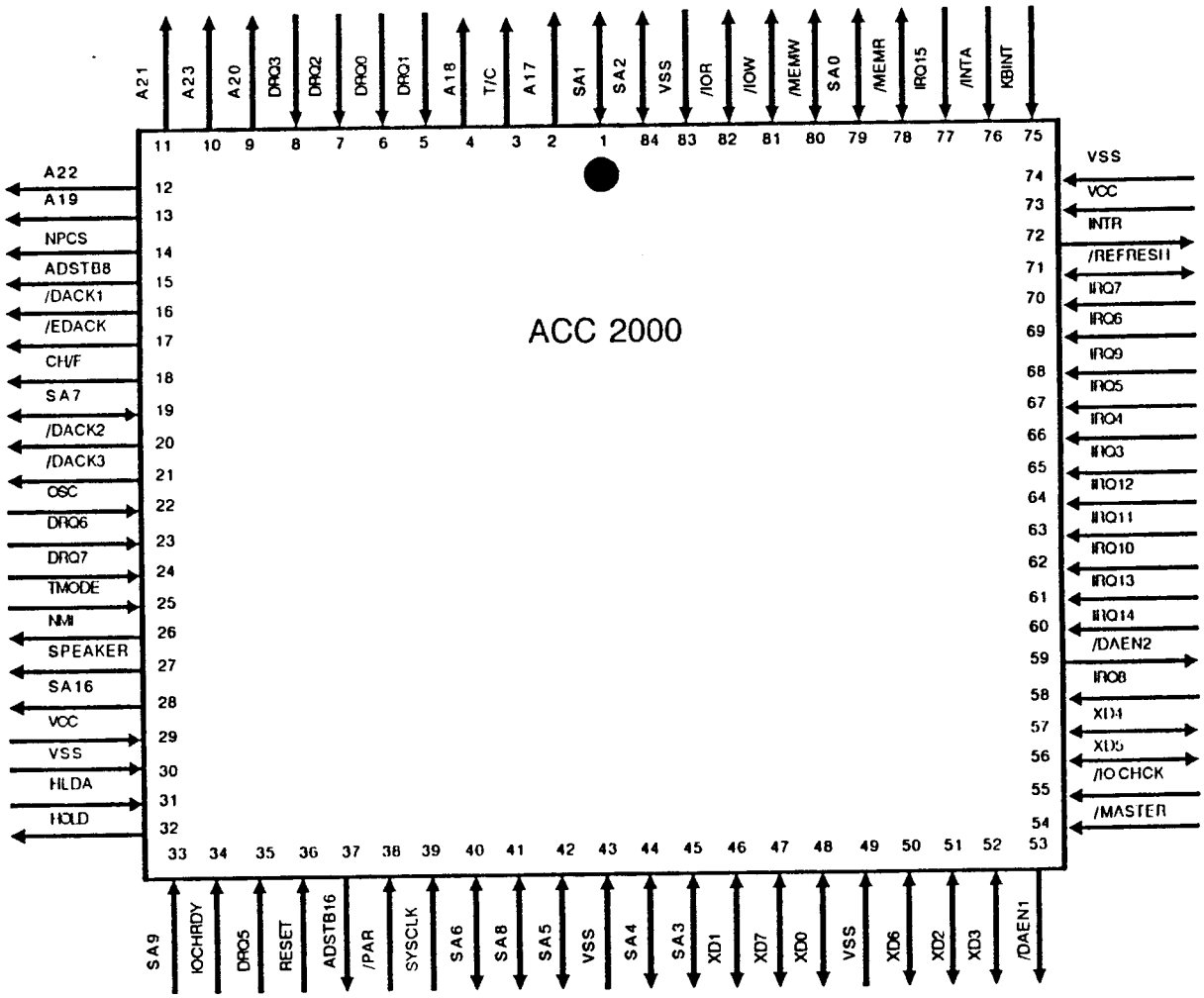
Pin Diagram


ACC 2000
A21 11
A23 10
A20 9
DRQ3 8
DRQ2 7
DRQ0 6
DRQ1 5
A18 4
T/C 3
A17 2
SA1 1
SA2 84
VSS 83
/IOR 82
/IOW 81
/MEMW 80
SA0 79
/MEMR 78
IRQ15 77
/INTA 76
KBINT 75
A22 12
A19 13
NPCS 14
ADSTB8 15
/DACK1 16
/EDACK 17
CH/F 18
SA7 19
/DACK2 20
/DACK3 21
OSC 22
DRQ6 23
DRQ7 24
TMODE 25
NMI 26
SPEAKER 27
SA16 28
VCC 29
VSS 30
HLDA 31
HOLD 32
VSS 74
VCC 73
INTR 72
/REFRESH 71
IRQ7 70
IRQ6 69
IRQ9 68
IRQ5 67
IRQ4 66
IRQ3 65
IRQ12 64
IRQ11 63
IRQ10 62
IRQ13 61
IRQ14 60
/DAEN2 59
IRQ8 58
XD4 57
XD5 56
/IOCHCK 55
/MASTER 54
SA9 33
IOCHRDY 34
DRQ5 35
RESET 36
ADSTB16 37
/PAR 38
SYSCLK 39
SA6 40
SA8 41
SA5 42
VSS 43
SA4 44
SA3 45
XD1 46
XD7 47
XD0 48
VSS 49
XD6 50
XD2 51
XD3 52
/DAEN1 53

Pin Descriptions

Symbol	Pin	Type	Description
SA0	79	I/O	System address bus bit.
SA1	1		
SA2	84		
SA3	45		
SA4	44		
SA5	42		
SA6	40		
SA7	19		
SA8	41		
SA9	33	I	System address bus bit.
SA16	28	O	System address bus Bit 16.
A17	2	O	Address bus bit.
A18	4		
A19	13		
A20	9		
A21	11		
A22	12		
A23	10		
T/C	3	O	Terminal count pulsing. When the terminal count for DMA channel is reached.
DRQ0	6	I	DMA Request Line. Active high.
DRQ1	5		
DRQ2	7		
DRQ3	8		
DRQ5	35		
DRQ6	23		
DRQ7	24		
NPCS	14	O	Chip select for numeric processor 80287.
ADSTB8	15	O	Address strobe for 8 bit DMA transfers.
/DACK1	16	O	Encoded DMA acknowledge bit.
/DACK2	20		
/DACK3	21		
/EDACK	17	O	Enable DMA acknowledge decoder. Active low .
CH/F	18	O	Change operation speed with software, I/O port 3C5H Bit 0.

Pin Descriptions

Symbol	Pin	Type	Description
OSC	22	I	14.31818 MHz clock input.
TMODE	25	I	Test pin.
NMI	26	O	Non-maskable interrupt to 80286 CPU. Active high; NMI generated by the math processor, memory parity error, or error from bus /IOCHCK.
SPEAKER	27	O	Data to speaker.
HLDA	31	I	Hold acknowledge from CPU.
HOLD	32	O	Hold request to CPU. Active high.
IOCHRDY	34	I	I/O channel ready from expansion bus.
RESET	36	I	System reset.
ADSTB16	37	O	Address strobe for 16 bit DMA transfers.
/PAR	38	I	Parity error output from Data buffer. Active low.
SYSCLK	39	I	System clock.
XD0	48	I/O	Peripheral data bus Bit 0.
XD1	46		
XD2	51		
XD3	52		
XD4	57		
XD5	56		
XD6	50		
XD7	47		
/DAEN1	53	O	DMA address enable for 8 bit data transfer. Active low.
/MASTER	54	I	CPU I/O control for address, data, and control lines.
/IOCHCK	55	I	Error expansion bus. Active low.
/DAEN2	59	O	DMA address enable for 16 bit data transfer. Active low.

Pin Descriptions

Symbol	Pin	Type	Description
IRQ3	65	I	Interrupt request input. Active high.
IRQ4	66	I	
IRQ5	67	I	
IRQ6	69	I	
IRQ7	70	I	
IRQ8	58	I	
IRQ9	68	I	
IRQ10	62	I	
IRQ11	63	I	
IRQ12	64	I	
IRQ13	61	I	
IRQ14	60	I	
IRQ15	77	I	
/REFRESH	71	I/O	Refresh cycle. Active low.
INTR	72	O	Interrupt to CPU. Active high.
KBINT	75	I	Keyboard interrupt to 8259.
/INTA	76	I	Interrupt acknowledge. Active low.
/MEMR	78	I/O	Memory read. Active low.
/MEMW	80	I/O	Memory write. Active low.
/IOW	81	I/O	I/O write. Active low.
/IOR	82	I/O	I/O read. Active low.
VCC	29, 73		+5 volt supply
VSS	30, 43, 49, 74, 83		Ground

Functional Description

Interrupt Controller

Two programmable interrupt controllers in the ACC 2000 function as a system wide interrupt manager for an IBM PC/AT system, compatible with the Intel 8259 interrupt controller. The interrupt controller efficiently determines when and which I/O device is serviced by the microcomputer.

The two cascaded interrupt controllers in the ACC 2000 provide a total of 15 possible interrupt sources. One of these interrupt request lines is used internally, providing a total of 14 possible external interrupt sources. The internal line connects to the 8254 Counter 0 output.

Mode Controller

The system clock can be switched by either software or hardware.

With software switching, users can program Bit 0 in I/O port 3C5H to select the frequency of the system clock. When Bit 0 is programmed HIGH, it operates in "turbo" mode.

Hardware switching is with a button key or a jumper connecting to the CH/F pin to select the appropriate mode. If the CH/F signal is a rising edge trigger, it is set to "turbo" mode, and if a falling edge, it is set to "normal" mode.

Each switching scheme is independent of the other. The system is always set by the latest selection, hardware or software.

DMA

There are two 8237 equivalent DMA controllers cascaded together in the ACC 2000 chip. During a DMA cycle, one of the two external 8-bit latches hold the middle range address bits while the 74LS612 generates the upper range address bits. Once the hold request has been acknowledged, the DMA controller drives 24 address bits for a total addressing capability of 16 Megabytes. The middle address bits of the 24-bit address range are held in two sets of 8-bit registers, one register for each DMA controller. The DMA controller drives the value to be loaded onto the data bus, and then issues an address strobe signal to latch the data bus value into these registers.

The two 8237 compatible DMA controllers in the ACC 2000 provide a total of seven external DMA channels. Each channel has a 24-bit address output to access data throughout the entire 16 megabyte system address space. Channel 0 through channel 3 support 8-bit peripherals and an 8 or 16-bit memory. Each channel can transfer data in 64 Kbyte pages.

Channel 4 is used for cascading and is not available externally. Channel 5 through channel 7 support 16-bit I/O adapters to transfer data between 16-bit I/O adapters and 16-bit system memory. Each channel can transfer data in 128 Kbyte pages. The DMA function improves the computer system by allowing external devices to transfer information directly from and to the system memory.

Features include

- Address increment or decrement.
- Seven independent DMA channels with independent auto initialization for each channel.
- Each DMA request can be controlled individually to enable or disable.
- Software DMA request.

Timer/Counter

The Timer/Counter is the functional equivalent of an 8254 timer. It has three internal counters and clock inputs. The three clock inputs are tied to a clock of 1.19 MHz. The output of Counter 0 is connected to the IRQ input of interrupt controller one. Counter one output initiates a refresh cycle and Counter two output generates sound waveforms for speaker circuitry.

Features:

- Three independent 16-bit counters
- Count binary or BCD

Memory Mapper

The ACC 2000 has the equivalent of a 74LS612 to generate the upper address bits during a DMA cycle.

Source Memory Mapper	8237
(for DMA Channels 0 - 3)	
Address A23 <--> A16	A15 <--> A0
(for DMA Channels 5 - 7)	
Address A23 <--> A17	A16 <--> A1

PIO

The PIO is the system configuration to control the timer channel speaker ports. It also has circuitry to detect refresh. This condition can be read back as Bit 4.

Refresh Generation Logic

Refresh circuitry contains an 8-bit counter for address SA0-7 during a refresh.

Refresh/DMA Abitration Logic

ACC 2000 contains circuitry to control a refresh cycle. A 74LS590 equivalent 8-bit counter outputs the refresh addresses onto the memory bus when the refresh signal is pulled low.

There are two possible sources for a hold request to the CPU. Either the DMA controller issues a hold request or the output of Counter 1 in the 8254 makes a low to high transition. The HOLD line is active when either source is requesting a hold. The hold request from the DMA controller is sampled on the rising edge of the DMA clock and the request from the timer is sampled on the falling edge of the DMA clock.

If the DMA controller's hold wins the arbitration, the HOLD is asserted, and it waits for a signal back from the CPU. When the DMA controller is finished, it negates its hold request signal to the arbiter. The arbitration then switches to a REFRESH cycle if there is a pending hold from the Counter/Timer, otherwise the arbiter inactivates the HOLD line and returns control to the CPU.

If a refresh cycle wins the arbitration, the HOLD is asserted and the ACC 2000 pulls the /REFRESH pin low. /REFRESH remains low for four SYSCLK rising edges. On the fourth rising edge of SYSCLK, the HOLD line is inactivated. However, if there is a pending hold request from the DMA controller on the fourth rising edge of SYSCLK, the REFRESH cycle is extended for one more SYSCLK cycle. The Hold request arbiter then acknowledges the hold request from the DMA controller.

NMI and Port B Logic

The ACC 2000 contains non-maskable interrupt (NMI) signal generation logic. An NMI can be caused by an I/O error or by a parity error. Port B indentifies the source of the error. At power up, the NMI signal is masked off. NMI is enabled by writing to I/O address 070 hex with Bit 7 low; NMI is disabled by writing to I/O addresss 070 hex with Bit 7 high.

Rating Specifications

Absolute Maximum Ratings*

TA = 25° C

Parameter	Symbol	Min	Max	Unit
Power supply voltage	V_{CC}	-0.5	7.0	V
Power dissipation (@5.25 V)	W_d		1	W
Current (@5.25 V)	I_{DD}	20	50	mA
Input voltage	V_I	-0.5	VCC+0.5	V
Output voltage	V_O	-0.5	VCC+0.5	V
Operating temperature	T_{op}	0	70	°C
Storage temperature	T_{stg}	-50	150	°C

* Exposing the device to stress above these limits can cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Capacitance Limits

TA = +25° C, VCC = 5 V

Parameter	Symbol	Min	Max	Unit	Test Condition
Input capacitance	C_I		10	pF	fc = 1 MHz unmeasured pins at GND
I/O capacitance	C_{IO}		15	pF	

DC Characteristics

TA = 0° C to +70° C, VCC = +5 V +/- 10%

DRQ0-3, DRQ5-7, TMODE, HLDA, SA9, IOCHRDY, RESET, /PAR, SYSCLK, /MASTER, /IOCHCK, IRQ3-15, KBINT, /INTA, OSC

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 +/- 0.5 V
Input low current	IIL		-10	uA	VIN > VSS
Input high current	IIH		-10	uA	VIN < VCC

XD0-7

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.2VCC - 0.1 V		VCC = 5 +/- 0.5 V
Input high voltage	VIH	0.2VCC + 0.9	VCC	V	VCC = 5 +/- 0.5 V
Input low current	IIL		-10	uA	VIN > 0.0V
Input high current	IIH		10	uA	VIN < VCC
Output low voltage	VOL		0.45	V	IOL = 3.2mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA
Tristate leakage current	IOZ	-10	10	uA	0 V < VOUT < VCC

SA0-6, SA8, /REFRESH, /MEMR, /MEMW, /IOW, /IOR

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.2VCC - 0.1	V	VCC = 5V +/- 5%
Input high voltage	VIH	0.7VCC	VCC	V	VCC = 5V +/- 5%
Input low current	IIL		-10.0	uA	VIN > VSS
Input high current	IIH		10.0	uA	VIN < VCC
Output low voltage	VOL		0.45	V	IOL = 9.6mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA
Tristate leakage current	IOZ	-10.0	10.0	uA	0V < VOUT < VCC

NPCS, ADSTB8, /DACK1-3, /EDACK, CH/F, NMI, SPEAKER, HOLD, ADSTB16, /DAEN1-2, INTR

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 3.2mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA

T/C

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 9.6mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA

A17-23

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 3.2mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA
Tristate leakage current	IOZ	-10.0	10.0	uA	0V < VOUT < VCC

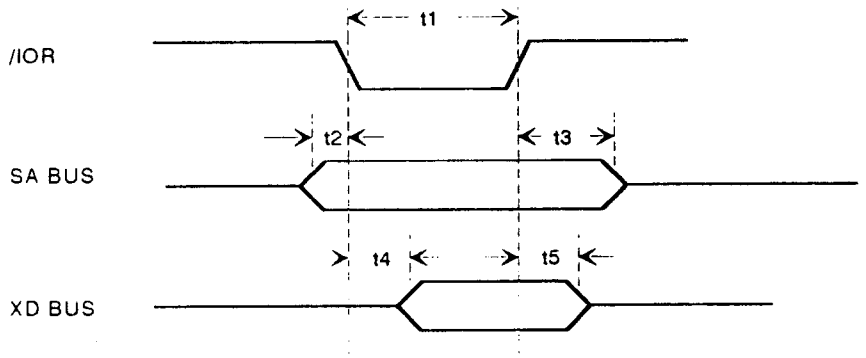
SA16

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 9.6mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA
Tristate leakage current	IOZ	-10.0	10.0	uA	0V < VOUT < VCC

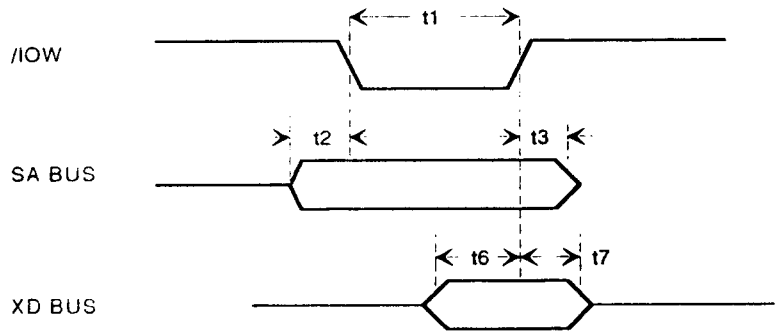
AC Specifications

Symbol	Parameter	Min	Max	Units
t1	/IOR or /IOW pulse width	110		ns
t2	SA address valid to /IOR /IOW low setup time	25		ns
t3	SA address hold time from /IOR /IOW high	13		ns
t4	XD data valid delay from /IOR low		110	ns
t5	XD data float delay from /IOR high	0	90	ns
t6	XD data valid to /IOW high setup time	70		ns
t7	XD data hold time from /IOW high	15		ns
t8	RESET high pulse width	250		ns
t9	RESET inactive to first /IOR or /IOW command	4		SYSCLK Cycle
t10	Command recovery time between successive /IOR or /IOW pulses	125		ns
t11	CH/F valid from /IOW high delay		60	ns
t12	NPCS valid from address delay		51	ns
t13	NMI output delay		68	ns

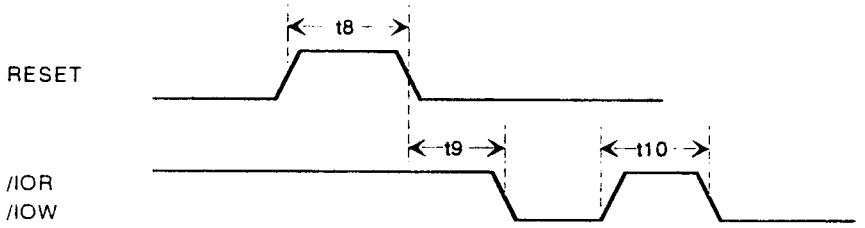
Peripheral Read Timing



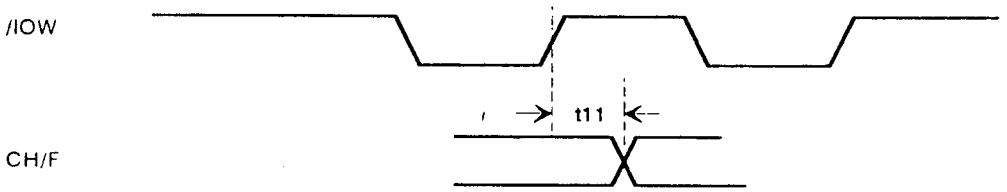
Peripheral Write Timing

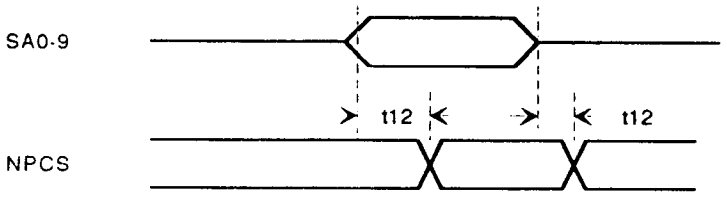


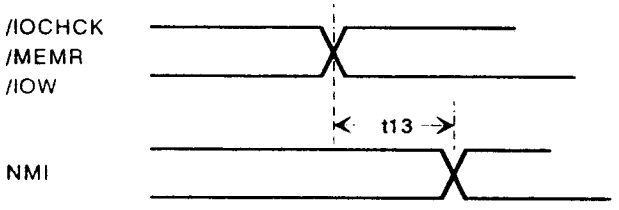
Command and Reset Timing



Other Timing Waveforms



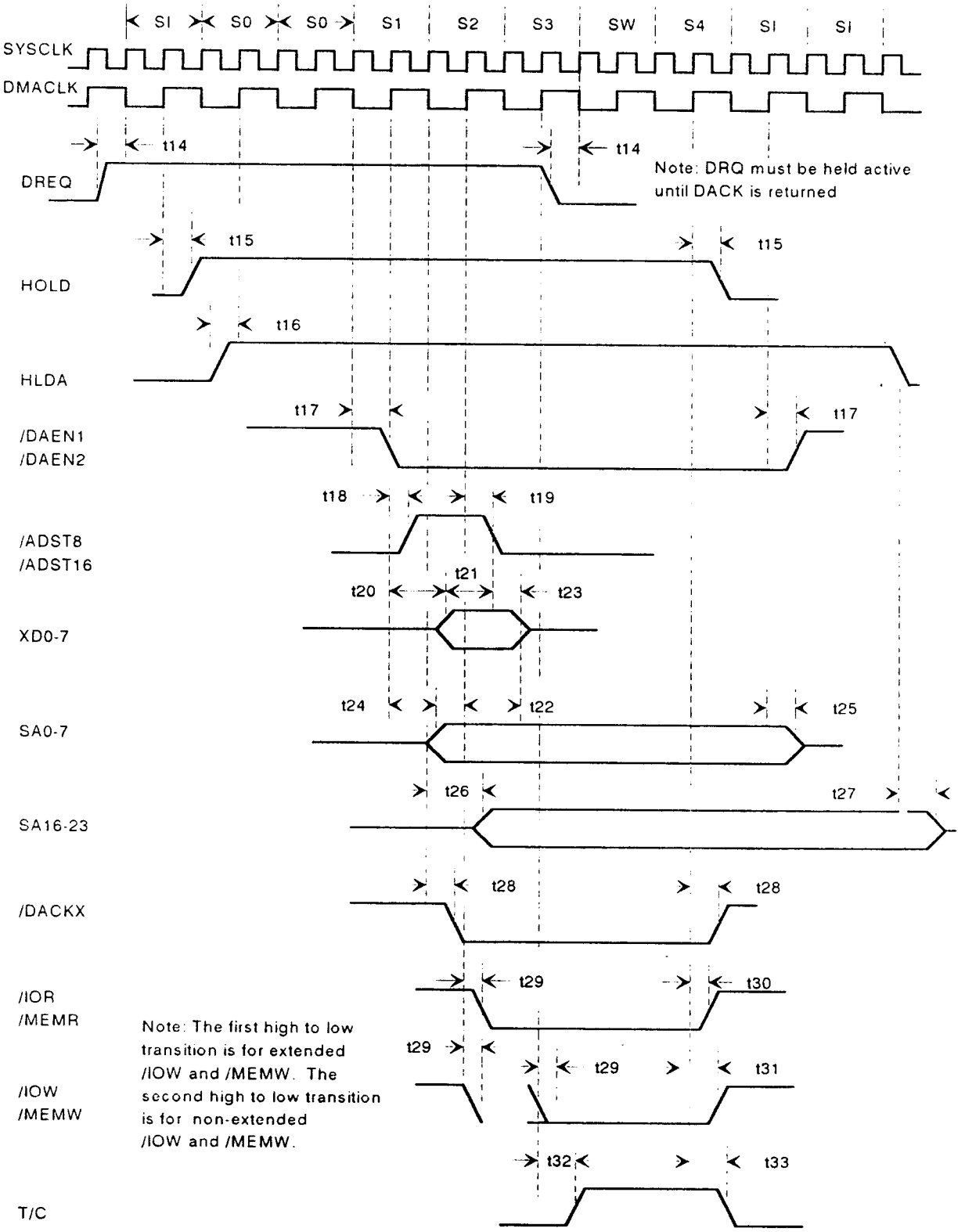




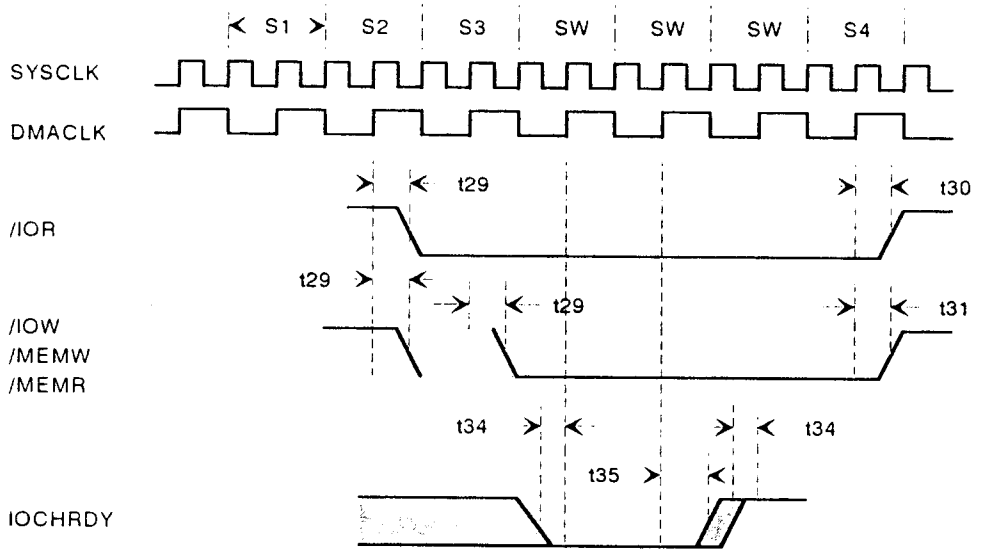
AC Specifications

Symbol	Parameter	Min	Max	Units
t14	DRQ to SYSCLK high setup time	0		ns
t15	HOLD valid from SYSCLK high delay time		50	ns
t16	HLDA to SYSCLK high setup time	25		ns
t17	/DAEN1 valid from SYSCLK high delay time		77	ns
t18	ADSTB8 or ADSTB16 high from SYSCLK high		72	ns
t19	ADSTB8 or ADSTB16 low from SYSCLK high delay time		76	ns
t20	Data float to active delay from SYSCLK high		93	ns
t21	Data to ADSTB8 or ADSTB16 low set up time	70		ns
t22	Data active to float delay from SYSCLK high		92	ns
t23	Data from ADSTB8 or ADSTB16 low HOLD time	8		ns
t24	low byte ADDR float to active from SYSCLK high		180	ns
t25	low byte ADDR active to float delay from SYSCLK high		70	ns
t26	high byte ADDR float to active delay from SYSCLK high		123	ns
t27	high byte add active to float from HLDA low		35	ns
t28	/DACK valid from SYSCK high delay time		83	ns
t29	/IOR, /IOW, /MEMR, /MEMW active from SYSCLK high delay time		53	ns
t30	/IOR and /MEMR inactive from SYSCLK high delay time		97	ns
t31	/IOW and /MEMW inactive from SYSCLK high delay time		80	ns
t32	T/C active from SYSCLK high delay time		82	ns
t33	T/C inactive from SYSCLK high delay time		82	ns
t34	IOCHRDY input setup time to SYSCLK high	26		ns
t35	IOCHRDY input hold time from SYSCLK high	15		ns

DMA Timing


SI
S0
S0
S1
S2
S3
SW
S4
SI
SI
SYSCLK
DMACLK
t14
t14
DREQ
Note: DRQ must be held active until DACK is returned
t15
t15
HOLD
t16
HLDA
t17
t17
/DAEN1
/DAEN2
t18
t19
/ADST8
/ADST16
t21
t20
t23
XD0-7
t24
t22
t25
SA0-7
t26
t27
SA16-23
t28
t28
/DACKX
t29
t30
/IOR
/MEMR
t29
t29
t31
/IOW
/MEMW
Note: The first high to low transition is for extended /IOW and /MEMW. The second high to low transition is for non-extended /IOW and /MEMW.
t32
t33
T/C

IOCHRDY Timing

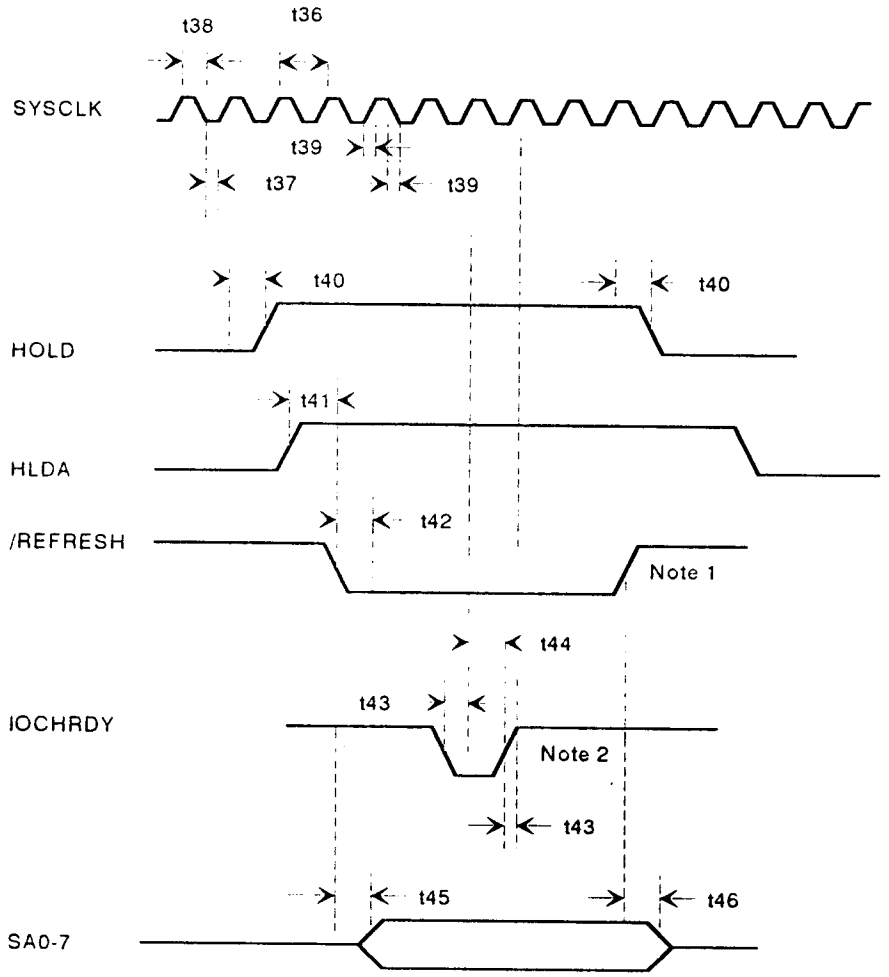


The first wait state is inserted by the internal circuitry of the ACC 2000 for all DMA cycles. Additional wait states must be inserted using IOCHRDY.

AC Specifications

Symbol	Parameter	Min	Max	Units
t36	SYSCLK cycle time	62		ns
t37	SYSCLK pulse width low	25		ns
t38	SYSCLK pulse width high	25		ns
t39	SYSCLK rise/fall time	10		ns
t40	HOLD valid from SYSCLK high delay time		50	ns
t41	/REFRESH low delay from HLDA		40	ns
t42	/REFRESH low to SYSCLK high setup time		20	ns
t43	IOCHRDY input setup time to SYSCLK high	26		ns
t44	IOCHRDY input hold time from SYSCLK high	15		ns
t45	REFRESH address valid delay from /REFRESH		92	ns
t46	Refresh address hold time from /REFRESH inactive		88	ns

Refresh Timing



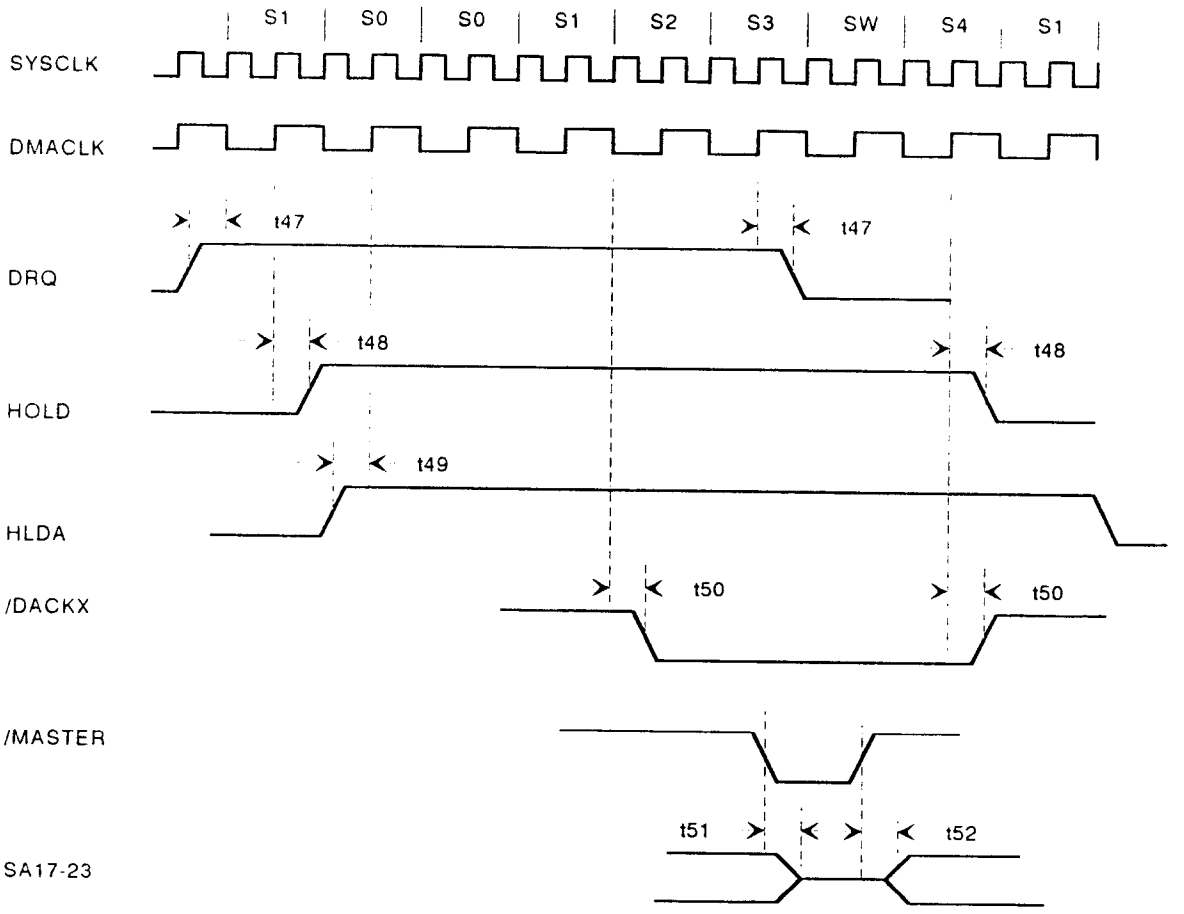
Notes

1 A /REFRESH pulse is normally four SYSCLK cycles long.
2 /REFRESH cycles can be extended by inserting wait states using IOCHRDY.

AC Specifications

Symbol	Parameter	Min	Max	Units
t47	DRQ to SYSCLK high setup time	0		ns
t48	HOLD valid from SYSCLK high delay time		50	ns
t49	HLDA to SYSCLK high set up time	25		ns
t50	/DACK valid from SYSCLK high delay time		83	ns
t51	SA17-SA23 float from /MASTER low delay time	11	36	ns
t52	SA17-SA23 active from /MASTER high delay time	11	36	ns

/MASTER Timing

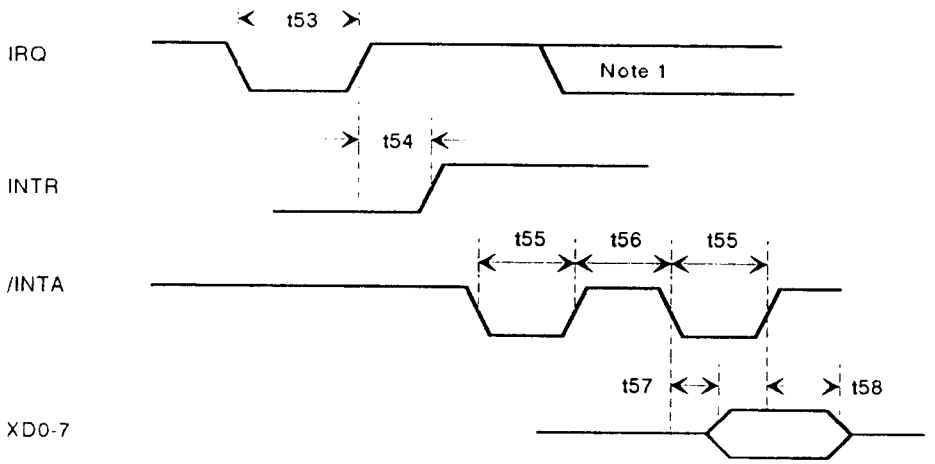


Note: A new bus master must be programmed in Cascade mode.
The new master must not pull /MASTER low until it has received the corresponding /DACK signal.

AC Specifications

Symbol	Parameter	Min	Max	Units
t53	Interrupt request pulse width low	60		ns
t54	Interrupt output delay		63	ns
t55	/INTA pulse width low	80		ns
t56	/INTA to next /INTA within an INTA sequence only	120		ns
t57	XD data valid delay from /INTA low		109	ns
t58	XD data float delay from /INTA high	22	69	ns

Interrupt Timing

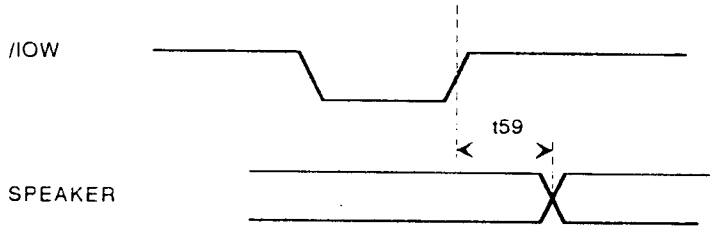


Note 1 IRQ must remain active until the first /INTA pulse.

AC Specifications

Symbol	Parameter	Min	Max	Units
t59	SPEAKER valid from /IOW high delay time		100	ns

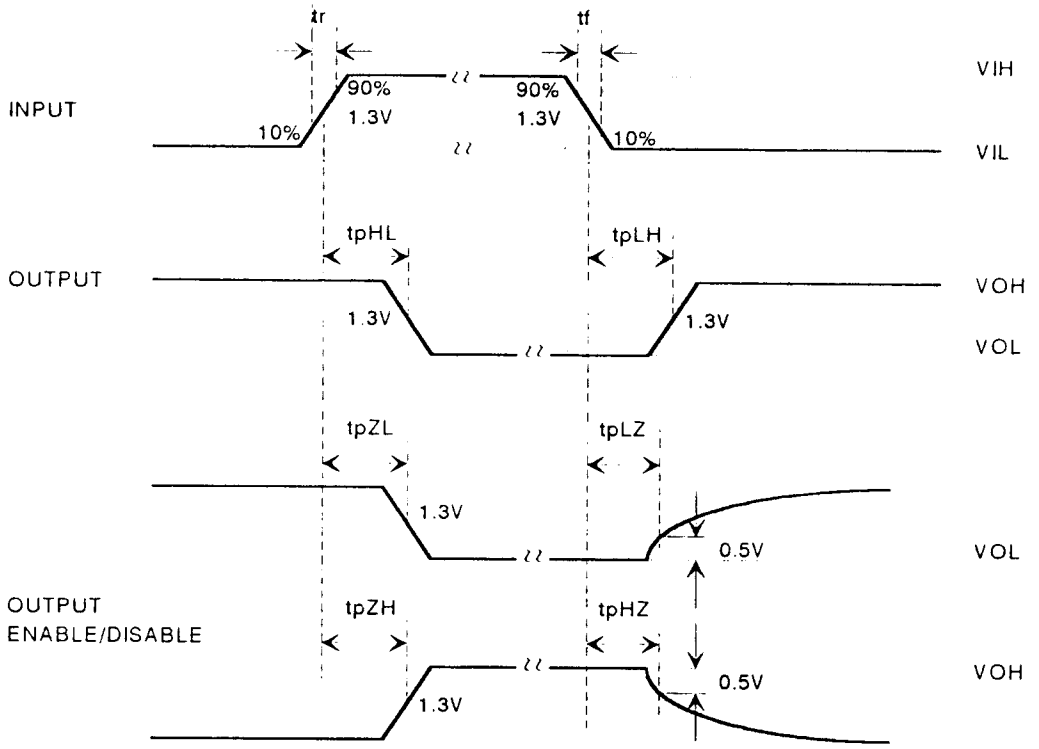
8254 Timing



Load Circuit and AC Characteristics Measurement

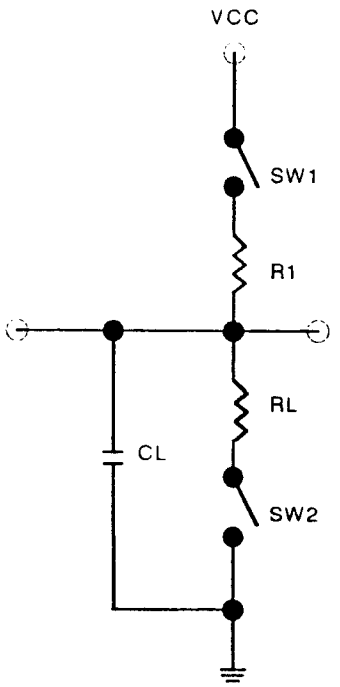
Parameter	Output Type	Symbol	CL(pF)	R1	RL	SW1	SW2
Propagation Delay Time	Totem pole 3-state Bidirectional	tPLH	50		1.0K	off	on
		tPHL	50		1.0K	off	on
Propagation Delay time	Open drain or Open collection	tPLH	50	0.5K		on	off
		tPHL	50	0.5K		on	off
Disable time	3-state Bidirectional	tPLZ	5	0.5K	1.0K	on	on
		tPHZ	5	0.5K	1.0K	off	on
Enable time	3-state Bidirectional	tPZL	50	0.5K	1.0K	on	on
		tPZH	50	0.5K	1.0K	off	on

AC Characteristics Measurement



VIH = 3 V, VIL = 0, tr < 10 ns, tf < 5 ns

Load Circuit



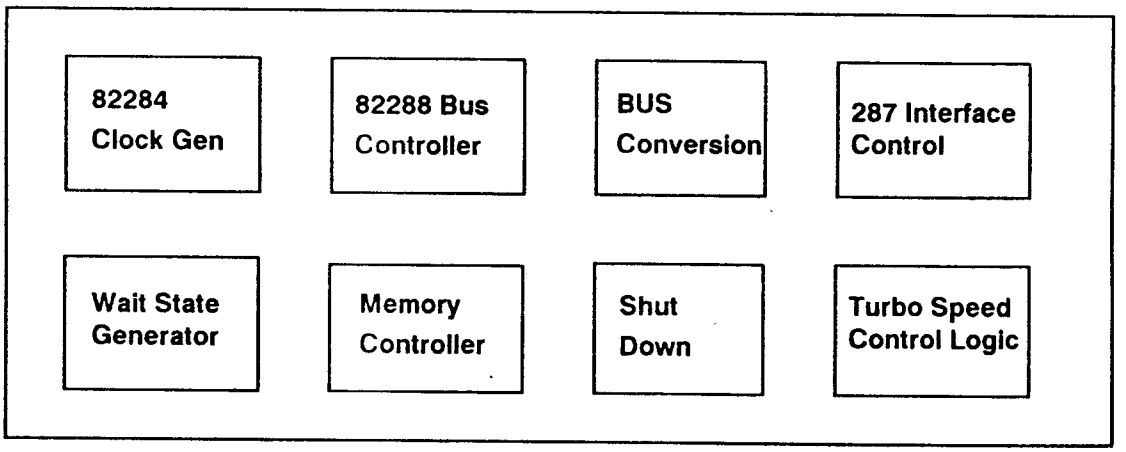
ACC 2100
PC/AT Integrated System Controller

The ACC 2100 is an integrated high performance CMOS PC/AT system controller that integrates the following functions and logic into one single chip: clock generator and selector, bus controller, bus swap logic, coprocessor interface logic, memory decoder, command delay and wait state generation circuits, reset and shut down logic, and ADDR/DATA control logic.

Features

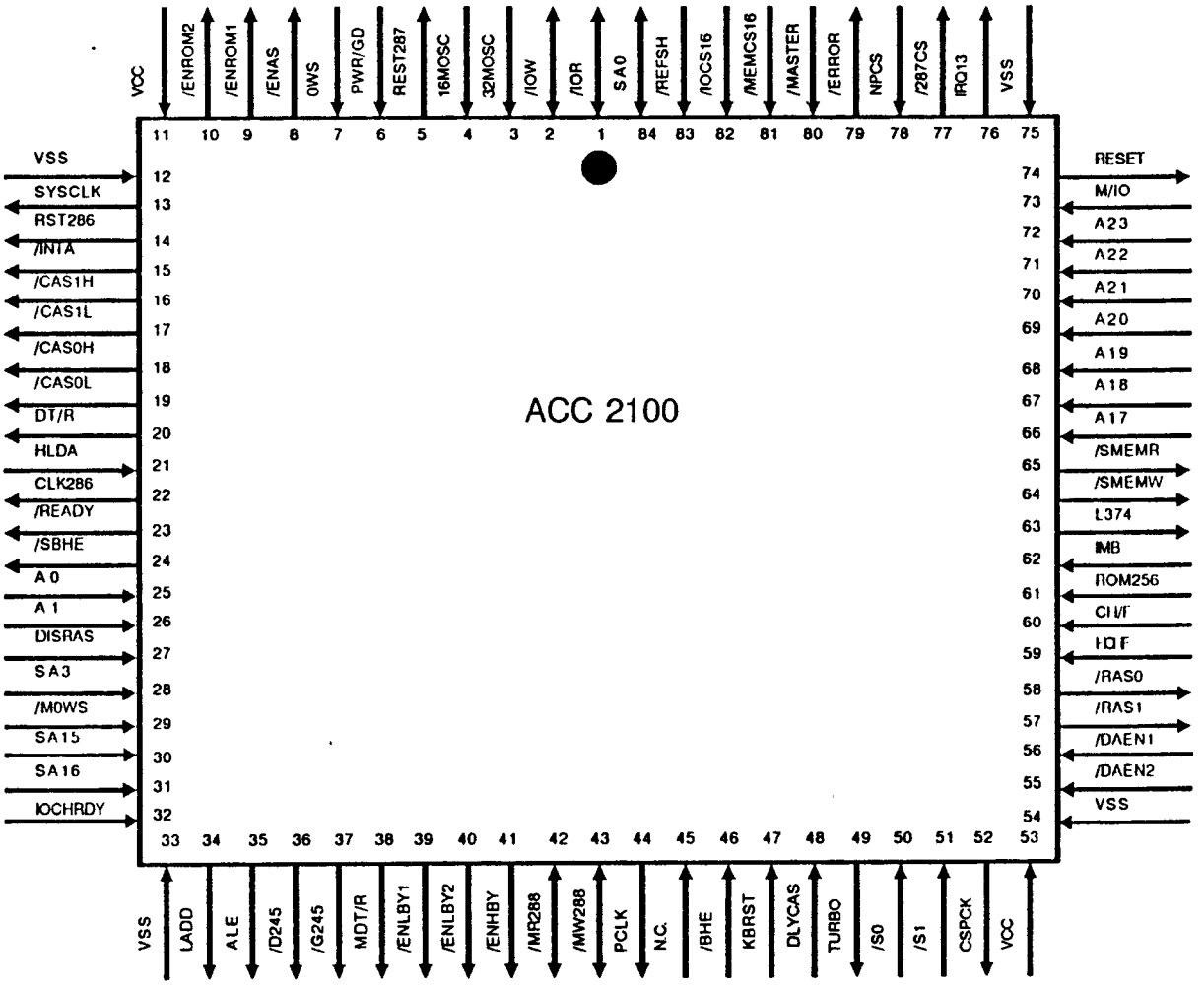
- 100% hardware and software compatible with the IBM PC/AT
- Fully compatible with Intel's 82284 clock generator, and 82288 bus controller
- Buit-in 80287 coprocessor interface logic
- Built-in command delay and wait state generation logic
- ROM chip select for 27128 or 27256
- Built-in memory controller
- Turbo speed change performed through hardware or software
- 8 MHz I/O AT BUS compatible
- Bus swap function
- 1.5 micron high performance CMOS technology
- TTL compatible
- 84-L PLCC package

Block Diagram



ACC Microelectronics Corporation · 3295 Scott Blvd.Suite · Santa Clara, CA 95054
Phone: 408-980-0622 FAX: 408-980-0626

Pin Diagram


ACC 2100
VCC 11
/ENROM2 10
/ENROM1 9
/ENAS 8
0WS 7
PWR/GD 6
REST287 5
16MOSC 4
32MOSC 3
/IOW 2
/IOR 1
SA0 84
/REFSH 83
/IOCS16 82
/MEMCS16 81
/MASTER 80
/ERROR 79
NPCS 78
/287CS 77
IRQ13 76
VSS 75
VSS 12
SYSCLK 13
RST286 14
/INTA 15
/CAS1H 16
/CAS1L 17
/CAS0H 18
/CAS0L 19
DT/R 20
HLDA 21
CLK286 22
/READY 23
/SBHE 24
A0 25
A1 26
DISRAS 27
SA3 28
/M0WS 29
SA15 30
SA16 31
IOCHRDY 32
RESET 74
M/IO 73
A23 72
A22 71
A21 70
A20 69
A19 68
A18 67
A17 66
/SMEMR 65
/SMEMW 64
L374 63
IMB 62
ROM256 61
CHF 60
HOF 59
/RAS0 58
/RAS1 57
/DAEN1 56
/DAEN2 55
VSS 54
VSS 33
LADD 34
ALE 35
/D245 36
/G245 37
MDT/R 38
/ENLBY1 39
/ENLBY2 40
/ENHBY 41
/MR288 42
/MW288 43
PCLK 44
N.C. 45
/BHE 46
KBRST 47
DLYCAS 48
TURBO 49
/S0 50
/S1 51
CSPCK 52
VCC 53

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/IOR	1	I/O	I/O read
/IOW	2	I/O	I/O write
32MOSC	3	I	32 MHz OSC input (Turbo)
16MOSC	4	I	16 MHz OSC input
REST287	5	O	Reset 80287 coprocessor.
PWR/GD	6	I	Power good.
0WS	7	I	Zero wait state input.
/ENAS	8	O	RTC address strobe enable.
/ENROM1	9	O	ROM chip select bank 1. Active low.
/ENROM2	10	O	ROM chip select bank 2. Active low.
SYSCLK	13	O	System clock.
RST286	14	O	Reset 286.
/INTA	15	O	Interrupt acknowledge. Active low.
/CAS1H	16	O	Column address select 1 high byte.
/CAS1L	17	O	Column address select 1 low byte.
/CAS0H	18	O	Column address select 0 high byte.
/CAS0L	19	O	Column address select 0 low byte.
DT/R	20	O	Data transmit/receive.
HLDA	21	I	Hold acknowledge from CPU.
CLK286	22	O	System clock output.
/READY	23	O	Ready signal to CPU.
/SBHE	24	O	System bus high enable.
DISRAS	27	I	RAS inactive control.
M0WS	29	I	Memory zero wait state input.
IOCHRDY	32	I	I/O channel ready.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
SA0	84	I/O	System address Bit 0, select low byte.
SA3	28	I	System address bus bit.
SA15	30	I	
SA16	31	I	
A0	25	I	Address bus bit.
A1	26		
A17	66		
A18	67		
A19	68		
A20	69		
A21	70		
A22	71		
A23	72		
/LADD	34	O	Load address.
ALE	35	O	Address latch enable.
/D245	36	O	Direction control for LS245.
/G245	37	O	Gate input for LS245.
MDT/R	38	O	Memory data transmit/receive.
/ENLBY1	39	O	Enable low byte Bank 1.
/ENLBY2	40	O	Enable low byte Bank 2.
/ENHBY	41	O	Enable high byte.
/MR288	42	I/O	Memory read.
/MW288	43	I/O	Memory write.
PCLK	44	O	Peripheral clock.
/BHE	46	I	High byte enable from CPU.
KBRST	47	I	Keyboard reset.
DLYCAS	48	I	Delay CAS active control.
TURBO	49	O	Turbo mode.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/S0 /S1	50 51	I	Bus cycle status bit.
CSPCK	52	O	Parity error output enable.
/DAEN2	55	I	DMA address enable for 16 bit data transfer. Active low.
/DAEN1	56	I	DMA address enable for 8 bit data transfer. Active low.
/RAS1	57	O	Row address select 1.
/RAS0	58	O	Row address select 0.
HCHF	59	I	Hardware turbo mode select.
CH/F	60	I	Software turbo mode select.
ROM256	61	I	256k ROM select.
1MB	62	I	1 megabyte memory select.
L374	63	O	Latch enable for CPU data bus to system data bus conversion.
/SMEMW	64	O	System memory write.
/SMEMR	65	O	System memory read.
M/IO	73	I	Memory or I/O select.
RESET	74	O	System reset.
IRQ13	76	O	IRQ 13
/287CS	77	O	80287 coprocessor select. Active low.
NPCS	78	I	Numeric processor chip select.
/ERROR	79	O	Error status.
/MASTER	80	I	Signal to gain system control.
/MEMCS16	81	I	Memory 16 bit chip select.
/IOCS16	82	I	I/O 16 bit chip select.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/REFRESH	83	I	Refresh cycle.
VCC	11, 53		+5 volt supply
VSS	12, 33, 54, 75		Ground
N.C.	45		

Functional Description

Wait State Generator

During a memory cycle, no wait state is inserted if /M0WS is active (low), otherwise one wait state is inserted. During an I/O cycle, no wait state is inserted when /0WS is active (low), otherwise 5 wait states are inserted for NONTURBO speed and 8 wait states are inserted for TURBO speed.

The IOCHRDY signal is also used to control wait states. When it is pulled low, the corresponding cycle has as many wait states inserted as possible until I/OCHRDY is returned high.

CPU Bus Control

The CPU bus controller is the functional equivalent of an 82288 for the CPU bus command and for the signals of both the system and peripheral buses. It generates the /IOR, /IOW, /INTA, /MR288, /MW288 and DT/R signals. Input signals, /S0, /S1, and M/IO, receive data from the 80286 CPU to inform the CPU bus controller of a bus cycle and to define the type of bus cycle. The bus cycles are defined in the following chart.

Bus Cycles

COD, /INTA	M/IO	/S1	/S0	Bus Cycle Initiated
0 (low)	0	0	0	Interrupt acknowledge
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	None, not a status cycle
0	1	0	0	If A1=1 then halt: else shutdown
0	1	0	1	Memory data read
0	1	1	0	Memory data write
0	1	1	1	None, not a status cycle
1 (high)	0	0	0	Reserved
1	0	0	1	I/O read
1	0	1	0	I/O write
1	0	1	1	None, not a status cycle
1	1	0	0	Reserved
1	1	0	1	Memory instruction read
1	1	1	0	Reserved
1	1	1	1	None, not a status cycle

Modes

The ACC 2100 operates in four basic modes:

AT CPU mode

This mode is active when HLDA is low. In this mode, the ACC 2100 drives /IOR, /IOW, /MR288 and /MW288.

DMA mode

If the inputs /DAEN1 or /DAEN2 are active, the ACC 2100 is in DMA mode. Commands such as /IOR, /IOW, /MR288 and /MW288 are driven by the DMA controller in the ACC 2000.

Refresh mode

When the refresh mode is active, /MR288 is driven to generate the refresh for the DRAMS, but /MW288, /IOR and /IOW are in high impedance state.

Master mode

A processor or DMA controller in cascade mode on the I/O slot can pull /MASTER low which causes it to control the system address, data and control line.

Data Conversion

The ACC 2100 contains logic to convert between 16-bit and 8-bit data accesses. Control signals /D245 and /G245 are generated from this chip to perform the conversions.

Memory Control

The memory control section of the ACC 2100 generates the Row Address Strobe (RAS) and Column Address Strobe (CAS) necessary to support dynamic RAMS in a PC/AT compatible system. /MR288 and /MW288 can be generated either by 82288 logic or by the DMA controller. Signals ENROM1 and ENROM2 generate output enable signals for BIOS and extend ROM.

Clock Generator

The ACC 2100 chip contains two clock generators. The first generates the system clock for the 80286 CPU and the DMA controllers in the ACC 2000. This clock generator can run the 80286 at dual frequencies, for example, 8 and 16 MHz, 8 and 12 MHz, or 8 and 10 MHz depending on the oscillator used. There is also a clock generator for the 8254 timer and the OSC signal (14.21818 MHz) for the standard AT BUS.

The frequency for the clock generator input must be twice the operating frequency of the CPU. For example, a 16 MHz system requires a 32 MHz oscillator. The CLK286 is generated directly from the oscillator and has the same frequency as the oscillator input. The CLK286 is connected directly to the CPU and Numerical Coprocessor clock inputs. The PCLK is half the frequency of the CLK286 and is used to clock the 8042 keyboard controller. The internal SYSCLK is also at half the CLK286 frequency with an inversed phase. The SYSCLK is used to drive the ACC 2000 peripheral controller.

Reset and Shut Down Logic

This functional block also contains the circuitry for reset and ready signals. The reset circuitry generates two resets. One is the general system reset with a power on. The other reset is used for the CPU power on or to take the 80286 out of a protected state when a request comes from the 8042 keyboard controller.

The PWR/GD input signal generates a system RESET signal and is sysnchronized to CLK286. When KBRST is generated from the 8042 keyboard controller (known as warm reset), the RST286 signal is activated to reset the 80286 CPU. RST286 is asserted for at least the 16 CLK286 cycles and then deactivated fot proper CPU operation. There is also circuitry for synchronizing the signal /READY to the 80286 CPU.

Oscillator Circuit

There a three oscillators in the AT system. One oscillator input is 14.21818 MHz. The second oscillator is 32 MHz which can also be 16, 20, 24 MHz as the overall system board clock frequency. The third oscillator is 16 MHz to support AT bus timing.

Numeric Processor 80287 Controls

The ACC 2100 contains circuitry to handle the decoding required to select and reset the Numeric Coprocessor. The /287CS signal is a chip select that is decoded at addresses 0F8-0FF hex. The REST287 output signal resets the 80287 coprocessor. The REST287 can be activated by a system reset or by performing a write operation to I/O port 0F1 hex. The IRQ13 pin is connected to the ACC 2000's line IRQ13 in a PC/AT environment.

Turbo and Normal Speed Conversion

The system clock can be switched between turbo speed and normal speed through either software or hardware.

If the CHF signal from the ACC 2000 is programmed high or HCHF is generating a rising edge trigger, the system clock generator can be set to turbo mode by selecting the higher speed (32 MHz) oscillator. Otherwise, a slower speed oscillator is selected, and the system clock runs at normal speed.

Rating Specifications

Absolute Maximum Ratings*

TA = 25° C

Parameter	Symbol	Min	Max	Units
Power supply voltage	VCC	3.0	7.0	V
Power dissipation (@5.25 V)	Wd		1	W
Current (@5.25 V)	IDD	20	50	mA
Input voltage	VI	0.0	5.5	V
Output voltage	VO	0.0	5.5	V
Operating temperature	Top	0	70	°C
Storage temperature	Tstg	-50	150	°C

* Exposing the device to stress above these limits can lcause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Capacitance

TA = +25° C, VCC = 5 V

Parameter	Symbol	Min	Max	Unit	Test Condition
Input capacitance	CI		10	pF	fc = 1 MHz unmeasured pins at GND
I/O capacitance	CIO		15	pF	

DC Specifications

TA = 0° C to +70° C, VCC = +5 V +/- 10%

32MOSC, 16MOSC, HLDA, 0WS, A0-1, DLYCAS, SA3, /M0WS, SA15-16, IOCHRDY, KBRST, /DAEN1-2, HCHF, CH/F, ROM256, 1MB, A17-23, M/IO, NPCS, /ERROR, /REFSH, /BHE, /MASTER, /MEMCS16, /IOCS16

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.5 V
Input low current	IIL		-1.0	uA	VIN = 0.0V
Input high current	IIH		1.0	uA	VIN = VCC

/IOR, /IOW, /MR288, /MW288, SA0

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.5 V
Output low voltage	VOL	0.4		V	IOL = 20mA
Output high voltage	VOH	2.4		V	IOH = -20mA
Tristate leakage current	IOZ	-30.0	30	uA	0 V < VOUT < VCC

SYSCLK, DT/R, ALE, /RAS0-1

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 8.0mA
Output high voltage	VOH	2.4		V	IOH = -8.0mA

CLK286, /READY, PCLK

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 20mA
Output high voltage	VOH	2.4		V	IOH = -20mA

/CAS1H, /CAS1L, /CAS0H, /CAS0L

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 4.0mA
Output high voltage	VOH	2.4		V	IOH = -4.0mA

/INTA, /SBHE

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 8.0mA
Output high voltage	VOH	2.4		V	IOH = -8.0mA
Tristate leakage current	IOZ	-10.0	10.0	uA	0V < VOUT < VCC

REST287, RST286, LADD, /D245, /G245, MDT/R, /ENLBY1, /ENLBY2, /ENHBY, TURBO, CSPCR, L374, IRQ13, /287CS ,ENAS, ENROM1, ENROM2

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 2.0mA
Output high voltage	VOH	2.4		V	IOH = -2.0mA

RESET

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 15mA
Output high voltage	VOH	2.4		V	IOH = -15mA

/S0, /S1

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0		V	VCC = 5 +/- 0.5 V
Input low current	IIL	-64	-250	uA	VIN = 0.0V

/SMEMW, /SMEMR

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 20.0mA
Output high voltage	VOH	2.4		V	IOH = -20.0mA
Tristate leakage current	IOZ	-30.0	30.0	uA	0V < VOUT < VCC

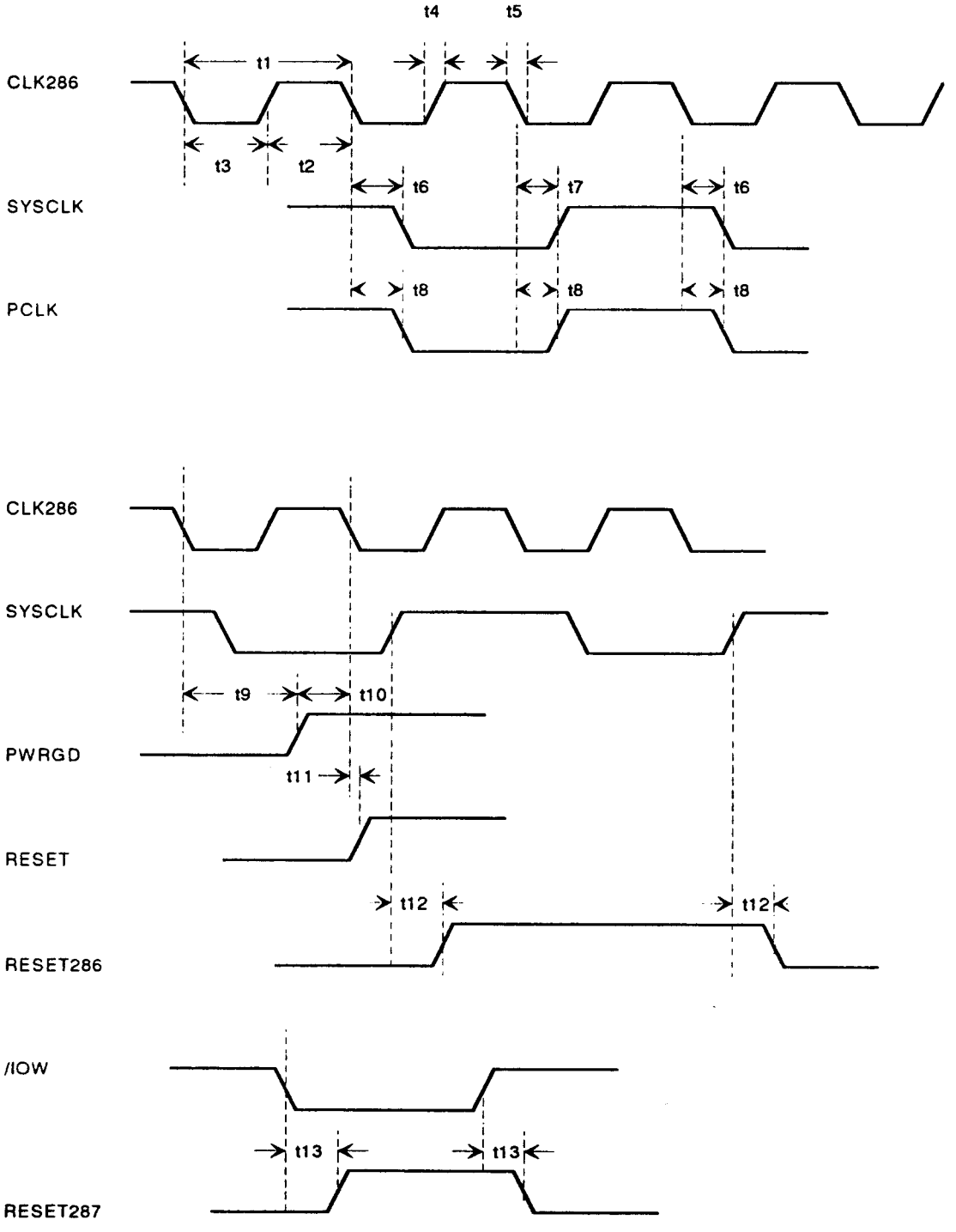
PWR/GD

Parameter	Symbol	Min	Max	Unit	Test Condition
Negative-Going Threshold	V_{t-}	0.7		V	
Positive-Going Threshold	V_{t+}		2.1	V	
Hysteresis	H	0.3		V	

AC Specifications

Symbol	Description	Min	Max	Unit	Condition
t1	CLK286 period	31	250	ns	
t2	CLK286 High pulse width	11	239	ns	
t3	CLK286 low pulse width	7	237	ns	
t4	CLK286 rise time		7	ns	1.0V to 3.6V
t5	CLK286 fall time		5	ns	3.6V to 1.0V
t6	SYSCLK low from CLK286 delay		23	ns	
t7	SYSCLK high from CLK286 delay		32	ns	
t8	PCLK from CLK286 delay		28	ns	
t9	PWRGD from CLK286 hold time	8		ns	
t10	PWRGD to CLK286 set up time	20		ns	
t11	RESET from CLK286 delay		26	ns	
t12	RESET 286 from SYSCLK		45	ns	
t13	RESET 287 from /IOW delay		45	ns	

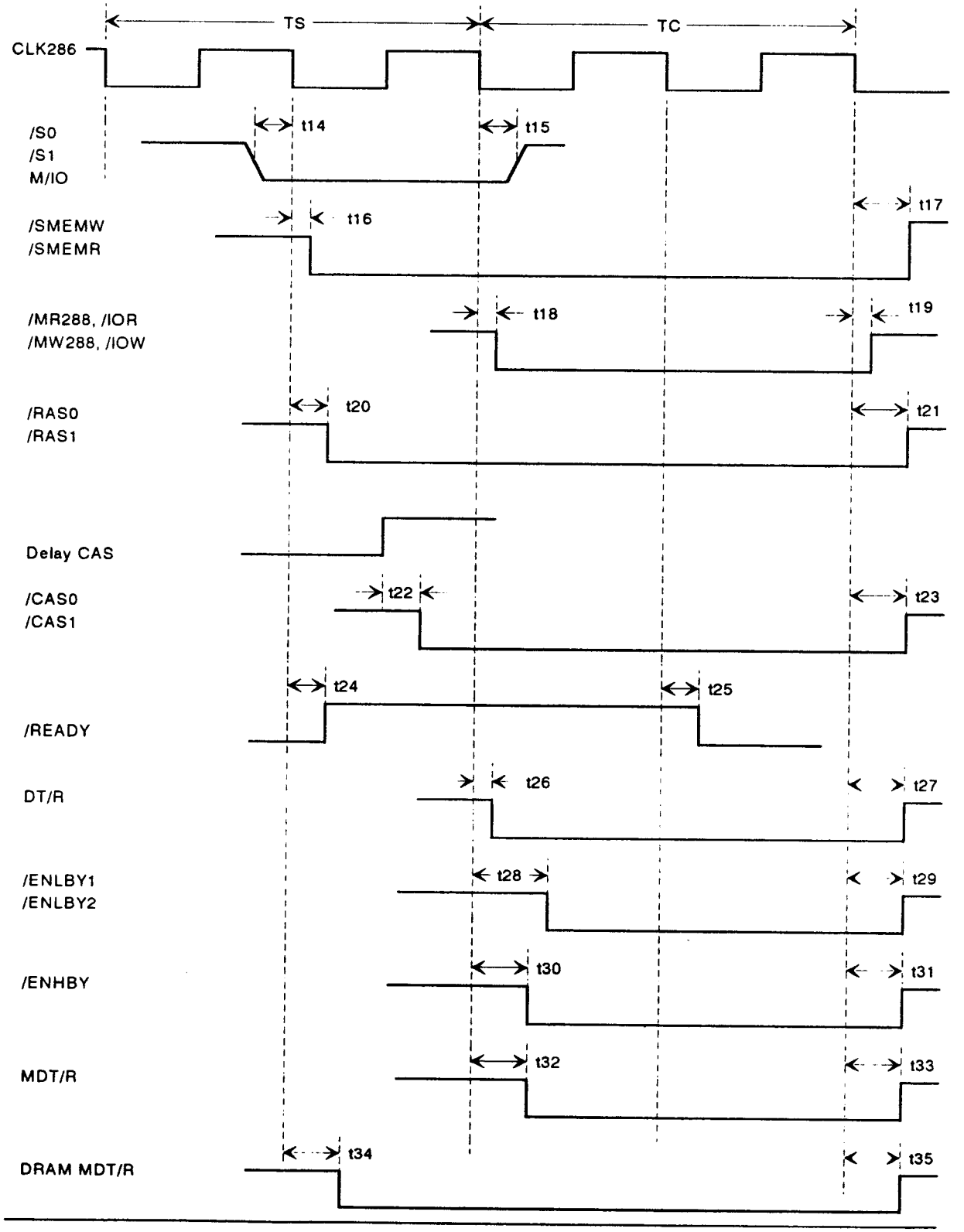
Processor and System Clock Timing



AC Specifications

Symbol	Description	Min	Max	Unit
t14	M/IO and status set up time	11		ns
t15	M/IO and status hold time	1		ns
t16	/SMEMR, /SMEMW active from CLK286 delay		25	ns
t17	/SMEMR, /SMEMW inactive from CLK286 delay		40	ns
t18	/IOR, /MR288, /IOW /MW288 active from CLK286 delay		29	ns
t19	/IOR, /MR288, /IOW, /MW288 inactive from CLK286 delay		27	ns
t20	/RAS0, /RAS1 active from CLK286 delay		35	ns
t21	/RAS0, /RAS1 inactive from CLK286 delay		40	ns
t22	/CAS0, /CAS1 active from delay CAS delay		28	ns
t23	/CAS0, /CAS1 inactive from CLK286 delay		40	ns
t24	/READY inactive from CLK286 delay		22	ns
t25	/READY active from CLK286 delay		22	ns
t26	DT/R low from CLK286 delay		29	ns
t27	DT/R high from CLK286 delay		40	ns
t28	/ENLBY1, /ENLBY2 active from CLK286 delay		56	ns
t29	/ENLBY1, /ENLBY2 inactive from CLK286 delay		40	ns
t30	/ENBY active from CLK286 delay		56	ns
t31	/ENBY inactive from CLK286 delay		40	ns
t32	MDT/-R low from CLK286 delay		56	ns
t33	MDT/-R high from CLK286 delay		50	ns
t34	DRAM MDT/-R low from CLK286 delay		44	ns
t35	DRAM MDT/-R high from CLK286 delay		50	ns

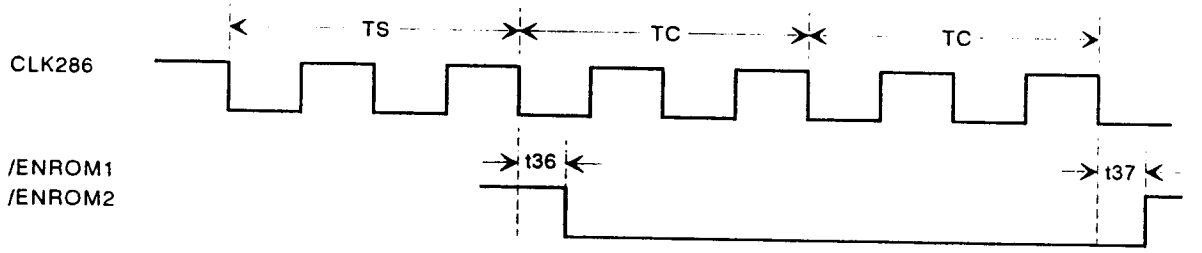
Worst Case Simulation + 0.5V 80°C Memory Timing



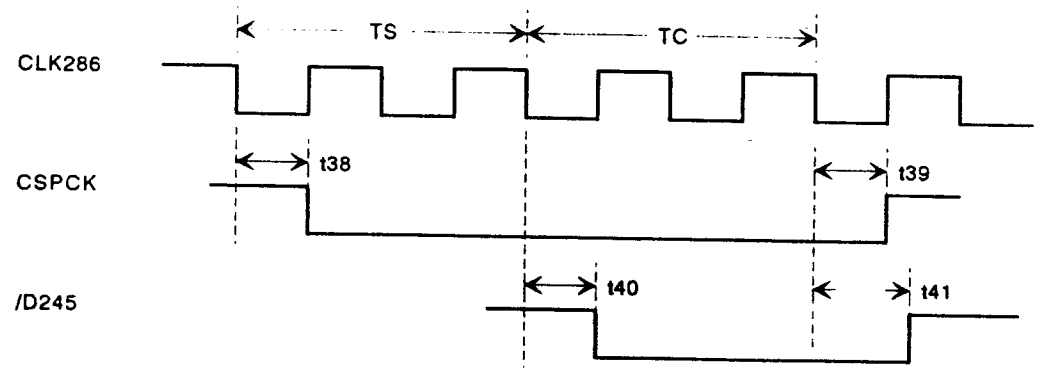
AC Specifications

Symbol	Description	Min	Max	Unit
t36	/ENROM1, /ENROM2 active from CLK286 delay		56	ns
t37	/ENROM1, /ENROM2 inactive from CLK286 delay		60	ns

ROM Access Timing



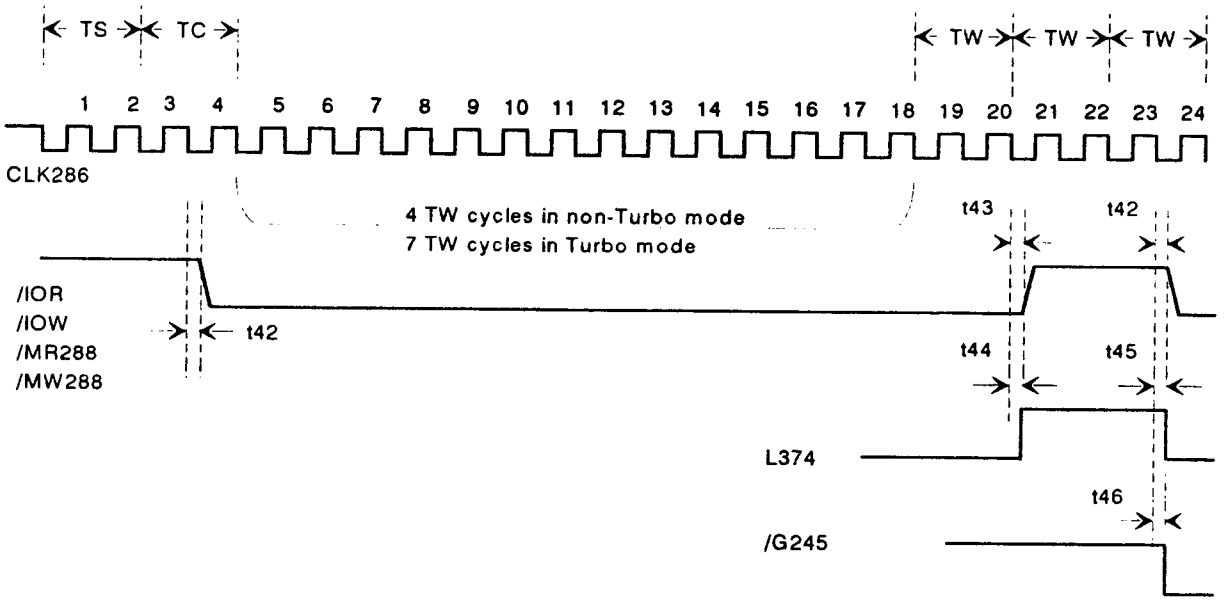
Symbol	Description	Min	Max	Unit
t38	CSPCK low from CLK286 delay		50	ns
t39	CSPCK high from CLK286 delay		50	ns
t40	/D245 active from CLK286 delay		50	ns
t41	/D245 inactive from CLK286 delay		60	ns

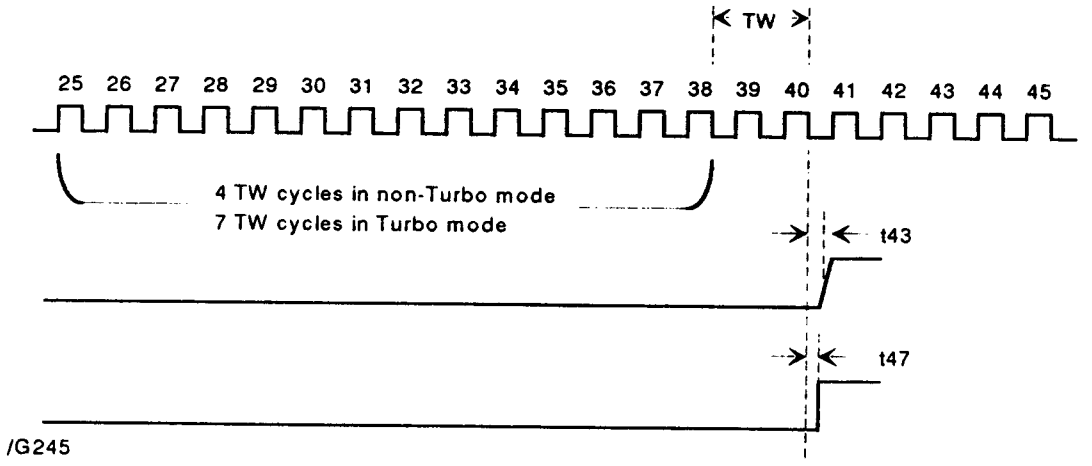


AC Specifications

Symbol	Description	Min	Max	Unit
t42	Conversion cycle command active from CLK286 delay		37	ns
t43	Conversion cycle command inactive from CLK286 delay		37	ns
t44	L374 active from CLK286 delay		50	ns
t45	L374 INACTIVE from CLK286 delay		50	ns
t46	/G245 active from CLK286 delay		60	ns
t47	G245 inactive from CLK286 delay		60	ns

Conversion Cycle /G245, L374 Timing

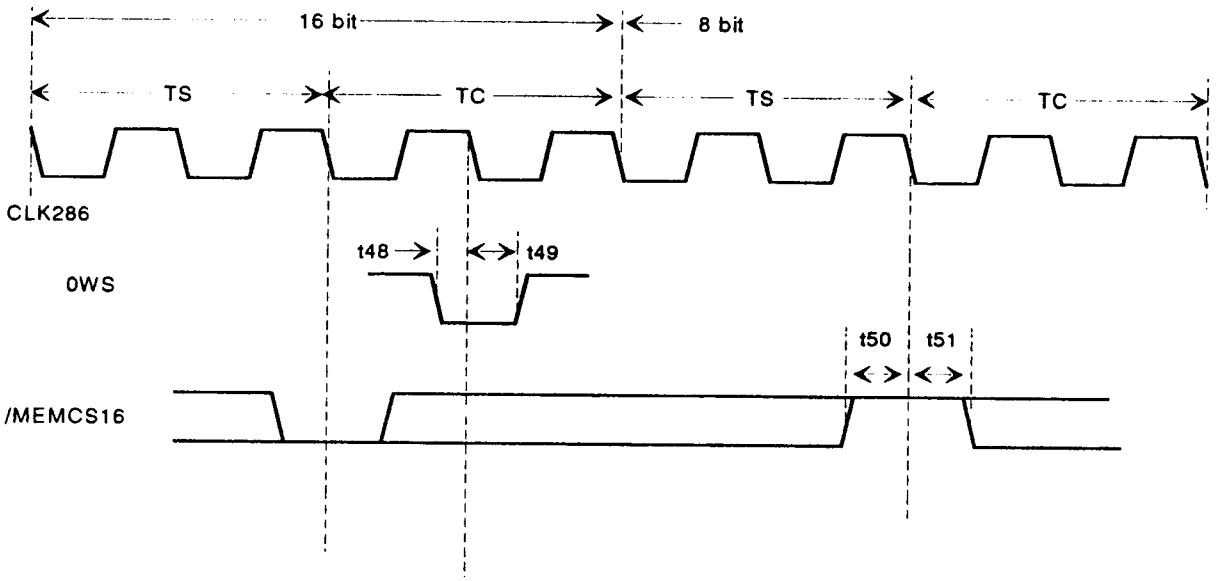


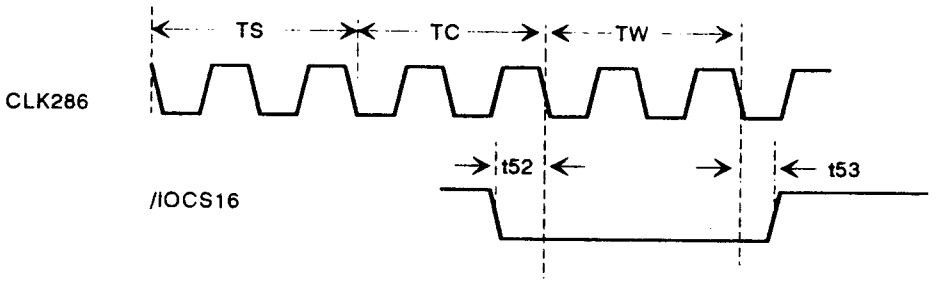


AC Specifications

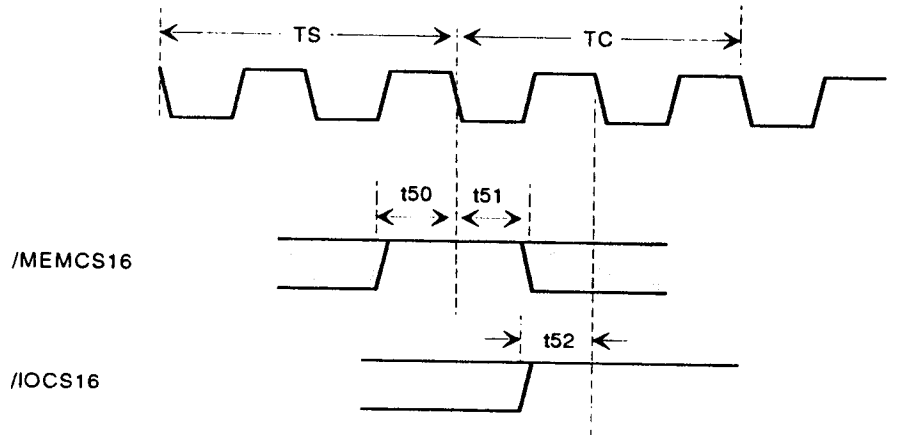
Symbol	Description	Min	Max	Unit
t48	0WS set up time from CLK286 delay	15		ns
t49	0WS hold time from CLK286 delay	2		ns
t50	/MEMCS16 set up time from CLK286 delay	15		ns
t51	/MEMCS16 hold time from CLK286 delay	2		ns
t52	/IOCS16 set up time from CLK286 delay	17		ns
t53	/IOCS16 hold time from CLK286 delay	2		ns

Off-Board Memory Access /MEMCS16 Timing



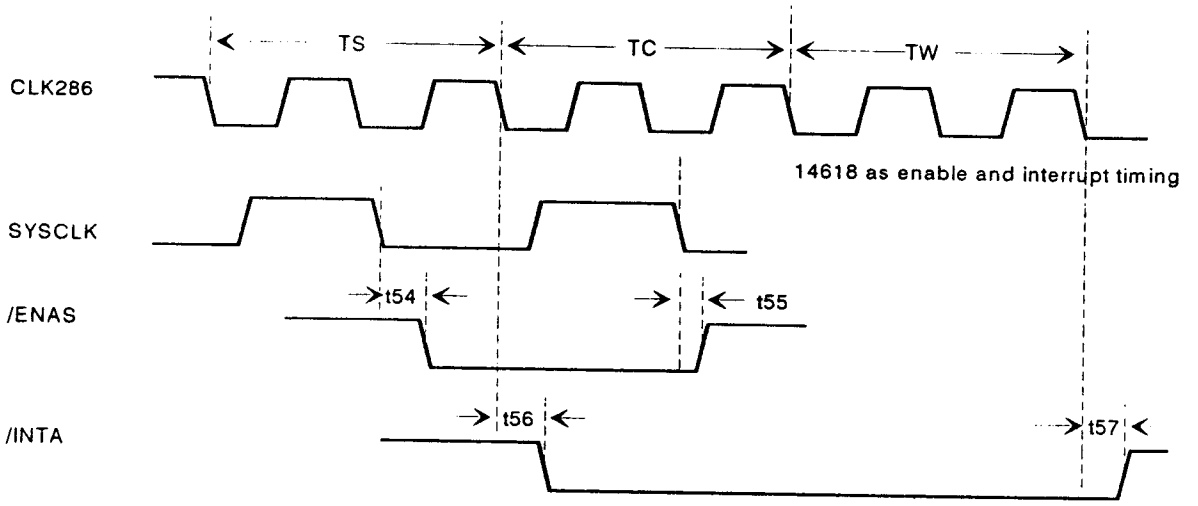


/MEMCS16 and /IOCS16 Timing in Conversion Cycle

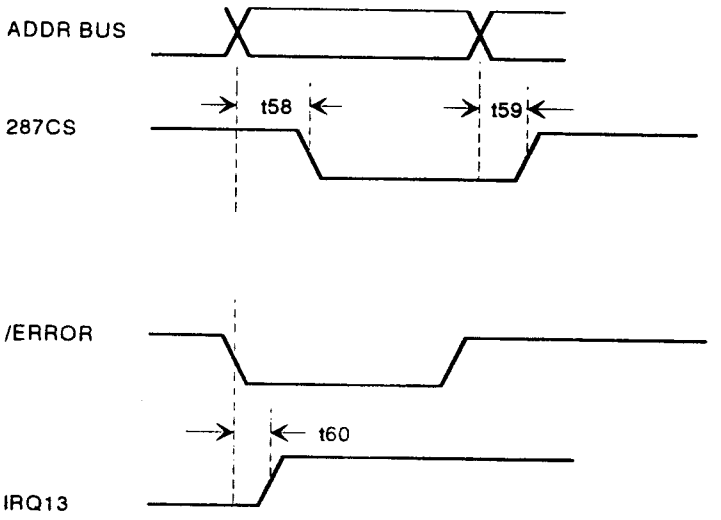


AC Specifacations

Symbol	Description	Min	Max	Unit
t54	/ENAS active from SYSCLK delay		35	ns
t55	/ENAS inactive from SYSCLK delay		35	ns
t56	/INTA active from CLK286 delay		30	ns
t57	/INTA inactive from CLK286 delay		30	ns
t58	287CS active from address valid delay		60	ns
t59	287CS inactive from address invalid delay		60	ns
t60	/IRQ high from /ERROR delay		44	ns



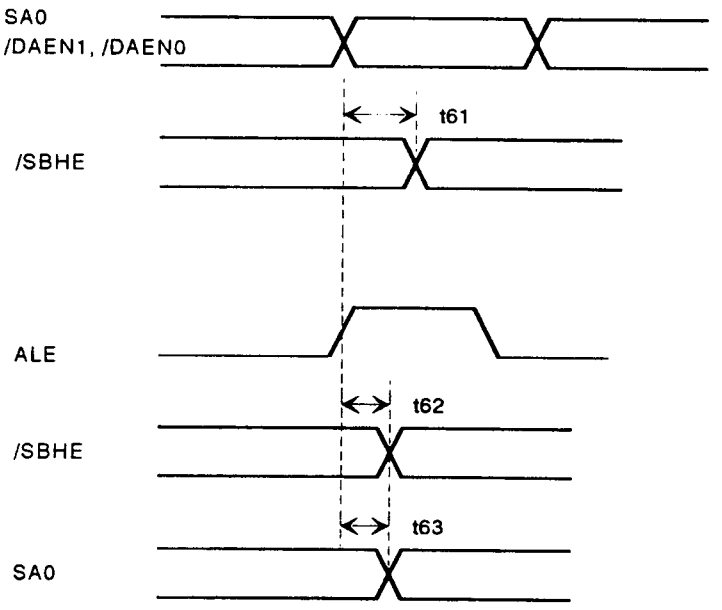
Numerical Processor Chip Select Timing



AC Specifications

Symbol	Description	Min	Max	Unit
t61	/SBHE delay from SA0, /DAEN1 or /DAEN2		28	ns
t62	/SBHE from ALE high delay		30	ns
t63	SA0 from ALE high delay		30	ns

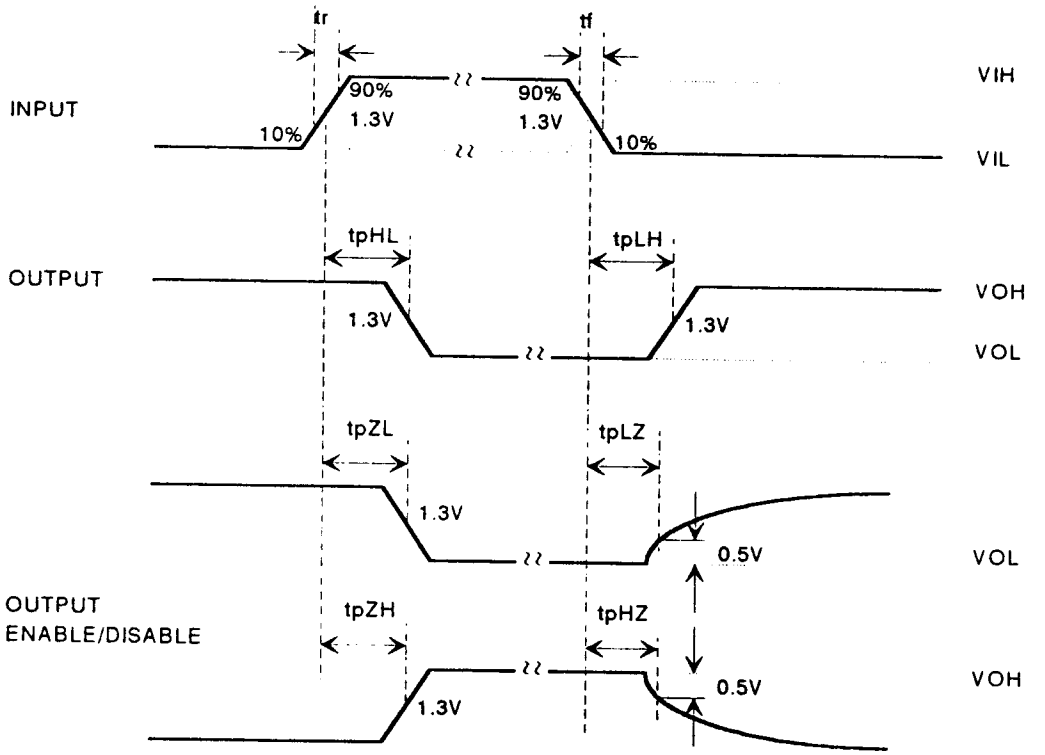
/SBHE Timing



Load Circuit and AC Characteristics Measurement

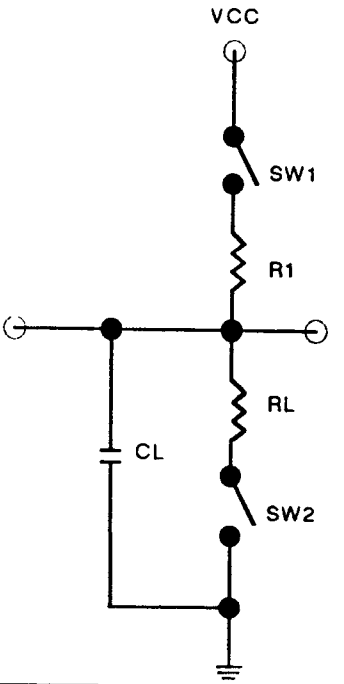
Parameter	Output Type	Symbol	CL(pF)	R1	RL	SW1	SW2
Propagation Delay Time	Totem pole 3-state Bidirectional	tPLH	50		1.0K	off	on
		tPHL	50		1.0K	off	on
Propagation Delay time	Open drain or Open collection	tPLH	50	0.5K		on	off
		tPHL	50	0.5K		on	off
Disable time	3-state Bidirectional	tPLZ	5	0.5K	1.0K	on	on
		tPHZ	5	0.5K	1.0K	off	on
Enable time	3-state Bidirectional	tPZL	50	0.5K	1.0K	on	on
		tPZH	50	0.5K	1.0K	off	on

AC Characteristics Measurement



VIH = 3 V, VIL = 0, tr ≤ 10 ns, tf ≤ 5 ns

Load Circuit



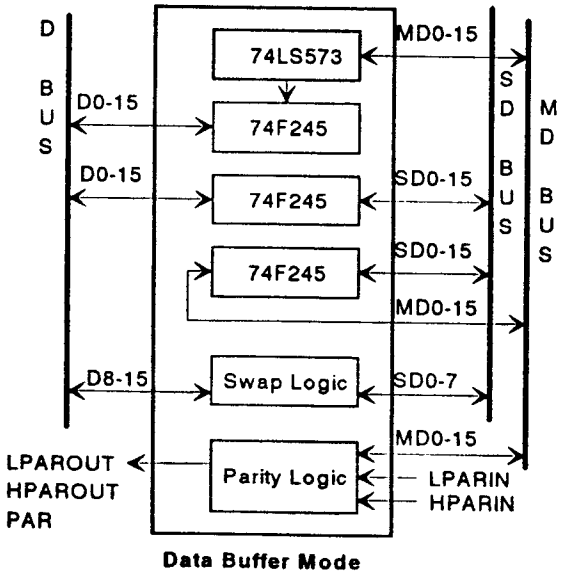
ACC 2220
PC/AT Integrated Data & Address Buffers

The ACC 2220 is a high performance buffer chip, running in two different modes. It activates the data buffers and latches mode when pin 25 is asserted low and the address buffers and latches mode when pin 25 is asserted high.

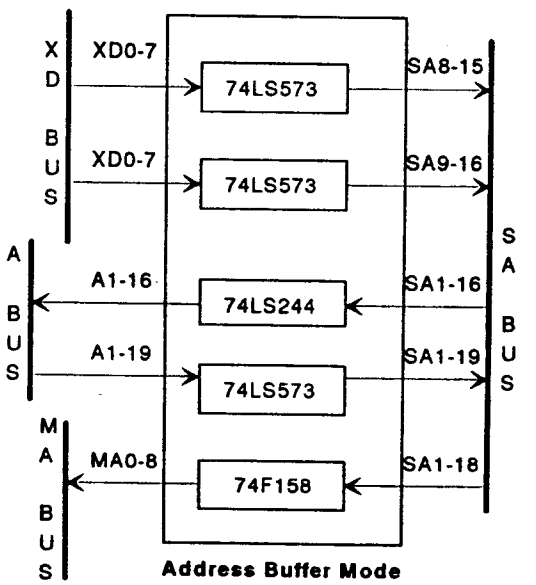
Features

- 100% hardware and software compatible to the IBM AT
- Data buffers and latches mode
- Address buffers and latches mode
- Built-in parity generation/detection logic
- Built-in bus conversion logic for 16-bit to 8-bit transfers
- Supports direct high drive for expansion slots
- 1.5 micron high performance CMOS technology
- TTL compatible
- 84-L PLCC package

Block Diagram



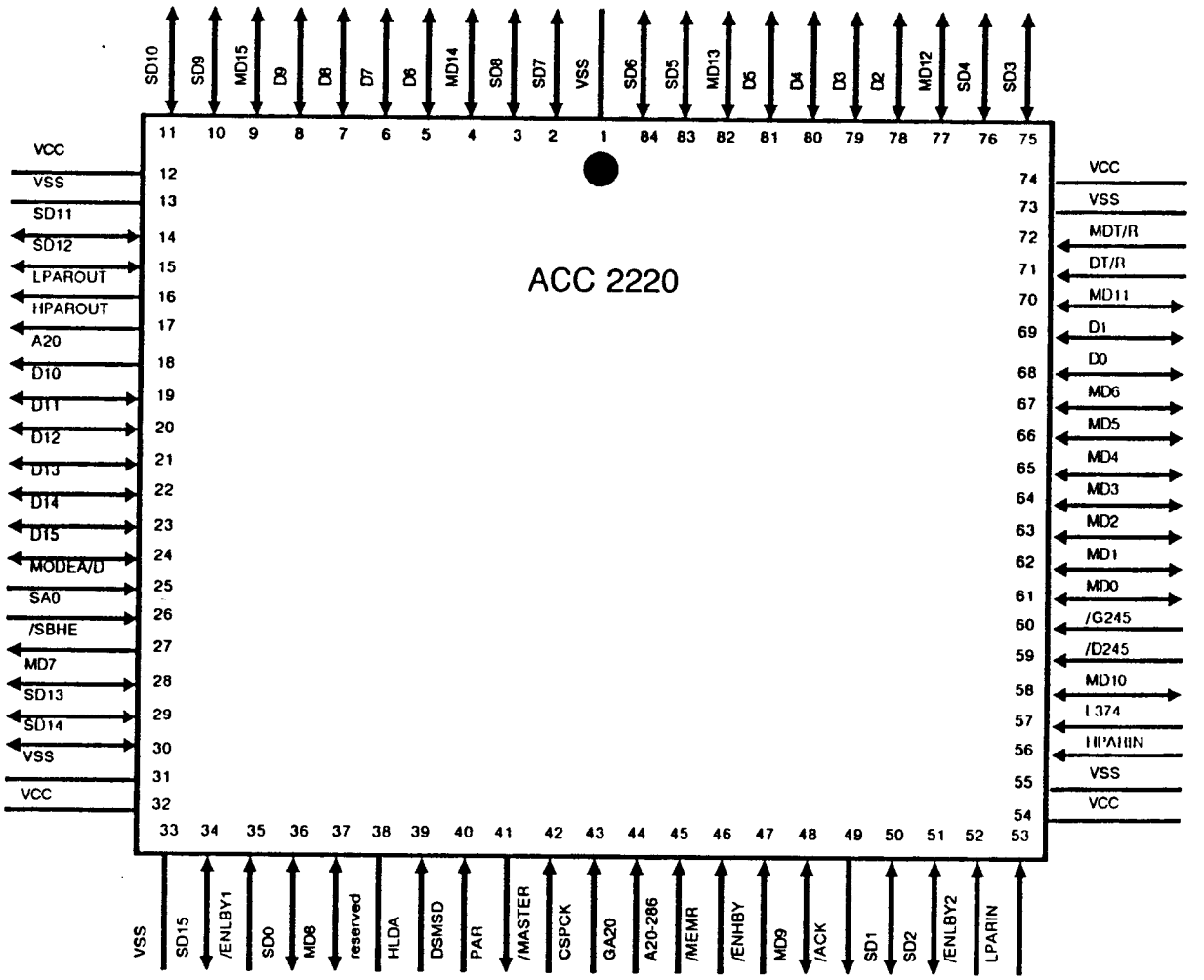
Data Buffer Mode



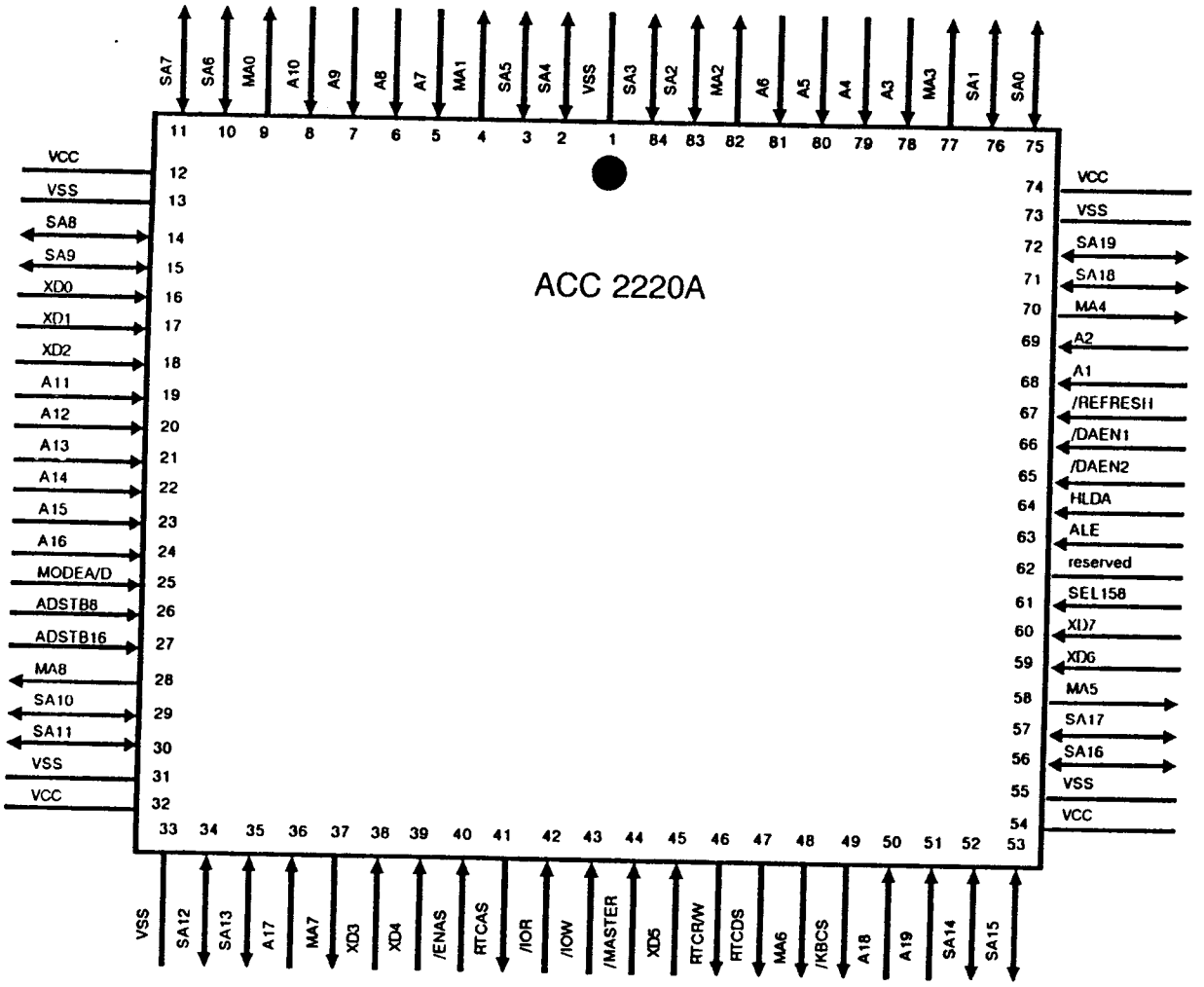
Address Buffer Mode

ACC Microelectronics Corporation · 3295 Scott Blvd. · Santa Clara, CA 95054
Phone: 408-980-0622 FAX: 408-980-0626

Pin Diagram (ACC 2220 Data Buffer Mode)



Pin Diagram (ACC 2220 Address Buffer Mode)



ACC 2220 Pin Descriptions - Data Buffer Mode

Symbol	Pin	I/O	Pin Description
SD0	36	I/O	System data bus bit.
SD1	50		
SD2	51		
SD3	75		
SD4	76		
SD5	83		
SD6	84		
SD7	2		
SD8	3		
SD9	10		
SD10	11		
SD11	14		
SD12	15		
SD13	29		
SD14	30		
SD15	34		
MD0	61	I/O	Memory data bus bit.
MD1	62		
MD2	63		
MD3	64		
MD4	65		
MD5	66		
MD6	67		
MD7	28		
MD8	37		
MD9	48		
MD10	58		
MD11	70		
MD12	77		
MD13	82		
MD14	4		
MD15	9		
LPAROUT	16	O	Low parity bit output.
HPAROUT	17	O	High parity bit output.
/SBHE	27	I	System bus high enable. Active low.
A20	18	O	CPU address bus Bit 20.
MODEA/D	25	I	Address (high) / Data mode select (low).
SA0	26	I	System address bus Bit 0.

ACC 2220 Pin Descriptions - Data Buffer Mode

Symbol	Pin	I/O	Pin Description
D0	68	I/O	CPU data bus bit.
D1	69		
D2	78		
D3	79		
D4	80		
D5	81		
D6	5		
D7	6		
D8	7		
D9	8		
D10	19		
D11	20		
D12	21		
D13	22		
D14	23		
D15	24		
/ENLBY1	35	I	System data bus to local data bus low byte output enable (active low). Used for 8-bit I/O port or extension memory read.
HLDA	39	I	Hold acknowledge.
DSMSD	40	I	Memory data / System data bus disable.
PAR	41	O	Memory parity error.
/MASTER	42	I	External master. Active low.
CSPCK	43	I	Parity check enable.
GA20	44	I	Protect mode A20 select. Active high.
A20-286	45	I	80286 address bus Bit 20.
/MEMR	46	I	Memory read. Active low.
/ENHBY	47	I	System /Local data bus (CSPCK=0) or Memroy/Local data bus (CSPCK=1) high byte transfer enable. Active low.
/ENLBY2	52	I	System /Local data bus (CSPCK=0) or Memory/Local data bus (CSPCK=1) low byte transfer enable. Active low.
/ACK	49	O	Bus hold acknowledge. Active low.

ACC 2220 Pin Descriptions - Data Buffer Mode

Symbol	Pin	I/O	Pin Description
LPARIN HPARIN	53 56	I I	Low parity bit input. High parity bit input.
L374	57	I	Clock input for the data bus to local data bus low byte latch.
/D245	59	I	System data bus byte swap direction high-to-low (high) /low-to-high (low).
/G245	60	I	System data bus byte swap enable. Active low.
DT/R	71	I	Local data bus to system data bus transmit (high) / receive (low).
MDT/R	72	I	System data bus to memory data bus transmit (high) / receive (low).
VCC	12, 32, 54, 74		+5 volt supply
VSS	1, 13, 31, 33, 55, 73		Ground
Reserved	38		Tied to VCC.

ACC 2220 Pin Descriptions - Address Buffer Mode

Symbol	Pin	I/O	Pin Description
SA0	75	I/O	System address bus bit.
SA1	76		
SA2	83		
SA3	84		
SA4	2		
SA5	3		
SA6	10		
SA7	11		
SA8	14		
SA9	15		
SA10	29		
SA11	30		
SA12	34		
SA13	35		
SA14	52		
SA15	53		
SA16	56		
SA17	57		
SA18	71		
SA19	72		
A1	68	I	CPU address bus bit.
A2	69		
A3	78		
A4	79		
A5	80		
A6	81		
A7	5		
A8	6		
A9	7		
A10	8		
A11	19		
A12	20		
A13	21		
A14	22		
A15	23		
A16	24		
A17	36		
A18	50		
A19	51		

ACC 2220 Pin Descriptions - Address Buffer Mode

Symbol	Pin	I/O	Pin Description
MA0	9	O	Memory address bus bit.
MA1	4		
MA2	82		
MA3	77		
MA4	70		
MA5	58		
MA6	48		
MA7	37		
MA8	28		
XD0	16	I	Peripheral data bus bit.
XD1	17		
XD2	18		
XD3	38		
XD4	39		
XD5	45		
XD6	59		
XD7	60		
MODEA/D	25	I	Address/data buffer mode select.
ADSTB8	26	I	Byte transfer DMA high address strobe.
ADSTB16	27	I	Word transfer DMA high address strobe.
/ENAS	40	I	REAL_TIME_CLOCK address strobe enable. Actve low.
RTCAS	41	O	REAL_TIME_CLOCK multiplexed address strobe. The falling edge causes the address to be latched in 146818.
/IOR	42	I	I/O read. Active low.
/IOW	43	I	I/O write. Active low.
/MASTER	44	I	External master. Active low.
RTCR/W	46	O	REAL_TIME_CLOCK read/write.
RTCDS	47	O	REAL_TIME_CLOCK data strobe or read. Identifies the time period when the REAL_TIME_CLOCK and RAM drive the bus with read data.
KBCS	49	O	Keyboard chip select. Active low.

ACC 2220 Pin Descriptions - Address Buffer Mode

Symbol	Pin	I/O	Pin Description
SEL158	61	I	System address bus to memory column address select. Active high.
ALE	63	I	Address latch enable.
HLDA	64	I	Hold acknowledge.
/DAEN2	65	I	Word transfer DMA address output enable.
/DAEN1	66	I	Byte transfer DMA address output enable.
/REFRESH	67	I	Memory refresh.
VCC	12, 32, 54, 74		+5 volt supply
VSS	13, 31, 33, 55, 73		Ground
Reserved	62		Tied to VCC

Functional Description

ACC 2220 Data Buffer Mode

When the MODEA/D pin is set to low, the ACC 2220 operates in DATA Mode. In this mode, the ACC 2220 consists of 48 data bus (D BUS, SD BUS, and MD BUS) drivers, each capable of sinking 4 or 16 MA of current, and two parity generators for high byte and low byte memory data. The parity detection logic generates the parity error signal for the system. The bus conversion logic works in conjunction with the ACC 2100 performing 16-bit to 8-bit transfers.

Data Buffers and Latches

The primary function of the Data Buffer is multiplexing the iAPX286 microprocessor data lines (D0 - D15) to the System Data Bus (SD0 - SD15) and the Memory Data Bus (MD0-MD15). The data is latched from the System Data Bus to the CPU or Local Data Bus direction only.

Bus Conversion Logic

When the 16-bit CPU reads from or writes to an 8-bit device, the ACC 2100 sends control signals /D245 and /G245 to the ACC 2220. The ACC 2220 then performs the bus conversion.

Parity Generation/Detection Logic

The ACC 2220 provides data parity generator/checker logic. All data on the Memory Data Bus passes through the parity logic. If an error is detected, the PAR signal is fed back to the ACC 2000 to generate an NMI to the CPU.

ACC 2220 Address Buffer Mode

When the MODEA/D pin is set to high, the ACC 2220 operates in ADDRESS Mode. The ACC 2220 consists of 28 address bus (SA BUS and MA BUS) drivers, each capable of sinking 16MA of current and the logic to provide control signals to the real time clock.

Address Buffers and Latches

The primary function of the Address Buffer is multiplexing the iAPX 286 microprocessor address lines (A1 - A19) to the System Address Bus (SA1 - SA19) and the Memory Address Bus (MA0 - MA8). The System Address Bus (SA0-SA19) is shared by the coprocessor, ROM memory, the DMA controller in the ACC 2000 and the expansion slots.

Real Time Clock Control Signals

The ACC 2220 provides data strobe (RTCDS), read/write (RTCR/W) and address strobe (RTCAS) to 146818.

Rating Specifications

Absolute Maximum Ratings*

Parameter	Symbol	Min	Max	Units
Power supply voltage	VCC	0	7.0	V
Power dissipation (@5.25 V)	Wd		1	W
Current (@5.25 V)	IDD	20	50	mA
Input voltage	VI	0.0	5.5	V
Output voltage	VO	0.0	5.5	V
Operating temperature	Top	0	70	°C
Storage temperature	Tstg	-50	150	°C

* Exposing the device to stress above these can cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Capacitance Limits

TA = +25° C, VCC = 5 V

Parameter	Symbol	Min	Max	Unit	Test Condition
Input capacitance	CI		10	pF	fc = 1 MHz unmeasured pins at GND
I/O capacitance	CIO		15	pF	

DC Specifications

TA = 0° C to +70° C, VCC = +5 V +/- 10%

Pins 25-27, 38-40, 42-45, 59, 60

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 +/- 0.5 V
Input low current	IIL		-1.0	uA	VIN = 0.0V
Input high current	IIH		1.0	uA	VIN = VCC

Pins 5-8, 16-24, 46, 47, 61-69, 78-81

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 +/- 0.5 V
Input low current	IIL		-1.0	uA	VIN = 0.0V
Input high current	IIH		1.0	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 4mA
Output high voltage	VOH	2.4		V	IOH = -4mA

Pins 2-4, 9-11, 14-15, 28-30, 34-37, 48, 50-53, 56-58, 70-72, 75-77, 82-84

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 +/- 0.5 V
Input low current	IIL		-1.0	uA	VIN = 0.0V
Input high current	IIH		1.0	uA	VIN = VCC
Output low voltage	VOL		0.4	V	IOL = 16mA
Output high voltage	VOH	2.4		V	IOH = -16mA

Pin 41

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 4mA
Output high voltage	VOH	2.4		V	IOH = -4mA

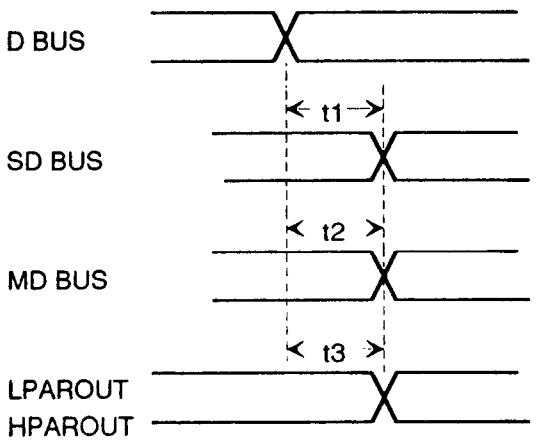
Pin 49

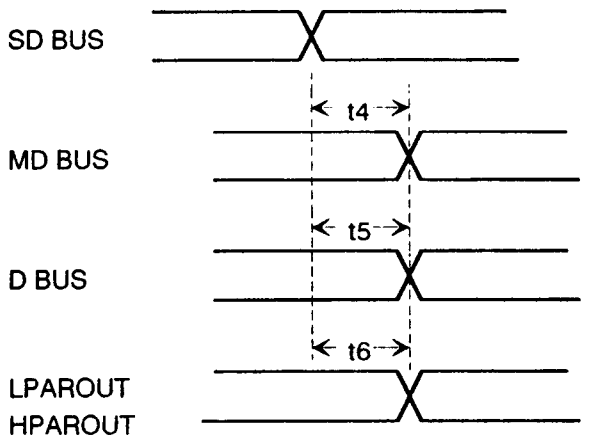
Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 16mA
Output high voltage	VOH	2.4		V	IOH = -16mA

AC Specifications - Data Buffer Mode

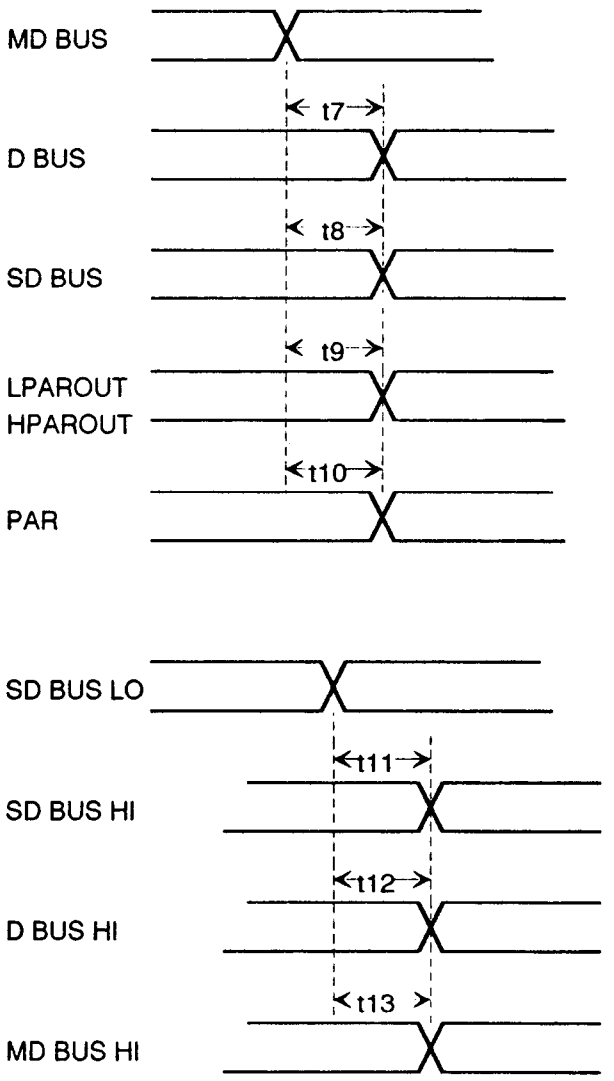
Symbol	Description	Min	Max	Units	Condition
t1	D BUS in to SD BUS out	14	39	ns	CL = 80 pF
t2	D BUS in to MD BUS out	14	33	ns	CL = 80 pF
t3	D BUS in to LPAROUT or HPAROUT (CPU to memory access)	11	41	ns	CL = 80 pF
t4	SD BUS in to MD BUS out	15	33	ns	CL = 80 pF
t5	SD BUS in to D BUS out	15	33	ns	CL = 80 pF
t6	SD BUS in to LPAROUT or HPAROUT (DMA memory access)	11	41	ns	CL = 80 pF
t7	MD BUS in to D BUS out	15	34	ns	CL = 80 pF
t8	MD BUS in to SD BUS out	14	32	ns	CL = 80 pF
t9	MD BUS in to LPAROUT or HPAROUT	13	42	ns	CL = 80 pF
t10	MD BUS in to PAR	13	42	ns	CL = 80 pF
t11	SD BUS low to SD BUS high data out	16	36	ns	CL = 80 pF
t12	SD BUS low to D BUS high data out	24	44	ns	CL = 80 pF
t13	SD BUS low to MD BUS high data out	24	44	ns	CL = 80 pF
t14	LPARIN (or HPARIN) to LPAROUT (or HPAROUT)	18	40	ns	CL = 80 pF
t15	A20 active to GA20 delay	11	41	ns	CL = 80 pF
t16	ACK active to HLDA or MASTER	8	29	ns	CL = 80 p

Data Buffer Timing

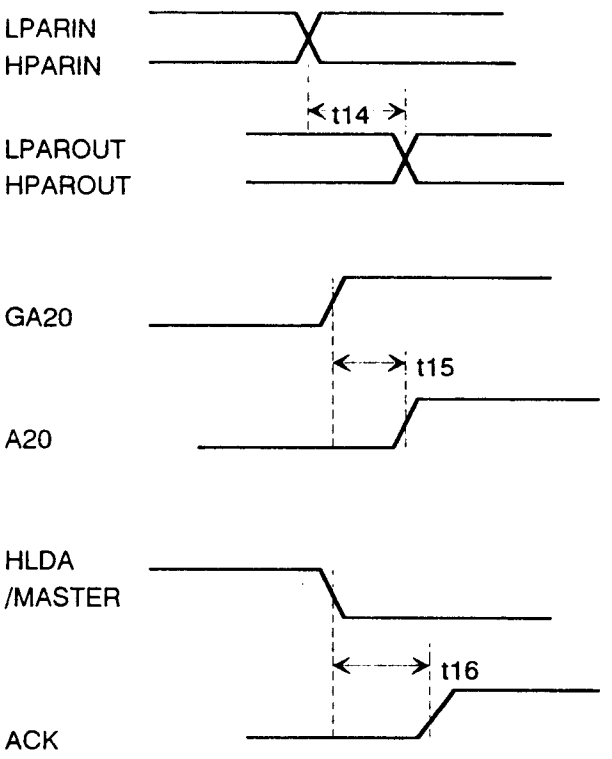




Data Buffer Timing



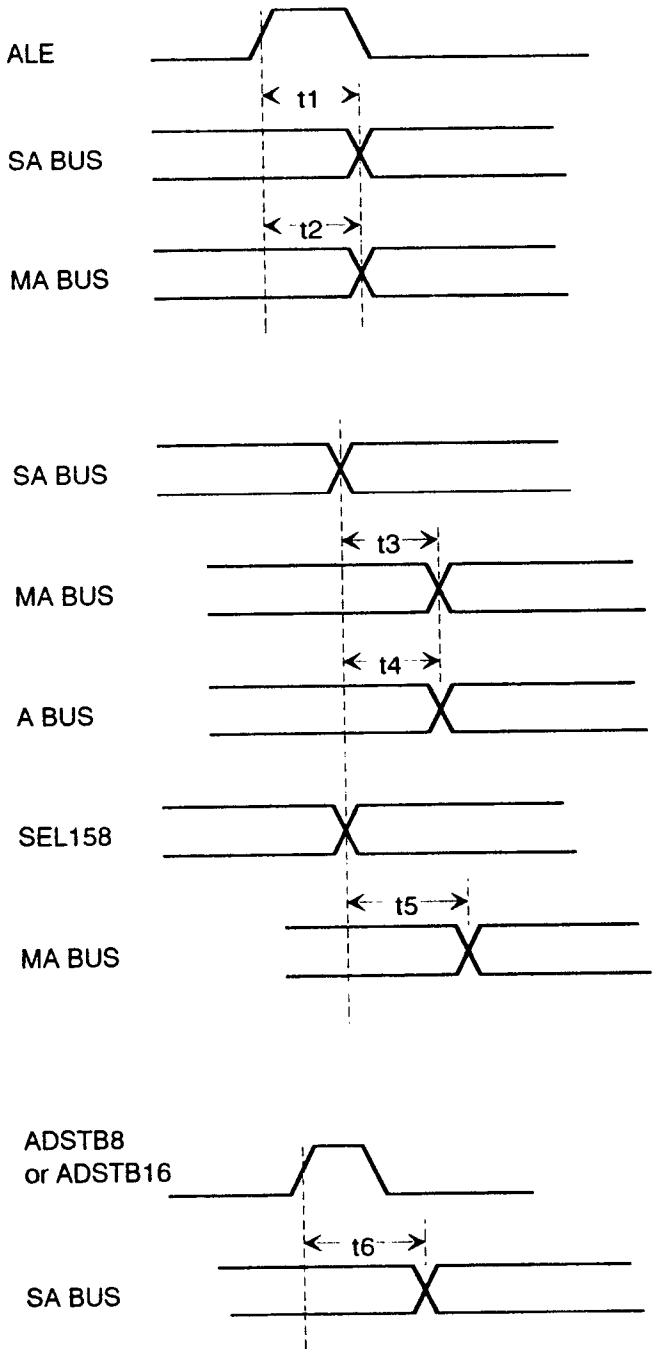
Data Buffer Timing



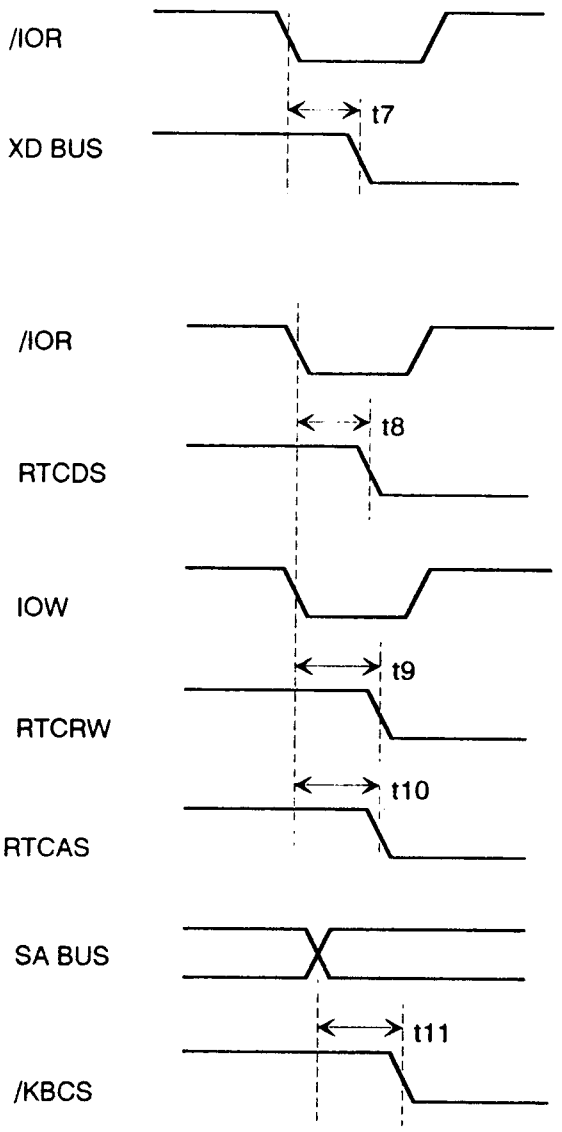
AC Specifications - Address Buffer Mode

Symbol	Description	Min	Typ	Max	Units	Condition
t1	ALE to SA BUS valid address	11	22	40	ns	CL = 200 pF
t2	ALE to MA BUS valid address	10	19	36	ns	CL = 160 pF
t3	SA BUS in to MA BUS out	8	15	28	ns	CL = 160 pF
t4	SA BUS in to A BUS out in master mode	9	17	31	ns	CL = 80 pF
t5	Address select to MA BUS out	8	15	28	ns	CL = 160 pF
t6	ADSTB8 (or ADSTRB16) to SA BUS valid address	11	21	39	ns	CL = 200 pF
t7	/IOR to XDOUT (Read config Reg 0F3H)	12	23	43	ns	CL = 80 pF
t8	/IOR to RTCDS	8	15	28	ns	CL = 80 pF
t9	/IOW to RTCR/W	8	15	28	ns	CL = 80 pF
t10	IOW to RTCAS	5	10	18	ns	CL = 80 pF
t11	SA BUS valid address to /KBCS	7	14	26	ns	CL = 80 pF
t12	CPU address valid to chip select output (/CSFLOP, /CSSER, /CSPAR, /CSHDISK) and XDENABLE	9	17	31	ns	CL = 80 pF

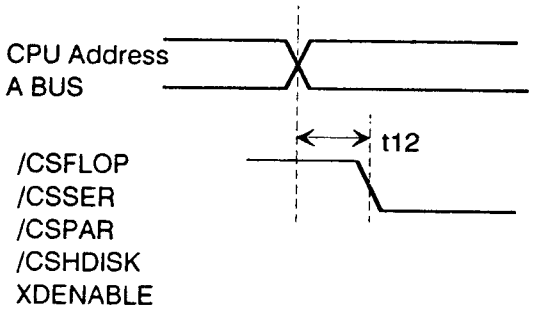
Address Buffer Timing



Address Buffer Timing



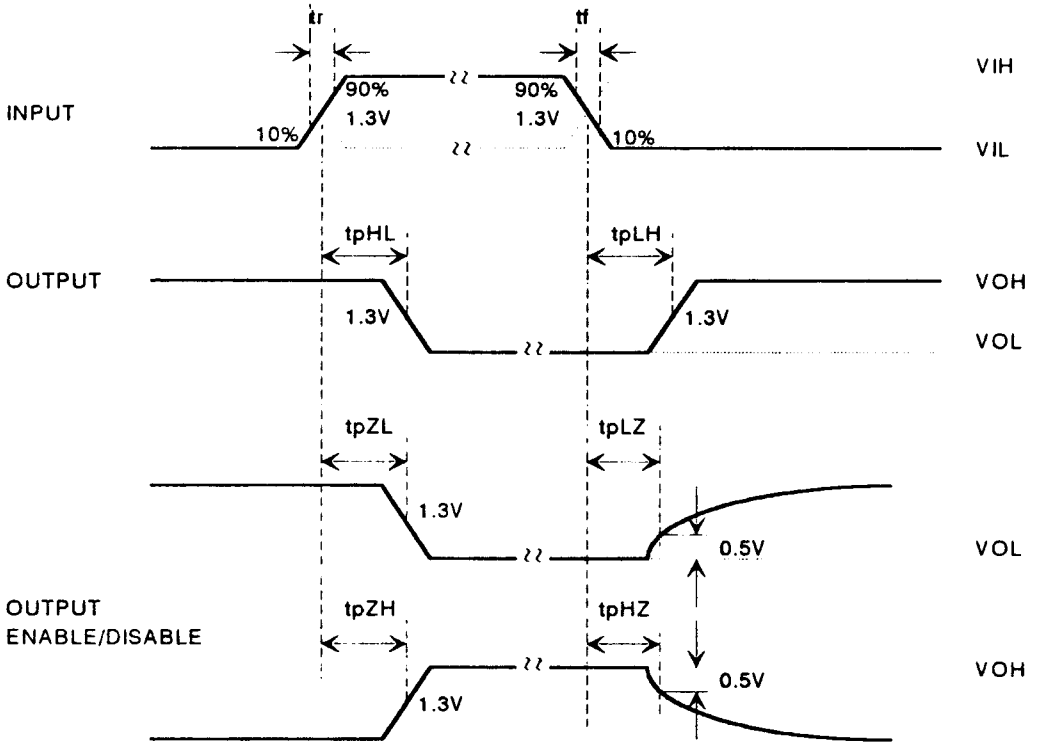
Address Buffer Timing



Load Circuit and AC Characteristics Measurement

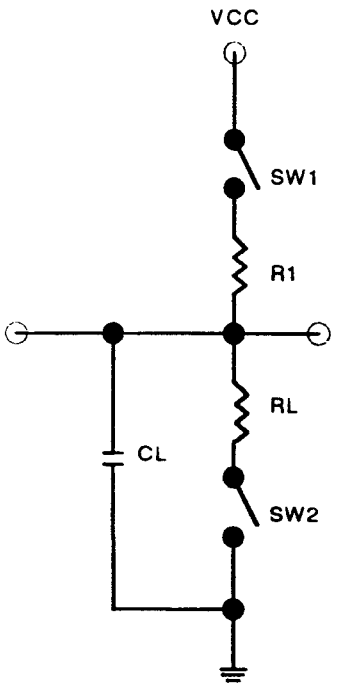
Parameter	Output Type	Symbol	CL(pF)	R1	RL	SW1	SW2
Propagation Delay Time	Totem pole 3-state	tPLH	50		1.0K	off	on
		tPHL	50		1.0K	off	on
	Bidirectional						
Propagation Delay time	Open drain or Open collection	tPLH	50	0.5K		on	off
		tPHL	50	0.5K		on	off
Disable time	3-state Bidirectional	tPLZ	5	0.5K	1.0K	on	on
		tPHZ	5	0.5K	1.0K	off	on
Enable time	3-state Bidirectional	tPZL	50	0.5K	1.0K	on	on
		tPZH	50	0.5K	1.0K	off	on

AC Characteristics Measurement



VIH = 3 V, VIL = 0, tr ≤ 10 ns, tf ≤ 5 ns

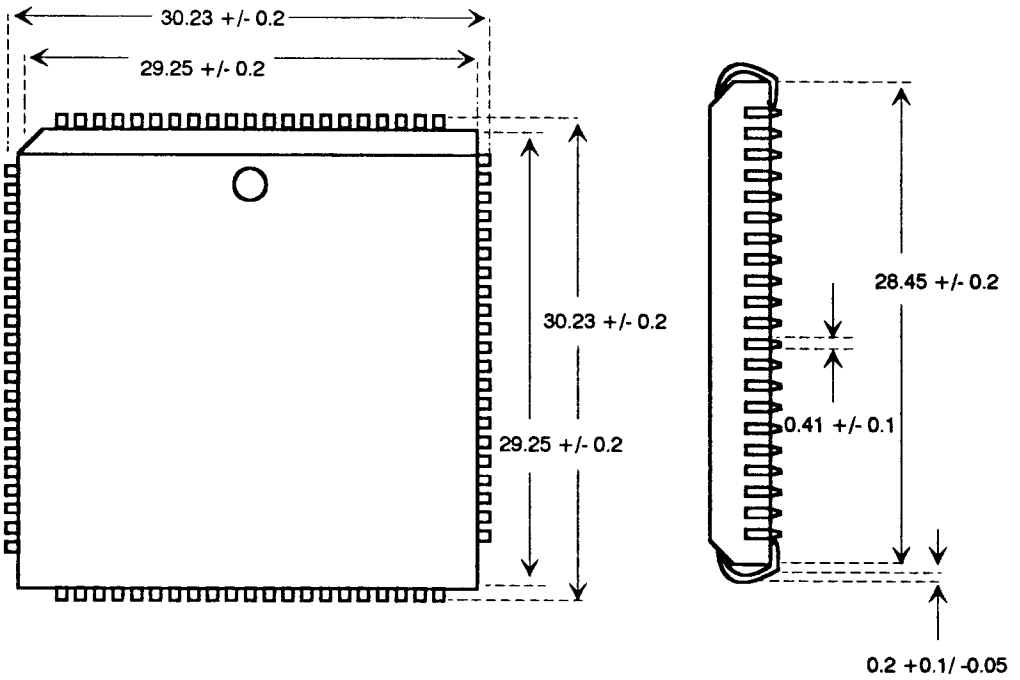
Load Circuit

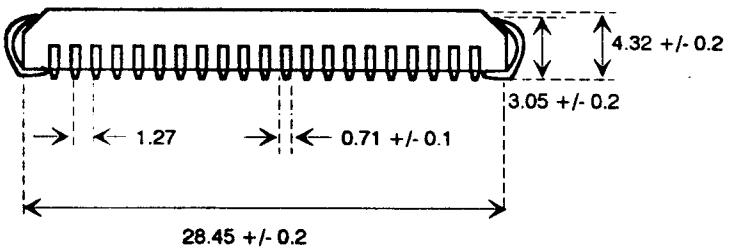


Production Package Specification

Package: 84-pin PLCC
Unit: mm

Chip: ACC 2000, ACC 2100, ACC 2220





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