ACC 1000

Turbo PC/XT
Integrated Bus and Peripheral Controller

Advance Information

(Rev. A)

April 2, 1988

ACC 1000
Turbo PC/XT Integrated Bus & Peripheral Controller

The ACC 1000 is a high performance CMOS PC/XT* bus and peripheral controller for designers to build a PC BUS-compatible single-board computer with "turbo" power. The ACC 1000 replaces most TTL/SSI/MSI devices including six Intel peripheral controller ICs required to build a typical "Turbo XT." The LED output which indicates running frequency is supported by the ACC 1000. The ACC 1000 integrates all the controller functions of a typical "Turbo/XT" high performance motherboard. This high integration not only increases system performance but also reduces the total system cost because of lower power requirements, increased reliability, and reduced components and board size.

Features

- 100% hardware and software compatible with IBM* PC/XT
- Fully compatible with Intel's

  8284 Clock Generator
  8288 Bus Controller
  8237 DMA Controller
  8259 Interrupt Controller
  8254 Timer/Counter
- 8255 compatible peripheral I/O port
- Built-in parity generator and checker, wait state logic, and NMI control logic
- Built-in ROM decoder for 2764/27256
- Built-in RAM decoder for 4164/41256
- Supports both 9.54 MHz and 4.77 MHz system clock with a single common crystal
- System clocks switchable by both software and hardware on the fly
- Keyboard Interface
- Memory Controller
- Supports LED output to indicate running frequency
- 640K total memory support
- 1.5 micron high performance CMOS technology
- TTL compatible
- 84-L PLCC package

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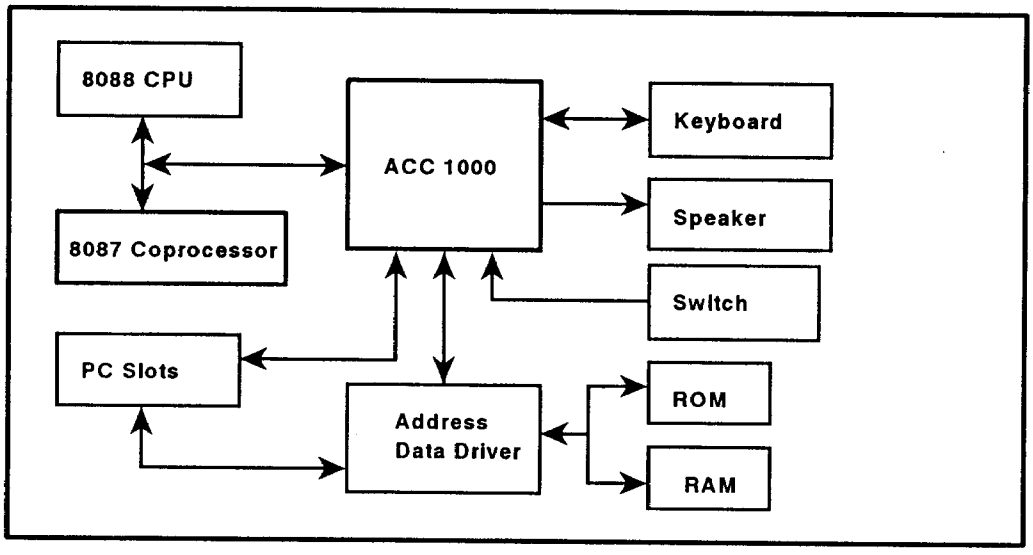
ACC Miroelectronics Corporation · 3295 Scott Blvd. · Santa Clara, CA 95054
Phone: 408-980-0622 FAX: 408-980-0626

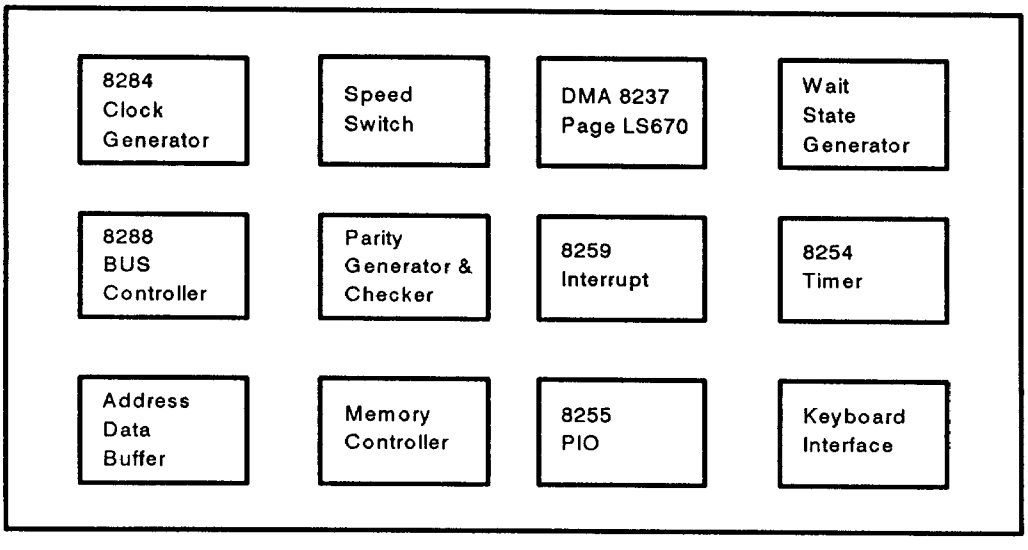
System Configuration

A typical PC/XT compatible system using the ACC 1000 is shown below.

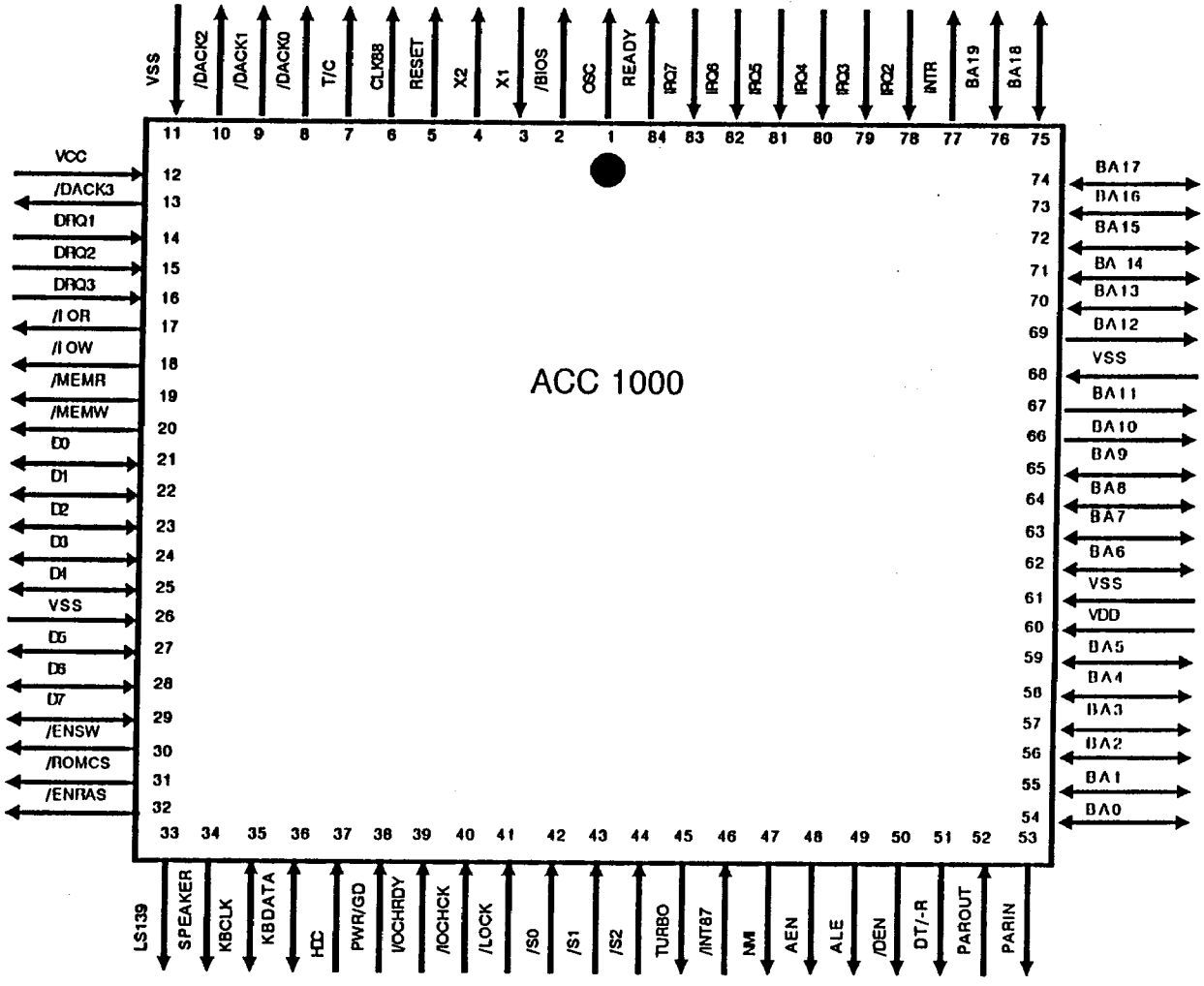


Functional Blocks

The functional blocks of the ACC 1000 are shown below.



Pin Diagram


ACC 1000
VSS 11
/DACK2 10
/DACK1 9
/DACK0 8
T/C 7
CLK88 6
RESET 5
X2 4
X1 3
/BIOS 2
OSC 1
READY 84
IRQ7 83
IRQ6 82
IRQ5 81
IRQ4 80
IRQ3 79
IRQ2 78
INTR 77
BA19 76
BA18 75
VCC 12
/DACK3 13
DRQ1 14
DRQ2 15
DRQ3 16
/I OR 17
/I OW 18
/MEMR 19
/MEMW 20
D0 21
D1 22
D2 23
D3 24
D4 25
VSS 26
D5 27
D6 28
D7 29
/ENSW 30
/ROMCS 31
/ENRAS 32
BA17 74
BA16 73
BA15 72
BA 14 71
BA13 70
BA12 69
VSS 68
BA11 67
BA10 66
BA9 65
BA8 64
BA7 63
BA6 62
VSS 61
VDD 60
BA5 59
BA4 58
BA3 57
BA2 56
BA1 55
BA0 54
LS139 33
SPEAKER 34
KBCLK 35
KBDATA 36
HD 37
PWR/GD 38
/OCHRDY 39
/OCHCK 40
/LOCK 41
/S0 42
/S1 43
/S2 44
TURBO 45
/INT87 46
NM 47
AEN 48
ALE 49
/DEN 50
DT/-R 51
PAROUT 52
PARIN 53

Pin Descriptions

Symbol	Pin	I/O	Pin Description
OSC	1	O	OSC to expansion bus, NOT crystal frequency. 14.31818 MHz clock (crystal frequency / 2).
/BIOS	2	O	Output enable signal for ROM 2764. Top 8K decode (FE000 to FFFFF). Active low.
X1	3	I	28.63636 MHz fundamental crystal in, or single phase. TTL level clock.
X2	4	O	Crystal output. Not used when the TTL level clock is input as X1.
RESET	5	O	System reset.
CLK88	6	O	System clock.
T/C	7	O	Terminal count pulse when the DMA channel is reached.
/DACK0	8	O	DMA acknowledge for Channel 0. Indicates a refresh cycle. Active low.
/DACK1	9	O	DMA acknowledge of Channel 1. Active low.
/DACK2	10	O	DMA acknowledge of Channel 2. Active low.
/DACK3	13	O	DMA acknowledge of Channel 3. Active low.
DRQ1	14	I	DMA request line. Active high.
DRQ2	15		
DRQ3	16		
/IOR	17	O	I/O read. Active low.
/IOW	18	O	I/O write. Active low.
/MEMR	19	O	Memory read. Active low.
/MEMW	20	O	Memory write. Active low.
D0	21	I/O	Data bus bit.
D1	22		
D2	23		
D3	24		
D4	25		
D5	27		
D6	28		
D7	29		

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/ENSW	30	O	Enable signal to load switch settings to DBUS.
/ROMCS	31	O	ROM chip select.
/ENRAS	32	O	RAS enable.
LS139	33	O	Input for RAS and CAS decode.
SPEAKER	34	O	Speaker output.
KBCLK	35	I/O	Keyboard clock disable and enable. "0" to disable keyboard input clock.
KBDATA	36	I/O	Keyboard data disable and enable signal. Active high.
HDC	37	I	System clock switch. Selects either 9.54 MHz (high) or 4.77 MHz (low) system clock.
PWR/GD	38	I	Power good to generate reset.
IOCHRDY	39	I	I/O channel ready.
/IOCHCK	40	I	Error from expansion bus. Active low.
/LOCK	41	I	System bus lock by CPU.
/S0 /S1 /S2	42 43 44	I	8088 CPU status bit.
TURBO	45	O	Turbo or Normal mode indicator. Turbo: TURBO = 1 ; Normal: TURBO = 0
/INT87	46	I	Unmasked exception during numeric instruction execution when 8087 coprocessor interrupts are enabled.
NMI	47	O	Non-maskable interrupt to 8088 CPU. Active high. NMI generated by 8087, memory parity error, or error from bus (/IOCHCK).
AEN	48	O	System address enable.
ALE	49	O	Address latch enable. Active high.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/DEN	50	O	Data enable to transceiver for local or system bus. Active low.
DT/-R	51	O	Data transmit or receive. Active high. Signal to data transceiver indicating a write cycle.
PAROUT	52	I	Parity bit input for DRAM.
PARIN	53	O	Parity bit output from DRAM.
BA0	54	I/O	Address bus bit.
BA1	55	I/O	
BA2	56	I/O	
BA3	57	I/O	
BA4	58	O	
BA5	59	O	
BA6	62	O	
BA7	63	O	
BA8	64	I/O	
BA9	65	I/O	
BA10	66	O	
BA11	67	O	
BA12	69	O	
BA13	70	I/O	
BA14	71	I/O	
BA15	72	I/O	
BA16	73	I/O	
BA17	74	I/O	
BA18	75	I/O	
BA19	76	I/O	
INTR	77	O	Interrupt to 8088 CPU. Active high.
IRQ2	78	I	Interrupt request input. Active high.
IRQ3	79		
IRQ4	80		
IRQ5	81		
IRQ6	82		
IRQ7	83		
READY	84	O	Ready to 8088 CPU. Active high.
VCC	12, 60		+5 volt supply
VSS	11, 26, 61, 68		Ground

Functional Description

Interrupt Controller

The programmable interrupt controller in the ACC 1000 functions as a system-wide interrupt manager for a Turbo XT system. It is compatible to an Intel 8259A interrupt controller. It controls which I/O device is serviced by the microprocessor and when it is serviced.

The ACC 1000 interrupt controller has the following features:

- Eight level priority controller
- Programmable base vector address
- Programmable interrupt modes (algorithms)
- Compatible with the 8088

Wait State Generator

When the system clock runs at 4.77 MHz, the wait state generator generates one wait state for all CPU I/O and DMA operations. When system clock is 9.54 MHz, the wait state generator inserts 4 wait states for all CPU I/O operations and 2 wait states for all DMA operations. It also synchronizes the external ready signal (IOCHRDY) that generates wait states for slower I/O devices.

No wait state is inserted for on board memory access. When the system clock runs at turbo speed (9.54 MHz), one wait state is inserted for memory access on the expansion slots (address range C000H to EFFFH).

Mode Controller

The system clock can be switched by either software or hardware.

The software user can program Bit 2 in Port B of the 8255 to select the system clock. When Bit 2 is programmed HIGH, it operates in "turbo" mode. The hardware user can use a button key or a jumper to the HDC signal to select the appropriate mode. If the HDC signal is generated with a rising edge trigger, it is set in TURBO mode; with a falling edge, it is set in NORMAL mode.

Software and hardware control are independent. The system is always set to the latest setting. At power on, the default mode is TURBO mode.

Clock Generator

The clock generator is the functional equivalent of an 8284 generator. It also generates the clock for the timer.

The clock generator has the following features:

- Generates the system clock for the 8088
- Frequency source can be a crystal or a TTL signal
- TTL output for peripheral devices
- Power up reset for the processor
- READY synchronization

Oscillator Circuit

One oscillator circuit generates the system clock signals. The oscillator is designed to use an external, parallel resonant fundamental mode crystal to generate the basic operating frequency.

The crystal connections for the CPU and video clock are made to Pins X1 and X2. The crystal oscillator frequency must be three or six times the CPU operating frequency (e.g., 28.6 MHz

crystal for a 4.77 MHz or 9.54 MHz CPU). In an IBM PC, a 28.63636 MHz crystal might require a trimmer capacitor that can be adjusted to eliminate unwanted color shifts in video signals. Recommended circuit and crystal specifications for the oscillator are shown in Figure 1.

Bus Controller

The bus controller is the functional equivalent of an 8288 for CPU bus operations. It generates the bus controls for CPU operations.

Parity Generator

The parity generator checks and generates even parity for RAM memory.

Keyboard Port

The keyboard port connects to an IBM compatible keyboard.

DMA

DMA (Direct Memory Access) improves system performance by allowing external devices to transfer information directly from the system memory without CPU intervention. Channel 0 is reserved for RAM memory refresh. The ACC 1000 DMA has the following features:

- Address increment or decrement
- Four independent DMA channels
- Software DMA request. Enable/disable control of individual DMA requests. Independent autoinitialization for all channels.

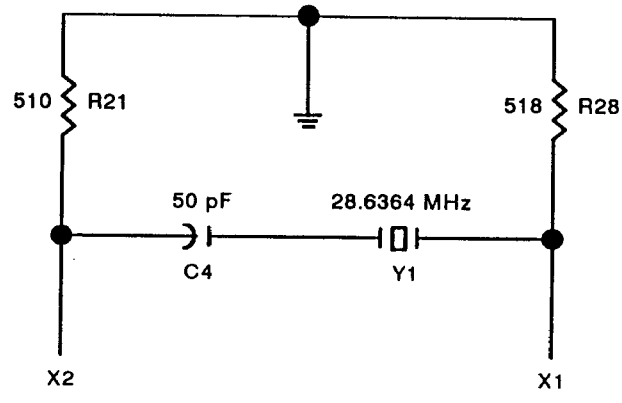


Figure 1 Example Crystal Oscillator Circuit using the ACC 1000

Timer

The timer is the functional equivalent of an 8254 timer. Channel 0 is tied to Interrupt 0. Channel 1 generates refresh. Channel 2 is the speaker port.

The ACC 1000 timer has the following features:

- Three independent 16-bit counters.
- Count binary or BCD

PIO

The PIO is for system configuration, keyboard and speaker port control, and enabling error checks.

Programming

The ACC 1000 accepts I/O read/write commands from the CPU.

I/O Address Map

Address	Use
000-00F	DMA controller
020-021	Interrupt controller
040-043	Timer
060-063	PIO
081-083	DMA page registers
0A0	NMI mask register
100-1FF	Reserved

The timer is programmed like the 8254 timer. The DMA controller is programmed like the 8237 DMA controller, and the interrupt controller is programmed like the 8259 interrupt controller.

PIO

The PIO is the equivalent of the 8255 PIO, but is configured in a fixed way for system configuration, controlling the speaker port, and the keyboard port.

Keyboard Data Register

The keyboard data register is a read only register to read data from the keyboard. When a character is in the register, Interrupt 1 is sent to the interrupt controller. The register can be cleared by setting Bit 7 of the PIO register.

Control Register (061H)

Data Bit	Use
0	Gate speaker timer channel
1	Gate speaker data
2	Switch register select
3	Not used
4	Disable parity check
5	Disable I/O check
6	Enable keyboard clock
7	Clear keyboard data register

Control Register (062H)

Data Bit	PB3 = LOW	PB3 = HIGH
0	Loop on POST	Display 0
1	+Coprocessor installed	Display 1
2	+Planar RAM size 0	#5-1/4 drive 0
3	+Planar RAM size 1	#5-1/4 drive 1
4	Spare	Spare
5	+Timer channel 2 out	+Timer channel 2 out
6	+I/O channel check	+I/O channel check
7	+RAM parity check	+RAM parity check

Command/Mode Register (063H)

	HEX 99
Mode Register Value	7 6 5 4 3 2 1 0
	1 0 0 1 1 0 0 1

Page Registers (081-083H)

The page registers are read/write registers to generate address bits 16-19 during a DMA transfer.

Address	Page Register
81	DMA Channel 2
82	DMA Channel 3
83	DMA Channel 1

Data Bit	Use
0	Address bit 16
1	Address bit 17
2	Address bit 18
3	Address bit 19

NMI Mask Register (0A0H)

The NMI mask register enables the NMI to the CPU (8088).

Data Bit	Use
0-6	Not used
7	Enable NMI

Rating Specifications

Absolute Maximum Ratings*

TA = 25° C

Parameter	Symbol	Min	Max	Units
Power supply voltage	VCC	3.0	7.0	V
Power dissipation (@5.25 V)	Wd	100	265	mW
Current (@5.25 V)	IDD	20	50	mA
Input voltage	VI	0.0	5.5	V
Output voltage	VO	0.0	5.5	V
Operating temperature	Top	0	70	°C
Storage temperature	Tstg	-40	125	°C

* Exposing the device to stresses above those listed can cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Capacitance

TA = +25° C, VCC = 5 V

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Capacitance	CI		10	pF	fc = 1 MHz unmeasured pins at GND
I/O Capacitance	CIO		15	pF	

DC Specifications

TA = 0° C to +70° C, VCC = +5 V +/- 10%

HDC, DRQ1-3, IOCHRDY, IRQ2-7, /IOCHCK, /S0, /S1, /S2, /LOCK, PAROUT, /INT87

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	-0.5	0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 +/- 0.5 V
Input low current	IIL	-10.0	-300.0	uA	VIN = 0.0V
Input high current	IIH		40.0	uA	VIN = VCC

D0-7, BA0-3, BA8-9, BA13-19

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0	VCC+0.5	V	VCC = 5 +/- 0.5 V
Input low current	IIL		-10.0	uA	VIN = 0.0V
Input high current	IIH		10.0	uA	VIN = VCC
Output low voltage	VOL		0.45	V	IOL = 3.2mA
Output high voltage	VOH	2.4		V	IOH = 0.08mA
Output impedance	IOZ	-90.0	-1.0	uA	0 V < VOUT < VCC

X1

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.2*VCC - 0.1	V	VCC = 5V +/- 5%
Input high voltage	VIH	0.7*VCC	VCC	V	VCC = 5V +/- 5%
Input low current	IIL		-10.0	uA	VIN = 0.0V
Input high current	IIH		10.0	uA	VIN = VCC

X2

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 3.2mA
Output high voltage	VOH	2.4		V	IOH = 0.08mA

PWR/GD

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	1.0	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.4	VCC	V	VCC = 5 +/- 0.5 V

AEN, DT/-R, INTR, TURBO, /BIOS, T/C, SPEAKER, LS139, NMI, READY, RESET, /ENSW, /ROMCS, /ENRAS, /IOR, /MEMR, /MEMW, DACK0-3, /DEN

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 3.2mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA

KBCLK, KBDATA, BA4-7

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VCC = 5 +/- 0.5 V
Input high voltage	VIH	2.0	VCC	V	VCC = 5 +/- 0.5 V
Input low current	IIL		-10.0	uA	VIN = 0.0V
Input high current	IIH		10.0	uA	VIN = VCC
Output low voltage	VOL		0.45	V	IOL = 3.2mA
Output high voltage	VOH	2.4			IOH = -0.08mA
Output impedance	IOZ	-10.0	10.0	uV	OV<VOUT<VCC

CLK88, OSC

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 3.2mA
Output high voltage	VOH	4.0		V	IOH = -0.08mA

BA10-12

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 3.2mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA
Output impedance	IOZ	-10.0	10.0	uA	0V < VOUT < VCC

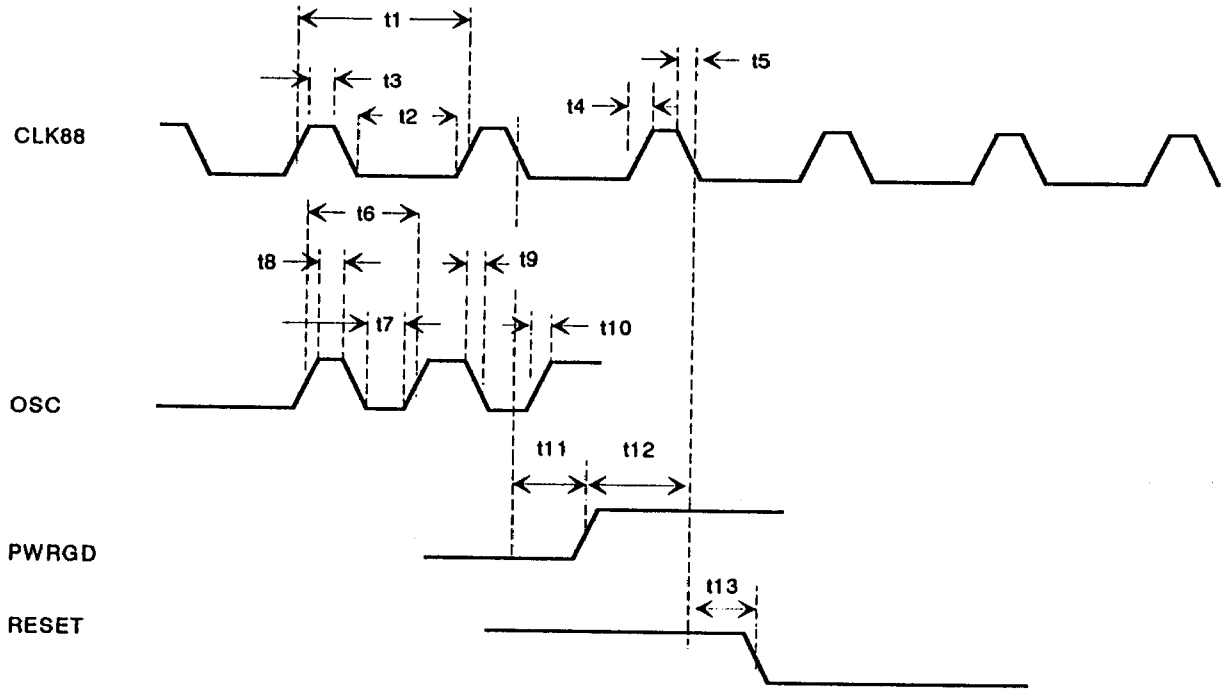
ALE, PARIN

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.45	V	IOL = 6.4mA
Output high voltage	VOH	2.4		V	IOH = -0.08mA

AC Specifications

Symbol	Description	Min	Max	Units
t1	CLK cycle period	80		ns
t2	CLK low time	1/3 t1 + 5.8		ns
t3	CLK high time	2/3 t1-7.1		ns
t4	CLK rise time (1.0V to 3.5V)		10	ns
t5	CLK fall time (3.5V to 1.0V)		10	ns
t6	OSC cycle period	40	69.8	ns
t7	OSC low time	1/2 t6-2		ns
t8	OSC high time	1/2 t6-4		ns
t9	OSC rise time (1.0V to 3.5V)		10	ns
t10	OSC fall time (3.5V to 1.0V)		10	ns
t11	PWRGD hold time to CLK88	10		ns
t12	PWRGD setup time to CLK88	30		ns
t13	INTR delay from IRQ		64	ns

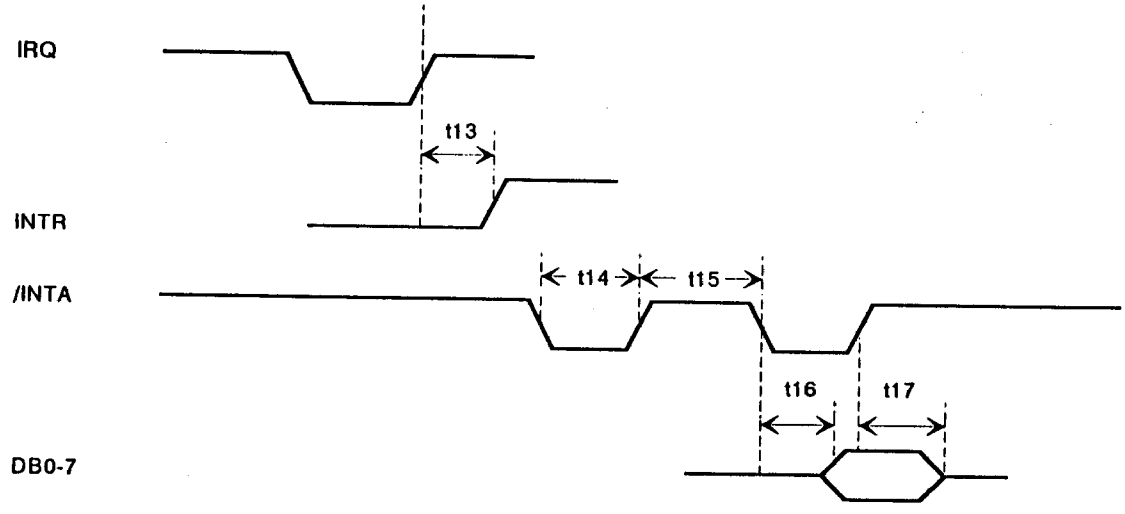
Clock Timing



AC Specifications

Symbol	Description	Min	Max	Units
t14	/INTA pulse width low	100		ns
t15	End of /INTA pulse to next /INTA pulse		100	ns
t16	DB data valid delay from /INTA low		90	ns
t17	DB data float delay from /INTA high	0	50	ns

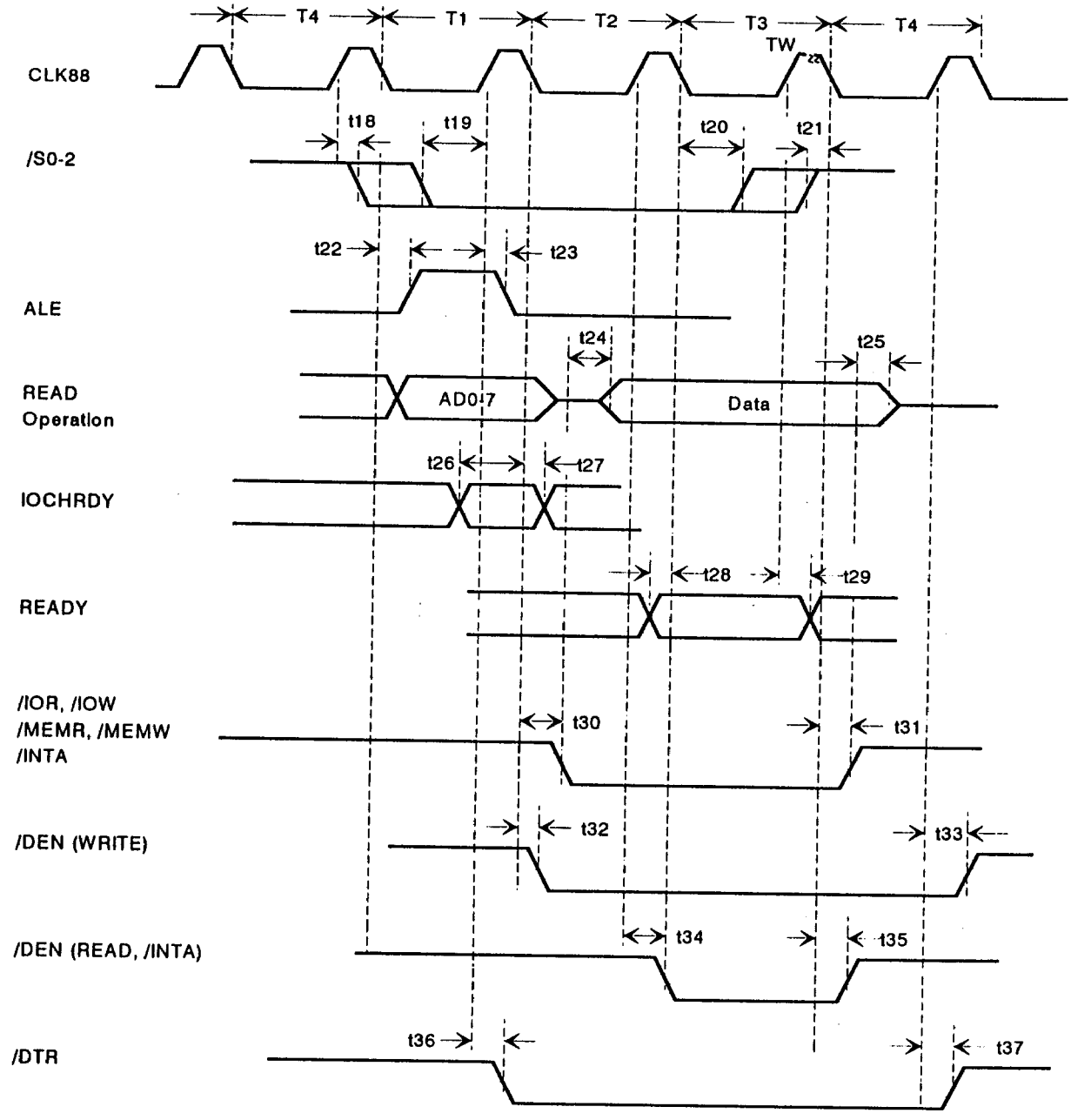
Interrupt Timing



AC Specifications

Symbol	Description	Min	Max	Units
t18	Status inactive hold time	5		ns
t19	Status active setup time	20		ns
t20	Status active hold time	5		ns
t21	Status inactive setup time	20		ns
t22	ALE active delay		23	ns
t23	ALE inactive delay		18	ns
t24	READ data delay from /IOR active		46	ns
t25	Read data float from /IOR inactive	13		ns
t26	IOCHRDY active setup time	20		ns
t27	IORCHRDY active hold time	5		ns
t28	READY setup to CLK88	35		ns
t29	READY hold from CLK88	10		ns
t30	Command active from CLK88 delay		36	ns
t31	Command inactive from CLK88 delay		42	ns
t32	/DEN (write) active from CLK88 delay		35	ns
t33	/DEN (write) inactive from CLK88 delay or /INTA		21	ns
t34	/DEN (read) active from CLK88 delay		23	ns
t35	/DEN (read) inactive from CLK88 delay or /INTA		31	ns
t36	/DTR active from CLK delay		19	ns
t37	/DTR inactive from CLK delay		13	ns

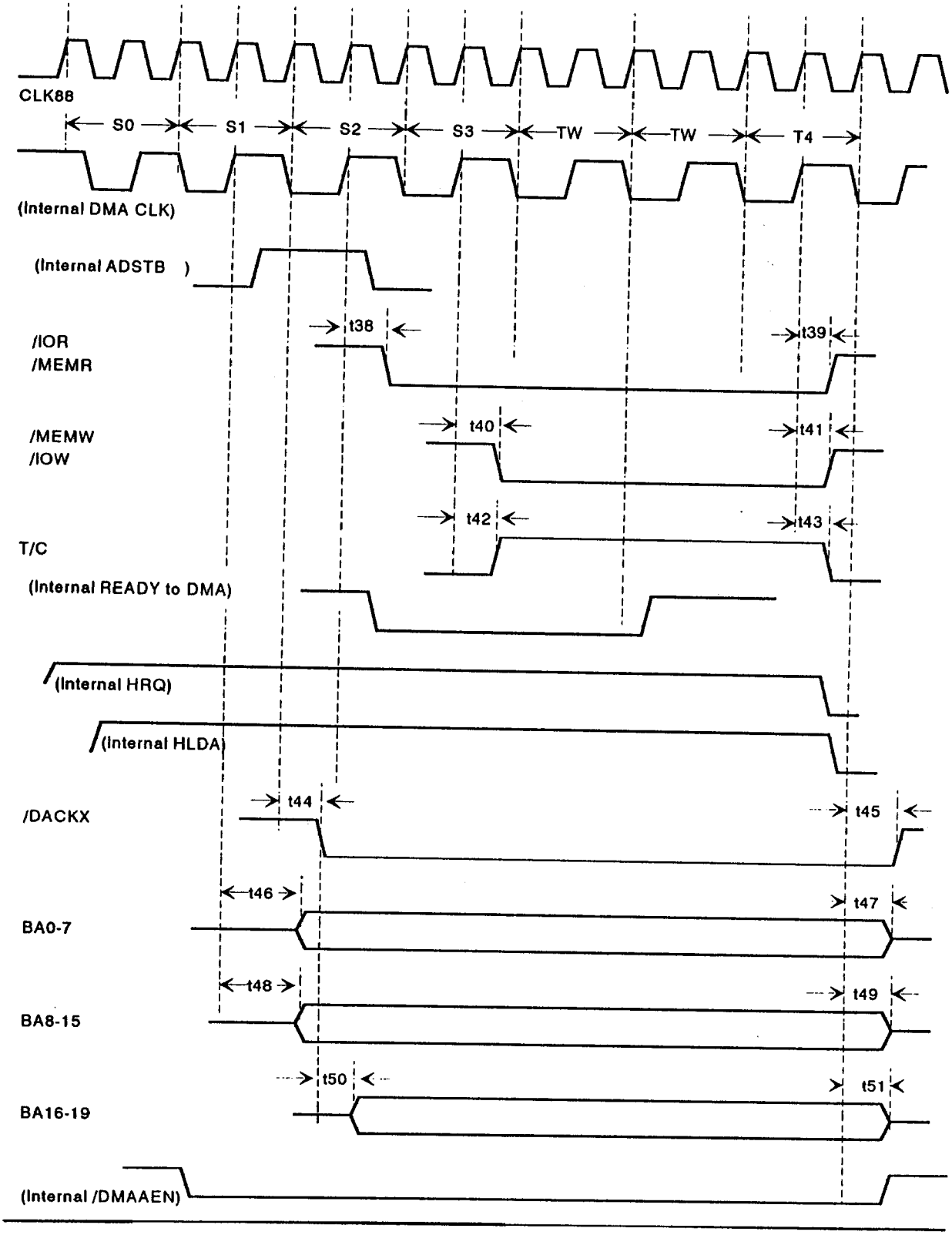
BUS Timing


T4
T1
T2
T3
TW
T4
CLK88
t18
t19
t20
t21
/S0-2
t22
t23
ALE
t24
t25
READ
Operation
AD0-7
Data
t26
t27
IOCHRDY
t28
t29
READY
/IOR, /IOW
/MEMR, /MEMW
/INTA
t30
t31
/DEN (WRITE)
t32
t33
/DEN (READ, /INTA)
t34
t35
/DTR
t36
t37

AC Specifications

Symbol	Description	Min	Max	Units
t38	DMA, /IOR, or /MEMR active from CLK88 delay		52	ns
t39	DMA, /IOR, or /MEMR inactive from CLK88 delay		65	ns
t40	DMA, /MEMW, or /IOW active from CLK88 delay		55	ns
t41	DMA, /MEMW, or /IOW inactive from CLK88 delay		62	ns
t42	T/C active from CLK88 delay		70	ns
t43	T/C inactive from CLK88 delay		70	ns
t44	/DACK active from CLK88 DELAY		48	ns
t45	/DACK inactive from CLK88 delay		80	ns
t46	BA0-7 active from CLK88 delay		105	ns
t47	BA0-7 inactive from CLK88 delay		27	ns
t48	BA8-15 active from CLK88 delay		124	ns
t49	BA8-15 inactive from CLK88 delay		27	ns
t50	BA16-19 active from /DACK		8	ns
t51	BA16-19 inactive from CLK88		27	ns

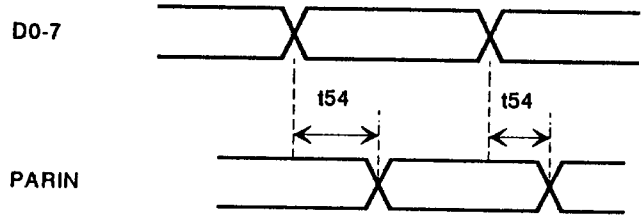
DMA Timing


CLK88
S0
S1
S2
S3
TW
TW
T4
(Internal DMA CLK)
(Internal ADSTB)
t38
t39
/IOR
/MEMR
t40
t41
/MEMW
/IOW
t42
t43
T/C
(Internal READY to DMA)
(Internal HRQ)
(Internal HLDA)
t44
t45
/DACKX
t46
t47
BA0-7
t48
t49
BA8-15
t50
t51
BA16-19
(Internal /DMAAEN)

AC Specifications

Symbol	Description	Min	Max	Units
t54	PARIN from data delay	10	55	ns

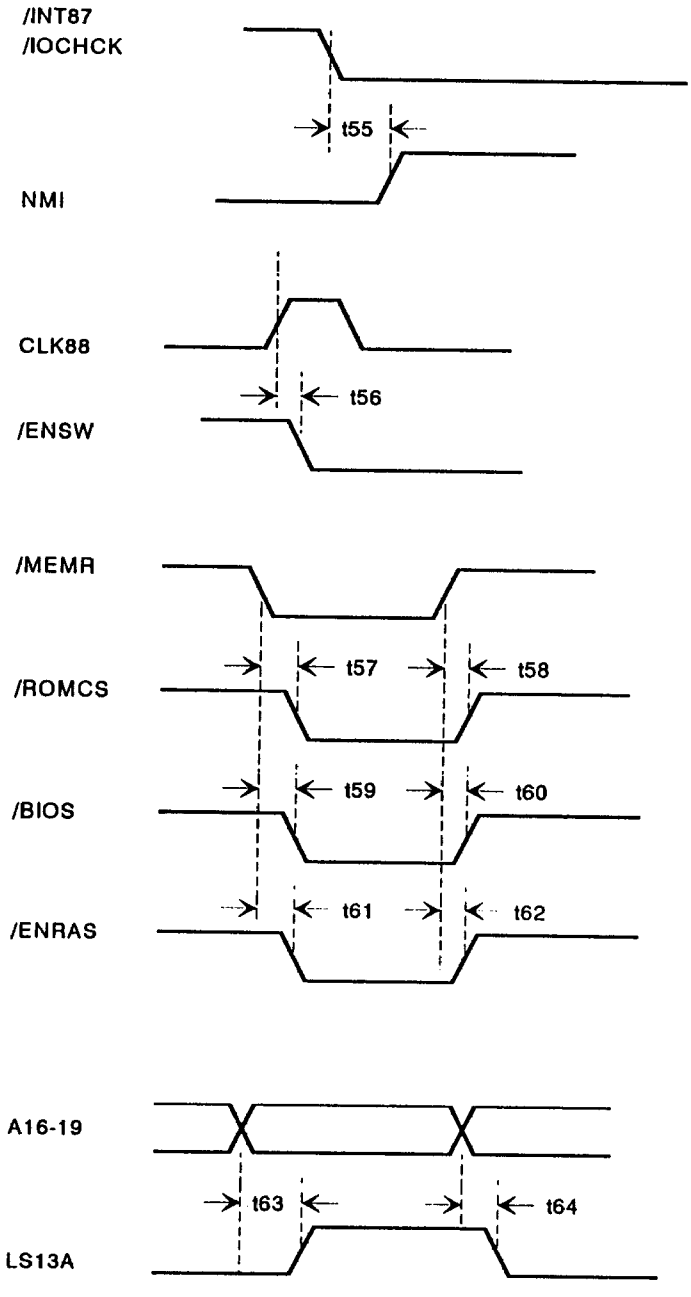
Parity Timing



AC Specifications

Symbol	Description	Min	Max	Units
t55	NMI delay from INT87 or IOCHCK		28	ns
t56	/ENSW from CLK88 delay		15	ns
t57	/ROMCS active from /MEMR delay		12	ns
t58	/ROMCS hold from /MEMR inactive	3		ns
t59	/BIOS active from /MEMR delay		5	ns
t60	/BIOS hold from /MEMR inactive	2		ns
t61	ENRAS active from /MEMR delay		9	ns
t62	ENRAS hold from /MEMR inactive	2		ns
t63	LS139A active from addness delay		33	ns
t64	LS139A inactive from addness delay	10	39	ns

Other Timing



Bill of Materials

Typical PC/XT Motherboard BOM is listed below.

Component	Quantity
74LS00	3
74LS02	1
74LS04	3
7407	1
74LS08	4
74S08	1
74LS10	1
74S08	1
74LS10	1
74LS14	1
74LS20	2
74LS30	1
74LS32	2
74S32	2
74LS74	3
74S74	2
74LS90	1
74LS123	1
74LS125	1
74LS138	2
74LS139	1
74S157	3
74LS175	2
74S175	1
74LS244	4
74LS245	4
74LS280	1
74LS299	1
74LS373	4
74LS670	1
D41256-12	18
2764-15	1
8088-1-P	1
8237AC-5	1
8253C-2	1
8255AC-2	1
8259AC-2	1
8284BIP	1
8288D	1
Inductor 31A-27	1
Socket 16P DIP	36
Socket 20P DIP	1
Socket 28P DIP	2

Bill of Materials con't

Component	Quantity
Socket 40P	DIP 2
Con. 5P Din. FM.	1
Con.62P DIP slot	8
Osc. 30MHz	11
XTAL 14.318MHz	1
XTAL 30MHz	1
Con. 12Pin SIP	1
Pin. 2P*1	3
Pin. 5P*1	2
DIPSW 8 Positions	1
Tr. 2N3904	1
Res. 20 Ohm	1
Res. 22 Ohm	9
Res. 47 Ohm	1
Res. 120 Ohm	3
Res. 510 Ohm	2
Res. 470K Ohm	1
Res. net A4.7K*5	5
Res. net A4.7K*9	4
Cap. C 22pf.80808	1
VCap. 50pf.60702	1
Cap. C 470pf	2
Cap. C 250ph	2
Cap. C 0.1uf.91007	79
Cap. C 0/1uf.	1
Cap. C 22uf/25v	3
Diode IN4148	1

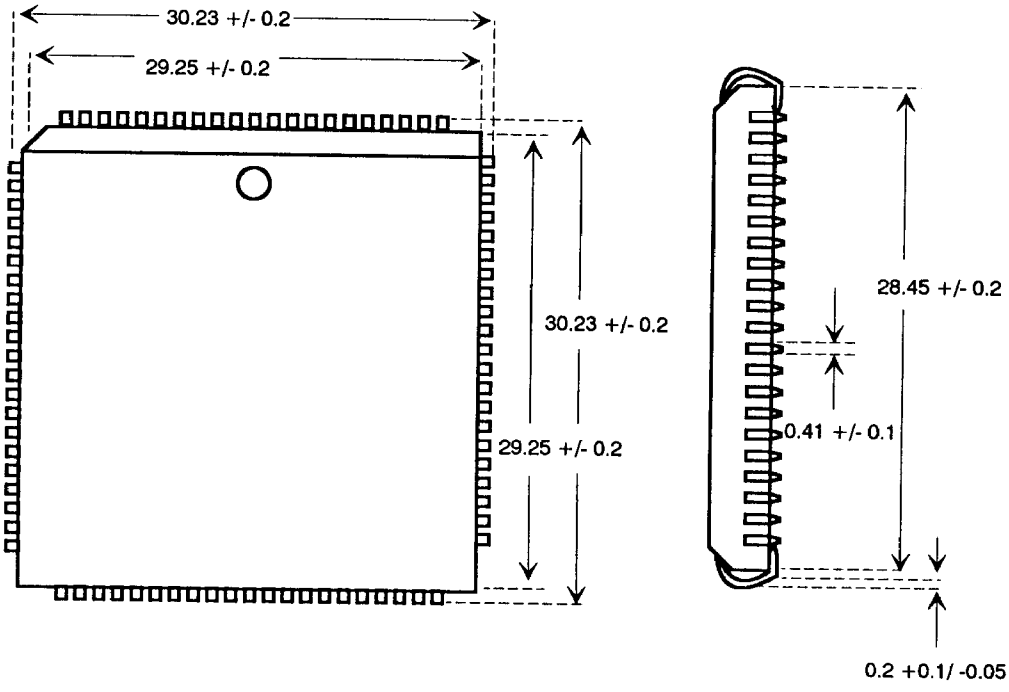
Total Component Count

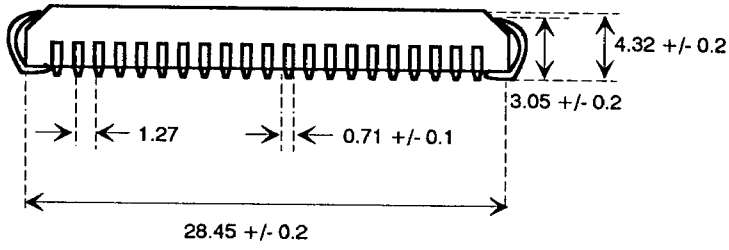
TTL/MSI/LSI	60
Crystal	2

Production Package Specification

Package: 84-pin PLCC
Unit: inches

Chip: ACC 1000





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P/N 520009 Rev. A 7/31/88