From John Titor Aug. 2024 v1.0

To upgrade a 64M MVME-167/177/187 (MVME259D-260D) mezzanine card to 128M:

- Acquire 36 x 4Mx4 60ns fast page mode ('FPM') DRAMs in suitable packages.

  01-W3178F-01A "1996" requires 300mil SOJ packages, e.g. HY5116400CJ-60DR, MB8116400A-60, M5M417400DJ-6, etc.

  01-W3828B-01A "1993" originally used 400mil SOJ packages, e.g. KM44C4000AJ-6, etc. Note that spacing with these parts is very tight, making assembly and inspection quite difficult. It may be significantly easier to use 300mil TSOP devices instead, e.g. K4F170411D-FC60 etc.

- If the board is missing capacitors, acquire 27 x 0.1µF SMD ceramic capacitors in 0805 or similar footprint, and 5 x 33µF 16V SMD tantalum capacitors in 2512 or similar footprint. This is more likely required for 01-W3178F-01A; at least some 01-W3828B-01A appear to have these already mounted.

- Remove excess solder from the unpopulated landings on the PCB.

- Assemble parts to the PCB using your preferred SMD soldering method. Inspect carefully as you go. With nearly 900 pins to solder it is very easy to get distracted and miss a few.

- Adjust the memory configuration strapping resistors:
  01-W3178F-01A: R5 should be removed leaving only R7 installed.
  For other boards the correct resistor to be removed is the one pulling pin 5 of the 22V10 GAL down.

- Inspect the board carefully using strong lighting and a loupe or microscope, and rework as necessary.

- With a continuity tester, check for shorts between VCC and GND (e.g. across one of the tantalum capacitors), and between adjacent pins on the newly installed DRAMs.

- Attach the mezzanine to your test board and install in slot 1 as usual.

- Boot to DBug.

- Use the setup or env command (varies by DBug version) to either disable or move the master aperture(s) so that they do not overlap DRAM. Adjust slave apertures as necessary for your application (e.g. if using a bus-mastering disk or network controller, etc.).

  ```
  167-Bug>env
  ...
  Master Enable #1 [Y/N] = Y?
  Master Starting Address #1 = 04000000? 08000000
  Master Ending Address #1   = EFFFFFFF?
  ... (check all master apertures for overlap in the 0-07ffffff range)
  Update Non-Volatile RAM (Y/N)? y
  Reset Local System (CPU) (Y/N)? y
  ```

- Switch to diagnostics mode after reset and run the RAM tests:

```
167-Bug>sd
167-Diag>cf ram
RAM Configuration Data:
Starting/Ending Address Enable [Y/N] =y ?
Starting Address =00000000 ? 04000000
Ending Address   =00000000 ? 07FFFFFC
Random Data Seed =12301984 ? .
167-Diag>ram
...
167-Diag>ram march
...
```

- Assuming the DRAM parts are good (NOS are your best bet) errors in the RAM test will be indicative of soldering problems.

  The DRAMs are arranged as a single bank 144b (16B) wide. A 4-aligned group of bits misbehaving indicates a problem with a single DRAM.

  When in doubt, clean the board of any flux or other debris and re-inspect. SOJ joints are difficult to judge when viewed from above with a microscope; angle the board so that the fillet on the outside of the leg can be clearly seen.

- To soak-test, use the LC prefix, which will run the tests continuously until either BREAK is set from your terminal or the board is reset.

  ```
  167-Diag>lc;ram
  ```

Photos with RAM size configuration resistors (R5 R6 R7):
http://marc.retronik.fr/motorola/?dir=68K/VME/Boards/MVME257-258-259-260%20DRAM%20Module/Photos