MU9C4910, 4910V
24-BIT DIRECT COLOR GRAPHICS PALETTES

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Combination Look-up table and triple eight-bit Video DAC
- Pseudo-color mode displays 256 colors from a palette of 256K colors
- Adds 15-, 16-, and 24-bit (Blue byte first) Direct Color capability to standard VGA controllers
- Direct Color modes display 32K, 64K, or 16M colors
- Directly drives double-terminated 75-ohm transmission line
- Compatible with VGA, Super-VGA, VESA, TIGA™ and 8514/A with enhanced features
- Internal/external voltage reference (MU9C4910V) or external current reference (MU9C4910)
- Two power-down modes for extended battery life
- Monitor Sense comparators detect monitor connections
- Setup and programmable Sync for video monitor compatibility
- Asynchronous Microprocessor interface
- Pixel Replicate™ suppresses display noise when Look-up table or Mask register accessed during active display time
- Industry-standard 44-pin PLDCC and 28-pin PDIP packages
- 90-, 110-, and 125-MHz pixel rates
- High-performance, TTL-compatible CMOS for low power

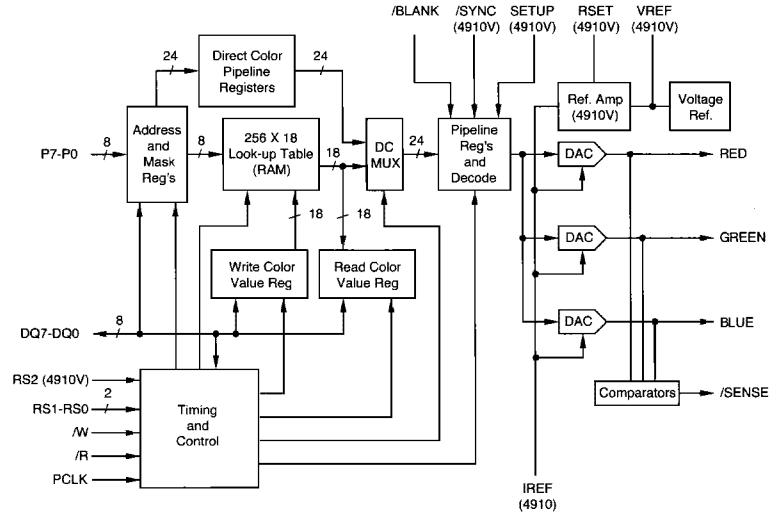
GENERAL DESCRIPTION

The MU9C4910 and MU9C4910V monolithic 24-bit Direct Color Graphics Color Palettes include a 256-word by 18-bit Look-up table, 24-bit Direct Color bypass, three eight-bit Video DACs, Monitor Sense comparators, and two Sleep modes. The VGA-compatible Look-up table accepts up to eight bits per pixel from a frame buffer and performs a translation into three six-bit values for conversion into Red, Green, and Blue analog signals. Each of the Video DACs can directly drive a double-terminated 75-ohm transmission line. The MU9C4910V includes an internal voltage reference, and may also be used with an external voltage reference. The MU9C4910 requires an external current reference.

The MU9C4910 and MU9C4910V are fully compatible with VGA, Super-VGA, VESA, TIGA and 8514/A industry standards while providing many enhanced features. Direct Color operation bypasses the Look-up table to provide 16M (24-bit Blue byte first), 64K (16-bit XGA™), or 32K (15-bit TARGA™) displayable colors. Direct Color data is clocked on two or three consecutive rising edges of the pixel clock, making these devices compatible with any VGA controller. Programmable Sync pulses and a Set-up pedestal are available on all three outputs (MU9C4910V only). Monitor Sense comparators (44-pin PLDCC only) permit the detection of color, monochrome, or no monitor connection. Two Sleep modes reduce power consumption in battery-powered applications. These devices also incorporate a proprietary Pixel Replicate™ feature that allows Look-up table read and write operations to occur during the active portion of the display.

The enhanced Direct Color features may be accessed through an industry-standard key sequence, allowing this device to directly upgrade standard VGA system designs. Available in 28-pin PDIP (MU9C4910 only) and 44-pin PLDCC packages, this device supports the screen resolution, color capability, and power requirements necessary for high-performance Desktop and Notebook Personal computers and Desktop Publishing systems.

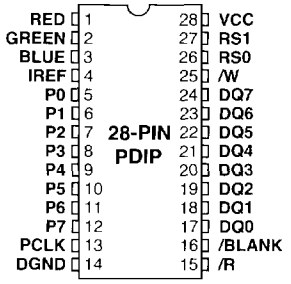
BLOCK DIAGRAM



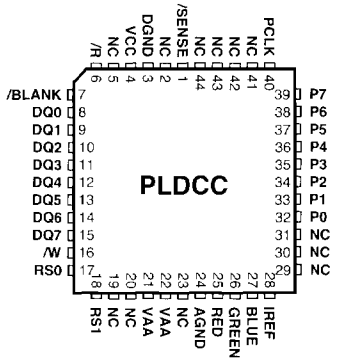
February 15, 1993, Rev. 0

MU9C4910/V

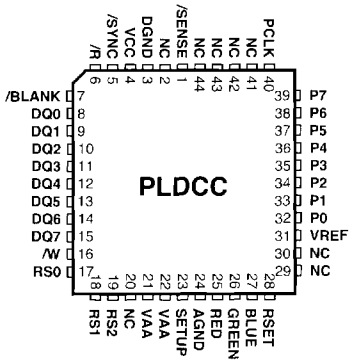
PINOUT DIAGRAMS



MU9C4910



MU9C4910



MU9C4910V

PIN DESCRIPTIONS

RED, GREEN, BLUE (Video Signal, Output, Analog)

These signals are the outputs of the three Video DACs and are capable of driving a double- or single-terminated 75-Ω transmission line directly connected to a suitable monitor or video amplifier.

IREF (Reference Current, Input, Analog, 4910 only)

The IREF pin current sets the full scale output of the Video DACs. This pin must be driven by an external current sink providing a regulated current. This reference current, I_{REF}, is determined by Equation [1], where V_{FS} is the the desired full scale DAC output and Ro is the DAC load resistance with a monitor attached. The IREF pin will be turned off (no current) during Sleep modes.

$$I_{REF}\,[mA] = \frac{V_{FS}\,[mV]}{R_O\,[\Omega] * 2.1} \qquad [1]$$

RSET (Reference Current, Input, Analog, 4910V only)

For the 4910V, the DACs' full scale outputs are determined by a resistor from the RSET pin to AGND. The value of the resistor, R_{SET}, is determined by Equation [2], where V_{REF} is the reference voltage, V_{FS} is the desired full scale DAC output voltage, Ro is the DAC load resistance with a monitor attached, and K is a constant from Table 1.

$$R_{SET}\,[\Omega] = \frac{K * V_{REF}\,[V] * R_O\,[\Omega]}{V_{FS}\,[V]} \qquad [2]$$

Pedestal	K (without Sync)	K (with Sync)
0 IRE	2.100	3.008
7.5 IRE	2.270	3.178

Table 1: DAC Full Scale Constants

VREF (Reference Voltage, Input, Analog, 4910V only)

The voltage on the VREF pin helps set the Video DAC full scale output. A voltage in the range of 1.0 to 1.5 volts applied to this pin will override the internal 1.235-volt reference. VREF should be capacitively bypassed to AGND when using the internal voltage reference, but otherwise should not drive any external circuitry.

SETUP (Setup Control, Input, TTL, 4910V only)

The SETUP pin controls the Blanking pedestal. With the SETUP pin HIGH, the /BLANK pin switches a 7.5 IRE Blanking pedestal on and off. With the SETUP pin LOW the Blanking pedestal is 0 IRE, and the Black Reference level and the Blanking level are the same. The SETUP pin must be connected either HIGH or LOW, and is connected to ground if the Setup function is not desired.

P7-P0 (Pixel Address, Input, TTL)

P7-P0 are the addresses used to reference a color value stored in the Look-up table or the direct DAC values used for conversion to analog video signals. Individual Pixel Address bits are ANDed with the corresponding Mask Register bits before being sent to the Look-up Table. P7-P0 are registered on the rising edge of PCLK.

PIN DESCRIPTIONS (CONT'D)

PCLK (Pixel Clock, Rising-edge-active Input, TTL)

The Pixel clock registers the Pixel address (P7-P0) and the /BLANK and /SYNC inputs, transfers data in the internal pipeline, and internally synchronizes the Microprocessor Port signals. One pixel is displayed on the monitor for each PCLK cycle in Pseudo-color mode, two PCLK cycles in 15- and 16-bit direct Color modes, and three PCLK cycles in 24-bit Direct Color Mode.

/BLANK (Blank Control, Active-LOW Input, TTL)

The state of the /BLANK input is registered by the rising edge of PCLK. When /BLANK is HIGH, the DAC outputs reflect their digital input values. When /BLANK is LOW, the DAC outputs are forced to the Blanking level to turn off the display during retrace. /BLANK has the same pipeline delay as P7-P0. In Direct Color modes, the first PCLK rising edge that /BLANK is HIGH synchronizes Byte Zero or Blue data, after which /BLANK is registered on the same rising edge of PCLK as Byte Zero or Blue data until /BLANK goes LOW again.

/SYNC (Sync Control, Active-LOW Input, TTL, 4910V only)

The state of the /SYNC input is registered by the rising edge of PCLK. The /SYNC signal controls the Sync pulses on the analog outputs. When /SYNC is HIGH, a 40 IRE (Setup = 7.5 IRE) or 43 IRE (Setup = 0 IRE) current source is added to each analog output; when /SYNC is LOW, the current source is switched off. /SYNC has the same pipeline delay as P7-P0. In Direct Color modes, /SYNC is registered on the same rising edge of PCLK as Byte Zero or Blue data. Sync pulses on the individual analog output pins may be disabled by D4-D2 in the Command register. Because /SYNC does not affect the /BLANK pin or the DAC input data, it should only be asserted when /BLANK is LOW. The /SYNC pin is grounded if Sync is not required on the analog outputs.

/SENSE (Monitor Sense, Active-LOW Output, TTL, 44-pin PLDCC only)

The /SENSE pin is LOW if one or more of the Red, Green, or Blue outputs is higher than the internal 335-mV sense threshold. /SENSE is HIGH during Sleep modes.

/R (Read, Active-LOW Input, TTL)

A negative-going pulse on /R controls the DQ7-DQ0 Read cycle. RS2-RS0, registered on the falling edge of /R, determine the source of the Read Cycle data. The DQ7-DQ0 outputs become valid after the specified access time from the falling edge of /R. The DQ7-DQ0 outputs become high-impedance after the rising edge of /R.

/W (Write, Active-LOW Input, TTL)

A negative-going pulse on /W controls the DQ7-DQ0 Write cycle. RS2-RS0, registered on the falling edge of /W, determine the destination of the Write Cycle data. The DQ7-DQ0 data must meet set-up and hold times referenced to the rising edge of /W.

DQ7-DQ0 (Data Bus, I/O, Three-state TTL)

DQ7-DQ0 transfer all data to and from the Microprocessor port. The Color Value registers use only the six low-order bits (DQ5-DQ0); all other registers use all eight bits.

RS2-RS0 (Register Select, Input, TTL)

The states of RS2-RS0 at the beginning of a Microprocessor Port cycle determine the register to be read or written during that cycle as shown in Table 2. The beginning of the cycle is initiated by the falling edge of either /R or /W, depending on the type of cycle. RS2 is only available on the 4910V, but the Command register may be accessed after using a key sequence consisting of four reads of the Pixel Mask register.

VAA (Analog Power Supply)
AGND (Analog Ground)

The VAA and AGND pins provide the positive power supply and ground, respectively, for the analog portions of the device. On the 44-pin PLDCC package, they are separated from the VCC and DGND digital supplies to enhance noise margins. VAA and VCC should be tied to the same power plane, and AGND and DGND should be tied to the same ground plane, with appropriate care taken to minimize noise. For the 28-pin PDIP, these signals are internally tied to VCC and DGND.

VCC (Digital Power Supply)
DGND (Digital Ground)

The VCC and DGND pins provide the positive power supply and ground, respectively, for the digital portions of the device. On the 44-pin PLDCC package, they are separated from the VAA and AGND analog supplies to enhance noise margins. VAA and VCC should be tied to the same power plane, and AGND and DGND should be tied to the same ground plane, with appropriate care taken to minimize noise. For the 28-pin PDIP, these signals are internally tied to VAA and AGND.

RS2	RS1	RS0	Register
0	0	0	Address Register (RAM Write)
0	0	1	RAM Color Value
0	1	0	Pixel Mask /ID Register†
0	1	1	Address Register (RAM Read)
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Command Register*
1	1	1	Reserved

* Command Register also accessed after four Read cycles to Pixel Mask Register.
† ID register accessed on fourth consecutive Read cycle to Pixel Mask Register.

Table 2: Register Access

FUNCTIONAL DESCRIPTION

Command Register D7	D6	D5	Mode	Colors
0	x	x	Pseudo-Color	256
1	0	1	15-bit Direct Color	32K
1	1	0	16-bit Direct Color	64K
1	1	1	24-bit Direct Color	16M

Table 3: Operational Modes

OPERATIONAL CHARACTERISTICS

The MU9C4910/V includes a Video port, Address logic, a 256-word by 18-bit Look-up table (RAM), registers and multiplexers to bypass the Look-up table for Direct Color operation, three eight-bit Video DACs, internal voltage reference, Monitor Sense comparators, and the logic needed for a Microprocessor interface to access the Mask register, Look-up table and control functions.

Video Port Operation

The Video port includes the Pixel Address (P7-P0), /BLANK, /SYNC, and PCLK pins. The four operational modes are shown in Table 3. The video data is sent to three eight-bit Video DACs, each capable of driving a double-terminated 75-ohm transmission line (75-ohm termination at both ends of the line).

Pseudo-color Mode

Pseudo-color mode provides VGA-compatible Look-up Table operation. P7-P0 are registered on the rising edge of PCLK by the Pixel register. P7-P0 are ANDed with the Mask register, then passed on to the Look-up table RAM as an address. The 18-bit content of this address is transferred to the six MSBs of the three eight-bit Video DACs (the two LSBs are set to zero). Pseudo-color mode is enabled upon power-up and whenever D7 in the Command register is set to zero. The pipeline delay in this mode is four registers (three PCLK cycles).

15- and 16-bit Direct Color Modes

The 15- and 16-bit Direct Color modes are enabled by the Command register codes shown in Table 3. These modes, shown in Figure 1, use two PCLK cycles per Direct Color pixel. The multiplexed Pixel Bus data is synchronized by the rising edge of /BLANK: Byte Zero is registered on the first rising edge of PCLK that /BLANK is HIGH, and Byte One is registered on the next rising edge of PCLK. Byte Zero and Byte One continue to alternate on successive rising edges of PCLK until /BLANK goes LOW again. Byte Zero and Byte One are mapped to the DAC inputs as shown in Table 4 and Table 5. The internal pipeline and the DAC inputs are clocked on the same rising edge of PCLK that registers the Byte Zero data; therefore, one pixel is displayed every two PCLK cycles. The pipeline delay is four PCLK cycles.

24-bit Direct Color Mode

The 24-bit Direct Color mode is enabled by the Command register code shown in Table 3. In this mode, three bytes are read from P7-P0 for every pixel, as shown in Figure 2. The multiplexed Pixel Bus data is synchronized by the rising edge of /BLANK: the Blue byte is registered on the first rising edge of PCLK that /BLANK is HIGH, the Green byte is registered on the next rising edge of PCLK, and the Red byte on the following rising edge of PCLK. The Blue, Green, and Red bytes continue in sequence on successive PCLK rising edges until /BLANK goes LOW again. The internal pipeline and the DAC inputs are clocked on the same PCLK rising edge that registers the Blue data; therefore, one pixel is displayed every three PCLK cycles. The pipeline delay is six PCLK cycles.

/BLANK, SETUP, and /SYNC

The /BLANK (active LOW) input blanks the display during retrace. A LOW level on /BLANK forces the analog outputs to the Blanking level without reference to the data at the DAC inputs. A HIGH level on /BLANK allows the DAC inputs to be converted to analog levels. After being LOW, the first PCLK cycle that /BLANK is HIGH synchronizes Direct Color data.

The Setup pedestal provides a separation between the Blanking level and the Black Reference level, and is selected by the SETUP pin. When the SETUP pin is LOW, the Setup pedestal is 0 IRE and the Blanking level is the same as the Black Reference level. When the SETUP pin is HIGH, the Black and Blanking levels are separated by 7.5 IRE.

The /SYNC (active LOW) input adds composite Sync information to the video outputs. A LOW level on /SYNC turns off a current pedestal, creating a negative Sync pulse. A HIGH level on /SYNC turns on the pedestal and establishes the

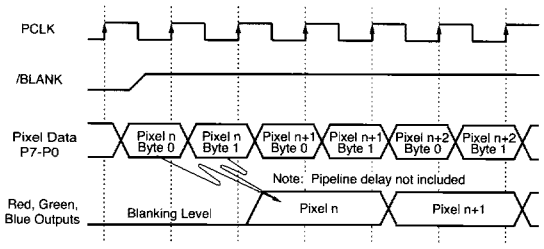


Figure 1: 15- and 16-bit Direct Color Modes

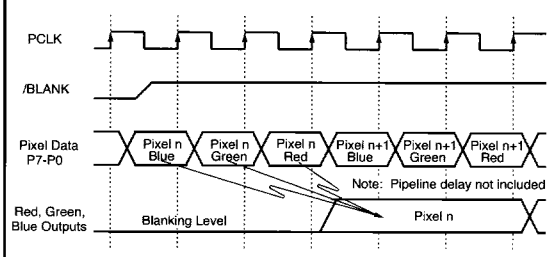


Figure 2: 24-bit Direct Color Mode

FUNCTIONAL DESCRIPTION (CONT'D)

Pixel Bus	15-bit Byte Zero	15-bit Byte One	16-bit Byte Zero	16-bit Byte One	24-bit Blue Byte	24-bit Green Byte	24-bit Red Byte
P7	G5	N/A	G4	R7	B7	G7	R7
P6	G4	R7	G3	R6	B6	G6	R6
P5	G3	R6	G2	R5	B5	G5	R5
P4	B7	R5	B7	R4	B4	G4	R4
P3	B6	R4	B6	R3	B3	G3	R3
P2	B5	R3	B5	G7	B2	G2	R2
P1	B4	G7	B4	G6	B1	G1	R1
P0	B3	G6	B3	G5	B0	G0	R0

Rn, Gn and Bn refer to Red, Green and Blue DAC Inputs
(e.g., R7 is the MSB of the Red DAC)

Table 4: Direct Color Pixel Bus Mappings

Blanking level. The Setup current and DAC bit currents are added to this pedestal. /SYNC does not affect any other inputs, and should only be exercised when /BLANK is LOW.

The Sync pedestal is 40 IRE when Setup = 7.5 IRE as established by the NTSC standard. When Setup = 0 IRE, the Sync pedestal is within the tolerance of the 43 IRE Sync pedestal required by the PAL and SECAM standards.

Tha actual presence of the Sync pedestal (and therefore the Sync pulse) on any given analog output is controlled by the Sync Enable bits (D4-D2) in the Command register. If the Sync Enable bit for a particular output is a logical one, that Sync pedestal is enabled and will turn on and off with the /SYNC input. If the Sync Enable bit for an output is a logical zero, that Sync pedestal is turned off (lowering the VCC current), and no current is added to that output.

The /BLANK and /SYNC pins are registered on the rising edge of PCLK. For the Direct Color modes, they are registered on the same PCLK cycle as Byte Zero or Blue data. The pipeline delays for /BLANK and /SYNC are identical to the delay for P7-P0 for each mode.

Monitor Sense Comparators

The Monitor Sense comparators test the output voltage level against an internally derived 335-mV threshold. The /SENSE output goes LOW if any output exceeds the threshold voltage. The /SENSE output may be read by the host processor, typically through a controller pin dedicated to this purpose. Monitor Sense may be used to detect the presence or absence of color or monochrome monitors or to perform diagnostics. The /SENSE pin should only be read when the DAC outputs are in a predictable state. Note that the /SENSE output may toggle when exercising the /SYNC pin. /SENSE is HIGH when either sleep mode is enabled.

Sleep Modes

The two Sleep modes provide the MU9C4910/V with a low-power capability that permits battery-powered systems to operate longer. The Sleep modes are controlled from the Command register. The device operates normally at power on and whenever the Sleep Enable bit (D0) and Clock Inhibit bit (D1) are logical zeroes. These two bits power down the device to two different supply current levels.

When the Sleep Enable bit is a logical one, power is turned off to the DACs, the DAC reference circuits are turned off (including external current references), and the RAM is placed in a low-power Standby mode. The RAM retains data in this mode, and it is possible to read or write RAM data as long as PCLK is running and the Clock Inhibit bit is a logical zero. The RAM is enabled during a Read or Write cycle and returns to Standby mode when the operation is finished. permitting the RAM to function for applications that access the Color Palette RAM even though the palette is not driving a display.

The Clock Inhibit bit further reduces power consumption. When this bit is set to a logical one, all internal clocking stops, and the RAM may not be accessed. All previous data is retained but the RAM will not be updated. The Command register may be accessed at any time to restore normal operation.

Microprocessor Port Operation

The Microprocessor port provides read and write access to the Look-up table's RAM array (256 words of 18 bits), the Mask register, the read-only ID register, and the Command register. Although the external operations of the Video port and Microprocessor port are asynchronous, Microprocessor port transactions destined for the Look-up Table RAM or the Mask register are internally synchronized by PCLK such that only one video cycle is interrupted for each 18-bit read or write of the

DAC Input	Red 15-bit	Red 16-bit	Red 24-bit	Green 15-bit	Green 16-bit	Green 24-bit	Blue 15-bit	Blue 16-bit	Blue 24-bit
7 (MSB)	B1-P6	B1-P7	R-P7	B1-P1	B1-P2	G-P7	B0-P4	B0-P4	B-P7
6	B1-P5	B1-P6	R-P6	B1-P0	B1-P1	G-P6	B0-P3	B0-P3	B-P6
5	B1-P4	B1-P5	R-P5	B0-P7	B1-P0	G-P5	B0-P2	B0-P2	B-P5
4	B1-P3	B1-P4	R-P4	B0-P6	B0-P7	G-P4	B0-P1	B0-P1	B-P4
3	B1-P2	B1-P3	R-P3	B0-P5	B0-P6	G-P3	B0-P0	B0-P0	B-P3
2	0	0	R-P2	0	B0-P5	G-P2	0	0	B-P2
1	0	0	R-P1	0	0	G-P1	0	0	B-P1
0 (LSB)	0	0	R-P0	0	0	G-P0	0	0	B-P0

B0/B1 -- Byte Zero/Byte One for 15- and 16-bit Direct Color Mode
R/G/B -- Red/Green/Blue Byte for 24-bit Direct Color Mode
(e.g.; B1-P6: P6 bit of Byte One; R-P7: P7 of Red Byte)

Table 5: Direct Color DAC Input Mappings

FUNCTIONAL DESCRIPTION (CONT'D)

Look-up table. To avoid noise on the display during this operation, the color data from the previous pixel is repeated (replicated) at the DAC outputs. This Pixel Replicate™ feature allows Look-up Table or Mask register access during the active portion of the display.

In Sleep mode with the clock inhibited (D0 and D1 logical ones), only the Command register may be accessed. As a result, RAM data will not be updated, although the previous data is retained.

INTERNAL REGISTERS

Any internal register listed in Table 2 may be read or written through the Microprocessor port. All registers are a single byte and are read or written in a single Microprocessor Port cycle, except for the RAM Color Value registers which require three Microprocessor Port cycles.

For a Microprocessor Port Write cycle, the states of RS2-RS0 are first set to the desired value. The falling edge of /W registers the state of RS2-RS0. The Microprocessor Data bus signals (DQ7-DQ0) are registered on the rising edge of /W for transfer to the proper byte of the selected register.

When writing to the Look-up Table, the Address register is first initialized by a Write cycle to RS2-0 = 0H. After three bytes have been written to the Color Value Write register, data is transferred to the Look-up Table RAM at the specified address. The Address register is then incremented in anticipation of writing to the next location, allowing sequential blocks of registers to be written.

For a Microprocessor Port Read cycle, RS2-RS0 are set to the desired value and registered on the falling edge of /R. The output data is placed on DQ7-DQ0 until after the rising edge of /R, resulting in the data bus resuming a high-impedance state.

When reading from the Look-up Table, the Address register is initialized with a Write cycle to RS2-0 = 3H. At this point, data is transferred from the selected address to the Color Value Read register, and then the Address register is incremented. After three bytes have been read from the Color Value Read register, data is again transferred from the location selected by the Address register (now pointing to the next address), and the address register is again incremented in anticipation of the next read, allowing sequential blocks of registers to be read.

(Note: The Bit Assignment table indicates the function or value of each bit when programmed to the state indicated at the left-hand edge of the table. D7 is read and written on DQ7; D0 is read and written on DQ0.)

Mask Register

The eight-bit Mask register allows manipulation of the Pixel addresses. P7-P0 are bit-wise logically ANDed with the contents of this register before being sent to the Look-up table as an address. If the Mask register contains the byte value FFH, then the state of P7-P0 is unaltered. If the Mask register contains 00H, then the Look-up table will be passed 00H. The masking of individual bits may be used to create animation effects on the screen. Mask register operations are internally synchronized to PCLK, allowing unlimited read and write access during any portion of the display.

Address Register

The eight-bit Address register is accessed through one of two register select addresses depending upon the desired action. Separate addresses are provided for reading and writing color values. The Address register auto-increments to allow sequential block transfers of color values without re-programming the Address register.

RAM Color Value

The RAM color values are written through the Write Color Value register (18 bits) and read through the Read Color Value register (18 bits) in three Read or Write cycles. The RAM address of the accessed color value is determined by the Address register. The DQ5-DQ0 pins transfer the six-bit Red field on the first Microprocessor port cycle, the six-bit Green field on the second cycle and the six-bit Blue field on the third. DQ5 corresponds to the DAC MSB, and DQ0 to the LSB. Sequential blocks of color values may be transferred without re-programming the Address register.

Command Register

The Command register (see Table 6) controls the Direct Color, Sleep, and Sync Enable features of the MU9C4910/V. There are two ways to read or write the Command register. On the 4910V, the Command register may be directly accessed by setting RS2-0 = 6H. Since some controllers and the 4910 do not support the RS2 pin, the Command register may also be accessed by a key sequence consisting of four consecutive reads of the Mask register address (RS2-0 = 2H; note that the fourth read returns the ID register); the next read or write cycle to the Mask Register address will access the Command register. The Command register continues to be accessible after a read, but not after a write. Any interruption of the key sequence, such as reading a different register or writing any register, will reset an internal access-enable counter, and the key sequence must be restarted from the beginning. After reading the Command register, the access-enable counter should be reset by reading another register unless further access to the Command register is required. For compatibility, the key sequence may also be used on the 4910V with RS2 = 0 or ground.

The recommended method of altering the Command Register is to read the Command register into the host processor, change the required bit(s) and write back to the Command register. This method keeps all other Command register selections intact.

ID Register

The read-only ID register reads back 82H for the 4910 and 4910V. It may be read from DQ7-DQ0 on the fourth consecutive read from the Pixel Mask Register address. The ID register always contains both ones and zeroes. After reading the ID register, a Read cycle of the Address register (RS2-0 = 0) should be executed to prevent accidental access of the Command register unless such access is also desired.

FUNCTIONAL DESCRIPTION (CONT'D)

	D7	D6	D5	D4	D3	D2	D1	D0
	Direct Color Enable	**Mode Select**		**Blue Sync Enable**	**Green Sync Enable**	**Red Sync Enable**	**Clock Inhibit**	**Sleep Enable**
0	**P-color**	**0**	**0**	Sync off	Sync off	Sync off	**Clock on**	**Normal**
1	D-color	1	1	**Sync on**	**Sync on**	**Sync on**	Clock off	Sleep

Power-on initialized state in **Bold-italic**

Table 6: Command Register Bit Assignments

APPLICATIONS

SYSTEM APPLICATIONS

The VGA-compatible Look-up table of the MU9C4910/V can display up to 256 colors at a time. Each of these colors can be any combination of 64 levels each of Red, Green and Blue. Bypassing the Look-up table allows the display of 32K, 64K, or 16M colors at a time. As a result, color digitized images will look more realistic and the cartoon-like quality that results from limited numbers of colors will be eliminated, making the MU9C4910/V particularly well suited to color desk-top publishing and video image-processing applications. Although 15- and 16-bit Direct Color modes do not use the full capability of the eight-bit DACs, they allow the display of a wide range of colors at 800 by 600 pixels with a 1 MB frame buffer. 24-bit Direct Color mode allows color shaded objects to be realistically displayed at resolutions up to 640 by 480 with a 1 MB frame buffer.

When driving analog monochrome (grey-scale) displays, only one DAC output is connected to the single video input of the monitor. The other DAC outputs must be terminated with the equivalent of a single- or double-terminated 75-Ω transmission line (37.5- to 75-Ω resistive load to ground) or tied directly to AGND. If the video frame buffer information is intended to be displayed on a color monitor, the Look-up table can be reprogrammed to provide only the intensity portion of the color information. This technique allows the display of a digitized color frame in monochrome.

The Look-up table also allows pseudo-color image processing techniques, such as density slicing, to be easily implemented on monochrome digitized images. Density slicing is a technique that assigns each grey-scale level in a monochrome image a unique color for display. Small differences in intensity (one bit of the grey scale) are difficult for the eye to differentiate in monochrome, but become readily apparent when assigned unique colors. By changing only the contents of the Look-up table, the displayed image can be transformed from monochrome into color.

CHANGING COLOR MODES

Direct Color modes are enabled by setting D7-D5 in the Command register to one of the codes in Table 3, either by a direct write with RS2-0 = 6H or a key sequence. Since this operation is controlled by the host processor at speeds much slower than the video display rate, mode changes are typically done during a blanking interval when /BLANK is LOW.

DAC REFERENCE

The MU9C4910 requires an external current sink to set the DAC output levels. Such a reference can easily be built from a minimum of low-cost components, as shown in Figure 3. No additional components are required to turn off external current references during Sleep modes, since the IREF current is internally turned off by the MU9C4910. Shunt-type current regulators should not be used with Sleep modes, since this type of regulator requires a second current path from VCC to ground that bypasses the IREF pin for proper operation, increasing the total current consumption. Designs using low power modes should also avoid current regulators connected to a negative supply. Better results are obtained if IREF is not capacitively bypassed to VAA; in fact a ferrite bead (L2 in Figure 3) between the IREF pin and the current regulator can reduce high-frequency current variations, and is recommended in noisy environments.

The MU9C4910V may be configured to use the internal voltage reference or an external voltage reference. When using the internal 1.235-volt reference, only an external resistor and capacitor are required (Figure 4). The internal reference should be accurate enough for most applications. If more accuracy is desired, an external voltage reference may be used. The wide operating range of the reference amplifier allows the user to choose a standard 1.235-volt two-terminal reference or a lower-cost 1.25-volt regulator (Figure 5). The internal DAC reference circuits, including the internal voltage reference and reference amplifier, are turned off during low-power modes. External voltage references require additional external components or a Shutdown pin to achieve the lowest possible Sleep mode power consumption.

The DAC Reference constants in Equation [1] and Table 1 reflect the values for Pseudo-color mode, when only six DAC bits are used. In 15-bit Direct Color mode, the grey scale portion (White to Black) of all three DAC outputs will be 1.6 % lower than Pseudo-color mode. In 16-bit Direct Color mode, the full grey scale output of the Red and Blue DACs will be 1.6 % lower than the Green DAC with all bits on. For 24-bit Direct Color mode, the DAC grey scale will be 1.2 % higher than for Pseudo-color mode.

SLEEP MODE

The two Sleep modes make the MU9C4910/V ideal for battery-powered applications such as notebook computers.

APPLICATIONS (CONT'D)

RAM data is retained during both Sleep modes, and may be read or modified unless the clock is inhibited by setting D1 in the Command register to a logical one. To achieve the lowest possible supply current, the Pixel Address inputs (P7-P0) should remain static and all digital inputs should be within 200 mV of either DGND or VCC. 10-KΩ pull-up resistors to VCC are recommended for all the digital inputs, especially the three-state DQ7-DQ0 pins.

PC LAYOUT GUIDELINES

The MU9C4910/V must receive power from a noise-free, low-impedance power distribution system. The use of VCC and ground planes is highly recommended. Since one side of the package has the digital supplies (VCC and DGND) and opposite side has the analog supplies (VAA and AGND), high quality 0.01-µF and 100-pF high-frequency ceramic bypass capacitors should be placed on both sides of the package. A 4.7-µF tantalum electrolytic capacitor should be placed nearby to filter low frequency noise. The other TTL and CMOS devices on the PCB should also be capacitively bypassed.

A separate power distribution network is recommended for the MU9C4910/V color palettes to ensure a noise-free power supply. One approach is to provide a separate power plane for the color palette and its associated analog circuitry, as shown in Figure 6. The separate analog power plane is isolated from the PCB's digital logic supplies by a ferrite bead (L1) and is connected to the VCC and VAA pins on the color palette. A 4.7-µF tantalum electrolytic capacitor to ground (C3) filters low-frequency noise. C2a consists of a pair of ceramic capacitors, as described above, located near VAA and AGND to bypass the analog power and ground pins. C2b is similarly constructed and placed near VCC and DGND to bypass the digital power and ground pins. The ground plane should be common to both analog and digital circuits on the board.

The signal lines connected to the P7-P0, /BLANK, /SYNC, and PCLK inputs must be either very short or terminated at the input to eliminate ringing or undershoot that might affect critical timing parameters. The traces for these signals should be led over the ground plane and avoid the analog power plane. This device is fabricated in CMOS technology with high-impedance inputs that may not clamp to ground.

To reduce noise, traces connecting external IREF, VREF, and DAC output circuitry should only be run over the analog sections of the ground plane, and should be kept as short as possible. Care should be taken to physically locate the reference input and DAC output components and their ground plane connections away from digital circuits. If the distance from the DAC outputs to the Video connector cannot be kept extremely short, the connecting traces should be constructed as 75-Ω microstrip transmission lines. In general, this constraint implies wider traces, but the exact dimensions must be calculated from the board material and construction.

DEVICE HANDLING AND PROTECTION

CMOS devices are subject to a condition known as latch-up. Latch-up can occur when parasitic four-layer devices similar to SCRs are turned on, typically leading to excessive current flow from VCC to ground. If left to continue, this current may cause the bond wires to open and the device to fail catastrophically. Although steps are taken during design to minimize a product's sensitivity to latch-up, additional precautions should be taken by the user. Digital signals that go directly off the board should be terminated with either a 47-Ω series resistor or a 1-KΩ resistor to DGND. If a 1-KΩ resistor to DGND is used, be sure that the output driver connected to that node can pull the inputs above VIH(min) (typically 2.4 mA source current per 1-KΩ pull-down resistor). Either method will greatly increase the latch-up threshold, as well as reduce EMI radiation (which will aid in meeting FCC standards for radiated noise) and improve Electro-static Discharge (ESD) damage protection.

CMOS devices are subject to damage from ESD. To avoid permanent damage from high-energy electrostatic fields, always follow proper handling procedures. Store unused devices in conductive foam, carriers, or tubes. Devices should be handled only at ESD protected workstations (grounded floor mat and work surface) while wearing a grounded wrist strap and anti-static smock. Never insert devices into powered sockets or insert circuit boards into powered edge-connectors.

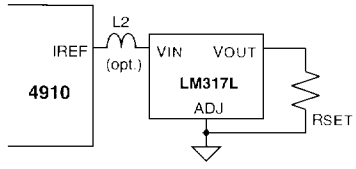


Figure 3: Typical Current Reference

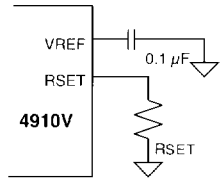


Figure 4: Internal Voltage Reference

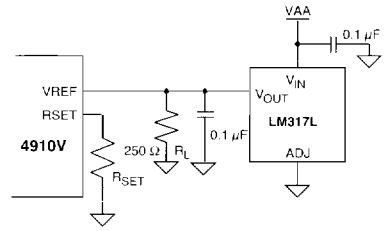


Figure 5: Typical External Voltage Reference
(not recommended for battery-powered applications)

APPLICATIONS (CONT'D)

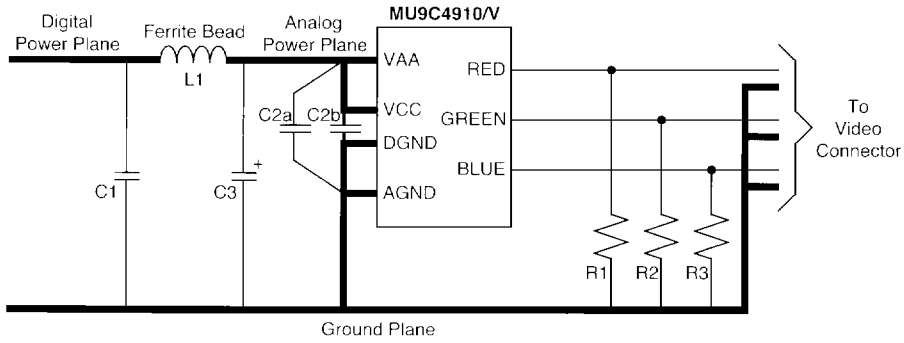


Figure 6: Typical Connection Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 to 7.0 volts
Voltage on all Other Pins	-0.5 to VCC+0.5 Volts (-2.0 Volts for 10 ns at the 50% point; see Figure 10)
Temperature Under Bias	-40 C to +85 C
Storage Temperature	-55 C to +125 C
Maximum Reference Current Magnitude	15 mA
Maximum DAC Output Current Magnitude	50 mA (per Output)
Maximum DC TTL Output Current Magnitude	20 mA (per Output, one at a time, one second duration)

Stresses exceeding the Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

All voltages are referenced to DGND at the device pin, except the Internal Voltage Reference and Monitor Sense Comparator Thresholds which are referenced to AGND.

OPERATING CONDITIONS

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{CC}	Operating Supply Voltage	4.5	5.0	5.5	Volts	
V_{IH}	Input Voltage Logic "1"	2.0		V_{CC}+0.5	Volts	
V_{IL}	Input Voltage Logic "0"	-0.5		0.8	Volts	-1.0 Volts for 10 ns measured @ 50% amplitude (Fig. 10)
V_{REF}	External Voltage Reference	1.0	1.235 1.25	1.5	Volts	10 Precision Reference Voltage Regulator
I_{SET}	Reference Current Magnitude	3.5	8.89	10	mA	3, 10
I_{REF}	Reference Current Magnitude	3.5	8.89	10	mA	3, 11
T_A	Ambient Operating Temperature	0		70	°C	Still Air

CAPACITANCE

T_A = 0 to 70 °C; V_{CC} = 5.0 V ± 10%; f = 1.0 MHz

Symbol	Parameter	Max	Notes
C_I	Digital Input	7 pF	9; /R, /W, RS2-0, SETUP, P7-0, PCLK, /BLANK, /SYNC
C_O	Digital Output	7 pF	9; DQ7-0, /SENSE
C_{OA}	Analog Output	TBD pF	9, 12; RED, GREEN, BLUE

ELECTRICAL CHARACTERISTICS
(over the Operating Temperature and Voltage ranges)

Symbol	Parameter	Min	Typ	Max	Units	Notes
I_{CC}	Average Power Supply Current					
	Normal Operation					
	4910; 4910V with R, G, & B SYNC		95	115	mA	PCLK=90 MHz; 1
	disabled and SETUP LOW (0 IRE)		100	125	mA	PCLK=110 MHz; 1
			105	125	mA	PCLK=125 MHz; 1
	4910V with R, G, & B SYNC enabled		130	145	mA	PCLK=90 MHz; 1
	and SETUP HIGH (7.5 IRE)		135	155	mA	PCLK=110 MHz; 1
			135	155	mA	PCLK=125 MHz; 1
	Sleep Mode					
	Clock Enabled		1	2	mA	2
	Clock Inhibited		250	750	µA	2
$V_{REF(INT)}$	Internal Voltage Reference	1.110	1.235	1.360	Volts	I_{VREF} = 0 µA; 10
I_{VREF}	Voltage Ref. Input Current	-15		15	µA	1.2 V ≤ V_{REF} ≤ 1.3 V; 10
$I_{IREF(OFF)}$	Reference OFF current			5	µA	V_{IREF} = 0 V; 11
V_{TH}	Monitor Sense Comparator Threshold	300	335	370	mV	
V_{OH}	Output Voltage Logic "1"	2.4			Volts	I_{OH}=-5.0 mA
V_{OL}	Output Voltage Logic "0"			0.4	Volts	I_{OL}=5.0 mA
I_{ILK}	Input Leakage Current	-2		2	µA	$V_{DGND} \le V_{IN} \le V_{CC}$
I_{OLK}	Leakage Current (DQ7-DQ0)	-10		10	µA	$V_{DGND} \le V_{IN} \le V_{CC}$, $/R \ge V_{IH}$(min)

DAC Parameter Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IREF}	Voltage on IREF	V_{CC}-3.0		V_{CC}	Volts	3, 11; 3.5 mA≤I_{REF}≤10.0 mA
V_O MAX	Max. Output Voltage			1.5	Volts	3, 4; I_O≤20 mA
I_O MAX	Max. Output Current	31			mA	3; V_O≤1.25 Volts
I_{GS}MAX	Max. Grey Scale Current	21			mA	3; V_O≤1.0 Volts
I_{GS}	Black level to White (Grey Scale)	17.73	18.67	19.60	mA	3, 5
I_{SET}	Blank level to Black (Setup)					3, 5, 10
	Setup = 7.5 IRE	1.36	1.51	1.66	mA	
	Setup = 0 IRE	0	5	50	µA	
I_{SYNC}	Sync level to Blank (Sync)					3, 5, 10
	/SYNC HIGH	7.26	8.07	8.88	mA	
	/SYNC LOW	0	5	50	µA	
	Resolution	6			bits	Pseudo-color mode
		8			bits	24-bit Direct Color mode
	Analog Output Matching			0.5	%	5, 6; I_O = Black and White levels; also Sync and Blank levels on 4910V
	Integral Nonlinearity			±0.5	LSB	5, 7
	Rise Time (DAC Output)			3	ns	9; 10% to 90%; Load as shown in Fig. 7
	Full Scale Settling Time			8	ns	8, 9; Load as shown in Fig. 7
	Glitch Energy			40	pV-sec	9; Load as shown in Fig. 7

SWITCHING CHARACTERISTICS

AC TEST CONDITIONS

Input Signal Transitions	0.0 to 3.0 Volts
Video Port Signal Rise and Fall Times	≤ 2 ns
Microprocessor Port Signal Rise and Fall Times	≤ 3 ns
Digital Input Timing Reference Level	1.5 Volts
Digital Output Timing Reference Levels	0.8 V and 2.4 V
DAC Switching Test Load	Figure 7
TTL Switching Test Load	Figure 8

VIDEO PORT - ALL MODES

			-90		-11		-12			
No.	Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units	Notes
	f_{MAX}	PCLK Frequency								
		Pseudo-color Mode		90		110		125	MHz	
		Direct Color Mode		95		110		125	MHz	
1	t_{CHCH}	PCLK Period								
		Pseudo-color Mode	11		9		8		ns	
		Direct Color Mode	10.5		9		8		ns	
2	t_{CLCH}	PCLK LOW	4		3.5		3		ns	
3	t_{CHCL}	PCLK HIGH	4		3.5		3		ns	
4	t_{PVCH}	P7-P0, /BLANK, and /SYNC Setup to PCLK HIGH	3		2.5		2		ns	
5	t_{CHPX}	P7-P0, /BLANK, and /SYNC Hold from PCLK HIGH	3		2.5		2		ns	
6	t_{CHAV}	PCLK to DAC Valid	0	25	0	25	0	20	ns	9, 13
6a	Δt_{CHAV}	DAC to DAC Skew		0.5		0.5		0.5	ns	9, 14
7	t_{AVQV}	DAC Valid to /SENSE Valid	1		1		1		µs	
8	t_{GLGH}	/BLANK LOW								
		15/16-bit Direct Color	9*P1		9*P1		9*P1		ns	15
		24-bit Direct Color	12*P1		12*P1		12*P1		ns	15

SWITCHING TEST CIRCUITS

Figure 7: DAC Switching Test Load

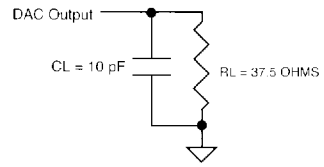


Figure 8: TTL Switching Test Load

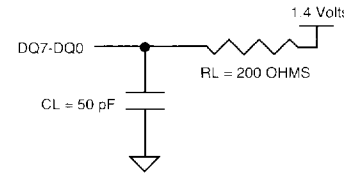


Figure 9: TTL Three-state Test Load

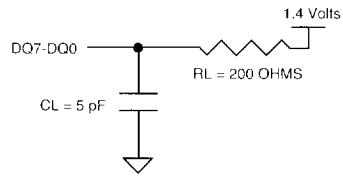
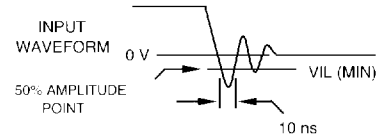


Figure 10: V_{IL} Waveform



Rev. 0

SWITCHING CHARACTERISTICS (CONT'D)

MICROPROCESSOR PORT READ CYCLE

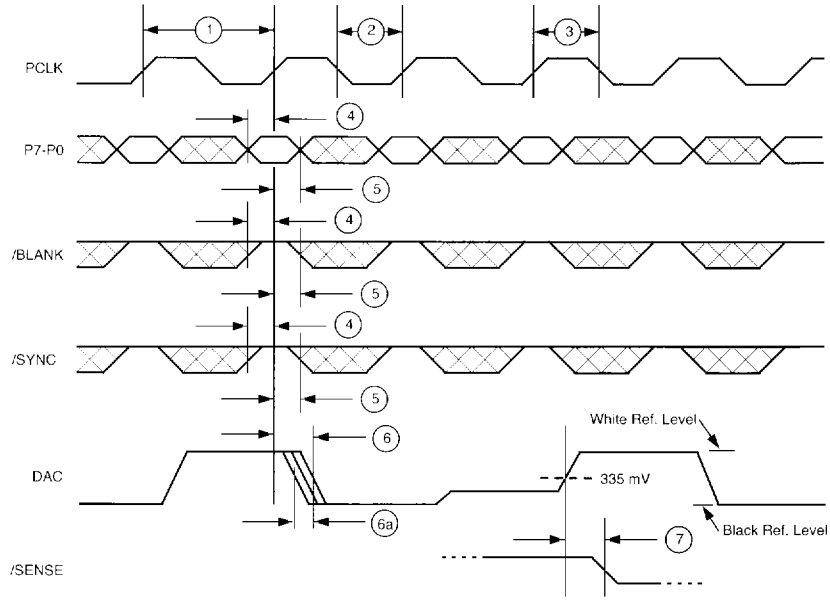
			All Speed Grades			
No.	Symbol	Parameter	Min	Max	Units	Notes
9	t_{RLRH}	Read Pulse Width	50		ns	
10	t_{RHRL1}	Successive Read Interval	3 X P1		ns	15
11	t_{RHWL1}	Read to Write	3 X P1		ns	15
12	t_{RHRL2}	Color Read to Read	6 X P1		ns	15
13	t_{RHWL2}	Color Read to Write	6 X P1		ns	15
14	t_{SVRL}	Register Select Setup to /R LOW	10		ns	
15	t_{RLSX}	Register Select Hold from /R LOW	3		ns	
16	t_{RLQV}	Data Access from /R LOW		40	ns	
17	t_{RLQX}	Output Turn-on from /R LOW	3		ns	16
18	t_{RHQX}	Data Hold from /R HIGH	3		ns	
19	t_{RHQZ}	Data Three-state Delay from /R HIGH		20	ns	16

MICROPROCESSOR PORT WRITE CYCLE

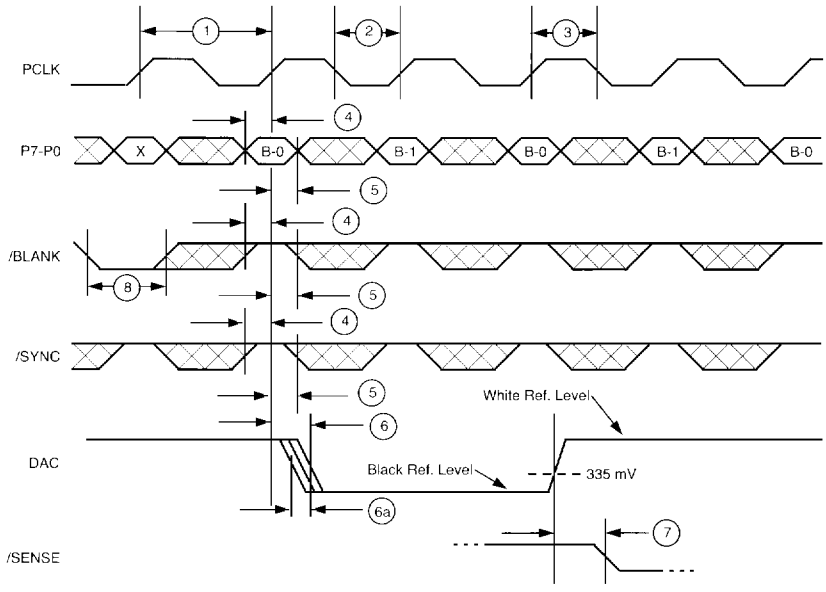
			All Speed Grades			
No.	Symbol	Parameter	Min	Max	Units	Notes
20	t_{WLWH}	Write Pulse Width	50		ns	
21	t_{WHWL1}	Successive Write Interval	3 X P1		ns	15
22	t_{WHWL2}	Write after Color Write	3 X P1		ns	15
23	t_{WHRL1}	Write to Read	3 X P1		ns	15
24	t_{WHRL2}	Color Write to Read	3 X P1		ns	15
25	t_{WHRL3}	Read after Read Address Write	6 X P1		ns	15
26	t_{SVWL}	Register Select Setup to /W LOW	10		ns	
27	t_{WLSX}	Register Select Hold from /W LOW	3		ns	
28	t_{DVWH}	Data Setup to /W HIGH	10		ns	
29	t_{WHDX}	Data Hold from /W HIGH	3		ns	

TIMING DIAGRAMS

VIDEO PORT — PSEUDO-COLOR MODE

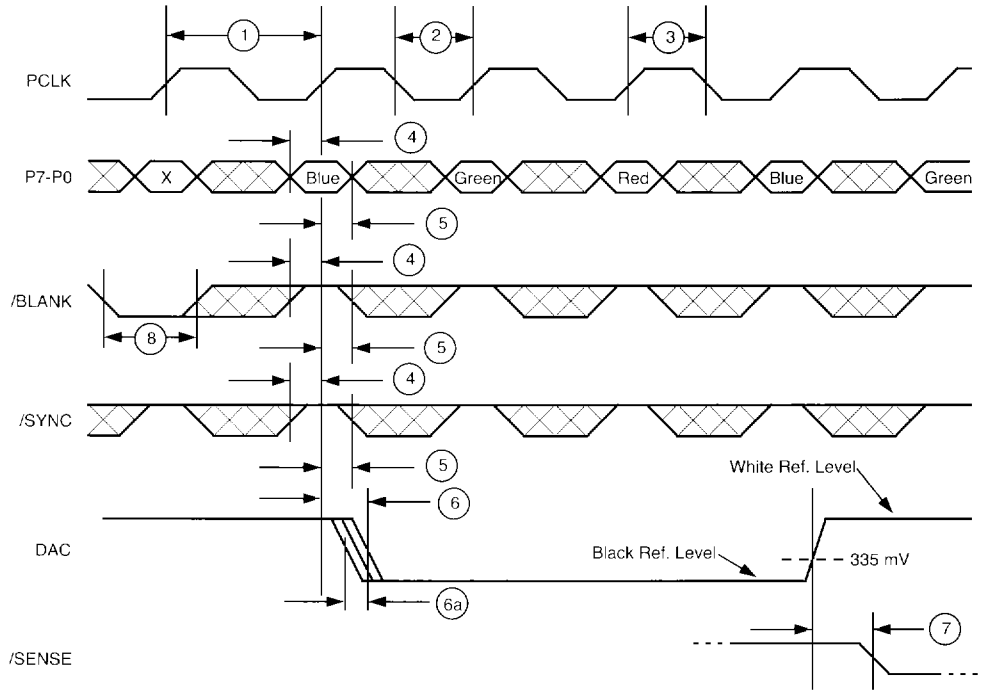


VIDEO PORT — 15- AND 16-BIT DIRECT COLOR MODE

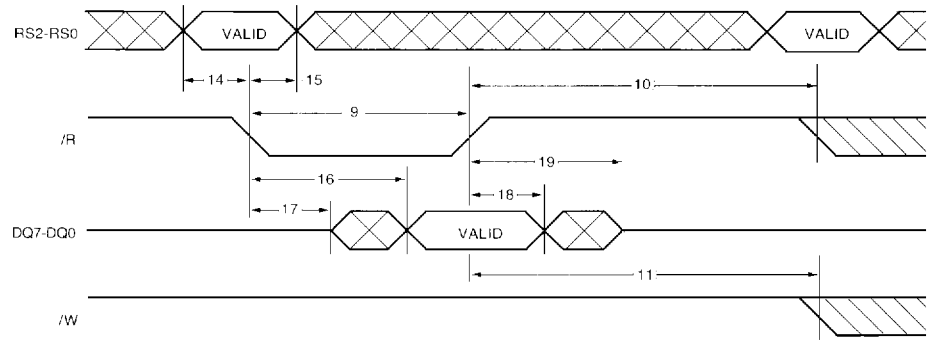


TIMING DIAGRAMS (CONT'D)

VIDEO PORT — 24-BIT DIRECT COLOR MODE

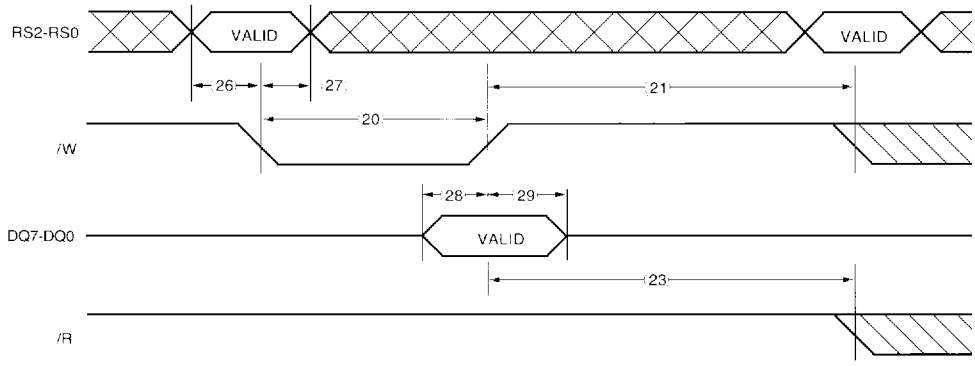


MICROPROCESSOR READ CYCLE

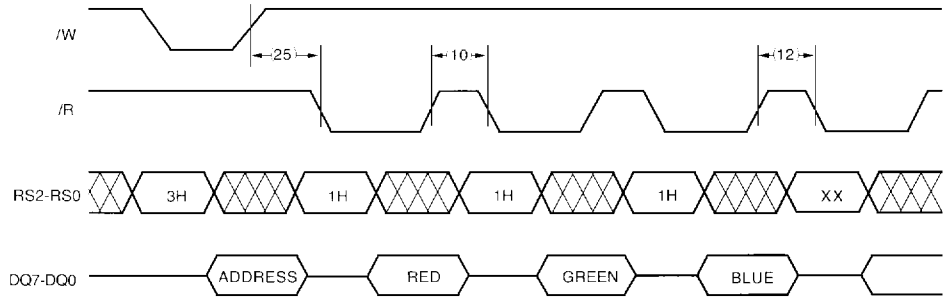


TIMING DIAGRAMS (CONT'D)

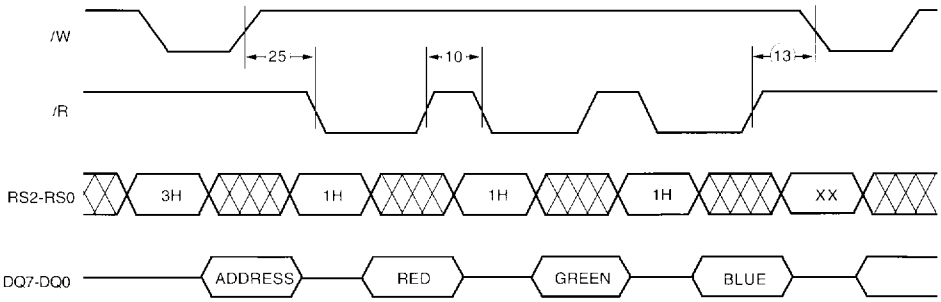
MICROPROCESSOR WRITE CYCLE



COLOR VALUE READ TO READ



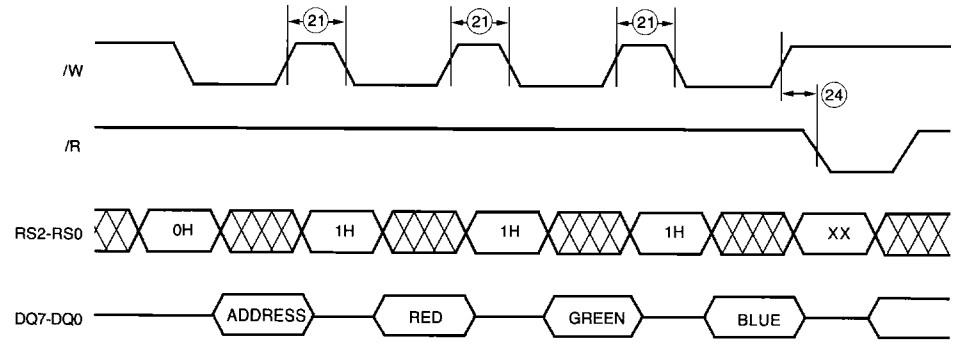
COLOR VALUE READ TO WRITE



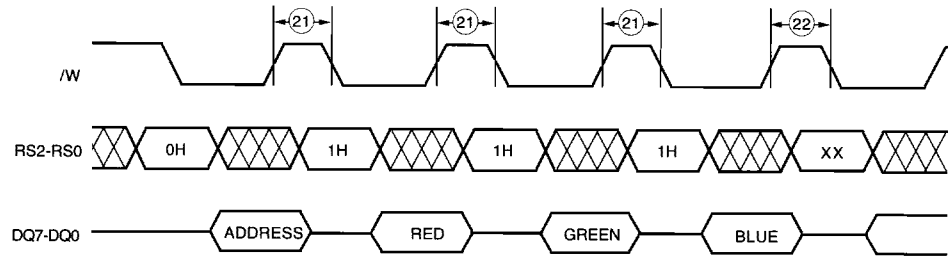
Rev. 0

TIMING DIAGRAMS (CONT'D)

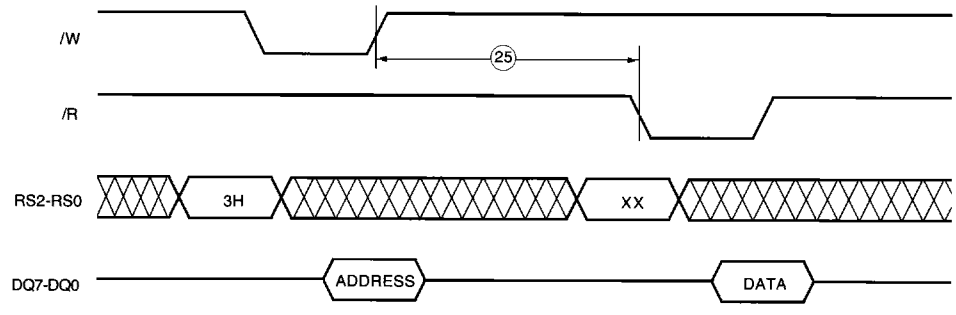
READ AFTER COLOR VALUE WRITE



WRITE AFTER COLOR VALUE WRITE

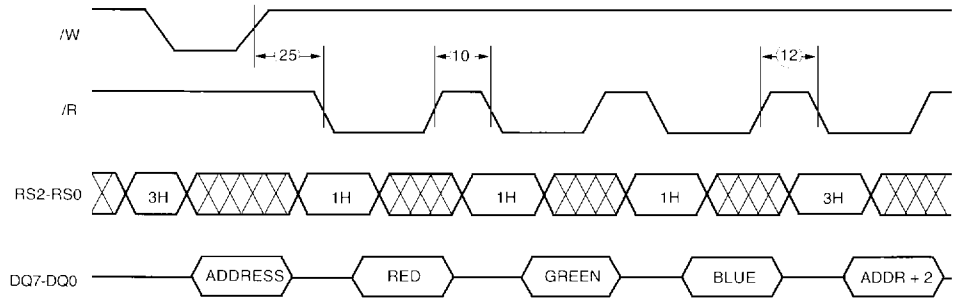


READ AFTER WRITING READ ADDRESS REGISTER

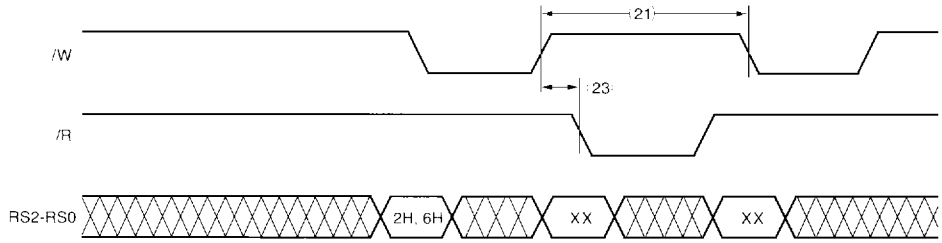


TIMING DIAGRAMS (CONT'D)

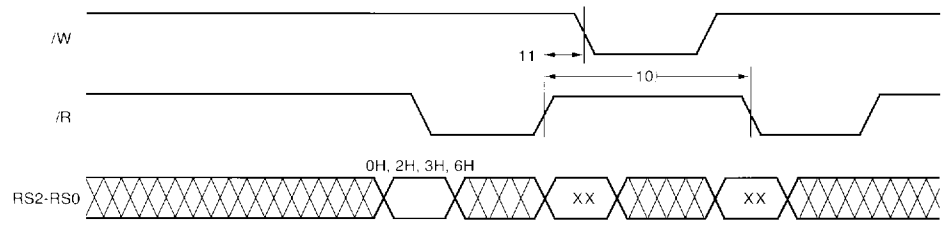
READ COLOR VALUE THEN READ ADDRESS



MASK OR COMMAND REGISTER WRITE TO READ OR WRITE

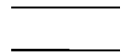
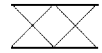


READ FROM COMMAND, MASK OR ADDRESS REGISTER TO READ OR WRITE



WAVEFORM KEY

KEY

WAVEFORMS	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from H to L	Will be changing from H to L
	May change from L to H	Will be changing from L to H
	Don't care. Any change permitted	Undefined. State unknown
	Does not apply	Center line is high impedance "off state"

Notes

1. ICC is measured with VCC=VCC(max) and tCHCH=tCHCH(min). SETUP=VCC (7.5 IRE). The DAC test load is as shown in Figure 6-1. DQ7-DQ0 are unloaded. IREF = -8.89 mA or Ext. VREF = 1.235 volts and RSET = 139 Ω.
2. Sleep Mode ICC is measured with VCC=VCC(max), tCHCH=40 ns, and VCC-0.2 V ≤ VIN ≤ VCC for all inputs, including DQ7-DQ0 and /R.
3. The IREF pin, RSET pin, and analog output pins always source current; this specification shows a current magnitude and ignores the algebraic sign.
4. All DAC outputs should be terminated with the equivalent of a single- or double-terminated 75-Ω transmission line (75-Ω or 37.5-Ω resistive load to ground), independent of the number of DAC outputs used. Unused DAC outputs may also be tied directly to AGND.
5. Measured with IREF = -8.89 mA for IREF devices, or Ext. VREF = 1.235 volts and RSET = 139 Ω ± .05 % for VREF devices. These typical reference values give an output voltage of 700 mV into a 37.5-Ω load (75-Ω local termination in parallel with 75-Ω monitor) with SETUP and /SYNC LOW.
6. Measured from center value of the DAC outputs.
7. Measured from a straight line between the endpoints in Pseudo-color mode. Monotonicity is guaranteed in all modes.
8. Full Scale Settling Time is measured from a 2% change in output voltage until the output voltage has settled to within ±2% of final value.
9. Guaranteed but not 100% tested.
10. 4910V only.
11. 4910 only.
12. /BLANK≤VIL(MAX) to Disable RED, GREEN, and BLUE Analog outputs.
13. Measured from the PCLK transition that causes the DAC to change. The internal pipeline delay from P7-P0 to the DAC output is not included.
14. Measured at the 50% point between the starting and ending DAC values.
15. P1=tCHCH.
16. Measured from a ±200 mV change from the steady-state voltage using the Figure 6-3 Test Load.

NOTES

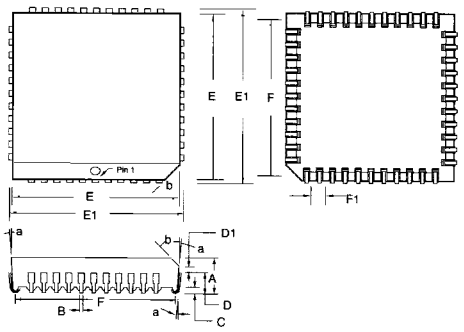
MU9C4910/V

ORDERING INFORMATION

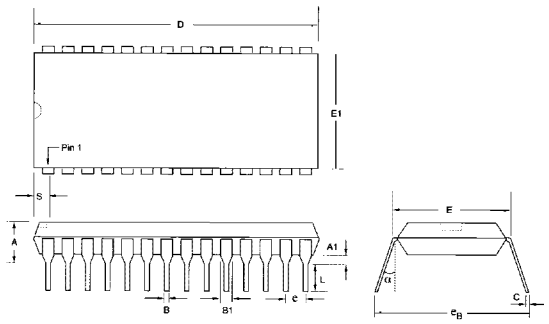
PART NUMBER	SPEED	REFERENCE	PACKAGE	TEMPERATURE RANGE
MU9C4910-YYPC		CURRENT	28-PIN PDIP	0-70°C
MU9C4910-YYDC		CURRENT	44-PIN PLDCC	0-70°C
MU9C4910V-YYDC		VOLTAGE	44-PIN PLDCC	0-70°C
YY=90	90 MHz			
YY=11	110 MHz			
YY=12	125 MHz			

PACKAGE OUTLINES

Lead Count	Dim. A	Dim. A1	Dim. B	Dim. B1	Dim. C	Dim. D	Dim. E	Dim. E1	Dim. e	Dim. e_B	Dim. L	Dim. S	Dim. α
28	.170 .210	.020 .050	.015 .020	.055 .065	.008 .013	1.440 1.460	.590 .610	.540 .560	.090 .110	.640 .690	.125 min	.025 .070	0° 15°



44-PIN PLASTIC LEADED CHIP CARRIER



28-PIN PLASTIC 600-MIL DIP

Lead Count	Dim A	Dim B	Dim C	Dim D	Dim D1	Dim E	Dim. E1	Dim. F	Dim. F1	Dim. a	Dim. b		
44	.170 .176	.017 TYP	.033 .043	.098 TYP	.050 TYP	.650 .656	.685 .695	.620 .626	.050 TYP	3° 6°	45° TYP		

MUSIC SEMICONDUCTORS

USA Headquarters
MUSIC Semiconductors
1150 Academy Park Loop, Suite 202
Colorado Springs, CO 80910
USA
Tel: (1) 719-570-1550
Fax: (1) 719-570-1555
Tel within USA: (1) 800-933-1550

European Headquarters
MUSIC Semiconductors
Torenstraat 28
PO Box 184
6470 ED Eygelshoven
The Netherlands
Tel: +31 45 467878
Fax: +31 45 467822

Far East Headquarters
MUSIC Semiconductors
3/F U-Warehouse Building
Barangay Vitalez, NAIA Complex
Parañaque, Metro Manila
Philippines
Tel: +63-2-834-2156
Fax: +63-2-833-3959

MUSIC Semiconductors agent or distributor:

Find price and stock options from leading distributors for mu9c4910 on Findchips.com:

https://findchips.com/search/mu9c4910

Find CAD models and details for this part:

https://findchips.com/detail/mu9c4910