IBM

DESIGN TIP

RGB51x/RGB52x/RGB62x VRAM to VGA Input Port Switching

The RGB51x, RGB52x and RGB62x families of Palette DACs have two sources of pixel data: the VRAM input port and the VGA input port. One port or the other is selected with the "PORT SEL" bit (bit 0) of Miscellaneous Control 2 register.

For some of these products there are two problems that can occur when switching from the VRAM port back to the VGA port:

- Internally latched data from the previously selected VRAM port can corrupt the VGA data.
- The SCLK can stop running momentarily.

The following table summarizes the status of each product:

Product	Corrupted VGA Data	SCLK Stopped
RGB513	Yes	No
RGB514	Yes	No
RGB524	No	Yes
RGB525	Yes	No
RGB528	No	Yes
RGB624	No	No

Both problems can be circumvented with a software work-around. This software prevents either problem where present, and is otherwise innocuous. Therefore, for software compatibility among all of the RGB51x, RGB52x, and RGB62x products, it is recommended that this software work-around be universally applied.

Software Fix

The software modification is as follows:

When doing a "mode switch" into VGA mode, the following additional steps should be taken:

1. Set bits 1 and 0 to '1's in VRAM Mask Low register, to mask off the lowest VRAM byte. The remaining VRAM Mask bits are "don't care".
2. Set bit 6 (VMSK CNTL) in Miscellaneous Control 1 register to '1', to enable the VRAM MASKing.
3. Make sure at least one SCLK occurs. This means setting up the chip for VRAM pixel data operation. In particular, make sure that the Pixel Format register is set to one of the valid formats (4 BPP…32 BPP). A valid pixel format must be set or SCLK will not run.
4. At this point the low byte of the internal VRAM pixel data should be '0's, and will not interfere with the VGA data.

The VGA Port can now be selected. A two step process is required:

5. Write to the Miscellaneous Control 2 register. Set bit 0 (PORT SEL) to '0' for VGA, but write bits 7 and 6 as '01' (PCLK SEL = Internal PLL.)
6. Do a second write to the Miscellaneous Control 2 register. Again, set bit 0 (PORT SEL) to '0' for VGA. But now set bits 7 and 6 to '00' (PCLK SEL = LCLK.) The VGA port is now selected.

When doing a mode switch back to VRAM port operation, make sure that bit 6 (VMSK CNTL) in Miscellaneous Control 1 register is set back to '0', to disable the VRAM MASKing.

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY
12533-6531

The IBM home page can be found at
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