APPLICATION NOTE

RGB 524-526-624 Palette DAC Conversion

by Tim Ebbers

The RGB526 and RGB624 are third generation designs in IBM's family of high-performance Palette DAC products. One of the important features common to the RGB526 and RGB624 is their compatibility with each other and with the existing RGB524 Palette DAC. The RGB624 is a superset of the RGB526, which is itself a superset of the RGB524, with the same pin out, package, and base register set. The RGB526 can generally be considered a "drop-in" replacement for the RGB524, and the RGB624 is a "drop-in" for either the RGB524 or RGB526. This allows graphics developers to easily migrate the advanced features of the newer Palette DACs into existing RGB524-based products without undergoing costly, time-consuming board redesigns.

This application note provides a summary of the features new to the RGB526 and RGB624, followed by a detailed listing of the differences among the RGB524, RGB526 and RGB624.

Part Numbers

The following RGB part numbers are considered in this Application Note.

Product	Part Numbers	Data Sheet
RGB624	IBM37RGB624 CF 17 IBM37RGB624 CF 22	IOG624DSU
RGB526	IBM37RGB526 CF 17 IBM37RGB526 CF 22	IOG526DSU
RGB524	IBM37RGB524 CF 17-A IBM37RGB524 CF 22-A IBM37RGB524 CF 17 IBM37RGB524 CF 22	IOG524DSU

RGB526 and RGB624 Common Features

The RGB526 and RGB624 both improve on the RGB524 with the following features:

- Enhanced programming of the two PLL clock generators (Pixel PLL and SYSCLK PLL.) While retaining the programming features of the RGB524 for compatibility, the RGB526 and RGB624 offer a new mode for programming the PLLs. Called "full M over N", this new mode has larger M and N ranges, and removes restrictions on M and N combinations that exist with the previous generation. Full M over N gives finer control in programming for the desired output frequencies, and allows the internal operating points of the PLLs to be tuned.
- The Pixel PLL clock generator resets to VGA frequencies.

  When the RGB524 is reset the Pixel PLL clock is "disabled" and runs at some indeterminate frequency, generally in the range of 5 KHz to 250 KHz.

  On the RGB526 and RGB624 the Pixel PLL clock is "enabled", with two sets of programming values. These programming values produce frequencies of 7/4 and 79/40 times the incoming reference frequency (REFCLK). These ratios will produce the standard VGA frequencies of 25.175 MHz and 28.322 MHz when used with an incoming reference clock frequency of 14.31818 MHz (an industry standard.)

  The desired frequency, 25.175 MHz or 28.322 MHz, is selected with the FS[1:0] (Frequency Select) input pins. (Note: the actual frequencies are 25.057 MHz and 28.278 MHz.)

- The SYSCLK PLL clock generator does not glitch on changes of any of the programming values.

  For the RGB524 the M and N values (VCO DIV COUNT and REF DIV COUNT), when changed, will produce a smooth change from the currently programmed frequency to the new frequency. However, a change to the postscaler value P (the DF bits) can cause a glitch on the SYSCLK output.

  For the RGB526 and RGB624 the SYSCLK output will not glitch when changing any of the programming values. As a side effect, however, a postscaler divide value of '1' is now illegal for the SYSCLK PLL (for the old style programming method the DF bits cannot be '10' or '11', for the new M over N programming method the P bits cannot be '001'.)

  For all products the Pixel PLL will accept a postscaler value of '1', and the output can glitch when this value is changed.

- When $\overline{\text{RESET}}$ is active (low), both PLLs run at their reset frequencies.

  For the RGB524 when $\overline{\text{RESET}}$ is low both the SYSCLK and Pixel PLLs oscillated at some indeterminate frequency, generally in the range of 5 KHz to 250 KHz.

  For the RGB526 and RGB624, when $\overline{\text{RESET}}$ is low both the SYSCLK and Pixel PLLs will oscillate at their power on programmed values. When $\overline{\text{RESET}}$ becomes high the PLLs will continue to oscillate at these same frequencies.

- For the RGB524 there is a skew specification that requires the rising edge of LCLK to not be too close to the rising edge of SCLK (a "dead zone" must be maintained.). This is identified in the data sheet in the table "AC Characteristics" as "SCLK to LCLK skew", with the symbol t_{18}.

  For the RGB526 and RGB624 this restriction is eliminated.

- The cursor operation has been extended with the ability to display a "translucent" cursor. With this pixel type, the underlying pixel appears to "shine through" the translucent cursor color. This function is enabled in a new register, Advanced Cursor Attribute, which can specify whether the cursor pixel is transparent, solid, translucent, or highlighted.

The standard cursor is either hard to find or it's in the way.

The RGB526 and RGB624 translucent cursor changes all that. Now, you can see what you're pointing at.

- Overlay/underlay layers are added to the 32 BPP format, with layer selection based on a "chroma key". (8-bit indirect color overlay, 24-bit direct color underlay.)
- Composite sync can be generated from the XOR of HSYNC and VSYNC.
- Adjacent bytes in the incoming VRAM data can be swapped.

Additional RGB624 Features

The RGB624 shares all of the features described above with the RGB526. Beyond this, the RGB624 has a YUV-RGB color space converter. With this converter the RGB624 offers the following additional pixel formats:

- 16 bit 4:2:2 YUV
- 16 bit - mixed 4:2:2 YUV/5:5:5 RGB, selected with a tag bit
- 24 bit packed 4:4:4 YUV
- 32 bit - 24 4:4:4 YUV, 8 unused
- 32 bit - 24 4:4:4 YUV, 8 RGB indirect (overlay)

Swapping of Y/U/V values is available to handle a variety of pixel configurations.

New Feature Details

Non-Transparent Changes

The “non transparent” changes listed below have been made to enhance the usability of the RGB526 and RGB624, or to work with the new features. For drop-in replacement of the RGB524 these changes should be examined to determine the effect on existing designs, if any. Users of other members of the RGB51x and RGB52x product family should also examine these changes to determine the effects on programming compatibility. It is felt that for the most part these changes will be considered desirable or non-consequential.

Register Default Settings

Register	Index	524 Value	526 Value	624 Value
ID	0x0001	0x02	0x02	0x30
Revision	0x0000	0xf0 0xe0	0xc0	0xc0
DAC Operation	0x0006	0x00	0x02	0x02
Fixed Pixel PLL Ref Div	0x0014	-	0x05	0x05
F0	0x0020	0x00	0x05	0x05
F1	0x0021	0x00	0x0e	0x0e
Misc Clock Control	0x0002	0x00	0x01	0x01

The default settings of the RGB526 and RGB624 registers were changed from the RGB524 defaults for the following reasons:

ID Register: The ID of the RGB624 is different to indicate that the YUV pixel formats are available.

Revision Register: The values in this register vary depending on the hardware revisions, if any.

The two values for the RGB524 are related to SCLK INVT (bit 4 of the Miscellaneous Clock Control register.) SCLK INVT does not function correctly on the original RGB524 (part numbers IBM37RGB524 CF 17 and IBM37RGB524 CF 22). These part numbers have a Revision Register value 0xf0.

SCLK INVT functions correctly for part numbers IBM37RGB524 CF 17-A and IBM37RGB524 CF 22-A. These part numbers have a Revision Register value 0xe0.

The RGB526 and RGB624 each have a Revision Register value of 0xc0. SCLK INVT functions correctly for these two products.

DAC Operations Register: For the RGB526 and RGB624, the reset value for this register is changed from 0x00 to 0x02. This changes the default setting of the DSR bit (DAC Slew Rate) from ‘0’ to ‘1’.

Pixel PLL Registers: For the RGB526 and RGB624 the defaults for the Fixed Pixel PLL Reference Divider register and the F0 and F1 frequency registers are changed. The new defaults provide frequencies of 7/4 and 79/40 times the reference clock frequency. As described previously, these ratios generate standard VGA frequencies when used with a reference clock of 14.31818 MHz.

Misc Clock Control: For the RGB526 and RGB624, the reset value is changed from 0x00 to 0x01. This sets the PPLL ENAB (Pixel PLL Enable) bit, so that the Pixel PLL is enabled and running. With the new values in the Pixel PLL programming registers and a reference clock of 14.31818 MHz, described above, the Pixel PLL will be running at 25.057 MHz or 28.278 MHz, as selected by the FS[1:0] input pins.

Pixel PLL Default Values

As described above, when reset the RGB526 and RGB624 Pixel PLL will run at 7/4 or 79/40 times the reference frequency. For the RGB524 the Pixel PLL runs at some indeterminate frequency.

Pixel PLL and SYSCLK PLL Behavior During Reset

As described above for the RGB526 and RGB624, when $\overline{\text{RESET}}$ is active (low), both PLLs run at their reset frequencies and will continue to run at the same frequencies when $\overline{\text{RESET}}$ becomes high.

For the RGB524 when $\overline{\text{RESET}}$ is active the two PLLs run at some indeterminate frequency. When $\overline{\text{RESET}}$ becomes high the SYSCLK PLL goes to the default reset frequency

(33/16 time the reference clock frequency), and the Pixel PLL continues to run at some indeterminate frequency.

SYSCLK DF Values

As described previously, SYSCLK PLL programming values of ‘10’ and ‘11’ for the DF bits are not valid for the RGB526 and RGB624. This is to accommodate the change to the SYSCLK PLL such that glitches will not occur on the SYSCLK output.

SYSCLK Source

For the RGB524 the source of the SYSCLK output can be either the SYSCLK PLL, or the REFCLK input. The System Clock Control register (index `0x0008`), bit 1 (SYS SRC) selects the SYSCLK source.

For the RGB526 and RGB624 REFCLK cannot be used as the source of the SYSCLK output. Bit 1 of the System Clock Control register becomes “reserved”.

MISR Operation

For the previous generation RGB51x and RGB52x products, including the RGB524, the diagnostic MISR (Multiple Input Signature Register) is armed to accumulate a signature by “pulsing” the MISR CNTL bit in the Miscellaneous Control 1 register. That is, writing this register to change the MISR CNTL bit from ‘0’ to ‘1’ and back to ‘0’.

For the RGB526 and RGB624 the MISR is armed by changing the MISR CNTL bit from ‘0’ to ‘1’. Also, MISR CNTL must stay at ‘1’ throughout the frame, until the entire signature has been accumulated.

To accumulate another signature the software changes the MISR CNTL bit back to ‘0’, and then follows the steps above (change the MISR CNTL bit from ‘0’ to ‘1’ and leave at ‘1’ throughout a frame).

To detect the end of signature accumulation a new register, MISR Status, has been added at index `0x0083`. This register contains a single bit, MISR DONE, that indicates when a signature has finished accumulating.

Transparent Changes

The remaining changes are considered “transparent” because they remove previous restrictions, or they are added features that are enabled by setting register bits that are reserved in the RGB524.

“Dead Zone” Elimination

As described previously, for the RGB526 and RGB624 the skew specification that requires the rising edge of LCLK to not be too close to the rising edge of SCLK is eliminated. This is identified in the data sheet in the table “AC Characteristics” as “SCLK to LCLK skew”, with the symbol t_{18}.

The ability to invert SCLK (with the SCLK INVT bit of the Miscellaneous Clock Control register) is provided on the RGB524 as a way to change the LCLK to SCLK timing relationship, as a means of satisfying the t_{18} specification. With this specification eliminated on the RGB526 and RGB624 this function is no longer necessary, but it is still provided for compatibility.

Generated Composite Sync

Miscellaneous Control 1 register (index `0x0070`) changes bit 2 from “reserved” for the RGB524 to XOR SYNC for the RGB526 and RGB624. This bit, when set, generates composite sync internally as the Exclusive OR of the incoming horizontal and vertical sync signals.

VRAM Input Byte Swapping

Miscellaneous Control 3 register (index `0x0072`) changes bits 3 and 2 from “reserved” for the RGB524 to SWAP BYTE for the RGB526 and RGB624. These bits, when set, cause incoming bytes on the PIX[63:00] inputs to be swapped within byte pairs.

Enhanced PLL Programming (General)

For compatibility with the RGB524, both PLLs reset to “old” programming mode (using VCO DIV COUNT, REF DIV COUNT, and DF bit programming values).

The new “full M over N” programming mode has new programming values called M, N and P. Because there are more variations on how the internal sections of the PLLs can operate, an additional programming value, “C”, must

be supplied to adjust the operating point of the analog circuits.

The SYSCLK and Pixel PLL are each explicitly enabled to use the new “full M over N” programming mode.

For new applications the full M over N programming mode is preferred; in the product data sheets full M over N programming is called “standard mode”. The original programming mode is called “compatibility mode”.

Enhanced Programming - SYSCLK PLL

The System Clock Control register (index `0x0008`) changes bit 2 from “reserved” to PROG MODE. This bit, when set, enables the new (standard) programming mode for the SYSCLK PLL.

When set for full M over N programming, the contents of the two SYSCLK programming registers located at indices `0x0015` and `0x0016` are redefined to supply the N and M values, and two new registers at indices `0x0017` and `0x0018` are added to supply the P and C values.

Index	524	526 & 624
`0x0015`	Ref Div Count	N
`0x0016`	VCO Div Count	M
`0x0017`	Reserved	P
`0x0018`	Reserved	C

Enhanced Programming - Pixel PLL

The Pixel PLL Control 1 register (index `0x0010`) changes the EXT/INT bit values of 100 and 101 from “reserved” to “Standard Mode”, to enable the new standard programming mode for the Pixel PLL. ‘100’ is for external frequency select and ‘101’ is for internal frequency select.

The Pixel PLL Control 2 register (index `0x0011`) extends the meaning of the INT FS bits for use with the new standard programming mode, when the EXT/INT bits of Pixel PLL Control 1 are set to ‘101’.

With standard programming the F0 - F15 pixel PLL programming register values are redefined. The old programming mode organizes the F0 - F15 pixel PLL programming registers as 8 banks of 2 programming values, for a 1-of-8 frequency selection. The new standard programming mode organizes F0 - F15 as 4 banks of 4 programming values, for a 1-of-4 frequency selection. This is a consequence of having more programming bits needed for the new programming mode.

For diagnostic readback, with the new standard programming mode the contents of the readback registers at indices `0x008e` and `0x008f` are redefined to reflect the pixel PLL M and N values, and registers are added at indices `0x008c` and `0x008d` to reflect the P and C values.

Index	524	526 & 624
`0x0020,0x0024, 0x0028,0x002c`	DF/VCO Div	M
`0x0021,0x0025, 0x0029,0x002d`	Ref Div	N
`0x0022,0x0026, 0x002a,0x002e`	DF/VCO Div	P
`0x0023,0x0027, 0x002b,0x002f`	Ref Div	C
`0x008c`	Reserved	P Readback
`0x008d`	Reserved	C Readback
`0x008e`	DF/VCO Div Readback	M Readback
`0x008f`	Ref Div Readback	N Readback

Translucent Cursor

The RGB524 has three cursor modes which can be programmed. For the RGB526 and RGB624 these “standard” modes are retained for compatibility. A new mode, called “advanced cursor”, is added to the RGB526 and RGB624.

A new register, Advanced Cursor Control (index `0x0037`) is added. This register has a single bit, ACA ENAB (Advanced Cursor Attribute Enable) to enable the new cursor operation. The power on value of this bit is “disabled”, so that the standard cursor operation is used following a reset.

A second new register, Advanced Cursor Attribute (index `0x0038`) is added. When the advanced cursor operation is enabled the two bit cursor value specifies one of four col-

ors. Each of these colors has a two bit entry in the Advanced Cursor Attribute register which specifies whether the cursor pixel is transparent, solid, translucent, or highlighted.

32 BPP Overlay

Two new registers, the Key (index `0x0068`) and the Key Mask (index `0x006c`) are added for chroma key matching of the overlay layer for the new 32 BPP overlay pixel format.

A third register, the Key Control (index 0x0078) is also added. This register has a single bit, KEY ENAB, to enable the chroma key matching operation. This in effect enables the overlay format when the 32 BPP format is selected. The power on value of this bit is “disabled”, so that normal 32 BPP operation is used following a reset.

If chroma key matching is enabled with the new Key Control register, and 32 BPP is selected, the 24 low order bits are the underlay, and the 8 high order bits are the overlay. If key matching is not enabled the 8 high order bits are unused and the 24 low order bits are used as before.

The 32 bit Pixel Control register (index `0x000e`) has been extended with a new bit, bit 6 = B8 DCOL. This bit determines whether the 8 bit overlay is indirect (through the palette) or direct (to the DACs, for grey scale). This bit has no effect if chroma key matching is not enabled.

YUV (RGB624 Only)

The RGB624 adds YUV support, in which incoming pixels are represented by a luminance (brightness) value Y, and two chrominance (color difference) signals U and V. Several variations of YUV are supported:

- 24-bit, with 8 bits each of Y, U and V.
- 16-bit sub-sampled chrominance, with 8 bits of Y and 8-bits of either U or V. For a stream of pixels the 8-bit chrominance portion alternates between U and V.
- 15-bit sub-sampled chrominance. 8 bits of Y with 7 bits of U/V, and 7 bits of Y with 8 bits of U/V are supported.

  The 15-bit format is for use with “tagged” 16-bit pixels, in which the high order bit is used as a tag to denote the remaining 15 bits as either 5:5:5 RGB or 15-bit sub-sampled chrominance YUV.

Internally, all YUV formats are converted to 24-bit YUV, and then converted to 24-bit RGB. The “color space conversion” from YUV to RGB is programmable and uses the following equations:

$R = Y + K1(V-128)$

$G = Y - K2(V-128) - K3(U-128)$

$B = Y + K4(U-128)$

For programming the color space converter (changing the constants K1 - K4), four new registers K1, K2, K3, K4 (indices `0x00a0` - `0x00a3`) are added to the RGB624.

The 16-bit YUV format supports a key matching mode called “luma key”. When luma key is enabled, the luminance (Y) value is compared to a luma key. If there is no match the pixel is treated as 16-bit YUV. If the Y value matches the luma key, then the remaining 8-bit value is used as an 8-bit RGB value. The Y value is discarded, and the 8-bit RGB value is used as indirect color (used as a lookup address for the palettes.)

16-bit YUV luma key uses the same key registers added to the RGB526 for 32 BPP overlay: the Key (index `0x0068`), Key Mask (index `0x006c`) and Key Control (index `0x0078`).

There are a number of issues involved with YUV: the encoding and range of the input values, the use of the programming constants, and the range and bit precision of the output values. The sub-sampled chrominance formats involve pair alignment issues, U,V ordering, interpolation, and “edge effect” handling. Consult the RGB624 data sheet for discussions of these topics.

The remainder of this section details the control register changes for the RGB624 that enable the YUV formats:

For 16 BPP operation the 16 Bit Pixel Control register (index `0x000c`) has been extended. Bits 4 and 3 were previously reserved. These two bits are now called the B16 MODE bits. When these two bits are `00` the 16 bit pixels are used as before. When `01` or `11`, the 16 bit pixels are interpreted as the “tagged (mixed) RGB/YUV” format. When `10`, the 16 bit pixels are interpreted as 16 bit 4:2:2 YUV. Also, when B16 MODE = 10 and key matching is enabled, 8 bits are used for luma keying and the remaining 8 bits are used as an 8 bit indirect RGB underlay.

For the tagged RGB/YUV formats, the high order bit tags the remaining bits as RGB or YUV. For pixels tagged as YUV, the B16 MODE bits determine the allocation of the remaining 15 bits. Following the high order tag bit, when B16 MODE = `01` the next 8 bits contain a Y or U/V value, with the lowest 7 bits containing the remaining U/V or Y value. When B16 = `11`, following the tag bit the next 7 bits contain Y or U/V, with the lowest 8 bits containing the remaining U/V or Y value.

When the B16 MODE bits are `01`, `10` or `11` the remaining bits of the 16 Bit Pixel Control register are redefined to control various uses of the incoming pixel. One bit, SWAP YC, determines which value (high or low) is the Y value and which is the U/V value. See the detailed register description in the data sheet for more information.

For 24 BPP packed operation the 24 Bit Packed Pixel Control register (index `0x000d`) has been extended with an additional bit, bit 7 = RGB/YUV. When 0, the format is 24 bit packed RGB, the same as before. When 1, the format is 24 bit packed 4:4:4 YUV. When YUV is selected bit 0, the B24P DCOL bit, is not used.

For 32 BPP operation, the 32 bit Pixel Control register (index `0x000e`) has been extended with two bits. Bit 7 = RGB/YUV determines the use of the lower 24 pixel bits. When 0, these bits are RGB. When 1, these bits are 4:4:4 YUV. When YUV is selected bits 1 and 0, the B32 DCOL bits, are not used.

If chroma key matching is enabled with the new Key Control register, the 24 low order bits, RGB or YUV, are the underlay, and the 8 high order bits are the overlay. If key matching is not enabled the 8 high order bits are unused and the 24 low order bits are used as before.

The second new bit, bit 6 = B8 DCOL, determines whether the 8 bit overlay is indirect (through the palette) or direct (to the DACs, for grey scale). This bit has no effect if chroma key matching is not enabled.

The power on value is `0x00` for the 16 Bit, 24 Bit Packed, and 32 Bit Pixel Control registers. Thus, none of the new pixel formats are enabled following a reset.

Pixel Format Tables

Tables 1, 2 and 3 on the following pages contain summaries of the VRAM input pixel formats, for the RGB524, RGB526 and RGB624 products.

Table 1. 24/32 bit Pixel Formats

RGB 524	RGB 526	RGB 624	Pixel Data Format	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
✔	✔	✔	32bit RGB	-								R_{7-0}								G_{7-0}								B_{7-0}							
✔	✔	✔	32bit RGB w/ dynamic bypass	-							T	R_{7-0}								G_{7-0}								B_{7-0}							
		✔	32bit YUV	-								Y_{7-0}								U_{7-0}								V_{7-0}							
		✔	32bit YUV swapped	-								Y_{7-0}								V_{7-0}								U_{7-0}							
	✔	✔	32bit RGB w/ 8bit OVLY	$OVLY_{7-0}$								R_{7-0}								G_{7-0}								B_{7-0}							
		✔	32bit YUV w/ 8bit OVLY	$OVLY_{7-0}$								Y_{7-0}								U_{7-0}								V_{7-0}							
		✔	32bit YUV swapped 8bit OVLY	$OVLY_{7-0}$								Y_{7-0}								V_{7-0}								U_{7-0}							
✔	✔	✔	24bit RGB									R_{7-0}								G_{7-0}								B_{7-0}							
		✔	24bit 4:4:4 YUV									Y_{7-0}								U_{7-0}								V_{7-0}							
		✔	24bit 4:4:4 YUV swapped									Y_{7-0}								V_{7-0}								U_{7-0}							

Table 2. 15/16 bit Pixel Formats

RGB 524	RGB 526	RGB 624	Pixel Data Format	B16 Mode	Swap YC	Swap UV	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
✔	✔	✔	15bit RGB (sparse)	00	na	na																	T	R_{7-3}			G_{7-3}				B_{7-3}							
✔	✔	✔	15bit RGB (contig)	00	na	na																	T	R_{4-0}			G_{4-0}				B_{4-0}							
		✔	15bit YUV 8+7	01	0	0	T	Y_{7-0}							V_{7-1}								T	Y_{7-0}							U_{7-1}						
		✔	15bit YVU 8+7	01	0	1	T	Y_{7-0}							U_{7-1}								T	Y_{7-0}							V_{7-1}						
		✔	15bit UVY 8+7	01	1	0	T	V_{7-0}							Y_{7-1}								T	U_{7-0}							Y_{7-1}						
		✔	15bit VUY 8+7	01	1	1	T	U_{7-0}							Y_{7-1}								T	V_{7-0}							Y_{7-1}						
		✔	15bit YUV 7+8	11	0	0	T	Y_{7-1}							V_{7-0}								T	Y_{7-0}							U_{7-0}						
		✔	15bit YVU 7+8	11	0	1	T	Y_{7-1}							U_{7-0}								T	Y_{7-0}							V_{7-0}						
		✔	15bit UVY 7+8	11	1	0	T	V_{7-1}							Y_{7-0}								T	U_{7-0}							Y_{7-0}						
		✔	15bit VUY 7+8	11	1	1	T	U_{7-1}							Y_{7-0}								T	V_{7-0}							Y_{7-0}						
✔	✔	✔	16bit RGB (sparse)	00	na	na																		R_{7-3}			G_{7-2}				B_{7-3}							
✔	✔	✔	16bit RGB (contig)	00	na	na																		R_{4-0}			G_{5-0}				B_{4-0}							
		✔	16bit YUV	10	0	0	Y_{7-0}								V_{7-0}								Y_{7-0}								U_{7-0}						
		✔	16bit YVU	10	0	1	Y_{7-0}								U_{7-0}								Y_{7-0}								V_{7-0}						
		✔	16bit UVY	10	1	0	V_{7-0}								Y_{7-0}								U_{7-0}								Y_{7-0}						
		✔	16bit VUY	10	1	1	U_{7-0}								Y_{7-0}								V_{7-0}								Y_{7-0}						
		✔	16bit YUV Luma No match	10	0	0	Y_{7-0}								V_{7-0}								Y_{7-0}								U_{7-0}						
		✔	16bit YVU Luma No match	10	0	1	Y_{7-0}								U_{7-0}								Y_{7-0}								V_{7-0}						
		✔	16bit UVY Luma No match	10	1	0	V_{7-0}								Y_{7-0}								U_{7-0}								Y_{7-0}						
		✔	16bit VUY Luma No match	10	1	1	U_{7-0}								Y_{7-0}								V_{7-0}								Y_{7-0}						
		✔	16bit YUV Luma Match	10	0	na	Luma Key_{7-0}								$CLUT_{7-0}$								Luma Key_{7-0}								$CLUT_{7-0}$						
		✔	16bit YUV Luma Match	10	1	na	$CLUT_{7-0}$								Luma Key_{7-0}								$CLUT_{7-0}$								Luma Key_{7-0}						

Table 3. 4/8 bit Pixel Formats

RGB 524	RGB 526	RGB 624	Pixel Data Format	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
✔	✔	✔	8bit RGB (indirect)																									A_{7-0}							
✔	✔	✔	4bit RGB (indirect) w/ swap																									B_{7-0}				A_{7-0}			
✔	✔	✔	4bit RGB (indirect) w/o swap																									A_{7-0}				B_{7-0}			

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY
12533-6531

The IBM home page can be found at
http://www.ibm.com.

The IBM Microelectronics Division home page can be found at
http://www.chips.ibm.com.

Fast Fax Service 415-885-4121

Document No. SK10-3016-00