APPLICATION NOTE

RGB Palette DAC Card Design and Layout Guidelines

R. G. Schaaf

Introduction

Graphics adapter design entails interconnection of various digital and analog components to support a desired function. Key to satisfying one's design objectives is to create a *low noise* environment which permits reliable component behavior. Rail to rail switching of signal voltages can create troublesome card noise that can effect the operation of low signal voltage (millivolt) circuits. Mindful card design and component layout can eliminate or minimize the effects of such noise.

The RGB Family of Palette DACs combines both digital and analog functions on the same silicon die. While the digital logic functions at standard 3.3 volt CMOS levels, the analog circuitry (PLL(s) and DAC) function at millivolt signal levels.

Care must be taken in card design and layout to assure that the Palette DAC's low voltage, external analog nets (PLL control filters, power supplies and DAC video) are void of switching noise. The following is a set of recommendations that will aid the designer in developing a low noise environment.

Part Numbers

Guidelines are provided for:

- ❑ RGB 514
- ❑ RGB 525
- ❑ RGB 524, RGB526, RGB624
- ❑ RGB 528

General Discussion

High edge rate digital signals generate electrical and magnetic fields that can induce unwanted voltages *i.e. noise* into adjacent signal traces or power supplies. Sources of card level noise are numerous. VRAM ports, system clocks, controller and Palette DAC digital outputs are all potential sources.

Noise coupled into the external PLL network(s) or power supplies of the Palette DAC can effect the stability of the pixel and system clocks and/or video outputs. Typical behavior associated with noise would be measurable pixel clock shift *i.e. jitter,* or observable (on screen) pixel shift.

The design goal is to create a low to no noise environment for the Palette DAC's low voltage support circuitry. In general, this can be accomplished thru the application of good design practices, while paying special attention to component placement, signal trace routing and power supply decoupling.

Place and Wire considerations

1. Place and wire Palette DAC analog support components (i.e. loop filters, PLL control resistors, DAC capacitors) on the *component side* of the card. Keep the *Rs & Cs* as close as possible to the connection pins. Keep the traces as short as possible. The use of VIAs for analog interconnection or as testpoints *is not recommended* in these areas. Should VIAs be unavoidable clear the area surrounding the VIA, through all signal planes, of any digital traces (*min 0.25" spacing*). Placement of VIAs that support digital signal interconnect *is not recommended* in this area (see figures 6 - 9 pages 5 - 8).

2. Keep digital and analog nets physically distant from one another. Do not route digital traces adjacent to analog traces. Nets and VIAs supporting clocks, Vram serial and parallel ports, Palette DAC and controller I/O should be routed away from PLL support circuitry and video nets. In the vicinity of the PLL R's and C's Palette DAC digital I/O should be routed on a signal layer below the component wiring layer (first available signal layer *below* the ground plane). If layout permits, a component layer ground shield surrounding the PLL(s) components should be added.
3. Keep the Palette DAC's video output traces short and direct when routing to the video connector. Consider module orientation to obtain the shortest, most direct routes. Avoid VIAs on video traces. The use of a ground shield or *stripline* adjacent to these traces is recommended.
4. The Palette DAC's reference oscillator should be located within 0.75" of the Palette DAC's *RefClk* input. Use preferred routing when connecting. Avoid the use of VIAs or 'T' s connections.

   In general, route fast board clocks first (*i.e*. system, ref, dot, serial etc.). Where possible route clocks on signal layers below the ground plane. Minimize the use of VIAs and avoid 'T' connections. Smoothly 'daisy chain' multiple drop signals where possible to avoid signal reflections from trace edges.

Power Distribution and Filtering

1. Minimize ground noise by using a single, continuous, common ground plane. Do not segment the ground plane. Locate it as the *first* plane below the component wiring plane (see Figure 1).
2. Create separate VDD planes for the Palette DAC's digital, PLL(s) and DAC (video) power. This is done by *segmenting* the card's VDD plane. Power for each plane can be derived from the Palette DAC's 3.3 volt digital supply.

   Separately decouple each plane through an inductor and filter network (bulk and high frequency capacitors (see Figure 10 on page 9).
3. Decouple VRAM supplies. Where ever possible, bulk decouple (22µF to 47µF) each VRAM module. Also, high frequency decouple (0.1µF) each power/ground pin pair (see Figure 4 on page 4). Use short, wide, direct traces when connecting to the module pins and power/ground VIAs.
4. Apply the same bulk and high frequency supply decoupling concepts to any potential source of noise *i.e.* graphics and video controllers, VGA controllers etc.

Card Wiring Plane Assignment

Figure 1 is a cross section of a six layer, 4s2p graphics card in the vicinity of the Palette DAC and support circuitry. The recommended ordering of wiring planes for a 4s2p card is: Signal(*top/component*), Ground, Signal, Signal, Power, Signal (*bottom/solder side)*. A 2s2p cards is: Signal (t*op/component*), Ground, Power, Signal (*bottom/solder side*). In all cases, a continuous ground plane should be positioned as the first plane beneath the top/component wiring plane.

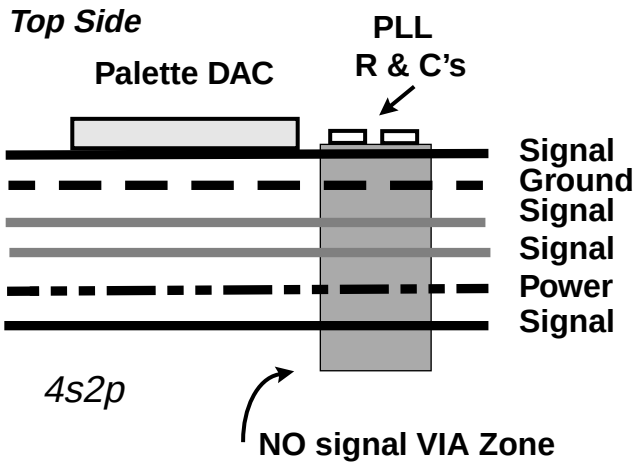


Figure 1. Card Cross Section

Note that the use of VIAs for signal or testpoints should be avoided in the *R & C's* region. Vias for power or ground are permitted.

PLL Component Placements

Figures 6 - 9, pages 5 - 8, suggest optimal PLL component placements for Palette DAC types RGB 514, 524/526/624, 525, and 528.

DAC Component Placements

RRef, Cgref and Ccvref are passive components that support the video out, DAC portion, of the Palette DAC. RRef controls DAC output current. Cgref and Ccvref decouple internal gate and comparator reference supplies.

These components should be mounted on the top side of the card. Short, direct connections are recommended. Keep connection and trace routing away from all digital nets and VIAs.

Other Termination Techniques

High edge rates on bus type signals may result in overshoot, undershoot and ringing. Simultaneously switching of such signals can significantly contribute to card noise. Controlling signal transition rates can aid in minimizing signal noise. Termination of address, data and control signals may be necessary. Two techniques are available, *Series* termination and *AC or parallel* termination.

Series Termination

Series termination entails connecting a low ohm resistor in series with the driving source of a net. This helps to slow or dampen the signal transition and minimize over/undershoots. The resistor should be placed as close to the driving source as possible and before any ‘receiving’ branches of the net (Figure 2). General recommendation is to layout the prototype card with zero ohm resistors (SMT’s or Rpacks) in any fast transitioning buses or control nets. Lab analysis of the card’s signal quality is then required to determine which nets may be problematic and what resistance values helps the most. Generally 33 to 75 ohms are used. Care must be taken to assure that signals are not over compensated (i.e signal transition too slowly). Should your signal audit indicate no problems on particular nets, the series connection can be eliminated on the final version of the card.

Figure 2. Series Termination

Parallel Termination

AC or parallel termination is generally used on long (trace length), lightly loaded nets that carry high transition rate signals (i.e. clocks). Parallel termination aids in minimizing signal reflections; a signal ‘ghost’, derived from the source, that is reflected back from the non-driving (high impedance) end of the signal trace. This *reflection* may have an additive or subtractive effect on the original signal, resulting in a miss-shapen waveform. Parallel termination aids in reducing the electrical energy of the reflection by presenting a low impedance path at the end of the signal trace. Generally, a series resistor and capicator to signal ground is used for this type of termination.

Typical termination values are shown in Figure 3. Note that the precise values for the R and C must be determined through analysis of edge rates and are generally *tuned* during lab testing.

.

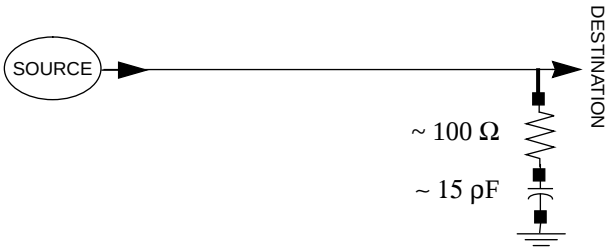


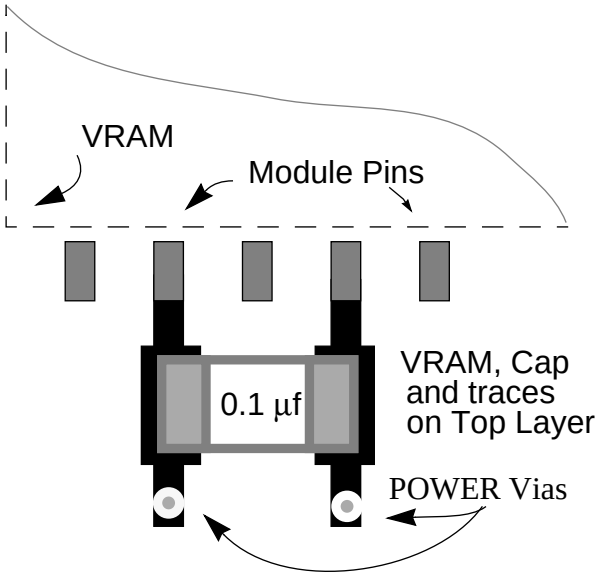
Figure 3. AC signal termination

VRAM High Frequency Decoupling

The recommended layout for connection of the VRAM’s 0.1µF high frequency decoupling capacitor(s) is shown in Figure 4 on page 4. Short, direct, wide traces with the

decoupling cap intervening between the power VIAs and module pins has proven to be the most effective implementation. Each power/ground pin pair should be decoupled to minimize power supply noise. Use of low voltage, 3.3 volt, VRAM also helps to minimize supply noise.

Figure 4. VRAM High Frequency Decoupling



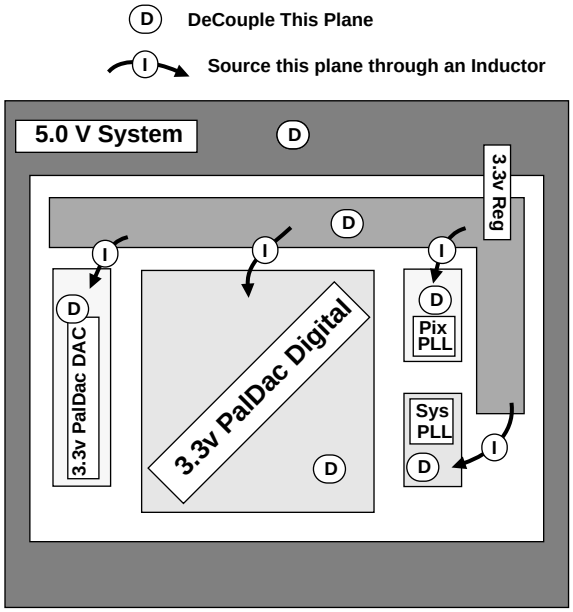
Segmenting the Palette DAC VDD Plane

To better isolate the analog portions of the Palette DAC circuitry from sources of power supply noise the VDD power plane should be divided into discrete power planes for each Palette DAC power type. This can be done by segmenting the existing card VDD plane in the region of the Palette DAC. This does not require additional card layers. Figure 5 is a conceptual diagram showing how the VDD plane can be segmented for a two PLL Palette DAC (i.e. RGB524, RGB624). The card depicted here is shown with a system based 5.0 volt power plane. Should the card be 3.3 volt only, the segmented 3.3 volt plane for the Palette DAC Digital is not required. PLL(s) and DAC power segments, however, must still be provided and properly decoupled (inductor feed, with bulk and high frequency capacitors).

For 5.0 volt cards (with no 3.3 volt system supply available) a 3.3 volt regulator is required. The regulator supplies the Palette DAC's 3.3 volt Digital, the Pixel PLL, the System PLL and the DAC power segments. Each segment is sourced thru an inductor and is decoupled as recommended (see Figure 10 on page 9).

Segmenting of the power plane applies *only* to the VDD plane. Segmenting of the card ground plane *IS NOT* recommended.

Figure 5. Palette DAC 3.3 volt Power Planes



Reference Clock Requirements

The Palette DAC PLL(s) use a card supplied clock as its base reference. *RefClk in* is generally a low frequency clock which the PLL samples to develop higher frequency pixel and system clocks. Pixel clocks are programmable up though 220 Mhz, while RefClks tend to be in the low Mhz range (14 - 40Mhz). If the RefClk frequency tends to drift (the clock period varies over time) the Palette DAC PLL(s),will attempt to readjust its higher frequency clocks in response. This can result in pixel jitter, an observable screen effect.

To minimize this effect, source the RefClk from a high quality, fix frequency oscillator. Use of a PLL based reference clock *is not recommended.*

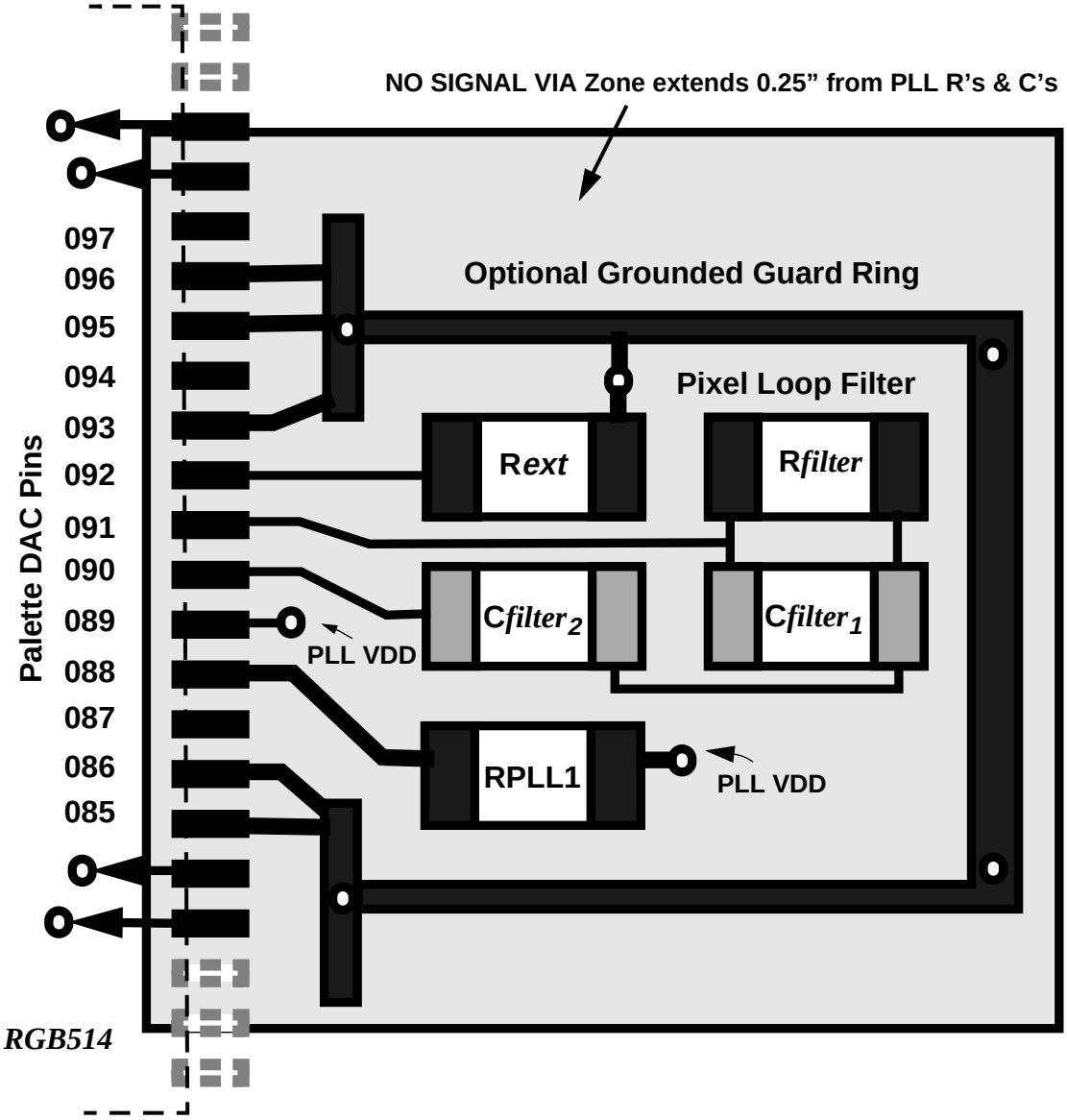


Figure 6. RGB514 PLL Component layout

RGB514 contains one PLL for pixel clock generation. Figure 6 represents an optimal placement for the PLL support components. Note that all traces and components are on the top (component) side of the card. Make connections using short direct traces. Do not uses VIAs to connect the components with the exception of PLL VDD and ground. Digital signals that are present on adjacent Palette DAC pins should be swept under the module and connected, by VIA, to wiring planes below the ground plane. Do not route digital signals or place VIAs that support digital nets within the ‘*NO SIGNAL Via Zone*’. The use of a grounded guard ring is recommended.

Five passive components support the PLL function. R*ext* is a 10KΩ resistor that sets the VCO gain. It is connected between module pin 92 and card ground. RPLL1 is a 8.66KΩ resistor that controls the current to the VCO charge pump. It is connected between module pin 88 and the PLL VDD power plane.

The VCO Loop Filter is comprised of R*filter (*1.3KΩ*)*, C$filter_1$ (680 pF) and C$filter_2$ (8.2 nF). Module pin 91 connects to R*filter.* R*filter* connects in parallel to C$filter_1$.The loop filter returns to module pin 90, thru C$filter_2$.

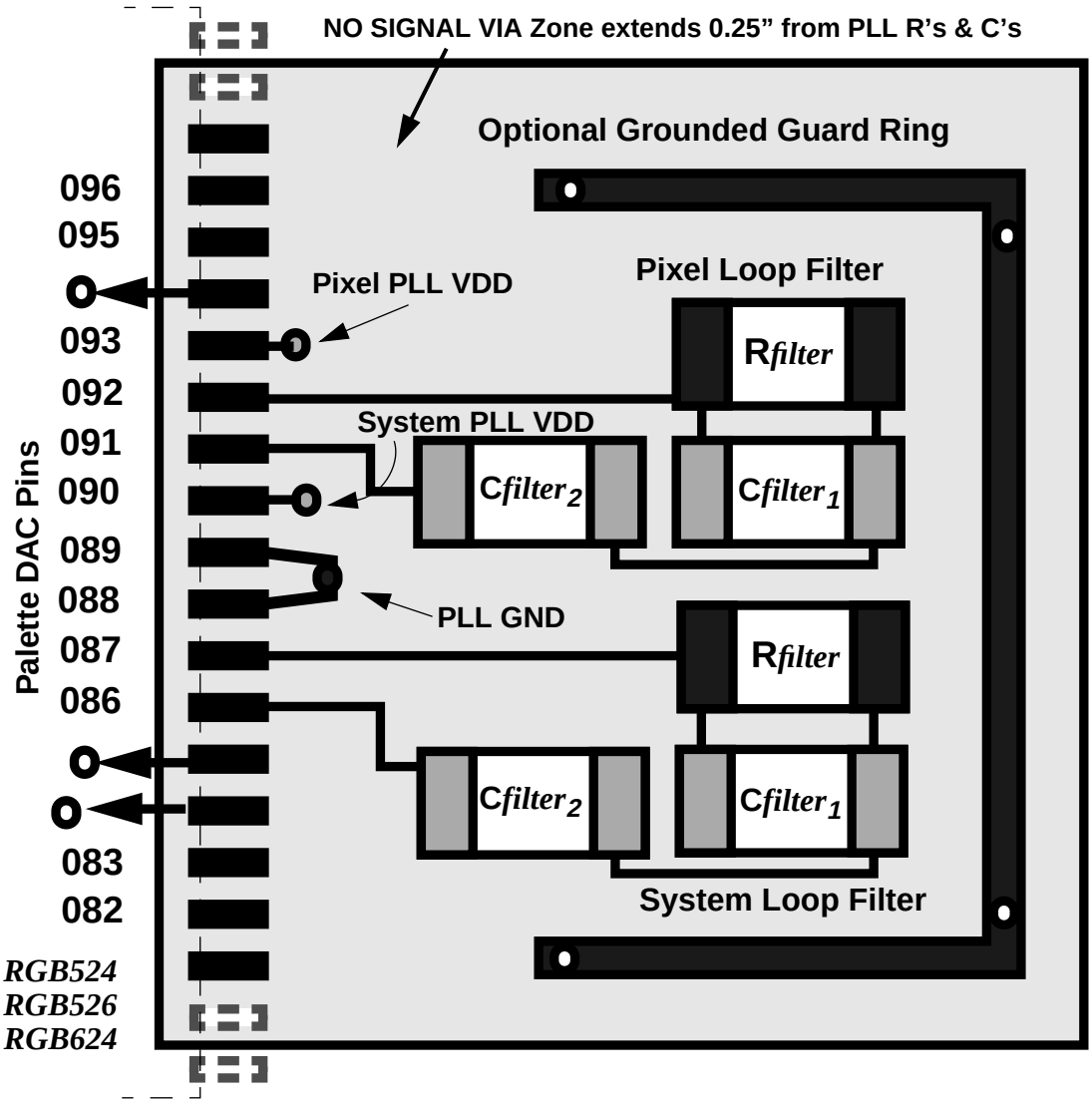


Figure 7. 524/526/624 PLL Component Layout

The RGB524, RGB526 and RGB624 are pin compatible Palette DACs. Each contain two PLL’s; one for system clock and one for pixel clock. Figure 7 represents the optimal loop filter component placement when both PLL’s are enabled. All filter wiring should be made on the top (component) side of the card. Make connections using short direct traces. Do not use VIAs to connect the filter components. Do not route digital signals or place VIAs that support digital nets within the ‘*NO SIGNAL Via Zone*’. A grounded guard ring is recommended.

The loop filter components values are identical for both pixel and system PPL filters: R*filter* = 1.3KΩ, C$filter_{1}$ = 680 pF and C$filter_{1}$ = 8.2 nF.

The *pixel* loop filter connects between pins 91 and 92. VDD for the pixel PLL is supplied on pin 93. The *system* loop filter connects between pins 86 and 87. VDD for the system PLL is supplied on pin 90.

Power for the PLL’s should be provided thru separate System and pixel PLL VDD power planes (see Figure 5 on page 4.) Each plane should be decoupled as recommended in Figure 10 on page 9. Directly connect the PLL grounds (pins 88, 89) to the common card ground by VIA. Use short, wide traces between pin and VIA.

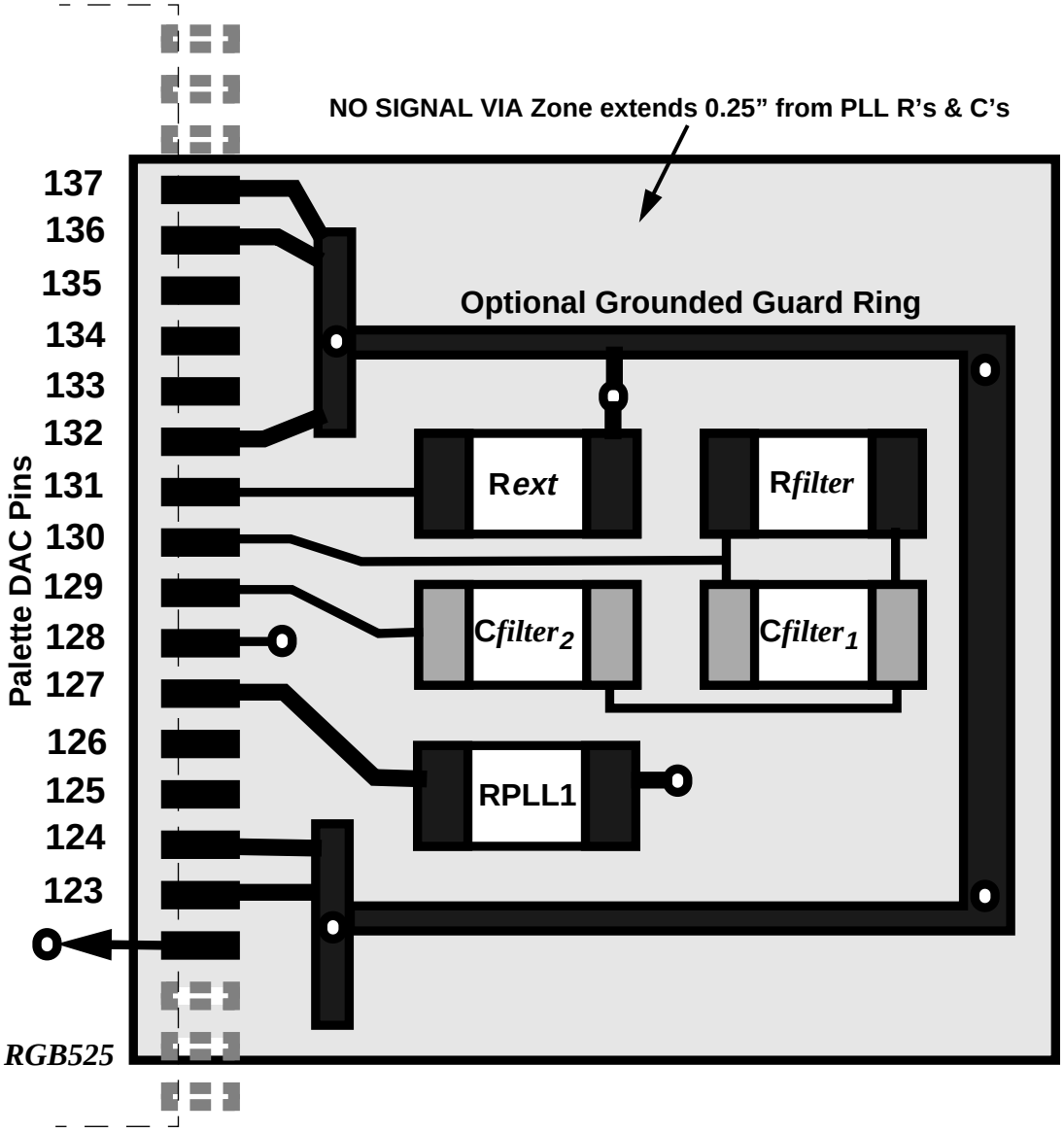


Figure 8. 525 PLL Component Layout

RGB525 contains one PLL for Pixel clock generation. Figure 8 represents an optimal placement for these components. Note that all traces and components are on the top (component) side of the card. Make connections using short direct traces. Do not uses VIAs to connect the components with the exception of PLL VDD and ground. Digital signals that are present on adjacent Palette DAC pins should be swept under the module and connected, by VIA, to wiring planes below the ground plane. Do not route digital signals or place VIAs that support digital nets within the ‘*NO SIGNAL Via Zone*’. The use of a grounded guard ring is recommended.

Five passive components support the PLL function. R*ext* is a 10KΩ resistor that sets the VCO gain. It is connected between module pin 131 and card ground. RPLL1 is a 8.66KΩ resistor that controls the current to the VCO charge pump. It is connected between module pin 127 and the PLL VDD power plane.

The VCO Loop Filter is comprised of R*filter (*1.3KΩ*)*, C*filter*$_1$ (680 pF) and C*filter*$_2$ (8.2 nF). Module pin 130 connects to R*filter*. R*filter* connects in parallel to C*filter*$_1$.The loop filter returns to module pin 129, thru C*filter*$_2$

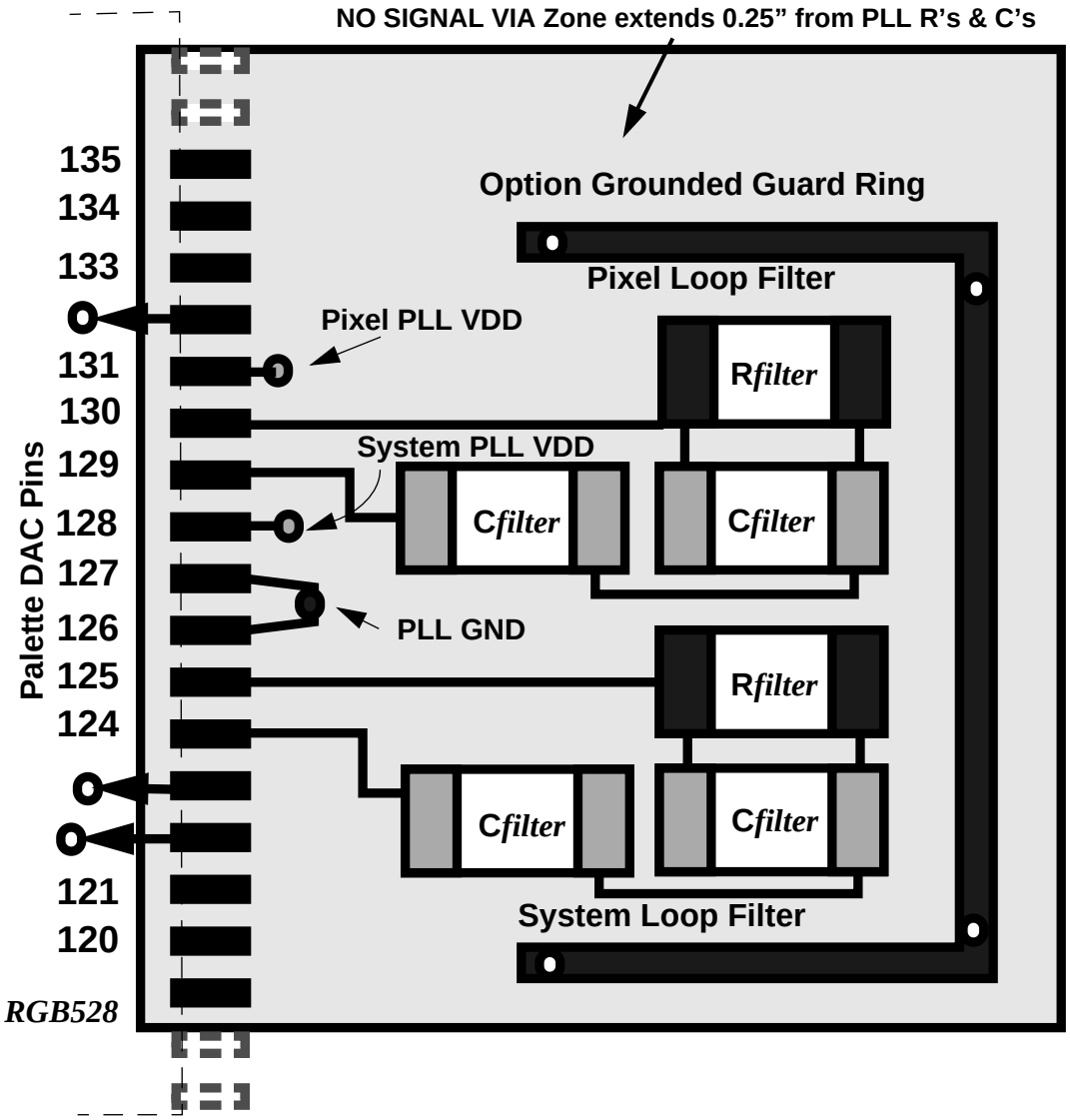


Figure 9. RGB528 PLL Component Layout

The RGB528 contains two PLL’s; one for system clock and one for pixel clock. Figure 9 represents the optimal loop filter component placement when both PLL’s are enabled. All filter wiring should be made on the top (component) side of the card. Make connections using short direct traces. Do not use VIAs to connect the filter components. Do not route digital signals or place VIAs that support digital nets within the ‘*NO SIGNAL Via Zone*’. A grounded guard ring is recommended.

The loop filter components values are identical for both pixel and system PPL filters: R*filter* = 1.3KΩ, C*filter*$_{1}$ = 680 pF and C*filter*$_{1}$ = 8.2 nF.

The *pixel* loop filter connects between pins 129 and 130. VDD for the pixel PLL is supplied on pin 131. The *system* loop filter connects between pins 124 and 125. VDD for the system PLL is supplied on pin 128.

Power for the PLL’s should be provided thru separate System and pixel PLL VDD power planes (see Figure 5 on page 4.) Each plane should be decoupled as recommended in Figure 10 on page 9. Directly connect the PLL grounds (pins 126, 127) to the common card ground by VIA. Use short, wide traces between pin and VIA.

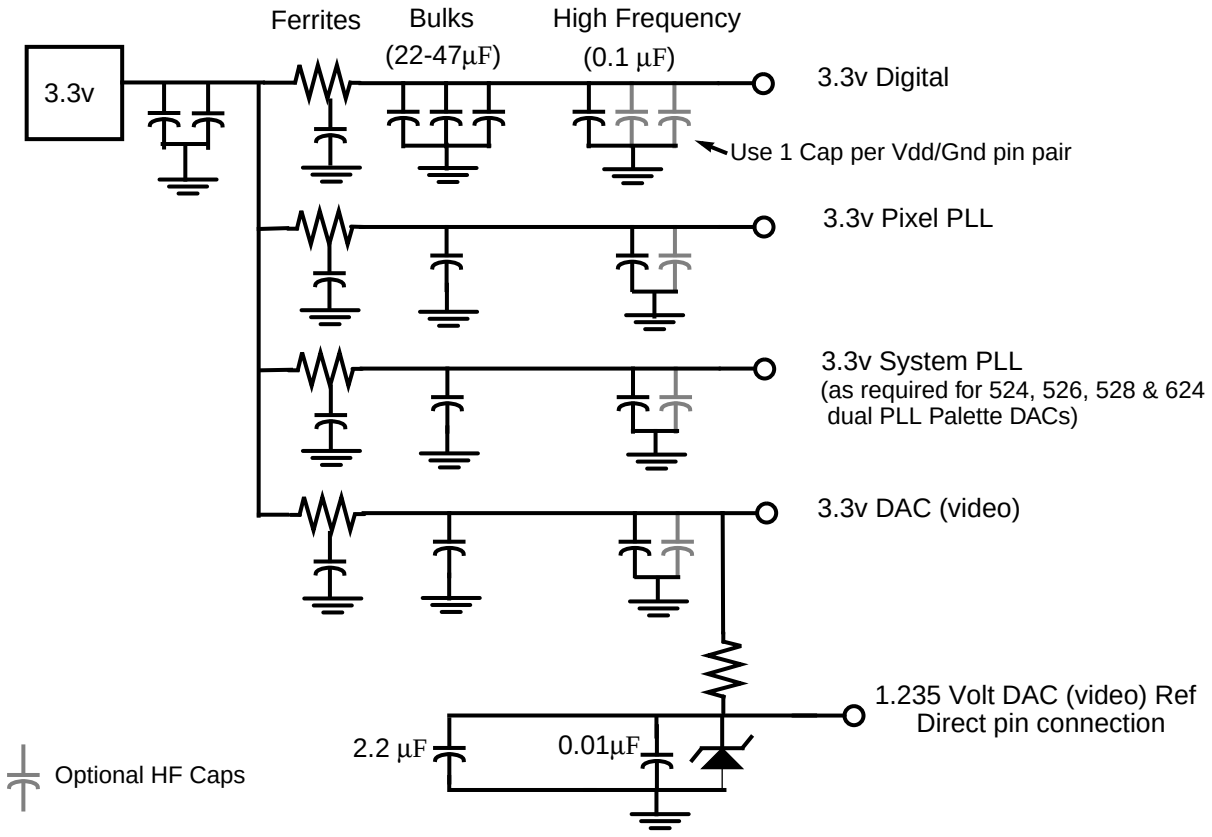


Figure 10. 3.3 Volt Power Network

Figure 10 represents the recommended power network for the Palette DAC products.

1.RGB514, 525 require four power sources for: 1) Digital, 2) Pixel PLL, 3) DAC (video) and 4) DAC reference. RGB524, 526, 528 and 624 require an additional System PLL supply if the Palette DAC system PLL is utilized.

2. Bulk 3.3 volt power can be supplied from an on card regulator or system-card slot. The designer should adequately bulk and high frequency decouple the 3.3 volt supply before sourcing it to the individual power plane.

3. Each Palette DAC power net (above), except for DAC Reference, should feed individual VDD power plane segments (see Figure 5 on page 4). Each segment is a unique power island that is defined within the card's existing VDD plane. Each segment is sourced from the primary 3.3 volt supply by an inductor (e.g., EMI filter, SMT Panasonic EXC-CET103U). Each segment is individually decoupled using bulk and high frequency capacitors.

4. The high frequency capacitors should be located as close as to the module pins as possible. Use short, wide direct traces. Reference Figure 4 on page 4. For digital power, connect one 0.1µF cap at each power/ground pin pair. In general, Palette DAC digital power/ground pins are located at the corners of the module.

5. The 1.235 volt DAC (video) reference voltage is connected directly to the module VREFIN pin and does not require a VDD plane segment.

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY
12533-6531

The IBM home page can be found at
http://www.ibm.com.

The IBM Microelectronics Division home page can be found at
http://www.chips.ibm.com.

Fast Fax Service 415-885-4121

Document No. SK10-3011-00