Bt457/Bt458

125 MHz/135 MHz/165 MHz Monolithic CMOS 256 Color Palette RAMDAC

The Bt457 and Bt458 are pin- and software-compatible RAMDACs designed specifically for high-performance, high-resolution color graphics. The architecture enables a display of 1280 x 1024 bit-mapped color graphics (up to 8 bits per pixel plus up to 2 bits of overlay information). This minimizes the use of costly ECL interfacing, because most of the high-speed (pixel clock) logic is contained on-chip. The multiple pixel ports and internal multiplexing enable TTL-compatible interface (up to 32 MHz) to the frame buffer, while maintaining the 165 MHz video data rates required for sophisticated color graphics.

The Bt457 is a single-channel version of the Bt458 and has a 256 x 8 color lookup table with a single 8-bit video D/A converter. It includes a PLL output to enable subpixel synchronization of multiple Bt457s.

On-chip features include programmable blink rates, bit plane masking and blinking, color overlay capability, and a dual-port color palette RAM.

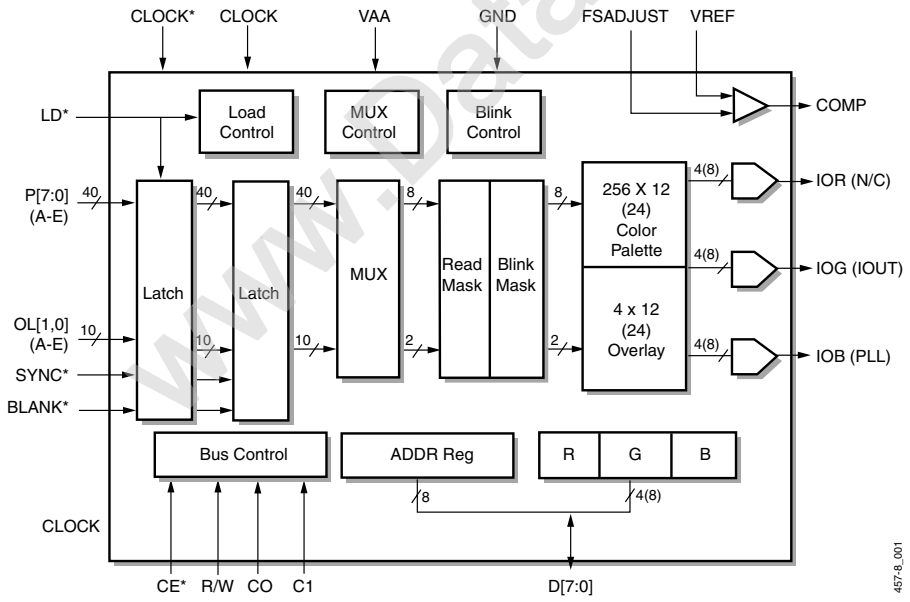
Distinguishing Features

- 165, 135, 125, 110, 80 MHz operation
- 4:1 or 5:1 input mux
- 256-word dual-port color palette
- Four dual-port overlay registers
- RS-343A-compatible outputs
- Bit plane read and blink masks
- Standard MPU interface
- 84-pin PLCC or PGA package
- +5 V CMOS monolithic construction

Applications

- High-resolution color graphics
- CAE/CAD/CAM
- Image processing
- Video reconstruction

Functional Block Diagram



Ordering Information

Model Number	RAM	DACs	Speed	Package	Ambient Temperature Range
Bt458LG165	256 x 24	Triple 8-bit	165 MHz	84-Pin Ceramic PGA	0 to + 70 °C
Bt458KG135	256 x 24	Triple 8-bit	135 MHz	84-Pin Ceramic PGA	0 to + 70 °C
Bt458KG125	256 x 24	Triple 8-bit	125 MHz	84-Pin Ceramic PGA	0 to + 70 °C
Bt458KG110	256 x 24	Triple 8-bit	110 MHz	84-Pin Ceramic PGA	0 to + 70 °C
Bt458KG80	256 x 24	Triple 8-bit	80 MHz	84-Pin Ceramic PGA	0 to + 70 °C
Bt458LPJ165	256 x 24	Triple 8-bit	165 MHz	84-Pin Plastic J-Lead	0 to + 70 °C
Bt458LPJ135	256 x 24	Triple 8-bit	135 MHz	84-Pin Plastic J-Lead	0 to + 70 °C
Bt458LPJ125	256 x 24	Triple 8-bit	125 MHz	84-Pin Plastic J-Lead	0 to + 70 °C
Bt458LPJ110	256 x 24	Triple 8-bit	110 MHz	84-Pin Plastic J-Lead	0 to + 70 °C
Bt458LPJ80	256 x 24	Triple 8-bit	80 MHz	84-Pin Plastic J-Lead	0 to + 70 °C
Bt457KG135	256 x 8	Single 8-bit	135 MHz	84-Pin Ceramic PGA	0 to + 70 °C
Bt457KG125	256 x 8	Single 8-bit	125 MHz	84-Pin Ceramic PGA	0 to + 70 °C
Bt457KG110	256 x 8	Single 8-bit	110 MHz	84-Pin Ceramic PGA	0 to + 70 °C
Bt457KG80	256 x 8	Single 8-bit	80 MHz	84-Pin Ceramic PGA	0 to + 70 °C
Bt457KPJ135	256 x 8	Single 8-bit	135 MHz	84-Pin Plastic J-Lead	0 to + 70 °C
Bt457KPJ125	256 x 8	Single 8-bit	125 MHz	84-Pin Plastic J-Lead	0 to + 70 °C
Bt457KPJ110	256 x 8	Single 8-bit	110 MHz	84-Pin Plastic J-Lead	0 to + 70 °C
Bt457KPJ80	256 x 8	Single 8-bit	80 MHz	84-Pin Plastic J-Lead	0 to + 70 °C

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1.0 Circuit Description

1.1 Pin Descriptions

The Bt457/Bt458 is available in both 84-pin Plastic Leaded Chip Carrier (PLCC) and Ceramic PGA packages, as illustrated in Figures 1-1 and 1-2. Table 1-1 provides pin descriptions. Table 1-2 gives pin labels for the PGA package.

Figure 1-1. Bt457/Bt458 84-Pin J-Lead Package

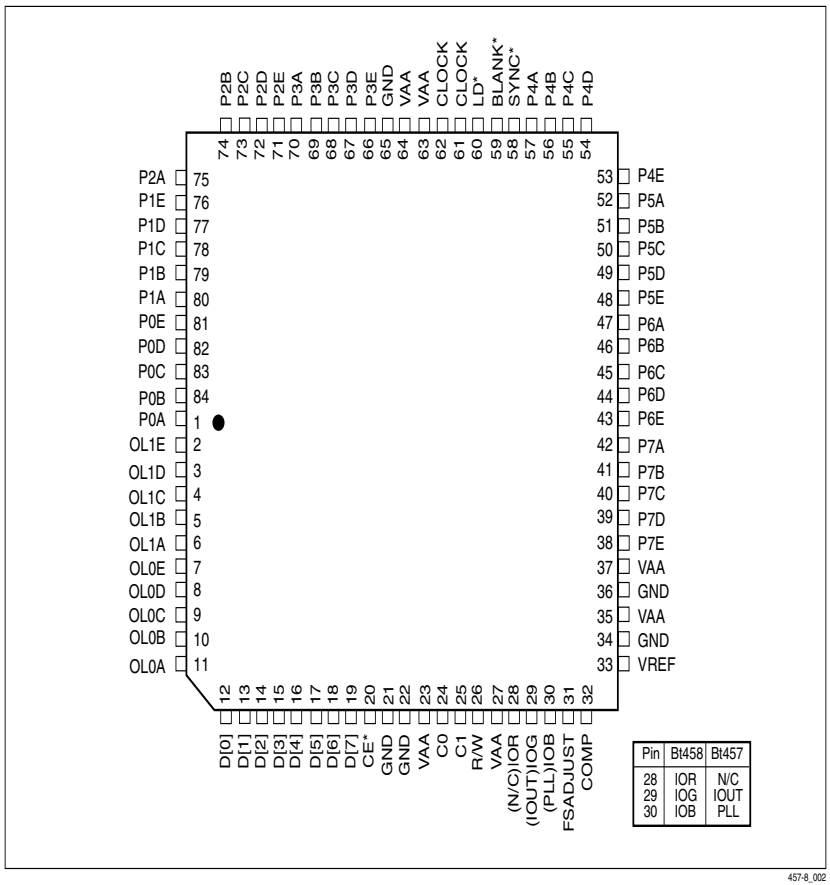
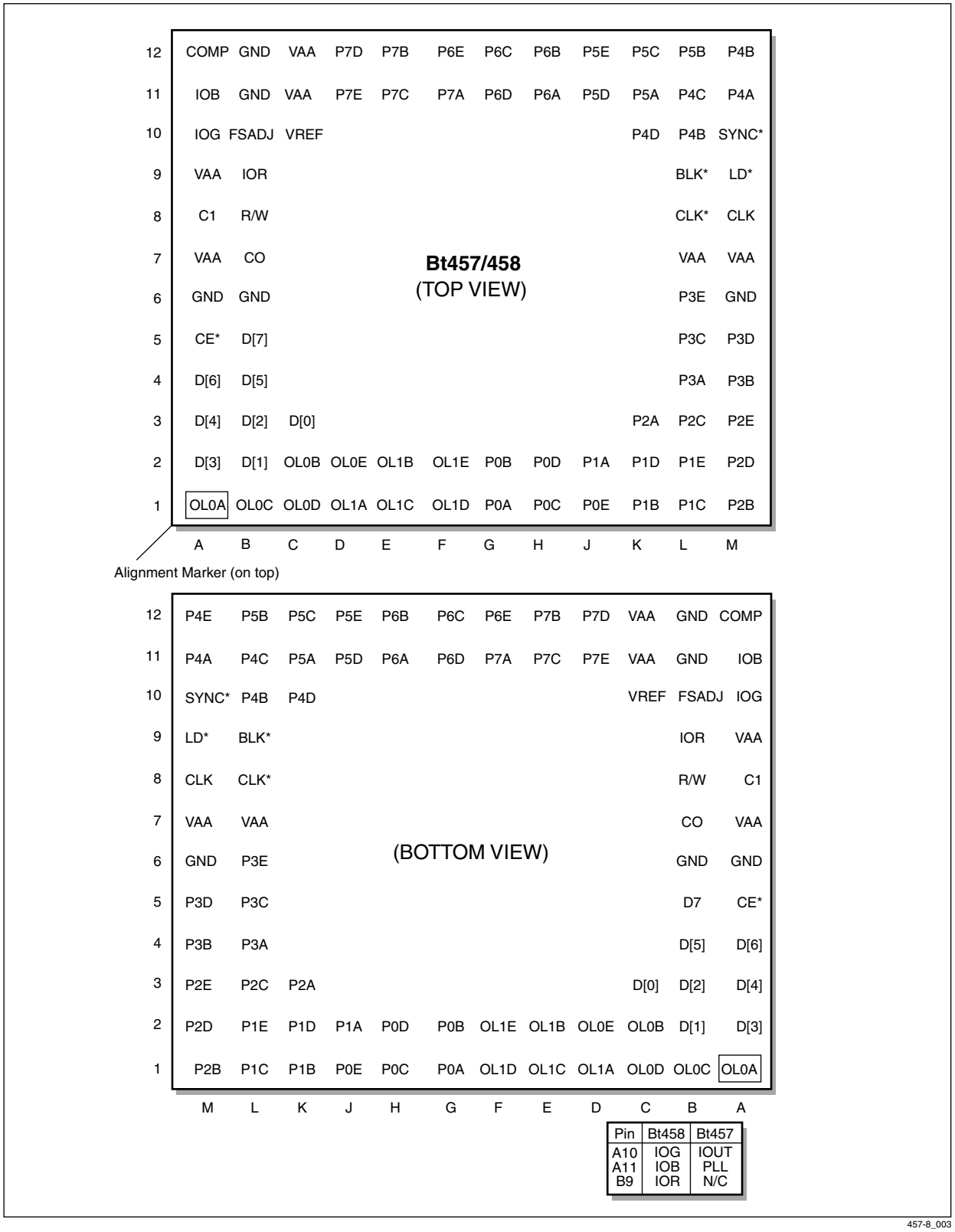


Figure 1-2. Bt457/Bt458 84-Pin PGA Package



1.2 Pin Descriptions

Table 1-1. Pin Descriptions *(1 of 2)*

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical 0 drives the analog outputs to the blanking level, as specified in Table 1-5. BLANK* is latched on the rising edge of LD*. When BLANK* is a logical 0, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical 0 on this input switches off a 40 IRE current source on the IOG output (see Figure 1-4). SYNC* does not override any other control or data input, as illustrated in Table 1-5; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of LD*. If sync information is not generated on the IOG output, this pin should be connected to GND.
LD*	Load control input (TTL compatible). The P[7:0] {A–E}, OL[1,0] {A–E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. While LD* is either one fourth or one fifth the CLOCK rate, it can be phase independent of the CLOCK and CLOCK* inputs. LD* can have any duty cycle within the limits specified in the AC Characteristics section.
P[7:0] {A–E}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which of the 256 entries in the color palette RAM is used to provide color information. Either 4 or 5 consecutive pixels (up to 8 bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. The {A} pixel is output first, followed by the {B} pixel, then the {C} pixel, etc., until all 4 or 5 pixels have been output, at which point the cycle repeats.
OL[1,0] {A–E}	Overlay select inputs (TTL compatible). These control inputs are latched on the rising edge of LD*. In conjunction with bit 6 of the command register, they specify which palette is to be used for color information, as follows: **OL1 / OL0 / CR6 = 1 / CR6 = 0** 0 / 0 / Color Palette RAM / Overlay Color 0 0 / 1 / Overlay Color 1 / Overlay Color 1 1 / 0 / Overlay Color 2 / Overlay Color 2 1 / 1 / Overlay Color 3 / Overlay Color 3 When accessing the overlay palette, the P[7:0] {A–E} inputs are ignored. Overlay information bits (up to 2 bits per pixel) for either 4 or 5 consecutive pixels are input through this port. Unused inputs should be connected to GND.
IOR, IOG, IOB, IOUT	Red, green, and blue video current outputs. These high-impedance current sources can directly drive a doubly terminated 75 Ω coaxial cable (see Figure 3-2). The Bt457 outputs IOUT rather than IOR, IOG, and IOB.

Table 1-1. Pin Descriptions *(2 of 2)*

Pin Name	Description
PLL	Phase lock loop current output—Bt457 only. This high-impedance current source is used to enable multiple Bt457s to be synchronized with subpixel resolution when used with an external PLL. A logical 1 on the BLANK* input results in no current being output onto this pin, while a logical 0 results in the following current being output: PLL (mA) = 3,227 * VREF (V) / RSET (Ω) If subpixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 Ω).
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 3-2). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and to maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. The PC Board Layout Considerations section contains critical layout criteria.
FSADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 3-1). The IRE relationships in Figure 1-4 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG (or IOUT for the Bt457) is as follows: RSET (Ω) = 11,294 * VREF (V) / IOG (mA) The full-scale output current on IOR and IOB (for the Bt458) for a given RSET is as follows: IOR, IOB (mA) = 8,067 * VREF (V) / RSET (Ω)
VREF	Voltage reference input. An external voltage reference circuit, such as that illustrated in Figure 3-2, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, because any low-frequency power supply noise on VREF is directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 3-2. If VAA is excessively noisy, better performance can be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are driven by ECL logic configured for single-supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system. Refer to the PC Board Layout Considerations section for critical layout criteria.
CE*	Chip enable control input (TTL compatible). This input must be a logical 0 to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Glitches should be avoided on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical 0. To read data from the device, CE* must be a logical 0 and R/W must be a logical 1. R/W is latched on the falling edge of CE*.
C[1,0]	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as presented in Table 1-3. They are latched on the falling edge of CE*.
D[7:0]	Data bus (TTL compatible). Data transfers into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.

Table 1-2. Pin Labels

Pin Number	Pin Label	Pin Number	Pin Label	Pin Number	Pin Label
L9	BLANK*	K11	P5A	C12	VAA
M10	SYNC*	L12	P5B	C11	VAA
M9	LD*	K12	P5C	A9	VAA
L8	CLOCK*	J11	P5D	L7	VAA
M8	CLOCK	J12	P5E	M7	VAA
				A7	VAA
G1	P0A	H11	P6A		
G2	P0B	H12	P6B	B12	GND
H1	P0C	G12	P6C	B11	GND
H2	P0D	G11	P6D	M6	GND
J1	P0E	F12	P6E	B6	GND
				A6	GND
J2	P1A	F11	P7A		
K1	P1B	E12	P7B	A12	COMP
L1	P1C	E11	P7C	B10	FS ADJUST
K2	P1D	D12	P7D	C10	VREF
L2	P1E	D11	P7E		
				A5	CE*
K3	P2A	A1	OL0A	B8	R/W
M1	P2B	C2	OL0B	A8	C1
L3	P2C	B1	OL0C	B7	C0
M2	P2D	C1	OL0D		
M3	P2E	D2	OL0E	C3	D[0]
				B2	D[1]
L4	P3A	D1	OL1A	B3	D[2]
M4	P3B	E2	OL1B	A2	D[3]
L5	P3C	E1	OL1C	A3	D[4]
M5	P3D	F1	OL1D	B4	D[5]
L6	P3E	F2	OL1E	A4	D[6]
				B5	D[7]
M11	P4A	A10	IOG(IOUT)		
L10	P4B	A11	IOB (PLL)		
L11	P4C	B9	IOR (N/C)		
K10	P4D				
M12	P4E				

NOTE(S): Bt457 Pin names are in parentheses.

1.3 MPU Interface

As illustrated in the functional block diagram on the cover page, the Bt457/458 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and dual-port overlay registers allow color updating, without contention, with the display refresh process.

As presented in Table 1-3, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register, color palette RAM entry, or overlay register is accessed by the MPU.

The 8-bit address register (ADDR[7:0]) is used to address the internal RAM and registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D[0] and is the least significant bit.

Table 1-3. Address Register (ADDR) Operation

ADDR[7:0]	C1	C0	Addressed by MPU
$xx	0	0	Address Register
$00–$FF	0	1	Color Palette RAM
$00	1	1	Overlay Color 0
$01	1	1	Overlay Color 1
$02	1	1	Overlay Color 2
$03	1	1	Overlay Color 3
$04	1	0	Read Mask Register
$05	1	0	Blink Mask Register
$06	1	0	Command Register
$07	1	0	Control/Test Register

Bt458 Reading/Writing Color Data

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU can modify by writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location, which the MPU can read by reading another sequence of red, green, and blue data.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay register three. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits that count modulo three. They are reset to 0 when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR[7:0]) are accessible to the MPU.

Bt457 Reading/Writing Color Data (Normal Mode)

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs a color write cycle, using C0 and C1 to select either the color palette RAM or the overlay registers. The address register then increments to the next location, which the MPU can modify by writing another color.

Reading color data is similar to writing it, except the MPU executes read cycles.

This mode is useful if a 24-bit data bus is available, because 24 bits of color information (8 bits each of red, green, and blue) can be read or written to three Bt457s in a single MPU cycle. In this application, the CE* inputs of all three Bt457s are connected together. If only an 8-bit data bus is available, the CE* inputs must be individually selected during the appropriate color write cycle (red CE* during red write cycle, blue CE* during blue write cycle, and green CE* during green write cycle).

When accessing the color palette RAM, the address register resets to $00 after a read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a read or write cycle to overlay register three.

Bt457 Reading/Writing Color Data (RGB Mode)

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the color palette RAM or the overlay registers. After the blue write cycle, the address register then increments to the next location, which the MPU can modify by writing another sequence of red, green, and blue data. Reading color data is similar to writing it, except the MPU executes read cycles.

This mode is useful if only an 8-bit data bus is available. Each Bt457 is programmed to be a red, green, or blue RAMDAC and responds only to the assigned color read or write cycle. In this application, the Bt457s share a common 8-bit data bus. The CE* inputs of all three Bt457s must be asserted simultaneously only during color read/write cycles and address register write cycles.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay register three. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits that count modulo three. They are reset to 0 when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR[7:0]) are accessible to the MPU.

Additional Information

Although the color palette RAM and overlay registers are dual-ported, if the pixel and overlay data are addressing the same palette entry being written to by the MPU during the write cycle, one or more of the pixels on the display screen can be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

The control registers are also accessed through the address register in conjunction with the C0 and C1 inputs, as specified in Table 1-3. All control registers can be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations.

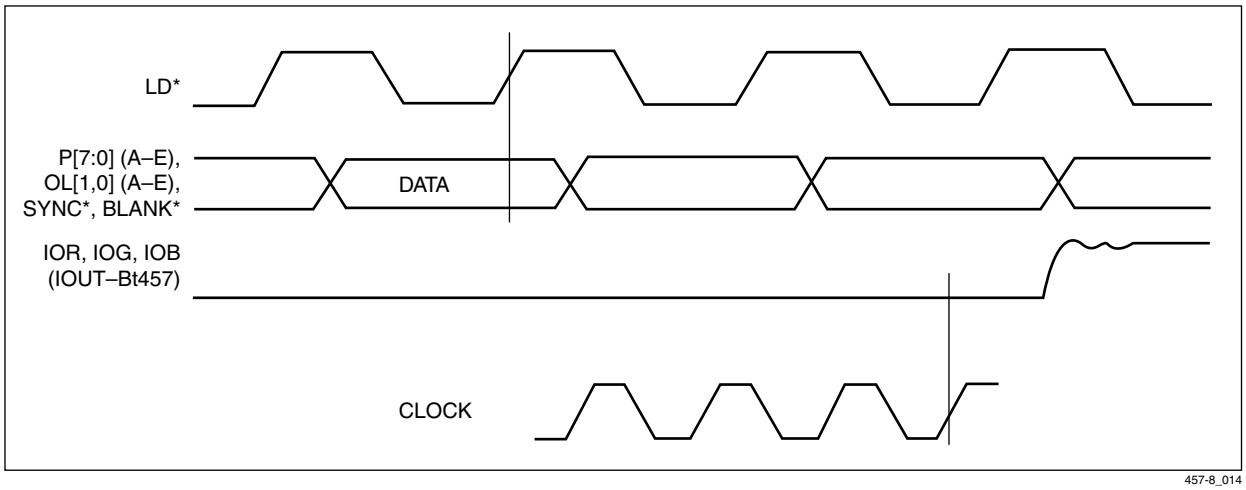
If an invalid address loads into the address register, data written to the device is ignored, and invalid data is read by the MPU.

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt457/458 incorporates internal latches and multiplexers. As illustrated in Figure 1-3, on the rising edge of LD*, sync and blank information, color (up to 8 bits per pixel), and overlay (up to 2 bits per pixel) information, for either 4 or 5 consecutive pixels, are latched into the device. With this configuration, the sync and blank timing is recognized only with 4- or 5-pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate basic video timing.

Each clock cycle, the Bt457/458 outputs color information based on the {A} inputs, followed by the {B} inputs, then the {C} inputs, etc., until all 4 or 5 pixels have been output, at which point the cycle repeats.

Figure 1-3. Video Input/Output Timing



The overlay inputs can have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis. On the other hand, they can be controlled by external character or cursor generation logic.

To simplify the frame buffer interface timing, LD* can be phase shifted in any amount relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by 4 or 5 independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal synchronous to CLOCK and is guaranteed to follow the LD* signal by at least one, but not more than four, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every five clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal and continuously attempts to resynchronize itself to LD*.

Color Selection

Each clock cycle, 8 bits of color information (P7:0) and 2 bits of overlay information (OL1,0) for each pixel are processed by the read mask, blink mask, and command registers. Through the control registers, individual bit planes can be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure blinking does not cause a color change to occur during the active display time (i.e., in the middle of the screen), the Bt457/458 monitors the BLANK* input to determine vertical retrace intervals. A vertical retrace interval is recognized by determining that BLANK* has been a logical 0 for at least 256 LD* cycles.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. P[0] is the LSB when addressing the color palette RAM. Table 1-4 is the truth table used for color selection.

Table 1-4. Palette and Overlay Select Truth Table

CR[6]	OL[1]	OL[0]	P[7:0]	Addressed by Frame
1	0	0	$00	Color Palette Entry $00
1	0	0	$01	Color Palette Entry $01
:	:	:	:	:
1	0	0	$FF	Color Palette Entry $FF
0	0	0	$xx	Overlay Color 0
x	0	1	$xx	Overlay Color 1
x	1	0	$xx	Overlay Color 2
x	1	1	$xx	Overlay Color 3

Video Generation

Every clock cycle, the selected color information, from the color palette RAMs or overlay registers, is presented to the D/A converters.

The SYNC* and BLANK* inputs are pipelined to maintain synchronization with the pixel data. They add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as described in Figure 1-4.

Varying output current from each D/A converter produces a corresponding voltage level, used to drive the color CRT monitor. Only the green output (IOG) on the Bt458 contains sync information. Table 1-5 details how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt457 and Bt458 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for

precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the D/A converter's full-scale output current against temperature and power supply variations.

Figure 1-4. Composite Video Output Waveforms

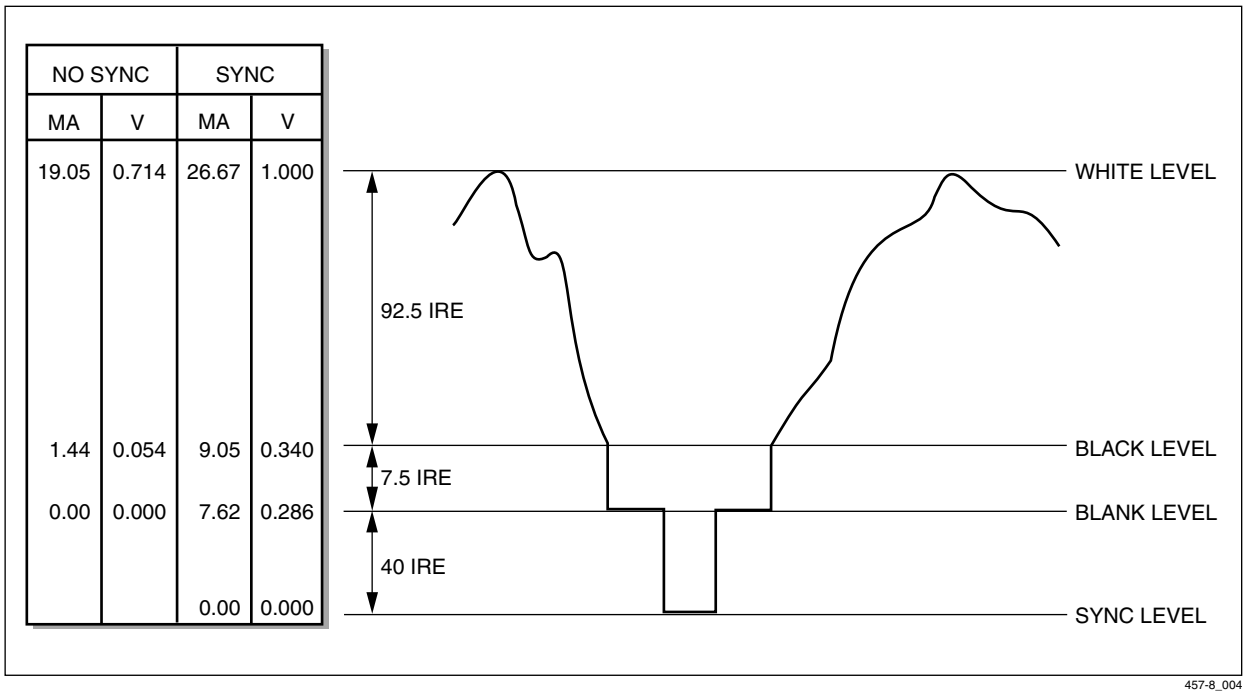


Table 1-5. Video Output Truth Table

Description	IOG (Iout) (mA)	IOR, IOB (mA)	Sync*	BLANK*	DAC Input Data
White	26.67	19.5	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK-SYNC	1.44	1.44	0	1	$00
BLACK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx
NOTE(S): Typical with full-scale IOG = 26.67 mA. RSET = 523 Ω and VREF = 1.235 V.					

2.0 Registers

2.1 Internal

2.1.1 Command Register

The command register can be written or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR0 corresponds to data bus bit D[0].

Table 2-1. Command Registers *(1 of 2)*

Function			Description
CR7	Multiplex select		This bit specifies whether 4:1 or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 4:1 is specified, the {E} pixel and {E} overlay inputs are ignored and should be connected to GND, and the LD* input should be one fourth the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be one fifth the CLOCK rate. The pipeline delay of the Bt457/458 can be reset to a fixed eight clock cycles. In this instance, each time the input multiplexing is changed, the Bt457/458 must again be reset to a fixed pipeline delay.
	(0) (1)	4:1 Multiplexing 5:1 Multiplexing	
CR6	RAM Enable		When the overlay select bits are 00, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information.
	(0) (1)	Use Overlay Color 0 Use Color Palette RAM	
CR5,4	Blink Rate Selection		These 2 bits control the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (percent on/off).
	(00) (01) (10) (11)	16 on, 48 off (25/75) 16 on, 16 off (50/50) 32 on, 32 off (50/50) 64 on, 64 off (50/50)	
CR3	OL1 Blink Enable		If a logical 1, this bit forces the OL1 {A–E} inputs to toggle between a logical 0 and the input value at the selected blink rate prior to palette section. A value of logical 0 does not affect the value of the OL1 {A–E} inputs. In order for overlay 1 bit plane to blink, bit CR1 must be set to a logical 1.

Table 2-1. Command Registers *(2 of 2)*

Function			Description
CR2	OL0 Blink Enable		If a logical 1, this bit forces the OL0 {A–E} inputs to toggle between a logical 0 and the input value at the selected blink rate prior to palette selection. A value of the logical 0 does not affect the value of the OL0 {A–E} inputs. In order for overlay 0 bit plane to blink, bit CR0 must be set to a logical 1.
CR1	OL1 Display Enable		If a logical 0, this bit forces the OL1 {A–E} inputs to a logical 0 prior to selecting the palettes. A value of a logical 1 does not affect the value of the OL1 {A–E} inputs.
	(0) (1)	Disable Enable	
CR0	OL0 Display Enable		If a logical 0, this bit forces the OL0 {A–E} inputs to a logical 0 prior to selecting the palettes. A value of a logical 1 does not affect the value of the OL0 {A–E} inputs.
	(0) (1)	Disable Enable	

2.2 Read Mask Register

The read mask register enables (logical 1) or disables (logical 0) a bit plane from addressing the color palette RAM. D[0] corresponds to bit plane 0 (P0 {A–E}), and D[7] corresponds to bit plane 7 (P7 {A–E}). Each register bit is logically ANDed with the corresponding bit plane input. This register can be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

2.3 Blink Mask Register

The blink mask register enables (logical 1) or disables (logical 0) a bit plane from blinking at the blink rate and duty cycle specified by the command register. D[0] corresponds to bit plane 0 (P0 {A–E}), and D[7] corresponds to bit plane 7 (P7 {A–E}). In order for a bit plane to blink, the corresponding bit in the read mask register must be a logical 1. This register can be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

2.4 Bt458 Test Register

The test register provides diagnostic capability by enabling the MPU to read the D/A converters inputs. It can be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. When writing to the register, the upper 4 bits (D[7:4]) are ignored.

The contents of the test register are defined as follows:

Table 2-2. Bt458 Test Register

D[7:4]	Color Information
D[3]	Low (Logical 1) or High (Logical 0) Nibble
D[2]	Blue Enable
D[1]	Green Enable
D[0]	Red Enable

To use the test register, the host MPU writes to it, setting only one of the red, green, or blue enable bits. These bits specify which four bits of color information the MPU wishes to read (R[3:0], G[3:0], B[3:0], R[7:4], G[7:4], or B[7:4]). When the MPU reads the test register, the four bits of color information from the DAC

inputs are contained in the upper four bits, and the lower four bits contain the red, green, blue, and low or high nibble enable information previously written. Either the CLOCK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

For example, to read the upper four bits of red color information being presented to the D/A converters, the MPU writes to the test register, setting only the red enable bit. The MPU then reads the test register, keeping the pixel data stable, which results in D[7:4] containing R[7:4] color bits and D[3:0] containing red, green, blue, and low or high nibble enable information, as illustrated below:

D[7]	R7
D[6]	R6
D[5]	R5
D[4]	R4
D[3]	0
D[2]	0
D[1]	0
D[0]	1

2.5 Bt457 Control/Test Register

The control/test register provides diagnostic capability by enabling the MPU to read the D/A converter inputs. It can be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. When writing to the register, the upper four bits (D[7:4]) are ignored.

The contents of the test register are defined as follows:

Table 2-3. Bt457 Control Test Register

D[7:4]	Color Information
D[3]	Low (Logical 1) or High (Logical 0) Nibble
D[2]	Blue Channel Enable
D[1]	Green Channel Enable
D[0]	Red Channel Enable

To use the control/test register, the MPU writes to it, specifying the low or high nibble of color information. When the MPU reads the register, the four bits of color information from the DAC inputs are contained in the upper four bits, and the lower four bits contain whatever was previously written to the register. Either the CLOCK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

The red, green, and blue enable bits specify the mode in which color data is written to and read from, the Bt457. If all three enable bits are logical 0s, each write cycle to the color palette RAM or overlay registers loads 8 bits of color data. During each read cycle of the color palette RAM or overlay registers, 8 bits of color data are output onto the data bus. If a 24-bit data bus is available, three Bt457s can be accessed simultaneously.

If any of the red, green, or blue enable bits is a logical 1, the Bt457 assumes the MPU is reading and writing color information using red-green-blue cycles, such as are used in the Bt458. Setting the appropriate enable bit configures the Bt457 to output or input color data only for the color read/write cycle corresponding to the enabled color. Thus, if the green enable bit is a logical 1, and a red-green-blue write cycle occurred, the Bt457 would input data only during the green write cycle. If a red-green-blue read cycle occurred, the Bt457 would output data only during the green read cycle. CE* must be a logical 0 during each of the red-green-blue cycles. Only one of the enable bits must be a logical 1. This mode of operation is useful when only an 8-bit data bus is available and the software drivers are written for RGB operation.

3.0 PC Board Layout Considerations

3.1 PC Board Considerations

The Bt457 and Bt458 layouts should be optimized for lowest noise on their power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

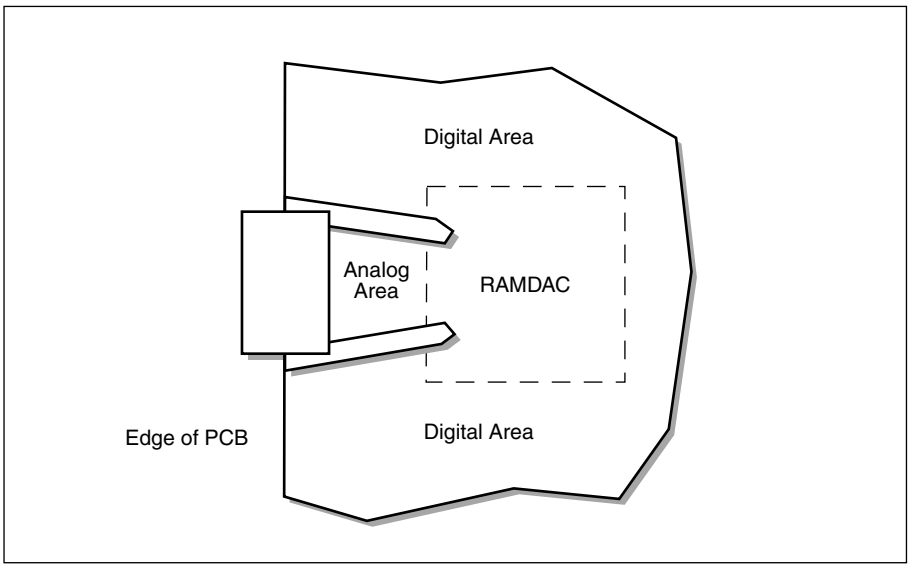
A well-designed power distribution network is critical to eliminate digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer is used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer two the ground plane, layer three the analog power plane, and the remaining layers used for digital traces and digital power supplies.

The optimum layout enables the Bt457 and Bt458 to be located as close as possible to the power supply connector and the video output connector.

3.2 Power and Ground Planes

Power and ground planes need isolation gaps to minimize digital switching noise effects on the analog signals and components. These gaps need to be at least 1/8-inch wide. They are placed so that digital currents cannot flow through a peninsula that contains the analog components, signals, and video connector. Figure 3-1 illustrates a sample layout.

Figure 3-1. Sample Layout Showing Power and Ground Plane Isolation Gaps



3.3 Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, using the shortest possible leads (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors can be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values chosen have self-resonance above the pixel clock.

3.4 Power Supply Decoupling

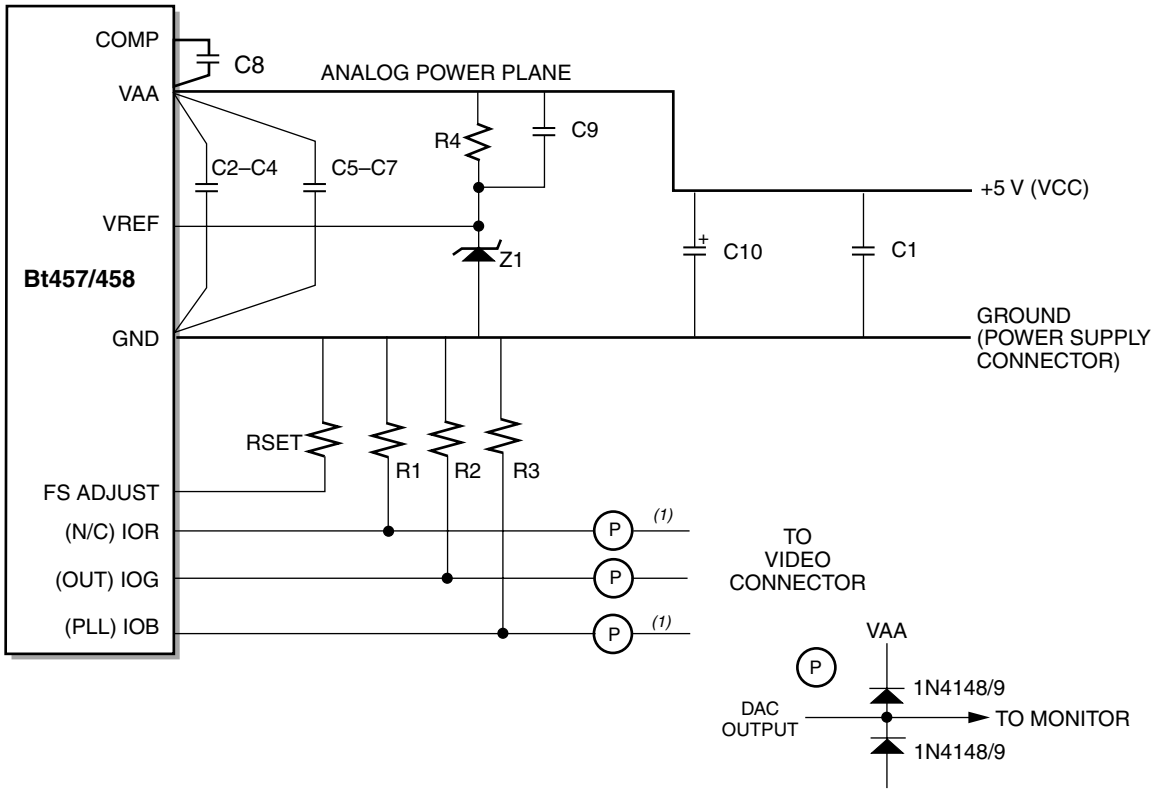
The best power supply decoupling performance is obtained by providing a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor to decouple each group of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins.

The 10 µF capacitor illustrated in Figure 3-2 is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection. The decoupling capacitors should be connected at the VAA and GND pins, using short, wide traces.

When using a linear regulator, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than 200 mV. This is especially important when using a switching power supply and the switching frequency is close to the raster scan frequency.

NOTE: About 10 percent of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

Figure 3-2. Typical Connection Diagram



NOTE(S):
(1) Not used with Bt457.
2. Bt457 pin names are in parentheses. Each pair of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors

457-8_006

Table 3-1. Typical Parts List

Location	Description‘	Vendor Part Number
C1–C4, C8, C9	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C5–C7	0.01 µF Ceramic Chip Capacitor	AVX 12102T103QA1018
C10	10 µF Tantalum Capacitor	Mallory CSR13G106KM
L1	Ferrite Bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% Metal Film Resistor	Dale CMF-55C
R4	1000 Ω 1% Metal Film Resistor	Dale CMF-55C
RSET	523 Ω 1% Metal Film Resistor	Dale CMF-55C
Z1	1.2 V Voltage Reference	National Semiconductor LM385Z-1.2
NOTE(S): The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics does not affect the performance of the Bt457/458. R3 is not used with Bt457 (see Section 4.0, *Application Information*).		

3.5 COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise requires a larger value. The COMP capacitor must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces also reduce lead inductance.

If the display has a ghosting problem, additional capacitance connected in parallel with the COMP capacitor can help.

3.6 Digital Signal Interconnect

Digital inputs to the Bt457 and Bt458 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs is caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should be no faster than necessary, because feedthrough noise is proportional to the digital edge rates. Lower speed applications benefit from using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines mismatch if the lines do not match the source and destination impedance. This degrades signal fidelity if the line length reflection time is greater than one fourth the signal edge time. Line termination or line length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than four inches without using termination. Ringing can be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the signals 90 degrees to any analog signals.

The clock driver and all other digital devices on the circuit board must be adequately decoupled to prevent the noise generated by digital devices from coupling into the analog circuitry.

3.7 Analog Signal Interconnect

The Bt457 and Bt458 should be located as close as possible to the output connectors. This minimizes noise pickup and reflections caused by impedance mismatch.

Analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

3.8 Analog Output Protection

The Bt457 and Bt458 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from “hot-switching” AC-coupled monitors.

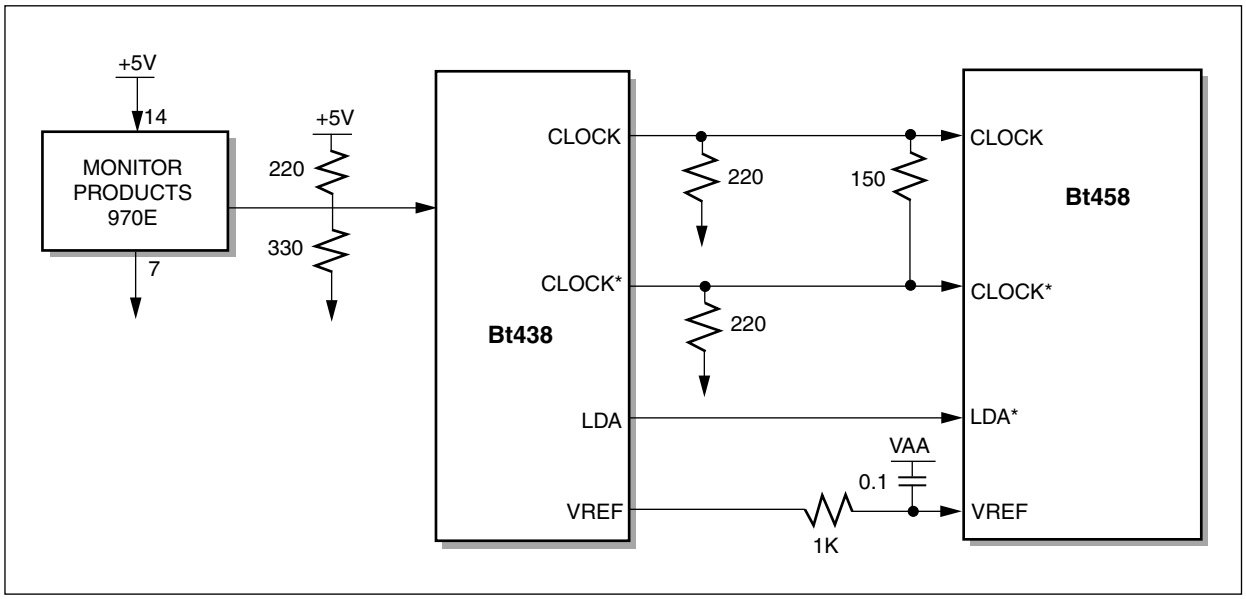
The diode protection circuit illustrated in Figure 3-2 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

4.0 Application Information

4.1 Clock Interfacing

Because of the high clock rates at which the Bt457 and Bt458 can operate, they will accept differential clock signals (CLOCK and CLOCK*). These clock inputs are generated by ECL logic operating at +5 V. The CLOCK and CLOCK* inputs require termination resistors (220 Ω to GND) that should be located as close as possible to the clock driver. A 150 Ω chip resistor connected between the RAMDAC's CLOCK and CLOCK* pins is also required to ensure proper termination. It should be located as close as possible to the RAMDAC. Figure 4-1 illustrates the location.

Figure 4-1. Generating the Bt458 Clock Signals



Applications of 165 MHz require robust ECL clock signals with strong pulldown (–20 mA at VOH) and double termination for clock trace lengths greater than 2 inches.

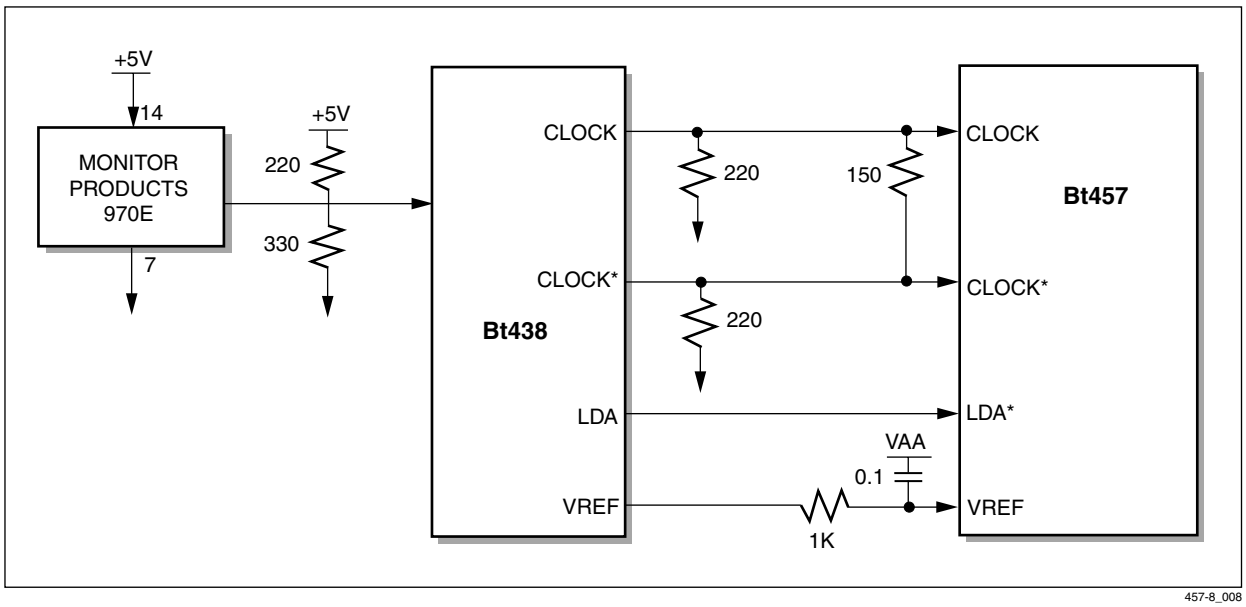
The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak to peak because of the noise margins of the CMOS process. The Bt457/458 will not function if it uses a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by 4 or 5 (depending on whether 4:1 or 5:1 multiplexing was specified) and translating the result to TTL levels. As LD* can be phase shifted relative to CLOCK, propagation delays need not be considered when the LD* signal is derived. LD* can be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (e.g., SYNC* and BLANK*).

It is recommended that the Bt438 or Bt439 Clock Generator Chips be used to generate the clock and load signals. Both support the 4:1 and 5:1 input multiplexing of the Bt457/458, and set the pipeline delay of the Bt457 and Bt458 to eight clock cycles. Figure 4-1 and Figure 4-2 illustrate use of the Bt438 with the Bt457/458.

When a single Bt457 is used, the PLL output is ignored and should be connected to GND (either directly or through a resistor up to 150 Ω).

Figure 4-2. Generating the Bt457 Signals (Monochrome Application)



Setting the Pipeline Delay (Bt457 and Bt458)

The pipeline delay of the Bt457/458, although fixed after a power-up condition, can be anywhere from six to ten clock cycles. The Bt457/458 contains additional circuitry enabling the pipeline delay to be fixed at eight clock cycles. The Bt438 and Bt439 Clock Generator Chips support this mode of operation when they are used with the Bt457/458.

To reset the Bt457/458, it should be powered up with LD*, CLOCK, and CLOCK* running. The CLOCK and CLOCK* signals should be stopped with CLOCK high and CLOCK* low for at least three rising edges of LD*. The device can be held with CLOCK and CLOCK* stopped for an unlimited time.

CLOCK and CLOCK* should be restarted so that the first edge of the signals is as close as possible to the rising edge of LD*. (The falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When the clocks are restarted, the minimum clock pulse width must not be violated.

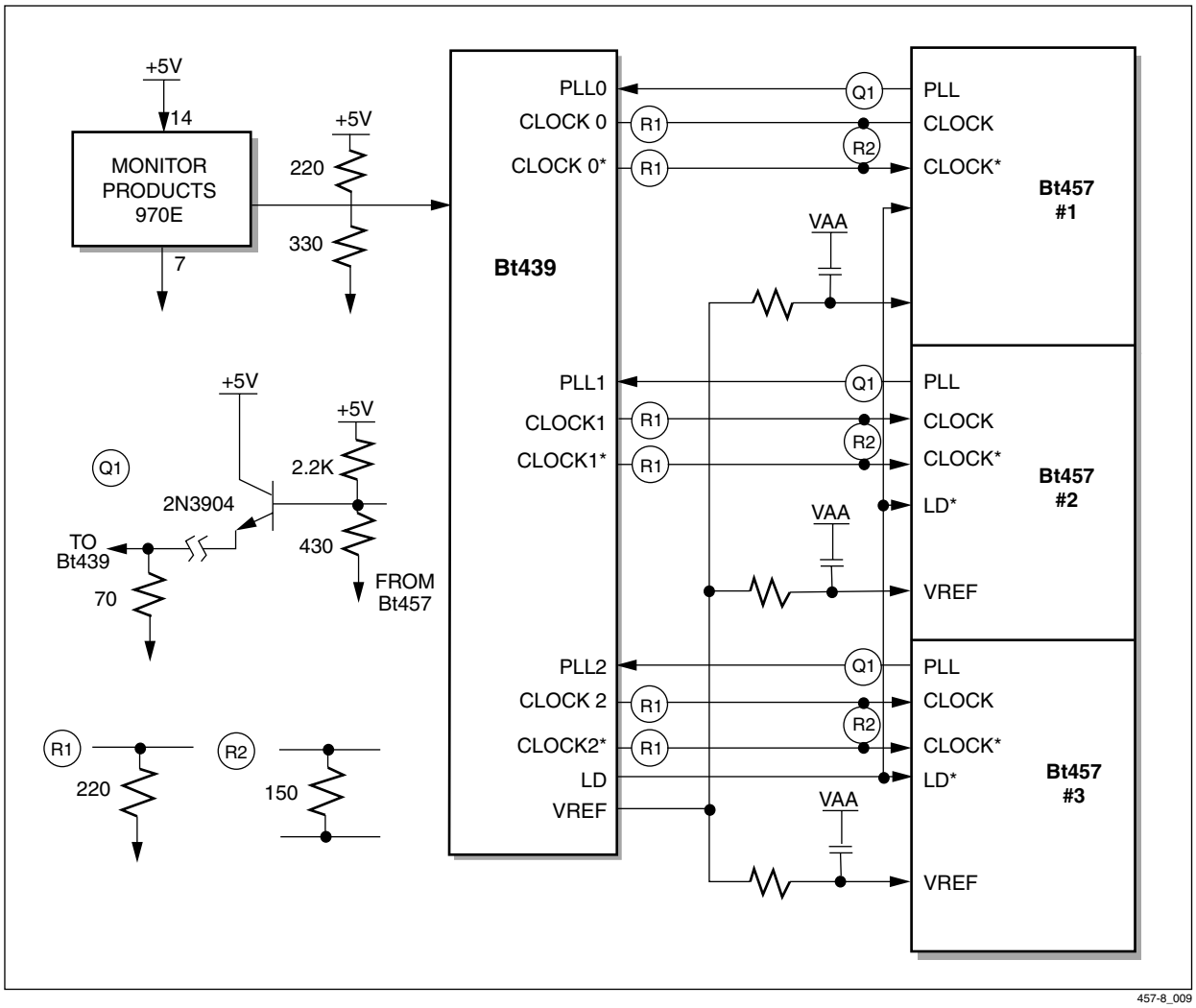
When the Bt457/458 is reset to an eight-clock-cycle pipeline delay, the blink counter circuitry is not reset. Therefore, if multiple Bt457/458s are used in parallel, the on-chip blink counters cannot be synchronized. In this instance, the blink mask register should be $00, and the overlay blink enable bits should be logical 0s. Software can control blinking through the read mask register and overlay display enable bits.

In standard operation, the Bt457/458 must be reset only following a power-up or reset condition. Under these circumstances the on-chip blink circuitry can be used.

Bt457 Color Display Applications

For color display applications in which up to four Bt457s are used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 and 5:1 input multiplexing of the Bt457, synchronizes the clock and load signals to subpixel resolution, and sets the pipeline delay of the Bt457 to eight clock cycles. The Bt439 can also be used to interface the Bt457 to a TTL clock. Figure 4-3 illustrates use of the Bt439 with the Bt457.

Figure 4-3. Generating the Bt457 Clock Signals (Color Application)



Subpixel synchronization is supported by the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt457 relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by up to four Bt457s, and adjusts the phase of each of the CLOCK and CLOCK* signals to the Bt457s to minimize the PLL phase difference. There should be minimal layout skew in the CLOCK and PLL trace paths to ensure proper clock alignment.

If subpixel synchronization of multiple Bt457s is not necessary, the Bt438 Clock Generator Chip can be used rather than the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt457s are connected together and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). The VREF inputs of the Bt457s must still have a 0.1 µF bypass capacitor to VAA. The PLL outputs would not be used and should be connected to GND (either directly or through a resistor up to 150 Ω).

4.2 Using Multiple Devices

When multiple RAMDACs are used, each RAMDAC should have its own power plane ferrite bead. In addition, a single voltage reference can drive multiple devices; however, isolation resistors are recommended to reduce color channel crosstalk.

Higher performance can be obtained if each RAMDAC has its own voltage reference. This can further reduce the amount of color channel crosstalk and color palette interaction.

Each RAMDAC must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

4.3 Bt457 Nonvideo Applications

The Bt457 can be used in nonvideo applications by disabling the video-specific control signals. SYNC* should be a logical 0, and BLANK* should be a logical 1.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

$$RSET\ (\Omega) = 7{,}457 * VREF\ (V) / Iout\ (mA)$$

With the DAC data inputs at $00, there is a DC offset current (Imin) defined as follows:

$$Imin\ (mA) = 610 * VREF\ (V) / RSET\ (\Omega)$$

Therefore, the total full-scale output current is Iout + Imin.

4.4 Initializing the Bt458

Following a power-on sequence, the Bt458 must be initialized. If the clock/LD* sequence is controlled to reset the pipeline delay of the Bt458 to a fixed pipeline delay of eight clock cycles, this initialization sequence must be performed after the reset sequence. The command register must also be reinitialized when the multiplex selection changes (e.g., from 4:1 to 5:1 input multiplexing).

This sequence configures the Bt458 as follows:

4:1 Multiplexed Operation
No Overlays
No Blinking

Control Register Initialization	**C1,C0**
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $00 to test register	10
Color Palette RAM Initialization	
Write $00 to address register	00
Write red data to RAM (location $00)]	01
Write green data to RAM (location $00)	01
Write blue data to RAM (location $00)	01
Write red data to RAM (location $01)	01
Write green data to RAM (location $01)	01
Write blue data to RAM (location $01)	01
:	:
Write red data to RAM (location $FF)	01
Write green data to RAM (location $FF)	01
Write blue data to RAM (location $FF)	01
Overlay Color Palette Initialization	
Write $00 to address register	00
Write red data to overlay (location $00)	11
Write green data to overlay (location $00)	11
Write blue data to overlay (location $00)	11
Write red data to overlay (location $01)	11

Write green data to overlay (location $01)	11
Write blue data to overlay (location $01)	11
:	:
Write red data to overlay (location $03)	11
Write green data to overlay (location $03)	11
Write blue data to overlay (location $03)	11

4.5 Initializing the Bt457 (Monochrome)

Following a power-on sequence, the Bt457 must be initialized. If the clock/LD* sequence is controlled to reset the pipeline delay of the Bt457 to a fixed pipeline delay of eight clock cycles, this initialization sequence must be performed after the reset sequence. The command register must also be reinitialized when the multiplex selection changes (e.g., from 4:1 to 5:1 input multiplexing).

This sequence configures the Bt457 as follows:

4:1 Multiplexed Operation
No Overlays
No Blinking
Color data written/read every cycle

Control Register Initialization	**C1,C0**
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $00 to test register	10
Color Palette RAM Initialization	
Write $00 to address register	00
Write data to RAM (location $00)	01
Write data to RAM (location $01)	01
:	:
Write data to RAM (location $FF)	01
Overlay Color Palette Initialization	
Write $00 to address register	00
Write data to overlay (location $00)	11
Write data to overlay (location $01)	11
:	:
Write data to overlay (location $03)	11

4.6 Initializing the Bt457 (Color) 24-bit MPU Data Bus

In this example, three Bt457s are used in parallel to generate true color. A 24-bit MPU data bus is available to access all three Bt457s in parallel.

The operation and initialization are the same as the monochrome application of the Bt457.

4.7 Initializing the Bt457 (Color) 8-bit MPU Data Bus

In this example, three Bt457s are used in parallel to generate true color. An 8-bit MPU data bus is available to access the Bt457s.

While accessing the command, read mask, blink mask, and control/test and address registers, each Bt457 must be accessed individually. While accessing the color palette RAM or overlay registers, all three Bt457s are accessed simultaneously.

Following a power-on sequence, the Bt457s must be initialized. If the clock/LD* sequence is controlled to reset the pipeline delay of the Bt457s to a fixed pipeline delay of eight clock cycles, this initialization sequence must be performed after the reset sequence. The command register must also be reinitialized when the multiplex selection changes (e.g., from 4:1 to 5:1 input multiplexing).

This sequence configures the Bt457s as follows:

4:1 Multiplexed Operation

No Overlays

No Blinking

Each Bt457 initialized as a red, green, or blue device

Control Register Initialization	**C1,C0**
Red Bt457	
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $00 to test register	10

Green Bt457	
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $02 to test register	10
Blue Bt457	
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $04 to test register	10
Color Palette RAM Initialization	
Write $00 to all three address registers	00
Write red data to RAM (location $00)	01
Write green data to RAM (location $00)	01
Write blue data to RAM (location $00)	01
Write red data to RAM (location $01)	01
Write green data to RAM (location $01)	01
Write blue data to RAM (location $01)	01
:	:
Write red data to RAM (location $FF)	01
Write green data to RAM (location $FF)	01
Write blue data to RAM (location $FF)	01
Overlay Color Palette Initialization	
Write $00 to all three address registers	00
Write red data to overlay (location $00)	11
Write green data to overlay (location $00)	11
Write blue data to overlay (location $00)	11
Write red data to overlay (location $01)	11
Write green data to overlay (location $01)	11
Write blue data to overlay (location $01)	11
:	:
Write red data to overlay (location $03)	11
Write green data to overlay (location $03)	11
Write blue data to overlay (location $03)	11

5.0 Parametric Information

5.1 DC Electrical Parameters

Table 5-1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0	—	+70	°C
Output Load	RL	—	37.5	—	Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET	—	523	—	Ω

Table 5-2. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (Measured to GND)	—	—	—	7.0	V
Voltage on Any Signal Pin(1)	—	GND–0.5	—	VAA +0.5	V
Analog Output Short-Circuit Duration to Any Power Supply or Common	ISC	—	Indefinite	—	—
Ambient Operating Temperature	TA	—	—	—	—
Storage Temperature	TS	–55	—	+125	°C
Junction Temperature	TJ	–65	—	+150	°C
Ceramic Package	—	—	—	+175	°C
Plastic Package	—	—	—	+150	°C
Soldering Temperature (5 Seconds, 1/4” from Pin)	TSOL	—	—	260	°C
Vapor Phase Soldering (1 Minute)	TVSOL	—	—	220	°C

NOTE(S):

(1) This device uses high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5-3. DC Characteristics *(1 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs	—	—	—	—	—
Resolution (Each DAC)	—	8 (4)	8 (4)	8 (4)	Bits
Accuracy (Each DAC)	—	—	—	—	—
Integral Linearity Error	IL	—	—	±1 (1/8)	LSB
Differential Linearity Error	DL	—	—	±1 (1/16)	LSB
Gray-Scale Error	—	—	—	±5	%Gray Scale
Monotonicity	—	—	Guaranteed	—	—
Coding	—	—	—	—	Binary
Digital Inputs (Except CLOCK, CLOCK*)	—	—	—	—	—
Input High Voltage	VIH	2.0	—	VAA + 0.5	V
Input Low Voltage	VIL	GND – 0.5	—	0.8	V
Input High Current (Vin = 4.0 V)	IIH	—	—	1	µA
Input Low Current (Vin = 0.4 V)	IIL	—	—	–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN	—	4	10	pF
Clock Inputs (CLOCK, CLOCK*)	—	—	—	—	—
Differential Input Voltage	VIN	0.6	—	6	V
Input High Current (Vin = 4.0 V)	IKIH	—	—	1	µA
Input Low Current (Vin = 0.4 V)	IIKIL	—	—	–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN	—	4	10	pF
Digital Outputs D[7:0]	—	—	—	—	—
Output High Voltage (IOH = –800 µA)	VOH	2.4	—	—	V
Output Low Voltage (IOL = 6.4 mA)	VOL	—	—	0.4	V
3-State Current	IOZ	—	—	10	µA
Output Capacitance	CDOUT	—	10	—	pF
Analog Outputs	—	—	—	—	—
Output Current	—	—	—	—	—
White Level Relative to Blank	—	17.69	19.05	20.40	mA
White Level Relative Black	—	16.74	17.62	18.50	mA
Black Level Relative to Blank	—	0.95	1.44	1.90	mA
Blank Level on IOR, IOB	—	0	5	50	µA
Blank Level on IOG or IOUT	—	6.29	7.62	8.96	mA
Sync Level on IOG or IOUT	—	0	5	50	µA
LSB Size	—	—	—	—	—

Table 5-3. DC Characteristics *(2 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
Bt457, Bt458	—	—	69.1	—	µA
DA0-to-DAC Matching[1]	—	—	2	5	%
Output Compliance	VOC	–0.5	—	+1.2	V
Output Impedance	RAOUT	—	50	—	kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT	—	13	20	pF
Voltage Reference Input Current	IREF	—	10	—	µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR	—	0.5	—	% / %Δ VAA

NOTE(S):
(1) Does not apply to the Bt457.
2. Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. As the parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

5.2 AC Electrical Parameters

Table 5-4. AC Characteristics for 165 MHz and 135 MHz Devices *(1 of 2)*

		165 MHz Devices			135 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax	—	—	165	—	—	135	MHz
LD* Rate	LDmax	—	—	41.25	—	—	33.75	MHz
R/W, C0, C1 Setup Time	1	0	—	—	0	—	—	ns
R/W, C0, C1 Hold Time	2	15	—	—	15	—	—	ns
CE* Low Tiime	3	50	—	—	50	—	—	ns
CE* High Time	4	25	—	—	25	—	—	ns
CE* Asserted to Data Bus Driven	5	7	—	—	7	—	—	ns
CE* Asserted to Data Valid	6	—	—	75	—	—	75	ns
CE* Negated to Data Bus 3-Stated	7	—	—	15	—	—	15	ns
Write Data Setup Time	8	35	—	—	35	—	—	ns
Write Data Hold Time	9	3	—	—	3	—	—	ns
Pixel and Control Setup Time	10	3	—	—	3	—	—	ns
Pixel and Control Hold Time	11	2	—	—	2	—	—	ns
Clock Cycle Time	12	6.06	—	—	7.4	—	—	ns
Clock Pulse Width High Time	13	2.6	—	—	3	—	—	ns
Clock Pulse Width Low Time	14	2.6	—	—	3	—	—	ns
LD* Cycle Time	15	24.24	—	—	29.63	—	—	ns
LD* Pulse Width High Time	16	10	—	—	12	—	—	ns
LD* Pulse Width Low Time	17	10	—	—	12	—	—	ns
Analog Output Delay	18	—	12	—	—	12	—	ns
Analog Output Rise/Fall Time	19	—	2	—	—	2	—	ns
Analog Output Settling Time	20	—	—	8	—	—	8	ns
Clock and Data Feedthrough[(1)]	—	—	35	—	—	35	—	pV–sec
Glitch Impulse[(1)]	—	—	50	—	—	50	—	pV–sec
Analog Output Skew[(2)]	—	—	0	2	—	0	2	ns
Pipeline Delay	—	6	—	10	—	—	—	Clocks

Table 5-4. AC Characteristics for 165 MHz and 135 MHz Devices *(2 of 2)*

		165 MHz Devices			135 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
VAA Supply Current[3]	IAA	—	—	—	—	—	—	—
Bt458	—	—	310	370	—	235	340	mA
Bt457	—	—	n/a	n/a	—	207	257	mA

NOTE(S):

(1) Clock and data feedthrough is a function of the number of edge rates and the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 k Ω resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

(2) Does not apply to the Bt457.

(3) At Fmax. IAA (typ) at VAA = 5.0 V and TA = 20° C. IAA (max) at VAA = 5.25 V and TA = 0° C.

4. Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are VAA–0.8 to VAA–1.8 V with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF and D[7:0] output load ≤ 75 pF. See timing notes in Figure 5-1. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Table 5-5. AC Characteristics for 125 MHz and 110 MHz Devices *(1 of 2)*

		125 MHz Devices			110 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax	—	—	125	—	—	110	MHz
LD* Rate	LDmax	—	—	31.25	—	—	27.5	MHz
R/W, C0, C1 Setup Time	1	0	—	—	0	—	—	ns
R/W, C0, C1 Hold Time	2	15	—	—	15	—	—	ns
CE* Low Time	3	50	—	—	50	—	—	ns
CE* High Time	4	25	—	—	25	—	—	ns
CE* Asserted to Data Bus Driven	5	7	—	—	7	—	—	ns
CE* Asserted to Data Valid	6	—	—	75	—	—	75	ns
CE* Negated to Data Bus 3-Stated	7	—	—	15	—	—	15	ns
Write Data Setup Time	8	35	—	—	35	—	—	ns
Write Data Hold Time	9	3	—	—	3	—	—	ns
Pixel and Control Setup Time	10	3	—	—	3	—	—	ns
Pixel and Control Hold Time	11	2	—	—	2	—	—	ns
Clock Cycle Time	12	8	—	—	9.09	—	—	ns
Clock Pulse Width High Time	13	3.2	—	—	4	—	—	ns
Clock Pulse Width Low Time	14	3.2	—	—	4	—	—	ns
LD* Cycle Time	15	3.2	—	—	36.36	—	—	ns
LD* Pulse Width High Time	16	13	—	—	15	—	—	ns
LD* Pulse Width Low Time	17	13	—	—	15	—	—	ns
Analog Output Delay	18	—	12	—	—	12	—	ns
Analog Output Rise/Fall Time	19	—	2	—	—	2	—	ns
Analog Output Settling Time	20	—	—	8	—	—	8	ns
Clock and Data Feedthrough[(1)]	—	—	35	—	—	35	—	pV–sec
Glitch Impulse[(1)]	—	—	50	—	—	50	—	pV–sec
Analog Output Skew[(2)]	—	—	0	2	—	0	2	ns
Pipeline Delay	—	6	—	10	6	—	10	Clocks

Table 5-5. AC Characteristics for 125 MHz and 110 MHz Devices *(2 of 2)*

		125 MHz Devices			110 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
VAA Supply Current[3]	IAA	—	—	—	—	—	—	—
Bt458	—	—	225	330	—	210	315	mA
Bt457	—	—	200	250	—	190	240	mA

NOTE(S):

(1) Clock and data feedthrough is a function of the number of edge rates and the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 k Ω resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

(2) Does not apply to the Bt457.

(3) At Fmax. IAA (typ) at VAA = 5.0 V and TA = 20° C. IAA (max) at VAA = 5.25 V and TA = 0° C.

4. Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are VAA–0.8 to VAA–1.8 V with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF and D[7:0] output load ≤ 75 pF. See timing notes in Figure 5-1. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Table 5-6. AC Characteristics for 80 MHz Device *(1 of 2)*

		80 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax	—	—	80	MHz
LD* Rate	LDmax	—	—	20	MHz
R/W, C0, C1 Setup Time	1	0	—	—	ns
R/W, C0, C1 Hold Time	2	15	—	—	ns
CE* Low Time	3	50	—	—	ns
CE* High Time	4	25	—	—	ns
CE* Asserted to Data Bus Driven	5	7	—	—	ns
CE* Asserted to Data Valid	6	—	—	75	ns
CE* Negated to Data Bus 3-Stated	7	—	—	15	ns
Write Data Setup Time	8	35	—	—	ns
Write Data Hold Time	9	3	—	—	ns
Pixel and Control Setup Time	10	4	—	—	ns
Pixel and Control Hold Time	11	2	—	—	ns
Clock Cycle Time	12	12.5	—	—	ns
Clock Pulse Width High Time	13	5	—	—	ns
Clock Pulse Width Low Time	14	5	—	—	ns
LD* Cycle Time	15	50	—	—	ns
LD* Pulse Width High Time	16	20	—	—	ns
LD* Pulse Width Low Time	17	20	—	—	ns
Analog Output Delay	18	—	12	—	ns
Analog Output Rise/Fall Time	19	—	2	—	ns
Analog Output Settling Time	20	—	—	8	ns
Clock and Data Feedthrough[(1)]	—	—	35	—	pV–sec
Glitch Impulse[(1)]	—	—	50	—	pV–sec
Analog Output Skew[(2)]	—	—	0	2	ns
Pipeline Delay	—	6	—	10	Clocks

Table 5-6. AC Characteristics for 80 MHz Device *(2 of 2)*

		80 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
VAA Supply Current[3]	IAA	—	—	—	—
Bt458	—	—	200	285	mA
Bt457	—	—	170	220	mA

NOTE(S):

(1) Clock and data feedthrough is a function of the number of edge rates and the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 k Ω resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

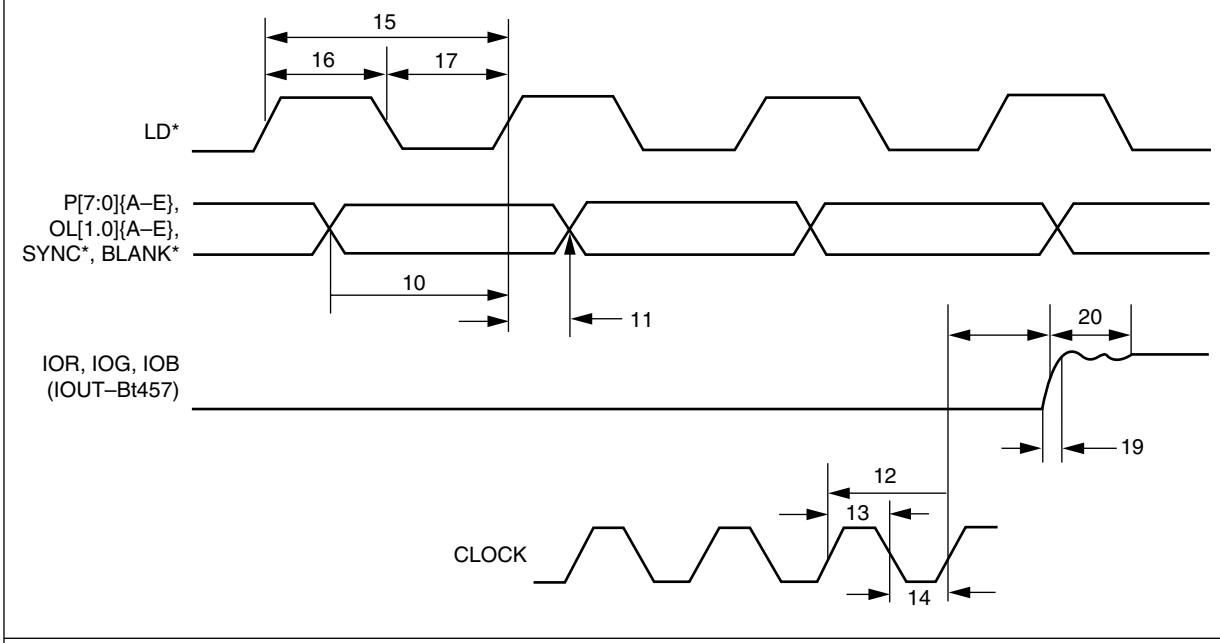
(2) Does not apply to the Bt457.

(3) At Fmax. IAA (typ) at VAA = 5.0 V and TA = 20° C. IAA (max) at VAA = 5.25 V and TA = 0° C.

4. Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are VAA–0.8 to VAA–1.8 V with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF and D[7:0] output load ≤ 75 pF. See timing notes in Figure 5-1. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

5.3 Timing Waveforms

Figure 5-1. Video Input/Output Timing

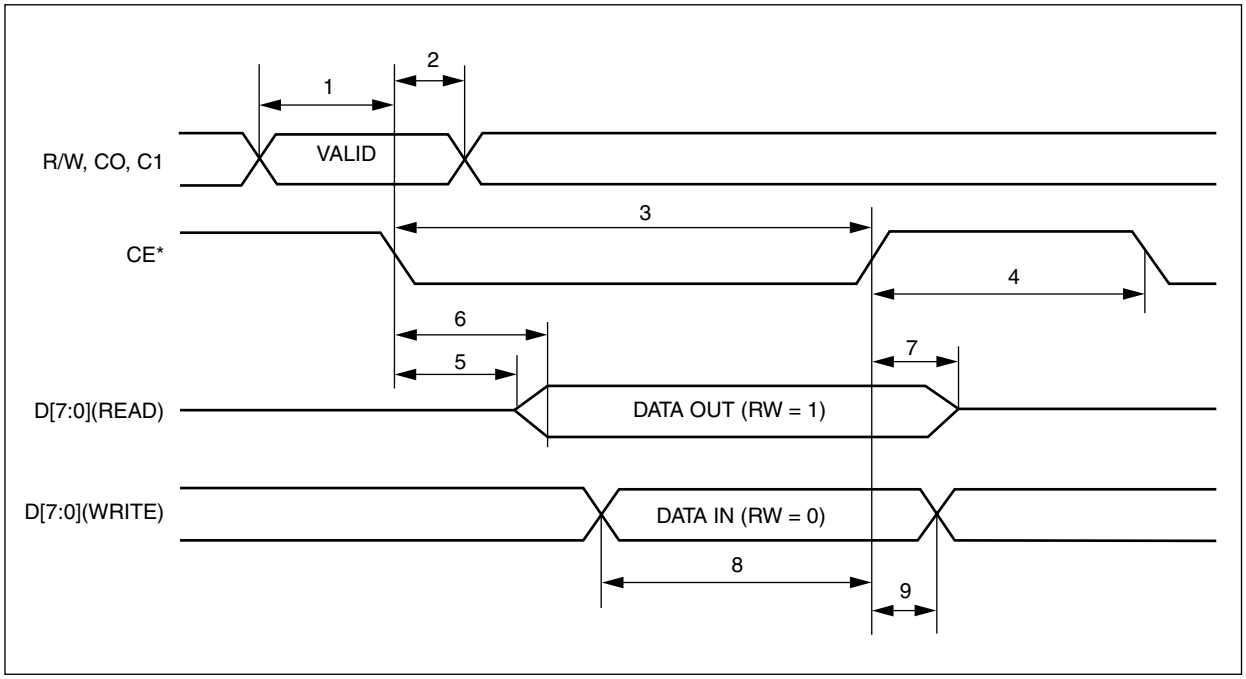


NOTE(S):

1. Output delay time is measured from the 50% point of the rising clock edge to the 50% point of full-scale transition.
2. Output settling time is measured from the 50% point of full-scale transition to the output settling within ±1 LSB for the Bt457/458.
3. Output rise/fall time is measured between the 10% and 90% points of full-scale transition.

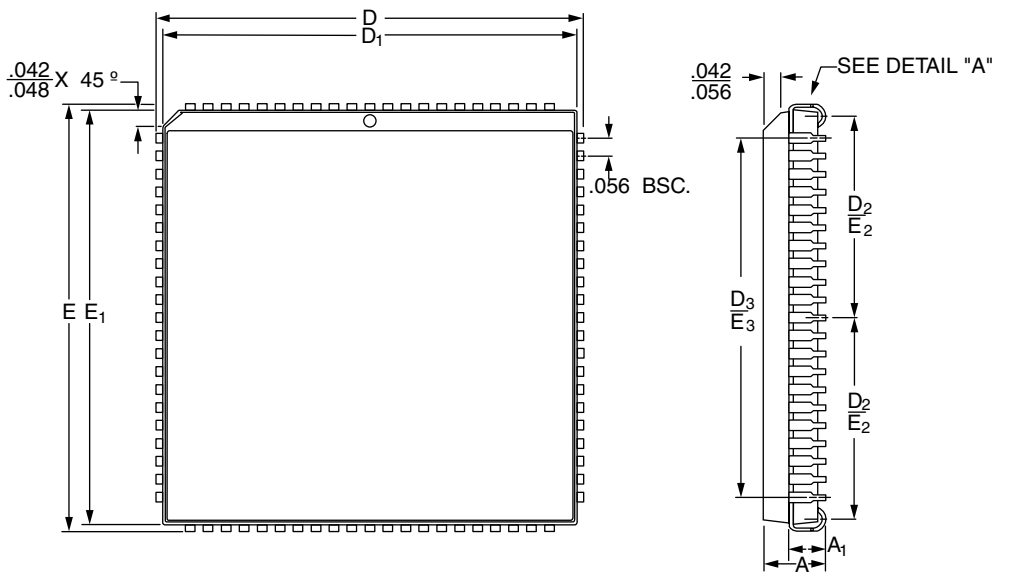
457-8_010

Figure 5-2. MPU Read/Write Timing

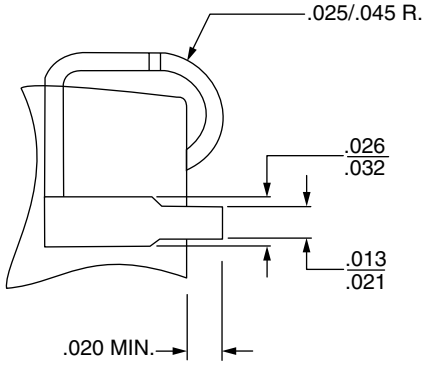


5.4 Package Drawing

Figure 5-3. 84-Pin Plastic J-Lead (PLCC)



SYMBOL	INCHES			MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	.165		.200	4.20		5.08
A_1	.090		.130	2.29		3.30
D	1.185		1.195	30.10		30.35
D_1	1.150		1.158	29.21		29.41
D_2	.545		.565	13.84		14.35
D_3	1.000 REF.			25.40 REF.		
E	1.185		1.195	30.10		30.35
E_1	1.150		1.158	29.21		29.41
E_2	.545		.565	13.84		14.35
E_3	1.000 REF.			25.40 REF.		



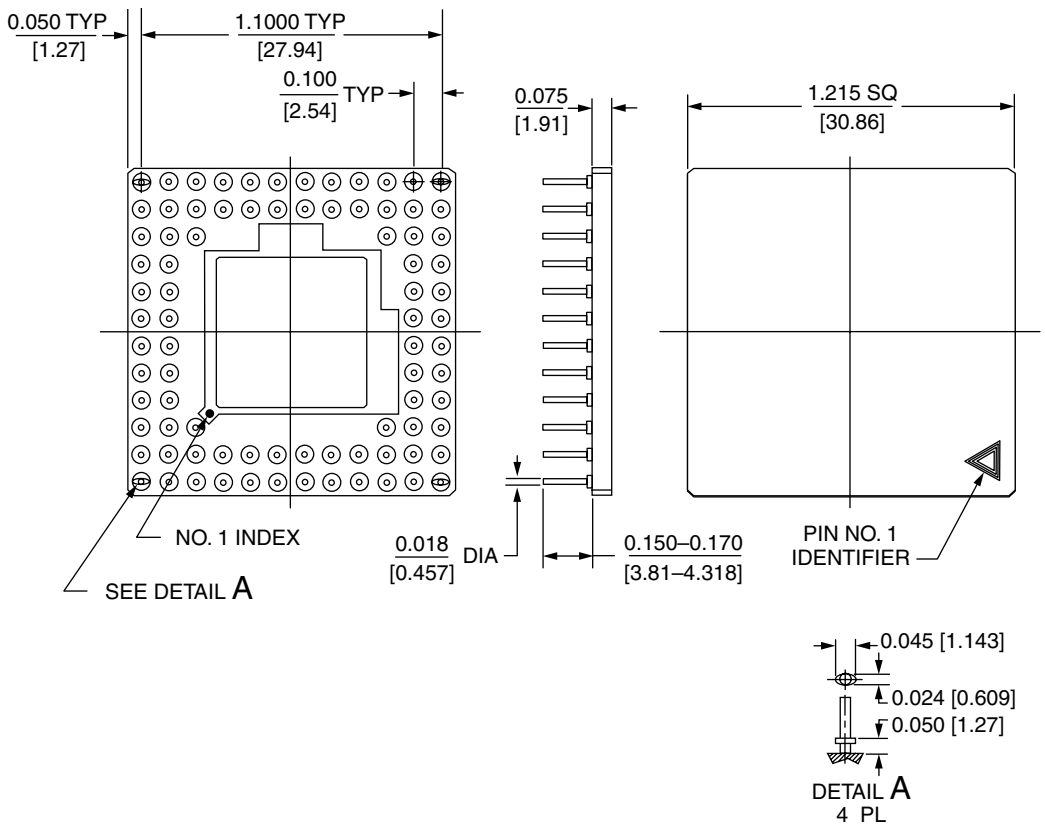
DETAIL "A"

NOTE(S):

1. Dimensions are in inches [millimeters].
2. Tolerances are: .xxx ±0.005 [0.127].
3. PLCC Packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

457-8_012

Figure 5-4. 84-Pin Ceramic PGA



NOTE(S):

1. Dimensions are in inches [millimeters].
2. Tolerances are: .xxx ±0.005 [0.127].
3. Pins are intended for insertion in hole rows on 0.100" [2.54] centers.

457-8_013

5.5 Revision History

Table 5-7. Revision History

Datasheet Revision	Change From Previous Revision
I	Expanded PC Board Layout Considerations section. Changed AC parameter "CE* asserted to data bus driven" from 10 ns to 7 ns minimum.
J	Changed AC parameter "VAA Supply Current (Max)" for the Bt457: 80 MHz changed from 190 mA to 220 mA, 110 MHz changed from 210 mA to 240 mA, and 125 MHz changed from 220 mA to 250 mA.
K	Changed speed grade from 170 MHz to 165 MHz. Changed PLL feedback circuitry. Consolidated Bt458 power specifications. Changed AC Characteristics CLOCK, Load Cycle, and Pulse Width times. Changed typical analog output delay times.
L	Added 135 MHz speed grade.
M	Revised PCB Layout section.
N	Bt451 obsolete.

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