Alpine™ VGA Family – CL-GD543X/'4X

Technical Reference Manual

February 1995

CL-GD543X/'4X Extended Video Modes Summary

Mode No.	VESA® No.	Colors	Display Resolution	Chars.	CL-GD5430 CL-GD5440 Refresh (Hz)	CL-GD5434 Refresh (Hz)	CL-GD5436 Refresh (Hz)
14, 55	109	16/256K	1056 × 400	132 × 25	70	70	70
54	10A	16/256K	1056 × 350	132 × 43	70	70	70
58, 6A	102	16/256K	800 × 600	100 × 37	56, 60, 72, 75	56, 60, 72, 75	56, 60, 72, 75
5C	103	256/256K	800 × 600	100 × 37	56, 60, 72, 75	56, 60, 72, 75	56, 60, 72, 75
5D	104	16/256K	1024 × 768	128 × 48	43i, 60, 70, 72, 75	43i, 60, 70, 72, 75	43i, 60, 70, 72, 75
5E	100	256/256K	640 × 400	80 × 25	70	70	70
5F	101	256/256K	640 × 480	80 × 30	60, 72, 75	60, 72, 75	60, 72, 75
60	105	256/256K	1024 × 768	128 × 48	43i, 60, 70, 72, 75	43i, 60, 70, 72, 75	43i, 60, 70, 72, 75
64	111	64K	640 × 480	–	60, 72, 75	60, 72, 75	60, 72, 75
65	114	64K	800 × 600	–	56, 60, 72, 75	56, 60, 72, 75	56, 60, 72, 75
66	110	32K	640 × 480	–	60, 72, 75	60, 72, 75	60, 72, 75
67	113	32K	800 × 600	–	56, 60, 72, 75	56, 60, 72, 75	56, 60, 72, 75
68	116	32K	1024 × 768	–	43i	43i, 60, 70, 75	43i, 60, 70, 75
69	119	32K	1280 × 1024	–	–	43i	43i, 60
6C	106	16/256K	1280 × 1024	160 × 64	43i	43i	43i
6D	107	256/256K	1280 × 1024	160 × 64	43i	43i, 60, 71, 75	43i, 60, 71, 75
71	112	16M	640 × 480	–	60	60	60, 72, 75
72	–	16M + A	800 × 600	–	–	56, 60	56, 60
73	–	16M + A	1024 × 768	–	–	43i	–
74	117	64K	1024 × 768	–	43i	43i, 60, 70, 75	43i, 60, 70, 75
75	11A	64K	1280 × 1024	–	–	43i	43i
76	–	16M + A	640 × 480	–	–	60, 72, 75	60, 72, 75
78	115	16M	800 × 600	–	–	–	56, 60, 70, 75
79	118	16M	1024 × 768	–	–	–	43i, 60, 72, 75

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Fourth Edition

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Contents

Revision History

The following are major changes between the third edition, dated March 1994, and the fourth edition, dated February 1995, of this technical reference manual:

- The CL-GD5440 and the CL-GD5436 were added to the Alpine chip family. Pertinent register, timing, and functionality information was added to both the technical reference manual and the data book.
- Appendices B10 and B16 were added.
- The package diagram names in the data book were updated to remove HQFP package information.

Table of Contents

Appendices

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Introduction

1. INTRODUCTION

1.1 Scope of Document

This manual provides technical discussion of the Alpine CL-GD543X/'4X family of VGA controllers. This manual includes descriptions of each major component integrated into the chip, a data book, detailed information on each register, a BIOS description, and appendices intended to assist hardware and software designers.

1.2 Chip Types Covered

This manual documents the CL-GD5430, CL-GD5434, CL-GD5436, and CL-GD5440. The following table shows the production versions covered.

Table 1-1. Production Versions Covered

Revision	A	B	C	D	E	F
CL-GD5430	✔	✔	✔	✔	✔	
CL-GD5434	✔	✔	✔	✔	✔	✔
CL-GD5436	✔					
CL-GD5440	✔					

The CL-GD543X/'4X ID register — CR27, will read back a value specifying the Alpine family member. Refer to Chapter 9, "Extension Registers", for further information.

1.3 Intended Audience

This manual is intended for a technically sophisticated audience. It is assumed that the reader is familiar with assembly language programming on the 8088/8086, 80286/80386/80486, Pentium™, or similar microprocessor, and understands the fundamentals of video display technology.

Hardware engineers should find Chapter 3, "Data Book", useful. It contains the pinouts and detailed pin descriptions and detailed DC and AC characteristics. In addition, the application notes in Appendix B should be helpful for board designs.

Software engineers should find Chapters 4–9 (register descriptions) useful for BIOS- and driver-level codes. All registers are described to the bit level. Also, the application notes in Appendices B–D should be helpful, especially those discussing the palette DAC and clock options, and programming methods.

Management personnel should find Chapter 2, "Overview", useful.

1.4 Conventions

This section discusses conventions used throughout this document. Conventions include acronyms, abbreviations, and nomenclature usage. For a quick reference of acronyms see Table 1-2.

Table 1-2. Acronym Quick Reference

Acronym	Definition
BIOS	basic input output system
BitBLT	bit boundary block transfer
bpp	bits per pixel
CAS	column address strobe
CGA	color graphics adapter
CMOS	complementary metal-oxide semiconductor
DRAM	dynamic random access memory
EEPROM	electrically erasable/programmable read-only memory
EGA	enhanced graphics adapter
EPROM	electrically programmable read-only memory
FIFO	first-in/first-out
HSYNC/ VSYNC	horizontal/vertical synchronization
I/O	input/output
LSB	least-significant bit
MSB	most-significant bit
PCI	peripheral component interconnect
RAM	random access memory
RAS	row address strobe
RGB	red, green, blue
RFI	radio frequency interference
R/W	read/write
TTL	transistor-transistor logic
VESA®	Video Electronics Standards Association
VGA	video graphics array

Bits

Bits are always listed in descending order, most-significant (highest number) to least-significant (lowest number). When discussing a bit field within a register or memory, the bit number of the most-significant bit is given on the left, followed by a colon (:) and then the bit number of the least-significant bit (for example, bits 7:0). A field consists of a set of adjoining bits with common functionality. Registers are made up of fields of one or more bits.

Acronyms

Throughout this manual, the first usage of all acronyms has the definition following in parentheses. Table 1-2 lists the most used acronyms found in this manual. For further definitions, refer to Appendix F1, "Glossary and Bibliography".

Abbreviations

The unit 'K byte' designates 1024 bytes. The unit 'Mbyte' designates 1,048,576 bytes (1024 squared). The unit 'Gbyte' designates 1,024 megabytes. The unit 'Hz' designates hertz. The unit 'kHz' designates 1,000 hertz. The unit 'MHz' designates 1,000 kilohertz. The unit 'ns' designates nanosecond. The unit 'µs' designates microsecond (1,000 nanoseconds). The unit 'ms' designates millisecond (1,000 microseconds). The unit 'mA' designates milliampere. The use of 'tbd' in tables indicates values that are 'to be determined'. The unit 'µF' designates the capacitance measurement micro-farad (10^{-6} farad). N/A designates 'not available'. The use of 'n/c' indicates the pin is a 'no connect'.

Numeric Naming

Hexadecimal numbers are represented with all letters in upper case and a lower-case 'h' is appended to them (e.g., '14h', '3A7h', and 'C000h' are hexadecimal numbers). Numbers not indicated by an 'h' are decimal. Octal numbers are not used in this manual.

Reserved

When a system memory or I/O address is referred to as 'reserved', it means that writing to that address is not permitted. Reserved bits *must* be written as '0' to maintain upward compatibility.

Read-Only

The word 'read-only' is used to indicate registers and bits that can be read, but not written to.

Logic States

In this manual, logic states are indicated in all capitals (for example, reset HIGH).

2

Overview

2. OVERVIEW

The Alpine family of VGA controllers supports high-resolution graphics and text display modes for a variety of color CRT monitors using industry-standard graphics, video, software, and host interfaces.

The CL-GD543X/'4X VGA controllers are hardware- and software-compatible with the IBM® VGA, and provide improved performance and additional functionality. The CL-GD543X/'4X family members provide extensions to the VGA standard such as high resolution, an integrated BitBLT engine, and integrated video playback support. The CL-GD543X/'4X devices are compatible with the industry-standard CL-GD542X VGA family.

Highly integrated, these devices include a programmable dual-frequency synthesizer and palette DAC, allowing a motherboard Super VGA solution with as few as two ICs.

2.1 Features

The following is a list of the major features of the CL-GD543X/'4X family of VGA controllers:

Table 2-1. CL-GD543X Features List

Features	'GD5430	'GD5434	'GD5436	'GD5440
100% hardware- and BIOS-compatible with IBM® VGA display standards	✔	✔	✔	✔
Minimum chip count for motherboard VGA solution	2	3	3	2
GUI acceleration width (in bits)	32	64	64	32
32-bit Direct-connect CPU interface	✔	✔	✔	✔
64-bit DRAM display memory interface	✔	✔	✔	✔
Memory size (Mbytes)	1/2, 1, 2	1, 2, 4	1, 2, 4	1/2, 1, 2
Resolutions up to 1280 × 1024 (see inside front cover)	✔	✔	✔	✔
Integrated 24-bit DAC	✔	✔	✔	✔
Programmable dual-clock synthesizer	✔	✔	✔	✔
4-, 8-, 16-bit-wide DRAMs	✔	✔	✔	✔
EDO DRAM support			✔	
Maximum dot clock	86 MHz	135 MHz	135 MHz	86 MHz
Maximum memory clock	60 MHz	50 MHz	80 MHz	60 MHz
'Green PC' power-saving features	✔	✔	✔	✔
Direct 80486 interface	✔	✔	✔	✔
Direct VESA® VL-Bus™ interface (2.0)	✔	✔	✔	✔
Direct PCI™ bus interface (2.0)	✔	✔	✔	✔
Direct ISA bus interface (up to 12.5 MHz)	–	✔	–	–
VESA® pass-through feature connector	✔	✔	✔	✔
Multimedia ready	✔	✔	✔	✔
Video overlay and color key support	✔	✔	✔	✔
YCrCb and AccuPak™ Support	–	–	–	✔

Table 2-1. CL-GD543X Features List *(cont.)*

Features	'GD5430	'GD5434	'GD5436	'GD5440
Integrated video playback support	–	–	–	✔
Color space conversion	–	–	–	✔
Interpolated zooming	–	–	–	✔
16-bit Pixel bus	–	–	✔	–
CL-GD542X register- and software-compatible	✔	✔	✔	✔
Low-power CMOS, 208-pin PQFP package	✔	✔	✔	✔

2.2 Chip Architecture

The CL-GD543X/'4X includes all the hardware required to implement CPU updates to display memory, screen refresh, and DRAM refresh. The CL-GD543X/'4X directly interfaces with the PCI™ bus, VESA® VL-Bus™, or ISA (CL-GD5434 only) bus, the display memory, the feature connector, and the monitor.

The major activities supported by the CL-GD543X/'4X are:

- **Host access to CL-GD543X/'4X registers**
- **Host access to display memory**
- **BitBLT engine access to display memory**
- **Display access to display memory (screen refresh)**
- **Display memory refresh**

2.2.1 Host Access to CL-GD543X/'4X Registers

The host (typically a PCI local bus, VESA VL-Bus, or ISA bus) can access CL-GD543X/'4X registers by setting up 16- or 24-bit addresses and generating I/O control signals to read or write 8- or 16-bit data. Other activities, such as DRAM refresh, screen refresh, and delayed CPU writes to display memory can occur concurrently with accesses to registers. The bitBLT registers can be written for up to 32 bits per access, using Memory-mapped I/O (see Appendix B20).

The registers are listed in Chapter 3, "Data Book", and described in Chapters 4–9. These registers include all the standard VGA registers. Nearly all registers can be read by the host to allow BIOS and driver software to determine the state of the graphics adapter.

2.2.2 Host Access to Display Memory

The CL-GD543X/'4X handles the host access to display memory. The host executes memory accesses in the VGA address range or in a linear address range to transfer data to or from display memory. All of the required handshake interface signals are internally generated by the CL-GD543X/'4X with no requirement for external logic decoding.

The CL-GD543X/'4X takes 24- or 32-bit addresses from the host and transforms them according to the selected addressing mode and address space mappings, finally issuing multiplexed addresses to the planes via the MA[9:0] Address bus. RAS*, CAS*, OE*, and WE* provide timing and control to the display memories.

A Write Buffer is logically located at the CPU interface to isolate the CPU from the display memory. Writes to display memory occur immediately until the Write Buffer is full. The address and data are written into the Write Buffer, and the actual write into display memory occurs later. If the Write Buffer is full, wait states will be inserted until space is available.

2.2.3 AccuPak™ Encoding/Decoding

The CL-GD5440 has an encoder preceding the Write Buffer that compresses four 16-bit YCrCb or RGB 5-5-5 pixels into a single 32-bit word that is written into display memory. The compression method is a Cirrus Logic proprietary scheme called AccuPak. For display, the AccuPak packets are decoded into four YCrCb pixels that are eventually converted to RGB prior to being applied to the DACs.

2.2.4 BitBLT Engine Access to Display Memory

The CL-GD543X/'4X contains a bitBLT engine to effect block transfers within display memory or from system memory to display memory. Color Expansion allows optimum use of available host bandwidth by expanding single bits across the bus into complete 8-, 16-, 24-, or 32-bit pixels. Table 2-2 indicates which color expansion widths are available by chip type. Pattern-fill operations are available using either monochrome or full-color source operands. All 16 two-operand raster OPs are implemented in hardware.

Table 2-2. Color Expansion Widths

Width (bpp)	CL-GD5430	CL-GD5434	CL-GD5436	CL-GD5440
8	✔	✔	✔	✔
16	✔	✔	✔	✔
24			✔	
32			✔	✔

2.2.5 Display Access to Display Memory

The CL-GD543X/'4X also contains an intelligent Address Sequencer that allocates display memory cycles not only to the host and the bitBLT engine, but also to the display CRT Controller for screen refresh.

A FIFO, logically between the Memory Sequencer and the Attribute Controller, decouples the memory speed from the display speed, allowing the execution of Fast-page mode accesses for screen refresh. This minimizes the memory bandwidth required. The display is blanked during horizontal and vertical retrace intervals, freeing additional memory bandwidth for host access.

The CL-GD5436 provides optimized timing support for EDO (Extended Data Out) DRAMs.

2.2.6 Display Memory Refresh

The CL-GD543X/'4X handles the refresh of the dynamic RAMs used for the display memory. During each horizontal blanking period, a selectable number of CAS*-before-RAS* refresh cycles are executed.

2.3 Major Components

The CL-GD543X/'4X incorporates all of the following major subsections of the IBM VGA/EGA into a single integrated circuit:

- **Sequencer**
- **CRT Controller**
- **Graphics Controller**
- **Attribute Controller**
- **Programmable Dual-frequency Synthesizer**
- **Palette DAC**

In addition to the sections of the original VGA/EGA architecture, the CL-GD543X/'4X also contains a flexible local bus interface, a bitBLT engine, and video playback support logic.

- **PCI™, VESA® VL-Bus™ Local Bus Interface**
- **BitBLT Engine**
- **Video Overlay Logic**
- **Video Pipeline (CL-GD5440)**
- **Video Window Generator (CL-GD5440)**

In describing the CL-GD543X/'4X family of VGA controllers, it is useful to retain the identity of the original major subsections found in the IBM EGA and VGA controllers. The architectures of these major subsections, as well as CL-GD543X/'4X enhancements, are described in the following sections.

2.3.1 Sequencer

The Sequencer controls access to the display memory. It ensures that the necessary screen refresh and dynamic memory refresh cycles are executed, and that the remaining memory cycles are made available for CPU and BLT read/write operations.

The Sequencer consists of a Memory Arbitrator and a Memory Controller. It accepts requests from memory address counters associated with the CRTC, and address-transformation logic associated with the Graphics Controller. It uses the video FIFOs to deliver data to the Attribute Controller and to the AccuPak decoder, and the Write Buffer to transfer data to the Graphics Controller. The Memory Sequencer registers are described in Chapter 5, "VGA Sequencer Registers".

The Memory Controller is driven by a memory clock (MCLK) optimized for the speed of the DRAM used, independent of the video clock (VCLK). The Memory Controller generates the signals and addresses necessary for accessing display memory. The Memory Arbitrator and host bus interface are also driven by MCLK.

2.3.2 CRT Controller

The CRT Controller generates the horizontal and vertical synchronization signals for the CRT display. It includes various registers that allow flexible configuration options. These options include user-configurable horizontal and vertical timing and polarity, cursor position, horizontal scanlines, and both horizontal and vertical GENLOCK. The CRT Controller registers are described in Chapter 6.

The CRT Controller is software compatible with IBM VGA hardware. The CRT Controller also provides split-screen capability and smooth scrolling. A simplified block diagram of the CRT Controller is shown in Figure 2-1.

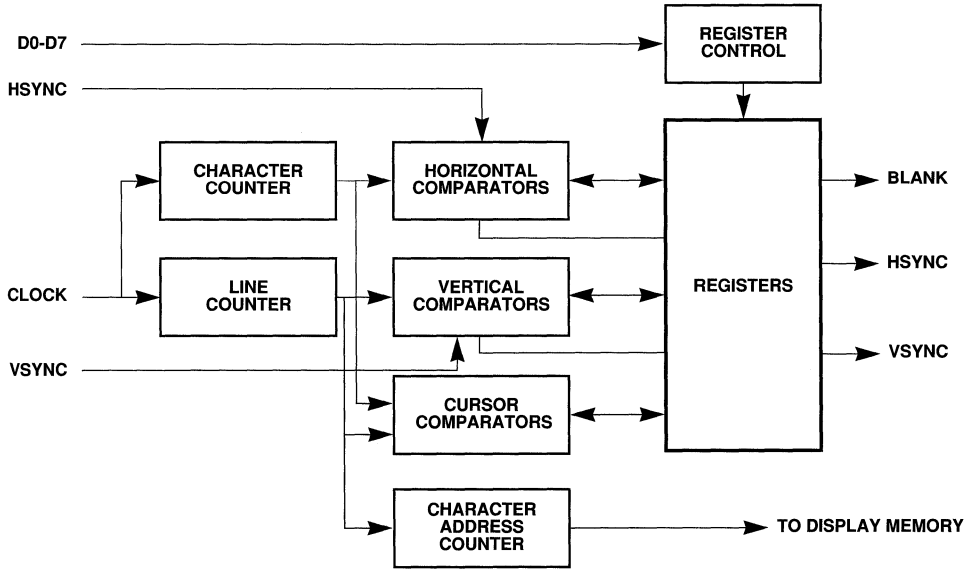

Figure 2-1. CRT Controller Functional Block Diagram

2.3.3 Graphics Controller

The Graphics Controller operates in either text or graphics modes and has the following major functions:

- **provides the host CPU with a read/write access path to display memory**
- **controls all four memory planes in planar modes**
- **allows data to be manipulated prior to being written to display memory**
- **formats data for use in various backward compatibility modes**
- **provides color comparators for use in color painting modes**
- **reads/writes 32- or 64-bit words through the 32- or 64-bit display memory interface**
- **combines display memory data and attributes for output to the Pixel bus**

The Graphics Controller directs data from the display memory to the Attribute Controller and to the CPU. Figures 2-2 and 2-3 illustrate typical write and read operations.

For a write operation, the data from the CPU bus are combined with the data from the Set/Reset Logic, depending on the Write mode and video mode. In addition, the data may be combined with the contents of the read latches, and some bits or planes may be masked (prevented from being changed). See the descriptions in Chapter 7, *VGA Graphics Controller Registers*, for more information.

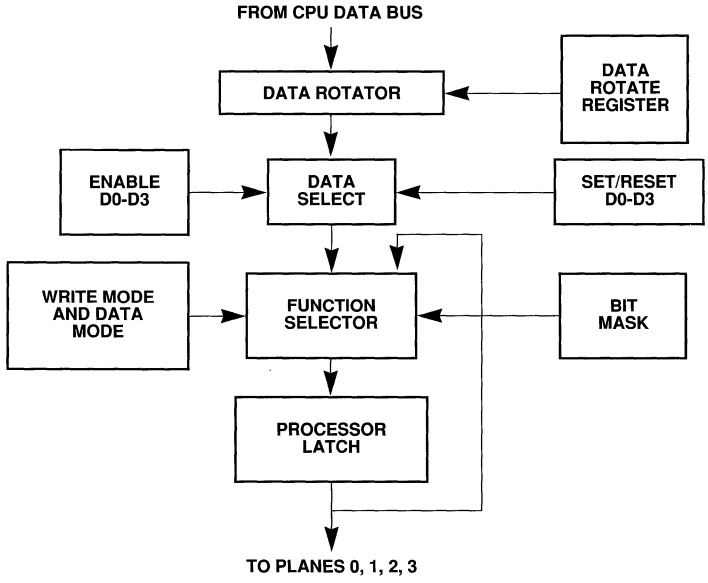

Figure 2-2. Graphics Controller Write Operation

The Graphics Controller is also involved when the CPU is reading data from display memory. Depending on the Read mode, the data returned may be the actual contents of the display memory, or it may reflect the outcome of comparisons with the color value in one of the Graphics Controller registers. See the descriptions in Chapter 7, "VGA Graphics Controller Registers", for more information.

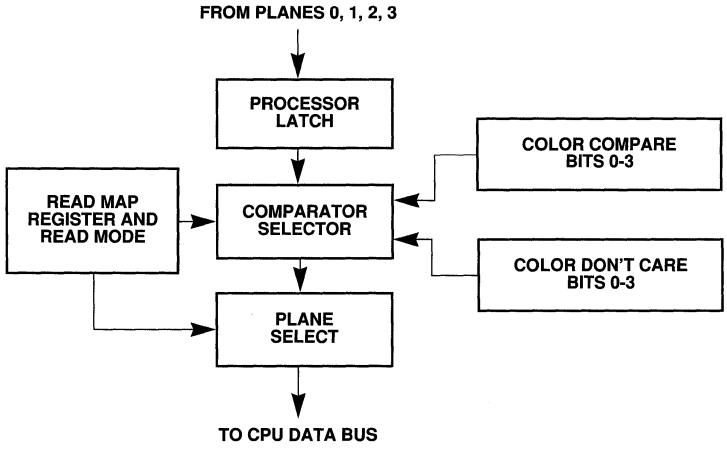

Figure 2-3. Graphics Controller Read Operation

2.3.4 Attribute Controller

The Attribute Controller controls blinking and underline operations in alphanumeric modes. It also provides the horizontal pixel-panning capability in both alphanumeric and graphics modes. The Attribute Controller registers are described in Chapter 8. Figure 2-4 depicts the functional block diagram of the Attribute Controller.

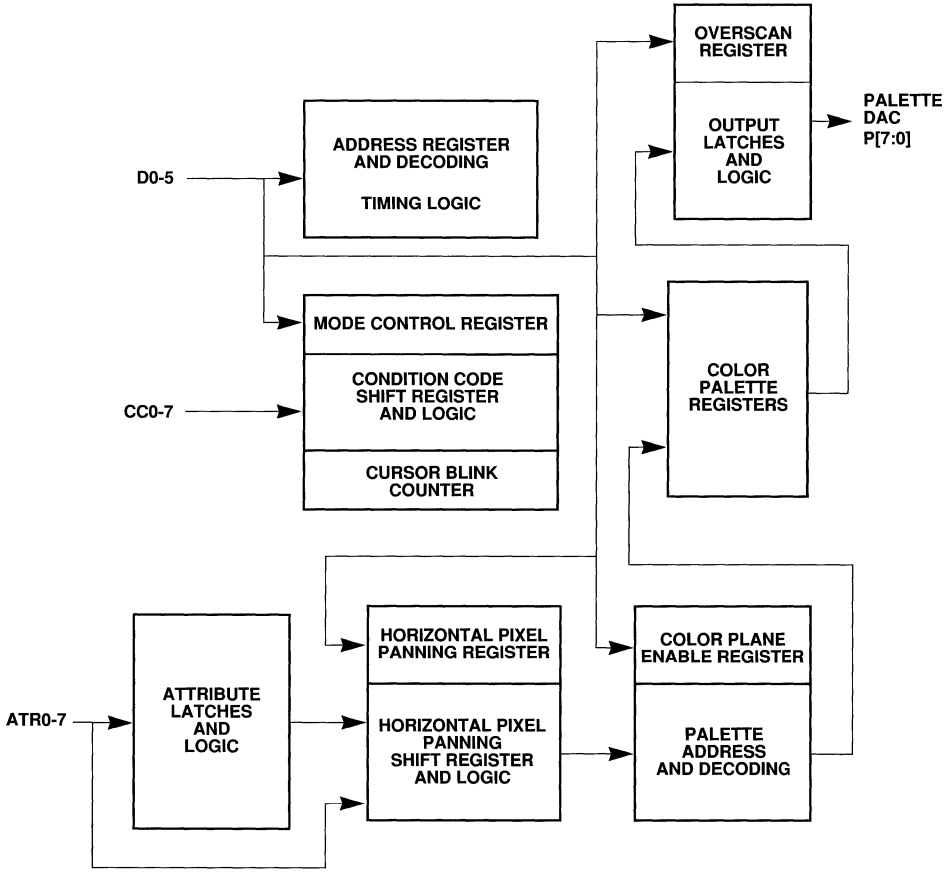

Figure 2-4. Attribute Controller Functional Block Diagram

2.3.5 Programmable Dual-Frequency Synthesizer

The CL-GD543X/'4X includes an integrated dual-frequency synthesizer that can be programmed to generate the VCLK for all supported screen formats, and the MCLK used by the Sequencer. The dual-frequency synthesizer requires a single reference frequency of 14.31818 MHz from an external source. Figure 2-5 depicts the programmable dual-frequency synthesizer.

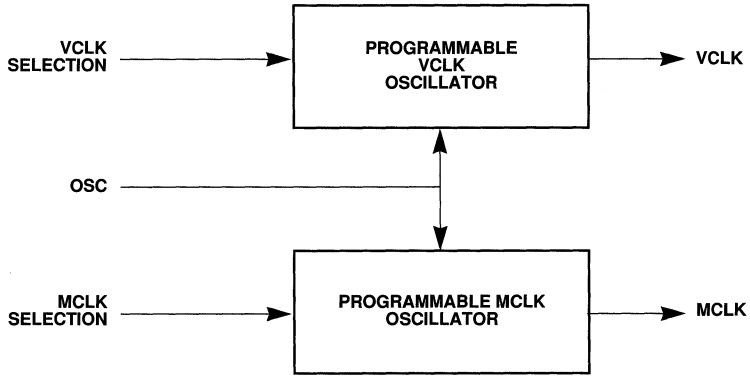

Figure 2-5. Programmable Dual-Frequency Synthesizer Functional Diagram

2.3.6 Palette DAC

The CL-GD543X/'4X includes an integrated palette DAC that can interface directly to the monitor connector via appropriate RFI filters. The palette DAC can be programmed for 256 simultaneous colors from a palette of 256K, or it can be programmed for Direct-color mode. In Direct-color mode, two, three, or four contiguous bytes from the display memory are combined for each pixel. This allows 32K, 64K, or 16.8 million simultaneous colors on the screen. Figure 2-6 is a functional block diagram of the palette DAC.

The Pixel bus, DCLK, and BLANK* can be driven into the CL-GD543X/'4X. This allows it to operate in the VESA-standard VGA Pass-through Connector mode. Eight-, 15-, or 16-bit data can also be inserted from an external source through the P[7:0] pins. In addition to the VESA standard, the EVIDEO* input is capable of switching at the pixel rate for dynamic overlay.

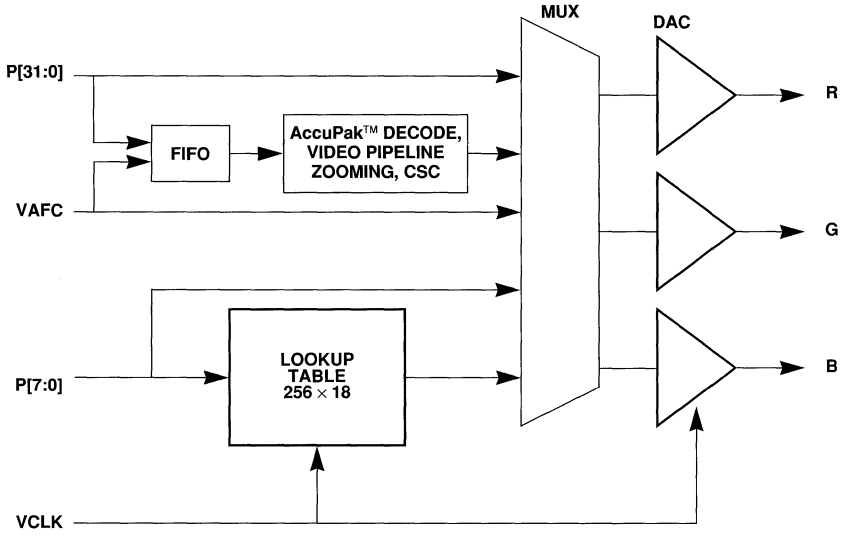

Figure 2-6. 256-Color/Direct-Color Palette DAC

2.3.7 Local Bus Interface

The CL-GD543X/'4X includes a glueless interface for the 80486, VESA VL-Bus, and PCI bus with host transfers taking place at up to 32 bits.

2.3.8 BitBLT Engine

The CL-GD543X/'4X includes a bitBLT engine for block transfers within display memory at full memory bandwidth. System-to-display transfers can also be effected with the bitBLT engine. All 16 two-operand Raster OPs are implemented in hardware. Color Expansion leverages the host bandwidth by up to 32 times.

2.3.9 Video Overlay Logic

The CL-GD543X/'4X supports extensive dynamic-video overlay and DAC mode switching. Pixels chosen by color key, or an internal or external timing generator, can be overlayed with video data from the P[7:0] bus on a dynamic basis. This capability allows for full-motion video without consuming valuable CPU host bandwidth. The CL-GD5430 and CL-GD5440 support VAFC (VESA Advanced Feature Connector) Baseline input and output. The CL-GD5436 supports a 16-bit Pixel bus for overlay when configured for PCI bus.

2.3.10 Video Pipeline (CL-GD5440)

The CL-GD5440 Video Pipeline performs format conversion, interpolated zooming, and color space conversion for a rectangular region of the display called the Video Window.

The AccuPak decoder accepts two 32-bit words, one from each scan line, or from the VAFC connector. Each word is expanded and error diffused into four 16-bit YCrCb pixels. For video in standard 5-5-5 RGB, 5-6-5 RGB, or YCrCb formats, the AccuPak decoder is bypassed.

The chrominance interpolator accepts 16-bit YCrCb or RGB pixels from the AccuPak decoder. For YCrCb pixels, a chrominance interpolation is performed to generate a 24-bit YCrCb pixel. RGB pixels are repacked to produce a 24-bit RGB pixel.

The Y interpolator accepts two vertically adjacent 24-bit pixels and calculates a resampled output pixel using a four subpixel granularity. The X interpolator accepts horizontally adjacent pixels and calculates the resampled output pixel using a four subpixel granularity. For line replication mode, the Y interpolator is bypassed.

The YCrCb to RGB color matrix performs color conversion on the 24 bit interpolated data. The color converter supports standard CCIR (International Radio Consultive Committee) 601 format.

2.3.11 Video Window Generator (CL-GD5440)

The CL-GD5440 has a hardware window that allows the video overlay of graphics data or graphics overlay of video data. Registers CR31–CR3F control the overlay function and are described in Chapter 9, "Extension Registers". Appendix B10 discusses the CL-GD5440 functional extensions.

2.4 Hardware/Software Compatibility

The CL-GD543X/'4X includes all registers and data paths required for VGA controllers. Enhancements include up to 1024 × 768, 32-bpp video modes, an internal color palette, eight simultaneously loadable text fonts, Extended Write modes, and readable registers.

Extended-resolution Display modes are made possible by high video clock rates and high display-memory bandwidth.

Extended text and graphics resolutions, beyond the 640 × 350 IBM EGA and 640 × 480 VGA standards, are also supported by the Cirrus Logic BIOS on both fixed-frequency PS/2™-compatible monitors, as well as multiple-frequency monitors.

The CL-GD543X/'4X family is software-compatible with the CL-GD542X family.

2.5 Video Subsystem Architecture

Figure 2-7 shows the main components needed to implement a functional VGA subsystem using the CL-GD543X/'4X. The interfaces that must be implemented are the host CPU, the BIOS (for adapter board implementation only), the display memory, and the CRT. If live-video overlay is required, the overlay interface must be implemented.

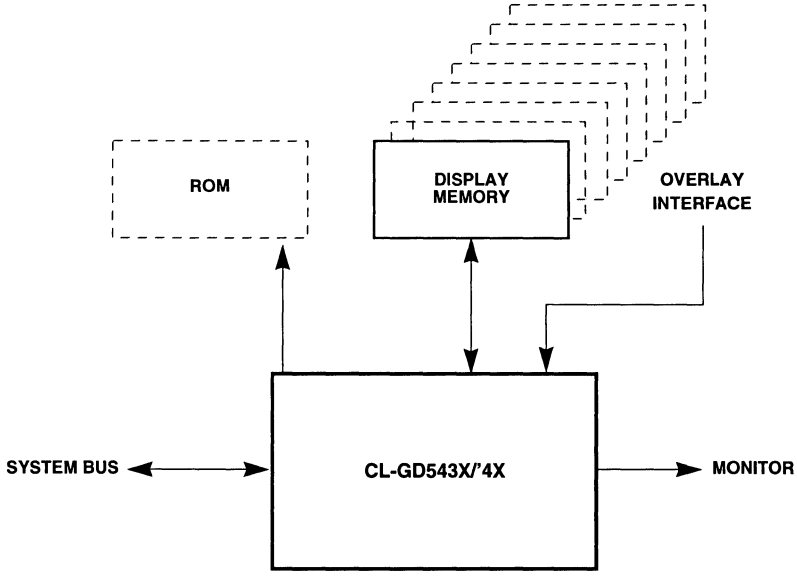

Figure 2-7. Video Subsystem Architecture

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3

Data Book

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CIRRUS LOGIC®

CL-GD543X/'4X

Preliminary Data Book

FEATURES

CL-GD543X/'4X Family

- **Pin- and software-compatible VGA graphics accelerators**
- **Integrated dual-clock synthesizer and 24-bit DAC**
  - — Pixel clock programmable to 135 MHz (CL-GD5434/'36), and to 86 MHz (CL-GD5430/'40)
  - — Memory clock programmable to 60 MHz (CL-GD5430/'34/'40), and to 80 MHz (CL-GD5436)
- **32-bit direct-connect CPU interface**
  - — PCI bus (v2.0 compliant) with burst-cycle support
  - — VESA® VL-Bus™ (v2.0 with 50 MHz)
  - — ISA bus (12.5 MHz) (CL-GD5434 only)
  - — Zero-wait-state write buffer for CPUs to 33 MHz
- **64-bit DRAM display memory interface**
  - — 1-, 2-, and 4-Mbyte display memory support (CL-GD5434/'36)
  - — 1/2-, 1-, and 2-Mbyte display memory support (CL-GD5430/'40)
  - — Optimized EDO (extended data out) DRAM support (CL-GD5436)
- **64 × 64 hardware cursor**
- **Glueless PCI bus interface with VGA BIOS ROM support for single 8-bit EPROM**
- **Low-power 5-V CMOS, 208-pin PQFP package**

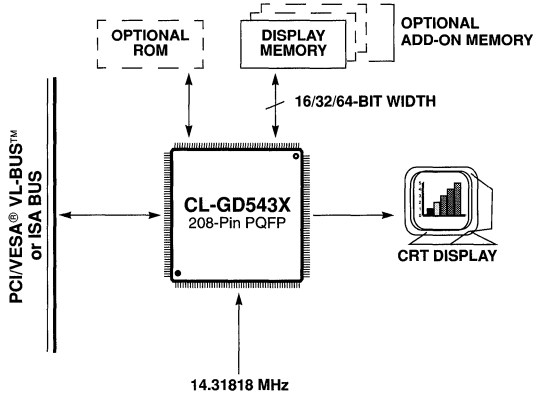
VGA GUI Accelerators

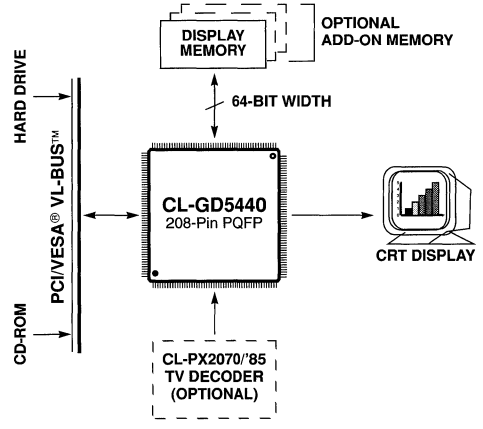
CL-GD5440	— Video Accelerator
CL-GD5434/'36	— 64-bit GUI Accelerators
CL-GD5430	— 32-bit GUI Accelerator

- **'Green PC' power-saving features**
  - — VESA® support for DPMS (display power-management signalling)
  - — Internal DAC with Power-Down mode
  - — Low-frequency DRAM refresh (CL-GD5430/'36/'40)
  - — Static monitor sync signals
- **100% hardware- and BIOS-compatible with IBM® VGA display standard**
- **Programmable dual-clock synthesizer**
- **Multimedia-ready *CL-GD5430/'34/'36***
  - — Video overlay with external video data and 'Color Keying'
  - — GENLOCK support with external HSYNC and/or VSYNC
  - — VAFC (VESA® advanced feature connector) Baseline support (CL-GD5430/'36)
  - — Horizontal pixel interpolation for baseline VAFC 2× mode (CL-GD5436)
- **CL-GD5428/'29 register- and software-compatible**

(cont.)

System Block Diagrams





DEVICE-SPECIFIC FEATURES

CL-GD5430/'34

- **Enhanced GUI acceleration**
  - — 64-bit BitBLT (bit block transfer) engine (CL-GD5434)
  - — 32-bit BitBLT engine (CL-GD5430)
- **Resolutions to 1280 × 1024**
  - — Up to 1024 × 768 × 64K colors, non-interlaced
  - — Up to 800 × 600 × 16M colors, non-interlaced
  - — Up to 1280 × 1024 × 256 colors, non-interlaced
- **VESA® DDC2B monitor support *(CL-GD5434)***
- **Integrated clock filter and current reference *(CL-GD5434-I)***

CL-GD5436

- **64-bit GUI acceleration**
  - — Double-buffered, memory-mapped BitBLT registers
  - — Color expansion for all data widths
  - — Efficient use of DRAM Fast-Page mode cycles
  - — Large BitBLT data buffers
- **Accelerated support for Packed-24 modes**
  - — Better performance than 32-bit true color
  - — Supports Microsoft® Windows95™
  - — Allows 1024 × 768 × 16M colors at 75 Hz with DRAM
- **Resolutions to 1280 × 1024**
  - — Up to 1024 × 768 × 16M colors, non-interlaced
  - — Up to 1280 × 1024 × 256 colors, non-interlaced
- **Integrated clock filter and current reference**
- **PCI byte-swapping for PowerPC™**
- **VESA® DDC2B monitor support**

CL-GD5440

- **Cost-effective hardware-accelerated video playback**
  - — High-quality video playback from CD-ROM and disk-based files
  - — High-quality video playback in 256 and 64K color modes
  - — Indeo™ and Cinepack™ file playback to 30 fps
- **Continuous hardware-interpolated zoom (CD-Zoom™)**
  - — X-interpolated zoom from 1× to 4×
  - — Y-interpolated zoom from 2× to 4×
  - — Full-screen playback to 1024 × 768
- **Integrated color space converter**
  - — On-the-fly YUV-to-RGB conversion
  - — YUV 4:2:2 (CCIR601)
- **Error-diffusion filtering offers color enhancement for video**
  - — 'High color' quality playback in 8- and 16-bit color graphic modes
- **Unique 32-bit multimedia frame buffer**
  - — Video (YUV) and graphics (RGB) share one frame buffer
  - — Allows different color depths between video and graphics
  - — Full operation with 512-Kbyte, 1-Mbyte, or 2-Mbyte DRAM
- **Video data encoding reduces frame-buffer bandwidth requirement**
  - — High-quality video playback of 1024 × 768 in 256 colors, and 800 × 600 in 64K colors with only 1 Mbyte of DRAM
- **Resolutions to 1280 × 1024**
  - — Up to 1024 × 768 × 256 colors, non-interlaced
  - — Up to 800 × 600 × 64K colors, non-interlaced
  - — Up to 1280 × 1024 × 16 colors, interlaced
- **Direct TV-decoder interface**
- **VESA® DDC2B monitor support**
- **Integrated clock filter and current reference**

FAMILY OVERVIEW

Based on a 64-bit GUI engine, the CL-GD543X/'4X incorporates a BitBLT (bit block transfer) VGA controller with a 24-bit true-color DAC, dual-clock synthesizer, and direct-connect 32-bit PCI and VESA® VL-Bus™ interface. Optimized for Microsoft Windows®, Windows95™, Windows NT™, OS/2®, and other graphical interfaces, the Alpine family offers performance, surpassing current DRAM and many VRAM-based GUI accelerators.

The CL-GD543X/'4X forms the heart of a cost-effective, high-performance DRAM-based graphics system. By combining a 32-bit external local bus interface with a 64-bit path to the DRAM frame buffer, the CL-GD543X/'4X eliminates the video-memory bottleneck found in traditional DRAM architectures. This combination also maximizes system-to-video bandwidth critical for outstanding graphics acceleration.

BitBLT support, linear addressing, hardware cursor, color expansion, and memory-mapped I/O are some of the many built-in CL-GD543X/'4X features that ensure outstanding GUI performance. The internal palette DAC can be configured for industry-standard 16- or 256-color VGA modes, or extended to high- and true-color modes (32K, 64K, or 16M colors).

The CL-GD5434-I, CL-GD5436, and CL-GD5440-I devices have an integrated clock filter and current reference that allow a low-cost board solution.

The highly integrated 208-pin PQFP package makes the CL-GD543X/'4X ideal for both motherboard systems and add-in cards. The only external support needed is cost-effective DRAM memory and a 14.31818-MHz frequency reference.

CL-GD5430/'34

The software- and pin-compatible CL-GD5430/'34 allow OEMs to meet different price and performance targets with one graphic subsystem design. Built on a 1-Mbyte frame buffer, the CL-GD5430 can be quickly upgraded to the higher-performance CL-GD5434. With a 2-Mbyte frame buffer, the CL-GD5434 offers performance beyond current 32-bit standard and interleaved architectures.

Operating at pixel clock rates programmable to 135 MHz (CL-GD5434) and 86 MHz (CL-GD5430), the CL-GD543X devices supports standard and VESA high-resolution extended modes. Display resolutions up to 1280 × 1024 are supported.

CL-GD5436

The CL-GD5436 is a high-performance accelerated super VGA controller. The CL-GD5436 features a 64-bit BitBLT engine and a 64-bit display memory interface with support for EDO DRAMs.

Operating at pixel clock rates programmable to 135 MHz and memory clock rates programmable to 80 MHz, the CL-GD5436 supports resolutions and color depths at the following standard refresh rates:

Resolution	256 Colors	64K Colors	16M Colors
640 × 480	75 Hz	75 Hz	75 Hz
800 × 600	75 Hz	75 Hz	75 Hz
1024 × 768	75 Hz	75 Hz	75 Hz
1280 × 1024	75 Hz	43i Hz	–

The CL-GD5436 supports Packed-24 RGB video modes, providing 16M colors at only 3 bytes per pixel. This allows 1024 × 768 true color at a 75-Hz refresh rate with DRAMs. The CL-GD5436 also supports three types of byte-swapping on the PCI bus, which provide PowerPC™ support.

CL-GD5440

The CL-GD5440 is the first product in its class to integrate on a single chip the CL-GD5430 (32-bit graphics accelerator) and the CL-PX2070/'85 video-processor accelerator (video technology from Pixel Semiconductor). Hardware-accelerated zoom with X and Y linear interpolation and color space conversion are combined with an enhanced BitBLT accelerator, integrated 24-bit RAMDAC, and a dual-clock synthesizer.

The CL-GD5440 accelerates both graphics and video playback for Microsoft Windows and Windows NT, OS/2, and other graphical interfaces. High-quality video playback is supported in both 64K, and the popular 256-color modes, allowing video playback without compromising graphics performance.

Operating at pixel clock rates programmable to 86 MHz, the CL-GD5440 supports standard and VESA high-resolution extended modes. Display resolutions up to 1280 × 1024 are supported.

A flexible 512-Kbyte to 2-Mbyte frame buffer, glueless PCI and VESA VL-Bus interface, and direct interface to NTSC/PAL decoder (and fully integrated video/graphics accelerator) provides OEMs with a cost-effective multimedia solution.

CD-Zoom, 'on-the-fly' color space conversion, video data encoding/decoding, and a multi-format frame buffer are integrated features that ensure high-performance video playback.

UNIQUE FEATURES

BENEFITS

Cost Effectiveness

- Interface to as few as one DRAM (CL-GD5430/'34/'40) or two DRAMs (CL-GD5434/'36), built-in true-color palette DAC and dual-frequency synthesizer
  - ❒ Minimizes chip count, system cost, and board space for cost-effective solution.
- Interface to ×4, ×8, ×16 DRAMs
  - ❒ Allows design flexibility for appropriate type and amount of memory.

High Performance

- Hardware BitBLT for Microsoft® Windows®
  - ❒ Accelerates GUIs such as Microsoft® Windows® and similar applications.
- 32-bit PCI, VESA® VL-Bus™, and local bus interface
  - ❒ Increases system throughput.
- 64-bit-wide DRAM interface (CL-GD5434/'36 only)
  - ❒ Eliminates display-memory bottleneck.
- Independent video and DRAM timing
  - ❒ Optimizes timing for increased performance.
- Maximum Fast-Page mode access to display-memory DRAMs
  - ❒ Improves CPU performance by accessing maximum bandwidth available from DRAM display memory.
- Host access to DRAMs through advanced write buffers
  - ❒ Provides fast host access for writes to display memory.
- EDO DRAM support (CL-GD5436)
  - ❒ Uses latest DRAM technology.
- 32-bit memory-mapped BitBLT Control registers
  - ❒ Improves graphics-application performance.
- 15-, 16-, or 24-bit true-color palette DAC
  - ❒ Provides high-color and true-color display for photo-realistic images. 32K, 64K, or 16M colors on screen at once for lifelike images.

Multimedia

- Overlay, color keying, and GENLOCK
  - ❒ Allows 16-bit-pixel interfacing through the VESA® connector for multimedia applications.

CL-GD5440–Specific

- Hardware-interpolated video zoom
  - ❒ Increases speed and quality of video playback at full screen.
- Single video-and-graphics frame buffer
  - ❒ Increases DRAM efficiency — RGB and YCrCb share one frame buffer.
- Hardware YUV-to-RGB conversion
  - ❒ Reduces CPU overhead with a multiformat frame buffer.
- Video data encoding converts 16-bit YUV pixels into 8-bit data
  - ❒ Reduces frame buffer bandwidth requirement.
- Vision Port™ enhanced feature connector
  - ❒ Enables CD-Zoom™ functionality on the VAFC or 8-bit standard feature connector; this eliminates need for an additional frame buffer and controller.
- Direct TV-decoder interface
  - ❒ Removes need for separate video frame buffer.

Compatibility

- Compatible with VGA and VESA® standards
  - ❒ Allows compatibility with installed base of systems and software.
- Drivers supplied at various resolutions for Windows® 3.1, Windows NT™, Windows95™, AutoCAD7®, OS/2®, and other key applications
  - ❒ Provides a 'ready-to-go' solution that minimizes the need for additional driver development.
- Connects directly to IBM® PS/2® and multifrequency analog monitors
  - ❒ Drives all industry-standard, high-resolution PC-monitors to ensure compatibility.

SOFTWARE SUPPORT

CL-GD543X VGA Software Drivers

Cirrus Logic provides an extensive and expanding range of software drivers to enhance the resolution and performance of many software packages. However note, that the CL-GD543X/'4X VGA graphics portion of a system *does not* require software drivers to run applications in standard-resolution mode.

Software Drivers	Resolution Supported[a]	No. of Colors
Microsoft® Windows® v3.1	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600, 1024 × 768	256 65,536 16.8 million
Microsoft® Windows NT™ v3.1	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	16 and 256
Microsoft® Windows NT™ v3.5	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	16 256 65,536
Microsoft® Windows NT™ v3.5 for PowerPC™	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	16 256 65,536
OS/2® v2.1, v2.1.1, v3.0	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480	256 65,536 16.8 million
AutoCAD® v11, v12 Autoshade® v2.0 w/ Renderman, 3D Studio v1, v2	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600, 1024 × 768	16 256 32,768 65,536 16.8 million
WordStar® v5.5–7.0	800 × 600, 1024 × 768	16
SCO[b] UNIX®	640 × 480, 800 × 600, 1024 × 768	16 and 256

[a] All resolutions may not run on all monitor types; 640 × 480 drivers will run on IBM® PS/2®-type monitors. Extended resolutions are dependent upon monitor type and VGA system implementation.

[b] Shipped by Santa Cruz Operations.

BIOS SUPPORT

- **Fully IBM® VGA-compatible BIOS**
- **Relocatable, 32 Kbytes with VESA® VL-Bus™ and PCI local bus support**
- **VBE (VESA® BIOS extensions) support in ROM**
- **Support for DPMS (display power management signaling) in ROM**
- **VESA® monitor timing-compliant**

UTILITIES

- **Manufacturing test**
- **Windows DOS utilities**
- **Video mode configuration utility — CLMODE**
- **Set resolution in Windows— WINMODE**
- **Configured OEM system integration — OEMSI**

Table of Contents

Revision History

Major changes between the previous data book, dated March 1994, and this version are listed below.

The CL-GD5440 and the CL-GD5436 have been added to the Alpine family with pertinent package, timing, and functionality information provided.

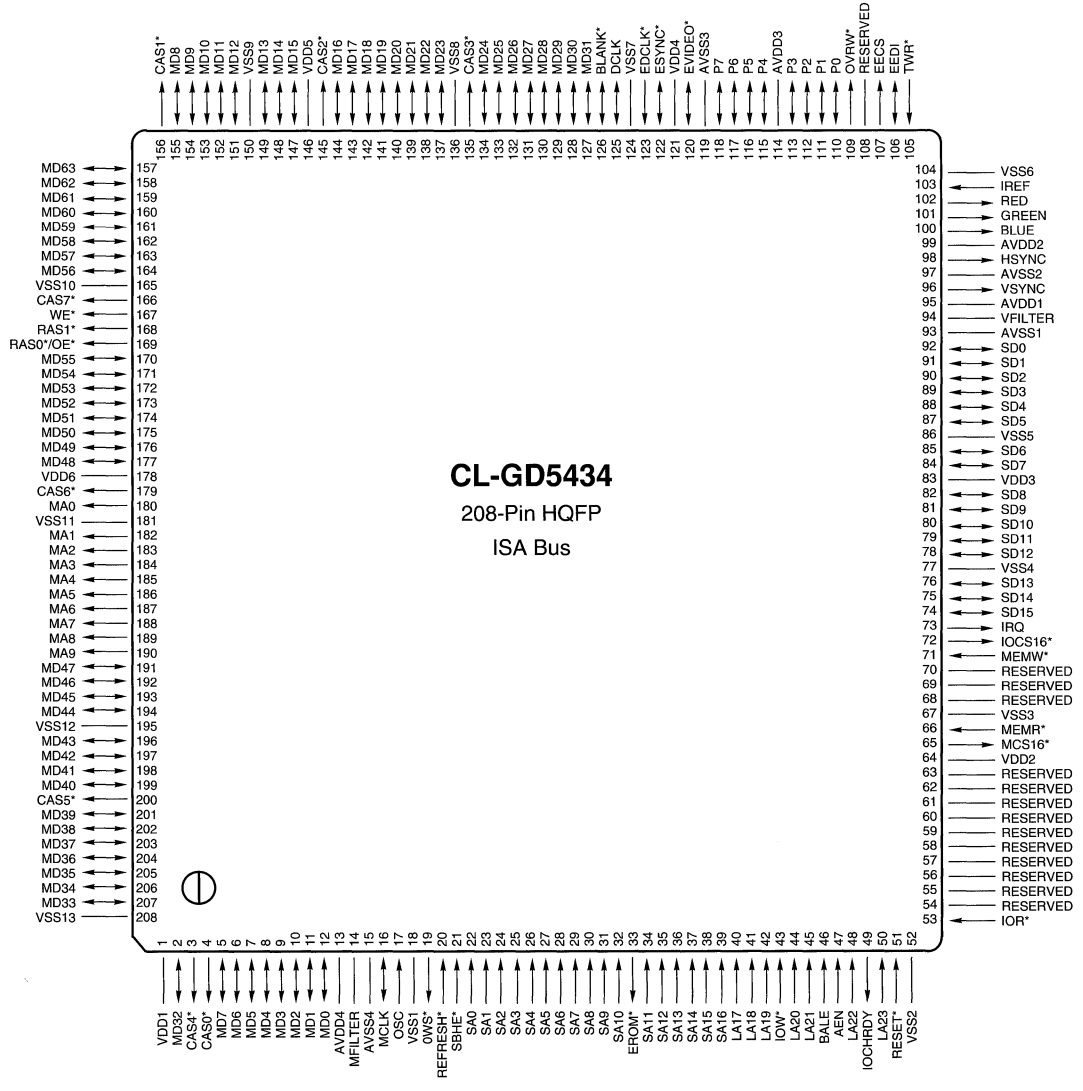
The timing diagrams and tables for the display memory bus are new.

The timing diagrams and tables for the P-bus have been modified.

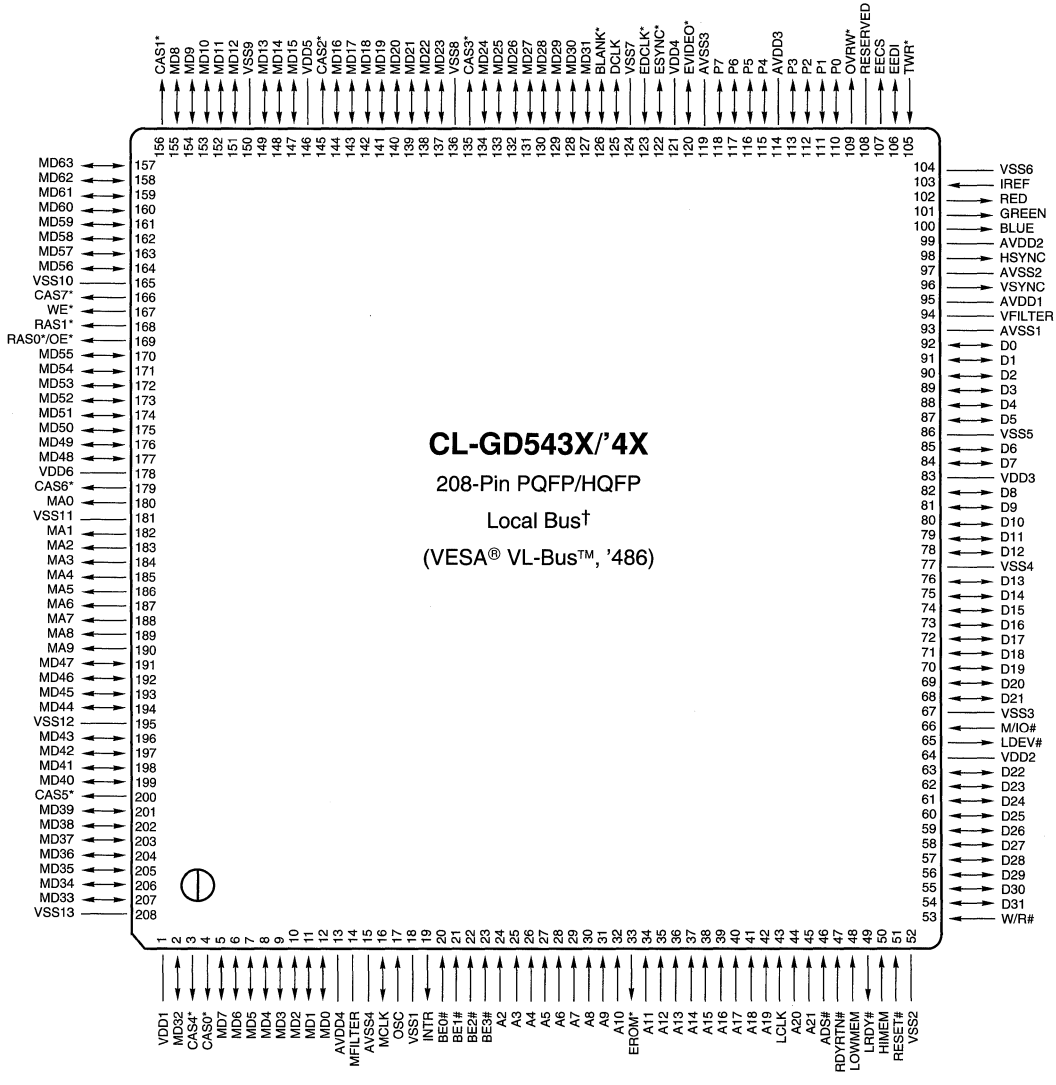
1. PIN INFORMATION

The CL-GD543X/'4X VGA GUI controllers are available in a 208-pin PQFP (plastic quad flat pack) or HQFP (high-performance quad flat pack) configuration. The CL-GD5430/'36/'40 devices can be configured for the VESA VL-Bus or PCI bus only. Additionally, the CL-GD5434 can be configured for the VESA VL-Bus, PCI, or ISA bus.

1.1 Pin Diagram — ISA Bus (CL-GD5434 Only)

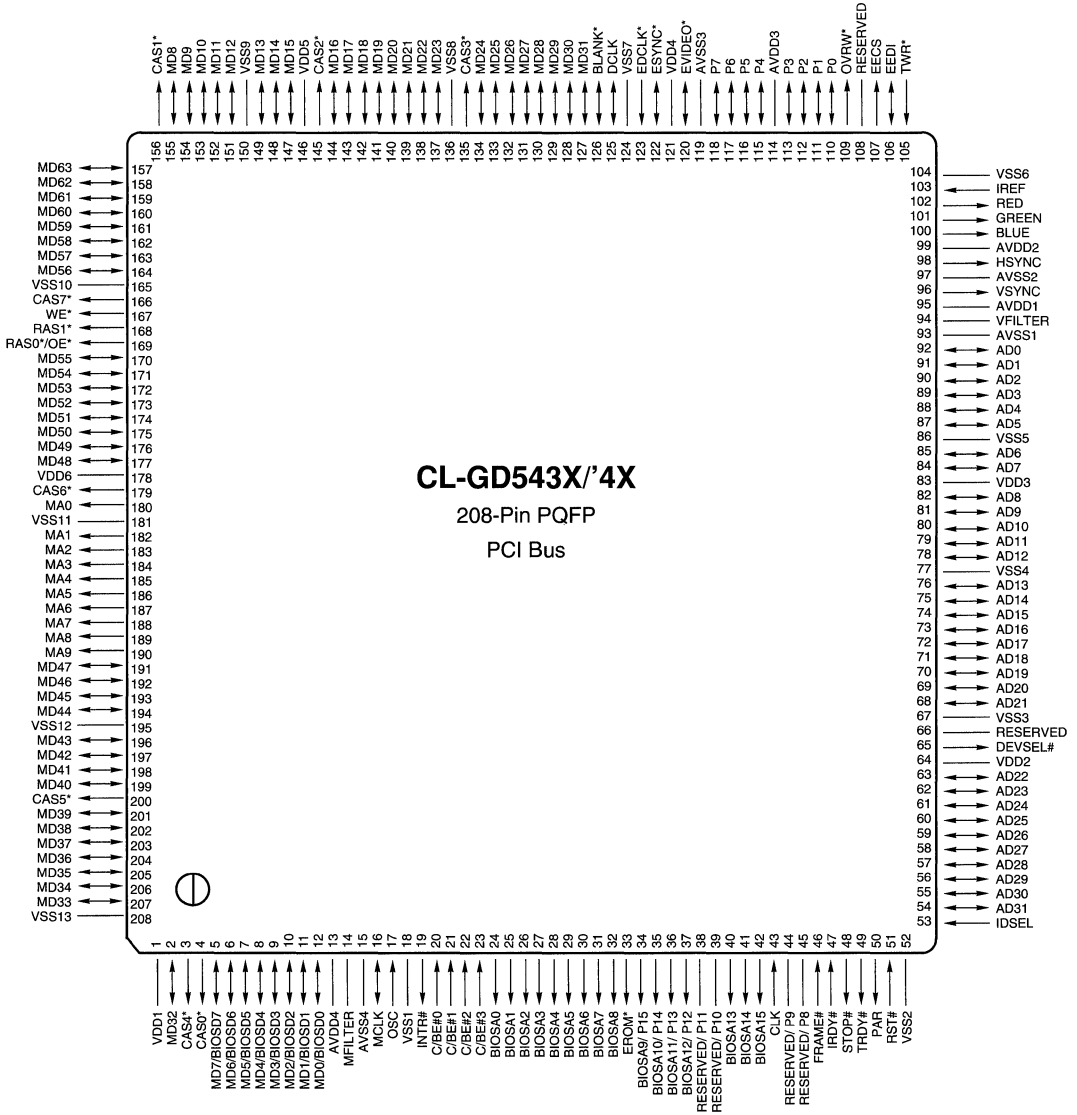


1.2 Pin Diagram — Local Bus (VESA® VL-Bus™, '486)



NOTE: † This pin diagram defines the pins forthe VESA VL-Bus and '486 local bus interfaces.

1.3 Pin Diagram — PCI Bus



1.4 Pin Summary

The following abbreviations are used for pin types in the following tables: (I) indicates input; (O) indicates output; (TS) indicates three-state; (OC) indicates open collector, I/O indicates input or output depending on how the device is configured.

Table 1-1. Host Interface

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	VESA® VL-Bus™	PCI	ISA *(CL-GD5434 only)*
50	I					HIMEM	–	LA23
50	O		–3	8	240	–	PAR	–
48	I					LOWMEM	–	LA22
48	O		–3	8	240	–	STOP#	–
45	I					A21	Reserved/P8[b]	LA21
44	I					A20	Reserved/P9[b]	LA20
42	I/O		–3	8	50	A19	BIOSA15	LA19
41	I/O		–3	8	50	A18	BIOSA14	LA18
40	I/O		–3	8	50	A17	BIOSA13/P10[b]	LA17
39	I/O			8	50	A16	Reserved /P11[b]	SA16
38	I/O					A15	Reserved/P12[b]	SA15
37	I/O					A14	BIOSA12/P13[b]	SA14
36	I/O		–3	8	50	A13	BIOSA11/P14[b]	SA13
35	I/O		–3	8	50	A12	BIOSA10/P15[b]	SA12
34	I/O		–3	8	50	A11	BIOSA9	SA11
32	I/O		–3	8	50	A10	BIOSA8	SA10
31	I/O		–3	8	50	A9	BIOSA7	SA9
30	I/O		–3	8	50	A8	BIOSA6	SA8
29	I/O		–3	8	50	A7	BIOSA5	SA7
28	I/O		–3	8	50	A6	BIOSA4	SA6
27	I/O		–3	8	50	A5	BIOSA3	SA5
26	I/O		–3	8	50	A4	BIOSA2	SA4
25	I/O		–3	8	50	A3	BIOSA1	SA3
24	I/O		–3	8	50	A2	BIOSA0	SA2
23	I					BE3#	C/BE#3	SA1
22	I					BE2#	C/BE#2	SA0
54	I/O	❍[c]	–3	12	240	D31	AD31	Reserved
55	I/O	❍	–3	12	240	D30	AD30	Reserved
56	I/O	❍	–3	12	240	D29	AD29	Reserved
57	I/O	❍	–3	12	240	D28	AD28	Reserved
58	I/O	❍	–3	12	240	D27	AD27	Reserved
59	I/O	❍	–3	12	240	D26	AD26	Reserved
60	I/O	❍	–3	12	240	D25	AD25	Reserved
61	I/O	❍	–3	12	240	D24	AD24	Reserved

Table 1-1. Host Interface *(cont.)*

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	VESA® VL-Bus™	PCI	ISA *(CL-GD5434 only)*
62	I/O	❍	–3	12	240	D23	AD23	Reserved
63	I/O	❍	–3	12	240	D22	AD22	Reserved
68	I/O	❍	–3	12	240	D21	AD21	Reserved
69	I/O	❍	–3	12	240	D20	AD20	Reserved
70	I/O	❍	–3	12	240	D19	AD19	Reserved
71	I/O		–3	12	240	D18	AD18	MEMW*
72	I/O		–3	12	240	D17	AD17	IOCS16*
73	I/O		–3	12	240	D16	AD16	IRQ
74	I/O		–3	12	240	D15	AD15	SD15
75	I/O		–3	12	240	D14	AD14	SD14
76	I/O		–3	12	240	D13	AD13	SD13
78	I/O		–3	12	240	D12	AD12	SD12
79	I/O		–3	12	240	D11	AD11	SD11
80	I/O		–3	12	240	D10	AD10	SD10
81	I/O		–3	12	240	D9	AD9	SD9
82	I/O		–3	12	240	D8	AD8	SD8
84	I/O		–3	12	240	D7	AD7	SD7
85	I/O		–3	12	240	D6	AD6	SD6
87	I/O		–3	12	240	D5	AD5	SD5
88	I/O		–3	12	240	D4	AD4	SD4
89	I/O		–3	12	240	D3	AD3	SD3
90	I/O		–3	12	240	D2	AD2	SD2
91	I/O		–3	12	240	D1	AD1	SD1
92	I/O		–3	12	240	D0	AD0	SD0
21	I					BE1#	C/BE#1	SBHE*
20	I					BE0#	C/BE#0	REFRESH*
46	I					ADS#	FRAME#	BALE
47	I	●				RDYRTN#	IRDY#	AEN
53	I					W/R#	IDSEL	IOR*
43	I					LCLK	CLK	IOW*
66	I	●				M/IO#	Reserved	MEMR*
51	I					RESET#	RST#	RESET*[d]
49	TS		–3	8	240	LRDY#	TRDY#	IOCHRDY
65	O		–3	24	200	LDEV#	DEVSEL#	MCS16*
19	TS		(OC)	24	200	INTR	INTR#	0WS*

[a] ● indicates the presence of an internal 250 kΩ +/– 50% pull-up resistor.

[b] For the CL-GD5436 only, pins 35:40,44,45 can be redefined as P[15:8] inputs.

[c] ❍ indicates the presence of an internal 250 kΩ +/– 50% pull-up resistor when the CL-GD5434 is configured for ISA bus.

[d] An inverter is required to generate an active-low RESET* for ISA bus.

Table 1-2. Clock Synthesizer Interface

Pin Number	Pin Type	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
17	I				OSC
14	Analog				MFILTER
94	Analog				VFILTER
16	I/O	–12	12	20	MCLK

Table 1-3. Video Interface

Pin Number	Pin Type	Pull-up [a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
96	TS		–12	24	50	VSYNC
98	TS		–12	24	50	HSYNC
126	I/O		–12	12	50	BLANK*
35	I/O		–3	8	50	P15 [b]
36	I/O		–3	8	50	P14 [b]
37	I/O		–3	8	50	P13 [b]
38	I/O		–3	8	50	P12 [b]
39	I/O		–3	8	50	P11 [b]
40	I/O		–3	8	50	P10 [b]
44	I/O		–3	8	50	P9 [b]
45	I/O		–3	8	50	P8 [b]
118	I/O		–12	12	50	P7
117	I/O		–12	12	50	P6
116	I/O		–12	12	50	P5
115	I/O		–12	12	50	P4
113	I/O		–12	12	50	P3
112	I/O		–12	12	50	P2
111	I/O		–12	12	50	P1
110	I/O		–12	12	50	P0
125	I/O		–12	12	50	DCLK
122	I/O	●	–12	12		ESYNC* [c]
120	I/O	●	–12	12		EVIDEO* [d]
123	In	●				EDCLK*
102	Analog Out					RED
101	Analog Out					GREEN
100	Analog Out					BLUE
103	Analog In					IREF

[a] ● indicates the presence of an internal 250 kΩ +/– 50% pull-up resistor.

[b] For the CL-GD5436 only, P[15:8] are redefined PCI pins. See the definition of register GRE[7].

[c] ESYNC* is redefined as EEPROM SK if EEPROM interface is enabled.

[d] EVIDEO* is redefined as EEPROM DI if EEPROM interface is enabled.

Table 1-4. Display Memory Interface

Pin Number	Pin Type	Pull-up [a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
168	O		–12	12	50	RAS1*
169	O		–12	12	50	RAS0*/OE*
166	O		–12	12	50	CAS7* [b]
179	O		–12	12	50	CAS6* [b]
200	O		–12	12	50	CAS5* [b]
3	O		–12	12	50	CAS4* [b]
135	O		–12	12	50	CAS3* [b]
145	O		–12	12	50	CAS2* [b]
156	O		–12	12	50	CAS1* [b]
4	O		–12	12	50	CAS0* [b]
167	O		–12	12	150	WE* [c]
190	O		–12	12	150	MA9
189	O		–12	12	150	MA8 [d]
188	O		–12	12	150	MA7
187	O		–12	12	150	MA6
186	O		–12	12	150	MA5
185	O		–12	12	150	MA4
184	O		–12	12	150	MA3
183	O		–12	12	150	MA2
182	O		–12	12	150	MA1
180	O		–12	12	150	MA0 [e]
157	I/O	●	–8	8	50	MD63
158	I/O	●	–8	8	50	MD62
159	I/O	●	–8	8	50	MD61
160	I/O	●	–8	8	50	MD60
161	I/O	●	–8	8	50	MD59
162	I/O	●	–8	8	50	MD58
163	I/O	●	–8	8	50	MD57
164	I/O	●	–8	8	50	MD56
170	I/O	●	–8	8	50	MD55
171	I/O	●	–8	8	50	MD54
172	I/O	●	–8	8	50	MD53
173	I/O	●	–8	8	50	MD52
174	I/O	●	–8	8	50	MD51
175	I/O	●	–8	8	50	MD50
176	I/O	●	–8	8	50	MD49
177	I/O	●	–8	8	50	MD48
191	I/O	●	–8	8	50	MD47
192	I/O	●	–8	8	50	MD46

Table 1-4. Display Memory Interface *(cont.)*

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
193	I/O	●	–8	8	50	MD45
194	I/O	●	–8	8	50	MD44
196	I/O	●	–8	8	50	MD43
197	I/O	●	–8	8	50	MD42
198	I/O	●	–8	8	50	MD41
199	I/O	●	–8	8	50	MD40
201	I/O	●	–8	8	50	MD39
202	I/O	●	–8	8	50	MD38
203	I/O	●	–8	8	50	MD37
204	I/O	●	–8	8	50	MD36
205	I/O	●	–8	8	50	MD35
206	I/O	●	–8	8	50	MD34
207	I/O	●	–8	8	50	MD33
2	I/O	●	–8	8	50	MD32
127	I/O	●	–8	8	50	MD31
128	I/O	●	–8	8	50	MD30
129	I/O	●	–8	8	50	MD29
130	I/O	●	–8	8	50	MD28
131	I/O	●	–8	8	50	MD27
132	I/O	●	–8	8	50	MD26
133	I/O	●	–8	8	50	MD25
134	I/O	●	–8	8	50	MD24
137	I/O	●	–8	8	50	MD23
138	I/O	●	–8	8	50	MD22
139	I/O	●	–8	8	50	MD21
140	I/O	●	–8	8	50	MD20
141	I/O	●	–8	8	50	MD19
142	I/O	●	–8	8	50	MD18
143	I/O	●	–8	8	50	MD17
144	I/O	●	–8	8	50	MD16
147	I/O	●	–8	8	50	MD15
148	I/O	●	–8	8	50	MD14
149	I/O	●	–8	8	50	MD13
151	I/O	●	–8	8	50	MD12
152	I/O	●	–8	8	50	MD11
153	I/O	●	–8	8	50	MD10
154	I/O	●	–8	8	50	MD9
155	I/O	●	–8	8	50	MD8
5	I/O	●	–8	8	50	MD7/BIOSD7[f]

Table 1-4. Display Memory Interface *(cont.)*

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
6	I/O	●	–8	8	50	MD6/BIOSD6[f]
7	I/O	●	–8	8	50	MD5/BIOSD5[f]
8	I/O	●	–8	8	50	MD4/BIOSD4[f]
9	I/O	●	–8	8	50	MD3/BIOSD3[f]
10	I/O	●	–8	8	50	MD2/BIOSD2[f]
11	I/O	●	–8	8	50	MD1/BIOSD1[f]
12	I/O	●	–8	8	50	MD0/BIOSD0[f]

[a] ● indicates the presence of an internal 250 kΩ +/– 50% pull-up resistor.
[b] CAS[7:0]* are redefined as WE[7:0]* for dual-WE* 256K × 16 DRAMs.
[c] WE* is redefined as CAS* for dual-WE* 256K × 16 DRAMs.
[d] MA8 is connected to Memory Address 0 for asymmetric DRAMs.
[e] MA0 is connected to Memory Address 8 for asymmetric DRAMs.
[f] For the PCI bus, MD[7:0] can also be configured as BIOSD[7:0].

Table 1-5. Miscellaneous Pins

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
107	O		–12	12	35	EECS
106	I/O		–12	12	35	EEDI
33	O		–12	12	35	EROM*
109	O		–12	12	35	OVRW*
105	I	●				TWR*
108	–					Reserved

[a] ● indicates the presence of an internal 250 kΩ +/– 50% pull-up resistor.

Table 1-6. Power and Ground

Pin Number	Pin Type	Name	Note
178	Power	VDD6	Digital
146	Power	VDD5	Digital
121	Power	VDD4	Digital
83	Power	VDD3	Digital
64	Power	VDD2	Digital
1	Power	VDD1	Digital
208	Ground	VSS13	Digital
195	Ground	VSS12	Digital
181	Ground	VSS11	Digital
165	Ground	VSS10	Digital
150	Ground	VSS9	Digital
136	Ground	VSS8	Digital
124	Ground	VSS7	Digital
104	Ground	VSS6	Digital
86	Ground	VSS5	Digital
77	Ground	VSS4	Digital
67	Ground	VSS3	Digital
52	Ground	VSS2	Digital
18	Ground	VSS1	Digital
95	Power	AVDD1	VCLK
93	Ground	AVSS1	VCLK
13	Power	AVDD4	MCLK
15	Ground	AVSS4	MCLK
114	Power	AVDD3	DAC
99	Power	AVDD2	DAC
119	Ground	AVSS3	DAC
97	Ground	AVSS2	DAC

2. DETAILED PIN DESCRIPTIONS

The following abbreviations are used for pin types in the following sections: (I) indicates input, (O) indicates output, (TS) indicates three-state, (OC) indicates open collector, I/O indicates input or output depending on how the chip is configured.

2.1 Host Interface — ISA Bus Mode (CL-GD5434 only)

Name	Type	Description
LA[23:17]	I	**ADDRESS [23:17]:** These inputs, in conjunction with SA[16:0], are used to select the resource to be accessed during memory operations. These address bits are latched with the falling edge of BALE.
SA[16:0]	I	**ADDRESS [16:0]:** These inputs, in conjunction with LA[23:17], are used to select the resource to be accessed during any memory or I/O operation. These address bits must remain valid throughout the cycle.
SD[15:8]	TS	**SYSTEM DATA [15:8]:** These bidirectional pins are used to transfer data during 16-bit memory or I/O operations. These pins may be connected directly to the corresponding ISA bus pins.
SD[7:0]	TS	**SYSTEM DATA [7:0]:** These bidirectional pins are used to transfer data during any memory or I/O operation. These pins may be connected directly to the corresponding ISA bus pins.
SBHE*	I	**SYSTEM BYTE HIGH ENABLE*:** This input is used in conjunction with A0 to determine the width and alignment of a data transfer. SBHE* and A0 are decoded as shown in Table 2-1 below: **Table 2-1. SBHE*/A0 Decoding** SBHE* / A0 / Function: 0 / 0 / 16-bit Transfer 0 / 1 / Upper-byte Transfer 1 / 0 / Lower-byte Transfer 1 / 1 / Lower-byte Transfer *(on odd address)*
BALE	I	**BUS ADDRESS LATCH ENABLE:** This active-high input is used to latch LA[23:17] on the high-to-low transition.
AEN	I	**ADDRESS ENABLE:** If this input is high, it indicates that the current cycle is a DMA cycle. In this case, the CL-GD5434 will not respond to I/O cycles. There is no effect on memory cycles.

2.1 Host Interface — ISA Bus Mode (CL-GD5434 only) *(cont.)*

Name	Type	Description
IOR*	I	**I/O READ*:** This active-low input is used to indicate that an I/O read is occurring. If the address on SA[15:0] is within the range of the CL-GD5434, it will respond by placing the contents of the appropriate register on the System Data bus.
IOW*	I	**I/O WRITE*:** This active-low input is used to indicate that an I/O write is occurring. If the address on SA[15:0] is within the range of the CL-GD5434, it will respond by transferring the contents of the System Data bus into the appropriate register. The transfer will occur on the trailing (rising) edge of this signal. A list of I/O addresses to which the CL-GD5434 will respond appears in Section 5, "VGA Register Port Map". When a 16-bit I/O write is done, the address specified will be the Index register for one of the VGA groups. The index must appear on SD[7:0] and the data must appear on SD[15:8].
MEMR*	I	**MEMORY READ*:** This active-low input is used to indicate that a memory read is occurring. If linear addressing is being used, this pin must be connected to ISA signal MEMR*. If linear addressing is not being used, this pin may be connected to ISA signal SMEMR*. The CL-GD5434 decodes LA[23:17] and SA[16:15] to determine if a display memory read is occurring. If so, data is placed on the System Data pins according to the Read mode and the contents of display memory. The CL-GD5434 decodes LA[23:17] and SA[16:15] to determine if a BIOS read is occurring. If so, the CL-GD5434 makes EROM* active for the duration of MEMR*.
MEMW*	I	**MEMORY WRITE*:** This active-low input is used to indicate that a memory write is occurring. If linear addressing is being used, this pin must be connected to ISA signal MEMW*. If linear addressing is not being used, this pin may be connected to ISA signal SMEMW*. The CL-GD5434 decodes LA[23:17] and SA[16:15] to determine if a display memory write is occurring. If so, data is written into display memory according to the Write mode and the data on SD[15:0]. The data is latched in the CL-GD5434 on the rising edge of this signal, and is actually transferred to display memory later.
RESET*	I	**RESET*:** This active-low signal is used to initialize the CL-GD5434 to a known state. The trailing (rising) edge of this input loads the Configuration register CF[15:0] with the data on MD[63:48], determined by internal pull-up resistors and optional external pull-down resistors. An inverter is required to generate an active-low RESET*.
REFRESH*	I	**REFRESH*:** This active-low signal indicates that a DRAM refresh is occurring. The CL-GD5434 ignores memory read operations occurring when REFRESH* is active since it explicitly controls the refresh of display memory.

2.1 Host Interface — ISA Bus Mode (CL-GD5434 only) *(cont.)*

Name	Type	Description
IOCHRDY	TS	**I/O CHANNEL READY:** This output, when driven low, indicates that additional wait states are to be inserted into the current display memory read or write cycle. This output is never driven low during I/O cycles or BIOS reads. During a display memory read cycle, this signal is always driven low as soon as MEMR* goes active. When the data are ready to be placed on the System Data bus, this signal is driven high. It remains high until MEMR* goes inactive; it then goes high-impedance. During a display memory write cycle, this signal is driven high as soon as MEMW* goes active if there is space in the Write Buffer. If there is no space in the Write Buffer, this signal is driven low as soon as MEMW* goes active and remains low until there is space. Once there is space in the Write Buffer, this signal is driven high. It will remain high until MEMW* goes inactive; it then goes high-impedance.
IOCS16*	OC	**I/O CHIP SELECT 16*:** This open-collector output is driven low to indicate that the CL-GD5434 can execute an I/O operation at the address currently on the bus in 16-bit mode. This signal is generated from a decode of SA[15:0] and AEN. Table 2-2 indicates the range of addresses for which the CL-GD5434 will generate IOCS16*: **Table 2-2. IOCS16* Addresses** **Address** / **Function** 3C4, 3C5 — Sequencer 3CE, 3CF — Graphics Controller 3B4/3D4, 3B5/3D5 — CRT Controller 3BA/3DA — Input Status Register 1

2.1 Host Interface — ISA Bus Mode (CL-GD5434 only) *(cont.)*

Name	Type	Description
MCS16*	OC	**MEMORY CHIP SELECT 16*:** This open-collector output is driven low to indicate that the CL-GD5434 can execute a memory operation at the address currently on the bus in 16-bit mode. Table 2-3 summarizes the conditions under which MCS16* is made active.

Table 2-3. MSC16* Addresses

Resource	Address Bits	Address Range	Qualifier
Display Memory	LA[23:17]	A000:0–BFFF:F	SR8[6] = 0 (No other VGA card)
Display Memory	LA[23:17]	1–4 Mbyte	SR7[7:4] ≠ 0 Linear Addressing
BIOS	LA[23:17] and SA[16:15]	C000:0–C7FF:F	CF[6] = 0 (16-bit BIOS)

NOTE: The SA bits are generated late, and cannot be used for generating MCS16* unless special provisions are made. The CL-GD5434 uses a fast path from SA[16:15] to MCS16*.

0WS*	OC	**ZERO WAIT STATE*:** This open-collector output is driven low to indicate that the current cycle can be completed without any additional wait states. This is typically connected to SRDY* with a jumper.
IRQ	TS	**INTERRUPT REQUEST:** This active-high output indicates the CL-GD5434 has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. This pin is typically unused in PC/AT add-in cards, but may be connected to IRQ2/IRQ9 via a jumper block. See register CR11 for a description of the controls for this pin.

2.2 Host Interface — Local Bus Mode

A number of bus interface pins are redefined according to the local bus type to which the CL-GD543X/'4X is connected. These are listed in Table 2-4, which is ordered by CL-GD543X/'4X pin number.

Table 2-4. Redefined Host Interface Pins

Pin Number	VESA® VL-Bus™	PCI™
20	BE0#	C/BE#0
21	BE1#	C/BE#1
22	BE2#	C/BE#2
23	BE3#	C/BE#3
43	LCLK	CLK
46	ADS#	FRAME#
47	RDYRTN#	IRDY#
48	LOWMEM	STOP#
49	LRDY#	TRDY#
50	HIMEM	PAR
51	RESET#	RST#
53	W/R#	IDSEL
65	LDEV#	DEVSEL#
66	M/IO#	LOCK#

2.2.1 VESA® VL-Bus™ and '486 Bus Interface

Name	Type	Description
HIMEM	I	**HIGH MEMORY:** This active-high input signal is used in conjunction with LOWMEM to indicate the address space being used. See the table with LOWMEM.
LOWMEM	I	**LOW MEMORY:** This active-high input signal is used in conjunction with HIMEM to indicate the address space being used as defined in Table 2-5.
A[21:2]	I	**ADDRESS [21:2]:** These inputs are used to select the resource to be accessed during memory or I/O operation. A[21:17] have internal pull-up resistors; A[16:2] do not.
D[31:0]	TS	**DATA[31:0]:** These bidirectional pins are used to transfer data during any memory or I/O operation. These pins are directly connected to D[31:0] of the VESA VL-Bus or the '486 bus.
BE[3:0]#	I	**BYTE ENABLE [3:0]#:** These active-low inputs are connected directly to the VESA VL-Bus or the '486 Byte Enable Outputs. BE0# applies to byte 0 and BE3# to byte 3.
ADS#	I	**ADDRESS STROBE#:** This active-low input indicates that a new cycle has begun. It must be connected directly to the ADS# pin on the VESA VL-Bus or the '486 bus.

Table 2-5. Memory Area

HIMEM	LOWMEM	Comments
0	0	No response
0	1	Standard VGA Map A000:0–BFFF:F SR7[7:4] = 0
1	0	No response
1	1	Linear display memory SR7[7:4] ≠ 0

2.2.1 VESA® VL-Bus™ and '486 Bus Interface *(cont.)*

Name	Type	Description
RDYRTN#	I	**READY RETURN#:** This input establishes a handshake between the CL-GD543X/'4X and VESA VL-Bus, so the CL-GD543X/'4X is informed when the cycle has ended. RDYRTN# is typically asserted in the same LCLK cycle as LRDY# is asserted. If LCLK is higher than 33 MHz, RDYRTN# may trail LRDY# by one LCLK cycle. During DMA or system I/O bus master signals, RDYRTN# is asserted for one LCLK cycle when the DMA or system I/O bus masters command ends. This pin is connected to RDYRTN# of the VESA VL-Bus.
LRDY#	TS	**READY#:** This active-low signal is used as an output to terminate a CL-GD543X/'4X bus cycle. This pin is connected to LRDY# for the VESA VL-Bus and RDY# of the '486 bus.
W/R#	I	**WRITE/READ#:** This input indicates whether a write or read operation is to occur. It must be connected directly to the W/R# pin on the CPU or VESA bus. If W/R# is high, a write will occur. If W/R# is low, a read will occur.
M/IO#	I	**MEMORY/IO#:** This input indicates whether a memory or I/O operation is to occur. It must be connected directly to the M/IO# pin on the CPU or VESA bus. If M/IO# is high, a memory operation will occur. If it is low, an I/O operation will occur.
LCLK	I	**CLOCK:** This input is the timing reference for the CL-GD543X/'4X. It must be connected directly to the corresponding CPU Clock pin. For VESA VL-Bus, this pin is connected to LCLK. For '486 bus, this pin is connected to CLK.
RESET#	I	**RESET#:** This active-low input initializes the CL-GD543X/'4X to a known state. The trailing (rising) edge of this input loads the Configuration register CF[15:0] with the data on MD[63:48], determined by internal pull-up resistors and optional external pull-down resistors.
LDEV#	O	**LOCAL DEVICE#:** This open-collector output is driven low to indicate that the CL-GD543X/'4X will respond to the current cycle. This pin is connected to LDEV#.
INTR	TS	**INTERRUPT REQUEST:** This active-high output indicates that CL-GD543X/'4X has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. See register CR11 for a description of controls for this pin.

2.2.2 PCI™ Bus Interface

Name	Type	Description
PAR	TS	**PARITY:** This signal provides even parity across AD[31:0] and C/BE#[3:0]. The CL-GD543X/'4X will sample this signal during write cycles and assert the correct parity for read cycles to the CL-GD543X/'4X.
STOP#	TS	**STOP#:** This active-low output indicates a current request to the PCI Bus Master to stop the current transaction.
AD[31:0]	TS	**ADDRESS AND DATA [31:0]:** These multiplexed and bidirectional pins are used to transfer system address and data during any memory or I/O operation on the PCI bus. These pins directly connect to AD[31:0] of the PCI bus Interface. During the first clock of a transaction, these pins contain a 32-bit physical byte address. During subsequent clocks, they contain data.
BIOSA[15:0]	O/I	**BIOS ADDRESS [15:0]:** These output pins are latched from the AD[31:0] bus, and are used to address the video system BIOS. These signals are directly connected to the address inputs of the 8-bit ROM. BIOSA[13:10] can be redefined as Pixel bus inputs for the the CL-GD5436.
BIOSD[7:0]	I	**BIOS DATA [7:0]:** These input pins are used to transfer data during a video system BIOS operation. These pins are directly connected to data outputs of an 8-bit ROM. These pins are multiplexed with MD[7:0].

2.2.2 PCI™ Bus Interface *(cont.)*

Name	Type	Description
C/BE#[3:0]	–	**COMMAND AND BYTE ENABLE#[3:0]:** These multiplexed pins are used to transfer Bus Command and Byte Enables during any memory or I/O operation on the PCI bus. These pins directly connect to C/BE#[3:0] of the PCI bus interface. During the address phase of the operation, C/BE#[3:0] define the bus command (refer to the Table 2-6). During the data phase, they are used as Byte Enable Outputs. C/BE#0 applies to byte 0 and C/BE#3 applies to byte 3.
FRAME#	I	**FRAME#:** This active-low input indicates the beginning and duration of an access. FRAME# will be asserted to indicate the beginning of a bus transaction. While FRAME# is asserted, data transfers continue. The transaction is in its final data phase when FRAME# is deasserted.

Table 2-6. Command and Byte Enable

C/BE#3	C/BE#2	C/BE#1	C/BE#0	Command Type	Comments
0	0	0	0	Interrupt Acknowledge	–
0	0	0	1	Special Cycle	–
0	0	1	0	I/O Read	Valid
0	0	1	1	I/O Write	Valid
0	1	0	0	Reserved	–
0	1	0	1	Reserved	–
0	1	1	0	Memory Read	Valid
0	1	1	1	Memory Write	Valid
1	0	0	0	Reserved	–
1	0	0	1	Reserved	–
1	0	1	0	Configuration Read	Valid
1	0	1	1	Configuration Write	Valid
1	1	0	0	Memory Read Multiple	–
1	1	0	1	Dual Address Cycle	–
1	1	1	0	Memory Read Line	–
1	1	1	1	Memory Write and Invalidate	–

2.2.2 PCI™ Bus Interface *(cont.)*

Name	Type	Description
IRDY#	I	**INITIATOR READY#:** This input establishes a handshake between the CL-GD543X/'4X and PCI bus so the CL-GD543X/'4X is informed when the cycle has ended. Wait states are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	TS	**TARGET READY#:** This active-low signal is used as an output to terminate a CL-GD543X/'4X bus cycle. This pin is connected to TRDY# for the PCI bus.
IDSEL	I	**INITIALIZATION DEVICE SELECT:** This input signal is used as a chip select in lieu of the upper 24 address lines during configuration read and write cycles.
CLK	I	**CLOCK:** This is the timing reference for the CL-GD543X/'4X when connected to a local bus. It must be connected directly to the CLK pin of the PCI bus.
RST#	I	**RESET#:** This active-low input initializes the CL-GD543X/'4X to a known state. The trailing (rising) edge of this input loads the Configuration register CF[15:0] with the data on MD[63:48], determined by internal pull-up resistors and optional external pull-down resistors.
DEVSEL#	TS	**DEVICE SELECT#:** This open-collector output is driven low to indicate that the CL-GD543X/'4X will respond to the current cycle. This pin is connected to DEVSEL# of the PCI bus.
INTR#	TS	**INTERRUPT REQUEST#:** This active-low output indicates that CL-GD543X/'4X has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. See register CR11 for a description of controls for this pin.

2.3 Dual-Frequency Synthesizer Interface

Name	Type	Description
OSC	I	**OSCILLATOR INPUT:** This TTL-input pin supplies the reference frequency for the dual-frequency synthesizer. It requires an input frequency of 14.31818 ± 0.01% MHz with a duty cycle of 50 ± 10%. This input can be supplied from the appropriate pin on the ISA bus, or from a crystal oscillator. For products with integrated synthesizer filters, this pin can connect to a 14.3 MHz crystal; the other connection is MFILTER.
MFILTER	O	**MEMORY CLOCK FILTER:** This pin must be connected to a π-RC filter returned to AVSS4. The values of the two capacitors and the resistor are shown in Appendixes B1–B3 in the *CL-GD543X/'4X Technical Reference Manual*. The filter components, especially the input capacitor and the resistor, must be placed as close as possible to this pin. For products with integrated synthesizer filters, this pin is either a n/c or the second connection to a 14.3 MHz crystal.
VFILTER	O	**VIDEO CLOCK FILTER:** This pin must be connected to a π-RC filter returned to AVSS1. The values of the two capacitors and the resistor are shown in Appendixes B1-B3 in the *CL-GD543X/'4X Technical Reference Manual*. The filter components, especially the input capacitor and the resistor, must be placed as close as possible to this pin. For products with integrated current reference, this pin is connected to a resistor in parallel with a capacitor to AVSS[3:2]. The resistor value is typically 135 ohms. The capacitor is typically 0.1 µF. See Appendix B8 for additional information.
MCLK	I/O	**MEMORY CLOCK:** This pin is normally an output and may be used to monitor the internal MCLK.Typically, it would not be connected. If CF[5] is a '0', MCLK will be an input and the internal MCLK Oscillator will be disabled. This configuration is intended for testing only. For the CL-GD5430/'36/'40 only, this pin can be configured to output the VCLK synthesizer.

2.4 Video Interface

Name	Type	Description
VSYNC	TS	**VERTICAL SYNC:** This output supplies the vertical synchronization pulse to the monitor. The polarity of this output is programmable. This pin is put into high-impedance when ESYNC* is low, or when vertical GENLOCK is enabled for those devices that support it. This pin may be connected directly to the corresponding pin on the feature connector.
HSYNC	TS	**HORIZONTAL SYNC:** This output supplies the horizontal synchronization pulse to the monitor. The polarity of this output is programmable. This pin is put into high-impedance when ESYNC* is low, or when horizontal GENLOCK is enabled for those devices that support it. This pin may be connected directly to the corresponding pin on the feature connector.
BLANK*	I/O	**BLANK*:** This is a bidirectional pin. If ESYNC* is high, BLANK* is an output. As an output, it supplies a blanking signal to the feature connector. If ESYNC* is low, BLANK* is an input. As an active-low input, it forces the RED, GREEN, and BLUE outputs to a '0' current. This pin may be connected directly to the corresponding pin on the feature connector. For the CL-GD5440 only, this pin is used as a handshake signal for Video Port mode.
P[7:0]	I/O	**PIXEL BUS [7:0]:** These are bidirectional pins. If EVIDEO* is high, these pins are outputs and reflect the address into the palette DAC. If EVIDEO* is low, these pins are inputs and can be used to drive pixel values into the palette DAC. These pins may be connected directly to the corresponding pins on the feature connector.
P[15:8]	I	**PIXEL BUS [15:8]** ***(CL-GD5436 only)*:** These pins are redefined PCI interface pins for the CL-GD5436 only. When the appropriate conditions are met, BIOSA[13:10] and four reserved pins are redefined as eight additional P-bus pins. See the description of register GRE[7].
DCLK	I/O	**DOT CLOCK:** This is a bidirectional pin. If EDCLK* is high, this is an output and may be used to externally latch the data on the Pixel bus. If EDCLK* is low, this is an input and may be used to clock data on the Pixel bus into the CL-GD543X/'4X. This pin may be connected directly to the corresponding pin on the feature connector.
ESYNC*	I/O	**ENABLE SYNC AND BLANK*:** This input is used to control the buffers on HSYNC, VSYNC, and BLANK*. If ESYNC* is high, the controlled pins are outputs. If ESYNC* is low, BLANK* is an input. HSYNC and VSYNC are not driven by the CL-GD543X/'4X, and *must* be driven externally to valid input levels. This pin may be connected directly to the corresponding pin on the feature connector. This pin is also an output where it is used to control the shift clock of the optional EEPROM, and should be connected directly to the SK pin.

2.4 Video Interface *(cont.)*

Name	Type	Description
EVIDEO*	I/O	**ENABLE VIDEO*:** This input controls the buffers on P[7:0]. If EVIDEO* is high, P[7:0] are outputs. If EVIDEO* is low, P[7:0] are inputs. This pin may be connected directly to the corresponding pin on the feature connector. This pin is not limited to static operation; it can switch at the DCLK rate. This pin is also an output where it is used to provide data for the optional EEPROM, and should be connected directly to the DI pin. This pin is also an output when color key overlay is enabled.
EDCLK*	I/O	**ENABLE DOT CLOCK*:** This input is used to control the buffer on DCLK. If EDCLK* is high, DCLK is an output. If EDCLK* is low, DCLK is an input. This pin may be connected directly to the corresponding pin on the feature connector.
RED	O	**RED VIDEO:** This analog output supplies current corresponding to the red value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, either the 6-bit value from the LUT or an appropriately-sized true-color value is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to IREF as follows: $If = (63/30) \times IREF$ Each DAC output is typically terminated to monitor ground with a 75-Ω 2% resistor. This resistor, in parallel with the 75-Ω resistor in the monitor, will yield a 37.5-Ω impedance to ground. For a full-scale voltage of 700 mV, full-scale current output should be 18.7 mA, and IREF should be 8.9 mA.
GREEN	O	**GREEN VIDEO:** This analog output supplies current corresponding to the green value of the pixel being displayed. See the description of RED for information regarding the termination of this pin.
BLUE	O	**BLUE VIDEO:** This analog output supplies current corresponding to the blue value of the pixel being displayed. See the description of RED for information regarding the termination of this pin.
IREF	I	**DAC CURRENT REFERENCE:** The current drawn from AVDD through this pin determines the full-scale output of each DAC. This pin should be connected to a constant current source. A recommended circuit is provided in Appendixes B1, B2, and B3 of the *CL-GD543X/'4X Technical Reference Manual.* For products with integrated current reference, this pin should be connected to a capacitor returned to AVSS[3:2]. The capacitor value is not specified at this time, but will be on the order of a few microfarads. See Appendix B8 for additional information.

2.5 Display Memory Interface

Name	Type	Description
RAS1*	O	**ROW ADDRESS STROBE*:** This active-low output is used to latch the row address from MA[9:0] into the DRAMs. This pin must be connected to the RAS* pins of the first bank of DRAMs in the display memory array. For the CL-GD5434, the first bank is the first two Mbytes. For the CL-GD5430, the first bank is the first one Mbyte. These pads, and those for the other DRAM controls, are matched for one to four loads. If eight DRAMs are used, damping resistors may be required to control edge rates and undershoot on these and other control pins. See the DRAM Configuration Appendix B7 in the *CL-GD543X/'4X Technical Reference Manual.*
RAS0*/OE*	O	**ROW ADDRESS STROBE*/OUTPUT ENABLE*:** For the CL-GD543X/'4X, this active-low output can be configured as the RAS0* signal or the OE* signal. This pin must be connected to the RAS* pins of the second bank of DRAMs. For the CL-GD5434, the second bank is the second two Mbytes. For the CL-GD5430, the second bank is the second Mbyte. If CF[10] = 1, this output is configured as OE* and only one bank of DRAM is supported. This output controls the output enable inputs of the DRAMs in the display memory array. See the DRAM Configuration Appendix B7 in the *CL-GD543X/'4X Technical Reference Manual.*
CAS[7:0]*	O	**COLUMN ADDRESS STROBE[7:0]*:** This active-low output is used to latch the Column Address from MA[9:0] into the DRAMs. These pins must be connected to the CAS* pins of all the DRAMs in the display memory array. See the DRAM Configuration Appendix B7 in the *CL-GD543X/'4X Technical Reference Manual.* **NOTE:** If CF[10] = 1 (dual-WE* DRAMs), these pins become WE[7:0]*.
WE*	O	**WRITE ENABLE*:** This active-low output is used to control the Write Enable inputs of the DRAMs. This pin must be connected to the WE* pins of the DRAMs. See DRAM Configuration Appendix B7 in the *CL-GD543X/'4X Technical Reference Manual.* **NOTE:** If CF[10] = 1 (dual-WE* DRAMs), this pin becomes CAS*.
MA[9:0]	O	**MEMORY ADDRESS [9:0]:** These pins control the address inputs of the DRAMs. These pins must be connected to the address pins of the DRAMs. Typically, MA[9] is connected to Address 9, and MA[0] to Address 0 of the DRAMs. See the DRAM Configuration Appendix B7 in the *CL-GD543X/'4X Technical Reference Manual.* **NOTE:** If CF[11] = (asymmetric DRAMs), MA8 is connected to Address 0 and MA0 to Address 8 of the asymmetric DRAMs.

2.5 Display Memory Interface *(cont.)*

Name	Type	Description
MD[63:0]	TS	**MEMORY DATA [63:0]:** These bidirectional pins are used to transfer data between the CL-GD543X/'4X and the display memory. These pins must be connected to the data pins of the DRAMs. See the DRAM Configuration Appendix B7 in the *CL-GD543X/'4X Technical Reference Manual*. MD[63:48] are forced into high-impedance when RESET is active; this allows the configuration pull-down resistors to override the weak pull-ups and be loaded into the Configuration register (CF). MD[7:0] are also used as the BIOSD[7:0] inputs for PCI configuration only.

2.6 Miscellaneous Pins

Name	Type	Description
EECS	O	**EEPROM CHIP SELECT:** This pin is used to control the Chip Select of the optional configuration EEPROM, and should be connected directly to that pin. This pin is also used for DDC2B support. See the description of register SR8 in Chapter 9 of the *CL-GD543X/'4X Technical Reference Manual*.
EEDI	I	**EEPROM DATA IN:** This pin is used to read the data from the optional configuration EEPROM, and should be connected directly to the Data Out pin. This pin is also used for DDC2B support. See the description of register SR8 in Chapter 9 of the *CL-GD543X/'4X Technical Reference Manual*.
EROM*	O	**ENABLE ROM BUFFERS*:** This active-low output is used to control the Output Enable pins of up to two 8-bit bus drivers. These buffers are used to connect the data pins of the BIOS EPROMs to the System Data bus. This output is forced high when RESET is active. This output goes active only for memory read cycles to the Address Range C000:0 through C7FF:F. This output is gated with MEMR* in ISA mode, and is un-latched Local Bus Address decode in local bus modes. For local bus only, this signal is active for I/O Addresses 3C6–3C9 when CF[12] = 0.
OVRW*	O	**OVERLAY WINDOW*:** This signal is active-low. It is intended to be used in applications involving video overlays. For additional connectivity information, see Appendix B14 in the *CL-GD543X/'4X Technical Reference Manual*.
TWR*	I	**TEST LATCH LOAD ENABLE*:** This pin is intended for factory testing and must be pulled up for normal operation. It can be used in board-level testing to disable most of the CL-GD543X/'4X output pins. For additional information, see Appendix B13 in the *CL-GD543X/'4X Technical Reference Manual*.

2.7 Power Pins

Name	Type	Description
VDD[6:1]	Power	**+5V (LOGIC):** These six pins are used to supply +5 volts to the digital logic of the CL-GD543X/'4X. Each pin must be connected to the VCC plane as described in Appendix B12 in the *CL-GD543X/'4X Technical Reference Manual.* Each pin must be bypassed with a 0.1-µF capacitor with proper high-frequency characteristics, as close to the pin as possible.
VSS[13:1]	Ground	**GROUND (LOGIC):** These 13 pins are used to supply ground reference to the digital logic of the CL-GD543X/'4X. Each VSS pin must be connected to the ground plane.
AVDD[1]	Power	**+5V (VCLK):** This pin is used to supply +5 volts to the Video Clock Synthesizer of the CL-GD543X/'4X. This pin must be connected to the VCC rail via a 33-Ω resistor and bypassed to AVSS1 with a 10-µF capacitor.
AVSS[1]	Ground	**GROUND (VCLK):** This pin is used to supply ground reference to the Video Clock Synthesizer of the CL-GD543X/'4X. This pin must be connected to the GND rail.
AVDD[4]	Power	**+5V (MCLK):** This pin is used to supply +5 volts to the Memory Clock Synthesizer of the CL-GD543X/'4X. This pin must be connected to the VCC rail via a 33-Ω resistor and bypassed to AVSS4 with a 10-µF capacitor.
AVSS[4]	Ground	**GROUND (MCLK):** This pin is used to supply ground reference to the Memory Clock Synthesizer of the CL-GD543X/'4X. This pin must be connected to the GND rail.
AVDD[3:2]	Power	**+5V (DAC):** These two pins are used to supply +5 volts to the palette DAC of the CL-GD543X/'4X. Each pin must be connected directly to the VCC plane. Each pin must be bypassed as close to the pin as possible with a 0.1-µF capacitor that has proper high-frequency characteristics.
AVSS[3:2]	Ground	**GROUND (DAC):** These two pins are used to supply ground reference to the palette DAC of the CL-GD543X/'4X. Each pin must be connected to the GND plane. See Appendixes B1, B2, and B3 for various adapter board and motherboard solutions in the *CL-GD543X/'4X Technical Reference Manual.*

3. FUNCTIONAL DESCRIPTION

3.1 General

The CL-GD543X/'4X offers a solution that is totally compatible with the IBM VGA standard. The CL-GD543X/'4X includes all of the necessary hardware for CPU updates to memory, screen refresh, and DRAM refresh. A complete VGA motherboard solution can be implemented by using two 256K × 16 DRAMs with the CL-GD5434 or CL-GD5436, or a single 256K × 16 DRAM with the CL-GD5430 or CL-GD5440.

Figure 3-1 shows the CL-GD543X/'4X connection to the host, display memory, and monitor.

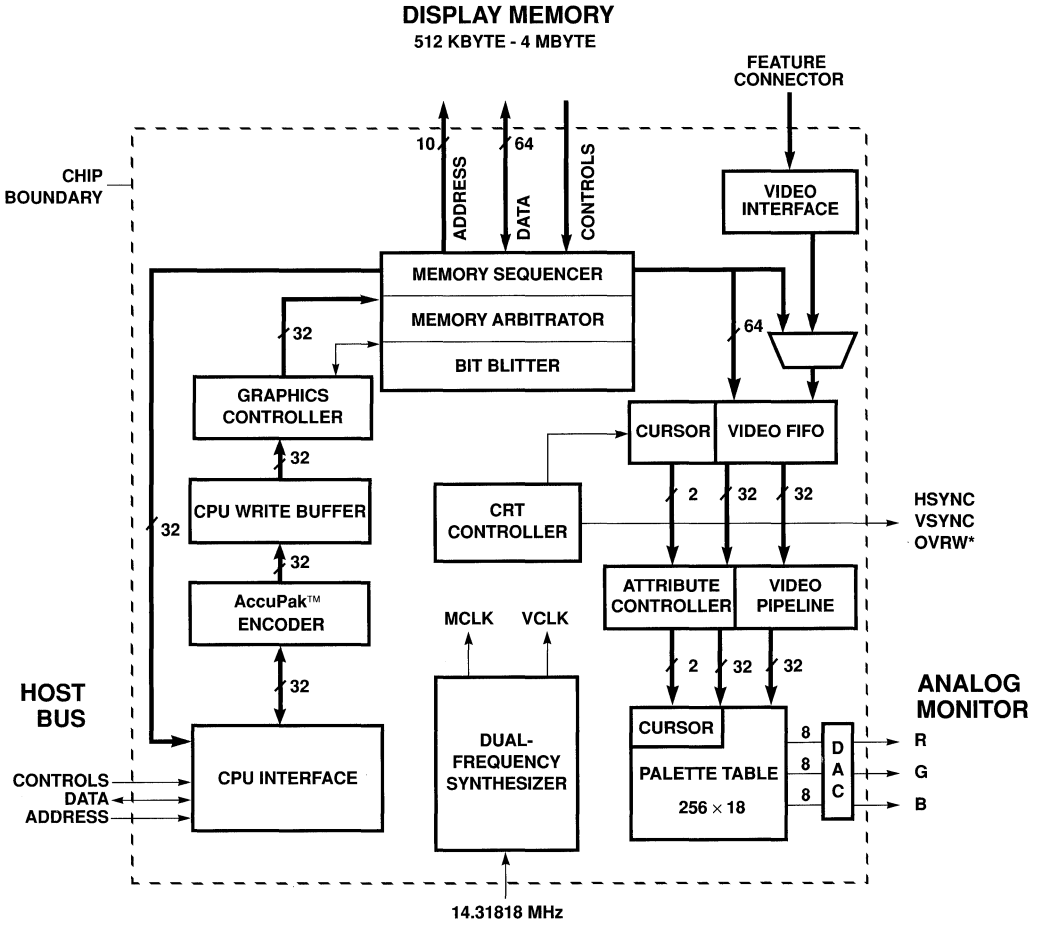


Figure 3-1. CL-GD543X/'4X Chip Block Diagram

3.2 Functional Blocks

The following sections describe functional blocks that are integrated into the CL-GD543X/'4X.

3.2.1 CPU Interface

The CL-GD543X/'4X connects directly to any '486, VESA VL-Bus, or PCI local bus. The CL-GD5434 also connects to the industry-standard ISA bus. No glue logic is required to implement any of these bus interfaces, except for a single inverter for ISA bus. The CL-GD543X/'4X internally decodes a 16- or 24-bit address and responds to the applicable control lines. It executes both I/O accesses and memory accesses as either an 8-, 16-, or 32-bit device.

'486/VESA® VL-Bus™

The CL-GD543X/'4X can interface with '486 microprocessors, and the VESA VL-Bus, at speeds of up to 50 MHz. The CL-GD543X/'4X provides single-clock support, which eliminates additional circuitry for a local bus subsystem design. The CL-GD543X/'4X also supports linear memory addressing to take full advantage of the local bus interface.

PCI Bus

The CL-GD543X/'4X is a highly integrated VGA controller that can interface with the PCI bus directly without any additional logic to support its multiplexed address and data pins. The CL-GD543X/'4X interface executes 32-bit I/O and memory accesses at a speed of up to 33 MHz. The CL-GD543X/'4X also supports memory burst cycles. The CL-GD543X/'4X is fully compliant with the single-load specification of PCI.

ISA Bus (CL-GD5434 only)

The CL-GD5434 supports the 16-bit ISA bus. The CL-GD5434 will execute either 8- or 16-bit I/O and memory accesses, and has a highly-integrated ISA interface so that no additional logic is required except for a single inverter.

3.2.2 CPU Write Buffer

The CL-GD543X/'4X has a multi-level 32-bit CPU write buffer, which dramatically increases GUI acceleration and enhances CPU performance. The CPU write buffer contains a queue of CPU write accesses to display memory that have not been executed because of memory arbitration. Maintaining a queue allows the CL-GD543X/'4X to release the CPU as soon as it has recorded the address and data, and then to execute the operation when display memory cycles are available.

3.2.3 Graphics Controller

The graphics controller is located between the CPU interface and the memory sequencer. It performs text manipulation, data rotation, color mapping, and miscellaneous operations.

3.2.4 BitBLT Engine

The CL-GD543X/'4X has a two-operand BitBLT engine. The BitBLT engine is designed to move data in packed-pixel modes with ROP (raster operations). The ROPs are defined in terms of function and Microsoft equivalents. The BitBLT function is designed to accelerate Microsoft Windows 3.1, Windows NT, Windows95, and OS/2 2.1. Other optional features (for example, color expansion and transparency) enhance the BitBLT function to offer GUI acceleration surpassing other DRAM- or VRAM-based GUI accelerators.

3.2.5 Memory Arbitrator

The memory arbitrator allocates bandwidth to the four functions that compete for the limited bandwidth of display memory: CPU access, screen refresh, DRAM refresh, and BitBLT. DRAM refresh is handled invisibly by allocating a selectable number of CAS*-before-RAS* refresh cycles at the beginning of each scanline. Screen refresh and CPU/BitBLT access are allocated cycles according to the FIFO-control parameters. Priority given is to screen refresh.

3.2.6 Memory Sequencer

The memory sequencer generates timing for display memory. This includes RAS*, CAS*, and multiplexed-address timing, as well as WE* timing. The Sequencer generates CAS*-before-RAS* refresh cycles, Random Read and Random Early Write cycles, and Fast-page mode Read and Early Write cycles. The memory sequencer generates multiple CAS* or WE* signals according to the memory type used. EDO (extended data output) DRAMs are supported.

3.2.7 CRT Controller

The CRT controller generates the HSYNC and VSYNC signals required for the monitor, as well as BLANK* signals required by the palette DAC. The CL-GD5434/'36 support both horizontal and vertical GENLOCK. The CL-GD5440 supports a hardware video window.

3.2.8 Video FIFO

The video FIFO allows the memory sequencer to execute display memory accesses needed for screen refresh at maximum memory speed rather than at the screen refresh rate. This makes it possible to collect the accesses for screen refresh near the beginning of the scanline, and to execute them in Fast-page mode rather than Random-read mode. The CL-GD5440 has two video FIFOs for video playback.

3.2.9 Attribute Controller

The attribute controller formats the display for the screen. Display color selection, text blinking, and underlining are performed by the attribute controller. Alternate font selection also occurs in the attribute controller.

3.2.10 Video Pipeline (CL-GD5440)

The CL-GD5440 video pipeline performs format conversion, interpolated X and Y zooming, and color space conversion for a rectangular region of the display called the 'video window'.

3.2.11 Palette DAC

The palette DAC block contains the color palette and three 8-bit digital-to-analog converters. The color palette, with 256 18-bit entries, converts a color code that specifies the color of a pixel into three 6-bit values, one each for red, green, and blue. Alternatively, the CL-GD543X/'4X can be configured for 15-, 16-, or 24-bit pixels. This allows 32K, 64K, or 16M simultaneous colors to be displayed on the screen. The 24 bits are allocated as 8-8-8 for 16M colors, 5-6-5 for 64K Color mode, or 5 to each (red, green, and blue) DAC for 32K Color mode. The CL-GD5440 also supports YCrCb and AccuPak formats.

The CL-GD5434 has a 32-bit data path width which supports direct 24/32-bit-per-pixel clock modes. The high byte of the 32-bit pixel (the 'alpha' byte) can be used for 'color key' overlay control. Refer to Appendix B14 in the *CL-GD543X/'4X Technical Reference Manual* for more detailed information. The CL-GD5436 supports Packed-24 modes for increased true color performance.

The palette DAC supports Power-down mode which temporarily turns the palette DAC off to conserve power.

3.2.12 Dual-Frequency Synthesizer

The dual-frequency synthesizer generates the memory sequencer and video display clocks from a single reference frequency. The frequency of each clock is independently programmable. The maximum memory sequencer clock and video display clock is listed on page 3-1. The reference frequency of 14.31818 MHz must be supplied from an external TTL source.

3.2.13 VESA®/VGA Pass-through Connector

The CL-GD543X/'4X is designed to connect directly to a VESA connector. The device supports the three enable/disable inputs; the Pixel bus can drive the connector directly. Through this connector, the overlay feature can be used in multimedia applications. This allows for internal DAC utilization in 16-bit-per-pixel mode. The CL-GD5430/'40 supports VAFC Baseline input and output. The CL-GD5436 supports direct 16-bit input when configured for the PCI bus.

3.3 Functional Operation

The following sections discuss the four major operations handled by the CL-GD543X/'4X.

CPU Access to Registers

The host can be any processor controlling any '486-based local bus architecture (for example, VESA VL-Bus or PCI interfaces). The host accesses CL-GD543X/'4X registers by setting up 16- or 24-bit addresses and making the appropriate controls active. The CL-GD543X/'4X can respond as either an 8- or 16-bit peripheral, depending on how it has been configured in the system.

DRAM and screen refresh occur concurrently with, and independently of, register access (unless the host is changing display parameters or has suppressed refresh). These registers are described in the *CL-GD543X/'4X Technical Reference Manual.*

CPU Access to Display Memory

The CL-GD543X/'4X can manage all host accesses to display memory. The host first sets up certain parameters (for example, color and write masks) then generates a memory access in the range where the CL-GD543X/'4X is programmed to respond. The CL-GD543X/'4X will transfer 32-bit-wide data for any of the local bus interfaces. The CL-GD5434 will transfer 16-bit-wide data for the ISA bus.

Display Memory Refresh

The CL-GD543X/'4X automatically generates a selectable number of CAS*-before-RAS* refresh cycles during each horizontal timing period.

Screen Refresh

The CRT monitor requires near-constant rewriting since its only memory is the phosphor persistence. The CL-GD543X/'4X fetches information from display memory for each scanline as quickly as possible, using Fast-page mode cycles to fill the video FIFO. This allows the maximum possible time for the host and BitBLT engine to access display memory.

3.4 Performance

The CL-GD543X/'4X is designed with the following performance-enhancing features:

- 64-bit display memory data bus for faster access to display memory (CL-GD5430/'40 has an effective 32-bit display memory data bus)
- Memory-mapped 32-bit BitBLT registers
- DRAM Fast-page mode operations for faster access to display memory
- Zero-wait-state performance and a CPU write buffer that allows faster CPU access for writes to display memory
- Accelerated Microsoft® Windows® with BitBLT
- Increased throughput with '486/VESA® local bus interface
- Increased throughput with PCI local bus interface with Burst mode
- 32-bit CPU interface to display memory for faster host access in all modes, including Planar mode
- 16- or 32-bit CPU interface to I/O registers for faster host access
- Multi-level, 32-bit system memory write cache
- 32-bit internal data inputs for internal DAC
- Video FIFO to minimize memory contention
- 32 × 32 and 64 × 64 hardware cursor to improve Microsoft® Windows® performance

3.5 Compatibility

The CL-GD543X/'4X includes all registers and data paths required for VGA controllers, and is upward-compatible with the CL-GD542X family.

The CL-GD543X/'4X supports extensions to VGA, including 1024 × 768 × 16M interlaced, 1024 × 768 × 64K interlaced and non-interlaced, and 1280 × 1024 × 256 interlaced and non-interlaced modes. Additionally, various 132-column text modes are supported.

3.6 Board Testability

The CL-GD543X/'4X chip is testable, even when installed on a printed circuit board. By using Pin-Scan testing, any IC signal pin not connected to the board or shorted to a neighboring pin or trace, will be detected. The signature generator allows the entire system, including the display memory, to be tested at speed.

4. CONFIGURATION TABLES

4.1 Video Modes

Table 4-1. IBM Standard VGA Video Modes

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
0, 1	0, 1	16/256K	40 × 25	9 × 16	360 × 400	Text	14	31.5	70
2, 3	2, 3	16/256K	80 × 25	9 × 16	720 × 400	Text	28	31.5	70
4, 5	4, 5	4/256K	40 × 25	8 × 8	320 × 200	Graphics	12.5	31.5	70
6	6	2/256K	80 × 25	8 × 8	640 × 200	Graphics	25	31.5	70
7	7	Monochrome	80 × 25	9 × 16	720 × 400	Text	28	31.5	70
D	D	16/256K	40 × 25	8 × 8	320 × 200	Graphics	12.5	31.5	70
E	E	16/256K	80 × 25	8 × 14	640 × 200	Graphics	25	31.5	70
F	F	Monochrome	80 × 25	8 × 14	640 × 350	Graphics	25	31.5	70
10	10	16/256K	80 × 25	8 × 14	640 × 350	Graphics	25	31.5	70
11	11	2/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
11+	11	2/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.9	72
11+	11	2/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.5	75
12	12	16/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
12+	12+	16/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.9	72
12+	12+	16/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.5	75
13	13	256/256K	40 × 25	8 × 8	320 × 200	Graphics	12.5	31.5	70

NOTE: The EGA-compatible text modes (which use an 8 × 14 font) and graphics modes 10 and F use a 16-dot high font, with the bottom two lines truncated, in the absence of TSRFONT (8 × 14 font TSR). This creates some errors when displaying characters with descenders, but does not restrict operation of programs using these modes. In text modes using the 8 × 14 font, the characters 'g', 'j', 'p', 'q', 'y', and 'ÿ' are truncated using a middle- and bottom-line algorithm to avoid truncation of descenders. For compatibility with some DOS applications using the 8 × 14 font, the TSRFONT utility should be used. Applications such as DOSSHELL in Graphics 25 or 34 line display modes require the TSRFONT utility be loaded.

Table 4-2. Cirrus Logic Extended Video Modes

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
14	–	16/256K	132 × 25	8 × 16	1056 × 400	Text	41.5	31.5	70
54	10A	16/256K	132 × 43	8 × 8	1056 × 350	Text	41.5	31.5	70
55	109	16/256K	132 × 25	8 × 14	1056 × 350	Text	41.5	31.5	70
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	36	35.2	56
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	40	37.8	60
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	50	48.1	72
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	49.5	46.9	75
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	36	35.2	56
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	40	37.9	60
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	50	48.1	72
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	49.5	46.9	75
5D†	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	44.9	35.5	43i†
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	65	48.3	60
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	75	56	70
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	77	58	72
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	78.7	60	75
5E	100	256/256K	80 × 25	8 × 16	640 × 400	Graphics	25	31.5	70
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.9	72
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.5	75
60†	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	44.9	35.5	43i†
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	65	48.3	60
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	75	56	70
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	77	58	72
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	78.7	60	75
64	111	64K	–	–	640 × 480	Graphics	25	31.5	60
64	111	64K	–	–	640 × 480	Graphics	31.5	37.9	72
64	111	64K	–	–	640 × 480	Graphics	31.5	37.5	75
65	114	64K	–	–	800 × 600	Graphics	36	35.2	56

Table 4-2. Cirrus Logic Extended Video Modes *(cont.)*

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
65	114	64K	–	–	800 × 600	Graphics	40	37.8	60
65	114	64K	–	–	800 × 600	Graphics	50	48.1	72
65	114	64K	–	–	800 × 600	Graphics	49.5	46.9	75
66	110	32K‡	–	–	640 × 480	Graphics	25	31.5	60
66	110	32K‡	–	–	640 × 480	Graphics	31.5	37.9	72
66	110	32K‡	–	–	640 × 480	Graphics	31.5	37.5	75
67	113	32K‡	–	–	800 × 600	Graphics	36	35.2	56
67	113	32K‡	–	–	800 × 600	Graphics	40	37.8	60
67	113	32K‡	–	–	800 × 600	Graphics	50	48.1	72
67	113	32K‡	–	–	800 × 600	Graphics	49.5	46.9	75
68†	116	32K‡	–	–	1024 × 768	Graphics	44.9	35.5	43i†
68	116	32K‡	–	–	1024 × 768	Graphics	65	48.3	60
68	116	32K‡	–	–	1024 × 768	Graphics	75	56	70
68	116	32K‡	–	–	1024 × 768	Graphics	78.7	60	75
69†	119	32K‡	–	–	1280 × 1024	Graphics	75	48	43i†
6C†	106	16/256K	160 × 64	8 × 16	1280 × 1024	Graphics	75	48	43i†
6D†	107	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	75	48	43i†
6D	107	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	108	65	60
6D	107	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	126	76	71.2
6D	107	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	135	80	75
71	112	16M	–	–	640 × 480	Graphics	25	31.5	60
71	112	16M	–	–	640 × 480	Graphics	31.5	37.9	72
71	112	16M	–	–	640 × 480	Graphics	31.5	37.5	75
72↕	–	16M + A	–	–	800 × 600	Graphics	36	35.2	56
72↕	–	16M + A	–	–	800 × 600	Graphics	40	37.8	60
73↕	–	16M + A	–	–	1024 × 768	Graphics	44.9	35.5	43i†
74†	117	64K	–	–	1024 × 768	Graphics	44.9	35.5	43i†
74	117	64K	–	–	1024 × 768	Graphics	65	48.3	60
74	117	64K	–	–	1024 × 768	Graphics	75	56	70

Table 4-2. Cirrus Logic Extended Video Modes *(cont.)*

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
74	117	64K	–	–	1024 × 768	Graphics	78.7	60	75
75†	11A	64K	–	–	1280 × 1024	Graphics	75	48	43i†
76‡	–	16M + A	–	–	640 × 480	Graphics	25	31.5	60
76‡	–	16M + A	–	–	640 × 480	Graphics	31.5	37.9	72
76‡	–	16M + A	–	–	640 × 480	Graphics	31.5	37.5	75
78	115	16M	–	–	800 × 600	Graphics	36	35.2	56
78	115	16M	–	–	800 × 600	Graphics	40	37.8	60
78	115	16M	–	–	800 × 600	Graphics	50	48.1	72
78	115	16M	–	–	800 × 600	Graphics	49.5	46.9	75
79	118	16M	–	–	1024 × 768	Graphics	44.9	35.5	43i†
79	118	16M	–	–	1024 × 768	Graphics	65	48.3	60
79	118	16M	–	–	1024 × 768	Graphics	75	56	70
79	118	16M	–	–	1024 × 768	Graphics	78.7	60	75

NOTES:

1) '‡' character indicates 32K Direct-Color/256-color Mixed mode.
2) †' character indicates Interlaced mode.
3) '↕' character indicates 16M colors, but with 32-bit-per-pixel format.
4) '16M + A' indicates 16M colors + Alpha channel
5) Some modes and some refresh rates are not supported by all CL-GD543X/'4X controllers. Refer to the CL-GD543X Software Release Kit for the list of video modes supported by the CL-GD543X/'4X BIOS. Also see the Inside Front Cover of the *CL-GD543X/'4X Technical Reference Manual.*
6) Some modes are not supported by all monitors. The fastest vertical refresh rate for the monitor type selected will be automatically used.
7) An 8 × 14 font for mode 55h may be provided with a DOS TSR. If the TSR has not been loaded when the mode is set, the 8 × 16 font will be used with the two bottom rows deleted. This causes truncation of characters with descenders, but does not restrict program operation nor does it make characters particularly difficult to read. For absolute compatibility with some DOS applications which use the 8 × 14 font, the TSR should be used.

4.2 Configuration Register, CF

When RESET (system power-on reset) goes active, the CL-GD543X/'4X samples the levels on several of the Display Memory Data (MD[63:48]) pins. These levels are latched into a write-only Configuration register (CF1). This register specifies the configuration of the CL-GD543X/'4X.

The levels on the Memory Data bus default to a logic '1' during power-on reset because of internal 250-kΩ pull-up resistors. A logic '0' is achieved by installing an external 6.8-kΩ pull-down resistor on the memory data line corresponding to the appropriate bit in the Configuration register. Refer to Appendix B9 in the *CL-GD543X /'4XTechnical Reference Manual*. Table 4-3 summarizes the Configuration register. The bits are described in detail in Appendix B9.

Table 4-3. Configuration Register Bits

CF Bits	Level	Description	Memory Data Bit	Pin Number
15	0 1	Enable Pin-Scan test Disable Pin-Scan test	MD63	157
14	0 1	PCI3C[8] = 1 (CL-GD5436/'40 only) PCI3C[8] = 0 (CL-GD5436/'40 only)	MD62	158
13	0 1	3c3[0] reset state = 0 (CL-GD5436 only) 3c3[0] reset state = 1 (CL-GD5436 only)	MD61	159
12	0 1 0 1	Source VCLK on MCLK (CL-GD5430/'36/'40 only) Source MCLK on MCLK (CL-GD5430/'36/'40 only) Disable internal DAC (CL-GD5434 only) Enable internal DAC (CL-GD5434 only	MD60	160
11	0 1	Asymmetric DRAM (RAS*/CAS* addressing) Symmetric DRAM (RAS*/CAS* addressing)	MD59	161
10	0 1	Multiple-CAS*, single-WE* Multiple-WE*, single-CAS*	MD58	162
9	0 1	7-MCLK RAS* cycle 6-MCLK RAS* cycle	MD57	163
8	0 1 0 1	50.11363-MHz MCLK default (except CL-GD5436) 41.16477-MHz MCLK default (except CL-GD5436) Enable byte swapping (PCI configured CL-GD5436 only) Disable byte swapping (PCI configured CL-GD5436 only)	MD56	164
7	0 1	64K ROM BIOS @ C0000h–CFFFFh 32K ROM BIOS @ C0000h–C7FFFh	MD55	170
6	0 1 0 1	16-bit BIOS ROM (ISA bus configuration) 8-bit BIOS ROM (ISA bus configuration) Zero-wait Write not supported (VESA VL-Bus configuration) Zero-wait Write supported (VESA VL-Bus configuration)	MD54	171
5	0 1	External MCLK (pin 16 is an input) Internal MCLK (pin 16 is an output)	MD53	172
4	0 1	I/O port 94h enables POS 102 access (video enable) I/O port 3C3h used for video enable	MD52	173
3	0 1	Port 3C3h is Video System Sleep register Port 46E8h is Video System Sleep register	MD51	174
2, 1, 0	000 001 010 011 100 110 111	Reserved Reserved VESA VL-Bus or '486 (> 33 MHz) Reserved PCI bus VESA® VL-Bus™ or '486 (≤ 33 MHz) ISA bus (CL-GD5434 only)	MD50, MD49, MD48	141, 142, 143

4.3 Host Interface Signals

With the pin connections listed in Table 4-4, the CL-GD543X/'4X will interface directly to an ISA or local bus.

Table 4-4. Bus Connections

CL-GD543X/'4X Pin	ISA Bus (CL-GD5434 only)	VESA® VL-Bus™	PCI Bus
50	LA23	HIMEM	PAR
48	LA22	LOWMEM	STOP#
[45..44]	LA[21:20]	A[21:20]	(unused)
[42..40]	LA[19:17]	A[19:17]	BIOSA[15:13]
39	SA[16]	A[16]	(unused)
38	SA[15]	A[15]	(unused)
37	SA[14]	A[14]	BIOSA12
[36..34], [32..24]	SA[13:2]	A[13:2]	BIOSA[11:0]
23	SA1	BE3#	C/BE#3
22	SA0	BE2#	C/BE#2
[54..63], [68..70]	(unused)	D[31:19]	AD[31:19]
71	MEMW*	D18	AD18
72	IOCS16*	D17	AD17
73	IRQ	D16	AD16
[74..76], [78..82], [84..85], [87..92]	SD[15:0]	D[15:0]	AD[15:0]
21	SBHE*	BE1#	C/BE#1
20	REFRESH*	BE0#	C/BE#0
46	BALE	ADS#	FRAME#
47	AEN	RDYRTN#	IRDY#
53	IOR*	W/R#	IDSEL
43	IOW*	LCLK	CLK
66	MEMR*	M/IO#	(unused)
51	RESET	RESET	RST
49	IOCHRDY	LRDY#	TRDY#
65	MCS16*	LDEV#	DEVSEL#
19	0WS	INTR	INTR
17	OSC	OSC	OSC
33	EROM*	EROM*	EROM*

NOTES:

1) For ISA bus applications, note that SA[19:17] are not found on the CL-GD5434; this means that an adapter board will only function in a 16-bit slot.

2) The OSC and EROM* pins are common in all configurations.

5. VGA REGISTER PORT MAP

Table 5-1. VGA Register Port Map

Address	Port
94	POS 102 Access Control (3C3 sleep)
102	POS102 register
3B4	CRT Controller Index (R/W — monochrome)
3B5	CRT Controller Data (R/W — monochrome)
3BA	Feature Control (W), Input Status register 1 (R — monochrome)
3C0	Attribute Controller Index/Data (Write)
3C1	Attribute Controller Index/Data (Read)
3C2	Miscellaneous Output (W), Input Status register 0 (R)
3C3	Motherboard Sleep
3C4	Sequencer Index (R/W)
3C5	Sequencer Data (R/W)
3C6	Video DAC Pixel Mask (R/W), Hidden DAC register (R/W)
3C7	Pixel Address Read Mode (W), DAC State (R)
3C8	Pixel Mask Write Mode (R/W)
3C9	Pixel Data (R/W)
3CA	Feature Control Readback (R)
3CC	Miscellaneous Output Readback (R)
3CE	Graphics Controller Index (R/W)
3CF	Graphics Controller Data (R/W)
3D4	CRT Controller Index (R/W — color)
3D5	CRT Controller Data (R/W — color)
3DA	Feature Control (W), Input Status register 1 (R — color)
46E8	Adapter Sleep

6. CL-GD543X/'4X REGISTERS

External/General Registers

Abbreviation	Register Name	Index	Port
POS94	POS102 Access Control	–	94
POS102	POS102	–	102
VSSM	Motherboard Sleep	–	3C3
VSSM	Adapter Sleep	–	46E8
MISC	Miscellaneous Output	–	3C2 (Write)
MISC	Miscellaneous Output	–	3CC (Read)
FC	Feature Control	–	3?A (Write)
FC	Feature Control	–	3CA (Read)
FEAT	Input Status Register 0	–	3C2 (Read)
STAT	Input Status Register 1	–	3?A
3C6	Pixel Mask	–	3C6
3C7	Pixel Address Read Mode	–	3C7 (Write)
3C7	DAC State	–	3C7 (Read)
3C8	Pixel Address Write Mode	–	3C8
3C9	Pixel Data	–	3C9
PCI00	PCI Device/Vendor ID	–	00
PCI04	PCI Command	–	04 (Write)
PCI04	PCI Status	–	04 (Read)
PCI08	PCI Class Code	–	08 (Read)
PCI10	PCI Display Memory Base Address	–	10
PCI14	PCI Relocatable I/O Base Address	–	14
PCI30	PCI ROM Base Address Enable	–	30
PCI3C	PCI Interrupt Line/ Interrupt Pin	–	3C

NOTE: '?' in the above address is 'B' in Monochrome mode and 'D' in Color mode.

VGA Sequencer Registers

Abbreviation	Register Name	Index	Port
SRX	Sequencer Index	–	3C4
SR0	Reset	0	3C5
SR1	Clocking Mode	1	3C5
SR2	Plane Mask	2	3C5
SR3	Character Map Select	3	3C5
SR4	Memory Mode	4	3C5

6. CL-GD543X/'4X REGISTERS *(cont.)*

CRT Controller Registers

Abbreviation	Register Name	Index	Port
CRX	CRTC Index	–	3?4
CR0	Horizontal Total	0	3?5
CR1	Horizontal Display End	1	3?5
CR2	Horizontal Blanking Start	2	3?5
CR3	Horizontal Blanking End	3	3?5
CR4	Horizontal Sync Start	4	3?5
CR5	Horizontal Sync End	5	3?5
CR6	Vertical Total	6	3?5
CR7	Overflow	7	3?5
CR8	Screen A Preset Row Scan	8	3?5
CR9	Character Cell Height	9	3?5
CRA	Text Cursor Start	A	3?5
CRB	Text Cursor End	B	3?5
CRC	Screen Start Address High	C	3?5
CRD	Screen Start Address Low	D	3?5
CRE	Text Cursor Location High	E	3?5
CRF	Text Cursor Location Low	F	3?5
CR10	Vertical Sync Start	10	3?5
CR11	Vertical Sync End	11	3?5
CR12	Vertical Display End	12	3?5
CR13	Offset	13	3?5
CR14	Underline Row Scan	14	3?5
CR15	Vertical Blanking Start	15	3?5
CR16	Vertical Blanking End	16	3?5
CR17	Mode Control	17	3?5
CR18	Line Compare	18	3?5
CR22	Graphics Data Latches Readback	22	3?5
CR24	Attribute Controller Toggle Readback	24	3?5
CR26	Attribute Controller Index Readback	26	3?5

NOTE: '?' in the above address is 'B' in Monochrome mode and 'D' in Color mode.

VGA Graphics Controller Registers

Abbreviation	Register Name	Index	Port
GRX	Graphics Controller Index	–	3CE
GR0	Set/Reset	0	3CF
GR1	Set/Reset Enable	1	3CF
GR2	Color Compare	2	3CF
GR3	Data Rotate	3	3CF
GR4	Read Map Select	4	3CF
GR5	Mode	5	3CF
GR6	Miscellaneous	6	3CF
GR7	Color Don't Care	7	3CF
GR8	Bit Mask	8	3CF

6. CL-GD543X/'4X REGISTERS *(cont.)*

VGA Attribute Controller Registers

Abbreviation	Register Name	Index	Port
ARX	Attribute Controller Index	–	3C0/3C1
AR0-ARF	Attribute Controller Palette	0:F	3C0/3C1
AR10	Attribute Controller Mode	10	3C0/3C1
AR11	Overscan (Border) Color	11	3C0/3C1
AR12	Color Plane Enable	12	3C0/3C1
AR13	Pixel Panning	13	3C0/3C1
AR14	Color Select	14	3C0/3C1

Extended Sequencer Registers

Abbreviation	Register Name	Index	Port
SR2	Enable Writing Pixel Extension	2	3C5
SR6	Unlock ALL Extensions	6	3C5
SR7	Extended Sequencer Mode	7	3C5
SR8	EEPROM Control	8	3C5
SR9	Scratch-Pad 0	9	3C5
SRA	Scratch-Pad 1	A	3C5
SRB	VCLK0 Numerator	B	3C5
SRC	VCLK1 Numerator	C	3C5
SRD	VCLK2 Numerator	D	3C5
SRE	VCLK3 Numerator	E	3C5
SRF	DRAM Control	F	3C5
SR10	Graphics Cursor X Position	10	3C5
SR11	Graphics Cursor Y Position	11	3C5
SR12	Graphics Cursor Attributes	12	3C5
SR13	Graphics Cursor Pattern Address Offset	13	3C5
SR14	Scratch-Pad 2	14	3C5
SR15	Scratch-Pad 3	15	3C5
SR16	Performance Tuning	16	3C5
SR17	Configuration Read Back and Extended Control	17	3C5
SR18	Signature Generator Control	18	3C5
SR19	Signature Generator Result Low Byte	19	3C5
SR1A	Signature Generator Result High Byte	1A	3C5
SR1B	VCLK0 Denominator and Post-Scalar Value	1B	3C5
SR1C	VCLK1 Denominator and Post-Scalar Value	1C	3C5
SR1D	VCLK2 Denominator and Post-Scalar Value	1D	3C5
SR1E	VCLK3 Denominator and Post-Scalar Value	1E	3C5
SR1F	MCLK Select	1F	3C5

6. CL-GD543X/'4X REGISTERS *(cont.)*

Extended Graphics Controller Registers

Abbreviation	Register Name	Index	Port
GR0	Write Mode 5 Background Extension	0	3CF
GR1	Write Mode 4, 5 Foreground Extension	1	3CF
GR9	Offset Register 0	9	3CF
GRA	Offset Register 1	A	3CF
GRB	Graphics Controller Mode Extensions	B	3CF
GRC	Color Key	C	3CF
GRD	Color Key Mask	D	3CF
GRE	Miscellaneous Control	E	3CF
GR10	Background Color Byte 1	10	3CF
GR11	Foreground Color Byte 1	11	3CF

BitBLT Registers

Abbreviation	Register Name	Index	Port
GR12	Background Color Byte 2 *(CL-GD5434 only)*	12	3CF
GR13	Foreground Color Byte 2 *(CL-GD5434 only)*	13	3CF
GR14	Background Color Byte 3 *(CL-GD5434 only)*	14	3CF
GR15	Foreground Color Byte 3 *(CL-GD5434 only)*	15	3CF
GR20	BLT Width Byte 0	20	3CF
GR21	BLT Width Byte 1	21	3CF
GR22	BLT Height Byte 0	22	3CF
GR23	BLT Height Byte 1	23	3CF
GR24	BLT Destination Pitch Byte 0	24	3CF
GR25	BLT Destination Pitch Byte 1	25	3CF
GR26	BLT Source Pitch Byte 0	26	3CF
GR27	BLT Source Pitch Byte 1	27	3CF
GR28	BLT Destination Start Byte 0	28	3CF
GR29	BLT Destination Start Byte 1	29	3CF
GR2A	BLT Destination Start Byte 2	2A	3CF
GR2B	Reserved	2B	3CF
GR2C	BLT Source Start Byte 0	2C	3CF
GR2D	BLT Source Start Byte 1	2D	3CF
GR2E	BLT Source Start Byte 2	2E	3CF
GR2F	BLT Destination Write Mask *(CL-GD5430 only)*	2F	3CF
GR30	BLT Mode	30	3CF
GR31	BLT Start/Status	31	3CF
GR32	BLT Raster Operation	32	3CF
GR33	BLT Mode Extensions	33	3CF

6. CL-GD543X/'4X REGISTERS *(cont.)*

Extended CRTC Registers

Abbreviation	Register Name	Index	Port
CR19	Interlace End	19	3?5
CR1A	Miscellaneous Control	1A	3?5
CR1B	Extended Display Controls	1B	3?5
CR1C	Sync Adjust and GENLOCK *(CL-GD5434 only)*	1C	3?5
CR1D	Overlay Extended Control	1D	3?5
CR25	Part Status	25	3?5
CR27	ID	27	3?5
CR28	CL-GD5430 Class ID	28	3?5
HDR	Hidden DAC	–	3C6

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

Extended CDX Registers (CL-GD5440 only)

Abbreviation	Register Name	Index	Port
CR1F	Video Capture and Video Port Configuration	1F	3?5
CR31	Video Window Horizontal Zoom Control	31	3?5
CR32	Video Window Vertical Zoom Control	32	3?5
CR33	Video Window Horizontal Region 1 Size	33	3?5
CR34	Video Window Horizontal Region 2 Active Size	34	3?5
CR35	Video Window Horizontal Region 2 Skip Size	35	3?5
CR36	Video Window Horizontal Overflow	36	3?5
CR37	Video Window Vertical Start	37	3?5
CR38	Video Window Vertical End	38	3?5
CR39	Video Window Vertical Overflow	39	3?5
CR3A	Video Window Start Address Byte 0	3A	3?5
CR3B	Video Window Start Address Byte 1	3B	3?5
CR3C	Video Window Start Address Byte 2	3C	3?5
CR3D	Video Window Address Offset	3D	3?5
CR3E	Video Window Master Control	3E	3?5
CR3F	Host Video Data Path Control	3F	3?5

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Ambient temperature under bias ..... 0° to 70° C

Storage temperature ..... -65° to 150° C

Voltage on any pin ..... V_{SS} -0.5 V to V_{CC} + 0.5 V

Operating power dissipation ..... 2.0 watts

Power supply voltage ..... 7 volts

Injection current (latch-up testing) ..... 100 mA

CAUTION: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

7.2 DC Specifications (Digital)

(V_{CC} = 5 V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
V_{CC}	Power Supply Voltage	4.75	5.25	Volts	Normal Operation	
V_{IL}	Input Low Voltage	0	0.8	Volts		
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	Volts		
V_{OL}	Output Low Voltage		0.5	Volts	I_{OL} = 4 mA	1
V_{OH}	Output High Voltage	2.4		Volts	I_{OH} = 400 µA	2
I_{CC}	Supply Current				V_{CC} = Nominal	3
I_{IH}	Input High Current		10	µA	$V_{IN} = V_{CC}$	
I_{IL}	Input Low Current	–10		µA	V_{CC} = 5.25, V_{IN} = 0	
I_{IHP}	Input High Current (Pull-up)	–10	10	µA	$V_{IN} = V_{CC}$	
I_{ILP}	Input Low Current (Pull-up)	–45	–12	µA	V_{CC} = 5.25, V_{IN} = 0	
I_{OZ}	Input Leakage	–10	10	µA	$0 < V_{IN} < V_{CC}$	
C_{IN}	Input Capacitance		10	pF		4
C_{OUT}	Output Capacitance		10	pF		4

NOTES:

1) I_{OL} is specified for a standard buffer. See Section 1.4, Pin Summary, for further information.
2) I_{OH} is specified for a standard buffer. See Section 1.4, Pin Summary, for further information.
3) I_{CC} is measured with VCLK and MCLK as indicated in the table below:

Device	VCLK	MCLK	I_{CC} (mA)
CL-GD5430	78 MHz	60 MHz	327
CL-GD5434	108 MHz	50 MHz	296
CL-GD5436	135 MHz	80 MHz	tbd
CL-GD5440	78 MHz	60 MHz	tbd

4) This is not 100% tested, but is periodically sampled.

7.3 DC Specifications (Palette DAC)

(V_{CC} = 5 V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
A_{VDD}	DAC Supply Voltage	4.75	5.25	Volts	Normal Operation	
I_{REF}	DAC Reference Current	–3	–10	mA		1

NOTE: 1)The nominal I_{REF} is 8.9 mA. See Appendix B8 for products with integrated I_{REF}.

7.4 DC Specifications (Frequency Synthesizer)

(V_{CC} = 5 V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
A_{VDD}	Synthesizer Supply Voltage	4.75	5.25	Volts		

7.5 DAC Characteristics

(V_{CC} = 5 V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter		MAX	Units	Test Conditions	Note
R	Resolution		8	Bits		
IO	Output Current		30	mA	VO < 1V	
TR	Analog Output Rise/Fall Time		8	ns		2, 3, 4
TS	Analog Output Settling Time		15	ns		2, 3, 5
TSK	Analog Output Skew		tbd	ns		2, 3, 6
FDT	DAC-to-DAC Correlation		2.5	%		6, 7
GI	Glitch Impulse	Typical		pV–sec.		2, 3, 6
IL	Integral Linearity		1.5	LSB		
DL	Differential Linearity		1.5	LSB		2

NOTES:
2) Load is 50 ohms and 30 pF per analog output.
3) I_{REF} = –6.67 mA.
4) TR is measured from 10% to 90% full-scale.
5) TS is measured from 50% of full-scale transition to output remaining within 2% of final value.
6) Outputs loaded identically.
7) About the mid-point of the distribution of the three DACs measured at full-scale output.
8) 'tbd' means 'to be determined'.

7.6 List of Waveforms

Table 7-1. I/O Write Timing (ISA Bus — CL-GD5434 only)[a]

Symbol	Parameter	MIN	MAX	Units
t_1	Address, SBHE* setup to IOW* active	5	–	ns
t_2	IOW* pulse width	40	–	ns
t_3	Data setup to IOW* inactive	5	–	ns
t_4	Data hold from IOW* inactive	0	–	ns
t_5	Address, SBHE* hold from IOW* inactive	0	–	ns
t_6	IOW* inactive to any command active	80	–	ns

[a] AEN must be inactive

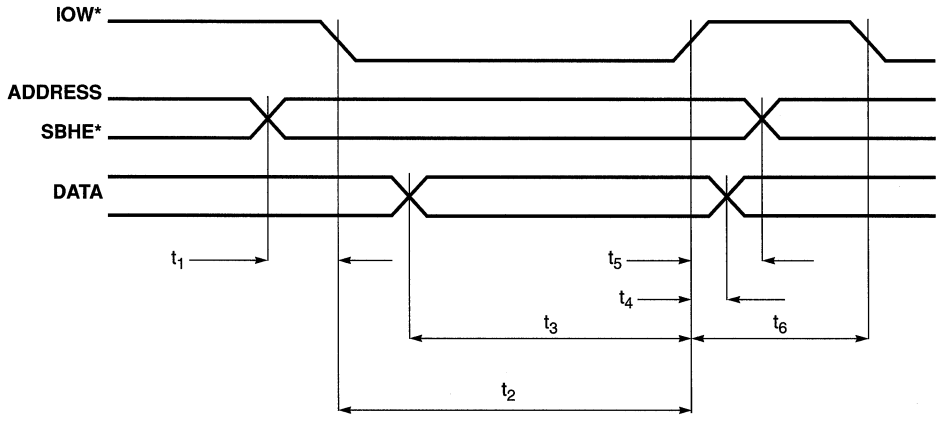


Figure 7-1. I/O Write Timing (ISA Bus — CL-GD5434 only)

Table 7-2. I/O Read Timing (ISA Bus — CL-GD5434 only)[a]

Symbol	Parameter	MIN	MAX	Units
t_1	Address, SBHE* setup to IOR* active	5	–	ns
t_2	IOR* active to low-impedance delay	0	–	ns
t_3	Data delay from IOR* active	–	60	ns
t_4	IOR* pulse width	70	–	ns
t_5	Data hold from IOR* inactive	0	20	ns
t_6	Address, SBHE* hold from IOR* inactive	0	–	ns
t_7	IOR* inactive to high-impedance delay	0	20	ns

[a] AEN must be inactive

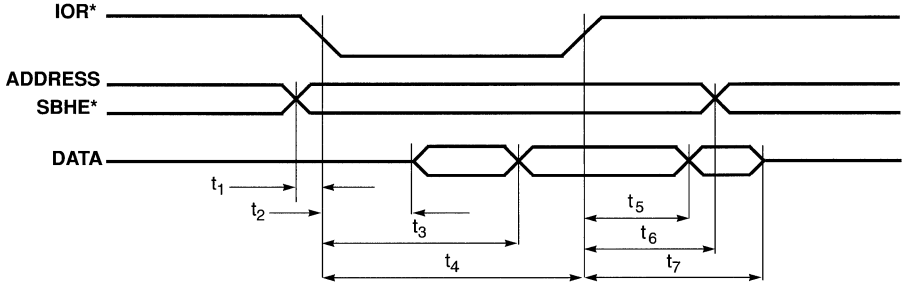


Figure 7-2. I/O Read Timing (ISA Bus — CL-GD5434 only)

Table 7-3. Memory Write Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_1	Address, SBHE* to SMEMW* active setup	5	–	ns
t_2	SMEMW* pulse width	3	–	MCLK
t_3	Data valid from SMEMW* active	–	3	MCLK
t_4	Data hold from SMEMW* inactive	10	–	ns
t_5	Address, SBHE* hold from SMEMW* inactive	0	–	ns
t_6	SMEMW* inactive to next SMEMW*	3	–	MCLK

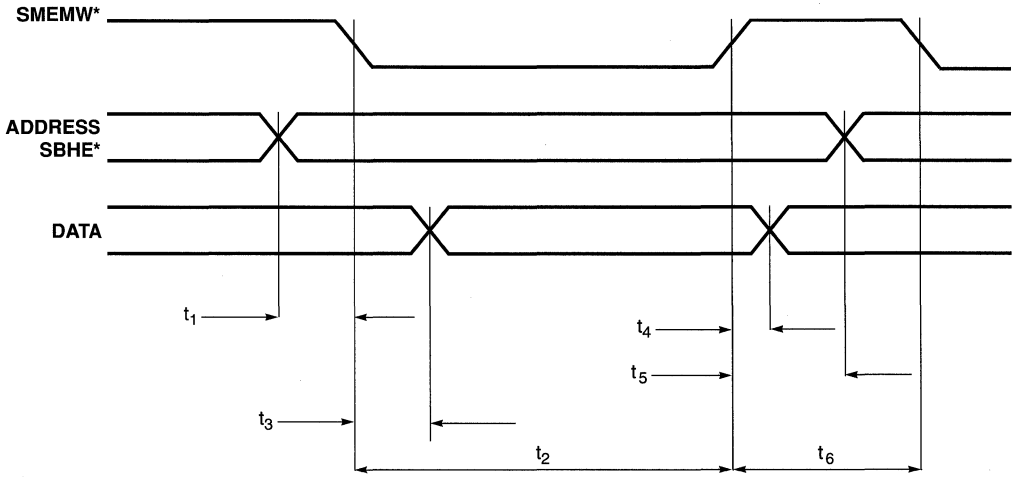


Figure 7-3. Memory Write Timing (ISA Bus — CL-GD5434 only)

Table 7-4. Memory Read Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_1	Address, SBHE* to SMEMR* active	5	–	ns
t_2	SMEMR* active to low-impedance delay	0	–	ns
t_3	Data delay from IOCHRDY active	–	15	ns
t_4	SMEMR* pulse width	–	[a]	ns
t_5	Data hold from SMEMR* inactive	0	20	ns
t_6	Address, SBHE* hold from SMEMR* inactive	0	–	ns
t_7	SMEMR* inactive to high-impedance delay	–	20	ns

[a] SMEMR* active-pulse width is determined by IOCHRDY.

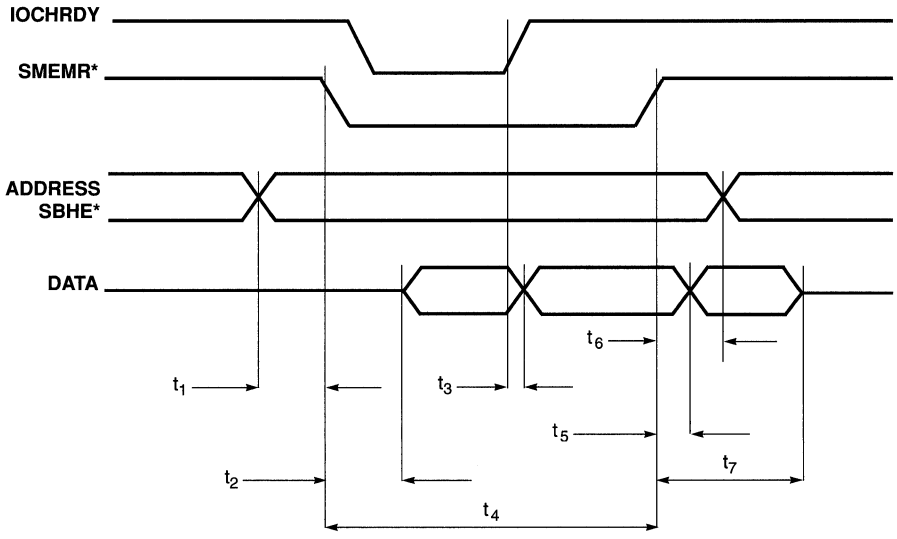


Figure 7-4. Memory Read Timing (ISA Bus — CL-GD5434 only)

Table 7-5. MCS16* Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_{1a}	MCS16* active delay from LA[23:17] valid	–	20	ns
t_{1b}	MCS16* active delay from SA[16:15] valid	–	14	ns
t_2	MCS16* inactive delay from address invalid	–	25	ns

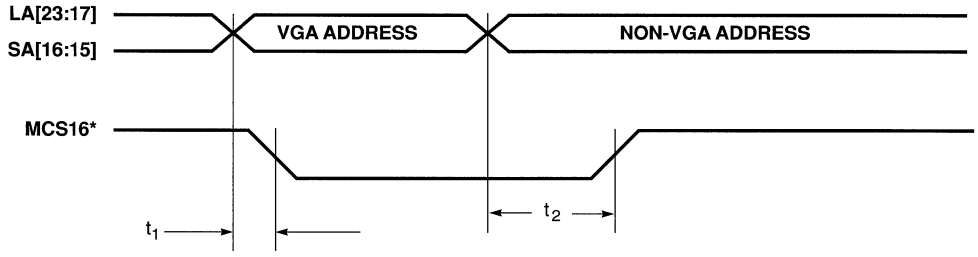


Figure 7-5. MCS16* Timing (ISA Bus — CL-GD5434 only)

Table 7-6. IOCS16* Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_1	IOCS16* active delay from address	–	25	ns
t_2	IOCS16* inactive delay from address	–	30	ns

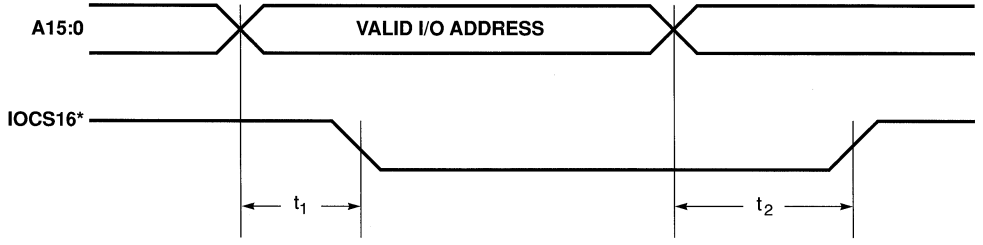


Figure 7-6. IOCS16* Timing (ISA Bus — CL-GD5434 only)

Table 7-7. BALE Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_1	LA[23:17] setup to BALE negative transition	20	–	ns
t_2	SBHE* setup to BALE negative transition	20	–	ns
t_3	LA[23:17] hold from BALE negative transition	20	–	ns
t_4	SBHE* hold from BALE negative transition	20	–	ns
t_5	BALE pulse width	20	–	ns

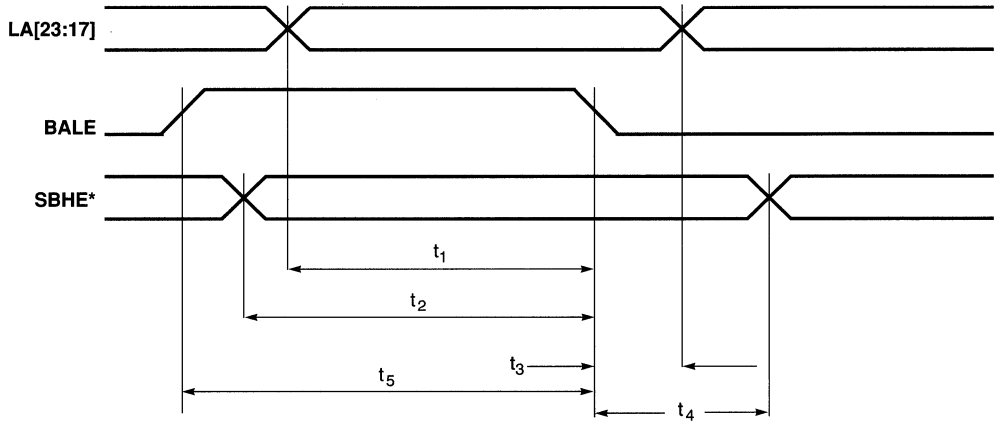


Figure 7-7. BALE Timing (ISA Bus — CL-GD5434 only)

Table 7-8. IOCHRDY for Memory Access Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_1	SMEMR* or SMEMW* active to IOCHRDY inactive low	–	28	ns
t_2	IOCHRDY inactive low pulse width	10	[a]	ns

[a] Video mode dependent.

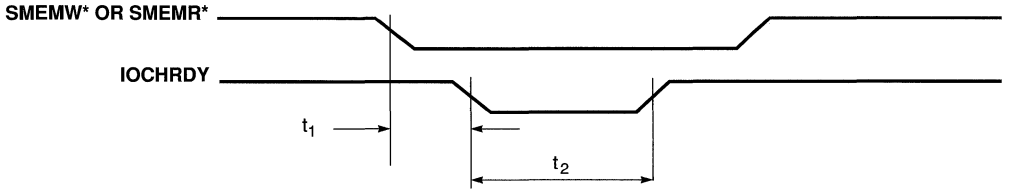
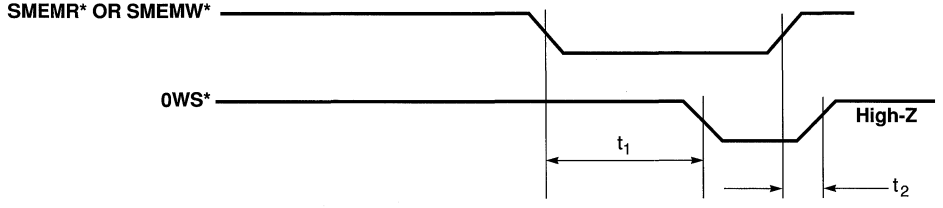


Figure 7-8. IOCHRDY for Memory Access Timing (ISA Bus — CL-GD5434 only)

Table 7-9. 0WS* Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_{1a}	0WS* active delay from SMEMR* (BIOS access)	–	22	ns
t_{1b}	0WS* active delay from SMEMW* (Display Memory write)	–	18	ns
t_{2a}	0WS* high-impedance delay from SMEMR*	–	18	ns
t_{2b}	0WS* high-impedance delay from SMEMW*	–	19	ns



High-Z = High-impedance

Figure 7-9. 0WS* Timing (ISA Bus — CL-GD5434 only)

Table 7-10. Refresh Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_1	REFRESH* active setup to SMEMR* active	20	–	ns
t_2	REFRESH* active hold from SMEMR* active	0	–	ns

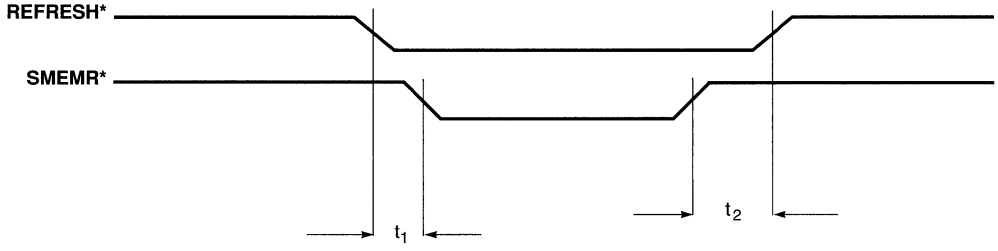


Figure 7-10. Refresh Timing (ISA Bus — CL-GD5434 only)

Table 7-11. EROM* Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_1	EROM* active delay from SMEMR* active	–	30	ns
t_2	EROM* inactive delay from SMEMR* inactive	–	20	ns

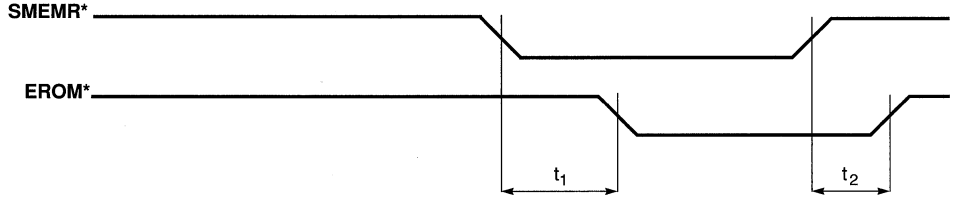


Figure 7-11. EROM* Timing (ISA Bus — CL-GD5434 only)

Table 7-12. AEN Timing (ISA Bus — CL-GD5434 only)[a]

Symbol	Parameter	MIN	MAX	Units
t_1	AEN setup to IOR* or IOW* active	5	–	ns
t_2	AEN hold from IOR* or IOW* inactive	5	–	ns

[a] AEN high, as shown below, will cause the CL-GD543X/'4X to **ignore** the I/O cycle.

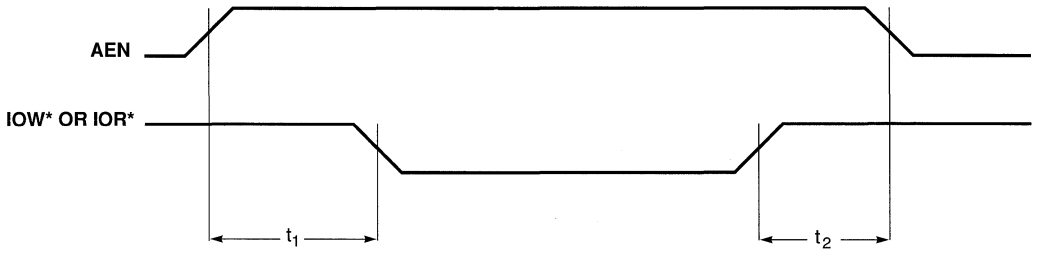


Figure 7-12. AEN Timing (ISA Bus — CL-GD5434 only)

Table 7-13. LCLK, CLK Timing ('486/VESA® VL-Bus™)

Symbol	Parameter	MIN	MAX	Units
t_1	Rise time (LCLK) VESA VL-Bus	–	4	ns
t_2	Fall time (LCLK) VESA VL-Bus	–	4	ns
t_3	High period (LCLK) VESA VL-Bus	40	60	% t_5
t_4	Low period (LCLK) VESA VL-Bus	40	60	% t_5
t_5	Period (LCLK) VESA VL-Bus	20	–	ns
t_1	Rise time (CLK) PCI bus	–	4	ns
t_2	Fall time (CLK) PCI bus	–	4	ns
t_3	High period (CLK) PCI bus	40	60	% t_5
t_4	Low period (CLK) PCI bus	40	60	% t_5
t_5	Period (CLK) PCI bus	30	–	ns

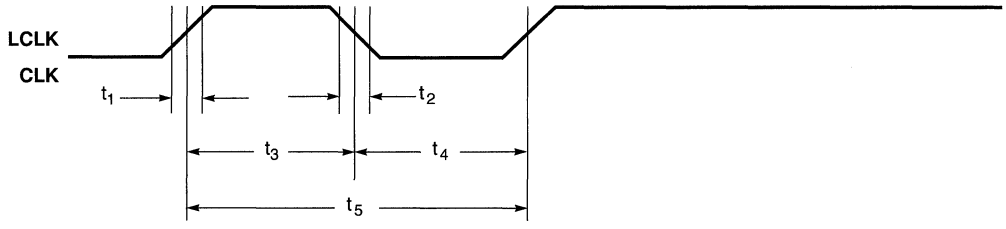
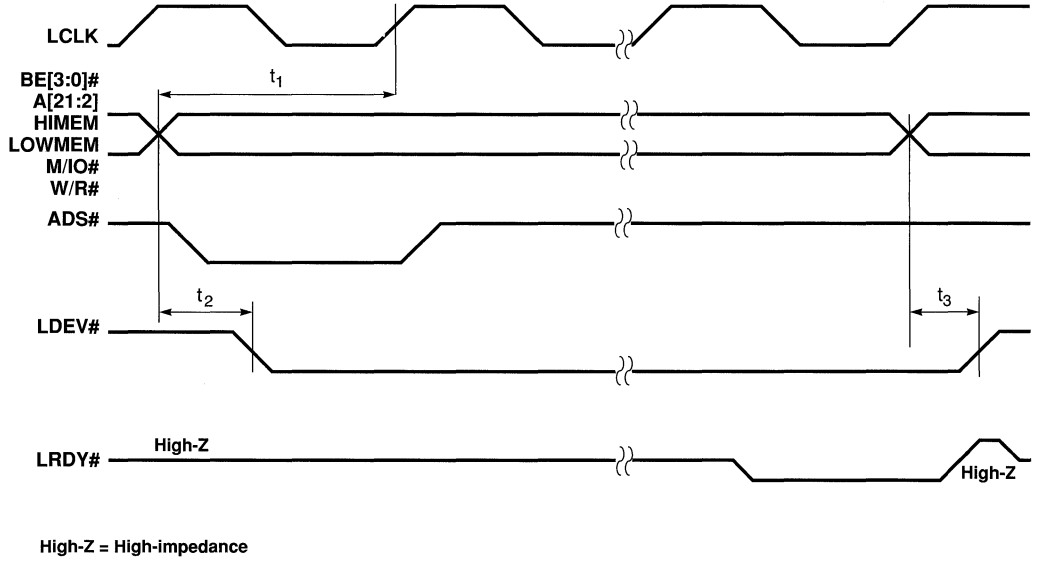


Figure 7-13. LCLK, CLK Timing ('486/VESA® VL-Bus™)

Table 7-14. ADS# and LDEV# Timing ('486/VESA® VL-Bus™)

Symbol	Parameter	MIN	MAX	Units
t_1	Address, Status, ADS# setup to LCLK	7	–	ns
t_2	LDEV# active delay from Address, Status (20-pF loading)	0	20	ns
t_3	LDEV# inactive delay from Address, Status	0	20	ns



High-Z = High-impedance

Figure 7-14. ADS#, and LDEV# Timing ('486/VESA® VL-Bus™)

Table 7-15. LRDY# Delay ('486/VESA® VL-Bus™)

Symbol	Parameter	MIN	MAX	Units
t_1	LRDY# active delay from LCLK	–	13	ns
t_2	LRDY# inactive delay from LCLK	–	13	ns
t_3	LRDY# high before high-impedance	0.4	0.5	LCLK

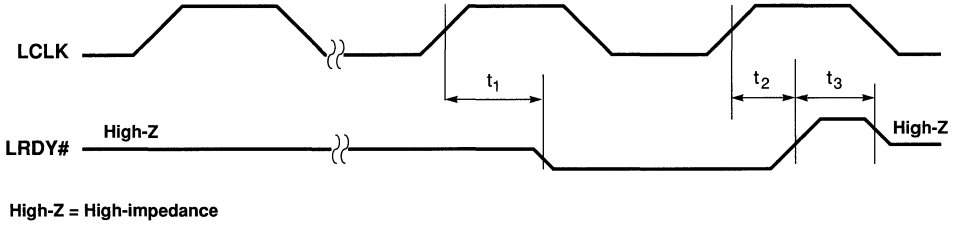


Figure 7-15. LRDY# Delay (486/VESA® VL-Bus™)

Table 7-16. Read Data/RDYRTN# Timing ('486/VESA® VL-Bus™)

Symbol	Parameter	MIN	MAX	Units
t_1	Read data setup to LCLK	4	–	ns
t_2	Read data hold from LCLK	2	–	ns
t_3	RDYRTN# setup to LCLK	5	–	ns
t_4	LRDY high	0.4	0.5	LCLK

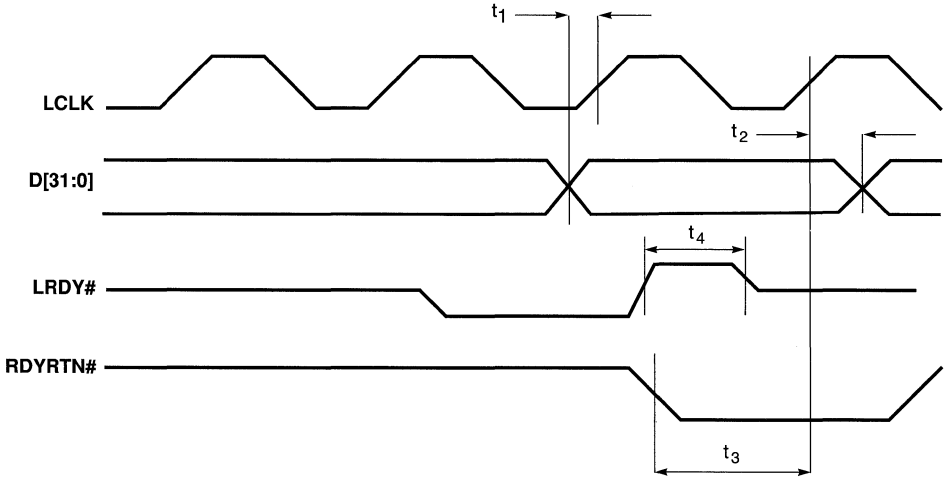


Figure 7-16. Read Data/RDYRTN# Timing ('486/VESA® VL-Bus™)

Table 7-17. FRAME#, DEVSEL#, AD[31:0], and C/BE[3:0]# (PCI Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	FRAME# setup to CLK	7	–	ns
t_2	AD[31:0] (Address) setup to CLK	7	–	ns
t_3	AD[31:0] (Address) hold from CLK	0	–	ns
t_4	AD[31:0] (Data) setup to CLK	7	–	ns
t_5	AD[31:0] (Data) hold from CLK	0	–	ns
t_6	AD[31:0], C/BE[3:0]# high-impedance from CLK	0	28	ns
t_7	C/BE[3:0]# (bus CMD) setup to CLK	7	–	ns
t_8	C/BE[3:0]# (bus CMD) hold from CLK	0	–	ns
t_{8a}	C/BE[3:0]# (byte enable) setup to CLK	7	–	ns
t_9	DEVSEL# delay from CLK	–	15	ns
t_{10}	DEVSEL# high before high-impedance	1	–	CLK

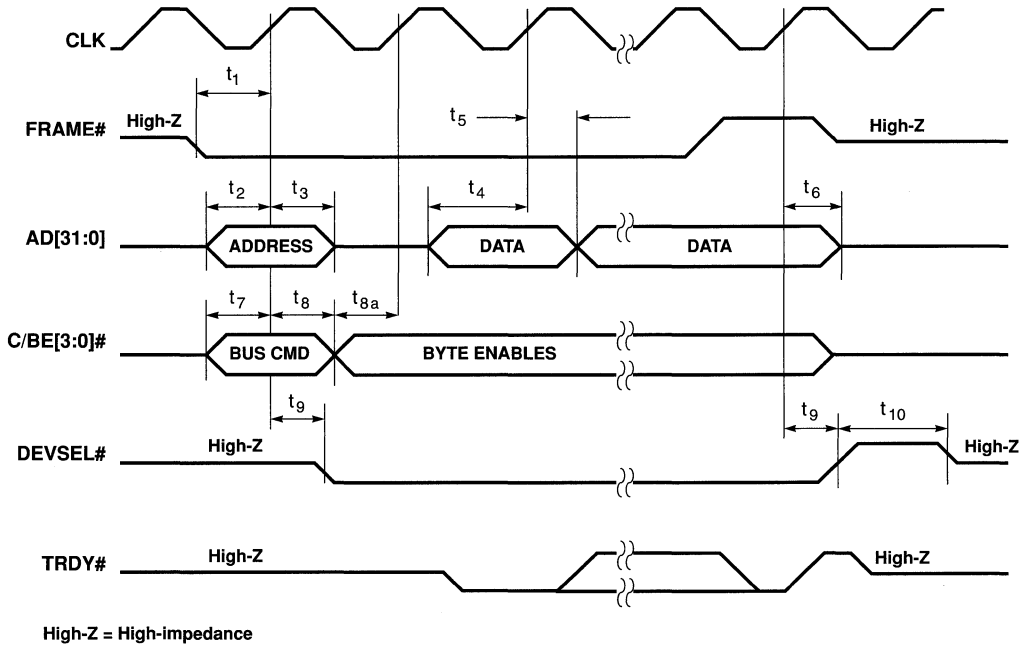
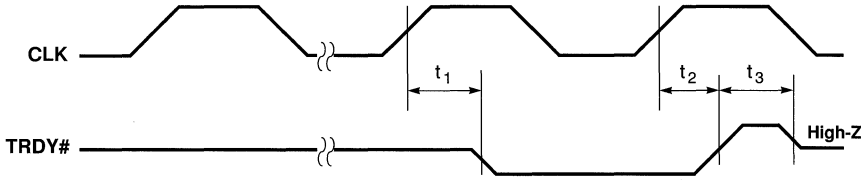


Figure 7-17. FRAME#, DEVSEL#, AD[31:0], and C/BE[3:0]# (PCI Bus)

Table 7-18. TRDY# Delay (PCI Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	TRDY# active delay from CLK	–	15	ns
t_2	TRDY# inactive delay from CLK	–	15	ns
t_3	TRDY# high before high-impedance	1	–	CLK



High-Z = High-impedance

Figure 7-18. TRDY# Delay (PCI Bus)

Table 7-19. Read Data/IRDY# Timing (PCI Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Read data setup to TRDY# active	7	–	ns
t_2	Read data hold from TRDY# inactive	0	–	ns
t_3	IRDY# setup to CLK	7	–	ns
t_4	IRDY# hold from CLK	0	–	ns

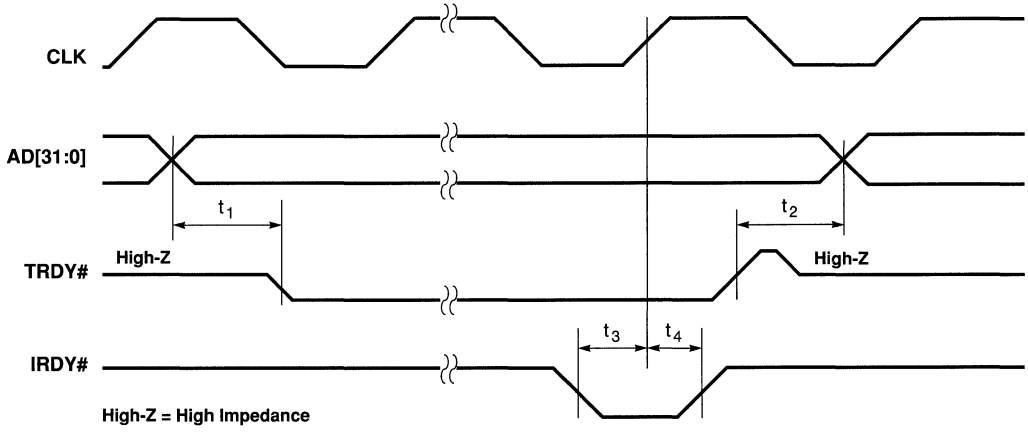
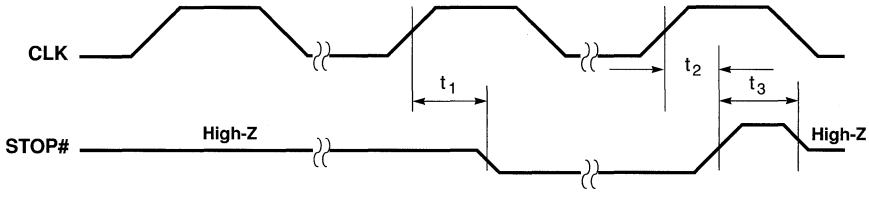


Figure 7-19. Read Data/IRDY# (PCI Bus)

Table 7-20. STOP# Delay (PCI Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	STOP# active delay from CLK	–	15	ns
t_2	STOP# inactive delay from CLK	–	15	ns
t_3	STOP# high before high-impedance	1	–	CLK

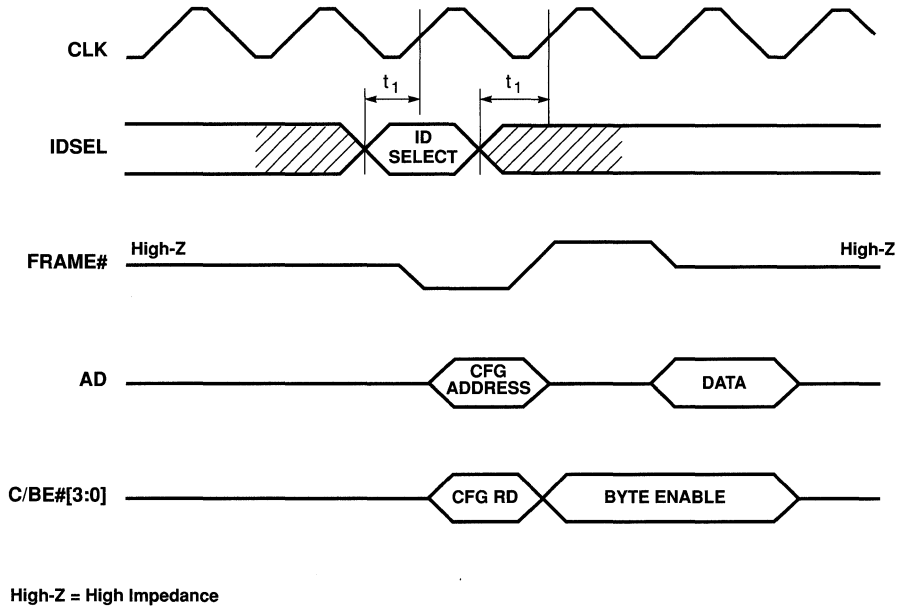


High-Z = High Impedance

Figure 7-20. STOP# Delay (PCI Bus)

Table 7-21. IDSEL Timing (PCI Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	IDSEL setup to CLK	–	15	ns

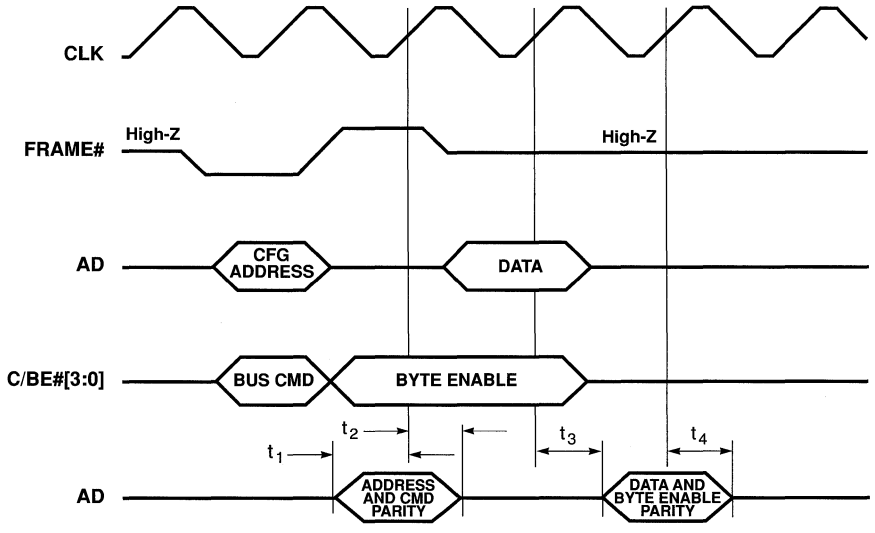


High-Z = High Impedance

Figure 7-21. IDSEL Timing (PCI Bus)

Table 7-22. PAR Timing (PCI Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	PAR setup from CLK (input to CL-GD543X/'4X)	7	–	ns
t_2	PAR hold from CLK (input to CL-GD543X/'4X)	0	–	ns
t_3	PAR delay from CLK (output from CL-GD543X/'4X)	7	–	ns
t_4	PAR hold from CLK (output from CL-GD543X/'4X)	0	–	ns

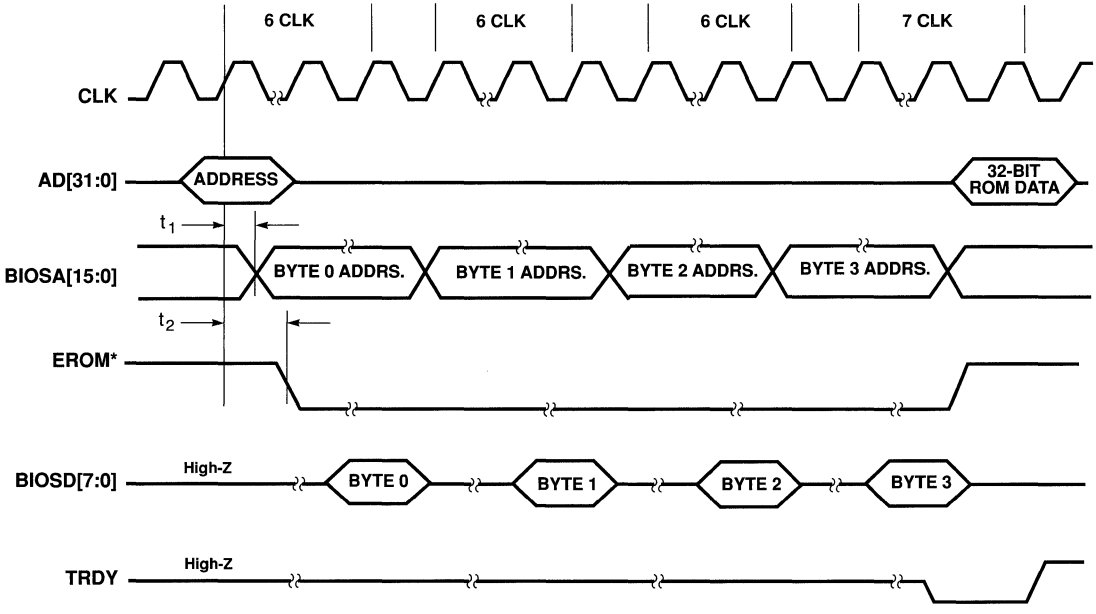


High-Z = High Impedance

Figure 7-22. PAR Timing (PCI Bus)

Table 7-23. EROM*, BIOSA[15:0] Timing (PCI Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	BIOSA[15:0] delay from CLK	–	80	ns
t_2	EROM* delay from CLK	–	50	ns



High-Z = High impedance

Figure 7-23. EROM*, BIOSA[15:0] Timing (PCI Bus)

Table 7-24. CAS*-before-RAS* Refresh Timing (Display Memory Bus)[a]

Symbol	Parameter	MIN	MAX
t_1	t_{CSR}: CAS* active setup to RAS* active	1 m[b]	–
t_2	t_{RAS}: RAS* low pulse width	4 m	–
t_3	t_{RP}: RAS* high pulse width	3 m	–

[a] There will be either three or five RAS* pulses while CAS* remains low. On the CL-GD5436, GR18[3] can be programmed to '1' for a single RAS* pulse.

[b] m = MCLK

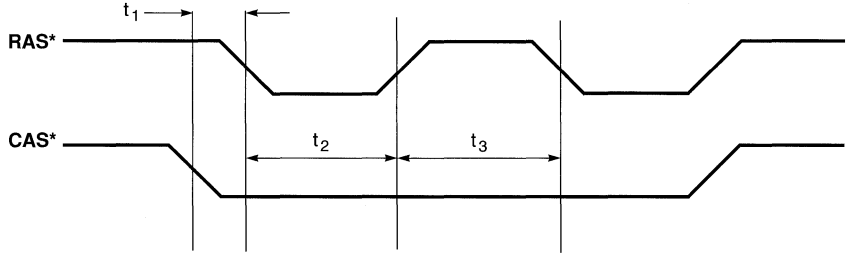


Figure 7-24. CAS*-before-RAS* Refresh Timing (Display Memory Bus)

Table 7-25. Display Memory Bus: Common Parameters

Symbol	Parameter	MIN	MAX
t_1	t_{ASR}: Address setup to RAS* active	1.5 m – 9 ns [a]	–
t_2	t_{RAH}: Row Address hold from RAS* active	1.5 m – 5 ns	–
t_3	t_{ASC}: Address Setup to CAS* active	1 m – 3 ns	–
t_4	t_{CAH}: Column Address hold from CAS* active	1 m	–
t_5	t_{RCD}: RAS* active to CAS* active delay (standard RAS)	2.5 m – 7.5 ns	–
t_5	t_{RCD}: RAS* active to CAS* active delay (extended RAS)	3 m	–
t_6	t_{RAS}: RAS* pulse width low (standard RAS)	3.5 m	–
t_6	t_{RAS}: RAS* pulse width low (extended RAS)	4 m – 1 ns	–
t_7	t_{RP}: RAS* precharge (RAS* pulse width high — standard RAS)	2.5 m – 2 ns	–
t_7	t_{RP}: RAS* precharge (RAS* pulse width high — extended RAS)	3 m – 1.5 ns	–
t_8	t_{CAS}: CAS* pulse width low	1 m + 3 ns	1m + 6 ns
t_9	t_{CP}: CAS* precharge (CAS* pulse width high)	1 m – 6 ns	1m – 3 ns
t_{10}	t_{RC}: Random cycle (standard RAS)	6 m	–
t_{10}	t_{RC}: Random cycle (extended RAS)	7 m	–
t_{11}	t_{PC}: Page mode cycle	2 m	–

[a] m = MCLK

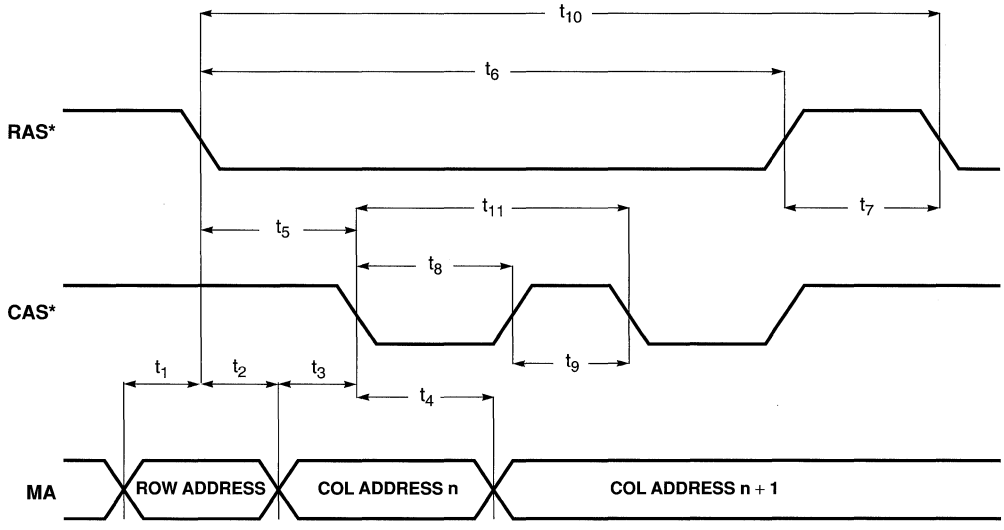


Figure 7-25. Display Memory Bus: Common Parameters

Table 7-26. Display Memory Bus: Read Cycles

Symbol	Parameter	MIN	MAX
t_1	Read data setup to CAS* rising edge	0	–
t_2	Read data hold from CAS* high	10 ns	–

Only parameters t_1 and t_2 are defined for the CL-GD543X/'4X. The remaining parameters in this table are calculated from parameters from this table and the previous table. These parameters are provided so that system designers can easily determine DRAM requirements.

t_3	DRAM access time from RAS* (standard RAS)	–	3.5 m – 1 ns
t_3	DRAM access time from RAS* (extended RAS)	–	4 m – 1 ns
t_4	DRAM access time from Column Address	–	2 m
t_5	DRAM access time from CAS* active	–	1 m + 3 ns
t_6	DRAM access time from CAS* precharge	–	2 m

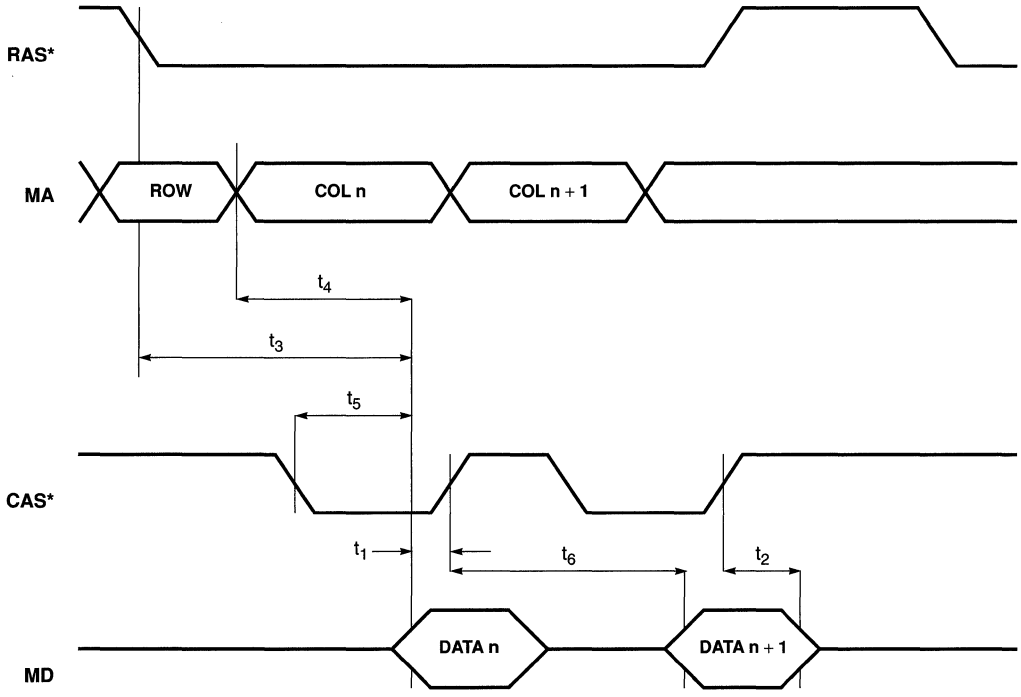


Figure 7-26. Display Memory Bus: Read Cycles

Table 7-27. Display Memory Bus: Write Cycles

Symbol	Parameter	MIN	MAX
t_1	t_{CWL}: WE* active setup to CAS* active	1 m + 0.5 ns [a]	–
t_2	t_{DS}: Write data setup to CAS* active	1 m – 2 ns	1 m + 2 ns
t_3	t_{DH}: Write data hold from CAS* active	1 m + 1 ns	–
t4	t_{WCH}: WE active hold from CAS* active	1.5 m – 2 ns	–

[a] m = MCLK

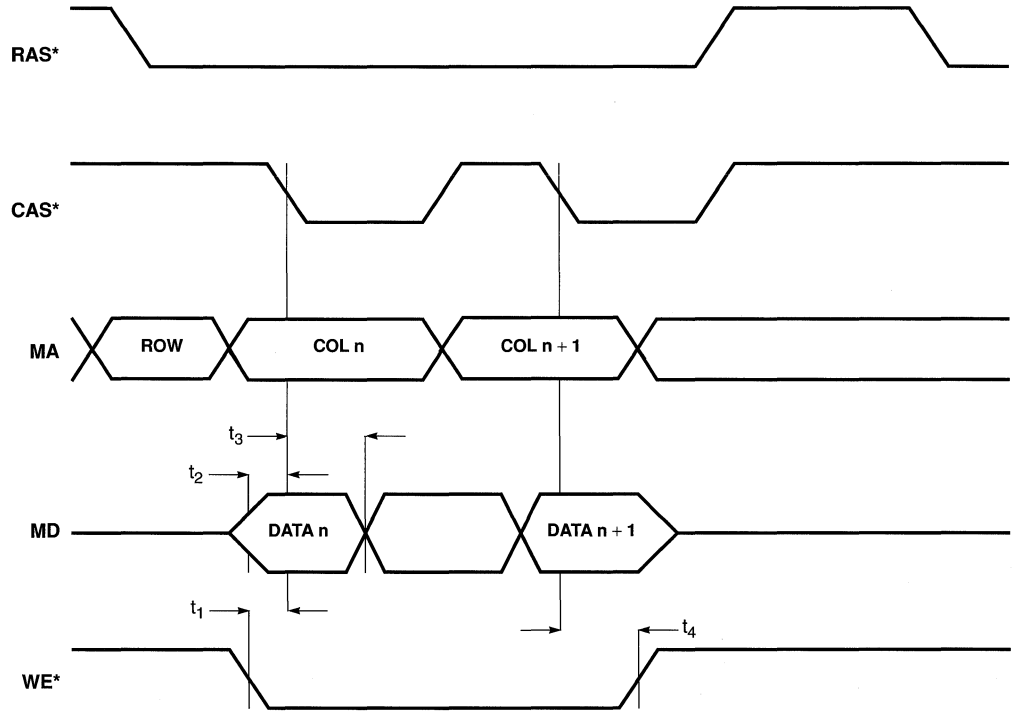


Figure 7-27. Display Memory Bus: Write Cycles

Table 7-28. Display Memory Bus: Common Parameters (EDO Timing — CL-GD5436)

Symbol	Parameter	MIN	MAX
t_1	t_{ASR}: Address setup to RAS* active	1.5 m – 9 ns [a]	–
t_2	t_{RAH}: Row Address hold from RAS* active	1.5 m – 5 ns	–
t_3	t_{ASC}: Address setup to CAS* active	1m – 3 ns	–
t_4	t_{CAH}: Column Address hold from CAS* active	1 m	–
t_5	t_{RCD}: RAS* active to CAS* active delay (EDO timing)	4 m	–
t_6	t_{RAS}: RAS* pulse width low (EDO timing)	5 m – 1 ns	–
t_7	t_{RP}: RAS* precharge (RAS* pulse width high) (EDO timing)	3 m + 1.5 ns	–
t_8	t_{CAS}: CAS* pulse width low	1m + 3 ns	1m + 6 ns
t_9	t_{CP}: CAS* precharge (CAS* pulse width high)	1m – 6 ns	1m – 3 ns
t_{10}	t_{RC}: Random cycle (EDO timing)	8 m	–
t_{11}	t_{PC}: Page mode cycle	2 m	–
t_{12}	t_{CAS}: CAS* pulse width low (last CAS* of Page mode read burst)	3 m	–
t_{13}	t_{CRP}: CAS* to RAS* precharge	1 m	–

[a] m = MCLK

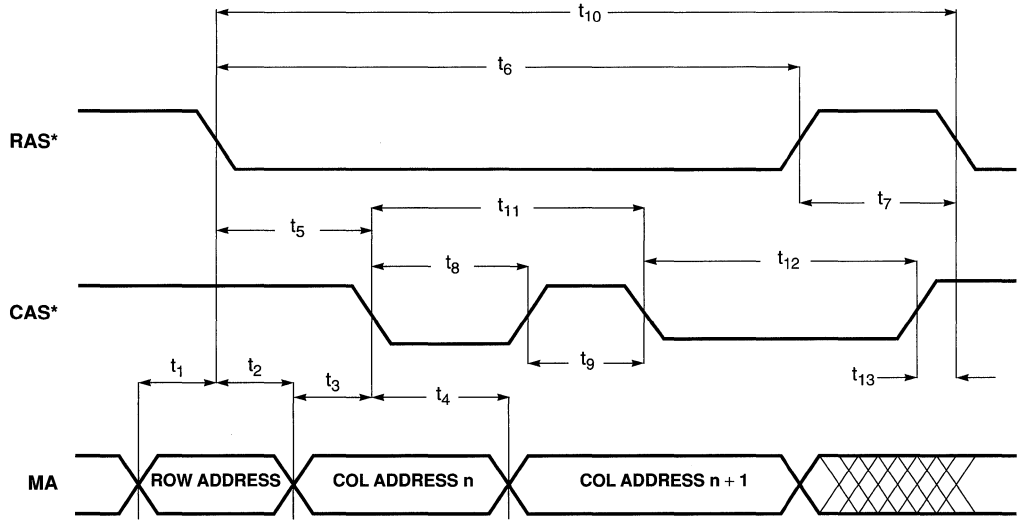


Figure 7-28. Display Memory Bus: Common Parameters (EDO Timing — CL-GD5436)

Table 7-29. Display Memory Bus: Read Cycles (EDO Timing — CL-GD5436)

Symbol	Parameter	MIN	MAX
t_1	Read data setup to CAS* falling edge	1 ns	–
t_2	Read data hold from CAS* falling edge	5 ns	–

The timing shown in this table and figure are for EDO Mode DRAM timing. See the description of register GR18[2]. This timing requires the display memory be populated with EDO DRAMs. These devices hold their read data valid past the rising edge of CAS*.

Depending on the cycle being executed, the read data setup and hold times may be defined with respect to CAS* falling edge (Page mode cycle other than last), WE* falling edge (read followed by write), or a timing term that is available only internally (Last Page mode cycle). If the DRAM can meet the timing requirements of the falling CAS* edge case, it will meet the other two cases.

Only parameters t_1 and t_2 are defined for the CL-GD543X/'4X. The remaining parameters in this table are calculated from parameters from this table and the previous table. These parameters are provided so that system designers can easily determine DRAM requirements.

t_3	DRAM access time from RAS* (EDO timing)	–	5 m
t_4	DRAM access time from column address (EDO timing)	–	3 m
t_5	DRAM access time from CAS* active (EDO timing)	–	2 m
t_6	DRAM access time from CAS* precharge (EDO timing)	–	3 m

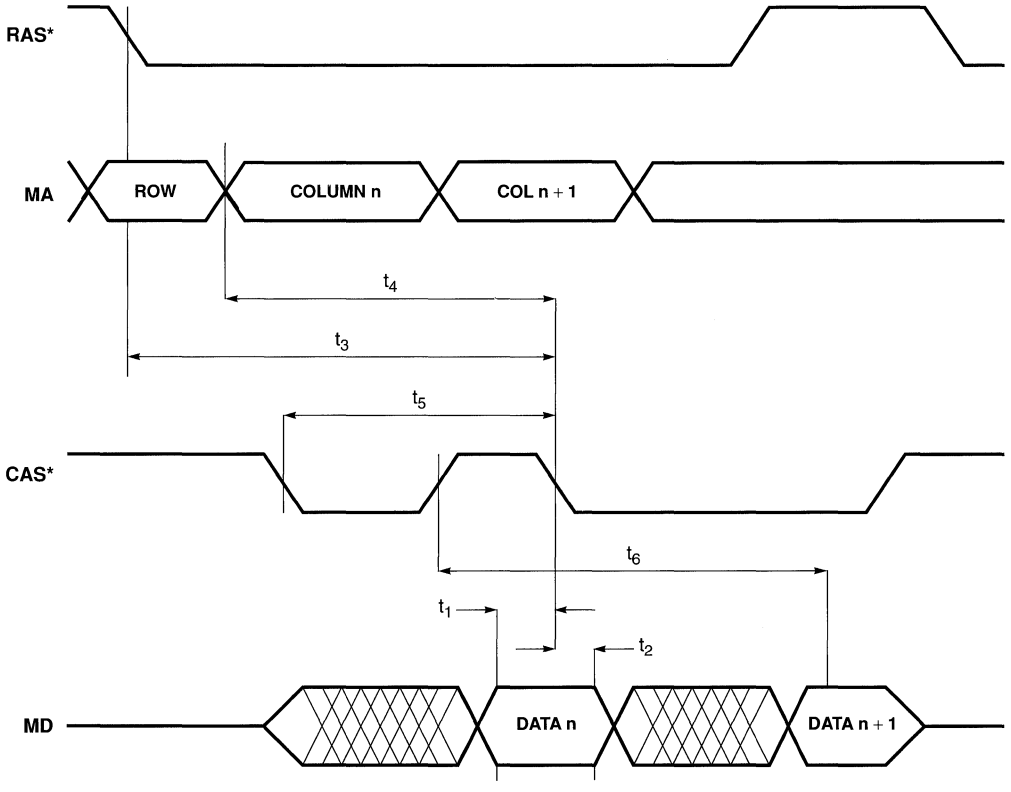


Figure 7-29. Display Memory Bus: Read Cycles (EDO Timing — CL-GD5436)

Table 7-30. Display Memory Bus: BitBLT R-W Cycle (CL-GD5436 only)

Symbol	Parameter	Nominal	
		GR18[2] = '0'	GR18[2] = '1'
t_1	t_{RCH}: WE* active delay from CAS* inactive (GR18[0] = '0')	2 m[a]	3 m
t_1	t_{RCH}: WE* active delay from CAS* inactive (GR18[0] = '1')	1 m	2 m
t_2	t_{CP}: Read CAS* to write CAS* delay (GR18[1] = '0')	3 m	4 m
t_2	t_{CP}: Read CAS* to write CAS* delay (GR18[1] = '1')	2 m	3 m
t_3	t_{CWL}: WE* active setup to CAS* active	1 m	1 m

[a] m = MCLK

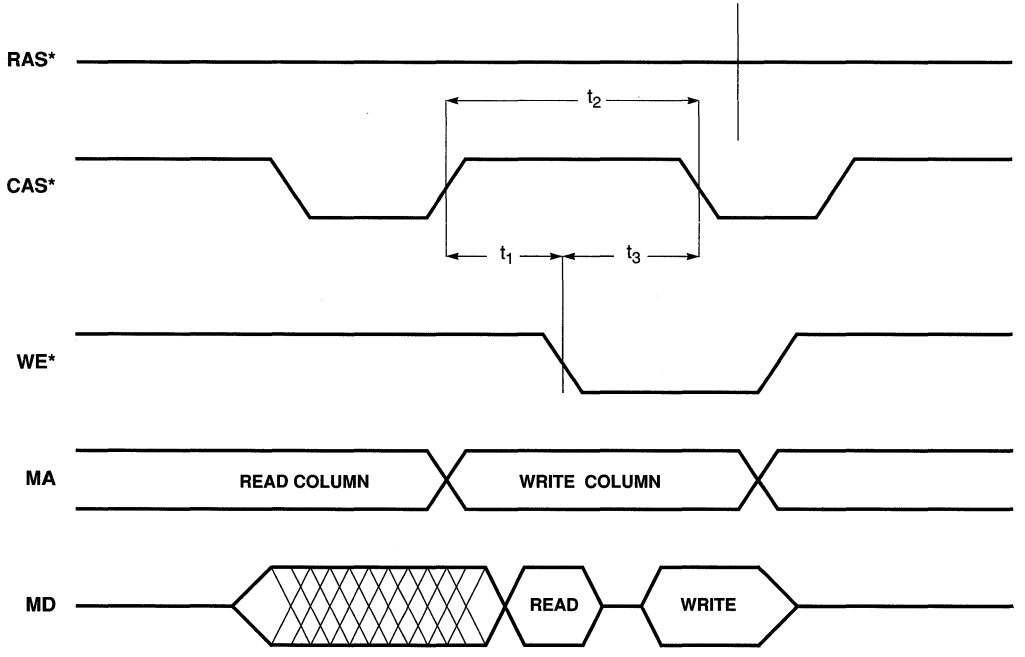


Figure 7-30. Display Memory Bus: BitBLT R-W Cycle (CL-GD5436 only)

Table 7-31. P-Bus as Inputs: 8-Bit Mode (DCLK input as reference)

Symbol	Parameter	MIN	MAX	Units
t_1	P[7:0], BLANK* setup to DCLK	0	–	ns
t_2	P[7:0], BLANK* hold from DCLK	6	–	ns

NOTE: The CL-GD543X/'4X RAMDAC is driven externally. For CL-GD543X/'4X Overlay modes, BLANK* is an output.

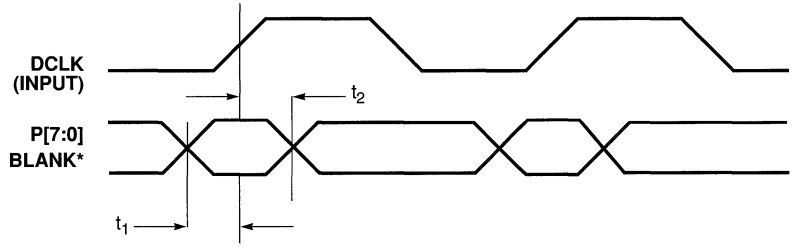


Figure 7-31. P-Bus as Inputs: 8-Bit Mode (External DCLK)

Table 7-32. Feature Bus Timing: 8-Bit Mode, Outputs (DCLK output as reference)

Symbol	Parameter	MIN	MAX	Units
t_1	DCLK to BLANK* delay	–1	1	ns
t_2	DCLK to HSYNC, VSYNC delay	1	3	ns
t_3	DCLK to P[7:0] delay	–2	0	ns
t_4	DCLK to OVRW* delay	–1	1	ns

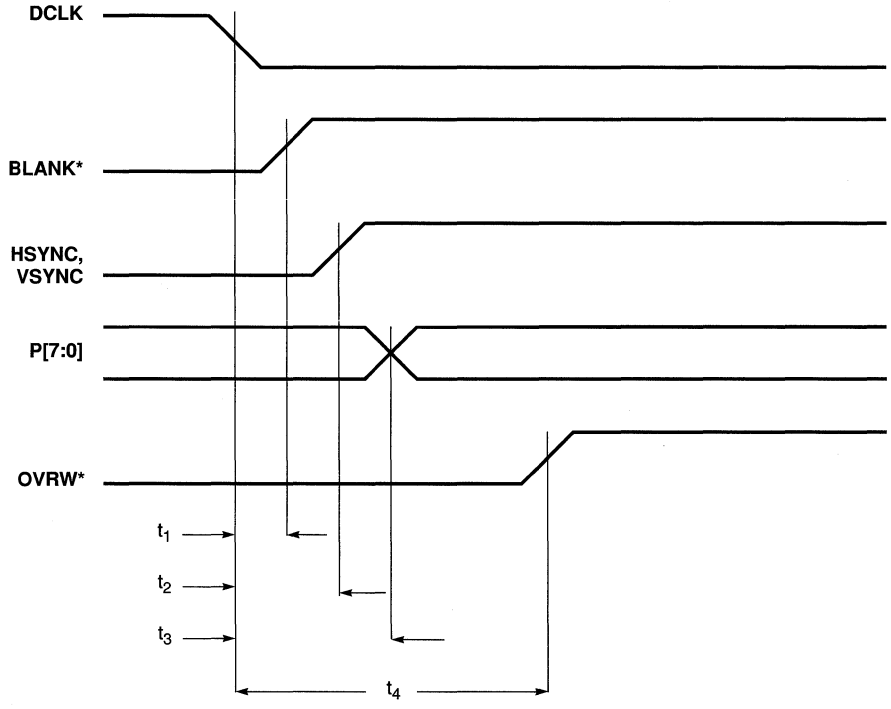


Figure 7-32. Feature Bus Timing: 8-Bit Mode, Outputs (Internal DCLK)

Table 7-33. P-Bus as Outputs: 16-Bit Mode (DCLK output as reference)

Symbol	Parameter	MIN	MAX	Units
t_1	DCLK (rising edge) to P[7:0] delay	–2	0	ns
t_2	DCLK (falling edge) to P[7:0] delay	–1	1	ns

NOTE: Register SR7[2:1] = '0,1' and register GRE[0] = '1'.

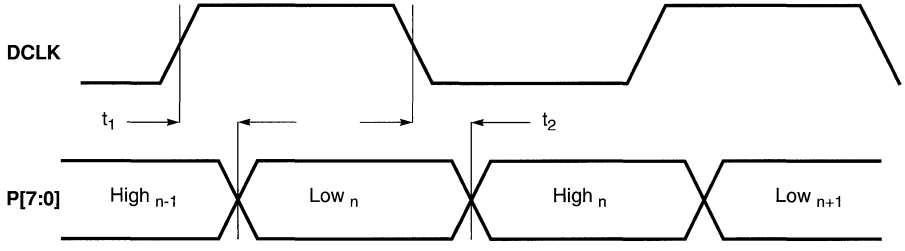


Figure 7-33. P-Bus as Outputs: 16-Bit Mode (Internal DCLK)

Table 7-34. P-Bus as Inputs: 16-Bit Mode (DCLK input as reference)

Symbol	Parameter	MIN 'GD5430	MIN 'GD5434	MIN 'GD5436	Units
t_1	P[7:0] setup to DCLK (rising edge — external DCLK)	–4	–2	tbd	ns
t_2	P[7:0] hold from DCLK (rising edge — external DCLK)	8	5	tbd	ns
t_3	P[7:0] setup to DCLK (falling edge — external DCLK)	–4	–2	tbd	ns
t_4	P[7:0] hold from DCLK (rising edge — external DCLK)	8	5	tbd	ns

NOTE: Clock mode 1 selected in Hidden DAC register (D5 = '0').

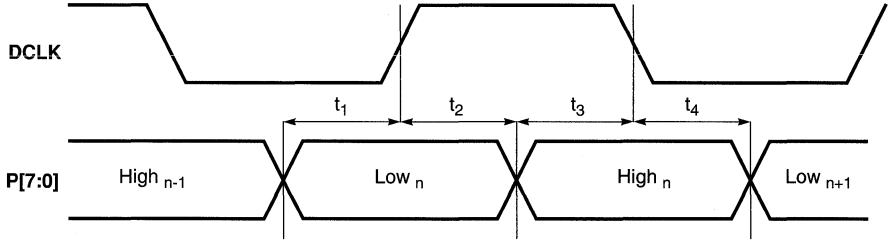


Figure 7-34. P-Bus as Inputs: 16-Bit Mode (External DCLK)

Table 7-35. P-Bus as Inputs: 16-Bit Mode, Clock Mode 2 (DCLK input as reference)

Symbol	Parameter	MIN	MAX	Units
t_1	P[7:0], BLANK* setup to DCLK	–2	–	ns
t_2	P[7:0], BLANK* hold from DCLK	5	–	ns

NOTES:

1) Clock mode 2 selected in HIdden DAC register (D5 = '1').
2) The first low byte of 16-bit data input must be synchronized with BLANK* or the start of the overlay window, whichever is later. The first high byte will be clocked on the next rising edge of DCLK.
3) For CL-GD543X/'4X Overlay modes, BLANK* will be an output.

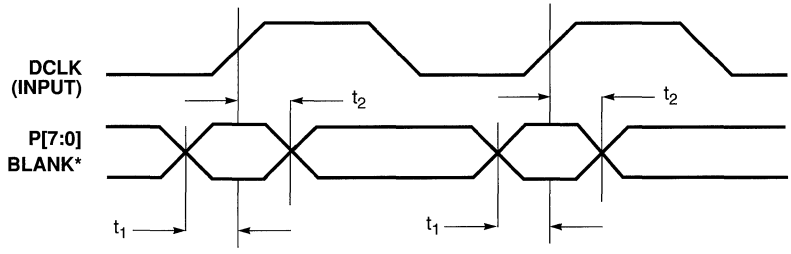


Figure 7-35. P-Bus as Inputs: 16-Bit Mode, Clock Mode 2 (External DCLK)

Table 7-36. P-Bus as Inputs: 16-Bit Mode (DCLK output as reference)

Symbol	Parameter	MIN	Units
t_1	P[7:0] setup to DCLK (rising edge — internal DCLK)	4	ns
t_2	P[7:0] hold from DCLK (rising edge — internal DCLK)	2	ns
t_3	P[7:0] setup to DCLK (falling edge — internal DCLK)	4	ns
t_4	P[7:0] hold from DCLK (rising edge — internal DCLK)	2	ns

NOTE: Clock mode selected in Hidden DAC register (D5 = '0').

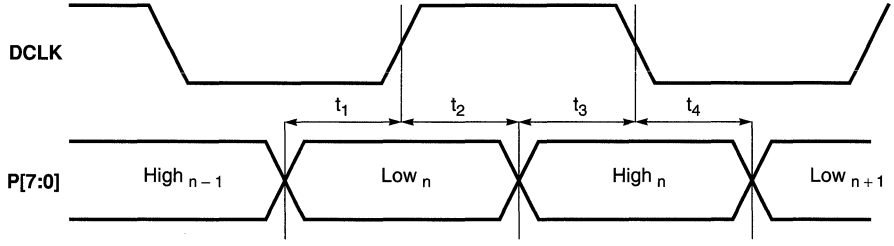


Figure 7-36. P-Bus as Inputs: 16-Bit Mode (External DCLK)

Table 7-37. Video Port Timing (CL-GD5440 only)

Symbol	Parameter	MIN	Units
t_1	Back porch	16	Pixel clocks

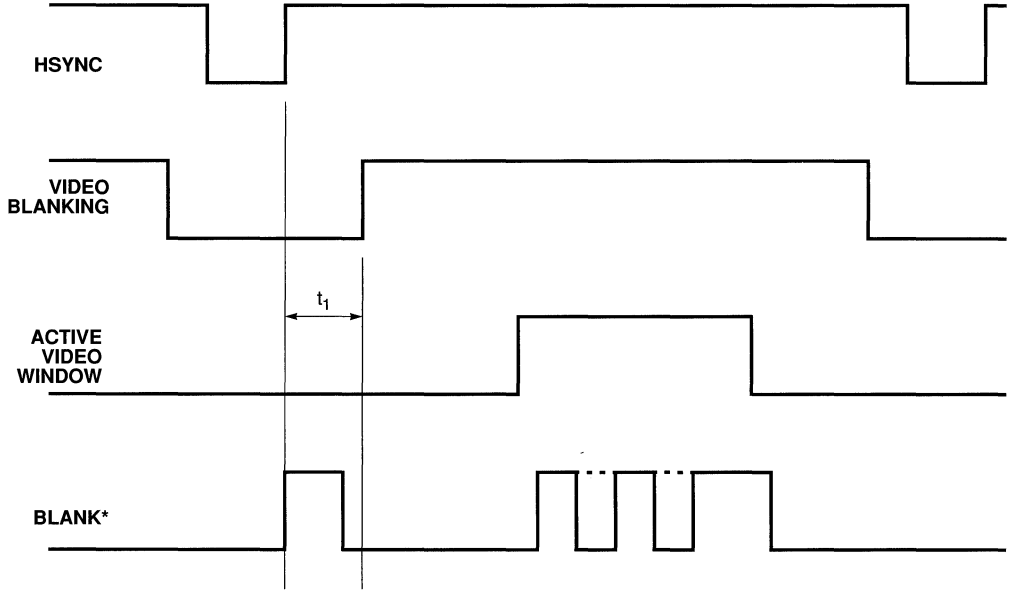


Figure 7-37. Video Port Timing (CL-GD5440 only)

Table 7-38. Video Port Timing: Detail (CL-GD5440 only)

Symbol	Parameter	MIN	MIN	Units
t_1	DCLK period	12	–	ns
t_2	BLANK* delay from DCLK rising edge	–	7	ns
t_3	P[7:0] setup to DCLK rising edge	5	–	ns
t_4	P[7:0] hold from DCLK rising edge	0	–	ns

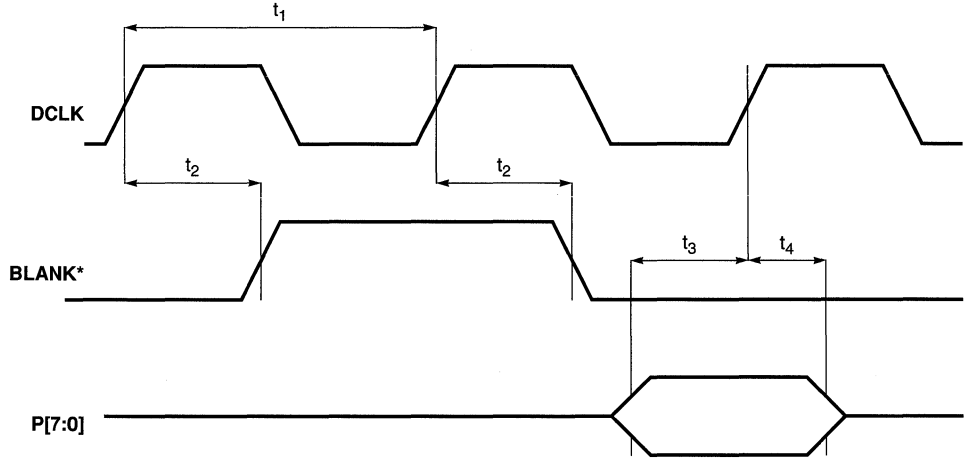


Figure 7-38. Video Port Timing: Detail (CL-GD5440 only)

Table 7-39. DCLK as Input

Symbol	Parameter: CL-GD5434	MIN	MAX	Units
t_1	Rise time	–	3	ns
t_2	Fall time	–	3	ns
t_3	High period	40	60	% of t_5
t_4	Low period	40	60	% of t_5
t_5	Period	17	–	ns
Parameter: CL-GD5430/'40				
t_1	Rise time	–	3	ns
t_2	Fall time	–	3	ns
t_3	High period: Clock mode 1	45	55	% of t_5
t_3	High period: Clock mode 2	30	70	% of t_5
t_4	Low period: Clock mode 1	45	55	% of t_5
t_4	Low period: Clock mode 2	30	70	% of t_5
t_5	Period	12.5	–	ns

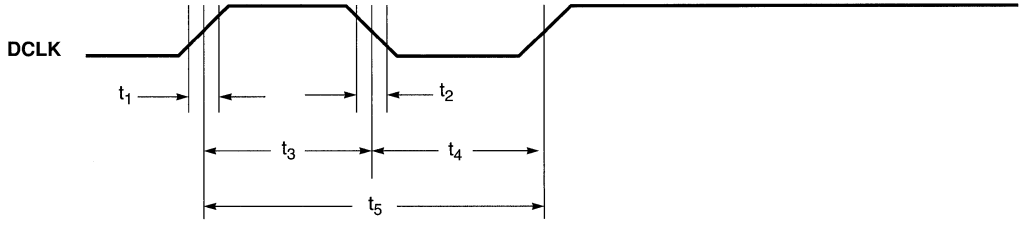


Figure 7-39. DCLK as Input

Table 7-40. RESET Timing

Symbol	Parameter	MIN	MAX	Units
t_1	RESET pulse width	12	–	MCLK
t_2	MD[31:16] setup to RESET falling edge	2	–	ns
t_3	MD[31:16] hold from RESET falling edge	25	–	ns
t_4	RESET low to first IOW* or command	12	–	MCLK

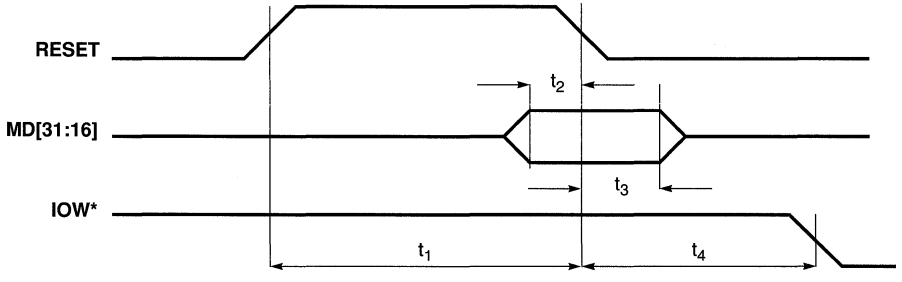
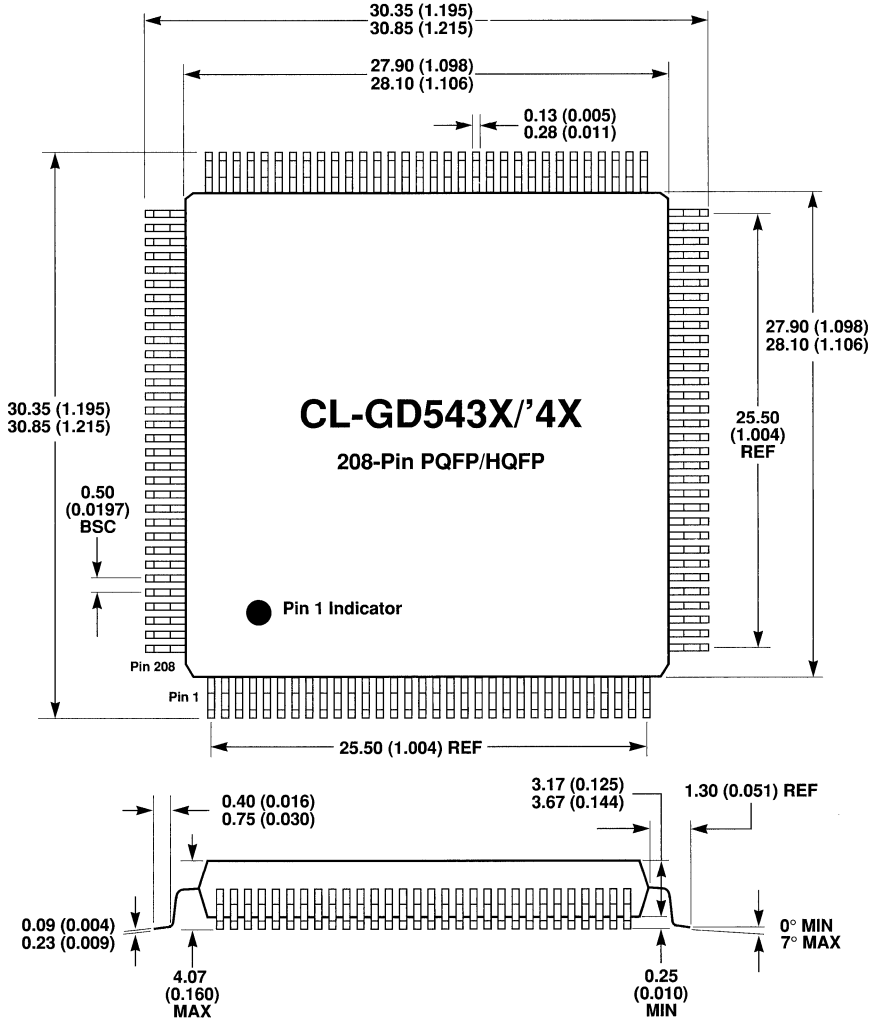


Figure 7-40. RESET Timing

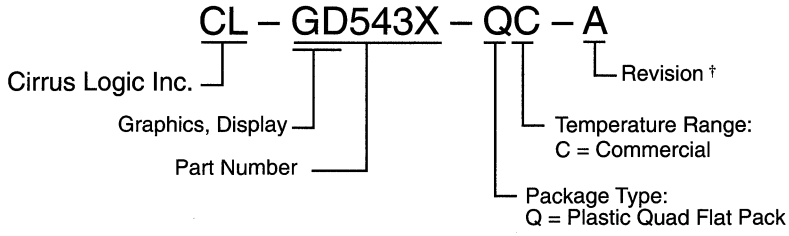
8. PACKAGE SPECIFICATIONS



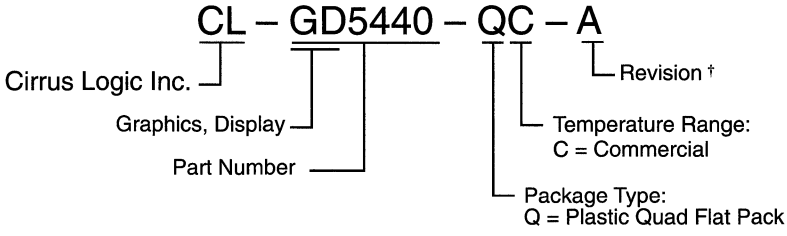
NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.
4) HQFP is a high-performance QFP with an exposed or unexposed heat sink.

9. ORDERING INFORMATION EXAMPLE



† Contact Cirrus Logic. for up-to-date information on revisions.



† Contact Cirrus Logic for up-to-date information on revisions.

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External and General Registers

4. EXTERNAL AND GENERAL REGISTERS

The External and General registers in the CL-GD543X/'4X are summarized in Table 4-1.

Table 4–1. External and General Registers Quick Reference

Abbreviation	Register Name	Index	Port	Reset	Page
POS94	POS94	–	94	20h	4 - 3
POS102	POS102	–	102	00h	4 - 4
VSSM	3C3 Sleep Address	–	3C3	01h	4 - 5
VSSM	46E8 Sleep Address	–	46E8	00h	4 - 6
MISC	Miscellaneous Output	–	3C2 (write)	n/a	4 - 7
MISC	Miscellaneous Output	–	3CC (read)	n/a	4 - 7
FC	Feature Control	–	3?A (write)	00h	4 - 9
FC	Feature Control	–	3CA (read)	00h	4 - 9
FEAT	Input Status Register 0	–	3C2	n/a	4 - 10
STAT	Input Status Register 1	–	3?A	n/a	4 - 11
–	Pixel Mask	–	3C6	n/a	4 - 12
–	Pixel Address (Read mode)	–	3C7 (write)	n/a	4 - 13
–	DAC State	–	3C7 (read)	n/a	4 - 14
–	Pixel Address (Write mode)	–	3C8	n/a	4 - 15
–	Pixel Data	–	3C9	n/a	4 - 16
PCI00	PCI Device/Vendor ID	–	00	00aoh 1013h	4 - 17
PCI04	PCI Command	–	04	n/a	4 - 18
PCI08	PCI Status	–	08	00h	4 - 19
PCI10	PCI Display Memory Base Address	–	10	0300h 00XXh	4 - 21
PCI14	PCI Relocatable I/O Base Address (CL-GD5430/'40 only)	–	14	000xh	4 - 22
PCI30	PCI Expansion ROM Base Address	–	30	00h	4 - 23
PCI3C	PCI Interrupt Line	–	3C	00h	4 - 24
PCI3C	PCI Interrupt Pin	–	3C	00h	4 - 25

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

4.1 POS94: POS94 Register

I/O Port Address: 94

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	POS102 Access	1
4	Reserved	
3	Reserved	
2	Reserved	
1	Reserved	
0	Reserved	

This register contains the enable bit for POS102. This register is accessible only if CL-GD543X/'4X is configured for 3C3 sleep and for ISA or VESA VL-Bus. This port is not accessible when the device is configured for the PCI bus. This port is not readable. When CL-GD543X/'4X is configured for VESA VL-Bus, it will respond to writes to this register by latching the data, but will not generate LBA# or LRDY#.

Bit	Description
7:6	**Reserved**
5	**POS102 Access:** This bit controls access to POS register 102 if CL-GD543X/'4X is configured for 3C3 sleep and is configured for ISA bus or VESA VL local bus. If this bit is programmed to a '0', POS102 is accessible; if it is programmed to a '1', POS102 is not accessible. In addition, if this bit is programmed to a '0', the Video Subsystem Enable in 3C3 is overridden, and CL-GD543X/'4X remains in Sleep mode.
4:0	**Reserved**

4.2 POS102: POS102 Register

I/O Port Address: 102

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Reserved	
0	Video Subsystem Enable	0

This register contains a Video Subsystem Enable bit. This port is not accessible when the device is configured for the PCI bus. This register is accessible according to the following table.

Bus Configuration	Sleep Address	102 Register Accessibility
ISA, VESA® VL-Bus™	46E8	46E8 [4] = 1
ISA, VESA® VL-Bus™	3C3	POS94[5] = 0

Bit	Description
7:1	**Reserved**
0	**Video Subsystem Enable:** If this bit is programmed to a '1', the CL-GD543X/'4X is enabled and operates normally if the VSE bit in 46E8 or 3C3 is also a '1'. If this bit is programmed to a '0', the CL-GD543X/'4X is disabled.

4.3 VSSM: 3C3 Sleep Address Register

I/O Port Address: 3C3

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Reserved	
0	Video Subsystem Enable	1 (see CF13)

This is the Sleep register when CL-GD543X/'4X is configured for 3C3 sleep. This port is not accessible when the device is configured for the PCI bus. This register is read/write.

Bit	Description
7:1	**Reserved**
0	**Video Subsystem Enable:** If CL-GD543X/'4X is configured for 46E8 sleep, this register is not accessible and this bit has no meaning. If CL-GD543X/'4X is configured for 3C3 sleep, this register is always accessible. **ISA or VESA VL-Bus Configuration:** If this bit is programmed to a '1', the CL-GD543X/'4X is enabled and operates normally if POS102[0] is programmed to a '1' and 94[5] is programmed to a '1'. If this bit is programmed to a '0', the CL-GD543X/'4X is disabled; it will not respond to any I/O accesses except those addressed to 3C3 or 94. It will not respond to any accesses to display memory, but will respond normally to BIOS accesses. The video display is unaffected. For the CL-GD5436 only, the reset state of this bit can be configured. See the description of CF13 in Appendix B9.

4.4 VSSM: 46E8 Sleep Address Register

I/O Port Address: 46E8

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Setup	0
3	Video Subsystem Enable	0
2	Reserved	
1	Reserved	
0	Reserved	

This is the Sleep Address register for an adapter VGA and can be accessed only if the CL-GD543X/'4X is configured for 46E8 Sleep Address. This port is not accessible when the device is configured for the PCI bus. This register is write-only.

Bit	Description
7:5	**Reserved**
4	**Setup:** If this bit is programmed to a '1', the CL-GD543X/'4X is in Setup mode. In Setup mode, the resister at I/O Address 102 is accessible, and the register at 46E8 is accessible. The chip will respond normally to accesses to BIOS, but will not respond to accesses to display memory. If this bit is programmed to a '0', the chip is not in Setup mode and operates normally.
3	**Video Subsystem Enable:** If the CL-GD543X/'4X is not configured for 46E8 Sleep Address, this bit cannot be accessed. If this bit is programmed to a '1', the CL-GD543X/'4X is enabled and operates normally. If this bit is programmed to a '0', the CL-GD543X/'4X is disabled; it will not respond to any I/O accesses except those addressed to 46E8 and 102. It will not respond to any accesses to display memory, but will respond normally to BIOS accesses. The video display is unaffected.
2:0	**Reserved**

4.5 MISC: Miscellaneous Output Register

I/O Port Address: 3C2 (write) 3CC (read)

Index: –

Bit	Description
7	Vertical Sync Polarity
6	Horizontal Sync Polarity
5	Page Select
4	Reserved
3	Clock Select [1]
2	Clock Select [0]
1	Enable Display Memory
0	CRTC I/O Address

This is one of the standard VGA register.

Bit **Description**

7 **Vertical Sync Polarity:** If this bit is programmed to a '0', the Vertical Sync will be a normally LOW signal, going HIGH to indicate the beginning of sync time. If this bit is programmed to a '1', the Vertical Sync will be a normally HIGH signal, going LOW to indicate the beginning of sync time. Refer to Chapter 9 for the description of GRE for information regarding Static Sync signals.

6 **Horizontal Sync Polarity:** If this bit is programmed to a '0', the Horizontal Sync will be a normally LOW signal, going HIGH to indicate the beginning of sync time. If this bit is programmed to a '1', the Horizontal Sync will be a normally HIGH signal, going LOW to indicate the beginning of sync time. Refer to Chapter 9 for the description of GRE for information regarding Static Sync signals.

For some monitors, the polarity of Vertical and Horizontal Sync indicate the number of scanlines per frame as summarized below:

MISC[7]	MISC[6]	Vertical Size	Vertical Total
0 (+)	0 (+)	Reserved	Reserved
0 (+)	1 (-)	400	414
1 (-)	0 (+)	350	362
1 (-)	1 (-)	480	496

4.5 MISC: Miscellaneous Output Register *(cont.)*

Bit **Description**

5 **Page Select:** This bit affects the meaning of the least-significant bit of the display memory address when in Even/Odd modes (SR4[2]=1). If this bit is programmed to a '0', only odd memory locations are selected. If this bit is programmed to a '1', only even memory locations are selected.

NOTE: This bit is effective in modes 6, D, E, 11, and 12. This bit is ignored if Chain (GR6[1]) or Chain4 (SR4[3]) are enabled.

4 **Reserved**

3:2 **Clock Select [1:0]:** This 2-bit field is used to choose among the four VCLK frequencies, as shown in the following table:

EDCLK	MISC[3]	MISC[2]	VCLK Source	Default Frequency
1	0	0	VCLK0	25.180 MHz
1	0	1	VCLK1	28.325 MHz
1	1	0	VCLK2	41.165 MHz
1	1	1	VCLK3	36.082 MHz
0	1	X	DCLK pin (DAC and CRTC counters)	
0	0	X	DCLK pin (DAC only)	

NOTE: Refer to Appendix B8, *Dual-Frequency Synthesizer*, for programming other VCLK frequencies than those in the table above, and for choosing additional VCLK sources.

1 **Enable Display Memory:** If this bit is programmed to a '0', the CL-GD543X/'4X will not respond to any accesses to display memory. If this bit is programmed to a '1', the CL-GD543X/'4X will respond normally to accesses to display memory.

0 **CRTC I/O Address:** This bit selects I/O addresses for either Monochrome or Color mode. The affected addresses are summarized in the table below:

MISC[0]	ISR/FC	CRTC Index	CRTC Data	Mode
0	3BA	3B4	3B5	Monochrome
1	3DA	3D4	3D5	Color

4.6 FC: Feature Control Register

I/O Port Address: 3?A (Write) 3CA (Read)

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	VSYNC Control	0
2	Reserved	
1	Reserved	
0	Reserved	

This is one of the original IBM PC registers. Nearly all the bits are no longer used.

Bit	Description
7:4	**Reserved**
3	**VSYNC Control:** If this bit is programmed to a '1', VSYNC is logically OR'ed with Display Enable (an internal signal) prior to going to the VSYNC pin. If this bit is programmed to a '0', VSYNC is unchanged.
2:0	**Reserved**

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

4.7 FEAT: Input Status Register 0

I/O Port Address: 3C2

Index: –

Bit	Description
7	Interrupt Pending
6	Reserved
5	Reserved
4	DAC Sensing
3	Reserved
2	Reserved
1	Reserved
0	Reserved

The bits in this read-only register are nearly all undefined.

Bit	Description
7	**Interrupt Pending:** If this bit is a '1', an interrupt request is pending. If this bit is a '0', no interrupt is pending. See the description in Chapter 6 of CR11 for more information regarding the CL-GD543X/'4X interrupt system.
6:5	**Reserved**
4	**DAC Sensing:** This read-only bit is used by the Cirrus Logic BIOS for Monitor sensing.
3:0	**Reserved**

4.8 STAT: Input Status Register 1

I/O Port Address: 3?A

Index: –

Bit	Description
7	Reserved
6	Reserved
5	Diagnostic [1]
4	Diagnostic [0]
3	Vertical Retrace
2	Reserved
1	Reserved
0	Display Enable

This read-only register contains some status bits.

Bit **Description**

7:6 **Reserved**

5:4 **Diagnostic [1:0]:** These bits follow two of eight outputs of the Attribute Controller. The selection is made according to AR12[5:4] (Color Plane Enable register) as indicated in the following table:

AR12[5]	AR12[4]	STAT[5]	STAT[4]
0	0	P[2]	P[0]
0	1	P[5]	P[4]
1	0	P[3]	P[1]
1	1	P[7]	P[6]

These bits can reflect the Input Data on P[7:0]. This occurs only if P[7:0] are inputs as set by CR1A[3:2].

3 **Vertical Retrace:** A '1' indicates that vertical retrace is in progress.

2:1 **Reserved**

0 **Display Enable:** If this bit is read as a '0', video is being serialized and displayed. If this bit is read as a '1', vertical or horizontal blanking is active.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

4.9 Pixel Mask Register

I/O Port Address: 3C6

Index: –

Bit	Description
7	Pixel Mask [7]
6	Pixel Mask [6]
5	Pixel Mask [5]
4	Pixel Mask [4]
3	Pixel Mask [3]
2	Pixel Mask [2]
1	Pixel Mask [1]
0	Pixel Mask [0]

The bits in this register form the Pixel Mask for the palette DAC. This is typically programmed to all ones by the Cirrus Logic BIOS. The same address is used to access the HDR (Hidden DAC register), described in Chapter 9, *Extension Registers*.

Bit	Description
7:0	**Pixel Mask [7:0]:** This field is the Pixel Mask for the palette DAC. If a bit in this field is programmed to a '0', the corresponding bit in the pixel data will be ignored in looking up an entry in the LUT (lookup table).

4.10 Pixel Address Register (Read Mode, Write-only)

I/O Port Address: 3C7

Index: –

Bit	Description
7	Pixel Address (Read Mode) [7]
6	Pixel Address (Read Mode) [6]
5	Pixel Address (Read Mode) [5]
4	Pixel Address (Read Mode) [4]
3	Pixel Address (Read Mode) [3]
2	Pixel Address (Read Mode) [2]
1	Pixel Address (Read Mode) [1]
0	Pixel Address (Read Mode) [0]

The bits in this write-only register form the Pixel Address (Read mode) for the palette DAC. This is used to specify the entry in the LUT that is to be read.

Bit	Description
7:0	**Pixel Address (Read Mode) [7:0]:** This field is the Pixel Address (Read mode) for the VLUT (video lookup table). This address is incremented at the conclusion of every third read of the Pixel Data register.

4.11 DAC State Register (Read Mode)

I/O Port Address: 3C7

Index: –

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	DAC State [1]
0	DAC State [0]

The bits in this read-only register indicate whether a read or a write occurred last to the LUT.

Bit	Description
7:2	**Reserved**
1:0	**DAC State [1:0]:** This field indicates whether the Pixel Address Read register or the Pixel Address Write register was accessed last. The two bits will always be the same. If they are '0,0', a write operation is in progress. If they are '1,1', a read operation is in progress.

4.12 Pixel Address Register (Write Mode)

I/O Port Address: 3C8

Index: –

Bit	Description
7	Pixel Address (Write Mode) [7]
6	Pixel Address (Write Mode) [6]
5	Pixel Address (Write Mode) [5]
4	Pixel Address (Write Mode) [4]
3	Pixel Address (Write Mode) [3]
2	Pixel Address (Write Mode) [2]
1	Pixel Address (Write Mode) [1]
0	Pixel Address (Write Mode) [0]

The bits in this register form the Pixel Address (Write Mode) for the palette DAC. This is used to specify the entry in the LUT that is to be written.

Bit	Description
7:0	**Pixel Address (Write Mode) [7:0]:** This field is the Pixel Address (Write mode) for the VLUT. This address is incremented at the conclusion of every third write to the Pixel Data register.

4.13 Pixel Data Register

I/O Port Address: 3C9

Index: –

Bit	Description
7	Pixel Data [7]
6	Pixel Data [6]
5	Pixel Data [5]
4	Pixel Data [4]
3	Pixel Data [3]
2	Pixel Data [2]
1	Pixel Data [1]
0	Pixel Data [0]

This is the Pixel Data register for the palette DAC.

Bit	Description
7:0	**Pixel Data [7:0]:** This field is the Pixel Data for the palette DAC. This is a read/write register. Prior to writing to this register, 3C8 is written with the first or only pixel address. Then three values, corresponding to the RED, GREEN, and BLUE values for the pixel are written to this address. Following the third write, the values are actually transferred to the LUT, and the Pixel Address is incremented in case new values for the next pixel address are to be written. Prior to reading from this register, 3C7 is written with the first or only pixel address. Then three values, corresponding to the RED, GREEN, and BLUE values for the pixel may be read from this address. Following the third read, the Pixel Address is incremented in case the value for the next pixel address are to be read.

4.14 PCI00: PCI Device/Vendor ID Register

PCI Configuration Address: 00

Index: –

Bit	Description	Reset Value
31	Device ID [15]	0
30	Device ID [14]	0
29	Device ID [13]	0
28	Device ID [12]	0
27	Device ID [11]	0
26	Device ID [10]	0
25	Device ID [9]	0
24	Device ID [8]	0
23	Device ID [7]	X
22	Device ID [6]	X
21	Device ID [5]	X
20	Device ID [4]	X
19	Device ID [3]	X
18	Device ID [2]	X
17	Device ID [1]	X
16	Device ID [0]	X
15	Vendor ID [15]	0
14	Vendor ID [14]	0
13	Vendor ID [13]	0
12	Vendor ID [12]	1
11	Vendor ID [11]	0
10	Vendor ID [10]	0
9	Vendor ID [9]	0
8	Vendor ID [8]	0
7	Vendor ID [7]	0
6	Vendor ID [6]	0
5	Vendor ID [5]	0
4	Vendor ID [4]	1
3	Vendor ID [3]	0
2	Vendor ID [2]	0
1	Vendor ID [1]	1
0	Vendor ID [0]	1

This is the Device/Vendor ID required for PCI compliance. This register is accessible and effective only if CL-GD543X/'4X is configured for PCI bus.

Bit	Description
31:16	**Device ID [15:0]:** This read-only field contains the device identifier assigned by Cirrus Logic. This field will always return the value 00A0h for the CL-GD5430, 00A8h for the CL-GD5434, 00ACh for the CL-GD5436, and 00A0h for the CL-GD5440.
15:0	**Vendor ID [15:0]:** This read-only field contains the Vendor ID assigned to Cirrus Logic. The value returned is 1013h.

4.15 PCI04: PCI Command Register

PCI Configuration Address: 04

Index: –

Bit	Description
15	Reserved
14	Reserved
13	Reserved
12	Reserved
11	Reserved]
10	Reserved
9	Reserved
8	Reserved
7	Reserved
6	Reserved
5	Enable DAC Shadowing
4	Reserved
3	Reserved]
2	Reserved
1	Enable Memory Accesses
0	Enable I/O Accesses

This is the PCI Command register. This register is accessible and effective only if CL-GD543X/'4X is configured for PCI bus.

Bit	Description
15:6	**Reserved:** These bits are reserved and must be programmed to a '0'.
5:	**Enable DAC Shadowing:** If this bit is programmed to a '1', PCI DAC Shadowing is enabled. Write accesses to CL-GD543X/'4X will be executed in the sense that the data are latched in the appropriate register or the palette. However, CL-GD543X/'4X will not acknowledge the access. Read accesses will be executed normally. If MD60 is pulled down, it will take precedence over this bit.
4:2	**Reserved:** These bits *must* be programmed to a '0'.
1	**Enable Memory Accesses:** If this bit is programmed to a '1', memory accesses are enabled on CL-GD543X/'4X. If this bit is programmed to a '0', memory accesses are not enabled on CL-GD543X/'4X. Memory-mapped I/O access is controlled with this bit.
0	**Enable I/O Accesses:** If this bit is programmed to a '1', I/O accesses are enabled on CL-GD543X/'4X. If this bit is programmed to a '0', I/O accesses are not enabled on CL-GD543X/'4X. I/O accesses to PCI registers are always enabled.

4.16 PCI04: PCI Status Register

PCI Configuration Address: 04

Index: –

Bit	Description	Reset State
31	Reserved	
30	Reserved	
29	Reserved	
28	Reserved	
27	Reserved	
26	DEVSEL# Timing [1]	0
25	DEVSEL# Timing [0]	0
24	Reserved	
23	Reserved	
22	Reserved	
21	Reserved	
20	Reserved	
19	Reserved	
18	Reserved	
17	Reserved	
16	Reserved	

This is the PCI Status register. This register is accessible and effective only if CL-GD543X/ '4X is configured for PCI bus.

Bit	Description
31:27	**Reserved**
26:25	**DEVSEL# Timing [1:0]:** This read-only field always returns the value '00' to indicate fast DEVSEL timing.
24:16	**Reserved**

4.17 PCI08: PCI Class Code Register

PCI Configuration Address: 08

Index: –

Bit	Description	Reset Value
31	Class Code [23]	0
30	Class Code [22]	0
29	Class Code [21]	0
28	Class Code [20]	0
27	Class Code [19]	0
26	Class Code [18]	0
25	Class Code [17]	1
24	Class Code [16]	1
23	Class Code [15]	0
22	Class Code [14]	0
21	Class Code [13]	0
20	Class Code [12]	0
19	Class Code [11]	0
18	Class Code [10]	0
17	Class Code [9]	0
16	Class Code [8]	0
15	Class Code [7]	0
14	Class Code [6]	0
13	Class Code [5]	0
12	Class Code [4]	0
11	Class Code [3]	0
10	Class Code [2]	0
9	Class Code [1]	0
8	Class Code [0]	0
7	Revision ID [7]	X
6	Revision ID [6]	X
5	Revision ID [5]	X
4	Revision ID [4]	X
3	Revision ID [3]	X
2	Revision ID [2]	X
1	Revision ID [1]	X
0	Revision ID [0]	X

This register contains the Class Code required for PCI 2.0 compliance. This register is accessible and effective only if CL-GD543X/'4X is configured for PCI bus.

Bit	Description
31:8	**Class Code [23:0]:** This read-only field contains the device identifier assigned to a VGA compatible controller. In particular, the Base Class is 03, the Sub-Class is 00, and the Programming Interface is 00.
7:0	**Revision ID [7:0]:** This read-only field contains a revision ID assigned by Cirrus Logic. No application program should ever take any action based on the contents of this field.

4.18 PCI10: PCI Display Memory Base Address Register

PCI Configuration Address: 10h

Index: –

Bit	Description	Reset Value
31	Display Memory Base Address	
30	Display Memory Base Address	
29	Display Memory Base Address	
28	Display Memory Base Address	
27	Display Memory Base Address	
26	Display Memory Base Address	
25	Display Memory Base Address	
24	Display Memory Base Address	
23:4	Reserved	
3	Prefetchable (CL-GD5430 only)	1
2:1	Reserved	
0	Memory/IO Indicator	0

This 32-bit register contains the Base Address of display memory when the CL-GD543X/'4X is configured for PCI bus. This register is accessible and effective only if CL-GD543X/'4X is configured for PCI bus.

Bit	Description
31:24	**Display Memory Base Address [31:24]:** This field contains the base address of the contiguous 16-Mbyte Memory Block reserved for CL-GD5434. The memory will actually occupy the first 4 Mbytes of this block. For the CL-GD5436, all 16 Mbytes will be addressable, as four byte-swapping apertures. See the description of CF13 in Appendix B9.
23:4	**Reserved**
3	**Prefetchable (CL-GD5430/'40 only):** This bit is always read as a '1' to indicate the CL-GD5430 and CL-GD5440 meet the appropriate PCI criteria.
2:1	**Reserved**
0	**Memory/IO Indicator:** This read-only field is used to indicate the type of address space requested. A '0' value indicates memory.

4.19 PCI14: PCI Relocatable I/O Base Address Register ('30/'36/'40 only)

PCI Configuration Address: 14h

Index: –

Bit	Description	Reset Value
31:16	Reserved	
15:10	I/O Base Address	
9:1	Reserved	
0	Enable Offset	$\overline{CF3}$

This 32-bit register contains the Base Address of the VGA I/O when the CL-GD543X/'4X is configured for PCI bus. This register is accessible and effective only if CL-GD543X/'4X is configured for PCI bus.

Bit	Description
31:16	**Reserved**
15:10	**I/O Base Address (CL-GD5430/'40 only):** This field contains the base for the relocatable 512-byte I/O address range. These bits correspond to address bits 15:10. This offset, combined with the linear address offset, provides hardware hooks for multiple VGA controllers in a single PCI system.
9:1	**Reserved**
0	**Enable Offset:** If a pull-down is installed on MD51, this bit will be read as a '1' and relocatable I/O addressing will be enabled. If no pull-down is installed on MD51, this bit will be read as '0' and relocatable I/O is effectively disabled.

4.20 PCI30: PCI Expansion ROM Base Address Enable Register

PCI Configuration Address: 30

Index: –

Bit	Description
31	Expansion ROM Base Address
30	Expansion ROM Base Address
29	Expansion ROM Base Address
28	Expansion ROM Base Address
27	Expansion ROM Base Address
26	Expansion ROM Base Address
25	Expansion ROM Base Address
24	Expansion ROM Base Address
23:1	Reserved
0	EROM Enable

This 32-bit register contains the Base Address of EPROM (BIOS) Memory when the CL-GD543X/'4X is configured for PCI bus. This register is accessible and effective only if CL-GD543X/'4X is configured for PCI bus.

Bit	Description
31:24	**Expansion ROM Base Address [31:24]:** This field contains the base address of the contiguous 16-Mbyte Memory Block reserved for CL-GD543X/'4X during POST. This field is programmed by the PCI system BIOS. During POST time, the PCI BIOS shadows the VGA BIOS through the programmed address range. In addition, it copies the run-time portion of the VGA BIOS to C000:0. This sequence happens only once, and therefore after POST all VGA BIOS calls are routed to the system memory.
23:1	**Reserved**
0	**EROM Enable:** When this bit is programmed to a '1'. the VGA BIOS at C000:0 is enabled and display memory is disabled (CAS0* is forced high). When this bit is programmed to a '0', the VGA BIOS at C000:0 is disabled.

4.21 PCI3C: PCI Interrupt Line Register

PCI Configuration Address: 3C

Index: –

Bit	Description
7	PCI Interrupt Line [7]
6	PCI Interrupt Line [6]
5	PCI Interrupt Line [5]
4	PCI Interrupt Line [4]
3	PCI Interrupt Line [3]
2	PCI Interrupt Line [2]
1	PCI Interrupt Line [1]
0	PCI Interrupt Line [0]

This register is used to contain an interrupt pointer. It has no direct effect on the CL-GD543X/'4X chip. This register is accessible and effective only if CL-GD543X/'4X is configured for PCI bus.

Bit	Description
7:0	**PCI Interrupt Line [7:0]:** This field contains an 8-bit value that has no direct effect on the CL-GD543X/'4X chip. It is used to transfer an interrupt pointer from the PCI system BIOS to the CL-GD543X/'4X VGA BIOS.

4.22 PCI3C: PCI Interrupt Pin Register

PCI Configuration Address: 3C

Index: –

Bit	Description	Reset Value
15	Interrupt Pin [7]	0
14	Interrupt Pin [6]	0
13	Interrupt Pin [5]	0
12	Interrupt Pin [4]	0
11	Interrupt Pin [3]	0
10	Interrupt Pin [2]	0
9	Interrupt Pin [1]	0
8	Interrupt Pin [0]	$\overline{CF14}$

This is the PCI Interrupt Pin register. This register is accessible and effective only if CL-GD543X/'4X is configured for PCI bus.

Bit	Description
15:8	**Interrupt Pin [7:0]:** If a pull-down resistor is installed on MD62, this read-only field contains the value '01'. This is an indication that the CL-GD543X/'4X Interrupt Request pin is connected to the INTA# pin. If no pull-down resistor is installed on MD62, this read-only field contains the value '00'.

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VGA Sequencer Registers

5. VGA SEQUENCER REGISTERS

The CL-GD543X/'4X VGA Sequencer registers are summarized in the following table. Please note that there are Extension registers that are accessed using the VGA Sequencer ports.

VGA Sequencer Registers Quick Reference

Abbreviation	Register Name	Index	Port	Page
SRX	Sequencer Index	–	3C4	5 - 3
SR0	Reset	0	3C5	5 - 4
SR1	Clocking Mode	1	3C5	5 - 5
SR2	Plane Mask	2	3C5	5 - 7
SR3	Character Map Select	3	3C5	5 - 8
SR4	Memory Mode	4	3C5	5 - 10

5.1 SRX: Sequencer Index Register

I/O Port Address: 3C4

Index: –

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Sequencer Index [4]
3	Sequencer Index [3]
2	Sequencer Index [2]
1	Sequencer Index [1]
0	Sequencer Index [0]

This register is used to specify the register in the sequencer block to be accessed by the next I/O read or write to Address 3C5. Indices greater than five point to the registers that are defined in Chapter 9, *Extension Registers*.

Bit	Description
7:5	**Reserved**
4:0	**Sequencer Index [4:0]:** This field selects the register to be accessed with the next I/O read or I/O write to 3C5.

5.2 SR0: Reset Register

I/O Port Address: 3C5

Index: 0

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Synchronous Reset	1
0	Asynchronous Reset	1

This register is used to reset the Sequencer. These bits are for compatibility only and never need to be used in the CL-GD543X/'4X.

Bit	Description
7:2	**Reserved**
1	**Synchronous Reset:** If this bit is programmed to a '0', the Sequencer will be cleared and halted. This disables screen refresh and display memory refresh. If this bit is programmed to a '1', the Sequencer will operate normally if SR0[0] is a '1'.
0	**Asynchronous Reset:** If this bit is programmed to a '0', the Sequencer will be cleared and halted. In addition, SR3 will be cleared. If this bit is programmed to a '1', the Sequencer will operate normally if SR0[1] is a '1'.

5.3 SR1: Clocking Mode Register

I/O Port Address: 3C5

Index: 1

Bit	Description
7	Reserved
6	Reserved
5	Full Bandwidth
4	Shift and Load 32
3	Dot Clock ÷ 2
2	Shift and Load 16
1	Reserved
0	8/9 Dot Clock

This register is used to control some miscellaneous functions in the Sequencer.

Bit	Description
7:6	**Reserved**
5	**Full Bandwidth:** If this bit is programmed to a '1', screen refresh will stop. This allows the CPU to use nearly 100 percent of the display memory bandwidth. HSYNC and VSYNC will continue normally and display memory refresh will continue. BLANK* will go active and stay active. If this bit is programmed to a '0', the CL-GD543X/'4X will operate normally.
4	**Shift and Load 32:** This bit, in conjunction with bit 2 of this register, controls the Display Data Shifters in the Graphics Controller according to the following table:
3	**Dot Clock ÷ 2:** If this bit is programmed to a '1', the VCLK is divided by two to generate DCLK. This is used for low-resolution Video modes such as 0, 1, 4, 5, and D. If this bit is programmed to a '0', the Master Clock is not divided by two.

SR1[4]	SR1[2]	Data Shifters Loaded
0	0	Every Character Clock
0	1	Every 2nd Character Clock
1	x	Every 4th Character Clock

5.3 SR1: Clocking Mode Register *(cont.)*

Bit	Description
2	**Shift and Load 16:** See the description of bit 4 of this register.
1	**Reserved**
0	**8/9 Dot Clock:** If this bit is programmed to a '1', DCLK is divided by eight to generate character clock. If this bit is programmed to a '0', DCLK is divided by nine to generate character clock. This is used for 720 x 350 and 720 x 400 resolution text (A.N.) modes.

5.4 SR2: Plane Mask Register

I/O Port Address: 3C5

Index: 2

Bit	Description
7	Enable Writing Pixel 7
6	Enable Writing Pixel 6
5	Enable Writing Pixel 5
4	Enable Writing Pixel 4
3	Map 3 Enable/Enable Writing Pixel 3
2	Map 2 Enable/Enable Writing Pixel 2
1	Map 1 Enable/Enable Writing Pixel 1
0	Map 0 Enable/Enable Writing Pixel 0

This register is used to enable or disable writing to the four planes of display memory. If Extended Write modes 4 or 5 are selected, or, if Write mode 1 is selected and GRB[1] = 1, this register is redefined as controlling the writing of up to eight pixels.

Bit	Description
7:4	**Reserved:** These four bits are reserved if Extended Write modes 4 and 5 are disabled. This would be the case for VGA-compatibility modes.
3:0	**Map Enable [3:0]:** These four bits are used to individually control whether Bit Planes 3:0 will be written with Write modes 0 through 3.
7:0	**Enable Writing Pixel [7:0]:** These eight bits are used to individually control whether Pixels 7:0 will be written if Extended Write modes 4 or 5 are selected, or if Write mode 1 is selected and GRB[2] = 1. Programming a '1' enables the corresponding pixel. This eight-bit field is also used as a write protect for the BitBLT engine (see Appendix D8).

5.5 SR3: Character Map Select Register

I/O Port Address: 3C5

Index: 3

Bit	Description
7	Reserved
6	Reserved
5	Secondary Map Select [0]
4	Primary Map Select [0]
3	Secondary Map Select [2]
2	Secondary Map Select [1]
1	Primary Map Select [2]
0	Primary Map Select [1]

This register is used to specify the primary and secondary character sets (fonts). This is applicable to text modes only.

Bit **Description**

7:6 **Reserved**

5, 3:2 **Secondary Map Select:** These three bits select the Secondary Character Map according to the following table:

SR3[5]	SR3[3]	SR3[2]	Map	Offset
0	0	0	0	0K
0	0	1	1	16K
0	1	0	2	32K
0	1	1	3	48K
1	0	0	4	8K
1	0	1	5	24K
1	1	0	6	40K
1	1	1	7	56K

5.5 SR3: Character Map Select Register *(cont.)*

Bit **Description**

4, 1:0 **Primary Map Select:** These three bits select the Primary Character Map according to the following table:

SR3[4]	SR3[1]	SR3[0]	Map	Offset
0	0	0	0	0K
0	0	1	1	16K
0	1	0	2	32K
0	1	1	3	48K
1	0	0	4	8K
1	0	1	5	24K
1	1	0	6	40K
1	1	1	7	56K

NOTES:

1) In text and video modes, the ASCII text character is stored in Plane 0, the attribute is stored in Plane 1, and the font is stored in Plane 2.
2) Bit 3 of the Attribute Byte normally controls the intensity of the foreground color. This bit may be redefined to be a switch between character sets, allowing 512 displayable characters. This switch is enabled whenever there is a difference between the values of the Primary Map Select and Secondary Map Select, and SR4[1] is a '1'.
3) The format of the Plane 2 Font Address bits 15:0 is:
   F2 F1 F0 C7 C6 C5 C4 C3 C2 C1 C0 R4 R3 R2 R1 R0,
   where F[2:0] is the Character Map Select, C[7:0] is the ASCII character, and R[4:0] is the Character Row (scanline in the character cell).

5.6 SR4: Memory Mode Register

I/O Port Address: 3C5

Index: 4

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Chain-4
2	Odd/Even
1	Extended Memory
0	Reserved

This register is used to control some miscellaneous functions in the Sequencer.

Bit	Description
7:4	**Reserved**
3	**Chain-4:** If this bit is programmed to a '1', A0 provides Plane Select bit 0, and A1 provides Plane Select bit 1. This has an effect similar to Odd/Even mode except that both A1 and A0 are used. This bit takes priority over SR4[2] (Odd/Even) and GR5[4]. There is not a separate bit in the Graphics Controller to select Chain4 as is the case with the Odd/Even bit. The Graphics Controller Read Map register (GR4) is ignored when this bit is a '1'.
2	**Odd/Even:** If this bit is programmed to a '0', the Sequencer will be put into Odd/Even mode. Even CPU addresses will access Planes 0 and 2; odd CPU addresses will access Planes 1 and 3. This bit must be programmed to a '0' for text modes. The value of this bit must track GR5[4] (Odd/Even). The values will be opposite.
1	**Extended Memory:** If this bit is programmed to a '0', the effective memory size will be 64K, regardless of the memory actually installed. EGA modes require this to be the case. If this bit is programmed to a '1', the effective memory size will be equal to the actual memory installed.
0	**Reserved**

CRT Controller Registers

6. CRT CONTROLLER REGISTERS

The CL-GD543X/'4X VGA CRT Controller registers are listed below in the quick reference table. Please note there are Extension registers that are accessed using the VGA CRT Controller Ports.

While reading this chapter, refer to Figure 6–1 and Table 6–1 for a detailed summary of CRTC registers.

CRT Controller Registers Quick Reference

Abbreviation	Register Name	Index	Port	Page
CRX	CRTC Index	–	3?4	6 - 4
CR0	Horizontal Total	0	3?5	6 - 7
CR1	Horizontal Display End	1	3?5	6 - 8
CR2	Horizontal Blanking Start	2	3?5	6 - 9
CR3	Horizontal Blanking End	3	3?5	6 - 10
CR4	Horizontal Sync Start	4	3?5	6 - 12
CR5	Horizontal Sync End	5	3?5	6 - 13
CR6	Vertical Total	6	3?5	6 - 15
CR7	Overflow	7	3?5	6 - 16
CR8	Screen A Preset Row-Scan	8	3?5	6 - 17
CR9	Character Cell Height	9	3?5	6 - 18
CRA	Text Cursor Start	A	3?5	6 - 19
CRB	Text Cursor End	B	3?5	6 - 20
CRC	Screen Start Address High	C	3?5	6 - 21
CRD	Screen Start Address Low	D	3?5	6 - 22
CRE	Text Cursor Location High	E	3?5	6 - 23
CRF	Text Cursor Location Low	F	3?5	6 - 24
CR10	Vertical Sync Start	10	3?5	6 - 25
CR11	Vertical Sync End	11	3?5	6 - 26
CR12	Vertical Display End	12	3?5	6 - 27
CR13	Offset	13	3?5	6 - 28
CR14	Underline Row Scanline	14	3?5	6 - 29
CR15	Vertical Blank Start	15	3?5	6 - 30
CR16	Vertical Blank End	16	3?5	6 - 31

CRT Controller Registers Quick Reference *(cont.)*

Abbreviation	Register Name	Index	Port	Page
CR17	Mode Control	17	3?5	6 - 32
CR18	Line Compare	18	3?5	6 - 34
CR22	Graphics Data Latches Readback	22	3?5	6 - 35
CR24	Attribute Controller Toggle Readback	24	3?5	6 - 36
CR26	Attribute Controller Index Readback	26	3?5	6 - 37

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

WARNING: The timing registers should never be programmed by any application program. Incorrect timing can cause permanent damage to some monitors. The correct way to program a Video mode is to use the appropriate INTI0. See Chapter 10, *VGA BIOS*, for further information.

6.1 CRX: CRTC Index Register

I/O Port Address: 3?4

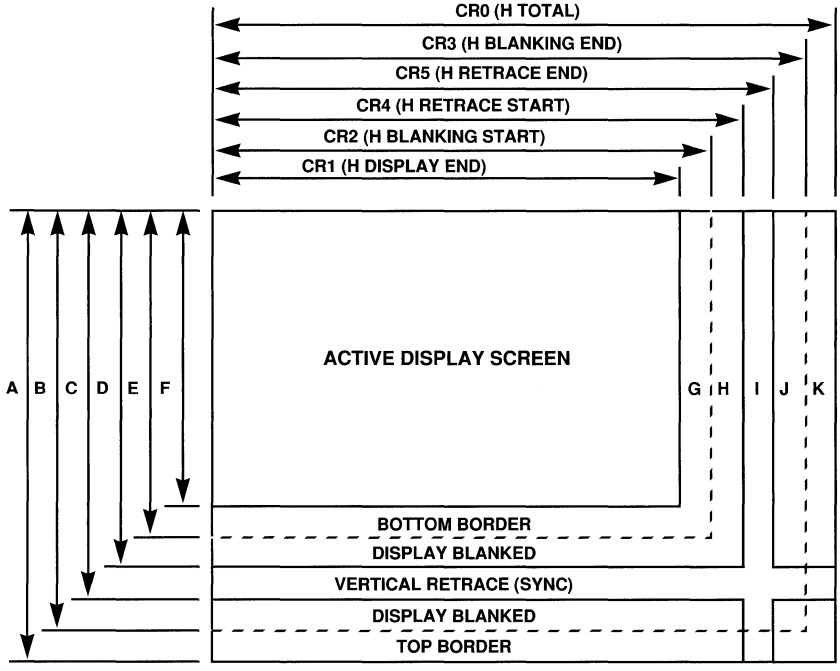
Index: –

Bit	Description
7	Reserved
6	Reserved
5	CRTC Index [5]
4	CRTC Index [4]
3	CRTC Index [3]
2	CRTC Index [2]
1	CRTC Index [1]
0	CRTC Index [0]

This register is used to specify the register in the CRTC Controller block to be accessed by the next I/O read or I/O write to Address 3?5. The registers at indices greater than 18h (excepting CR22, CR24, and CR26) are described in Chapter 9, *Extension Registers*.

Bit	Description
7:6	**Reserved**
5:0	**CRTC Index [5:0]:** This value points to the register to be accessed in the next I/O read or I/O write to Address 3?5. **NOTE:** Registers above 18 were never documented by IBM.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.



A - CR6 (V TOTAL)
B - CR16 (V BLANKING END)
C - CR11 (V RETRACE END)
D - CR10 (V RETRACE START)
E - CR15 (V BLANKING START)
F - CR12 (V DISPLAY END)
G - RIGHT BORDER
H - DISPLAY BLANKED
I - HORIZONTAL RETRACE (SYNC)
J - DISPLAY BLANKED
K - LEFT BORDER

Figure 6–1. CRTC Timing Registers

The Extension and Overflow bits are organized by parameter and bit position in the following table:

Table 6–1. Summary of CRTC Timing Registers[a]

Parameter/Bit	9	8	7	6	5	4:0
H Total			CR0[7]	CR0[6]	CR0[5]	CR0[4:0]
H Display End			CR1[7]	CR1[6]	CR1[5]	CR1[4:0]
H Blank Start			CR2[7]	CR2[6]	CR2[5]	CR2[4:0]
H Blank End			**CR1A[5]**	**CR1A[4]**	CR5[7]	CR3[4:0]
H Sync Start			CR4[7]	CR4[6]	CR4[5]	CR4[4:0]
H Sync End						CR5[4:0]
V Total	CR7[5]	CR7[0]	CR6[7]	CR6[6]	CR6[5]	CR6[4:0]
V Sync Start	CR7[7]	CR7[2]	CR10[7]	CR10[6]	CR10[5]	CR10[4:0]
V Sync End						CR11[3:0]
V Display End	CR7[6]	CR7[1]	CR12[7]	CR12[6]	CR12[5]	CR12[4:0]
V Blank Start	CR9[5]	CR7[3]	CR15[7]	CR15[6]	CR15[5]	CR15[4:0]
V Blank End	**CR1A[7]**	**CR1A[6]**	CR16[7]	CR16[6]	CR16[5]	CR16[4:0]
Line Compare	CR9[6]	CR7[4]	CR18[7]	CR18[6]	CR18[5]	CR18[4:0]
Offset		**CR1B[4]**	CR13[7]	CR13[6]	CR13[5]	CR13[4:0]

a. Bits shown in **bold** text are extensions.

The Extension and Overflow bits for the Screen Start A value are shown in the following table.

Table 6–2. Screen Start A Extensions[a]

19	18:17	16	15:8	7:0
CR1D[7] ('34/'36 only)	**CR1B[3:2]**	**CR1B[0]**	CRC[7:0]	CRD[7:0]

a. Bits shown in **bold** text are extensions.

6.2 CR0: Horizontal Total Register

I/O Port Address: 3?5

Index: 0

Bit	Description
7	Horizontal Total [7]
6	Horizontal Total [6]
5	Horizontal Total [5]
4	Horizontal Total [4]
3	Horizontal Total [3]
2	Horizontal Total [2]
1	Horizontal Total [1]
0	Horizontal Total [0]

This register is used to specify the total number of character clocks per horizontal period.

Bit	Description
7:0	**Horizontal Total [7:0]:** This 8-bit field specifies the total number of character clocks per horizontal period. The Character Clock (derived from the VCLK according to the character width) is counted in the Character Counter. The value of the Character Counter is compared with the value in this register to provide the basic horizontal timing. All horizontal and vertical timing is eventually derived from this register. The value in the register is 'Total number of character times minus five'. Figure 6–1 indicates the way the horizontal and vertical timing is defined. The horizontal timing is calculated in terms of character clock periods and the vertical timing is calculated in terms of horizontal periods. Table 6–1 indicates how the various timing registers are extended.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.3 CR1: Horizontal Display End Register

I/O Port Address: 3?5

Index: 1

Bit	Description
7	Horizontal Display End [7]
6	Horizontal Display End [6]
5	Horizontal Display End [5]
4	Horizontal Display End [4]
3	Horizontal Display End [3]
2	Horizontal Display End [2]
1	Horizontal Display End [1]
0	Horizontal Display End [0]

This register is used to specify the number of character clocks during horizontal display time.

Bit	Description
7:0	**Horizontal Display End [7:0]:** This register specifies the number of character clocks during horizontal display time. For text modes, this is the number of characters; for graphics modes, this is the number of pixels-per-scanline divided by the number of pixels-per-character clock (usually 8). The value in the register is the number of character clocks minus one. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.4 CR2: Horizontal Blanking Start Register

I/O Port Address: 3?5

Index: 2

Bit	Description
7	Horizontal Blanking Start [7]
6	Horizontal Blanking Start [6]
5	Horizontal Blanking Start [5]
4	Horizontal Blanking Start [4]
3	Horizontal Blanking Start [3]
2	Horizontal Blanking Start [2]
1	Horizontal Blanking Start [1]
0	Horizontal Blanking Start [0]

This register is used to specify the Character Count where Horizontal Blanking starts.

Bit	Description
7:0	**Horizontal Blanking Start [7:0]:** The contents of this register specify the Character Count where Horizontal Blanking starts. For text modes, this is the number of characters; for graphics modes, this is the number of pixels-per-scanline divided by the number of pixels-per-character clock. The value programmed into CR2 must always be larger than the value programmed into CR1. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.5 CR3: Horizontal Blanking End Register

I/O Port Address: 3?5

Index: 3

Bit	Description
7	Compatible Read
6	Display Enable Skew [1]
5	Display Enable Skew [0]
4	Horizontal Blanking End [4]
3	Horizontal Blanking End [3]
2	Horizontal Blanking End [2]
1	Horizontal Blanking End [1]
0	Horizontal Blanking End [0]

This register is used to determine the width of the Horizontal Blanking Period. In addition, this register controls Display Enable Skew and access to CR10 and CR11.

Bit **Description**

7 **Compatible Read:** If this bit is programmed to '0', registers CR10 and CR11 are write-only registers. If this bit is programmed to '1', registers CR10 and CR11 are read/write registers.

6:5 **Display Enable Skew [1:0]:** This 2-bit field is used to specify the number of Character Clocks that display enable is to be delayed from Horizontal Total. This is necessary to compensate for the accesses of the Character Code and Attribute Byte, the accesses of the font, etc. The following table indicates the coding of CR3[6:5]:

CR3[6]	CR3[5]	Skew	Note
0	0	0	
0	1	1	Typical setting
1	0	2	
1	1	3	

NOTE: If the skew is programmed too low, the left-most character will be repeated. If the skew is programmed too high, one or more characters will disappear at the left of each character row.

6.5 CR3: Horizontal Blanking End Register *(cont.)*

Bit	Description
4:0	**Horizontal Blanking End [4:0]:** This field determines the width of the Horizontal Blanking Period. This field is extended with CR5[7]. The least-significant five or six bits of the Character Counter are compared with the contents of this field. When a match occurs, the Horizontal Blanking Period is ended. Note that the Horizontal Blanking Period is limited to 63 character-clock times. The value to be programmed into this register may be calculated by subtracting the desired Blanking Period from the value programmed into CR2 (Horizontal Blanking Start). The Blanking Period must never be programmed to extend past the Horizontal Total. If CR1B[5] or CR1B[7] is programmed to '1', this field is extended with Extension register CR1A[5:4]. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.6 CR4: Horizontal Sync Start Register

I/O Port Address: 3?5

Index: 4

Bit	Description
7	Horizontal Sync Start [7]
6	Horizontal Sync Start [6]
5	Horizontal Sync Start [5]
4	Horizontal Sync Start [4]
3	Horizontal Sync Start [3]
2	Horizontal Sync Start [2]
1	Horizontal Sync Start [1]
0	Horizontal Sync Start [0]

This register specifies the time where Horizontal Sync becomes active.

Bit	Description
7:0	**Horizontal Sync Start [7:0]:** This field specifies the Character Count where HSYNC (Horizontal Sync) becomes active. Adjusting the value in this field moves the display horizontally on the screen. The Horizontal Sync Start *must* be programmed to a value equal to or greater than Horizontal Display End. The time from Horizontal Sync Start to Horizontal Total *must* be equal to or greater than four character times. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.7 CR5: Horizontal Sync End Register

I/O Port Address: 3?5

Index: 5

Bit	Description
7	Horizontal Blanking End [5]
6	Horizontal Sync Delay [1]
5	Horizontal Sync Delay [0]
4	Horizontal Sync End [4]
3	Horizontal Sync End [3]
2	Horizontal Sync End [2]
1	Horizontal Sync End [1]
0	Horizontal Sync End [0]

This register specifies the position where the Horizontal Sync pulse ends, effectively specifying the width of the pulse. In addition, this register contains an overflow bit and a skew field.

Bit **Description**

7 **Horizontal Blanking End [5]:** This bit extends the Horizontal Blanking End value by one bit. Refer to Chapter 6, register CR3 for an explanation of the Horizontal Blanking End Value.

6:5 **Horizontal Sync Delay [1:0]:** This 2-bit field is used to delay the external Horizontal Sync pulse from the position implied in CR4. This is necessary in some modes to allow internal timing signals triggered from Horizontal Sync Start to begin prior to Display Enable. The following table summarizes the HSYNC Delay:

CR[6]	CR5[5]	Skew In Character Clocks
0	0	0
0	1	1
1	0	2
1	1	3

6.7 CR5: Horizontal Sync End Register *(cont.)*

Bit	Description
4:0	**Horizontal Sync End [4:0]:** This field determines the width of the Horizontal Sync pulse. The least-significant five bits of the Character Counter are compared with the contents of this field. When a match occurs, the Horizontal Sync pulse is ended. Note the Horizontal Sync pulse is limited to 31 character-clock times. The value to be programmed into this register may be calculated by subtracting the desired Sync width from the value programmed into CR4 (Horizontal Sync Start). The Sync pulse must never be programmed to extend past the Horizontal Total. In addition, HSYNC should always end during the Horizontal Blanking period. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.8 CR6: Vertical Total Register

I/O Port Address: 3?5

Index: 6

Bit	Description
7	Vertical Total [7]
6	Vertical Total [6]
5	Vertical Total [5]
4	Vertical Total [4]
3	Vertical Total [3]
2	Vertical Total [2]
1	Vertical Total [1]
0	Vertical Total [0]

This register specifies the total number of scanlines per frame.

Bit	Description
7:0	**Vertical Total [7:0]:** This field is the low-order eight bits of a 10-bit field that defines the total number of scanlines per frame. This field is extended with CR7[5] and CR7[0]. The value programmed into the Vertical Total field is the total number of scanlines minus two. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.9 CR7: Overflow Register

I/O Port Address: 3?5

Index: 7

Bit	Description
7	Vertical Retrace Start [9]
6	Vertical Display End [9]
5	Vertical Total [9]
4	Line Compare [8]
3	Vertical Blanking Start [8]
2	Vertical Retrace Start [8]
1	Vertical Display End [8]
0	Vertical Total [8]

This register contains bits that extend various vertical count fields. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

Bit	Description
7	**Vertical Retrace Start [9]:** This bit extends the Vertical Retrace Start (CR10) field to ten bits.
6	**Vertical Display End [9]:** This bit extends the Vertical Display End (CR12) field to ten bits.
5	**Vertical Total [9]:** This bit extends the Vertical Total (CR6) field to ten bits.
4	**Line Compare [8]:** This bit extends the Line Compare (CR18) field to nine bits.
3	**Vertical Blanking Start [8]:** This bit extends the Vertical Blanking Start (CR15) field to nine bits.
2	**Vertical Retrace Start [8]:** This bit extends the Vertical Retrace Start (CR10) field to nine bits.
1	**Vertical Display End [8]:** This bit extends the Vertical Display End (CR12) field to nine bits.
0	**Vertical Total [8]:** This bit extends the Vertical Total (CR6) field to nine bits.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.10 CR8: Screen A Preset Row-Scan Register

I/O Port Address: 3?5

Index: 8

Bit	Description
7	Reserved
6	Byte Pan [1]
5	Byte Pan [0]
4	Screen A Preset Row Scan [4]
3	Screen A Preset Row Scan [3]
2	Screen A Preset Row Scan [2]
1	Screen A Preset Row Scan [1]
0	Screen A Preset Row Scan [0]

This register specifies the row scanline where Screen A begins, allowing scrolling on a scanline basis (soft scroll). In addition, this register specifies the Byte Pan (coarse panning).

Bit **Description**

7 **Reserved**

6:5 **Byte Pan [1:0]:** This 10-bit field controls coarse panning. It can specify a pan of up to 24 pixels with a resolution of eight pixels. AR13 provides for panning on a pixel basis. The values programmed into CR8[6:5] are interpreted as indicated in the following table:

CR8[6]	CR8[5]	Bytes	Pixels
0	0	0	0
0	1	1	8
1	0	2	16
1	1	3	24

4:0 **Screen A Preset Row Scan [4:0]:** This field specifies the scanline where the first character row will begin. This provides scrolling on a scanline basis (soft scrolling). The contents of this field should be changed only during Vertical Retrace time.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.11 CR9: Character Cell Height Register

I/O Port Address: 3?5

Index: 9

Bit	Description
7	CRTC Scan Double
6	Line Compare [9]
5	Vertical Blank Start [9]
4	Character Cell Height [4]
3	Character Cell Height [3]
2	Character Cell Height [2]
1	Character Cell Height [1]
0	Character Cell Height [0]

This register specifies the number of scanlines in the character cell. In addition, it contains two vertical overflow bits and one control bit.

Bit	Description
7	**CRTC Scan Double:** If this bit is programmed to '1', every scanline is displayed twice in succession. The Scanline Counter-based parameters (Character Height, Cursor Start and End, and Underline location) double. This bit is typically used to display 200-line modes at 400 scanlines. This function is not available in Interlaced Video modes.
6	**Line Compare [9]:** This bit extends the Line Compare field (CR18) to ten bits.
5	**Vertical Blank Start [9]:** This bit extends the Vertical Blank Start field (CR15) to ten bits.
4:0	**Character Cell Height [4:0]:** This field specifies the vertical size of the character cell in terms of scanlines. The value programmed into this field is the actual size minus 1. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.12 CRA: Text Cursor Start Register

I/O Port Address: 3?5

Index: A

Bit	Description
7	Reserved
6	Reserved
5	Disable Text Cursor
4	Text Cursor Start [4]
3	Text Cursor Start [3]
2	Text Cursor Start [2]
1	Text Cursor Start [1]
0	Text Cursor Start [0]

This register specifies the scanline where the text cursor is to begin. In addition, this register contains a bit that will disable the text cursor.

Bit	Description
7:6	**Reserved**
5	**Disable Text Cursor:** If this bit is programmed to '1', the text cursor will be disabled (that is, it will be removed). If this bit is programmed to '0', the text cursor will function normally.
4:0	**Text Cursor Start [4:0]:** This field specifies the scanline within the Character Cell where the text cursor is to start. If the Text Cursor Start value is greater than the Text Cursor End value, there will be no text cursor displayed. If the Text Cursor Start value is equal to the Text Cursor End value, the text cursor will occupy a single scanline.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.13 CRB: Text Cursor End Register

I/O Port Address: 3?5

Index: B

Bit	Description
7	Reserved
6	Text Cursor Skew [1]
5	Text Cursor Skew [0]
4	Text Cursor End [4]
3	Text Cursor End [3]
2	Text Cursor End [2]
1	Text Cursor End [1]
0	Text Cursor End [0]

This register specifies the scanline within the Character Cell where the Text Cursor is to end. It also contains a field that allows the Text Cursor to be skewed from the location specified in registers CRE and CRF.

Bit	Description
7	**Reserved**
6:5	**Text Cursor Skew [1:0]:** This 2-bit field specifies a delay in Character Clocks, from the Text Cursor location specified in CRE and CRF to the actual cursor.
4:0	**Text Cursor End [4:0]:** This field specifies the scanline within the character where the Text Cursor is to end. A value greater than the Character Cell Height will yield an effective ending value equal to the Cell Height.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.14 CRC: Screen Start Address High Register

I/O Port Address: 3?5

Index: C

Bit	Description
7	Screen Start A Address [15]
6	Screen Start A Address [14]
5	Screen Start A Address [13]
4	Screen Start A Address [12]
3	Screen Start A Address [11]
2	Screen Start A Address [10]
1	Screen Start A Address [9]
0	Screen Start A Address [8]

This register and register CRD specify the location in display memory where the data to be displayed on the screen begins.

Bit	Description
7:0	**Screen Start A Address [15:8]:** The Screen Start A field specifies the location in display memory where the screen begins. This register contains bits 15:8 of this value. Bits 7:0 are in register CRD, bits 18:16 are in CR1B, and bit 19 is in CR1D[7]. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.15 CRD: Screen Start Address Low Register

I/O Port Address: 3?5

Index: D

Bit	Description
7	Screen Start A Address [7]
6	Screen Start A Address [6]
5	Screen Start A Address [5]
4	Screen Start A Address [4]
3	Screen Start A Address [3]
2	Screen Start A Address [2]
1	Screen Start A Address [1]
0	Screen Start A Address [0]

This register and register CRC specify the location in display memory where the data to be displayed on the screen begins.

Bit	Description
7:0	**Screen Start A Address [7:0]:** The Screen Start A field specifies the location in display memory where the screen begins. This register contains bits 7:0 of this value, bits 15:8 are in register CRD, and bits 17:16 are in register CR1B. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.16 CRE: Text Cursor Location High Register

I/O Port Address: 3?5

Index: E

Bit	Description
7	Text Cursor Location [15]
6	Text Cursor Location [14]
5	Text Cursor Location [13]
4	Text Cursor Location [12]
3	Text Cursor Location [11]
2	Text Cursor Location [10]
1	Text Cursor Location [9]
0	Text Cursor Location [8]

This register with register CRF specifies the location in display memory where the Text Cursor is to be displayed.

Bit	Description
7:0	**Text Cursor Location [15:8]:** The Text Cursor Location is a 16-bit field that specifies the location in display memory where the Text Cursor is to be displayed. This register contains bits 15:8 of this field; register CRF contains bits 7:0. **NOTE:** The value contained in this field is an address in display memory, not an offset from the beginning of the screen. If the value of Screen A Start is changed without a compensating change in the Text Cursor Location field, the Text Cursor will move on the screen. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.17 CRF: Text Cursor Location Low Register

I/O Port Address: 3?5

Index: F

Bit	Description
7	Text Cursor Location [7]
6	Text Cursor Location [6]
5	Text Cursor Location [5]
4	Text Cursor Location [4]
3	Text Cursor Location [3]
2	Text Cursor Location [2]
1	Text Cursor Location [1]
0	Text Cursor Location [0]

This register, with register CRE, specifies the location in display memory where the Text Cursor is to be displayed.

Bit	Description
7:0	**Text Cursor Location [7:0]:** The Text Cursor location is a 16-bit field that specifies the location in display memory where the Text Cursor is to be displayed. This register contains bits 7:0 of this field. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.18 CR10: Vertical Sync Start Register

I/O Port Address: 3?5

Index: 10

Bit	Description
7	Vertical Sync Start [7]
6	Vertical Sync Start [6]
5	Vertical Sync Start [5]
4	Vertical Sync Start [4]
3	Vertical Sync Start [3]
2	Vertical Sync Start [2]
1	Vertical Sync Start [1]
0	Vertical Sync Start [0]

The Vertical Sync Start field specifies the scanline where the Vertical Sync pulse will become active. This register contains the low-order eight bits of that field.

Bit	Description
7:0	**Vertical Sync Start [7:0]:** The Vertical Sync field specifies the scanline where the Vertical Sync pulse will become active. This register contains bits 7:0 of that field. This register is extended by bits in register CR7. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.19 CR11: Vertical Sync End Register

I/O Port Address: 3?5

Index: 11

Bit	Description
7	Write Protect CR7-CR0
6	Refresh Cycle Control
5	Disable Vertical Interrupt
4	Clear Vertical Interrupt
3	Vertical Sync End [3]
2	Vertical Sync End [2]
1	Vertical Sync End [1]
0	Vertical Sync End [0]

This register specifies the scanline where the Vertical Sync pulse is to become inactive, thereby effectively specifying the Vertical Sync pulse width. In addition, this register contains controls for the interrupt and two miscellaneous control bits.

Bit	Description
7	**Write Protect CR7-CR0:** If this bit is programmed to '1', registers CR0 through CR7 cannot be written. Writes addressed to those registers will simply be ignored. CR7[4] (Line Compare Extension) can always be written. If this bit is programmed to '0', registers CR0 through CR7 can be written normally.
6	**Refresh Cycle Control:** If this bit is programmed to '1', five refresh cycles will be executed per scanline. If this bit is programmed to '0', three refresh cycles will be executed per scanline. For the CL-GD5436 only, if GR18[3] is programmed to '1', one refresh cycle will be executed per scanline.
5	**Disable Vertical Interrupt:** If this bit is programmed to '1', the vertical interrupt will be disabled. The Interrupt pin will never go active. If this bit is programmed to '0', the vertical interrupt will be enabled and will function normally.
4	**Clear Vertical Interrupt:** If this bit is programmed to '0', the Interrupt Pending bit (FEAT[7]) will be cleared to '0' and the Interrupt pin will be forced inactive. Programming this bit to '1' allows the next occurance of the interrupt. This may be done immediately after programming it to '0'.
3:0	**Vertical Sync End [3:0]:** This field determines the width of the Vertical Sync pulse. The least-significant four bits of the Scanline Counter are compared with the contents of this field. When a match occurs, the Vertical Sync pulse is ended. Note the Vertical Sync pulse is limited to 15 scanlines. The value to be programmed into this register may be calculated by subtracting the desired Sync width from the value programmed into the Vertical Sync Start field. The Sync pulse must never be programmed to extend past the Vertical Total. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.20 CR12: Vertical Display End Register

I/O Port Address: 3?5

Index: 12

Bit	Description
7	Vertical Display End [7]
6	Vertical Display End [6]
5	Vertical Display End [5]
4	Vertical Display End [4]
3	Vertical Display End [3]
2	Vertical Display End [2]
1	Vertical Display End [1]
0	Vertical Display End [0]

The Vertical Display End field is used to specify the scanline where the display is to end.

Bit	Description
7:0	**Vertical Display End [7:0]:** The Vertical Display End field is used to specify the scanline where the display is to end. This register contains the least-significant eight bits of this field. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.21 CR13: Offset Register

I/O Port Address: 3?5

Index: 13

Bit	Description
7	Offset [7]
6	Offset [6]
5	Offset [5]
4	Offset [4]
3	Offset [3]
2	Offset [2]
1	Offset [1]
0	Offset [0]

This register specifies the distance in display memory between the beginnings of adjacent character rows or scanlines. This is sometimes referred to as display 'pitch'.

Bit	Description
7:0	**Offset [7:0]:** This register specifies the distance in display memory between the beginnings of adjacent character rows or scanlines. This field is extended to nine bits with CR1B[4]. At the beginning of each scanline (except the first), the address that data should be fetched from is calculated by adding the contents of this register to the beginning address of the previous scanline or character row. The offset will be left-shifted one or two bit positions depending on CR17[6].

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.22 CR14: Underline Row Scanline Register

I/O Port Address: 3?5

Index: 14

Bit	Description
7	Reserved
6	DoubleWord Mode
5	Count by Four
4	Underline Scanline [4]
3	Underline Scanline [3]
2	Underline Scanline [2]
1	Underline Scanline [1]
0	Underline Scanline [0]

This register is used to specify the underline scanline for text modes.

Bit	Description
7	**Reserved**
6	**DoubleWord Mode:** When this bit is programmed to '1', double-word addresses are forced. The CRTC Memory Address Counter is rotated left two bit positions so that Display Memory Address bits 1 and 0 are sourced from CRTC Address Counter bits 13 and 12, respectively. When this bit is programmed to '0', CR17[6] controls whether the chip uses byte or word addresses.
5	**Count by Four:** This bit must be programmed to '1' when DoubleWord mode is enabled to clock the Memory Address Counter with Character Clock divided by four. This bit must be programmed to '0' when DoubleWord mode is not enabled.
4:0	**Underline Scanline [4:0]:** This field specifies the scanline within the Character Cell where the underline will occur.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.23 CR15: Vertical Blank Start Register

I/O Port Address: 3?5

Index: 15

Bit	Description
7	Vertical Blank Start [7]
6	Vertical Blank Start [6]
5	Vertical Blank Start [5]
4	Vertical Blank Start [4]
3	Vertical Blank Start [3]
2	Vertical Blank Start [2]
1	Vertical Blank Start [1]
0	Vertical Blank Start [0]

This register specifies the scanline where blank becomes active.

Bit	Description
7:0	**Vertical Blank Start [7:0]:** The Vertical Blank Start field specifies the scanline where Vertical Blank is to begin. The low-order eight bits of that field are in this register. Overflow bits are in CR7 and CR9. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.24 CR16: Vertical Blank End Register

I/O Port Address: 3?5

Index: 16

Bit	Description
7	Vertical Blank End [7]
6	Vertical Blank End [6]
5	Vertical Blank End [5]
4	Vertical Blank End [4]
3	Vertical Blank End [3]
2	Vertical Blank End [2]
1	Vertical Blank End [1]
0	Vertical Blank End [0]

The Vertical Blank End field specifies the scanline where Vertical Blank ends.

Bit	Description
7:0	**Vertical Blank End [7:0]:** The Vertical Blank End field specifies the scanline where Vertical Blank is to end. This register contains the low-order eight bits of that field. If CR1B[5] is programmed to '0', this register contains the entire field. The contents of the Vertical Blank End field are compared to the Scanline Counter to determine when to terminate Vertical Blank. This limits the duration of Vertical Blank to 255 scanlines if CR1B[5] is programmed to '0'. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.25 CR17: Mode Control Register

I/O Port Address: 3?5

Index: 17

Bit	Description
7	Timing Enable
6	Byte/Word Mode
5	Address Wrap
4	Reserved
3	Count by Two
2	Multiply Vertical Registers by Two
1	Select Row-scan Counter
0	Compatibility Mode (CGA) Support

This register contains a number of miscellaneous control bits.

Bit	Description
7	**Timing Enable:** If this bit is programmed to '1', the CRTC Timing Logic is enabled and functions normally. If this bit is programmed to '0', the CRTC Timing Logic is disabled.
6	**Byte/Word Mode:** If this bit is programmed to '1', the contents of the CRTC Address Counter are sent to the display memory without being rotated. If this bit is programmed to '0', the contents of the CRTC Address Counter are rotated left one bit position before being sent to the display memory.
5	**Address Wrap:** If CR17[6] is programmed to '1', this bit is ignored. If CR17[6] is programmed to '0' and this bit is programmed to '1', then the left rotation described above involves 16 bits of the CRTC Address Counter. If CR17[6] is programmed to '0' and this bit is programmed to '0', then the left rotation described above involves 14 bits of the CRTC Address Counter.
4	**Reserved**
3	**Count by Two:** If this bit is programmed to '1', then the CL-GD543X/'4X will clock the Memory Address Counter with Character Clock divided by two. If this bit is programmed to '0', then the CL-GD543X/'4X will clock the Memory Address Counter with Character Clock.
2	**Multiply Vertical Registers by Two:** If this bit is programmed to '1', the Scanline Counter is clocked with Horizontal Sync divided by two. This allows the number of scanlines to be doubled to 2048. Observe that all the periods will be even multiples of two scanlines. If this bit is programmed to '0', the Scanline Counter is clocked with Horizontal Sync.

6.25 CR17: Mode Control Register *(cont.)*

Bit	Description
1	**Select Row-scan Counter:** If this bit is programmed to '0', Row-scan Counter [1] is substituted for CRTC Address Counter [14]. This provides for Hercules™ compatibility. **NOTE:** The Cirrus Logic BIOS does *not* support Hercules compatibility. If this bit is programmed to '1', the substitution described above does not occur.
0	**Compatibility Mode (CGA) Support:** If this bit is programmed to '0', Row Scan Counter [0] is substituted for CRTC Address Counter [14]. This provides for CGA compatibility. If this bit is programmed to '1', the substitution described above does not occur.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.26 CR18: Line Compare Register

I/O Port Address: 3?5

Index: 18

Bit	Description
7	Line Compare [7]
6	Line Compare [6]
5	Line Compare [5]
4	Line Compare [4]
3	Line Compare [3]
2	Line Compare [2]
1	Line Compare [1]
0	Line Compare [0]

The Line Compare field is used to specify where Screen A terminates and Screen B begins.

Bit	Description
7:0	**Line Compare [7:0]:** The Line Compare field is used to specify where Screen A terminates and Screen B begins. This register contains the eight least-significant bits of this field. The Line Compare field may be used to implement a vertically split screen. The top portion of the screen is called Screen A and may begin anywhere in display memory. Screen A can be panned and scrolled on a pixel basis. The bottom portion of the screen is called Screen B. Screen B always begins at location '0' in display memory and cannot be panned or scrolled. Refer to Figure 6–1 and Table 6–1 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.27 CR22: Graphics Data Latches Readback Register

I/O Port Address: 3?5

Index: 22

Bit	Description
7	Graphics Data Latch n Readback [7]
6	Graphics Data Latch n Readback [6]
5	Graphics Data Latch n Readback [5]
4	Graphics Data Latch n Readback [4]
3	Graphics Data Latch n Readback [3]
2	Graphics Data Latch n Readback [2]
1	Graphics Data Latch n Readback [1]
0	Graphics Data Latch n Readback [0]

This register address is used to read the four Graphics Controller Data Latches.

Bit	Description
7:0	**Graphics Data Latch n Readback [7:0]:** This read-only register may be used to read back one of the four Graphics Controller Data Latches. The latch is selected with GR4[1:0]. These latches are loaded whenever display memory is read by the CPU.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.28 CR24: Attribute Controller Toggle Readback Register

I/O Port Address: 3?5

Index: 24

Bit	Description
7	Attribute Controller Toggle
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Reserved

This read-only register provides access to the Attribute Controller Toggle.

Bit	Description
7	**Attribute Controller Toggle:** If this bit is a '1', the Attribute Controller will read or write a data value on the next access. If this bit is a '0', the Attribute Controller will read or write an index value on the next access.
6:0	**Reserved**

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.29 CR26: Attribute Controller Index Readback Register

I/O Port Address: 3?5

Index: 26

Bit	Description
7	Reserved
6	Reserved
5	Video Enable
4	Attribute Controller Index [4]
3	Attribute Controller Index [3]
2	Attribute Controller Index [2]
1	Attribute Controller Index [1]
0	Attribute Controller Index [0]

This read-only register provides access to the current Attribute Controller Index.

Bit	Description
7:6	**Reserved**
5	**Video Enable:** This bit follows the Video Enable bit in the Attribute Controller Index register.
4:0	**Attribute Controller Index [4:0]:** This field follows the index in the Attribute Controller Index register.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

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VGA Graphics Controller Registers

7. VGA GRAPHICS CONTROLLER REGISTERS

The CL-GD543X/'4X VGA Graphics Controller registers are summarized in the following table. Please note that there are Extension registers that are accessed using the VGA Graphics Controller Port.

VGA Graphics Controller Registers Quick Reference

Abbreviation	Register Name	Index	Port	Page
GRX	Graphics Controller Index	–	3CE	7 - 3
GR0	Set/Reset	0	3CF	7 - 4
GR1	Set/Reset Enable	1	3CF	7 - 5
GR2	Color Compare	2	3CF	7 - 6
GR3	Data Rotate	3	3CF	7 - 7
GR4	Read Map Select	4	3CF	7 - 8
GR5	Mode	5	3CF	7 - 9
GR6	Miscellaneous	6	3CF	7 - 12
GR7	Color Don't Care	7	3CF	7 - 13
GR8	Bit Mask	8	3CF	7 - 14

7.1 GRX: Graphics Controller Index Register

I/O Port Address: 3CE

Index: –

Bit	Description
7	Reserved
6	Reserved
5	Graphics Controller Index [5]
4	Graphics Controller Index [4]
3	Graphics Controller Index [3]
2	Graphics Controller Index [2]
1	Graphics Controller Index [1]
0	Graphics Controller Index [0]

This register is used to specify the register in the VGA Graphics Controller group or the Extension register that will be accessed by the next I/O read or I/O write to Address 3CF. Registers with an index value greater than eight are described in Chapter 9.

Bit	Description
7:6	**Reserved**
5:0	**Graphics Controller Index [5:0]:** This field specifies the register in the VGA Graphics Controller group or the Extension register that will be accessed by the next I/O read or I/O write to Address 3CF.

7.2 GR0: Set/Reset Register

I/O Port Address: 3CF

Index: 0

Memory-mapped I/O Offset: 0

Bit	Description
7	Reserved/ Write Mode 5 Background [7]
6	Reserved/ Write Mode 5 Background [6]
5	Reserved/ Write Mode 5 Background [5]
4	Reserved/ Write Mode 5 Background [4]
3	Set/Reset Plane 3/Write Mode 5 Background [3]
2	Set/Reset Plane 2/Write Mode 5 Background [2]
1	Set/Reset Plane 1/Write Mode 5 Background [1]
0	Set/Reset Plane 0/Write Mode 5 Background [0]

This register specifies the values to be written into the respective display memory planes when the processor executes a Write mode 0 or Write mode 3 operation. If Extended Write mode 5 is selected and for BitBLTs with color expansion, this register specifies the low order byte of the Background Color.

Bit	Description
7:4	**Reserved:** If Extended Write mode 5 is not selected, these bits are reserved. If GRB[2] = 0, writes to these bits will be ignored and reads from these bits will return zeroes. If GRB[2] = 1, these bits will be read/write, but the contents will not be used.
3:0	**Set/Reset Plane [3:0]:** If Extended Write mode 5 is not selected, these bits will control the values written into the respective display memory planes for Write mode 0 and 3. Refer to the description of GR5 for an overview of the Write modes.
7:0	**Write Mode 5 Background [7:0]:** If Extended Write mode 5 is selected and for BitBLTs with color expansion, these bits specify the low order byte of the Background Color. Refer to Appendix D6 for a description of Color Expansion and Extended Write modes.

7.3 GR1: Set/Reset Enable Register

I/O Port Address: 3CF

Index: 1

Memory-mapped I/O Offset: 4

Bit	Description
7	Reserved/ Write Mode 4, 5 Foreground [7]
6	Reserved/ Write Mode 4, 5 Foreground [6]
5	Reserved/ Write Mode 4, 5 Foreground [5]
4	Reserved/ Write Mode 4, 5 Foreground [4]
3	Enable SR Plane 3/ Write Mode 4, 5 Foreground [3]
2	Enable SR Plane 2/ Write Mode 4, 5 Foreground [2]
1	Enable SR Plane 1/ Write Mode 4, 5 Foreground [1]
0	Enable SR Plane 0/ Write Mode 4, 5 Foreground [0]

This register is used with GR0 to determine the values to be written into the respective display memory planes when Write mode 0 is selected. If Extended Write modes 4 or 5 are selected and for BitBLTs with color expansion, this register defines the low order byte of the Foreground Color.

Bit	Description
7:4	**Reserved:** If Extended Write modes 4 or 5 are not selected, these bits are reserved. If GRB[2] = 0, writes to these bits will be ignored and reads from these bits will return zeroes. If GRB[2] = 1, these bits will be read/write, but the contents will not be used.
3:0	**Enable SR Plane [3:0]:** These bits are used with GR0 to determine the values written into the display memory planes when Write mode 0 is selected. If a bit in this field is programmed to a '1', the corresponding value in GR0 will be written into the corresponding display memory plane. If a bit in this field is programmed to a '0', the corresponding value from the CPU Data bus will be written into the corresponding display memory plane. Refer to the description of GR5 for an overview of the Write modes. Note that if High Resolution mode is selected by setting SR7[0], the Set/Reset Logic is disabled. The chip behaves as though this field is programmed to all 0's.
7:0	**Write Mode 4, 5 Foreground [7:0]:** If Extended Write mode 4 or 5 is selected and for BitBLTs with Color Expansion, these bits specify the low order byte of the Foreground Color. Refer to Appendix D6 for a description of Color Expansion and Extended Write modes.

7.4 GR2: Color Compare Register

I/O Port Address: 3CF

Index: 2

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Color Compare Plane [3]
2	Color Compare Plane [2]
1	Color Compare Plane [1]
0	Color Compare Plane [0]

This register specifies the Color Compare Value for Read mode 1.

Bit	Description
7:4	**Reserved**
3:0	**Color Compare Plane [3:0]:** These four bits are compared with each of eight bits from the corresponding display memory planes under the mask in GR7 when a Read mode 1 occurs. Refer to the description of GR5 for an overview of the Read modes.

7.5 GR3: Data Rotate Register

I/O Port Address: 3CF

Index: 3

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Function Select [1]
3	Function Select [0]
2	Rotate Count [2]
1	Rotate Count [1]
0	Rotate Count [0]

This register contains two fields that are used with Write modes 0 and 3.

Bit **Description**

7:5 **Reserved**

4:3 **Function Select [1:0]:** This field controls the operation that occurs between the data in the latches and the data from the CPU or SET/RESET logic. The result of this operation is written into display memory. This field is used for Write mode 0 only. The operations are summarized in the following table:

GR3[4]	GR3[3]	Operation
0	0	None: The data in the latches are ignored.
0	1	Logical 'AND'
1	0	Logical 'OR'
1	1	Logical 'XOR'

2:0 **Rotate Count [2:0]:** This field allows data from the CPU bus to be rotated as many as seven bit positions prior to being altered by the SET/RESET logic. Refer to the description of GR5 for an overview of the Write modes.

7.6 GR4: Read Map Select Register

I/O Port Address: 3CF

Index: 4

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Plane Select [1]
0	Plane Select [0]

This register is used to specify the display memory plane for Read mode 0.

Bit	Description
7:2	**Reserved**
1:0	**Plane Select [1:0]:** This field specifies the display memory plane for Read mode 0. The values are shown in the following table:

GR4[1]	GR4[0]	Plane Selected
0	0	0
0	1	1
1	0	2
1	1	3

7.7 GR5: Mode Register

I/O Port Address: 3CF

Index: 5

Bit	Description
7	Reserved
6	256-color Mode
5	Shift Register Mode
4	Odd/Even
3	Read Mode
2	Write Mode [2]
1	Write Mode [1]
0	Write Mode [0]

This register specifies the Read and Write modes. In addition, it controls the configuration of the Data Shift registers.

Bit	Description
7	**Reserved**
6	**256-color Mode:** If this bit is programmed to a '1', the Video Shift registers will be configured for 256-color Video modes. GR5[5] is ignored. If this bit is programmed to a '0', the Video Shift registers will be configured for 16-, 4-, or 2-color modes.
5	**Shift Register Mode:** If this bit is programmed to a '1', the Video Shift registers will be configured for CGA compatibility. This is used for Video modes 4 and 5. If this bit is programmed to a '0', the Video Shift registers will be configured for EGA compatibility.
4	**Odd/Even:** If this bit is programmed to a '1', the Graphics Controller will be configured for Odd/Even Addressing mode. This bit should always be programmed to the opposite value as SR4[2].

7.7 GR5: Mode Register *(cont.)*

Bit	Description
3	**Read Mode:** This bit specifies whether the chip is in Read mode 0 or Read mode 1. **Read Mode 0:** If this bit is programmed to a '0', the CPU will read data directly from display memory. Each read will return eight adjacent bits of the display memory plane specified in GR4[1:0]. The color-match logic is not used in Read mode 0. Note that an I/O read of CR22 will force a Read mode 0 operation. **Read Mode 1:** If this bit is programmed to a '1', the CPU will read the results of the Color Compare Logic. Read mode 1 allows eight adjacent pixels (in 16-color modes) to be compared to a specified color value in a single operation. Each of the eight bits returned to the processor indicates the result of a compare between the four bits of the Color Compare (GR2[3:0]) and the bits from the four display memory planes. If the four bits of the Color Compare match the four bits from the display memory planes, a '1' will be returned for the corresponding bit position. If any bits in the Color Don't Care (GR7[3:0]) are zeroes, the corresponding plane comparison will be forced to match.
2:0	**Write Mode [2:0]:** These three bits specify the Write mode or Extended Write mode. If GRB[2] is programmed to a '0', only Write modes 0 through 3 will be available. **Write Mode 0:** Each of the four display memory planes is written with the CPU data rotated by the number of counts in GR3[2:0]. If a bit in GR1[3:0] is programmed to a '1', the corresponding plane is written with the contents of the corresponding bit in GR0[3:0]. If SR7[0] is programmed to a '1', CPU data is written regardless of the contents of GR1[3:0]. The contents of the Data Latches may be combined with the data from the SR logic under control of GR3[4:3]. Bit planes are enabled with SR2[3:0]. Bit positions are enabled with GR8. **Write Mode 1:** Each of the four display memory planes is written with the data in the Data Latches. The Data Latches had been loaded from display memory with a previous read. GR8 is ignored in Write mode 1. **Write Mode 2:** Display memory planes 3:0 are written with value of Data bits 3:0, respectively. The four bits are replicated eight times each to write up to eight adjacent pixels. Bit planes are enabled with SR2[3:0]. Bit positions are enabled with GR8. The Data Rotator, SR logic and Function Select fields are ignored in Write mode 2.

7.7 GR5: Mode Register *(cont.)*

Bit	Description
2:0 *(cont.)*	**Write Mode 3:** The data for each display memory plane comes from the corresponding bit of GR0[3:0]. The bit-position-enable field is formed with the logical AND of GR8 and the rotated CPU data. The SET/RESET and Function Select fields are ignored in Write mode 3. **Extended Write Mode 4:** The contents of GR1 and GR11 are written into up to eight adjacent pixels per byte of source data. The CPU data is used to control whether pixels are written. If a bit in the CPU is a '1', the corresponding pixel is written. If a bit in the CPU data is a '0', the corresponding pixel is not changed. This mode is intended for 256- or 64K-color text expansion where the background is to be preserved. **Extended Write Mode 5:** The contents of either GR1/GR11 or GR0/GR10 are written into each of eight adjacent pixels per byte of source data. The choice between GR1 and GR0 is made for each of the eight pixels according the value of the corresponding bit of the CPU data. This is summarized in the following table. This mode is intended for 256- or 64K-color text expansion where both the foreground and background are to be written.

CPU Data	GR0/GR1	Note
0	GR0/GR10	Background
1	GR1/GR11	Foreground

See Appendix D6 for more information on Extended Write modes 4 and 5.

7.8 GR6: Miscellaneous Register

I/O Port Address: 3CF

Index: 6

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Memory Map [1]
2	Memory Map [0]
1	Chain Odd Maps to Even
0	Graphics Mode

This register contains miscellaneous control bits.

Bit **Description**

7:4 **Reserved**

3:2 **Memory Map [1:0]:** This field specifies the beginning address and size of the display memory in the Host Address Space. This is summarized in the following table:

GR6[3]	GR6[2]	Memory Map	Beginning Address	Length	Mode(s)
0	0	0	A000:0	128K	Extended
0	1	1	A000:0	64K	EGA/VGA
1	0	2	B000:0	32K	Hercules™[a]
1	1	3	B800:0	32K	CGA

a. The Cirrus Logic BIOS does not support Hercules modes.

1 **Chain Odd Maps to Even:** When this bit is programmed to a '1', CPU Address bit 0 is replaced with a higher-order address bit. This causes even host addresses to access Planes 0 and 2, and odd host addresses to access Planes 1 and 3. This mode is useful for MDA emulation.

0 **Graphics Mode:** If this bit is programmed to a '1', the CL-GD543X/'4X will function in Graphics (A.P.A.) modes. If it is programmed to a '0', the chip will function in Text (A.N.) modes.

7.9 GR7: Color Don't Care Register

I/O Port Address: 3CF

Index: 7

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Color Don't Care Plane [3]
2	Color Don't Care Plane [2]
1	Color Don't Care Plane [1]
0	Color Don't Care Plane [0]

This register is used with GR2 for Read mode 1 accesses.

Bit	Description
7:4	**Reserved**
3:0	**Color Don't Care Plane [3:0]:** These four bits are used to control whether the four planes will be involved in color compares. If a bit is programmed to a '1', the corresponding plane will be involved; if a bit is programmed to a '0', the corresponding plane will not be involved. Refer to the description of GR5 for an overview of the Read modes.

7.10 GR8: Bit Mask Register

I/O Port Address: 3CF

Index: 8

Bit	Description
7	Write Enable [7]
6	Write Enable [6]
5	Write Enable [5]
4	Write Enable [4]
3	Write Enable [3]
2	Write Enable [2]
1	Write Enable [1]
0	Write Enable [0]

This register is used to control writing to display memory on a bit basis in Write modes 0, 2, and 3.

Bit	Description
7:0	**Write Enable [7:0]:** Each bit in this register controls whether the corresponding bit in display memory is written in Write modes 0, 2, and 3. If a bit is programmed to a '1', the corresponding bit in display memory will be written. If a bit is programmed to a '0', the corresponding bit in display memory will not be written. This write protection is orthogonal to that provided by SR2.

Attribute Controller Registers

8. ATTRIBUTE CONTROLLER REGISTERS

The CL-GD543X/'4X Attribute Controller registers are summarized in the following table:

Attribute Controller Registers Quick Reference

Abbreviation	Register Name	Index	Port	Page
ARX	Attribute Controller Index	–	3C0/3C1	8 - 3
AR0-ARF	Attribute Controller Palette	0:F	3C0/3C1	8 - 4
AR10	Attribute Controller Mode	10	3C0/3C1	8 - 5
AR11	Overscan (Border) Color	11	3C0/3C1	8 - 7
AR12	Color Plane Enable	12	3C0/3C1	8 - 8
AR13	Pixel Panning	13	3C0/3C1	8 - 9
AR14	Color Select	14	3C0/3C1	8 - 10

8.1 ARX: Attribute Controller Index Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: –

Bit	Description
7	Reserved
6	Reserved
5	Video Enable
4	Attribute Controller Index [4]
3	Attribute Controller Index [3]
2	Attribute Controller Index [2]
1	Attribute Controller Index [1]
0	Attribute Controller Index [0]

This register is used to specify the register in the Attribute Controller block that is accessed with the next I/O read or I/O write to 3C1 or 3C0, respectively. Observe that the same port addresses are used for the index and data for the Attribute Controller block, unlike the other blocks for which the Index and Data registers are at different addresses. Alternate writes toggle between index and data. It is possible to read the toggle at CR24, and the index value at CR26.

Bit	Description
7:6	**Reserved**
5	**Video Enable:** When this bit is programmed to a '0', the screen displays the color indicated by the Overscan register (AR11). When this bit is programmed to a '1', normal video is displayed.
4:0	**Attribute Controller Index [4:0]:** This field is the index into the Data registers in the Attribute Controller block.

8.2 AR0-ARF: Attribute Controller Palette Registers

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 0:F

Bit	Description
7	Reserved
6	Reserved
5	Secondary Red
4	Secondary Green/Intensity
3	Secondary Blue/Monochrome
2	Red
1	Green
0	Blue

In 16-color Text and Graphics modes, these digital palette entries are chosen by the four bits of pixel data, and point to Video RAM entries. The Video RAM entries are normally programmed so that the DAC Outputs reflect these values. That is, the Video RAM is programmed to simulate standard EGA colors.

Bit	Description
7:6	**Reserved**
5:0	**Palette Entries**

8.3 AR10: Attribute Controller Mode Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 10

Bit	Description
7	AR14 Video Source Enable
6	Pixel Double Clock Select
5	Pixel Panning Compatibility
4	Reserved
3	Blink Enable
2	Line Graphics Enable
1	Display Type
0	Graphics Mode

This register contains some miscellaneous control bits for the Attribute Controller.

Bit	Description
7	**AR14 Video Source Enable:** If this bit is programmed to a '1', AR14[1:0] are used as the source for the Lookup Table Address bits [5:4]. This allows the rapid selection of four 16-color palettes. If an 8-, 16-, 24, or 32-bit Pixel mode is chosen, this bit is ignored. If this bit is programmed to a '0', the Palette registers AR0-F[5:4] are used as the source for the Lookup Table Address bits [5:4].
6	**Pixel Double Clock Select:** If this bit is programmed to a '1', pixels are clocked on every other clock cycle and AR0-F is bypassed. This is used with mode 13. The Sequencer Logic operates at twice the Pixel Rate. If this bit is programmed to a '0', pixels are clocked on every cycle.
5	**Pixel Panning Compatibility:** If this bit is programmed to a '1', a Line Compare match in the CRTC will force the output of the Pixel Panning register to a '0' until the next VSYNC occurs. This allows the panning of Screen A without Screen B. If this bit is programmed to a '0', the two parts of a split screen will pan together.
4	**Reserved**
3	**Blink Enable:** If this bit is programmed to a '1', character blinking is enabled at the Vertical Refresh Frequency divided by 32. If this bit is programmed to a '0', character blinking is disabled.
2	**Line Graphics Enable:** If this bit is programmed to a '1', the ninth bit of a nine-bit-wide character cell will be made the same as the eighth bit for character codes in the range C0 through DF. If this bit is programmed to a '0', the ninth bit of a nine-bit-wide character cell will be the same as the background.

8.3 AR10: Attribute Controller Mode Register *(cont.)*

Bit **Description**

1 **Display Type:** This bit is useful only if the CL-GD543X/'4X is in Alphanumeric modes. If this bit is programmed to a '1', the contents of the Attribute Byte are treated as MDA-compatible attributes. The following table shows examples of monochrome attributes:

Blink Bit 7	Background Bit [6:4]	Intensity Bit 3	Foreground Bit [2:0]	Hex Code	Attribute
0	0	0	7	07	Normal
0	0	1	7	0F	Intense
0	0	0	1	01	Underline
0	0	1	1	09	Underline Intense
0	7	0	0	70	Reverse
1	7	0	0	F0	Blinking Reverse

If this bit is programmed to a '0', the contents of the Attribute Byte are treated as color attributes.

0 **Graphics Mode:** If this bit is programmed to a '1', the Attribute Controller will function in Graphics (A.P.A.) mode. If this bit is programmed to a '0', the Attribute Controller will function in Alphanumeric (A.N.) modes.

8.4 AR11: Overscan (Border) Color Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 11

Bit	Description
7	Reserved
6	Reserved
5	Secondary Red
4	Secondary Green
3	Secondary Blue
2	Red
1	Green
0	Blue

This register points to the entry in the LUT that defines the Border Color. Typically, the LUT entries are programmed so that the color defined above is the color that actually results. The border is defined as that portion of the raster between blanking and active video, on all four sides. Refer to Figure 6–1 at register CR0. Refer also to the description of SR12[7].

Bit	Description
7:6	**Reserved**
5:0	**Border Color [5:0]:** Either four or six of these bits are used to select the LUT entry for the Border Color in CGA and EGA modes.

8.5 AR12: Color Plane Enable Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 12

Bit	Description
7	Reserved
6	Reserved
5	Video Status Mux [1]
4	Video Status Mux [0]
3	Enable Plane [3]
2	Enable Plane [2]
1	Enable Plane [1]
0	Enable Plane [0]

This register contains a field that enables the four planes into the Attribute Controller Palette registers. It also contains a field that chooses the inputs for Diagnostic bits in STAT[5:4].

Bit **Description**

7:6 **Reserved**

5:4 **Video Status Mux [1:0]:** This field chooses the inputs for the Diagnostic bits in STAT[5:4] as indicated in the following table:

AR12[5]	AR12[4]	STAT[5]	STAT[4]
0	0	P[2]	P[0]
0	1	P[5]	P[4]
1	0	P[3]	P[1]
1	1	P[7]	P[6]

3:0 **Enable Color Plane [3:0]:** If any bit in this field is programmed to a '1', the data from the corresponding display memory plane is enabled in the choice of the Attribute Controller Palette register. If any bit in this field is programmed to a '0', the data from the corresponding display memory plane is forced to a '0' in the choice of the Attribute Controller Palette register.

8.6 AR13: Pixel Panning Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 13

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Pixel Panning [3]
2	Pixel Panning [2]
1	Pixel Panning [1]
0	Pixel Panning [0]

This register specifies the number of pixels the display data will be shifted to the left. This field functions both in the Graphics (A.N.) and Alphanumeric (A.P.A.) modes.

Bit	Description
7:4	**Reserved**
3:0	**Pixel Panning [3:0]:** This field specifies the number of pixels the display data will be shifted to the left. This field is interpreted as indicated in the following table:

AR13[3:0]	9-Bit Characters	8-Bit Characters	Mode 13
0	1 bit left	(none)	(none)
1	2 bits left	1 bit left	–
2	3 bits left	2 bits left	1 bit left
3	4 bits left	3 bits left	–
4	5 bits left	4 bits left	2 bits left
5	6 bits left	5 bits left	–
6	7 bits left	6 bits left	3 bits left
7	8 bits left	7 bits left	–
8-F	no shift	1 bit right	–

8.7 AR14: Color Select Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 14

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Color Bit C [7]
2	Color Bit C [6]
1	Color Bit C [5]
0	Color Bit C [4]

This register contains two fields that are involved in the selection of addresses into the LUT.

Bit	Description
7:4	**Reserved**
3:2	**Color Bit C [7:6]:** These two bits are concatenated with the six bits from the Attribute Controller Palette register to form the address into the LUT and to drive P[7:6]. These bit are ignored in 8-, 16-, and 24-bit Pixel modes.
1:0	**Color Bits C [5:4]:** If AR10[7] is programmed to a '1', these two bits replace the corresponding two bits from the Attribute Controller Palette register to form the address into the LUT and to drive P[7:6]. If AR10[7] is programmed to a '0', these two bits are ignored. These bits are ignored in 8-, 16-, and 24-bit Pixel modes.

Extension Registers

9

9. EXTENSION REGISTERS

The CL-GD543X/'4X Extension registers are summarized in the following table:

Extension Registers Quick Reference

Abbreviation	Register Name	Index	Port	Page
SR2	Enable Writing Pixel Extension†	2	3C5	See notes
SR6	Unlock ALL Extensions	6	3C5	9-5
SR7	Extended Sequencer Mode	7	3C5	9-6
SR8	EEPROM Control/ DDC2B	8	3C5	9-9
SR9	Scratch Pad 0	9	3C5	9-11
SRA	Scratch Pad 1	A	3C5	9-11
SRB	VCLK0 Numerator	B	3C5	9-12
SRC	VCLK1 Numerator	C	3C5	9-12
SRD	VCLK2 Numerator	D	3C5	9-12
SRE	VCLK3 Numerator	E	3C5	9-12
SRF	DRAM Control	F	3C5	9-13
SR10	Graphics Cursor X Position	10	3C5	9-15
SR11	Graphics Cursor Y Position	11	3C5	9-16
SR12	Graphics Cursor Attribute	12	3C5	9-17
SR13	Graphics Cursor Pattern Address Offset	13	3C5	9-18
SR14	Scratch Pad 2	14	3C5	9-19
SR15	Scratch Pad 3	15	3C5	9-19
SR16	Performance Tuning	16	3C5	9-20
SR17	Configuration Readback and Extended Control	17	3C5	9-22
SR18	Signature Generator Control	18	3C5	9-24
SR19	Signature Generator Result Low-Byte	19	3C5	9-26
SR1A	Signature Generator Result High-Byte	1A	3C5	9-27
SR1B	VCLK0 Denominator and Post-Scalar	1B	3C5	9-28
SR1C	VCLK1 Denominator and Post-Scalar	1C	3C5	9-28
SR1D	VCLK2 Denominator and Post-Scalar	1D	3C5	9-28
SR1E	VCLK3 Denominator and Post-Scalar	1E	3C5	9-28
SR1F	BIOS ROM Write Enable and MCLK Select	1F	3C5	9-29
GR0	Write Mode 5 Background Extension ‡	0	3CF	See notes
GR1	Write Mode 4, 5 Foreground Extension ‡	1	3CF	See notes
GR9	Offset Register 0	9	3CF	9-31

Extension Registers Quick Reference *(cont.)*

Abbreviation	Register Name	Index	Port	Page
GRA	Offset Register 1	A	3CF	9-33
GRB	Graphics Controller Mode Extensions	B	3CF	9-34
GRC	Color Key Compare	C	3CF	9-36
GRD	Color Key Compare Mask	D	3CF	9-37
GRE	Power Management	E	3CF	9-38
GR10	Background Color Byte 1	10	3CF	9-40
GR11	Foreground Color Byte 1	11	3CF	9-41
GR12	Background Color Byte 2 (CL-GD5434/'36 only)	12	3CF	9-42
GR13	Foreground Color Byte 2 (CL-GD5434/'36 only)	13	3CF	9-43
GR14	Background Color Byte 3 (CL-GD5434/'36 only)	14	3CF	9-44
GR15	Foreground Color Byte 3 (CL-GD5434/'36 only)	15	3CF	9-45
GR18	Extended DRAM Controls (CL-GD5430/'36/'40 only)	18	3CF	9-46
GR20	BLT Width Byte 0	20	3CF	9-48
GR21	BLT Width Byte 1	21	3CF	9-48
GR22	BLT Height Byte 0	22	3CF	9-49
GR23	BLT Height Byte 1	23	3CF	9-49
GR24	BLT Destination Pitch Byte 0	24	3CF	9-50
GR25	BLT Destination Pitch Byte 1	25	3CF	9-50
GR26	BLT Source Pitch Byte 0	26	3CF	9-51
GR27	BLT Source Pitch Byte 1	27	3CF	9-51
GR28	BLT Destination Start Byte 0	28	3CF	9-52
GR29	BLT Destination Start Byte 1	29	3CF	9-52
GR2A	BLT Destination Start Byte 2	2A	3CF	9-52
GR2C	BLT Source Start Byte 0	2C	3CF	9-53
GR2D	BLT Source Start Byte 1	2D	3CF	9-53
GR2E	BLT Source Start Byte 2	2E	3CF	9-53
GR2F	BLT Write Mask Destination (CL-GD5430/'36/'40 only)	2F	3CF	9-54
GR30	BLT Mode	30	3CF	9-55
GR31	BLT Start/Status	31	3CF	9-58
GR32	BLT Raster Operation	32	3CF	9-60
GR33	BLT Mode Extensions	33	3CF	9-62
CR19	Interlace End	19	3?5	9-63

Extension Registers Quick Reference *(cont.)*

Abbreviation	Register Name	Index	Port	Page
CR1A	Miscellaneous Control	1A	3?5	9-64
CR1B	Extended Display Controls	1B	3?5	9-66
CR1C	Sync Adjust and Genlock (CL-GD5434/'36 only)	1C	3?5	9-68
CR1D	Overlay Extended Control	1D	3?5	9-70
CR1E	Video Port Configuration (CL-GD5440 only)	1E	3?5	9-72
CR25	Part Status	25	3?5	9-74
CR27	ID	27	3?5	9-75
CR28	CL-GD5430 Class ID	28	3?5	9-76
CR31	Video Window Horizontal Zoom Control (CL-GD5440 only)	31	3?5	9-77
CR32	Video Window Vertical Zoom Control (CL-GD5440 only)	32	3?5	9-78
CR33	Video Window Horizontal Region 1 Size (CL-GD5440 only)	33	3?5	9-79
CR34	Video Window Region 2 Skip Size (CL-GD5440 only)	34	3?5	9-81
CR35	Video Window Region 2 Active Size (CL-GD5440 only)	35	3?5	9-82
CR36	Video Window Horizontal Overflow (CL-GD5440 only)	36	3?5	9-83
CR37	Video Window Vertical Start (CL-GD5440 only)	37	3?5	9-84
CR38	Video Window Vertical End (CL-GD5440 only)	38	3?5	9-85
CR39	Video Window Vertical Overflow (CL-GD5440 only)	39	3?5	9-86
CR3A	Video Window Start Address Byte 0 (CL-GD5440 only)	3A	3?5	9-87
CR3B	Video Window Start Address Byte 1 (CL-GD5440 only)	3B	3?5	9-87
CR3C	Video Window Start Address Byte 2 (CL-GD5440 only)	3C	3?5	9-88
CR3D	Video Window Address Offset (CL-GD5440 only)	3D	3?5	9-89
CR3E	Video Window Master Control (CL-GD5440 only)	3E	3?5	9-90
CR3F	Host Video Data Path Control (CL-GD5440 only)	3F	3?5	9-92
HDR	Hidden DAC Register	–	3C6	9-94

NOTES:

† Refer to Chapter 5 (Section 5.4) for a description of this register.

‡ Refer to Chapter 7 (Sections 7.2 and 7.3) for a description of these registers.

9.1 SR6: Unlock All Extensions Register

I/O Port Address: 3C5

Index: 6

Bit	Description	Reset State
7	Don't Care	0
6	Don't Care	0
5	Don't Care	0
4	Unlock	0
3	Don't Care	1
2	Unlock	1
1	Unlock	1
0	Unlock	1

This register is used to enable or disable access to the Extension registers. All Extension registers on the CL-GD5430/'40 are always unlocked.

Bit	Description
7:0	**Extensions Register Access Value:** If this field is loaded with 'xxx1x010', it will be read as '00010010', and the Extension registers will be enabled for read and write access. If this field is loaded with any other value, it will be read as '00001111', and the Extension registers will be disabled for read and write access. All Extension registers on the CL-GD5430/'36/'40 are always unlocked.

NOTE: The standard Cirrus Logic BIOS unlocks the registers at POST. If an application subsequently locks the Extension registers, the BIOS will function only as a standard VGA controller. In particular, it will not set any Cirrus Logic Extended modes and it will not execute any VESA or Cirrus Logic extended calls.

9.2 SR7: Extended Sequencer Mode Register

I/O Port Address: 3C5

Index: 7

Bit	Description	Reset State
7	Memory Segment Select 3	0
6	Memory Segment Select 2	0
5	Memory Segment Select 1	0
4	Memory Segment Select 0	0
3	Sequencer Pixel Clock Control [2]	
2	Sequencer Pixel Clock Control [1]	
1	Sequencer Pixel Clock Control [0]	
0	Select High-resolution Modes	

This register has several purposes; these are described in the following bit descriptions.

Bit	Description
7:4	**Memory Segment Select [3:0]:** The detailed meaning of this field depends on the system bus configuration of the CL-GD543X/'4X. See Appendix D2 for detailed information on linear addressing. **ISA Bus:** If this field is set to '0000', the CL-GD5434 will be configured as a standard VGA, responding to accesses at Axxx:x or Bxxx:x or both. Refer to the description of GR6[3:2]. If this field is set to any value other than '0000', the CL-GD5434 will be configured for 1- or 2-Mbyte linear addressing. It will respond to any memory access for which Address bits 23:20 match the Memory Segment Select field. If GRB[5] is set to '1', Memory Segment Select [0] is ignored and the CL-GD5434 will respond to a 2-Mbyte address range on a 2-Mbyte boundary. **VESA Local Bus:** If this field is set to '0000', CL-GD543X/'4X will be configured as a standard VGA, responding to accesses at Axxx:x or Bxxx:x or both. Refer to Chapter 7 for a description of GR6[3:2]. If this field is set to any value other than '0000', CL-GD543X/'4X will respond to any system address if HIMEM and LOWMEM are both '1'. **PCI Bus:** If this field is set to '0000', the CL-GD543X/'4X will respond to access at Axxx:x and Bxxx:x as a standard VGA. If this field is set to any value other than '0000', the contents of the PCI Base Address register will specify the beginning of the 16-Mbyte area assigned to the CL-GD543X/'4X display memory. The display memory for the CL-GD5434 will be in the low 4 Mbytes of the range selected. The CL-GD5430 will respond to accesses in the low 2 Mbytes of the range selected. The CL-GD5436 will respond to all 16 Mbytes as four byte-swapping apertures. **NOTE:** The 4-Mbyte Address Range will have a one-to-one mapping to the 4 Mbyte of installed display memory only if the chip is configured for extended 256-color chain-4 addressing. If the chip is configured for unchained, x8 or x16 addressing, it will respond to the entire 1-Mbyte range, but address wrapping will occur.

9.2 SR7: Extended Sequencer Mode Register *(cont.)*

Bit **Description**

3:1 **Sequencer Pixel Clock Control [2:0]:** This field selects the CRTC Character Clock Divider mode, as indicated in the following table:

SR7[3:1]	Mode	Note	'36 Note
000	Normal Operation		
001	Clock ÷ 2 for 16 bit/Pixel Data	(Byte Serial)	Selects 011
010	Clock ÷ 3 for 24 bit/Pixel Data	(Byte Serial)	Packed-24
011	16 bit/Pixel Data at Pixel Rate		
100	32 bit/Pixel Data at Pixel Rate	CL-GD5434/'36 only	
101	Reserved		
110	Reserved		
111	Reserved		

Clock ÷ 2 for 16-Bit/Pixel Data: If this mode is selected, the DAC and Video Shift register are clocked at the VCLK (Data Byte) Rate, and the CRTC is clocked with a character clock of 8 pixels (16 VCLKs). This allows the CRTC timing values for 640 × 480 and 800 × 600 with 16-bit pixels to be set in units of an 8-pixel character clock. CR13 (Offset register) will be set to A0h for 640 × 480 mode and C8h for 800 × 600 mode. This mode is available only if the CL-GD543X/'4X is configured for a 32- or 64-bit DRAM Interface. The hardware cursor X-position may be set in pixel units. The cursor will only be supported with the internal DAC and not through the feature connector. The Cursor Data Invert function will operate on the actual 15-, 16-, or 18-bit RGB data presented to the DAC.

For the CL-GD5436, setting this value will be the same as setting '011'. The CL-GD5436 will never use the 16-bit serial mode. VCLK must be set to the pixel rate, rather than 2X.

Clock ÷ 3 for 24-Bit/Pixel Data: If this mode is selected, the DAC and Video Shift register are clocked at the VCLK (Data Byte) Rate, and the CRTC is clocked with a character clock of 8 pixels (24 VCLKs). This allows the CRTC timing values for 640 × 480 with 24-bit pixels to be set in units of an 8-pixel character clock. CRTC13 (Offset register) will be set to F0h. This mode is available only if the CL-GD543X/'4X is configured for a 32-bit or greater DRAM Interface. The hardware cursor is not supported in this configuration. This clocking mode is used only for video mode 71h.

For the CL-GD5436, this will select the Packed-24 mode. VCLK must be set to the pixel rate, rather than 3X. The Hardware Cursor is supported in Packed-24 modes.

9.2 SR7: Extended Sequencer Mode Register *(cont.)*

Bit	Description
3:1 *(cont.)*	**16-Bit/Pixel Data at Pixel Rate:** If this mode is selected, the Sequencer will provide 16-bit data to the palette DAC at the displayed Pixel Rate. This allows 5-5-5 or 5-6-5 Color modes to be selected with a 1x VCLK. The data at P[7:0] will be only the low byte of the Pixel Data. The high byte is not available externally. This mode provides for 1024 × 768, 5-5-5 or 5-6-5 color with VCLK equal to the Pixel Rate. The hardware cursor is supported in this mode. **32-Bit Pixel Data at Pixel Rate (CL-GD5434/'36 only):** The pixel data is output as 24-bits-per-pixel. The upper eight bits of pixel data are sent to the DAC LUT and used for Color Key Compare (see Appendix B14). The hardware cursor is supported in this mode. Character clock is 8 pixels (VCLKs) per character. This feature requires a 64-bit DRAM data path. This mode is not supported on the CL-GD5430/'40. When this mode is chosen, the Display Memory Offset registers (CR13[7:0] and CR1B[4]) are multiplied by two, so an offset of up to 8K bytes may be programmed.
0	**Select High-resolution Modes:** If this bit is set to '1', the Video Shift registers are configured so that one character clock is equal to eight pixels. In addition, true packed-pixel memory addressing is enabled. This mode is used with 8-, 16-, 24-, and 32-bit-per-pixel modes. In addition, GR0 and GR1 function only as color registers. SET/RESET is not enabled. **NOTE:** In true packed-pixel addressing, consecutive pixels are stored at consecutive addresses. This is in contrast with Chain-4 addressing in which consecutive pixels are stored at every fourth address in display memory. For the CL-GD5436 only, setting this bit to '0' forces 32-bit DRAM operation. Only a single Mbyte of display memory is available. Any additional display memory configured in SRF will be refreshed. The CRT FIFO is forced to 8 levels. If this bit is set to '1', all display memory configured in SRF will be available and the CRTC FIFO will be 28 levels.

9.3 SR8: EEPROM Control / DDC2B Control Register

I/O Port Address: 3C5

Index: 8

Bit	Description
7	EEDI Readback
6	Disable MCS16*/ DDC2B
5	Latch ESYNC and EVIDEO*/Reserved
4	Enable EEPROM Data and SK/Reserved
3	Data to EEPROM/Reserved
2	SK to EEPROM/EECS Readback
1	Enable EEPROM Data In/EEDI Output
0	EECS Output

This register controls the optional configuration EEPROM, or is used for Display Data Channel (DDC) control. See Appendix B15 for information regarding the EEPROM interfaces and programming. See Appendix B16 for information regarding DDC. The bits in this register completely change function when the CL-GD543X/'4X is configured for DDC2B by programming bit 6 to '1'. In the bit descriptions that follow, each bit (except bit 6) is described first for EEPROM configuration, and then for DDC2B configuration.

Bit	Description
7	**EEDI Readback (EEPROM Configuration):** This read-only bit reflects the state of the EEDI pin (pin 106) if SR8[1] is '1'. If SR8[1] is '0', this bit will always be read as '0'. **EEDI Readback (DDC2B Configuration):** This read-only bit reflects the state of the EEDI pin (pin 106).
6	**Disable MCS16* for Display Memory (ISA Configuration):** If the CL-GD5434 is configured for ISA bus, and if this bit is set to '1', accesses to display memory will not cause MCS16* to be made active in an ISA system. This prevents interference where two video cards are installed. This bit *must* be set to '0' when programming BitBLTs using system memory for the source. **DDC2B (PCI, VESA VL-Bus Configuration):** When CL-GD543X/'4X with DDC2B support are configured for PCI or VESA VL-Bus, this bit has the following meaning. If this bit is set to '0', the CL-GD543X/'4X will be configured for EEPROM and the remaining bits in this register will have their EEPROM meanings. If this bit is set to '1', the CL-GD543X/'4X will be configured for DDC2B support and the remaining bits will have their DDC2B meanings. DDC2B support is planned beginning with the following production releases.

Product	Production Revision Level
CL-GD5434	Production Revision E
CL-GD5436	Production Revision A
CL-GD5440	Production Revision A

9.3 SR8: EEPROM Control Register *(cont.)*

Bit	Description
5	**Latch ESYNC* and EVIDEO* (EEPROM Configuration):** When this bit is set to '0', the ESYNC and EVIDEO* pins are inputs and control the HSYNC, VSYNC, BLANK*, and P[7:0] drivers in the normal manner. When this bit is set to '1', the input levels on ESYNC* and EVIDEO* are latched internally and these latched levels control the HSYNC, VSYNC, BLANK*, and P[7:0] drivers. This frees the ESYNC* and EVIDEO* pins to control the EEPROM. This bit should be set to '1' prior to setting SR8[4] and it should be set to '0' only after clearing SR8[4]. **Reserved (DDC2B Configuration)**
4	**Enable EEPROM Data and SK (EEPROM Configuration):** When this bit is set to '1', ESYNC* and EVIDEO* become outputs and reflect the values in SR8[2] and SR8[3], respectively. When this bit is set to '0', ESYNC and EVIDEO* are inputs. **Reserved (DDC2B Configuration)**
3	**Data to EEPROM (EEPROM Configuration):** When SR8[4] is set to '1', the level on EVIDEO* will reflect the value of this bit. This bit is typically used to control the DI pin of EEPROM. **Reserved (DDC2B Configuration)**
2	**SK to EEPROM (EEPROM Configuration):** When SR8[4] is set to '1', the level on ESYNC will reflect the value of this bit. This bit is typically used to control the SK pin of EEPROM. **EECS Readback (DDC2B Configuration):** This read-only bit reflects the state of the EECS pin (pin 107).
1	**Enable EEPROM Data In (EEPROM Configuration):** When this bit is set to '1', the level on GPIO0 (EEDI) will be reflected on SR8[7]. **EEDI Output (DDC2B Configuration):** If this bit is set to '0', the EEDI pin will be driven LOW. If this bit is set to '1', the EEDI pin will be high-impedance (a nominal 1K Ω resistor will pull the pin HIGH).
0	**CS Out to EEPROM (EEPROM Configuration):** The level on GPIO1 (EECS) will reflect the value of this bit. **EECS Output (DDC2B Configuration):** If this bit is set to '0', the EECS pin will be driven LOW. If this bit is set to '1', the EECS pin will be high-impedance (a nominal 1K Ω resistor will pull the pin HIGH).

9.4 SR9, SRA: Scratch Pad 0, 1 Registers

I/O Port Address: 3C5

Index: 9, A

Bit	Description	Reset State
7	R/W Data [7]	0
6	R/W Data [6]	0
5	R/W Data [5]	0
4	R/W Data [4]	0
3	R/W Data [3]	0
2	R/W Data [2]	0
1	R/W Data [1]	0
0	R/W Data [0]	0

CAUTION: These two registers are reserved for the exclusive use of the CL-GD543X/'4X BIOS, and must never be written to by any application program. This register description is listed here for completeness only.

Bit	Description
7:0	These bits are reserved for the Cirrus Logic BIOS.

9.5 SRB, SRC, SRD, SRE: VCLK0, 1, 2, 3 Numerator Registers

I/O Port Address: 3C5

Index: B, C, D, E

Bit	Description
7	Reserved
6	VCLK Numerator [6]
5	VCLK Numerator [5]
4	VCLK Numerator [4]
3	VCLK Numerator [3]
2	VCLK Numerator [2]
1	VCLK Numerator [1]
0	VCLK Numerator [0]

These registers, in conjunction with SR1B-SR1E, are used to determine the frequency of video clocks. Refer to Appendix B8, "Dual-Frequency Synthesizer", for complete programming information for the synthesizers.

Bit **Description**

7 **Reserved**

6:0 **VCLK Numerator [6:0]:** The following table shows the values these registers are loaded with at RESET:

Clock	Freq. (MHz)	N	D	P	Numerator	Denominator/ Post-Scalar
VCLK0	25.180	102	29	1	66h	3Bh
VCLK1	28.325	91	23	1	5Bh	2Fh
VCLK2	41.165	69	24	0	45h	30h
VCLK3	36.082	126	25	1	7Eh	33h

9.6 SRF: DRAM Control Register

I/O Port Address: 3C5

Index: F

Bit	Description	Reset State
7	DRAM Bank Switch Control (CL-GD5434/'36 only)	
6	CPU Write Buffer Control	0
5	CRT FIFO Depth Control (5430/'40) only	0
4	DRAM Data Bus Width [1]	0
3	DRAM Data Bus Width [0]	0
2	RAS Timing: MD[57] (Read-only)	CF[9]
1	Reserved	
0	CF12: MD[60] (Read-only)	CF[12]

This register is used to control the display memory.

Bit	Description
7	**DRAM Bank Switch Control (CL-GD5434/'36 only):** When this bit is set to '0', bank switching is disabled. The RAS0*/OE* output will be inactive. When this bit is set to '1', bank switching is enabled. RAS1* will be made active for the first bank (first two Mbytes); RAS0* will be made active for the second bank (second two Mbytes).
6	**CPU Write Buffer Control:** When this bit is set to '0', Fast-Page Detection is enabled. Any CPU writes that can take place as Fast Page mode writes will. If this bit is set to '1' Fast-Page Detection is disabled. CPU writes will never take place as Fast Page mode writes. This bit must be set to '1' when loading font data for the 'page mode' text (132-column and CR1B[6] is set to '1'). This bit is set to '0' in all other circumstances.
5	**CRT FIFO Depth Control (CL-GD5430/'40 only):** When this bit is set to '0', the CRT FIFO depth will be set to eight levels (32 bits/level). This is the default. This will typically be used for standard video modes. Setting this bit to '1' will set the CRT FIFO depth to the maximum for the particular controller. This will be used for extended graphics modes. For the CL-GD5436, this bit is ignored. The CRT FIFO depth is controlled with SR7[0].

9.6 SRF: DRAM Control Register *(cont.)*

Bit **Description**

4:3 **DRAM Data Bus Width [1:0]:** This 2-bit field is used to specify the Display Memory Data bus width as shown in the following table:

SRF[4]	SRF[3]	Data Bus Width	Memory Size (CL-GD5430/'40)	Memory Size (CL-GD5434/'36)
0	0	Reserved	n/a	n/a
0	1	16 bits	512K	n/a
1	0	32 bits	1M	1M
1	1	64 bits	2M	2M / 4M (see bit 7)

These bits have one level of buffering. At the end of each horizontal scanline refresh interval (that is, when Horizontal Blanking begins), these bits are transferred to the timing logic. This avoids changing the timing logic in the middle of a scanline.

2 **RAS Timing MD[57]:** This read-only bit indicates the RAS timing as selected in CF[9]. This is summarized in the following table:

SRF[2] CF[9]	Pull-down on MD[57]	RAS High	RAS Low	Note
0	Yes	3 MCLK	4 MCLK	Extended RAS
1	No	2.5 MCLK	3.5 MCLK	Standard RAS

1 **Reserved**

0 **CF12: MD[60]:** This read-only bit indicates the contents of CF12. See Appendix B9.

9.7 SR10: Graphics Cursor X Position Register

I/O Port Address: 3C5

Index: 10, 30, 50, 70, 90, B0, D0, F0

Bit	Description	Reset State
7	Cursor X [10]	0
6	Cursor X [9]	0
5	Cursor X [8]	0
4	Cursor X [7]	0
3	Cursor X [6]	0
2	Cursor X [5]	0
1	Cursor X [4]	0
0	Cursor X [3]	0

This register, and bits 7:5 of the index used to access it, are used to define the horizontal (X) pixel offset of the Graphics Cursor. Refer to Appendix D3, *Hardware Cursor*, for more information regarding the Graphics Cursor, including code examples.

The data forms the upper-eight bits of the 11-bit position; bits 7:5 of the index form the lower three bits of the 11-bit position. This allows the entire 11-bit cursor offset to be written in a single 16-bit I/O write. The offset must be placed in AX[15-5], AX[4:0] must be 10000, and DX must be 03C4.

The three bits of stored cursor position may be read as follows. Execute a byte write to 3C4 using the data values 10, 30, 50..F0. A read of 3C4 will then return the previously stored three bits of cursor position.

Bit	Description
7:0	**Cursor X [10:3]:** This 8-bit field forms the upper eight bits of the 11-bit horizontal offset of the Graphics Cursor. The index used to access this register forms the low-order three bits of the 11-bit offset.

9.8 SR11: Graphics Cursor Y Position Register

I/O Port Address: 3C5

Index: 11, 31, 51, 71, 91, B1, D1, F1

Bit	Description	Reset State
7	Cursor Y [10]	0
6	Cursor Y [9]	0
5	Cursor Y [8]	0
4	Cursor Y [7]	0
3	Cursor Y [6]	0
2	Cursor Y [5]	0
1	Cursor Y [4]	0
0	Cursor Y [3]	0

This register, and bits 7:5 of the index used to access it, are used to define the vertical (Y) scanline offset of the Graphics Cursor. Refer to Appendix D3, "Hardware Cursor", for more information regarding the Graphics Cursor, including code examples.

The data forms the upper eight bits of the 11-bit position; bits 7:5 of the index form the lower three bits of the 11-bit position. This allows the entire 11-bit cursor offset to be written in a single 16-bit I/O write. The offset must be placed in AX[15:5], AX[4:0] must be '10001', and DX must be 03C4.

The three bits of stored cursor position may be read as follows. Execute a byte write to 3C4 using the data values 11, 31, 51..F1. Then a read of 3C4 will then return the previously stored three bits of cursor position.

Bit	Description
7:0	**Cursor Y [10:3]:** This 8-bit field forms the upper eight bits of the 11-bit vertical offset of the Graphics Cursor. The index used to access this register forms the low-order three bits of the 11-bit offset.

9.9 SR12: Graphics Cursor Attributes Register

I/O Port Address: 3C5

Index: 12

Bit	Description
7	Overscan Color Protect
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Cursor Size Select
1	Allow Access to DAC Extended Colors
0	Graphics Cursor Enable

This register is used to enable or disable the Graphics Cursor, as well as to set the cursor size and to enable the palette DAC table entries used to define the colors. Refer to Appendix D3, "Hardware Cursor", for a complete programming guide for the Graphics Cursor.

Bit	Description
7	**Overscan Color Protect:** If this bit is set to '1', the border color will be DAC LUT entry 258. Note that entry 258 can be accessed only if SR12[1] is set to '1'. If this bit is set to '0', the border color is normal; that is, the contents of the palette pointed to by AR11. AR11 normally contains '0', and palette entry '0' normally contains values corresponding to black.
6:3	**Reserved**
2	**Cursor Size Select:** If this bit is set to '0', the Graphics Cursor will be 32 x 32 pixels. If it is set to '1', the Graphics Cursor will be 64 x 64 pixels (available only with 32 or greater DRAM width).
1	**Allow Access to DAC Extended Colors:** If this bit is set to '1', DAC LUT entries 256 and 257 are accessible as locations X0h and XFh. Entry 256 will be used as the cursor background and entry 257 will be used as the cursor foreground. This provides for a cursor that is completely independent of the display data colors. Entry 258 is accessible as location X2h, and provides a selected overscan (border) color. If this bit is set to '0', the DAC LUT will be VGA-compatible.
0	**Graphics Cursor Enable:** If this bit is set to '1', the Graphics Cursor will be enabled and will appear on the screen. If it is set to '0', the Graphics Cursor will be disabled and will not appear on the screen.

9.10 SR13: Graphics Cursor Pattern Address Offset Register

I/O Port Address: 3C5

Index: 13

Bit	Description
7	Reserved
6	Reserved
5	Cursor Select [5]
4	Cursor Select [4]
3	Cursor Select [3]
2	Cursor Select [2]
1	Cursor Select [1]
0	Cursor Select [0]

This register is used to select one of 64 cursor patterns (32 × 32 cursor) or one of 16 cursor patterns (64 × 64 cursor). Refer to Appendix D3, "Hardware Cursor", for a complete programming guide for the Graphics Cursor.

Bit	Description
7:6	**Reserved**
5:0	**Cursor Select (32 × 32 Cursor) [5:0]:** This 6-bit field is used to select one of 64 possible cursor patterns stored at the top (highest addressed 16K bytes) of display memory. This definition is valid only if SR12[2] is set to '0'.
5:2	**Cursor Select (64 × 64 Cursor) [5:2]:** This 4-bit field is used to select one of 16 possible cursor patterns stored at the top (highest addressed 16K bytes) of display memory. This definition is valid only if SR12[2] is set to '1'. SR13[1:0] are ignored in this case.

9.11 SR14, SR15: Scratch Pad 2, 3 Registers

I/O Port Address: 3C5

Index: 14, 15

Bit	Description	Reset State
7	R/W Data [7]	0
6	R/W Data [6]	0
5	R/W Data [5]	0
4	R/W Data [4]	0
3	R/W Data [3]	0
2	R/W Data [2]	0
1	R/W Data [1]	0
0	R/W Data [0]	0

CAUTION: These two registers are reserved for the exclusive use of the CL-GD543X/'4X BIOS and must never be written to by any application program. These registers are listed here for completeness only.

Bit	Description
7:0	**R/W Data [7:0]:** These bits are reserved for the Cirrus Logic BIOS.

9.12 SR16: Performance Tuning Register

I/O Port Address: 3C5

Index: 16

Bit	Description	Reset State
7	PCI Burst (CL-GD5430/'40)	
6	LRDY Delay (not CL-GD5436)	1
5	Readback of CF6 (not CL-GD5436)	
4	LRDY Delay (not CL-GD5436)	1
3	FIFO Demand Threshold [3]	0
2	FIFO Demand Threshold [2]	0
1	FIFO Demand Threshold [1]	0
0	FIFO Demand Threshold [0]	0

This register is used to control the delay from ADS# to RDY#, and to control the threshold at which the CRT FIFO will be refilled. This register must never be written by an application program.

Bit	Description
7	**PCI Burst (CL-GD5430/'40):** If this bit is set to '1', continuous PCI burst is enabled for BitBLT writes. The target will not stop the burst after four writes. If this bit is set to '0', the maximum burst size for PCI is four. This bit is reserved on the CL-GD5434 and CL-GD5436.
6	**LRDY Delay for I/O Cycles (CL-GD5430/'34):** This field is used to control the delay from ADS# to LRDY# for I/O cycles. This field applies only when the CL-GD543X is configured for VESA VL-Bus. The following table summarizes the values:

SR16[6]	LRDY Delay for I/O Write	LDRY Delay for I/O Read
0	0	1
1	1	2

9.12 SR16: Performance Tuning Register *(cont.)*

Bit **Description**

6 *(cont.)* **LRDY Delay (CL-GD5440):** This bit is used in conjunction with SR16[4] to set the number of wait states for Non-BLT operations.

SR16[6]	SR16[4]	Programmable Wait States
0	0	4 cycles
0	1	5 cycles
1	0	6 cycles
1	1	7 cycles

This bit and SR16[4] are reserved on the CL-GD5436. When the CL-GD5436 is configured for VESA VL-bus, the minimum LRDY delay is always 1 for writes and 2 reads. This applies to both I/O and Memory operations.

5 **Readback of CF6 (not CL-GD5436):** This read-only bit reflects the reset value of CF6 (MD54). Refer to Appendix B9, "Configuration Notes", for additional information. This bit is reserved on the CL-GD5436.

4 **LRDY# Delay for Memory Cycles (CL-GD5430/34):** This field is used to control the minimum delay from ADS# to LRDY# for memory cycles. This field applies only when the CL-GD543X/'4X is configured for VESA VL-Bus. The following table summarizes the values:

SR16[4]	Write ('30/'34)	Read ('30/'34)	Write ('36)	Read ('36)
0	0	1	2	2
1	1	2	1	2

LRDY Delay (CL-GD5440): This bit is used in conjunction with SR16[6] to specify the number of wait states for non-BLT operations.

3:0 **FIFO Demand Threshold [3:0]:** The value written to this field will select the level at which the Sequencer will begin display memory cycles to refill the CRT FIFO (and thereby hold off CPU and BitBLT cycles). In particular, when the FIFO is set for 20 levels, the sequencer will begin to refill the FIFO when there are *n + 16* or fewer valid entries left. For each Video mode and MCLK frequency, there will be an optimum value that will most efficiently use the DRAM.
For the CL-GD5436, this value is in 64 bit FIFO levels, with no offset. For example, when this value is programmed to 1010b (10 decimal), FIFO demand will occur when there are 10 levels (20 DWORDs) remaining in the FIFO.

9.13 SR17: Configuration Readback and Extended Control Register

I/O Port Address: 3C5

Index: 17

Bit	Description	Reset State
7	Reserved	
6	Memory-mapped I/O Address (CL-GD5430/'36/'40 only)	
5	System Bus Select [2]: MD50 (Read-only)	CF[2]
4	System Bus Select [1]: MD49 (Read-only)	CF[1]
3	System Bus Select [0]: MD48 (Read-only)	CF[0]
2	Enable Memory-mapped I/O	
1	DDL DRAM Timing (CL-GD5430/'34/'40)	
0	Shadow DAC Writes on VESA-VL Bus	1

Bit	Description
7	**Reserved:** This bit must always be set to '0'.
6	**Memory-mapped I/O Address (CL-GD5430/'36/'40 only):** If Memory-mapped I/O is not enabled, or if linear addressing is not enabled, this bit is ignored. If linear addressing and Memory-mapped I/O are both enabled, this bit has the following meaning: if this bit is set to '0', the address space for Memory-mapped I/O will be 256 bytes beginning at B800:0. If this bit is set to '1' the address space for Memory-mapped I/O will be the last 256 bytes of linear address space.
5:3	**System Bus Select [2:0]:** This read-only field will reflect Configuration bits CF[2:0], the System Bus Select bits. See Appendix B9, "Configuration Notes", for the definition of these bits. This field is intended for use by the Cirrus Logic BIOS only.
2	**Enable Memory-mapped I/O:** If this bit is set to '0', the CL-GD543X/'4X will operate normally in the sense that the memory-mapped I/O is not enabled. If this bit is set to '1', the BLT registers (GR0, 1, 10-15 and 20-3F) will be addressable as a 36-byte block of memory, allowing faster access. See Appendix B20, "Memory Mapped I/O", for more information. For the CL-GD5430/'40 only, when configured for linear addressing, SR17[6] specifies the location of the block reserved for memory-mapped I/O.

9.13 SR17: Configuration Readback and Extended Control Register *(cont.)*

Bit **Description**

1 **DDL DRAM Timing (CL-GD5430/'34/'40):** If this bit is set to '0', Delayed Data Latch (DDL) DRAM timing will not be enabled. If this bit is set to '1', DDL DRAM timing will be enabled for those Alpines that support it. DDL DRAM timing is supported beginning with the following chip revisions. See the description of GR18[2] for EDO support on the CL-GD5436. See Application Alert 15 for a detailed description of DDL Timing.

Product	Revision
CL-GD5430	Production D
CL-GD5434	Production E
CL-GD5440	Production A

0 **Shadow DAC Writes on VESA-VL Bus:** If this bit is set to '0', writes to the internal DAC will return LBA# and RDY# normally. If this bit is set to '1', writes to the DAC addresses will accept data, but will not return LBA# or RDY#, causing the write to be transferred to an external DAC on the ISA bus. The reset state of this bit is '1'. Reads to the DAC addresses will always operate normally.

9.14 SR18: Signature Generator Control Register

I/O Port Address: 3C5

Index: 18

Bit	Description
7	Disable MCLK Driver
6	Disable DCLK/Pixel Bus Drivers
5	Enable Data Generator
4	Pixel Bus Select [2]
3	Pixel Bus Select [1]
2	Pixel Bus Select [0]
1	Reset Signature Generator
0	Signal Generator Enable/Status

This register is used to control and monitor the status of the Signature Generator. The CL-GD543X/'4X Signature Generator is used for board-level testing of the video subsystem. Refer to Appendix B11 for a complete description of the Signature Generator, including sample code.

Bit	Description
7	**Disable MCLK Driver:** If this bit is set to '1', the MCLK driver is disabled. This is intended for testing only. If this bit is set to '0', the MCLK driver operates normally.
6	**Disable DCLK/Pixel Bus Drivers:** If this bit is set to '1', the DCLK and pixel bus drivers are disabled. This is intended for testing only. If this bit is set to '0', the DCLK and pixel bus drivers operate normally. In addition, if the CL-GD543X/'4X is programmed for video overlay, programming this bit to '1' forces the overlay data to come from the Frame Buffer rather than the Pixel bus. For example, this is useful for changing the mode from VGA-LUT to 3-3-2 RGB. See Appendix B14, "Video Overlay and DAC Mode Switching", for more information.
5	**Enable Data Generator:** If this bit is set to '1', pseudo-random data will be placed on the memory data bus. This is used in conjunction with the Signature Generator. This mode is intended for factory testing only.

9.14 SR18: Signature Generator Control Register *(cont.)*

Bit **Description**

4:2 **Pixel Bus Select [2:0]:** This field is used to select the bit of the pixel bus that will be used as the input for the Signature Generator according to the following table:

SR18[4]	SR18[3]	SR18[2]	P-Bus Bit
0	0	0	P[0]
0	0	1	P[1]
0	1	0	P[2]
0	1	1	P[3]
1	0	0	P[4]
1	0	1	P[5]
1	1	0	P[6]
1	1	1	P[7]

1 **Reset Signature Generator:** When this bit is set to '1', the Signature Generator is reset to an initially-defined condition. When it is set to '0', the Signature Generator is allowed to run under the control of SR18[0].

0 **Signature Generator Enable/Status:** When this bit is set to '1', the Signature Generator will begin operation on the next VSYNC. It will accumulate a signature from the pixel bus bit chosen by SR18[4:2] for one video frame and will then stop, forcing this bit to '0'. The program can determine when the signature is complete by monitoring this bit.

9.15 SR19: Signature Generator Result Low-Byte Register

I/O Port Address: 3C5

Index: 19

Bit	Description	Reset State
7	Signature Generator Result [7]	0
6	Signature Generator Result [6]	0
5	Signature Generator Result [5]	0
4	Signature Generator Result [4]	0
3	Signature Generator Result [3]	0
2	Signature Generator Result [2]	0
1	Signature Generator Result/Byte Select [1]	0
0	Signature Generator Result/Byte Select [0]	0

This register is used to read the low-order byte of the Signature Generator result. The CL-GD543X/'4X Signature Generator is used for board-level testing of the video subsystem. Refer to Appendix B11 for a complete description of the Signature Generator.

Bit	Description
7:0	**Signature Generator Result [7:0]**
1:0	**Byte Select [1:0]**

9.16 SR1A: Signature Generator Result High-Byte Register

I/O Port Address: 3C5

Index: 1A

Bit	Description	Reset State
7	Signature Generator Result [15]	0
6	Signature Generator Result [14]	0
5	Signature Generator Result [13]	0
4	Signature Generator Result [12]	0
3	Signature Generator Result [11]	0
2	Signature Generator Result [10]	0
1	Signature Generator Result [9]	0
0	Signature Generator Result [8]	0

This register is used to read the high-order byte of the Signature Generator Result. The CL-GD543X/'4X Signature Generator is used for board-level testing of the video subsystem. Refer to Appendix B11 for a complete description of the Signature Generator.

Bit	Description
7:0	**Signature Generator Result [15:8]**

9.17 SR1B, SR1C, SR1D, SR1E: Denominator and Post-Scalar Registers

I/O Port Address: 3C5

Index: 1B, 1C, 1D, 1E

Bit	Description
7	Enable 6-bit Denominator ('34 Only)
6	VCLK Denominator [5] ('34 Only)
5	VCLK Denominator [4]
4	VCLK Denominator [3]
3	VCLK Denominator [2]
2	VCLK Denominator [1]
1	VCLK Denominator [0]
0	VCLK Post-Scalar (÷2)

These registers, in conjunction with SRB-SRE, are used to program the frequency of video clocks 0 (VCLK0) through 3 (VCLK3). Refer to Appendix B8, "Dual-Frequency Synthesizer", for complete programming information for the synthesizers. The reset values for these four registers are shown in the VCLK Numerator Table in Section 9.5.

Bit	Description
7	**Enable 6-bit Denominator:** If this bit is set to '0', the denominator is only five bits and bit 6 is ignored. If this bit is set to '1', the denominator is six bits and includes bit 6 as the high-order bit. This provides improved accuracy at low frequencies. This feature is available on the CL-GD5434 only, and only for register SR1B.
6	**VCLK Denominator [5]**
5:1	**VCLK Denominator [4:0]**
0	**VCLK Post-Scalar (÷2)**

9.18 SR1F: MCLK Select Register

I/O Port Address: 3C5

Index: 1F

Bit	Description	Reset State
7	Reserved	0
6	Use MCLK as VCLK	X
5	MCLK Frequency [5]	0
4	MCLK Frequency [4]	(Refer to MCLK Table below)
3	MCLK Frequency [3]	(Refer to MCLK Table below)
2	MCLK Frequency [2]	(Refer to MCLK Table below)
1	MCLK Frequency [1]	(Refer to MCLK Table below)
0	MCLK Frequency [0]	(Refer to MCLK Table below)

This register allows the MCLK frequency to be programmed directly. In addition, bit 7 is used to allow writing to a BIOS flash ROM. This register should never be programmed by an applications program. It is listed for completeness only.

Bit **Description**

7 **Reserved:** This bit must always be set to '0'.

6 **Use MCLK as VCLK:** If this bit is set to '0', the VCLK synthesizer will operate normally. If this bit is set to '1', VCLK is derived from MCLK as follows:

SR1F[6]	SR1E[0]	VCLK Source
0	x	VCLK (normal operation)
1	0	VCLK = MCLK
1	1	VCLK = MCLK ÷ 2

9.18 SR1F: MCLK Select Register *(cont.)*

Bit	Description
5:0	**MCLK Frequency [5:0]:** This field directly programs the MCLK frequency as indicated in the following equation:

$$MCLK = SR1F \bullet \frac{Reference}{8}$$

$$MCLK \cong SR1F \bullet 1.8MHz$$

This field may be programmed with any value from 4 to the specified maximum for each chip. Refer to Appendix B7, "Memory Configuration and Timing", for information regarding the DRAM specifications requirements for various MCLK frequencies. The following table shows examples (assuming a reference frequency of 14.31818 MHz):

SR1F[5:0] (Decimal)	SR1F[5:0] (Hex.)	MCLK Frequency
21	15	37.6 MHz
23	17	41.2 MHz
28	1C	50.1 MHz
30	1E	53.7 MHz
31	1F	55.5 MHz
32	20	57.3 MHz
33	21	59.1 MHz
35	23	62.6 MHz
37	25	66.2 MHz
40	28	71.6 MHz
42	2A	75.2 MHz
45	2D	80.5 MHz

9.19 GR9: Offset Register 0

I/O Port Address: 3CF

Index: 9

Bit	Description	Reset State
7	Offset 0 [7]	0
6	Offset 0 [6]	0
5	Offset 0 [5]	0
4	Offset 0 [4]	0
3	Offset 0 [3]	0
2	Offset 0 [2]	0
1	Offset 0 [1]	0
0	Offset 0 [0]	0

This register is used to provide access to up to 1 Mbyte of display memory with 4K bytes granularity or 4 Mbytes of display memory with 16K bytes granularity. The contents of this register are added to A[19:12] when Extension register GRB[0] is set to '0', and when GRB[0] is set to '1' and SA15 = 0. If GRB[5] is set to '1', bits 6:0 of this register are added to A[20:14] to provide access to up to 4 Mbytes of display memory with 16K bytes granularity. The CL-GD5430/'40 supports up to 2 Mbytes of display memory.

The Display Memory Address, prior to being modified by address wrap controls, is called XMA. It is the sum of XA and an Offset register. XA is the address on the bus with bits 16 and 15 possibly forced to '0' as indicated in the following table:

Configuration	XA[16]	XA[15]	XA[14:0]
64K Memory: GR6[3:2] = 0,1 **and** Offset 1 Disabled: GRB[0] = 0	0	SA[15]	SA[14:0]
64K Memory: GR6[3:2] = 0,1 **or** Offset 1 Enabled: GRB[0] = 1	0	0	SA[14:0]

The XA address is summed with the contents of an Offset register with one of three relative alignments according to the configuration. These are indicated in the following tables:

1 Mbyte Memory, 4K Granularity, VGA Mapping:

0	0	0	XA[16]	XA[15]	SA[14]	SA[13]	SA[12]
+OFF[7]	OFF[6]	OFF[5]	OFF[4]	OFF[3]	OFF[2]	OFF[1]	OFF[0]
XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

9.19 GR9: Offset Register 0 *(cont.)*

2 or 4 Mbyte Memory, 16K Granularity, VGA Mapping:

0	0	0	0	0	XA[16]	XA[15]	SA[14]	SA[13]	SA[12]
+OFF[7]	+OFF[6]	OFF[5]	OFF[4]	OFF[3]	OFF[2]	OFF[1]	OFF[0]	0	0
XMA[21]	XMA[20]	XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

1, 2 or 4 Mbyte Memory, 16K Granularity, Linear Addressing:

LA[21]	LA[20]	LA[19]	LA[18]	LA[17]	SA[16]	SA[15]	SA[14]	SA[13]	SA[12]
+OFF[7]	+OFF[6]	OFF[5]	OFF[4]	OFF[3]	OFF[2]	OFF[1]	OFF[0]	0	0
XMA[21]	XMA[20]	XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

NOTE: Refer to Appendix D1, "Extended Video Modes Programming", for programming notes regarding extended addressing. The CL-GD5430/'40 supports only up to 2 Mbytes of display memory.

Bit	Description
7:0	**Offset 0 [7:0]:** This value is added to A[19:12] to provide the address into display memory. This Offset register is selected when GRB[0] is set to '0' or when GRB[0] is a '1' and SA15 = 0.

9.20 GRA: Offset Register 1

I/O Port Address: 3CF

Index: A

Bit	Description	Reset State
7	Offset 1 [7]	0
6	Offset 1 [6]	0
5	Offset 1 [5]	0
4	Offset 1 [4]	0
3	Offset 1 [3]	0
2	Offset 1 [2]	0
1	Offset 1 [1]	0
0	Offset 1 [0]	0

This register is used to provide access to up to 1 Mbyte of display memory with 4K bytes granularity. The contents of this register are added to A[19:12] when Extension register GRB[0] is set to '1' and SA15 = 1. If GRB[5] is set to '1', bits 6:0 of this register are added to A[20:14] to provide access to up to 2 Mbytes of display memory with 16K bytes granularity.

This provides an additional 32K window into 1 Mbyte of display memory with 4K or 16K granularity.

Bit	Description
7:0	**Offset 1 [7:0]:** This value is added to A[19:12] to provide the address into display memory. This Offset register is selected when GRB[0] is set to '1' and SA15 = 1. If GRB[0] is set to '0', this register is unused.

9.21 GRB: Graphics Controller Mode Extensions Register

I/O Port Address: 3CF

Index: B

Bit	Description
7	Reserved
6	Reserved
5	Offset Granularity
4	Enable Enhanced Writes for 16-bit Pixels
3	Enable Eight Byte Data Latches
2	Enable Extended Write Modes
1	Enable BY8 Addressing
0	Enable Offset Register 1

This register is used to enable or disable extended write modes. These Extended Write modes provide compatibility with older Cirrus Logic non-BLT controllers.

Bit	Description
7:6	**Reserved**
5	**Offset Granularity:** If this bit is set to '1', the Offset registers are redefined as containing bits [6:0] which are added to Address bits [21:14] to provide access to 4Mbytes of display memory with 16K bytes granularity. SR7[4] (low-order bit of 1-Mbyte address page) becomes a 'don't care'. In addition, linear address memory mapping becomes 2 Mbytes on any 2-Mbyte boundary.
4	**Enable Enhanced Writes for 16-bit pixels:** When this bit and GRB[2] are both set to ones, the CL-GD543X/'4X will execute Enhanced Write mode 4 and 5 writes. In particular, • **BY16 Addressing Enabled:** The system address is shifted by four relative to true packed-pixel addressing so that each system byte address points to a different 8 pixel (16 byte) block in display memory. • **16 Byte Transfer Enabled:** Up to 16 bytes (8 pixels) can be written into display memory for each CPU byte transfer. • **GR10 and GR11 Enabled:** GR10 and GR11 are enabled as foreground and background color extensions. • **SR2 Doubling Enabled:** Each bit of SR2 is used as a pixel write mask for two bytes (one pixel). Note that this bit must be set to '0' for any BitBLT on the CL-GD5434.
3	**Enable Eight Byte Data Latches:** If this bit is set to '1', the display memory latches are eight-bytes wide rather than the normal four. Note that this bit must be set to '0' for any BitBLT on the CL-GD5434.

9.21 GRB: Graphics Controller Mode Extensions Register *(cont.)*

Bit	Description
2	**Enable Extended Write Modes:** If this bit is set to '1', the CL-GD543X/'4X will execute an Extended mode write. In particular, • **8 Byte Transfer Enabled:** Up to 8 bytes (8 pixels) can be written into display memory for each CPU byte transferred. If GRB[4] is set to '1', up to 16 bytes can be written for color expansion. • **GR5[2] Enabled:** Extended Write modes 4 and 5 can be enabled. • **GR0 Extended:** Register GR0 is extended from 4 bits to 8 bits. • **GR1 Extended:** Register GR1 is extended from 4 bits to 8 bits. • **SR2 Extended:** Register SR2 is extended from 4 bits to 8 bits. • **GRB[4] Enabled:** GRB[2] must be set to '1' to enable GRB[4]. A side effect of programming this bit from '1' to '0' is to clear GR0[7:4] and GR1[7:4] to '0'.
1	**Enable BY-8 Addressing:** The system address is shifted by three relative to true packed-pixel addressing so that each system byte address points to a different 8-pixel (8-byte) block in display memory. This bit must be set to '0' if GRB[4] is set to '1' (that is, BY-8 and BY-16 addressing must not be selected simultaneously). **NOTE:** This bit must be set to '0' for any BitBLT on the CL-GD5434.
0	**Enable Offset Register 1:** If this bit is set to '1', then SA15 will be used to choose between Offset registers '0' and '1'. If this bit is set to '0', then Offset register '0' will always be chosen regardless of the value of SA15. This bit must always be set to '0' for 1 Mbyte of linear addressing.

9.22 GRC: Color Key Compare Register

I/O Port Address:3CF

Index: C

Bit	Description	Reset State
7	Color Key Compare [7]	1
6	Color Key Compare [6]	1
5	Color Key Compare [5]	1
4	Color Key Compare [4]	1
3	Color Key Compare [3]	1
2	Color Key Compare [2]	1
1	Color Key Compare [1]	1
0	Color Key Compare [0]	1

This register contains an 8-bit value that is compared to the Video Data. A match will cause DAC Mode Switching to be invoked, when Mode Switching 10 or 11 is chosen.

For the CL-GD5430/'34, only a single byte of each pixel is actually compared, as indicated in the following table: Refer to Appendix B14, "Video Overlay and DAC Mode Switching."

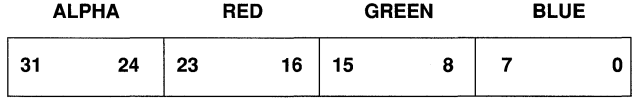
Mode	Bytes Compared	Note
8 bits per pixel	Every Byte	
16 bits per pixel	High Byte	Requires SR7[3:1] = 011
32 bits per pixel	'Alpha' Byte	CL-GD5434/'36 only

For the CL-GD5436/'40 only, both bytes of each 16-bit pixel can be compared. This value is compared with the low byte of the VGA value if 16-bit color compare is selected by programming CR1D[3] to '1'.

Bit **Description**

7:0 **Color Key Compare [7:0]:** This value is the color key used with Mode Switching 10 and 11. Refer to Appendix B14, "Video Overlay and DAC Mode Switching."

The following diagram identifies the Alpha Byte in the 32-bit-per-pixel format. Only the CL-GD5434/'36 supports the Alpha Byte.



9.23 GRD: Color Key Compare Mask Register

I/O Port Address: 3CF

Index: D

Bit	Description	Reset State
7	Color Key Compare Mask [7]	0
6	Color Key Compare Mask [6]	0
5	Color Key Compare Mask [5]	0
4	Color Key Compare Mask [4]	0
3	Color Key Compare Mask [3]	0
2	Color Key Compare Mask [2]	0
1	Color Key Compare Mask [1]	0
0	Color Key Compare Mask [0]	0

This register contains an 8-bit mask under which the Color Key Compare is made. A '1' will cause the corresponding bit to *not* participate in the compare. Refer to Appendix B14, "Video Overlay and DAC Mode Switching."

Bit	Description
7:0	**Color Key Compare Mask [7:0]:** This value is the mask under which the Color Key Compare is made. For the CL-GD5436/'40 only, this value is compared to the high byte of the VGA value if 16-bit color compare is selected by programming CR1D[3] to '1'.

9.24 GRE: Power Management Register

I/O Port Address: 3CF

Index: E

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	System Level Power Management (CL-GD5436 only)
3	Static Clock Mode (CL-GD5436 only)
2	Static VSYNC
1	Static HSYNC
0	DCLK Output ÷2

This register contains bits that are used for Power Management.

Bit	Description
7:5	**Reserved**
4	**System Level Power Management (CL-GD5436 only):** If this bit is set to '1', host access to the display memory is disabled (see MISC[1]) and screen refresh is disabled (see SR1[5]). This bit must be set to '1' prior to setting GRE[3] to '1'. This bit must be set to '0' only after programming GRE[3] to '0'. The MCLK and VCLK VCO's continue to operate at their programmed frequencies, but the chip consumes very little power.
3	**Static Clock Mode (CL-GD5436 only):** If this bit is set to '1', the CL-GD5436 will be placed in Static Clock mode. VCLK and MCLK are gated off, so the chip does not dissipate any dynamic power. DRAM refresh continues. When the chip is in Static Clock mode, memory reads and writes are not valid. I/O accesses other than Palette registers are valid.
2	**Static VSYNC:** If this bit is set to '1', the VSYNC output will be static. The level will be as programmed into MISC[7]. In addition, the DAC will be put into the power-down state. If this bit is set to '0', the VSYNC pin will function as programmed by the CRTC registers. See Appendix B19, "Power Management," for detailed information regarding power management.
1	**Static HSYNC:** If this bit is set to '1', the HSYNC output will be static. The level will be as programmed into MISC[6]. In addition, the DAC will be put into the power-down state. If this bit is set to '0', the HSYNC pin will function as programmed by the CRTC registers. See Appendix B19 for detailed information regarding power management.

9.24 GRE: Miscellaneous Control Register *(cont.)*

Bit	Description
0	**DCLK Output ÷2:** If this bit is set to '0', the CL-GD543X/'4X operates normally. If this bit is set to '1', the CL-GD543X/'4X will simulate external DAC Clocking mode 1. The rising edge of DCLK may be used to clock the low byte of 16-bit data; the falling edge of DCLK may be used to clock the high byte of 16-bit data.

9.25 GR10: Background Color Byte 1 Register

I/O Port Address: 3CF

Index: 10

Memory-mapped I/O Offset: 1h

Bit	Description
7	Background Color [15]
6	Background Color [14]
5	Background Color [13]
4	Background Color [12]
3	Background Color [11]
2	Background Color [10]
1	Background Color [9]
0	Background Color [8]

This register contains the Background Color High-order Byte for 16-bit color expansion or the Green Byte for 32-bit color expansion (CL-GD5434/'36 only).

Bit	Description
7:0	**Background Color [15:8]:** These are the high-order byte for 16-bit color expansion or green byte for 32-bit color expansion (CL-GD5434/'36 only). See Appendix D6 for detailed information regarding color expansion.

9.26 GR11: Foreground Color Byte 1 Register

I/O Port Address: 3CF

Index: 11

Memory-mapped I/O Offset: 5h

Bit	Description
7	Foreground Color [15]
6	Foreground Color [14]
5	Foreground Color [13]
4	Foreground Color [12]
3	Foreground Color [11]
2	Foreground Color [10]
1	Foreground Color [9]
0	Foreground Color [8]

This register contains the Foreground Color High-order Byte for 16-bit color expansion or the Green Byte for 24- or 32-bit color expansion (CL-GD5434/'36 only).

Bit	Description
7:0	**Foreground Color [15:8]:** This is the high-order byte for 16-bit color expansion or the Green Byte for 24- or 32-bit color expansion (CL-GD5434/'36 only). See Appendix D6 for detailed information regarding color expansion.

9.27 GR12: Background Color Byte 2 Register (CL-GD5434/'36 only)

I/O Port Address: 3CF

Index: 12

Memory-mapped I/O Offset: 2h

Bit	Description
7	Background Color [23]
6	Background Color [22]
5	Background Color [21]
4	Background Color [20]
3	Background Color [19]
2	Background Color [18]
1	Background Color [17]
0	Background Color [16]

This register contains the Background Color Red Byte for 32-bit color expansion.

Bit	Description
7:0	**Background Color [23:16]:** This is the Red Byte for 32-bit color expansion. See Appendix D6 for detailed information regarding color expansion.

9.28 GR13: Foreground Color Byte 2 Register (CL-GD5434/'36 only)

I/O Port Address: 3CF

Index: 13

Memory-mapped I/O Offset: 6h

Bit	Description
7	Foreground Color [23]
6	Foreground Color [22]
5	Foreground Color [21]
4	Foreground Color [20]
3	Foreground Color [19]
2	Foreground Color [18]
1	Foreground Color [17]
0	Foreground Color [16]

This register contains the Foreground Color Red Byte for 24- or 32-bit color expansion.

Bit	Description
7:0	**Foreground Color [23:16]:** This is the Red Byte for 24- or 32-bit color expansion. See Appendix D6 for detailed information regarding color expansion.

9.29 GR14: Background Color Byte 3 Register (CL-GD5434/'36 only)

I/O Port Address: 3CF

Index: 14

Memory-mapped I/O Offset: 3h

Bit	Description
7	Background Color [31]
6	Background Color [30]
5	Background Color [29]
4	Background Color [28]
3	Background Color [27]
2	Background Color [26]
1	Background Color [25]
0	Background Color [24]

This register contains the Background Color Alpha Byte for 32-bit color expansion.

Bit	Description
7:0	**Background Color [31:24]:** This is the Alpha Byte for 32-bit color expansion. See Appendix D6 for detailed information regarding color expansion.

9.30 GR15: Foreground Color Byte 3 Register (CL-GD5434/'36 only)

I/O Port Address: 3CF

Index: 15

Memory-mapped I/O Offset: 7h

Bit	Description
7	Foreground Color [31]
6	Foreground Color [30]
5	Foreground Color [29]
4	Foreground Color [28]
3	Foreground Color [27]
2	Foreground Color [26]
1	Foreground Color [25]
0	Foreground Color [24]

This register contains the Foreground Color Alpha Byte for 32-bit color expansion.

Bit	Description
7:0	**Foreground Color [31:24]:** This is the Alpha Byte for 32-bit color expansion. See Appendix D6 for detailed information regarding color expansion.

9.31 GR18: Extended DRAM Controls (CL-GD5430/'36/'40 Only)

I/O Port Address: 3CF

Index: 18

Bit	Description	Reset State
7	Reserved	
6	Enable 16-bit Pixel Bus (CL-GD5436 only)	
5	Enable CD and Overlay Interpolation (CL-GD5436 only)	
4	Tristate DRAM Interface (CL-GD5436 only)	0
3	Single Refresh Cycle (CL-GD5436 only)	0
2	Enable 8-MCLK EDO Timing (CL-GD5436)	0
1	Decreased Write Following Read Timing	0
0	Decreased WE* Active Delay	0

This register contains bits for DRAM timing controls. This register is reset to '0'. This register is implemented on the CL-GD5430/'36/'40 only.

Bit	Description
7	**Reserved**
6	**Enable 16-bit Pixel Bus (CL-GD5436 only):** If this bit is set to '1', the 16-bit pixel bus extension will be enabled on the CL-GD5436 only. This requires that the CL-GD5436 be configured for PCI bus and that the BIOS ROM is disabled by programming PCI30[0] to '0'. When these three conditions are met, the Pixel Bus will be extended to 16 bits for input only. See Appendix B14 for detailed information.
5	**Enable Clock Doubling and Overlay Interpolation (CL-GD5436 only):** If this bit is set to '1', 16-bits from pixel bus can be used to overlay 8-bit LUT data at pixel rates up to 80 MHz. The 16-bit data will be clocked in at 1/2 the pixel rate and interpolation is used to create the extra pixels. This mode must be used with the 16-bit pixel bus extension. See Appendix B14 for detailed information.
4	**Tristate DRAM Interface (CL-GD5436 only):** If this bit is set to '1', the DRAM interface will be forced to high impedance. The pins are MD[63:0], MA[9:0], CAS*[7:0], RAS*[1:0], and WE*. Since this is not synchronized with the DRAM state machine, it is necessary to suppress DRAM activity prior to setting this mode. See GRE[4:3]. The lines must be driven externally to prevent them from floating to the threshold.

9.31 GR18: Extended DRAM Controls (CL-GD5430/'36/'40 only) *(cont.)*

Bit **Description**

3 **Single Refresh Cycle (CL-GD5436 only):** If this bit is set to '1', the CL-GD5436 will generate a single CAS*-before-RAS* refresh cycle per scanline, allowing more MLCK cycles for CPU access. The value programmed into CR11[6] will be ignored. This mode should be enabled only when the horizontal frequency is high enough to guarantee the DRAM refresh period specification is met. If this bit is set to '0', the CL-GD5436 will generate either three or five refresh cycles per scanline according to CR11[6]

2 **Enable 8-MCLK EDO Timing (CL-GD5436):** If this bit is set to '1', the CL-GD5436 will generate CL-GD5436 EDO DRAM timing. It must have been configured for Extended RAS* timing (pull-down installed on MD57). See Appendix B9 for a detailed discussion of EDO support.
In addition, programming this bit to '1' inserts an extra MCLK cycle between read and write CAS* of BLT operations that modify the destination using extended page cycles, such as DST INV.

1 **Decreased Write Following Read Timing:** If this bit is set to '1', the timing for a write CAS* immediately following a read CAS* is reduced by one MCLK. This is enumerated in the following table.

GR18[1]	CL-GD5430/'40	CL-GD5436: GR18[2] =0	CL-GD5436: GR18[2]=1
0	3	3	4
1	2	2	3

0 **Decreased WE* Active Delay:** If this bit is set to '1', the timing to make WE* for a cycle immediately following a read cycle is reduced by one MCLK. This is enumerated in the following table.

GR18[1]	CL-GD5430/'40	CL-GD5436: GR18[2] =0	CL-GD5436: GR18[2]=1
0	2	2	3
1	1	1	2

9.32 GR20, 21: BLT Width Byte 0, 1 Registers[a]

I/O Port Address: 3CF

Index: 20, 21

Memory-mapped I/O Offset: 8, 9h

Bit	Description
7	BLT Width [7]
6	BLT Width [6]
5	BLT Width [5]
4	BLT Width [4] / [12]
3	BLT Width [3] / [11]
2	BLT Width [2] / [10]
1	BLT Width [1] / [9]
0	BLT Width [0] / [8]

This register pair contains the 13-bit value specifying the width-1, in bytes, of the areas involved in a BitBLT. A 13-bit value allows BLT widths of up to 8192 bytes. The CL-GD5430/'40 supports a BLT width of only 11 bits. This register pair is buffered on the CL-GD5436. Refer to Appendix D8, "BitBLT Engine".

Bit	Description
7:0	**BLT Width [12:0]:** Bits 12:8 are in GR21; bits 7:0 are in GR20.

a. Refer to Appendix D8, "BitBLT Engine", for additional information related to Sections 9.32 through 9.42.

9.33 GR22, 23: BLT Height Byte 0, 1 Registers

I/O Port Address: 3CF

Index: 22, 23

Memory-mapped I/O Offset: 0A, 0Bh

Bit	Description
7	BLT Height [7]
6	BLT Height [6]
5	BLT Height [5]
4	BLT Height [4]
3	BLT Height [3]
2	BLT Height [2] /[10]
1	BLT Height [1] / [9]
0	BLT Height [0] / [8]

This register pair contains the 11-bit value specifying height-1, in scanlines, of the areas involved in a BitBLT. An 11-bit field allows BLT Heights of up to 2048 scanlines. This register pair is double-buffered and the contents are not modified by the execution of a BLT. Thus, if multiple BLTs with a common height are being executed, they need not be loaded for each. This is especially useful for polygon fills which are synthesized from multiple single-scanline fills. This field is 10 bits on the CL-GD5430/'34/'40, allowing a BLT Height of up to 1024 scanlines.

Bit	Description
7:0	**BLT Height [10:0]:** Bits 10:8 are in GR23; bits 7:0 are in GR22.

9.34 GR24, 25: BLT Destination Pitch Byte 0, 1 Register

I/O Port Address: 3CF

Index: 24, 25

Memory-mapped I/O Offset: 0C, 0Dh

Bit	Description
7	BLT Destination Pitch [7]
6	BLT Destination Pitch [6]
5	BLT Destination Pitch [5]
4	BLT Destination Pitch [4] / [12]
3	BLT Destination Pitch [3] / [11]
2	BLT Destination Pitch [2] / [10]
1	BLT Destination Pitch [1] / [9]
0	BLT Destination Pitch [0] / [8]

This register pair contains the 13-bit value specifying the Pitch (that is, the scanline-to-scanline byte address offset) of the destination area involved in a BitBLT. This register pair is buffered on the CL-GD5436.

Bit	Description
7:0	**BLT Destination Pitch [12:0]:** Bits 12:8 are in GR25; bits 7:0 are in GR24. **NOTE:** The CL-GD5434 production Revision D or earlier requires that any screen-to-screen BitBLT that does not involve color expansion must have the low-order three bits of GR25 set to '0'.

9.35 GR26, 27: BLT Source Pitch Byte 0, 1 Registers

I/O Port Address: 3CF

Index: 26, 27

Memory-mapped I/O Offset: 0E, 0Fh

Bit	Description
7	BLT Source Pitch [7]
6	BLT Source Pitch [6]
5	BLT Source Pitch [5]
4	BLT Source Pitch [4] / [12]
3	BLT Source Pitch [3] / [11]
2	BLT Source Pitch [2] / [10]
1	BLT Source Pitch [1] / [9]
0	BLT Source Pitch [0] / [8]

This register pair contains the 13-bit value specifying the Pitch (that is, the scanline-to-scanline byte address offset) of the source area involved in a BitBLT. This register pair is buffered on the CL-GD5436.

Bit	Description
7:0	**BLT Source Pitch [7:0]:** Bits 12:8 are in GR27; bits 7:0 are in GR26. **NOTE:** The CL-GD5434 production Revision D or earlier requires that any screen-to-screen BitBLT that does not involve color expansion must have the low-order three bits of GR27 set to '0'.

9.36 GR28, 29, 2A: BLT Destination Start Byte 0, 1, 2 Registers

I/O Port Address: 3CF

Index: 28, 29, 2A

Memory-mapped I/O Offset: 10, 11, 12h

Bit	Description
7	BLT Destination Start [7] / [15]
6	BLT Destination Start [6] / [14]
5	BLT Destination Start [5] / [13] / [21]
4	BLT Destination Start [4] / [12] / [20]
3	BLT Destination Start [3] / [11] / [19]
2	BLT Destination Start [2] / [10] / [18]
1	BLT Destination Start [1] / [9] / [17]
0	BLT Destination Start [0] / [8] / [16]

This register triplet contains the 22-bit value specifying the byte address of the beginning destination pixel for a BitBLT. A 22-bit value allows an address of up to 4 Mbytes. The CL-GD5430/'40 is limited to 2 Mbytes, a 21-bit value. This register triplet is buffered on the CL-GD5436.

Bit	Description
7:0	**BLT Destination Start [21:0]:** Bits 21:16 are in GR2A, bits 15:8 are in GR29, and bits 7:0 are in GR28. For the CL-GD5430/'40, register GR2A contains only five bits.

9.37 GR2C, 2D, 2E: BLT Source Start Byte 0, 1, 2 Registers

I/O Port Address: 3CF

Index: 2C, 2D, 2E

Memory-mapped I/O Offset: 14, 15, 16h

Bit	Description
7	BLT Source Start [7] / [15]
6	BLT Source Start [6] / [14]
5	BLT Source Start [5] / [13] / [21]
4	BLT Source Start [4] / [12] / [20]
3	BLT Source Start [3] / [11] / [19]
2	BLT Source Start [2] / [10] / [18]
1	BLT Source Start [1] / [9] / [17]
0	BLT Source Start [0] / [8] / [16]

This register triplet contains the 22-bit value specifying the byte address of the beginning source pixel for a BitBLT. A 22-bit value allows an address of up to 4 Mbytes. The CL-GD5430/'40 supports only up to 2 Mbytes, a 21-bit value. This register triplet is buffered on the CL-GD5436.

Bit	Description
7:0	**BLT Source Start [21:0]:** Bits 21:16 are in GR2E, bits 15:8 are in GR2D, and bits 7:0 are in GR2C. For the CL-GD5430/'40, register GR2E contains only five bits. **NOTE:** For the CL-GD5430/'40, GR2C must be written when programming a system-to-screen BitBLT with color expansion. Any data value may be used.

9.38 GR2F: BLT Destination Write Mask Register (CL-GD5430/'36/'40 only)

I/O Port Address: 3CF

Index: 2F

Memory-mapped I/O Offset: 17h

Bit	Description
7	Reserved
6	System-to-Screen DWORD [1] (CL-GD5436 only)
5	System-to-Screen DWORD [0] (CL-GD5436 only)
4	Packed-24 Write Mask [1] (CL-GD5436 only)
3	Packed-24 Write Mask [0] (CL-GD5436 only)
2	Destination Write Mask [2]
1	Destination Write Mask [1]
0	Destination Write Mask [0]

This register contains a three -bit field that suppresses writing to the first 'n' pixels (or bytes) of color-expanded data to an aligned destination area. This register is for the CL-GD5430/'36/'40 only, and supports Color Expansion with left edge clipping. For the CL-GD5436 only, it also contains a two-bit field that expands the write mask to 5 bits for Packed-24 modes only. For the CL-GD5436 only, it also contains to two-bit field that specifies the byte alignment of the first byte for each scan line. See Appendix D8 for detailed information.

Bit	Description
7	**Reserved**
6:5	**System-to-Screen DWORD Pointer [1:0] (CL-GD5436 only):** This two bit field specifies the position of the first byte within the first DWORD of each destination scanline. This allows data which is unaligned in system memory to be transferred without the overhead of unaligned bus cycles. If this field is programmed to a non-zero value for a color-expand BLT, GR33[0] must be programmed to '1'.
4:3	**Packed-24 Byte Write Mask [1:0] (CL-GD5436 only):** For the CL-GD5436 only, this two bit field expands the write mask contained in bit 2:0. This is used for color expansion in Packed-24 modes only. The resulting five-bit field is a byte mask.
4:0	**Destination Write Mask [2:0]:** This two-bit field can be used to prevent writing the first n pixels (up to 7) of each scanline for a color-expanded or pattern copy BLT. For the CL-GD5436 only, this field can be expanded to 5 bits with bit 4:3 in Packed-24 modes. In these modes, the field is a count of bytes, not pixels.

9.39 GR30: BLT Mode Register

I/O Port Address: 3CF

Index: 30

Memory-mapped I/O Offset: 18h

Bit	Description
7	Enable Color Expand
6	Enable 8 x 8 Pattern Copy
5	Color Expand Width [1]
4	Color Expand Width [0]
3	Enable Color Expand with Transparency
2	BLT Source Display/System Memory
1	Reserved
0	BLT Direction

This register contains the bits that specify the details, but not the ROP, of the BLT. See Appendix D8 for more information regarding these bits.

Bit	Description
7	**Enable Color Expand:** If this bit is set to '1', the ROP source will be the expanded result from the bit-mapped source. The destination must be screen memory and the direction must be 'increment'. The Extended Write modes 4 and 5 Color registers at GR0, GR1, and GR10-GR15 are used for the bit-map color-expand BLT operations. For the CL-GD5430/'40, the color registers are GR1, GR10, and GR11 only. All ROPs are available. When the source data is expanded, the most-significant-bit of the first source byte will become the first pixel in the screen destination. When the source of color-expand data is display memory, the source starting address must be on an eight-byte boundary, and the source will be taken as a string of bytes (the source pitch will be ignored). If this bit is set to '0', the ROP source will be the pixel data read from the source.

9.39 GR30: BLT Mode Register *(cont.)*

Bit **Description**

6 **Enable 8 × 8 Pattern Copy:** If this bit is set to '1', the source pattern will be copied repeatedly to the destination rectangular area. The source pattern must be aligned on a boundary which is equal to the size of the pattern. The source must be display memory. The source will be a linear string of bytes, in one of five arrangements as shown in the following table:

Case	Arrangement	Note
Color Expansion	8 bytes of bitmap for 64 pixels	
8-bit pixels	64 bytes of color data for 64 pixels	
16-bit pixels	128 bytes of color data for 64 pixels	
24-bit pixels	8 × (24 bytes + 8 bytes filler per scanline)	CL-GD5436 only
32-bit pixels	256 bytes of color data for 64 pixels	CL-GD5434/'36 only

5:4 **Color Expand Width [1:0]:** This 2-bit field controls the width of color expand BLTs according to the following table:

GR30[5]	GR30[4]	Color Expansion Width	Note
0	0	8 bits per pixel	
0	1	16 bits per pixel	
1	0	24 bits per pixel	CL-GD5436 only
1	1	32 bits per pixel	CL-GD5434/'36 only

3 **Enable Color Expand with Transparency:** If this bit is set to '1', then zeroes in the monochrome image being expanded will result in the corresponding pixel not being written to. Only the foreground is written. If this bit is set to '0', then zeroes in the monochrome image being expanded will result in the background color being written to the corresponding pixel. See Appendix D8 for programming differences between the CL-GD5430/'40 and CL-GD5434/'36.

9.39 GR30: BLT Mode Register *(cont.)*

Bit	Description
2	**BLT Source Display/System Memory:** If this bit is set to '1', the BLT source will be system memory rather than display memory. The CPU will perform the system bus transfers; the CL-GD543X/'4X will ignore the address provided with such transfers. The CPU must use DWORD transfers. For system-screen BLTs without color expansion, up to three bytes of the last DWORD for each scanline will be ignored. For system-to-screen BLTs with color expansion, bytes left over at the end of a scanline will be used at the start of a new scanline. Individual bits left at the end of a scanline will be ignored. For the CL-GD5436 only, see the description of GR33[0]. The transfers must always be programmed as DWORD operations. If this bit is set to '0', the BLT source will be display memory.
1	**Reserved:** This bit must be set to '0'.
0	**BLT Direction:** If this bit is set to '1', the source and destination addresses will be decremented rather than incremented as the BLT proceeds. That is, the operation will proceed from right to left and bottom to top. This is intended for screen-to-screen BitBLTs only. In this case, the starting address will be the highest addressed byte in each area. Neither Color Expansion nor Pattern Copy can be used in this case. If this bit is set to '0', the source and destination addresses will be incremented. The BLT will proceed from lower addresses to higher addresses.

9.40 GR31: BLT Start/Status Register

I/O Port Address:3CF

Index: 31

Memory-mapped I/O Offset: 40h

Bit	Description
7	Enable Autostart (CL-GD5436 only)
6	Reserved
5	Pause (CL-GD5436 only)
4	Buffered Register Status (Read-only) (CL-GD5436 only)
3	BLT Progress Status (Read-only)
2	BLT Reset
1	BLT Start
0	BLT Status (Read-only)

This register contains bits that control the BitBLT as well as status bits.

Bit	Description
7	**Enable Autostart (CL-GD5436 only):** If this bit is set to '1', a BLT will start automatically whenever the engine is not busy and a set of parameters is available in the buffered registers. See Appendix D8 for detailed information regarding the BitBLT engine. If this bit is set to '0', BitBLTs will be started when GR31[1] is set to '1'.
6	**Reserved**
5	**Pause (CL-GD5436 only):** If this bit is set to '1', a system-to-screen BLT will pause. Writes to the display memory address range will be taken as ordinary display memory writes; the address supplied by the processor will be used as the entire address. This may be used to change the hardware cursor in response to a mouse interrupt during a system to screen BLT. Reads are not permitted and will return invalid data. If this bit is set to '0', writes to the display memory address range will go to the BitBLT engine (if a system-to-screen BLT requires additional data to complete).
4	**Buffered Register Status (Read-only) (CL-GD5436 only):** This bit will be '1' if the buffered registers are loaded and waiting for their BLT to start. See Appendix D6 for detailed information. This bit will be '0' if the buffered registers are available.
3	**BLT Progress Status (Read-only):** This bit will be set to '1' at the start of a BLT and will be reset to '0' when the entire operation completes. If the BLT is **suspended** (Refer to GR31[1]), this bit will remain '1'. If the BLT is **reset** (Refer to GR3[2]), this bit will be reset to '0'.

9.40 GR31: BLT Start/Status Register *(cont.)*

Bit	Description
2	**BLT Reset:** If this bit is set to '1', the entire BLT engine will be immediately reset and any operation in progress will be terminated. The operation *cannot* be restarted.
1	**BLT Start:** When this bit is set to '1', the BLT will begin with the next available display memory cycle. This bit will be cleared to '0' when the BLT is completed. If the write buffer is not empty when a BitBLT is started, the BitBLT will not take place properly. Any writes to DRAM that must occur should be programmed before the registers are programmed. This will allow the write buffer to empty before the operation begins.
0	**BLT Status (Read-only):** If this bit is '1', the BLT is in progress. If this bit is '0', the BLT is complete or has been successfully suspended.

9.41 GR32: BLT Raster Operation (ROP) Register

I/O Port Address: 3CF

Index: 32

Memory-mapped I/O Offset: 1Ah

Bit	Description
7	f [7]
6	f [6]
5	f [5]
4	f [4]
3	f [3]
2	f [2]
1	f [1]
0	f [0]

This register selects one of 16 two-operand Raster Operations. Raster Operations that do not use the Source (such as ~D) must not be used when color expansion is selected.

Bit **Description**

7:0 **f [7:0]:** This eight-bit value selects a two-operand ROP, as indicated in the table below. Observe that the value programmed into GR32 is identical for the cases of Source/Pattern where the actual logical operation is the same. This table is ordered by Microsoft ROP.

Z RPN	Z	ROP (hex)	Microsoft® Name	Microsoft® ROP
0	0	00	BLACKNESS	00000042
DPon	~P.~D	90	–	000500A9
DPna	~P.D	50	–	000A0329
Pn	~P	D0	–	000F0001
DSon	~S.~D	90	NOTSRCERASE	001100A6
DSna	~S.D	50	–	00220326
Sn	~S	D0	NOTSRCCOPY	00330008
SDna	S.~D	09	SRCERASE	00440328
PDna	P.~D	09	–	00500325
Dn	~D	0B	DSTINVERT	00550009
DPx	P~=D	59	PATINVERT	005A0049
DPan	~P+~D	DA	–	005F00E9
DSx	S~=D	59	SRCINVERT	00660046

9.41 GR32: BLT Raster Operation (ROP) Register *(cont.)*

Bit **Description**

7:0 *(cont.)*

Z RPN	Z	ROP (hex.)	Microsoft® Name	Microsoft® ROP
DSan	~S+~D	DA	–	007700E6
DSa	S.D	05	SRCAND	008800C6
DSxn	S=D	95	–	00990066
DPa	P.D	05	–	00A000C9
PDxn	P=D	95	–	00A50065
D	D	06	–	00AA0029
DPno	~P+D	D6	–	00AF0229
DSno	~S+D	D6	MERGEPAINT	00BB0226
S	S	0D	SRCCOPY	00CC0020
SDno	S+~D	AD	–	00DD0228
DSo	S+D	6D	SRCPAINT	00EE0086
P	P	0D	PATCOPY	00F00021
PDno	P+~D	AD	–	00F50225
DPo	P+D	6D	–	00FA0089
1	1	0E	WHITENESS	00FF0062

NOTES: In the first two columns, **D** denotes destination, **S** denotes source, and **P** denotes pattern.
The first column is RPN (reverse polish notation). **a** denotes 'and', **o** denotes 'or', **x** denotes 'exclusive or', and **n** denotes 'not'. For example, the second entry, DPon, would be interpreted as follows: Destination, (enter), Pattern, oR, nOT.
The second column is provided as a service for those who prefer to avoid RPN. ~ denotes 'not', **.** denotes 'and', and **+** denotes 'or'. For example, the second entry would be interpreted as follows: NOT pattern AND NOT destination. (Demorgan's theorem states that these two interpretations are equivalent.)

9.42 GR33: BLT Mode Extensions Register

I/O Port Address: 3CF

Index: 33

Memory-mapped I/O Offset: 1Bh

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Enable Solid Color Fill (CL-GD5436 only)
1	Invert Color Expand Source Sense (CL-GD5436 only)
0	Source Data Granularity (CL-GD5436 only)

This register contains some extended mode controls.

Bit	Description
7:3	**Reserved**
2	**Enable Solid Color Fill (CL-GD5436 only):** If this bit is set to '1', the destination area (rectangle) is filled with the foreground color. GR30[7] and GR30[6] must be set to '1's. GR30[3] must be set to '0' (no transparency). This function yields identical results as a color expanded, pattern-fill BLT with a pattern of all '1's, but is faster. If this bit is set to '0', this function is not enabled.
1	**Invert Color Expand Source Sense (CL-GD5436 only):** If this bit is set to '1', the sense of the CPU data for a color expanded BLT with transparency is inverted. A '1' will cause the pixel not to be written and a '0' will cause the foreground color to be written.
0	**Source Data Granularity (CL-GD5436 only):** If this bit is set to '1', DWORD granularity is enabled for color expanded system-to-screen BLTs. At the end of each scanline, unused source data will be discarded to the end of the current DWORD. The next scanline will begin with the next DWORD. Up to 31 bits may be discarded. If this bit is set to '0', unused source data to the end of the current BYTE will be discarded at the end of each scanline. This affects color expanded System-to-screen BLTs only. System-to-screen BLTs that do not use color expansion always discard to the end of the current DWORD. This bit must be set to '1' for any color expand BLT for which the GR32f[6:5] field is non-zero.

9.43 CR19: Interlace End Register

I/O Port Address: 3?5

Index: 19

Bit	Description
7	Interlace End [7]
6	Interlace End [6]
5	Interlace End [5]
4	Interlace End [4]
3	Interlace End [3]
2	Interlace End [2]
1	Interlace End [1]
0	Interlace End [0]

This register is used to hold the ending horizontal character count for the odd field VSYNC.

Bit	Description
7:0	**Interlace End:** This value is the number of characters in the last scanline of the odd field in interlaced timing. This can be adjusted to center the scanlines in the odd field halfway between scanlines in the even field. This register is typically set to approximately half the horizontal total.

9.44 CR1A: Miscellaneous Control Register

I/O Port Address: 3?5

Index: 1A

Bit	Description
7	Vertical Blank End Overflow [9]
6	Vertical Blank End Overflow [8]
5	Horizontal Blank End Overflow [7]
4	Horizontal Blank End Overflow [6]
3	Overlay/DAC Mode Switching Control [1]
2	Overlay/DAC Mode Switching Control [0]
1	Enable Double Buffered Display Start Address
0	Enable Interlaced

This register contains timing overflow bits as well as some miscellaneous control bits.

Bit **Description**

7:6 **Vertical Blank End Overflow [9:8]:** This 2-bit field is used to extend the vertical blank end value to 10 bits. Refer to the description in Chapter 6 of CR0 for a table containing all the timing value bits. These bits are enabled only if CR1B[5] is set to '1', or if CR1B[7] is set to '1'.
These two bits are intended for use when CR1B[5] is set to '1' and the blank counters are used to control OVRW*.

5:4 **Horizontal Blank End Overflow [7:6]:** This 2-bit field is used to extend the horizontal blanking end value to eight bits. Refer to Chapter 6 for a description of CR0 and a table containing all the timing value bits. These bits are enabled only if CR1B[5] is set to '1', or if CR1B[7] is set to '1'.
These two bits are intended for use when CR1B[5] is set to '1' and the blank counters are used to control OVRW*.

3:2 **Overlay/DAC Mode Switch Control [1:0]:** This field is used to select the Overlay and DAC Mode Switch term. The values are summarized in the following table. Refer to Appendix B14, "Video Overlay and DAC Mode Switching", for further information.

CR1A[3]	CR1A[2]	Switch enabled with	P[7:0]
0	0	Normal Operation (Switch Disabled)	Outputs
0	1	Timing: (EVIDEO* or OVRW*)	Inputs
1	0	Timing ANDed with Color Key	Inputs
1	1	Color Key only	Inputs

9.44 CR1A: Miscellaneous Control Register *(cont.)*

Bit	Description
1	**Enable Double Buffered Display Start Address:** If this bit is set to '1', the display start address will be updated on the VSYNC following a write to start address low. This provides control of display frame switching without the need to explicitly monitor VSYNC.
0	**Enable Interlaced:** If this bit is set to '1', interlaced timing is enabled. Interlaced timing means interlaced sync in Text mode, and interlaced sync and video data in Graphics mode. In addition, IRQ requests are generated only at the end of odd fields; that is, at the end of a frame. For interlaced sync and data in Graphics mode, the CRTC Scan Double (CR9[7]) must be set to '0'. Graphics modes 4 and 6 must always be non-interlaced.

9.45 CR1B: Extended Display Controls Register

I/O Port Address: 3?5

Index: 1B

Bit	Description
7	Enable Blank End Extensions
6	Enable Text Mode Fast-page
5	Blanking Control
4	Offset Register Overflow 8
3	Screen Start A Address Bit 18
2	Screen Start A Address Bit 17
1	Enable Extended Address Wrap
0	Extended Display Start Address Bit 16

This register contains a number of bits that control extended display functions.

Bit	Description
7	**Enable Blank End Extensions:** If this bit is set to '0', the Vertical and Horizontal Blank End Extension bits in CR1A are disabled if CR1B[5] is also '0'. If this bit is set to '1', the Vertical and Horizontal Blank End Extension bits in CR1A are enabled, regardless of programming the CR1B[5].
6	**Enable Text Mode Fast-page:** If this bit is set to '0', all font fetch cycles occur as random read cycles. This bit must be set to '0' for standard VGA dual-font operation. If this bit is set to '1', Fast-page mode cycles will be used to fetch font data. This allows for Text modes with a VCLK greater than 30 MHz, as is required for 132-column modes.
5	**Blanking Control:** If this bit is set to '0', the DAC blanking will be controlled by the Blanking Signal generated by the CRTC. In this case, the border can be used (Refer to Chapter 8 for a description of AR11). If this bit is set to '1', the DAC Blanking will be controlled by Display Enable. The DAC will be blanked during the time when the border is normally displayed. In addition, the OVRW* pin will follow the blanking signal generated by the CRTC. This signal may be directed to the feature connector or may be used to control an external overlay circuit. Finally, programming this bit to '1' enables the Vertical and Horizontal Blank End Extension bits in CR1A. Refer to Appendix B14, "Video Overlay and DAC Mode Switching" for details.

9.45 CR1B: Extended Display Controls Register *(cont.)*

Bit	Description
4	**Offset Register Overflow 8:** This bit extends the CRTC Offset register (CR13) by one bit. Refer to the description of CR0 in Chapter 6 (Table 6–1) for a summary of CRTC Timing register. This bit allows for offsets of greater than 2048 bytes, and should be used with 24-bit color modes to simplify pixel address calculations.
3:2	**Screen Start A Address [18:17]:** These two bits extend the Screen Start A Address.
1	**Enable Extended Address Wrap:** If this bit is set to '0', the Display Memory Address wraps at 64K maps (256K total memory). This provides VGA compatibility. If this bit is set to '1', the Display Memory Address wraps at the total available memory size. In particular, this bit provides the following functions: If this bit is set to '1', and Chain-4 addressing is selected (SR4[3]=1), then DRAM Addresses A0 and A1 are supplied from Addresses XMA[16] and XMA[17]. XMA[18:12] Addresses are the sum of XA[16:12] and either Offset register 0 or 1. If this bit is set to '1' and CRTC Double-word Addressing is selected (CR14[6]=1), then DRAM Addresses A0 and A1 are supplied from CRTC Addresses CR[14] and CR[15]. This provides four displayable pages in Video mode 13h. Character Counter Addresses CA[16] and CA[18] provide up to 256K bytes in each bit plane, or 1 Mbyte of packed-pixel memory. If this bit is set to '0', the CRTC Character Address Counter is 16-bits-wide, providing VGA compatibility. If this bit is set to '1', the CRTC Character Address Counter is 19-bits-wide.
0	**Extended Display Start Address Bit 16:** This is bit 16 of the Extended Display Start Address.

9.46 CR1C: Sync Adjust and GENLOCK Register (CL-GD5434/'36 only)

I/O Port Address: 3?5

Index: 1C

Bit	Description
7	Enable VSYNC GENLOCK
6	Enable HSYNC GENLOCK
5	Horizontal Total Adjust [2]
4	Horizontal Total Adjust [1]
3	Horizontal Total Adjust [0]
2	Horizontal Sync Start Adjust [2]
1	Horizontal Sync Start Adjust [1]
0	Horizontal Sync Start Adjust [0]

This register is used to enable GENLOCK, and for horizontal timing adjustments.

Bit	Description
7	**Enable VSYNC GENLOCK:** If this bit is set to '1', VSYNC GENLOCK is enabled. The VSYNC pin becomes an input. See Appendix B17, "GENLOCK Support". If the CL-GD543X is programmed for interlaced operation, the first transition sampled after this bit has been set to '1' will also clear the interlace field state to 'even'.
6	**Enable HSYNC GENLOCK:** If this bit is set to '1', HSYNC GENLOCK is enabled. The HSYNC pin becomes an input. The value programmed into the Horizontal Total register must be so that the external HSYNC will occur before the programmed value is reached. This function is independent of VSYNC GENLOCK. Either VSYNC GENLOCK or Horizontal GENLOCK is used with an external VCLK derived externally from the video source and supplied to DCLK (EDCLK is Low). MISC register 3C2[3:2] must be set to '1X' so that the externally generated DCLK drives the CRT Controller as well as the DAC. The external master supplies HSYNC and VSYNC to the display as well as to the CL-GD543X.

9.46 CR1C: Sync Adjust and GENLOCK Register *(cont.)*

Bit **Description**

5:3 **Horizontal Total Adjust [2:0]:** This field allows for a -3/+4 VCLK adjustment of the programmed Horizontal Total. The length of the character, which occurs two character clocks after the Horizontal Counter has reached the value programmed into Horizontal Total, is adjusted according to this field. The following table shows this adjustment:

CR1C[5:3]	Character Clock Adjustment
000	0 (Normal)
001	-3 VCLKs
010	-2 VCLKs
011	-1 VCLKS
100	+1 VCLKS
101	+2 VCLKS
110	+3 VCLKs
111	+4 VCLKS

2:0 **Horizontal Sync Start Adjust [2:0]:** This field allows a 0-7 VCLK adjustment of the position of Horizontal Sync Start (relative to BLANK). HSYNC is delayed an additional number of VCLKs programmed in this field. The HSYNC width is still adjustable only in Character Clock increments.

9.47 CR1D: Overlay Extended Control Register

I/O Port Address: 3?5

Index: 1D

Bit	Description
7	Screen Start A Address [19] (CL-GD5434/'36 only)
6	Overlay Timing Signal Source (CL-GD5430/'36/'40 only)
5	Color Key Compare Type [1] (CL-GD5434/'36 only)
4	Color Key Compare Type [0] (CL-GD5434/'36 only)
3	Overlay Clocking Mode (CL-GD5434)/Color Compare Width (CL-GD5436/'40)
2	DAC Mode Switching Control [1]
1	DAC Mode Switching Control [0]
0	Enable Alpha Overlay (CL-GD5434 only)

This register contains a number of bits that extend the Overlay functions.

Bit **Description**

7 **Screen Start A Address [19] (CL-GD5434/'36 only):** This is bit 19 of the Display Start Address. Refer to the description of CRD in Chapter 6 (Table 6–1) for a summary of CRTC Timing register.

6 **Overlay Timing Signal Source (CL-GD5430/'36/'40 only):** If this bit is set to '0', the EVIDEO* input is used as the timing signal for Overlay modes 01 and 10. This is the default.

If this bit is set to '1', the internally generated OVRW* signal is used as the timing signal for Overlay modes 01 and 10. This avoids the requirement to connect OVRW* to EVIDEO*.

5:4 **Color Key Compare Type [1:0] (CL-GD5434/'36 only):** This 2-bit field chooses the type of comparison done between the pixel data and the Color Key register (GRC) according to the following table:

CR1D[5:4]	Comparison	Note
00	Pixel Data = GRC	Logical
01	Pixel Data < GRC	Arithmetic
1x	Pixel Data > GRC	Arithmetic

9.47 CR1D: Overlay Extended Control Register *(cont.)*

Bit	Description
3	**Overlay Video Clocking Mode (CL-GD5434 Only):** This bit controls the Clocking mode for data on the P[7:0] bus when the CL-GD5434 is operating in Dynamic Overlay mode. If this bit is set to '0', one byte of data will be latched on every rising edge of DCLK. If this bit is set to '1', a low-byte of data will be latched on the rising edge of DCLK and a high-byte of data will be latched on the falling edge of DCLK. This operates to a maximum frequency of 25 MHz. **Color Compare Width (CL-GD5436/'40 Only):** If this bit is set to '1', and the SR7[2:1] field is set to '1,1', all 16 bits of each pixel will be used for the color key compare. The low byte of the VGA data will be compared to the value in GRC and the high byte of the VGA data will be compared to the value in GRD. Since GRD is used as the high byte comparand, no mask is available. This feature is not available when the SR7[2:1] field is programmed for the 16- or 24-bit serial modes.
2:1	**DAC Mode Switching Control [1:0]:** This 2-bit field controls DAC Mode Switching. This controls only the DAC Mode switching; the enabling of video overlay is still done as programmed in CR1A[3:2].
0	**Enable Alpha Overlay (CL-GD5434/'36 only):** If this bit is set to '1', the high byte of the 32-bit pixel will be used for overlay rather than the P-bus. For the CL-GD5436 only, the alpha byte will also be driven onto the P-bus. This is the only overlay configuration in which the P[7:0] are outputs.

CR1D[2:1]	DAC Mode Switching
00	Follows Switch as programmed in CR1A
01	Opposite Switch as programmed in CR1A
1x	Disable DAC Mode Switching

9.48 CR1E: Video Port Configuration (CL-GD5440 only)

I/O Port Address: 3?5

Index: 1E

Bit	Description
7	Closed Caption Enable
6	Interlaced Video Capture
5	Field Capture Enable
4	AccuPak Encode
3	Video Port Transfer Mode [1]
2	Video Port Transfer Mode [0]
1	Video Port Configuration [1]
0	Video Port Configuration [0]

This register is used to configure the video port.

Bit	Description
7	**Closed Caption Enable:** If video capture is enabled by setting bits 1:0 of this register to '1,1', this bit controls closed caption enable. If this bit is set to '1', a single scanline of closed caption information is captured at the start of the ODD interlaced field. See Appendix B10 for further information
6	**Interlaced Video:** If video capture is enabled by setting bits 1:0 of this register to '1,1', this bit enables interlaced video capture. If this bit is set to '1', the video capture address controller will operate in interlaced mode. See Appendix B10 for further information.
5	**Field Capture Enable:** If video capture is enabled by setting bits 1:0 of this register to '1,1', this bit enables the actual capture. If this bit is set to '1', the field of video data following the next trailing video port vertical sync will be captured. If this bit is set to '0', the next field will not be captured.

9.48 CR1E: Video Port Configuration *(cont.)*

Bit **Description**

3:2 **Video Port Transfer Mode [1:0]:** This 2-bit field specifies the transfer mode of the video port.

If video overlay is enabled (CR1E[1:0] = '01', this field specifies the clocking mode for data on the pixel bus (DCLK is configured as an output)).

VPTM[1:0]	DCLK	VGA Pixel Clock	Data Latched
00	VCLK	VCLK	Rising Edge
01	VCLK/2	VCLK	Rising Edge
10	VCLK VCO (before post-scalar)	VCLK VCO (after post-scalar)	Rising Edge
11	Reserved		

If video capture is enabled (CR1E[1:0] = '11', this field specifies the video port transfer mode. See Appendix B10 for the pin descriptions.

CR1E[3:2]	DCLK Edge(S)	Prescale
00	Rising	Disabled
01	Rising	Enabled
10	Rising and Falling	Disabled
11	Rising and Falling	Enabled

1:0 **Video Port Configuration [1:0]:** This 2-bit field specifies the configuration of the video port as indicated in the following table:

VPC[1:0]	Configuration	Handshake	Clock In	Clock Out
00	CL-GD5430–compatible	-	-	-
01	Video Overlay (CL-GD5520)	BLANK*	DCLK	DCLK
10	Reserved	-	-	-
11	Video Capture	(VACT)	DCLK	-

9.49 CR25: Part Status Register (Read-only)

I/O Port Address: 3?5

Index: 25

Bit	Description	Reset State
7	PSR [7]	0
6	PSR [6]	1
5	PSR [5]	
4	PSR [4]	
3	PSR [3]	
2	PSR [2]	
1	PSR [1]	
0	PSR [0]	

Caution: This read-only register is used for factory testing and internal tracking only. Application programs never need to read this register. This register description is included for completeness only.

Bit	Description
7:0	**Part Status Value [7:0]**

9.50 CR27: ID Register (Read-only)

I/O Port Address: 3?5

Index: 27

Bit	Description
7	Device ID [5]
6	Device ID [4]
5	Device ID [3]
4	Device ID [2]
3	Device ID [1]
2	Device ID [0]
1	Reserved
0	Reserved

This read-only register will return a value that identifies the chip. Applications programs have no requirement to read this register if a Cirrus Logic BIOS is available. Instead, they should use the Inquire VGA Type INT10 call. See Appendix E1.

Bit **Description**

7:2 **Device ID [5:0]:** This 6-bit field contains a unique identifier, as shown in the following table:

Product	CR27[7:2]
CL-GD5430	101000
CL-GD5434	101010
CL-GD5436	101011
CL-GD5440	101000

1:0 **Reserved**

9.51 CR28: Class ID Register (Read-only) (CL-GD5430 only)

I/O Port Address: 3?5

Index: 28

Bit	Description
7	Class ID [7]
6	Class ID [6]
5	Class ID [5]
4	Class ID [4]
3	Class ID [3]
2	Class ID [2]
1	Class ID [1]
0	Class ID [0]

This read-only register will return a value that identifies the specific class of CL-GD5430.

Bit	Description
7:0	**Class ID [7:0]:** This 8-bit field contains a CL-GD5430 Class identifier, as shown in the following table:

CR28[7:0]	CL-GD5430 Class
FFh	Standard CL-GD5430
03h	Video Windowing and DDC2 Support
01h	DDC2 Support

9.52 CR31: Video Window Horizontal Zoom Control (CL-GD5440 only)

I/O Port Address: 3?5

Index: 31

Bit	Description
7	Horizontal Zoom Control [7]
6	Horizontal Zoom Control [6]
5	Horizontal Zoom Control [5]
4	Horizontal Zoom Control [4]
3	Horizontal Zoom Control [3]
2	Horizontal Zoom Control [2]
1	Horizontal Zoom Control [1]
0	Horizontal Zoom Control [0]

This register controls the horizontal zooming of the accelerated video window.

Bit	Description
7:0	**Horizontal Zoom Control [7:0]:** This field controls the horizontal zooming of the video window. Continuous horizontal zooming from 1× to 4× is possible. The zoom factor is determined by following equation. $$HZoom = \frac{256}{HorZoomCont}$$ where values in the range 64 through 255 may be used for HorZoomCont. This provides continuous zooming from 4× (HorZoomCont = 64) to slightly more than 1× (HorZoomCont = 255). A value of 0 sets 1×. If a horizontal zoom of greater than 1× is chosen, some pixels will be generated by interpolation of source image pixels. This will make the actual width of the window on the screen greater than it would be if zooming was not enabled. That is, horizontal zooming is accomplished by making the window physically wider rather than by keeping the window width constant and displaying fewer source pixels.

9.53 CR32: Video Window Vertical Zoom Control (CL-GD5440 only)

I/O Port Address: 3?5

Index: 32

Bit	Description
7	Vertical Zoom Control [7]
6	Vertical Zoom Control [6]
5	Vertical Zoom Control [5]
4	Vertical Zoom Control [4]
3	Vertical Zoom Control [3]
2	Vertical Zoom Control [2]
1	Vertical Zoom Control [0]
0	Vertical Zoom Control [0]

This register controls the vertical zooming of the accelerated video window.

Bit	Description
7:0	**Vertical Zoom Control [7:0]:** This field controls the vertical zooming of the accelerated video window. Continuous vertical zooming from 1× to 4× is possible. The zoom factor is determined by the following equation.

$$VZoom = \frac{256}{VertZoomCont}$$

where values in the range 64 through 255 may be used for VertZoomCont.

This provides continuous zooming from 4× (VertZoomCont = 64) to slightly more than 1× (VertZoomCont = 255). A value of 0 sets 1×.

If a vertical zoom of greater than 1× is chosen, some scanlines will be generated by interpolation of source image scanlines (or by replication). Since the physical height of the window on the screen is fixed by the Vertical Start and Vertical End values, some scanlines at the bottom of the source image will not be displayed. That is, vertical zooming is accomplished by keeping the window height constant and displaying fewer source lines rather than by making the window physically higher. Vertical zooming and horizontal zooming are different in this respect.

Vertical zooming through interpolation requires twice the normal video bandwidth. This places restrictions on when zooming via interpolation can be used. In general, zooming via interpolation cannot be used if the screen resolution is greater than 640 × 480 at 256 colors and if the zoom factor is less than two. See Appendix B10 for further details.

9.54 CR33: Video Window Horizontal Region 1 Size (CL-GD5440 only)

I/O Port Address: 3?5

Index: 33

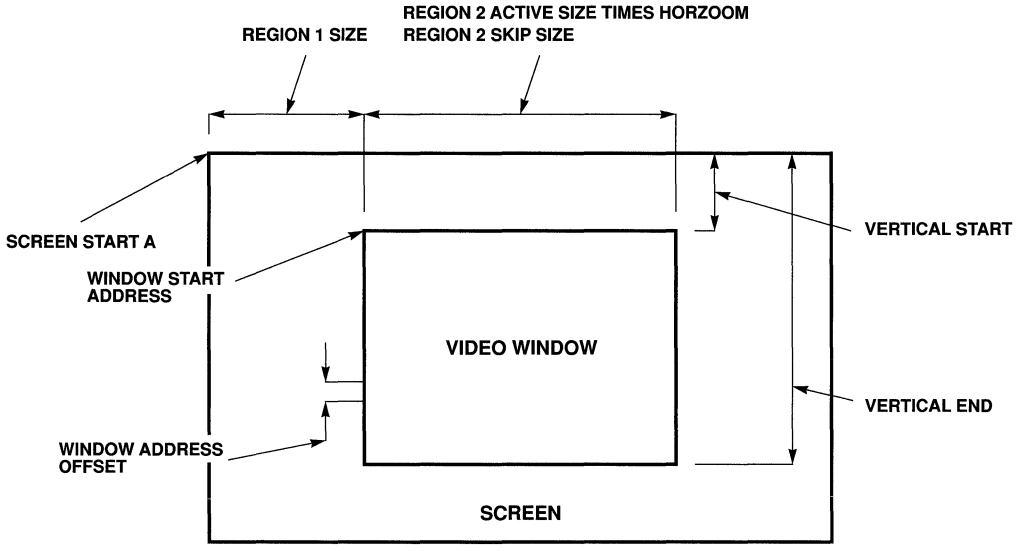
Bit	Description
7	HR1SZ [7]
6	HR1SZ [6]
5	HR1SZ [5]
4	HR1SZ [4]
3	HR1SZ [3]
2	HR1SZ [2]
1	HR1SZ [1]
0	HR1SZ [0]

This register contains the low-order bits of the Video Window Horizontal Region 1 Size.

Bit	Description
7:0	**HR1SZ [7:0]:** This field contains the low-order bits of the Video Window Horizontal Region 1 Size. This is extended to 10 bits in CR36[1:0]. The Horizontal Region 1 Size specifies the size of the background to the left of the video window. The units are DWORDs transferred to the CRT FIFO from the start of a scanline to the left boundary of the video window (that is, the last pixel before the window begins). The following equation can be used to determine the location of the first pixel of the video window. $$FirstPixel = \left(\frac{32}{32BitsPerPixel}\right) \bullet HR1SZ$$ Since the horizontal position and size of the video window are specified in terms of DWORDs into the FIFO rather than pixels on the scanline, it is not necessarily possible to position the window arbitrarily. For example, if the background were eight BPP, it would be possible to position the left edge of the window only at pixel locations that are even multiples of four (32/8). For detailed information regarding the video window, see Appendix B10. An overview is given in Section 9.55.

9.55 Video Window Definition: An Overview (CL-GD5440 only)

The following diagram indicates how the video window is positioned on the screen, and how the display memory is addressed for the background and the window.



The following table specifies the registers that control the video window and indicates how they relate to the above diagram.

Register	Address	Function
H Region 1 Size	CR33, 36	Screen size to the left of the video window
H Region 2 Skip Size	CR34, 36	Offset in display memory for the video window (distance in DWORDs across the window)
H Region 2 Active Size	CR35, 36	Size of the video window
Vertical Start	CR37, 39	First scanline of the video window
Vertical End	CR38, 39	Last scanline of the video window
Window Start Address	CR3A/B/C	Address of top left pixel in video window
Window Address Offset	CR3C/D	Distance in display memory between vertically adjacent pixel within video window

9.56 CR34: Video Window Region 2 Skip Size (CL-GD5440 only)

I/O Port Address: 3?5

Index: 34

Bit	Description
7	HR2SSZ [7]
6	HR2SSZ [6]
5	HR2SSZ [5]
4	HR2SSZ [4]
3	HR2SSZ [3]
2	HR2SSZ [2]
1	HR2SSZ [1]
0	HR2SSZ [0]

This register contains the low-order bits of the Video Window Horizontal Region 2 Skip Size.

Bit	Description
7:0	**HR2SSZ [7:0]:** This field contains the low-order bits of the Video Window Horizontal Region 2 Skip Size. This is extended to 10 bits in CR36[3:2]. The Horizontal Region 2 Skip Size is the size of the overlaid region in the background that is skipped for each scanline. The units are DWORDs that would have been transferred to the FIFO, but are not because the corresponding region on the screen displayed the window. This value may be calculated by evaluating the following equation. $$HR2SSZ = \left(\frac{BitsPerBackgroundPixel}{32}\right) \bullet WindowWidth$$ The second element of the equation is the number of screen pixels that are overlaid. The first element corrects for the number of pixels per DWORD.

9.57 CR35: Video Window Region 2 Active Size (CL-GD5440 only)

I/O Port Address: 3?5

Index: 35

Bit	Description
7	HR2ASZ [7]
6	HR2ASZ [6]
5	HR2ASZ [5]
4	HR2ASZ [4]
3	HR2ASZ [3]
2	HR2ASZ [2]
1	HR2ASZ [1]
0	HR2ASZ [0]

This register contains the low-order bits of the Video Window Horizontal Region 2 Active Size.

Bit **Description**

7:0 **HR2ASZ [7:0]:** This field contains the low-order bits of the video window Horizontal Region 2 Active Size. This is extended to 10 bits in CR36[5:4]. The Horizontal Region 2 Active Size specifies the width of the window. The units are DWORDs transferred to the CRT FIFO from the left to the right boundaries of the window. This value may be calculated by evaluating the following equation.

$$HR2ASZ = \left(\frac{BitsPerVideoPixel}{32}\right) \bullet \left(\frac{WindowWidth}{HorZoomFactor}\right)$$

WindowWidth is the number of actual physical pixels on the screen and will be modified by the horizontal zoom factor (if it is not unity). Also, the number of source pixels in each DWORD must be considered. The following table provides examples.

BPP	HR2ASZ	HorZoom	Window Width
16	160	2	640
8	106	1.5	636
16	128	4	1024

9.58 CR36: Video Window Horizontal Overflow (CL-GD5440 only)

I/O Port Address: 3?5

Index: 36

Bit	Description
7	Reserved
6	Reserved
5	HR2ASZ [9]
4	HR2ASZ [8]
3	HR2SSZ [9]
2	HR2SSZ [8]
1	HR1SZ [9]
0	HR1SZ [8]

This register contains bits that extend each of three horizontal fields to 10 bits.

Bit	Description
7:6	**Reserved**
5:4	**HR2ASZ [9:8]:** These two bits extend the Horizontal Region 2 Active Size to 10 bits. The low-order eight bits are contained in CR35.
3:2	**HR2SSZ [9:8]:** These two bits extend the Horizontal Region 2 Skip Size to 10 bits. The low-order eight bits are contained in CR34.
1:0	**HR1SZ [9:8]:** These two bits extend the Horizontal Region 1 Size to 10 bits. The low-order eight bits are contained in CR33.

9.59 CR37: Video Window Vertical Start (CL-GD5440 only)

I/O Port Address: 3?5

Index: 37

Bit	Description
7	VWVS [7]
6	VWVS [6]
5	VWVS [5]
4	VWVS [4]
3	VWVS [3]
2	VWVS [2]
1	VWVS [1]
0	VWVS [0]

This register contains the low-order bits of the Video Window Vertical Start.

Bit	Description
7:0	**VWVS [7:0]:** This field contains the low-order eight bits of the Video Window Vertical Start value. This is extended to 10 bits in CR39[1:0]. The Video Window Vertical Start specifies the first scanline that will contain the window. Together with the Video Window Vertical End value, this defines the vertical extent of the window.

9.60 CR38: Video Window Vertical End (CL-GD5440 only)

I/O Port Address: 3?5

Index: 38

Bit	Description
7	VWVE [7]
6	VWVE [7]
5	VWVE [7]
4	VWVE [7]
3	VWVE [7]
2	VWVE [7]
1	VWVE [7]
0	VWVE [7]

This register contains the low-order bits of the Video Window Vertical End.

Bit	Description
7:0	**VWVS [7:0]:** This field contains the low-order eight bits of the Video Window Vertical End value. This is extended to 10 bits in CR39[3:2]. The Video Window Vertical End specifies the last scanline that will contain the window. Together with the Video Window Vertical Start value, this defines the vertical extent of the window.

9.61 CR39: Video Window Vertical Overflow (CL-GD5440 only)

I/O Port Address: 3?5

Index: 39

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	VWVE [9]
2	VWVE [8]
1	VWVS [9]
0	VWVS [8]

This register contains bits that extend each of two vertical fields to 10 bits.

Bit	Description
7:4	**Reserved**
3:2	**VWVE [9:8]:** These two bits extend the Video Window Vertical End to 10 bits. The low-order eight bits are contained in CR38.
1:0	**VWVS [9:8]:** These two bits extend the Video Window Vertical Start to 10 bits. The low-order eight bits are contained in CR37.

9.62 CR3A, 3B: Video Window Start Address Byte 0, 1 (CL-GD5440 only)

I/O Port Address: 3?5

Index: 3A, 3B

Bit	Description
7	Video Start Address [7] / [15]
6	Video Start Address [6] / [14]
5	Video Start Address [5] / [13]
4	Video Start Address [4] / [12]
3	Video Start Address [3] / [11]
2	Video Start Address [2] / [10]
1	Video Start Address [1] / [9]
0	Video Start Address [0] / [8]

These two registers contain the low-order bits of the Video Window Start Address.

Bit	Description
15:0	**Video Start Address [15:0]:** This field contains the low-order 16 bits of the Video Window Start Address. This is extended to 19 bits in CR3C. The Video Window Start Address specifies the address in display memory of the first byte of the top left pixel of the rectangular video window.

9.63 CR3C: Video Window Start Address Byte 2 (CL-GD5440 only)

I/O Port Address: 3?5

Index: 3C

Bit	Description
7	Reserved
6	Reserved
5	Video Address Offset [9]
4	Video FIFO Threshold
3	Reserved
2	Video Start Address [18]
1	Video Start Address [17]
0	Video Start Address [16]

This register contains the high-order three bits of the Video Window Start Address field and an upper bit of the video address offset.

Bit	Description
7:6	**Reserved**
5	**Video Address Offset [9]:** These bits extend the Video Address Offset to 10 bits. The low-order bits are contained in CR3D.
4	**Video FIFO Threshold:** When video capture is enabled by setting CR1E[1:0] to '11', this bit controls the threshold for the video FIFO. If this bit is set to '1', the FIFO threshold is set to a smaller value. If this bit is set to '0', the FIFO threshold is set to the default value.
3	**Reserved**
1:0	**Video Start Address [18:16]:** These three bits extend the Video Window Start Address to 19 bits. The low-order bits are contained in CR3A and CR3B.

9.64 CR3D: Video Window Address Offset (CL-GD5440 only)

I/O Port Address: 3?5

Index: 3D

Bit	Description
7	Video Address Offset [8]
6	Video Address Offset [7]
5	Video Address Offset [6]
4	Video Address Offset [5]
3	Video Address Offset [4]
2	Video Address Offset [3]
1	Video Address Offset [2]
0	Video Address Offset [1]

This register contains the low-order bits of the Video Window Address Offset.

Bit	Description
7:0	**Video Address Offset [8:1]:** This field contains the low-order bits of the Video Address Offset. The low-order bit is always taken to be zero. This is extended to 10 bits in CR3C[5]. This 10-bit value specifies the distance in display memory between vertically adjacent pixels. This value is added to the video window address at the end of each scanline within the window to obtain the beginning address of the next scanline.

9.65 CR3E: Video Window Master Control (CL-GD5440 only)

I/O Port Address: 3?5

Index: 3E

Bit	Description
7	Occlusion Enable
6	Video Window Blank Enable
5	Error Diffusion Enable
4	Vertical Zoom Mode
3	Video Format [2]
2	Video Format [1]
1	Video Format [0]
0	Video Window Master Enable

This register configures the video window for the various modes of operation.

Bit	Description
7	**Occlusion Enable:** If this bit is set to '1', overlay can take place on a pixel-by-pixel basis, rather than on the basis of what is in or out of the video window. If this bit is set to '0', the overlay will be within the video window.
6	**Video Window Blank Enable:** If this bit is set to '1', the video window will be forced to black. This minimizes artifacts when switching to software-only video playback. If this bit is set to '0', the video window will not be forced to black.
5	**Error Diffusion Enable:** If this bit is set to '1', error diffusion is enabled for AccuPak™ to YCrCb 442 conversion. This will reduce contouring resulting from the truncated luminance value by inserting random values in place of the missing LSBs. If this bit is set to '0', error diffusion is not enabled.
4	**Vertical Zoom Mode:** If this bit is set to '1', line replication is used for vertical zooming. If this bit is set to '0', interpolation is used for vertical zooming.

9.65 CR3E: Video Window Master Control (CL-GD5440 only) *(cont.)*

3:1 **Video Format [2:0]:** This 3-bit field specifies the format of the video displayed in the video window. The following table shows the encoding.

CR3E[3:1]	Format	Note
000	YCrCb 4:2:2	Excess 128 Cr, Cb
001	AccuPak™	Encoded from YCrCb, Excess 128 Cr, Cb
010	Reserved	
011	RGB AccuPak™	Encoded from RGB
100	RGB 5-5-5	
101	RGB 5-6-5	
110	YCrCb 4:2:2	2's complement Cr, Cb
111	AccuPak™	2's complement Cr, Cb

0 **Video Window Master Enable:** If this bit is set to '1', the video window is enabled and will be displayed as configured. If this bit is set to '0', the video window is not enabled. When this bit is set to '1', the video window is enabled at the next leading edge of VSYNC. This avoids the requirement for the software to synchronize with VSYNC. When this bit is set to '0', the video window is disabled immediately.

9.66 CR3F: Host Video Data Path Control (CL-GD5440 only)

I/O Port Address: 3?5

Index: 3F

Bit	Description
7	Video Port VSYNC
6	Field ID/ Polarity Control
5	Reserved
4	AccuPak Encode Control [1]
3	AccuPak Encode Control [0]
2	ExceptErrStat
1	ExceptStartCheck
0	VPageBit

This register is used to control AccuPak encoding.

Bit **Description**

7 **Video Port VSYNC (R/O):** This read only bit follows the Video Port VSYNC signal (EDCLK*).

6 **Field ID/Polarity Control:** When this bit is read, it specifies the current field (odd/even). When this bit is set to '1', it inverts the polarity of the video field

5 **Reserved**

4:3 **AccuPak™ Encode Control [1:0]:** This 2-bit field is used to enable AccuPak encoding and specify the source format. The following table shows the field values.

AccuPak™ EC [1:0]	Enable Encode	Source Format
0x	No	–
10	Yes	YCC 422
11	Yes	RGB 555

See Appendix B10 for detailed information regarding AccuPak encoding.

2 **ExceptErrStat:** If this read-only bit is '1', the AccuPak addressing protocol has been violated. Programming the ExceptStartCheck bit (CR3F[0]) to '0' will clear this bit. If this read-only bit is '0', no AccuPak addressing protocol errors have occurred since CR3F[1] was last set to '0' and then set to '1'.

1 **ExceptStartCheck:** If this bit is set to '1', AccuPak addressing protocol checking will be enabled. If this bit is set to '0', AccuPak addressing protocol checking will be disabled; CR3F[2] will be forced to '0'.

0 **VPageBit:** If this bit is set to '0', the expanded video address is less than 2 Mbytes. If this bit is set to '1', the expanded video address is equal to or greater than 2 Mbytes.

9.67 HDR: Hidden DAC Register

I/O Port Address: 3C6

Index: –

Bit	Description	Reset State
7	Enable 5-5-5 Mode	0
6	Enable All Extended Modes	0
5	Clocking Mode	0
4	32K Color Control	0
3	Extended Mode Select [3]	0
2	Extended Mode Select [2]	0
1	Extended Mode Select [1]	0
0	Extended Mode Select [0]	0

This register selects the Extended Color modes, including 15-, 16-, and 24-bit-per-pixel modes. This register is cleared to all zeroes at reset, putting the CL-GD543X/'4X in VGA-Compatibility mode.

This register is accessed by reading the Pixel Mask register at 03C6h four times in succession; the next write or read at 03C6h will access the Hidden DAC register. Subsequent accesses require the four accesses to the Pixel Mask register.

Bit	Description
7	**Enable 5-5-5 Mode:** If this bit is set to '0', the Extended Color modes are disabled and the palette DAC is VGA-compatible. If this bit is set to '1', Extended Color modes are enabled, as chosen by bit 6 and bits 3:0 of this register.
6	**Enable All Extended Modes:** If this bit is set to '0' and bit 7 is set to '1', the palette DAC will be in 5-5-5 Sierra™ mode, regardless of the value set to bits 3:0. If this bit is set to '1' and bit 7 is set to '1', the Palette DAC mode will be chosen by the value set into bits 2:0 of this register.

9.67 HDR: Hidden DAC Register *(cont.)*

Bit	Description
5	**Clocking Mode (CL-GD5434):** If this bit is set to '0', Clocking mode 1 will be chosen. In Clocking mode 1, 16-bit-per-pixel modes will use both edges of DCLK to latch data. The rising edge of DCLK will latch the least-significant byte and the falling edge of DCLK will latch the most-significant byte. If this bit is set to '1', Clocking mode 2 will be chosen. In Clocking mode 2, 16-bit-per-pixel modes will use only the rising edge of DCLK to latch data. The DCLK must be supplied at twice the pixel rate. The least-significant byte is latched on the first rising edge and the most-significant byte is latched on the second rising edge. **Clocking Mode (CL-GD5430/'40):** If this bit is set to '0', both edges of DCLK will be used. The rising edge of DCLK will latch the low byte and the falling edge of DCLK will latch the high byte. If this bit is set to '1', the CL-GD5430 is configured for VESA® VAFC 2× mode. Each rising edge will clock in one byte. Every two bytes will be assembled into a single 16-bit pixel, which is displayed twice (two clock periods).
4	**32K Color Control:** If this bit is set to '0', 5-5-5 operation will occur normally. If this bit is set to '1', Pixel Data bit 15 will be used to choose between palette operation and 5-5-5 color. This allows 5-5-5 data to overlay 256-color images on a pixel-by-pixel basis. If Pixel Data bit 15 is '1', then bits 7:0 choose a palette entry and bits 14:8 are ignored. If pixel bit 15 is '0', then 5-5-5 operation is chosen.

9.67 HDR: Hidden DAC Register *(cont.)*

Bit **Description**

3:0 **Extended Mode Select [3:0]:** If bits 7 and 6 are both set to '1', then this 4-bit field selects the Extended Color mode according to the following table:

Bit 7	Bit 6	Bit 3	Bit 2	Bit 1	Bit 0	Function
0	x	x	x	x	x	VGA compatibility (Palette mode)
0	1	1	0	1	0	Palette mode > 85 MHz[a] CL-GD5434/'36 only
1	0	x	x	x	x	5-5-5 Sierra™
1	1	0	0	0	0	5-5-5 Sierra™[b]
1	1	0	0	0	1	5-6-5 XGA™
1	1	0	0	1	x	Reserved
1	1	0	1	0	0	Reserved
1	1	0	1	0	1	8-8-8 16M color (24- or 32-bit) (32-bit for CL-GD5434)
1	1	0	1	1	x	Power-down DAC[c]
1	1	1	0	0	0	8-bit grayscale
1	1	1	0	0	1	3-3-2 8-bit RGB
1	1	1	0	1	x	Reserved
1	1	1	1	x	x	Reserved

a. This mode is used for 8-bit-per-pixel modes where VCLK is > 85 MHz. The CRTC is clocked at one-half the programmed VCLK rate. SR7[3:0] must be set to '0111' (16-bit-per-pixel and high-resolution). The 16-bit data is sent through the LUT one byte at a time at the VCLK rate. This applies to the CL-GD5434/'36 only. This is for 8-bits-per-pixel modes only.

b. HDR[5] is used to choose the clocking mode for the 15- and 16-bit modes.

c. The result of programming this pattern is identical to the side effect of programming GRE[1] to '1': IREF is turned off, which greatly reduces the power consumed in the DACs; VCLK to the palette is gated off, putting it into low-power static operation.

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VGA BIOS

10. VGA BIOS

10.1 BIOS Overview

The CL-GD543X/'4X VGA BIOS is a high-performance firmware product optimized to take full advantage of the CL-GD543X/'4X VGA controller. The CL-GD543X/'4X BIOS is based on proven BIOS technology, and is fully compatible with the IBM VGA BIOS Interrupt 10H interface. The BIOS is designed to provide a well-defined interface between MS-DOS, application software, and special OEM utility programs. In addition, it provides an extended set of functions to support the CL-GD543X/'4X VGA controller. This document covers the standard VGA BIOS functions. The extended BIOS functions are covered in Appendix E1.

10.1.1 Main BIOS Features

The CL-GD543X/'4X VGA BIOS supports the following key features:

- Fully IBM VGA-compatible BIOS
- Support for high-resolution, extended 256-colors, Direct-Color™ and 16.8 million color True-color Video Modes
- High-performance operation
- Modular, proven design
- Adapter or system board implementation (C000/E000 segments)
- Can be integrated with system BIOS
- Supports switchless configuration
- Can be customized without source code
- VESA-compatible modes and interface

10.1.2 Extended Video Mode Support

The CL-GD543X/'4X VGA BIOS provides full support for all extended high-resolution video modes via interrupt 10H function calls. In addition, the CL-GD543X/'4X VGA BIOS supports a variety of extended functions, such as VGA display configuration and extended VGA inquiry. For a detailed description of these functions, refer to Appendix E1, VGA BIOS External Function Specification.

10.1.3 Direct-Color Operation

The CL-GD543X/'4X BIOS supports Direct-color and True-color Video Modes. These modes allow CL-GD543X/'4X to display 32K, 64K, or 16.8 million colors at resolutions of up to 1024 x 768.

10.1.4 High Performance

The BIOS is optimized to provide maximum performance in adapter or motherboard implementations. The CL-GD543X/'4X Local Bus, Display Memory Interface, Memory Clock, and Dot Clock Configurations are configurable using the VGA BIOS.

In addition, time-critical routines, such as TTY output and scroll, are designed to provide maximum throughput in both text and graphics modes.

10.1.5 System Integration

The CL-GD543X/'4X VGA BIOS can easily be integrated for an adapter or motherboard design. The BIOS, 32K bytes in size, is provided for both the C000 and E000 address segments. To save space on the system board, the CL-GD543X/'4X VGA BIOS can be incorporated into the system BIOS ROM at either C000 or E000 addresses.

The BIOS does not require DIP switches or external hardware for configuration. A well-defined interface to the CL-GD543X/'4X BIOS configuration is available for system BIOS or OEM set-up routines.

10.1.6 Customization

The default CL-GD543X/'4X BIOS is designed to be implemented without modification in almost all environments. However, the CL-GD543X/'4X BIOS can also be easily customized for a specific system environment. Modifications can also be accomplished with the Cirrus Logic OEM System Integration (OEMSI) utility program; such modifications do not require the CL-GD543X/'4X VGA BIOS source code. Hundreds of BIOS parameters and features can be modified, including:

- Sign-on message
- Display type configuration
- Video Mode parameter tables
- Font tables

10.1.7 Compatibility

The CL-GD543X/'4X BIOS is 100-percent compatible with the IBM VGA BIOS and supports BIOS-level compatibility for adapter card or integrated VGA on the system board. In addition, the CL-GD543X/'4X BIOS complies fully with the video modes and specifications issued by the Video Electronics Standards Association (VESA).

10.2 CL-GD543X/'4X VGA BIOS Initialization and Power-Up Diagnostics

The CL-GD543X/'4X VGA BIOS is shipped in two format: a segment-C000-based VGA BIOS configured for VGA adapter cards that will be plugged into PC systems, and segment-E000-based VGA BIOS configured for integrated VGA video subsystems on the motherboard. The following sequence of steps is performed by the VGA BIOS at power-up initialization:

For Segment-C000-Adapter-Based VGA BIOS:

1. Checks if VGA BIOS Vector Interrupt 10H is already initialized.
2. If so, calls the INT 10H function to disable the existing VGA card by putting it to sleep.
3. Disables the VGA adapter by writing a value of 10H to I/O Port 46E8H.
4. Programs I/O Port 102H with data 01H to enable video subsystem.
5. Writes a value of 08H to 46E8H to enable I/O and memory addressing.
6. Writes I/O Port 4AE8H to disable 8514/A.
7. Disables VGA video (by programming Sequencer Clocking Mode register, SR1[Bit 5] = 1).
8. Initializes Video Vectors INT 10H and INT 42H.

9. Enables extensions by writing SR06 (I/O Port 3C4, Index = 06) with data 012H.
10. Initializes CL-GD543X/'4X Extension registers.
11. Checks for co-resident MDA video adapter; if MDA is present, initializes co-resident bits and sets up MDA adapter.
12. Checks for CGA; if present, initializes co-resident bits, sets VGA to monochrome, and enables CGA.
13. Tests Video memory.
14. Initializes Text mode 3.
15. Displays sign-on message.
16. If any POST error flags are set, prints error messages.

For Segment-E000-Motherboard-Based VGA BIOS:

1. Enables VGA Setup mode by writing VGA Video Sleep Enable register (VSE I/O Port 46E8H with value of 10H).
2. Programs POS 2 register (I/O Port 102H with data 01H) to enable video subsystem.
3. Enables motherboard VGA by programming VSE register 46E8 with data value 1.
4. Writes I/O Port 4AE8H to disable 8514/A.
5. Disables VGA video (by programming Sequencer Clocking Mode register, SR1[bit 5] = 1).
6. Initializes Video Vectors INT 10H and INT 42H.
7. Enables extensions by writing SR06 (I/O Port 3C4, Index = 06H) with data 012H.
8. Initializes CL-GD543X/'4X Extension registers.
9. Checks for co-resident MDA video adapter; if MDA is present, initializes co-resident bits and sets up MDA adapter.
10. Checks for CGA; if present, initializes co-resident bits, and sets VGA to monochrome and enables CGA.
11. Tests Video memory.
12. Initializes Text mode 3.
13. Displays sign-on message.
14. If any POST error flags are set, prints error messages.
15. Checks to see if a VGA adapter is also present in the system; if so, disables motherboard VGA controller.

10.3 Video BIOS Interrupt Vectors

The interrupt vectors that must be initialized by DOS (including the planar and video BIOSes) are listed in Table 10-4 later in this chapter. Of these, the vectors (at locations 0:0040, 0000:007C, 0000:0108, 0000:010C) corresponding to vectors 10, 1F, 42, 43 are handled by the video BIOS.

10H — Video Services (Vector Location = 0000:0040H)

The CL-GD543X/'4X BIOS functions are accessed using interrupt 10H. Application programs place a function code in AH, and if required, in other registers calling parameters, then executes an INT 10H instruction. When the BIOS gains control, the appropriate code is executed to perform the function; parameter values may be left in processor registers to be returned to the calling program upon exit from the interrupt routine.

The functions supported by the CL-GD543X/'4X BIOS allow the calling program to: set the current mode, manipulate the cursor, place characters and individual pixels on the display, scroll the screen, load character fonts and color palette values, and read the light-pen position. These functions are described in following sections.

1DH — 6845 Initialization (Vector Location = 0000:0074H)

This vector points to the initialization routines that set up the 6845.

1FH — CGA Character Set (Vector Location = 0000:007CH)

This pointer is used for the table of the upper 128 characters in CGA modes 4, 5, and 6. The INT 43H Vector is used for the lower 128 characters for these modes.

42H — Old Video Services Pointer (Vector Location = 0000:0108H)

This location used to be the INT 10H vector for planar BIOS video services. When the EGA/VGA is installed, BIOS routines reload this address with a pointer to the planar INT 10H video service routine entry point.

43H — Graphics Character Table (Vector Location = 0000:010CH)

BIOS routines use this vector to point to a table of bitmaps that are used when graphics characters are displayed. This table is used for the lower 128 characters in Video modes 4, 5, and 6. This table is also used for 256 characters in all additional graphics modes (both IBM standard and Cirrus Logic extensions).

The Interrupt 10H calls constitute the bulk of the services provided by the video BIOS and will be described later in detail. They are listed along with the function and subfunction that define the particular service required. Note that some INT 10H services were introduced with the VGA and are not available on the earlier EGA. The services have been divided up into functional groupings.

10.3.1 Interrupt 10H: BIOS Video Service Routines Contents

Function	Sub-Function	Description	Adapter
00H		Set Video Mode	EGA,VGA
01H		Set Cursor Type	EGA,VGA
02H		Set Cursor Position	EGA,VGA
03H		Get Cursor Position	EGA,VGA
04H		Get Light Pen Position	EGA,VGA
05H		Select Active Display Page	EGA,VGA
06H		Window Scroll-Up	EGA,VGA
07H		Window Scroll-Down	EGA,VGA
08H		Read Character/Attribute at Cursor Position	EGA,VGA
09H		Write Character/Attribute at Cursor Position	EGA,VGA
0AH		Write Character at Cursor Position	EGA,VGA
0BH	00H	Set Background/Border Color	EGA,VGA
	01H	Select the Palette Set	EGA,VGA
0CH		Write Dot (Pixel)	EGA,VGA
0DH		Read Dot (Pixel)	EGA,VGA
0EH		Write Teletype Character to Active Page	EGA,VGA
0FH		Get Video Mode	EGA,VGA
10H		Palette Manipulations	EGA,VGA
	00H	Set Individual Palette Register (Internal Palette Register)	
	01H	Set OverScan (Border) Register	
	02H	Set All Palette Registers and OverScan Register	
	03H	Intensity/Blinking	
	04H-06H	Reserved	
	07H	Read Individual Palette Register (Internal Palette Register)	
	08H	Read OverScan (Border) Register	
	09H	Read All Palette Registers and OverScan Register	
	0AH-0FH	Reserved	
	10H	Set Individual Color Register (RAMDAC/External Palette Register)	
	11H	Reserved	
	12H	Set Block of Color Registers	
	13H	Select Color Page (Not Valid in Mode 13H)	
	14H	Reserved	
	15H	Read Individual Color Register (RAMDAC/External Palette Register)	
	16H	Reserved	
	17H	Read Block of Color Registers	
	18H-19H	Reserved	

10.3.1 Interrupt 10H: BIOS Video Service Routines Contents *(cont.)*

Function	Sub-Function	Description	Adapter
	1AH	Read Current State of Color Page	
	1BH	Sum Color Values To Gray Shades	
11H		CHARACTER GENERATOR	EGA,VGA
	00H	Load User Text Font	
	01H	Load 8 x 14 ROM Text Font	
	02H	Load 8 x 8 ROM Text Font	
	03H	Select Block Specifier	
	04H	Load 8 x 16 ROM Text Font	VGA
	10H	Load User Text Font and Reprogram Controller	
	11H	Load 8 x 14 ROM Text Font and Reprogram Controller	
	12H	Load 8 x 8 ROM Text Font and Reprogram Controller	
	14H	Load 8 x 16 ROM Text Font and Reprogram Controller	VGA
	20H	Set Pointer of User's Graphics Font Table to Interrupt 1FH	
	21H	Set Pointer of User's Graphics Font Table to Interrupt 43H	
	22H	Set Pointer of 8 x 14 ROM Graphics Font Table to Interrupt 43H	
	23H	Set Pointer of 8 x 8 ROM Graphics Font Table to Interrupt 43H	
	24H	Set Pointer of 8 x 16 ROM Graphics Font Table to Interrupt 43H	VGA
	30H	Get Font Information	
12H		Alternate Select	EGA,VGA
	10H	Get Configuration Information	
	20H	Select Alternate PrintScreen Routine	
	30H	Select Scanlines (Alphanumeric Mode)	
	31H	Enable/Disable Default Palette Loading	
	32H	Enable/Disable Video	
	33H	Enable/Disable Grayscale Summing	
	34H	Enable/Disable Cursor Emulation	
	35H	Switch Active Display	
	36H	Enable/Disable Screen Refresh	
	13H	Write String in Teletype	EGA,VGA
	1AH	Get/Set Display Combination Code	VGA
1BH		Get Functionality/State Information	VGA
1CH		Save/Restore Video State	VGA
	1DH - FFH	Reserved	

10.4 Description Of Functions

10.4.1 Function: 00H • Set Video Mode

[Entry]

AH = 00H
AL = Video Mode (see below)

[Return]

NONE

[Note]

1. Video Mode Table for standard VGA:

Mode	Resolution	Type	Colors	Pages
00H/01H	40 x 25 (360 x 400)	Text	16	8
02H/03H	80 x 25 (640 x 400)	Text	16	8
04H/05H	320 x 200 (40 x 25)	Graphics	4	1
06H	640 x 200) (80 x 25)	Graphics	2	1
07H	80 x 25 (720 x 400)	Text	Monochrome	8
08H - 0CH	Reserved			
0DH	320 x 200 (40 x 25)	Graphics	16	8
0EH	640 x 200 (80 x 25)	Graphics	16	4
0FH	640 x 350 (80 x 25)	Graphics	Monochrome	2
10H	640 x 350 (80 x 25)	Graphics	16	2
11H	640 x 480 (80 x 25)	Graphics	2	1
12H	640 x 480 (80 x 25)	Graphics	16	1
13H	320 x 200 (40 x 25)	Graphics	256	1

2. If bit 7 of AL is set, the display buffer will not be cleared. Otherwise, the display buffer will be cleared during mode setting (EGA, VGA only) (Clear Screen).
3. No hardware cursor in graphics modes.
4. Default mode during POST: mode 3H = Color Monitor, mode 07H = Monochrome Monitor.
5. There is no difference between Modes 00H and 01H, 02H and 03H, or 05H and 06H on EGA/VGA. They are only different on CGA, which supports composite video displays.
6. The default settings of each video mode can be overridden by several subfunctions in Function 12H or by supply user's video service table whose address is stored in BIOS data area 0040:A8H.
7. See Appendix E1, "VGA BIOS Extended Function Specifications", for extended modes.

10.4.2 Function: 01H • Set Cursor Type

[Entry]

AH = 01H
CH = Start scanline of cursor (0 base)
CL = End scanline of cursor (0 base)

[Return]

NONE

[Notes]

1. This function is available in text modes only. The values of cursor type are stored at [40:60].
2. The definition of value in register CH:

Bit	Definition
7:6	Reserved = 0
5	1 = No cursor display 0 = Normal blinking cursor
4:0	Start scanline (0 base)

3. The definition of value in register CL:

Bit	Definition
7	Reserved = 0
6:5	Number of character skew
4:0	End scanline (0 base)

4. Default setting:

Font Size	Start	End
8 x 8	6	7
8 x 14	11	12
8 x 16	13	14

5. To allow cursor displaying as the values set in the function call, turn off cursor emulation. The Cursor Emulation Flag is located in bit 0 of [40:87]. It can be turned on/off by Subfunction 34H of Function 12H call.

10.4.3 Function: 02H • Set Cursor Position

[Entry]

AH = 02H
BH = Display page (0 base)
DH = Row number of cursor location start (0 base)
DL = Column number of cursor location end (0 base)

[Return]

NONE

[Notes]

1. This function is available for both text and graphics modes.
2. If register DL is specified over the width of screen displayable area, it will cause the cursor to wrap to the next row. If register DH is specified over the height of screen displayable area, it causes the cursor to disappear.
3. Default setting for each mode: Cursor Location at 0000H.
4. BIOS maintains one cursor location for each page and supports up to eight pages. These values are recorded at [40:50], and occupy eight words (one word for each location).

10.4.4 Function: 03H • Get Cursor Position

[Entry]

AH = 03H
BH = Display page (0 base)

[Return]

CH = Start scanline of cursor (0 base)
CL = End scanline of cursor (0 base)
DH = Row number of cursor start location (0 base)
DL = Column number of cursor end location (0 base)

[Note]

1. Cursor type is same for all pages. The cursor location of each page is maintained separately.

10.4.5 Function: 04H • Get Light Pen Position*

[Entry]

AH = 04H

[Return]

AH = 00H	Light Pen inactive
or	
AH = 01H	Light Pen active and returns following values
BX = Pixel column	(X coordinate in graphics modes (0 base))
CX = Pixel row	(Y coordinate in graphics modes above Mode 06H (0 base))
CH = Pixel row	(Y coordinate in Graphics Modes 04H - 06H (0 base))
DH = Character row	(Y coordinate in text modes (0 base))
DL = Character column	(X coordinate in text modes (0 base))

[Notes]

1. The color of background and foreground will affect the sensitivity of light pen.
2. High-resolution device affects the accuracy of light pen.

* ***No longer supported***

10.4.6 Function: 05H • Select Active Display Page

[Entry]

AH = 05H
AL = Display page (0 base)

[Return]

None

[Notes]

1. The contents of each page will not be altered by changing to other pages.
2. Please refer to the video mode table of Function 00H.

10.4.7 Function: 06H • Window Scroll Up

[Entry]

AH = 06H
AL = Number of rows to be scrolled up (0 = scroll up and clear entire window)
BH = Attribute to be used in inserting blank lines
CH = Y coordinate of top left corner of window (0 base)
CL = X coordinate of top left corner of window (0 base)
DH = Y coordinate of bottom right corner of window (0 base)
DL = X coordinate of bottom right corner of window (0 base)

[Return]

None

[Notes]

1. This function will clear the entire window when it encounters the number of rows of window equal to the value in register AL or AL = 0.
2. The image outside the window will not be changed. The cursor will not be updated.
3. A new blank line, with attribute value specified in BH, is inserted from the bottom of window whenever an old line at the top of window is scrolled out of window.
4. This function is available for both Text and Graphics modes.

10.4.8 Function: 07H • Window Scroll Down

[Entry]

AH = 07H
AL = Number of rows to be scrolled down (0 = scroll down and clear entire window)
BH = Attribute to be used in inserting blank lines
CH = Y coordinate of top left corner of window (0 base)
CL = X coordinate of top left corner of window (0 base)
DH = Y coordinate of bottom right corner of window (0 base)
DL = X coordinate of bottom right corner of window (0 base)

[Return]

None

[Notes]

1. This function will clear entire window when it encounters the number of rows of window equal to the value in register AL or AL = 0.
2. The image outside the window will not be changed. The cursor will not be updated.
3. A new blank line, with attribute value specified in BH, is inserted from the top of window whenever an old line at the bottom of window is scrolled out of window.
4. This function is available for both Text and Graphics modes.

10.4.9 Function: 08H • Read Character/Attribute at Cursor Position

[Entry]

AH = 08H
BH = Display page (0 base)

[Return]

AH = Attribute (Valid on text modes)
AL = ASCII character code

[Notes]

1. This function is able to read data from other valid inactive pages in multiple page modes at any time.
2. The cursor is not updated after reading a character from the screen, and has to be moved explicitly.
3. No control characters such as, LF, CR, BACKSPACE, and BELL, are recognized.
4. In Graphics modes 04H–06H of CGA adapter, the first half of character font (Code 00H–7FH) is maintained in system ROM only. To support the second half of character font (Code 80H–FFH), the Interrupt Vector 1FH at 0000:007CH, has to be initialized to point to the second half of character font.
5. Graphics modes return the Character Code only. Three characters, 00H/20H/FFH, cannot be distinguished, and the function always reads them back as Character Code 00H.
6. The character codes will be read back as Character Code 00H when they are written with a color that is same as the background color in graphics modes.

10.4.10 Function: 09H • Write Character/Attribute at Cursor Position

[Entry]

AH = 09H
AL = ASCII character code
BH = Display page (0 base)

or

BL = Attribute (text modes)
Display color (graphics modes)
CX = Repeat character count

[Return]

None

[Notes]

1. This function is able to write data to other valid inactive pages in multiple page modes at any time.
2. The cursor is not updated after writing a character to the screen, and has to be moved explicitly.
3. No control characters such as, LF, CR, BACKSPACE, and BELL, are recognized.
4. Graphics modes 04H–06H of CGA adapter, the first half of character font (Code 00H–7FH) is maintained in system ROM only. To support the second half of character font (Code 80H–FFH), the Interrupt Vector 1FH at 0000:007CH, has to be initialized to point to the second half of character font.

5. In Graphics modes, the color (attribute) is treated as pixel color to generate an ASCII character pattern. The color value will be masked according to the number of colors in the video modes.
6. The character codes will be displayed as blank when they are written with the color that is the same as the background color in graphics modes.
7. The characters written to the screen, specified in CX, should not extend to the next row in graphics modes or invalid results will be generated.
8. If bit 7 of register BL is set, the function will take the color value X'OR'ed with the value in display memory. (Valid in all graphics modes except mode 13H). This feature can be used in fast character/dot erasing.

10.4.11 Function: 0AH • Write Character at Cursor Position

[Entry]

AH = 0AH
AL = ASCII character code
BH = Display page (0 base)

or

BL = Foreground color (graphics modes only)
CX = Repeat character count

[Return]

None

[Notes]

1. This function is able to write data to other valid inactive pages in multiple page modes at any time.
2. The cursor is not updated after writing a character to screen and has to be moved explicitly.
3. No control characters such as, LF, CR, BACKSPACE, and BELL, are recognized.
4. Graphics modes 04H–06H of CGA adapter, the first half of character font (Code 00H–7FH) is maintained in system ROM only. To support the second half of character font (Code 80H–FFH), the Interrupt Vector 1FH at 0000:007CH, has to be initialized to point to the second font.
5. In graphics modes, the color (attribute) is treated as pixel color to generate AN ASCII character pattern. The color value will be masked according to the number of colors in the video modes.
6. The character codes will be displayed as blank when they are written with the color same as background color in graphics modes.
7. The characters written to screen, specified in CX, should not extend to next row in graphics modes or invalid results will be generated.
8. If bit 7 of register BL is set, the function will take the color value X'OR'ed with the value in display memory (valid in all graphics modes except mode 13H). This feature can be used in fast character/dot erasing.

10.4.12 Function: 0BH

Function: 0BH • Subfunction: 00H — Set Background/Border Color

[Entry]

AH = 0BH
BH = 00H
BL = Color Value (0 - 31: Low-Intensity Colors = 0 - 15, High-Intensity Colors = 16 - 31)
– Border Color for text modes (modes 00H–03H)
– Color for 640 x 200 Graphics mode (mode 06H)

[Return]

None

[Note]

1. There are several functions in Function 10H that allow extensive display-colors control for both text and graphics modes.

Function: 0BH • Subfunction: 01H — Select Palette Set

[Entry]

AH = 0BH
BH = 01H (Valid on Modes 04H and 05H 320 x 200 only)
BL = 0 – palette set: Background, Green, Red, Brown
1 – palette set: Background, Cyan, Magenta, White

[Return]

None

[Note]

1. For the CGA adapter, the palette set is defined as follows:

Mode	BL	Palette Set
04H	00H	Background, Green, Red, Yellow
	01H	Background, Cyan, Violet, White
05H	00/01H	Background, Cyan, Red, White

10.4.13 Function: 0CH • Write Dot (Pixel)

[Entry]

AH = 0CH
AL = Color value for pixel (Bit 7 is X'OR flag)
BH = Display page (0 base)
CX = X coordinate, column number (0 base)
DX = Y coordinate, row number (0 base)

[Return]

None

[Notes]

1. For coordinates' range, please refer to the resolution field of video mode table in Function 00H.
2. If bit 7 of register AL is set, the requesting color value will be X'OR'ed with memory color value.

10.4.14 Function: 0DH • Read Dot (Pixel)

[Entry]

AH = 0DH
BH = Display page (0 base)
CX = X coordinate, column number (0 base)
DX = Y coordinate, row number (0 base)

[Return]

AL = Dot (Pixel) color

[Note]

1. For coordinates' range, please refer to the resolution field of video mode table in Function 00H.

10.4.15 Function: 0EH • Write Character to Active RAM in Teletype Mode

[Entry]

AH = 0EH
AL = ASCII character
BL = Foreground color in graphics modes

[Return]

None

[Notes]

1. Control characters such as LF, CR, Backspace, and BELL are recognized. (ASCII Codes: LF = 0AH, CR = 0DH, Backspace = 08H, BELL = 07H).

2. Line wrapping and screen scrolling are supported.
3. Cursor is moved to next position after writing a character to screen.
4. PC BIOS version 10/19/81 or earlier; the register BH has to be set to '0'.
5. The color value in register BL will do X'OR with the content of display memory if bit 7 of the register is set in Graphics modes.
6. In Text modes, the attribute of a character written to a new line is taken from the attribute of the last character in previous line. To control the attribute for a character, use Function 09H with blank character/attribute first before the function issued.

10.4.16 Function: 0FH • Get Video State

[Entry]
AH = 0FH

[Return]
AH = Number of displayable columns (1 base)
AL = Current video mode
BH = Current active page (0 base)

10.4.17 Function: 10H

Function 10H • Subfunction: 00H — Set Individual Palette Register (Internal Palette Register)

[Entry]
AH = 10H
AL = 00H (Subfunction)
BH = Color value
BL = Palette register (0–0FH)

[Return]
None

[Notes]
1. Color value in the Internal Palette register serves as a pointer that points to one of external registers (RAMDAC).
2. The color would not be changed by this function on mode 13H.

Function: 10H • Subfunction: 01H — Set Overscan (Border) Register

[Entry]

AH = 10H
AL = 01H (Subfunction)
BH = Color value (00H - FFH)

[Return]

None

[Note]

1. Border color is driven by one of 256 external registers.

Function: 10H • Subfunction: 02H — Set All Palette Registers and OverScan Register

[Entry]

AH = 10H
AL = 02H (Subfunction)
ES: DX = Point to a 17-byte buffer

[Return]

None

[Notes]

1. The first 16 bytes in the buffer are used to store the values for 16 Internal Palette registers. The last byte is the value for Overscan register.
2. The display color would not be affected, except Overscan register on mode 13H.

Function: 10H • Subfunction: 03H — Toggle Intensify/Blinking Bit

[Entry]

AH = 10H
AL = 03H (Subfunction)
BL = 00H - Intensify
01H - Blinking

[Return]

None

[Notes]

1. Bit 7 of the Attribute Byte is interpreted according to the setting state by this function. This function can provide 16 background colors (in intensify state) of 16-color Text modes.
2. This function also supports Monochrome modes (07H, 0FH).

Function: 10H • Subfunction: 4-6H — Reserved

Function: 10H • Subfunction: 07H — Read Individual Palette Register (Internal Palette Register)

[Entry]

AH = 10H
AL = 07H (Subfunction)
BL = Palette register (0–0FH)

[Return]

BH = Color value

[Note]

1. Color Value in Internal Palette register is served as a pointer that points to one of external registers (RAMDAC).

Function: 10H • Subfunction: 08H — Read OverScan (Border) Register

[Entry]

AH = 10H
AL = 08H (Subfunction)

[Return]

BH = Color value

[Note]

1. Border color is from 00H to FFH.

Function: 10H • Subfunction: 09H — Read All Palette Registers and OverScan Register

[Entry]

AH = 10H
AL = 09H (Subfunction)
ES: DX = Point to a 17-byte buffer
(The first 16 bytes for returning values from 16 palette registers respectively and the last byte for Overscan register).

[Return]

ES: DX = Point to the same buffer provided from the entry of function call.

Function: 10H • Subfunction: 0A-0FH — Reserved

Function: 10H • Subfunction: 10H — Set Individual Color Register (RAMDAC/External Palette Registers)

[Entry]

AH = 10H
AL = 10H (Subfunction)
BX = Color Register (00H - FFH)
DH = Red color
CH = Green color
CL = Blue color

[Return]

None

[Notes]

1. Currently, each color is only 6-bit significant. The three colors RGB, are worked as a group and are formed into a 18-bit datum stored in the Color register.
2. The maximum displayable colors are 256 out of 256K colors (two exponential 18).
3. In standard VGA, mode 13H uses all 256 Color registers to display colors.
4. The BIOS will load default values into Color registers whenever Function 00H (Set Video Mode) is called. This is true only when the disable flag of default palette loading is not set (refer to Subfunction 31H of Function 12H).
5. With the gray-summing flag set, the BIOS will weight three color values and sum-to-grayshade value, then it will use the value for all three colors.

Function: 10H • Subfunction: 11H — Reserved

Function: 10H • Subfunction: 12H — Set Block of Color Registers

[Entry]

AH = 10H
AL = 12H (Subfunction)
BX = Start Color register (00H–FFH)
CX = Number of color registers to set
ES: DX = Point to table of color values (each table entry is in RGB format)

[Return]

None

[Notes]

1. Currently, each color is only 6-bit significant. The three colors RGB, are worked as a group and are formed into a 18-bit datum stored in the Color register.
2. The maximum displayable colors are 256 out of 256K colors (2 exponential 18).
3. In standard VGA, mode 13H uses all 256 Color registers to display colors.

4. BIOS will load default values into Color registers whenever Function 00H (Set Video Mode) is called. This is true only when the disable flag of default palette loading is not set (refer to Subfunction 31H of Function 12H).
5. With the gray-summing flag set, the BIOS will weight three color elements (RGB) of Color register; and sum them to grayshade value, which is based on the formula: 30% Red + 59% Green + 11% Blue. The grayshade value will be written back to three elements (RGB) of Color register.

Function: 10H • Subfunction: 13H — Select Color Page (Not valid on Mode 13H)

[Entry]

AH = 10H
AL = 13H (Subfunction)
BL = 00H (select paging mode)
01H (select color page)
When BL = 00H -
BH = 00H (select 4 pages of 64-color register page)
01H (select 16 pages of 16-color register page)
When BL = 01H -
BH = Color page number (0 base)

[Return]

None

[Notes]

1. All video modes, except 256-color modes, are supported by the function.
2. This function treats 256-color registers as sets of 16- or 64-color registers. It can be used to display different colors quickly by switching among color sets (pages).
3. Default setting is Page 0 of 64-color Page mode after Video mode is set. Normally, Function 00H (Set Video Mode) will load the default colors of the first 64-color registers (Page 00H) for all standard VGA modes, except mode 13H (248 registers loading).

Function: 10H • Subfunction: 14H — Reserved

Function: 10H • Subfunction: 15H — Read Individual Color Register (RAMDAC/External Palette Registers)

[Entry]

AH = 10H
AL = 15H (Subfunction)
BX = Color register (00H–FFH)

[Return]

DH = Red color
CH = Green color
CL = Blue color

[Notes]

1. Currently, each color is only 6-bit significant. The three colors RGB, are worked as a group and they are formed into a 18-bit datum stored in the Color register.
2. The maximum displayable colors are 256 out of 256K colors (2 exponential 18).
3. In standard VGA, mode 13H uses all 256-color registers to display colors.
4. With the gray-summing flag set, the only value returned from all three color elements of Color register is the grayshade value.

Function: 10H • Subfunction: 16H — Reserved

Function: 10H • Subfunction: 17H — Read Block of Color Registers

[Entry]

AH = 10H
AL = 17H (Subfunction)
BX = Start Color register (00H–FFH)
CX = Number of Color registers to read
ES: DX = Point to user provided buffer for returned color values

[Return]

ES: DX = Point to same buffer from function call entry (buffer is treated as a color table and each entry of the table consists of three bytes in RGB format).

[Notes]

1. Currently, each color is a 6-bit value. All three colors form a 18-bit datum.
2. The maximum displayable colors are 256 out of 256K colors (two exponential 18).
3. In standard VGA, mode 13H uses all 256-color registers to display colors.
4. BIOS will load default values into Color registers whenever Function 00H (Set Video Mode) is called. This is true only when the disable flag of default palette loading is not set (please refer to Subfunction 31H of Function 12H).
5. With the gray-summing flag set, the only value returned for all three colors is grayshade value.

Function: 10H • Subfunction: 18-19H — Reserved

Function: 10H • Subfunction: 1AH — Read Current State of Color Page (Not valid on Mode 13H)

[Entry]

AH = 10H
AL = 1AH (Subfunction)

[Return]

BH = Current page (Value depends on Paging mode, 00H is default)
BL = Current Paging mode
(00H = 4 pages of 64-Color registers (default), 01H = 16 pages of 16-color registers)

[Notes]

1. All video modes except 256-color modes are supported by the function.
2. This function treats 256-color registers as sets of 16- or 64-color registers. It can be used to display different colors quickly by switching among color sets (pages).
3. Default setting is page 00H of 6-color page mode after Set Video Mode.

Function: 10H • Subfunction: 1BH — Sum Color Values to Grayshades

[Entry]

AH = 10H
AL = 1BH (Subfunction)
BX = Start Color register (00H–FFH)
CX = Number of Color registers to sum

[Return]

None

[Note]

1. This function will sum the Color registers desired into grayshade values regardless the gray-summing flag.

10.4.18 Function: 11H

Function: 11H • Subfunction: 00H — Load User Text Font

[Entry]

AH = 11H
AL = 00H (Subfunction)
BH = Number of bytes per character
BL = Block to load (00H - 07H)
CX = Number of characters to store
DX = ASCII character ID of the first character in the font table (ES: BP)
ES: BP = Point to user-provided font table

[Return]

None

[Notes]

1. This function is only available for text modes. The value in register BH represents the height of each character. The value can be specified a maximum of 32-bytes-per-character in standard VGA specification.
2. In VGA, the character font is loaded into RAM Map 2 (0 base), which can contain up to eight fonts at any time, and is available for the Character Generator only. Consequently, the block value specified in register BL is ranged from 00H (default) to 07H.
3. Two character fonts out of eight can be used at any time. This provides 512 simultaneously displayable characters instead of 256 characters. The way to display two different fonts at one time can be accomplished by the following:
   a) Load fonts into desired blocks.
   b) Subfunction 03H (Select Block Specifier) of Function 11H is called to select two different font blocks out of eight font blocks; one for primary font, the other for secondary font.
   c) The bit 3 of Attribute Byte serves as the Font Block Selector and foreground intensity for the character.
      Bit 3 = 0 — Primary font selected and normal display (eight foreground colors)
      if Subfunction 00H of Function 10H is called with BX = 0712H.
      Bit 3 = 1 — Secondary font selected and normal display (eight foreground colors)
      else
      Bit 3 = 1 — Secondary font selected and intensity display (16 foreground colors)
4. Default setting by BIOS loads a font into Block 0, which is used for both primary font and secondary font (256 displayable characters).
5. The font loading by Subfunction 00H requires caution since the controller is not reprogrammed, abnormal character display may occur. For example:
   If a font table is loaded to override the font in a block, a double image may result (especially when the loaded font size is smaller than the one previously displayed).

Function: 11H • Subfunction: 01H — Load 8 x 14 ROM Font

[Entry]

AH = 11H
AL = 01H (Subfunction)
BL = Block to load (00H - 07H)

[Return]

None

NOTE: This is actually an 8 x 16 font.

[Notes]

1. This function is only available for Text modes.
2. The height of character is 14 bytes, but the height of display cell is same as default setting.
3. In VGA, the character font is loaded into RAM Map 2 (0 base), which can contain up to eight fonts at any time, and is available for the Character Generator only. Consequently, the block value specified in register BL is ranged from 00H (Default) to 07H.
4. Two character fonts out of eight can be used at any time. This provides 512 simultaneously displayable characters, instead of 256 characters. The way to display two different fonts at one time can be accomplished by the following:
   a) Load fonts into desired blocks.
   b) Subfunction 03H (Select Block Specifier) of Function 11H is called to select two different font blocks out of eight font blocks; one for primary font, the other for secondary font.
   c) The bit 3 of Attribute Byte serves as the Font Block Selector and foreground intensity for the character.
      Bit 3 = 0 — Primary font selected and normal display (eight foreground colors)
      if Subfunction 00H of Function 10H is called with BX = 0712H
      Bit 3 = 1 — Secondary font selected and normal display (eight foreground colors)
      else
      Bit 3 = 1 — Secondary font selected and intensity display (16 foreground colors)
5. Default setting by BIOS loads a font into Block 0, which is used for both primary font and secondary font (256 displayable character).
6. The font loading by Subfunction 00H requires caution since the controller is not reprogrammed, abnormal character display may occur. For example:
   If a font table is loaded to override the font in a block, a double image may result (especially when the loaded font size is smaller than the one previously displayed).

Function: 11H • Subfunction: 02H — Load 8 x 8 ROM Font

[Entry]

AH = 11H
AL = 08H (Subfunction)
BL = Block to load (00H - 07H)

[Return]

None

[Notes]

1. This function is only available for text modes.
2. The height of the character is eight bytes, but the height of the display cell is the same as the default setting.
3. In VGA, the character font is loaded into RAM Map 2 (0 base), which can contain up to eight fonts at any time, and is available only for the Character Generator. Consequently, the block value specified in register BL is ranged from 00H (Default) to 07H.
4. Two character fonts out of eight can be used at any time. This provides 512 simultaneously displayable characters, instead of 256 characters. The way to display two different fonts at one time can be accomplished by the following:
   a) Load fonts into desired blocks.
   b) Subfunction 03H (Select Block Specifier) of Function 11H is called to select two different font blocks out of eight font blocks; one for primary font, the other for secondary font.
   c) The Bit 3 of Attribute Byte serves as the Font Block Selector and foreground intensity for the character.

      Bit 3 = 0 — Primary font selected and normal display (eight foreground colors)
      if Subfunction 00H of Function 10H is called with BX = 0712H
      Bit 3 = 1 — Secondary font selected and normal display (eight foreground colors)
      else
      Bit 3 = 1 — Secondary font selected and intensity display (16 foreground colors)
5. Default setting by BIOS loads a font into Block 0, which is used for both primary font and secondary font (256 displayable characters).
6. The font loading by Subfunction 00H requires caution since the controller is not reprogrammed, abnormal character display may occur. For example:

   If a font table is loaded to override the font in a block, a double image may result (especially when the loaded font size is smaller than the one previously displayed).

Function: 11H • Subfunction: 03H — Select Block Specifier

[Entry]

AH = 11H
AL = 03H (Subfunction)
BL = Selection of character generator blocks

[Return]

None

[Notes]

1. The definition of the value in register BL as follows:

Bits	Font Blocks
4, 1, 0	Primary Font Block (00H–07H)
5, 3, 2	Secondary Font Block (00H–07H)

2. For EGA-compatible operation, bits 0–1 are used for primary font, and bits 2–3 for secondary font.
3. To retain eight consistent colors during 512-character display, the Subfunction 00H of Function 10H has to be called first with the following setting:

   AX = 1000H, BX = 0712H

Function: 11H • Subfunction: 04H — Load 8 x 16 ROM Font

[Entry]

AH = 11H
AL = 04H (Subfunction)
BL = Block to load (00H - 07H)

[Return]

None

[Notes]

1. This function is only available for text modes.
2. The height of character is 16 bytes, but the height of the display cell is the same as default setting.
3. In VGA, the character font is loaded into RAM Map 2 (0 base), which can contain up to eight fonts, and is available for the Character Generator only. Consequently, the block value specified in register BL is ranged from 00H (default) to 07H.
4. Two character fonts out of eight can be used at any time. This provides 512 simultaneously displayable characters, instead of 256 characters. The way to display two different fonts at one time can be accomplished by the following:
   a) Load fonts into desired blocks.
   b) Subfunction 03H (Select Block Specifier) of Function 11H is called to select two different font blocks out of eight font blocks; one for primary font, the other for secondary font.

c) The bit 3 of Attribute Byte is served as the Font Block Selector and foreground intensity for the character.
Bit 3 = 0 — Primary font selected and normal display (eight foreground colors).
if Subfunction 00H of Function 10H is called with BX = 0712H
Bit 3 = 1 — Secondary font selected and normal display (eight foreground colors)
else
Bit 3 = 1 — Secondary font selected and intensity display (16 foreground colors).

5. Default setting by BIOS loads a font into Block 0, which is used for both primary font and secondary font (256 displayable characters).
6. The font loading by Subfunction 00H requires caution since the controller is not reprogrammed, abnormal character display may occur. For example:
If a font table is loaded to override the font in a block, a double image may result (especially when the loaded font size is smaller than the one previously displayed).

Function: 11H • Subfunction: 10H — Load User Text Font and Reprogram Controller

[Entry]
AH = 11H
AL = 10H (Subfunction)
BH = Number of bytes per character
BL = Block to load (00H–07H)
CX = Number of characters to store
DX = ASCII character ID of the first character in the font table (ES: BP)
ES: BP = Point to user-provided font table

[Return]
None

[Notes]
1. This function is only available for text modes.
2. The value in register BH represents the height of each character. It can be specified a maximum of 32 bytes per character in standard VGA specification.
3. In VGA, the character font is loaded into RAM Map 2 (0 base), which can contain up to eight fonts at any time, and is available for the Character Generator only. Consequently, the block value specified in register BL is ranged from 00H (default) to 07H.
4. Two character fonts out of eight can be at any time. This provides 512 simultaneously displayable characters, instead of 256 characters. The way to display two different fonts at one time can be accomplished by the following:
a) Load fonts into desired blocks.
b) Subfunction 03H (Select Block Specifier) of Function 11H is called to select two different font blocks out of eight font blocks; one for primary font, the other for secondary font.
c) The bit 3 of Attribute Byte is served as the Font Block Selector and foreground intensity for the character.
Bit 3 = 0 — Primary font selected and normal display (eight foreground colors).
if Subfunction 00H of Function 10H is called with BX = 0712H

Bit 3 = 1 — Secondary font selected and normal display (eight foreground colors)
else
Bit 3 = 1 — Secondary font selected and intensity display (16 foreground colors).

5. Default setting by BIOS loads a font into Block 0, which is used for both primary font and secondary font (256 displayable characters).
6. Subfunction 10H is almost identical to Subfunction 00H except the following differences:
   a) Page 00H has to be active.
   b) Character Height (bytes-per-character) will be recalculated.
   c) Number of rows (0 base) are recalculated as:
   (scanlines-per-screen/Character Height) minus 1.
   d) The length of display buffer will be recalculated as (Total number of rows × Total number of columns) × 2 (1 base).
   e) The CRTC Registers are reprogrammed as follows:

Index	Register Name	Change
09H	Maximum scanlines	Character Height minus 1
0AH	Cursor Start	Character Height minus 2
0BH	Cursor End	Character Height minus 1
12H	Vertical Display Enable End For 350 or 400 scanline Modes (Rows per screen × Character Height) minus 1 For 200 scanline modes (Rows per screen × Character Height) × 2) minus 1	
14H	Underline Location	Character Height minus 1 (Mode 07H only)

   f) It has to be called immediately after Function 00H call (Set Video Mode) or the result will be unpredictable.

Function: 11H • Subfunction: 11H — Load 8 x 14 ROM Font and Reprogram Controller

[Entry]
AH = 11H
AL = 11H (Subfunction)
BL = Block to load (00H–08H)

[Return]
None

NOTE This is actually an 8 x 16 font.

[Notes]
1. This function is only available for Text modes.
2. The character and display cells are both 14 bytes high (scanlines).
3. In VGA, the character font is loaded into RAM Map 2 (0 base), which can contain up to eight fonts at any time and is available for the Character Generator only. Consequently, the block value specified in register BL is ranged from 00H (default) to 07H.

4. Two character fonts out of eight can be used at any time. This provides 512 simultaneously displayable characters, instead of 256 characters. The way to display two different fonts at one time can be accomplished by the following:
   a) Load fonts into desired blocks.
   b) Subfunction 03H (Select Block Specifier) of Function 11H is called to select two different font blocks out of eight font blocks; one for primary font, the other for secondary font.
   c) The bit 3 of Attribute Byte is served as the Font Block Selector and foreground intensity for the character.
      Bit 3 = 0 — Primary font selected and normal display (eight foreground colors).
      if Subfunction 00H of Function 10H is called with BX = 0712H
      Bit 3 = 1 — Secondary font selected and normal display (eight foreground colors)
      else
      Bit 3 = 1 — Secondary font selected and intensity display (16 foreground colors).
5. Default setting by BIOS loads a font into Block 0, which is used for both primary font and secondary font (256 displayable characters).
6. Subfunction 11H is almost identical to Subfunction 01H except the following differences:
   a) Page 00H has to be active.
   b) Character Height = 14.
   c) Number of rows (0 base) are recalculated as:
      (scanlines-per-screen/Character Height) minus 1.
   d) The length of display buffer will be recalculated as:
      (Total number of rows × Total number of columns) × 2 (1 base)
   e) The CRTC registers are reprogrammed as follows:

Index	Register Name	Change
09H	Maximum Scanlines	13 (0DH)
0AH	Cursor Start	12 (0CH)
0BH	Cursor End	13 (0DH)
12H	Vertical Display Enable End	(Rows per screen × 14) minus 1
14H	Underline Location (mode 07H only)	13 (0DH)

   f) It has to be called immediately after Function 00H call (Set Video Mode) or the result will be unpredictable.

Function: 11H • Subfunction: 12H — Load 8 x 8 ROM Font and Reprogram Controller

[Entry]

AH = 11H
AL = 12H (Subfunction)
BL = Block to load (00H–07H)

[Return]

None

[Notes]

1. This function is only available for text modes.
2. The height of character and display cell are all eight bytes (scanlines).
3. In VGA, the character font is loaded into RAM Map 2 (0 base), which can contain up to eight fonts at any time and is available for the Character Generator only. Consequently, the block value specified in register BL is ranged from 00H (default) to 07H.
4. Two character fonts out of eight can be used at any time. This provides 512 simultaneously displayable characters, instead of 256 characters. The way to display two different fonts at one time can be accomplished by the following:
   a) Load fonts into desired blocks.
   b) Subfunction 03H (Select Block Specifier) of Function 11H is called to select two different font blocks out of eight font blocks; one for primary font, the other for secondary font.
   c) The bit 3 of Attribute Byte is served as the Font Block Selector and foreground intensity for the character.
      Bit 3 = 0 — Primary font selected and normal display (eight foreground colors).
      if Subfunction 00H of Function 10H is called with BX = 0712H
      Bit 3 = 1 — Secondary font selected and normal display (eight foreground colors)
      else
      Bit 3 = 1 — Secondary font selected and intensity display (16 foreground colors).
5. Default setting by BIOS loads a font into Block 0, which is used for both primary font and secondary font (256 displayable characters).
6. Subfunction 12H is almost identical to Subfunction 02H except the following differences:
   a) Page 00H has to be active.
   b) Character Height = 8.
   c) Number of rows (0 base) are recalculated as
      (Scanlines per screen/Character Height) minus 1.
   d) The length of display buffer will be recalculated as:
      (Total number of rows × Total number of columns) × 2 (1 base).
   e) The CRTC registers are reprogrammed as follows:

Index	Register Name	Change
09H	Maximum Scanlines	7 (07H)
0AH	Cursor Start	6 (06H)
0BH	Cursor End	7 (07H)
12H	Vertical Display Enable End	(Rows per screen × 8) minus 1
14H	Underline Location (mode 07H only)	7 (07H)

   f) It has to be called immediately after Function 00H call (Set Video Mode). Otherwise, the result will be unpredictable.

Function: 11H • Subfunction: 14H — Load 8 x 16 ROM Font and Reprogram Controller

[Entry]

AH = 11H
AL = 14H (Subfunction)
BL = Block to load (00H–07H)

[Return]

None

[Notes]

1. This function is only available for Text modes.
2. The height of character and display cell are all 16 bytes (scanlines).
3. In VGA, the character font is loaded into RAM Map 2 (0 base), which can contain up to eight fonts at any time and is available for the Character Generator only. Consequently, the block value specified in register BL is ranged from 00H (default) to 07H.
4. Two character fonts out of eight can be used at any time. This provides 512 simultaneously displayable characters, instead of 256 characters. The way to display two different fonts at one time can be accomplished by the following:
   a) Load fonts into desired blocks.
   b) Subfunction 03H (Select Block Specifier) of Function 11H is called to select two different font blocks out of eight font blocks; one for primary font, the other for secondary font.
   c) The bit 3 of Attribute Byte is served as the Font Block Selector and foreground intensity for the character.

   Bit 3 = 0 – Primary font selected and normal display (eight foreground colors).

   If Subfunction 00H of Function 10H is called with BX = 0712H

   Bit 3 = 1 — Secondary font selected and normal display (eight foreground colors)

   else

   Bit 3 = 1 — Secondary font selected and intensity display (16 foreground colors).
5. Default setting by BIOS loads a font into Block 0, which is used for both primary font and secondary font (256 displayable characters).
6. Subfunction 14H is almost identical to Subfunction 04H except the following differences:
   a) Page 00H has to be active.
   b) Character Height = 16.
   c) Number of Rows (0 base) are recalculated as:
   (Scanlines per screen ÷ Character Height) minus 1.
   d) The length of display buffer will be recalculated as (Total number of rows × Total number of columns) × 2 (1 base).
   e) The CRTC registers are reprogrammed as follows:

Index	Register Name	Change
09H	Maximum Scanlines	15 (0FH)
0AH	Cursor Start	14 (0EH)
0BH	Cursor End	15 (0FH)
12H	Vertical Display Enable End	(Rows per screen x16) minus 1
14H	Underline Location	15 (0FH) (mode 07H only)

   f) It has to be called immediately after Function 00H call (Set Video Mode) or the result will be unpredictable.

Function: 11H • Subfunction: 20H — Set Pointer of User's Graphics Font Table to Interrupt 1FH

[Entry]

AH = 11H
AL = 20H (Subfunction)
ES: BP = Point to user's graphics font table

[Return]

None

[Notes]

1. The value in this Interrupt Vector serves as a pointer that points to Graphics Font for character codes (80H–FFH) in modes 04H, 05H, and 06H.
2. In the CGA adapter, the planar BIOS only provides 128 character codes (00H–7FH). The user can supply the other half of character codes (80H–FFH), or use GRAFTABL in DOS to load these character codes.
3. This function has to be called immediately after Set Video Mode.

Function: 11H • Subfunction: 21H — Set Pointer of User's Graphics Font Table to Interrupt 43H

[Entry]

AH = 11H
AL = 21H (Subfunction)
BL = Character rows specifier
    00H = Value in register DL (the number of displayable rows specified by user)
    01H = 14 (0EH) character rows
    02H = 25 (19H) character rows
    03H = 43 (2BH) character rows
CX = Bytes per character
DL = Number of character rows (if register BL = 00H)
ES: BP = Point to user's graphics font table

[Return]

None

[Note]

1. The value in this Interrupt Vector serves as a pointer that points to Graphics Font for character codes (00H–7FH) in modes 04H, 05H, and 06H. The vector also handles Graphics Font for Character Codes (00H–FFH) in all other Graphics modes.
2. This function should only be called immediately after Set Video Mode.
3. The portion of character rows above displayable rows will not be displayed unless it is scrolled up.
4. The overlapping screen may occur on video modes that use all display memory addresses, such as mode 13H.

Function: 11H • Subfunction: 22H — Set Pointer of ROM 8 x14 Graphics Font Table to Interrupt 43H

[Entry]

AH = 11H
AL = 22H (Subfunction)
BL = The specifier of character rows on screen
- 00H = Value in register DL (the number of displayable rows specified by user)
- 01H = 14 (0EH) character rows
- 02H = 25 (19H) character rows
- 03H = 43 (2BH) character rows

DL = Number of character rows to display (if register BL = 00H)

[Return]

None

NOTE: This is actually an 8 x 16 font.

[Notes]

1. The value in this Interrupt Vector serves as a pointer that points to Graphics Font for Character Codes (00H–7FH) in Modes 04H, 05H, and 06H. The vector also handles Graphics Font for character codes (00H - FFH) in all other graphics modes.
2. This function should only be called immediately after setting Video Mode.
3. The portion of character rows above displayable rows will not be displayed unless it is scrolled up.
4. The overlapping screen may occur on video modes that use all Display Memory addresses, such as Mode 13H.

Function: 11H • Subfunction: 23H — Set Pointer of ROM 8 x 8 Graphics Font Table to Interrupt 43H

[Entry]

AH = 11H
AL = 23H (Subfunction)
BL = Specifier of character rows on screen
- 00H = Value in Register DL (the number of displayable rows specified by user)
- 01H = 14 (0EH) character rows
- 02H = 25 (19H) character rows
- 03H = 43 (2BH) character rows

DL = Number of character rows to display (if Register BL = 00H)

[Return]

None

[Notes]

1. The value in this Interrupt Vector serves as a pointer that points to Graphics Font for character codes (00H - 7FH) in Modes 04H, 05H, and 06H. The vector also handles Graphics Font for character codes (00H - FFH) in all other graphics modes.
2. This function should only be called immediately after setting Video Mode.

3. The portion of character rows above displayable rows will not be displayed unless it is scrolled up.
4. The overlapping screen may occur on video modes that use all Display Memory addresses, such as Mode 13H.

Function: 11H • Subfunction: 24H — Set Pointer of ROM 8 x 16 Graphics Font Table to Interrupt 43H

[Entry]

AH = 11H
AL = 24H (Subfunction)
BL = Specifier of character rows on screen
  00H = Value in Register DL (the number of displayable rows specified by user)
  01H = 14 (0EH) character rows
  02H = 25 (19H) character rows
  03H = 43 (2BH) character rows
DL = Number of character rows to display (if Register BL = 00H)

[Return]

None

[Notes]

1. The value in this Interrupt Vector serves as a pointer that points to Graphics Font for character codes (00H - 7FH) in Modes 04H, 05H, and 06H. The vector also handles Graphics Font for character codes (00H - FFH) in all other graphics modes.
2. This function should only be called immediately after setting Video Mode.
3. The portion of character rows above displayable rows will not be displayed unless it is scrolled up.
4. The overlapping screen may occur on video modes that use all Display Memory addresses, such as Mode 13H.

Function: 11H • Subfunction: 30H — Get Pointer Information of Fonts

[Entry]

AH = 11H
AL = 30H (Subfunction)
BH = Pointer information of fonts
- 00H - Current Font Pointer stored in Interrupt Vector 1FH
- 01H - Current Font Pointer stored in Interrupt Vector 43H
- 02H - Font Pointer of ROM 8 x 16 Font Table
- 03H - Font Pointer of ROM 8 x 8 Font Table (Character Codes 00H - 7FH)
- 04H - Font Pointer of ROM 8 x 8 Font Table (Character Codes 80H - FFH)
- 05H - Font Pointer of ROM 8 x 16 Alternate Font Table
- 06H - Font Pointer of ROM 8 x 16 Font Table
- 07H - Font Pointer of ROM 9 x 16 Alternate Font Table

[Return]

CX = Current character height (Bytes per Character)
DL = Number of rows of current video mode (0 base)
ES: BP = Pointer information of desired font

10.4.19 Function: 12H

Function: 12H • Subfunction: 10H — Get Current Video Configuration

[Entry]
AH = 12H
BL = 10H (Subfunction)

[Return]
BH = 00H - Color Mode (3Dx)
01H - Monochrome Mode (3Bx)
BL = Video Memory Size
00H = 64K bytes
01H = 128K bytes
02H = 192K bytes
03H = 256K bytes

CH = Feature Bits	Feature Control Output Bit Setting	Input Status Register 0 - (3C2H)
0	0	Bit 5
1	0	Bit 6
2	1	Bit 5
3	1	Bit 6
4 - 7	Reserved	

CL = Switch Settings	Description
Bit 0	Configuration Switch-1
Bit 1	Configuration Switch-2
Bit 2	Configuration Switch-3
Bit 3	Configuration Switch-4
Bit 4 - Bit 7	Reserved

Function: 12H • Subfunction: 20H — Alternate PrintScreen Handler

[Entry]
AH = 12H
BL = 20H (Subfunction)

[Return]
None

[Note]
1. This function call will replace original PrintScreen Interrupt Handler (Interrupt 05H) to support the modes whose displayable rows on screen are over 25 rows.

Function: 12H • Subfunction: 30H — Select Scanlines for Text Modes

[Entry]

AH = 12H
BL = 30H (Subfunction)
AL = Specifier of scanlines
00H = 200 scanlines
01H = 350 scanlines
02H = 400 scanlines

[Return]

AL = 12H (function supported)

[Notes]

1. The selected scanlines will take effect on next mode setting.
2. Mode 07H is only supported 350/400 scanlines. Modes 00H - 03H are supported by three scanlines.
3. The modes, 200 scanlines, are double scanned.

Function: 12H • Subfunction: 31H — Enable/Disable Default Palette Loading

[Entry]

AH = 12H
BL = 31H (Subfunction)
AL = 00H - Enable default palette loading
01H - Disable default palette loading

[Return]

AL = 12H (function supported)

[Notes]

1. This function will take effect on next mode setting.
2. All Internal/External Palette Registers will be affected.

Function: 12H • Subfunction: 32H — Enable/Disable Video

[Entry]
AH = 12H
BL = 32H (Subfunction)
AL = 00H - Enable Video
01H - Disable Video

[Return]
AL = 12H (function supported)

[Note]
1. Video subsystem will not respond to any I/O or Video Memory Addressing.

Function: 12H • Subfunction: 33H — Enable/Disable Summing-to-Grayshades

[Entry]
AH = 12H
BL = 33H (Subfunction)
AL = 00H - Enable summing-to-grayshades
01H - Disable summing-to-grayshades

[Return]
AL = 12H (function supported)

[Note]
1. This function will take effect on a subsequent mode setting or internal/external palettes setting.

Function: 12H • Subfunction: 34H — Enable/Disable Cursor Emulation

[Entry]
AH = 12H
BL = 34H (Subfunction)
AL = 00H - Enable cursor emulation
01H - Disable cursor emulation

[Return]
AL = 12H (function supported)

[Notes]
1. This function will take effect on a subsequent mode setting or Function 01H call (set cursor type).
2. Bit 0 of Address [40:87] Emulation Flag is affected.

Function: 12H • Subfunction: 35H — Switch Video Display

[Entry]

AH = 12H
BL = 35H (Subfunction)
AL = 00H - Initial video adapter turned off
(ES:DX must point to a 128-byte buffer for switching state save area)
01H - System board video turned on
02H - Active video turned off (ES:DX must point to a buffer for switching state save area)
03H - Inactive video turned on (ES:DX must point to a buffer which saves switching state previously)
ES:DX = Buffer for switching state (valid when AL = 00H, 02H, or 03H)

[Return]

AL = 12H (function supported)

[Notes]

1. There are several requirements that have to be met before using this function. These requirements are:
   a) Two video subsystems coexisting: system board video and video adapter.
   b) The usage of video resources has conflicted between two video systems.
   c) Video adapter is primary video system board is secondary video.
   d) This function has to be supported by system board video and video adapter.

2. If the first time switching from video adapter to system board video:
   Call the function with Register AL = 00H
   Call the function with Register AL = 01H
   else
   Call the function with Register AL = 02H
   Call the function with Register AL = 03H

Function: 12H • Subfunction: 36H — Enable/Disable Screen Display

[Entry]

AH = 12H
BL = 36H (Subfunction)
AL = 00H - Enable screen display
01H - Disable screen display

[Return]

AL = 12H (function supported)

[Note]

1. This function can be used for fast video memory updating without losing synchronization.

10.4.20 Function: 13H • Write Teletype String

[Entry]

AH = 13H

AL = Write function specifier

- 00H - Write character string without updating cursor (BL = Attribute)
- 01H - Write character string with updating cursor (BL = Attribute)
- 02H - Write character/attribute string without updating cursor
- 03H - Write character/attribute string with updating cursor

BH = Display page (0 base)

BL = Attribute (valid when AL = 00H or 01H)

CX = String length

DH = Start Y coordinate of string displayed on screen

DL = Start X coordinate of string displayed on screen

ES: BP = Start address of string (in Segment: Offset Format)

[Return]

None

[Notes]

1. Control Characters: LF, CR, Backspace, and BELL are recognized. (ASCII Codes: LF = 0AH, CR = 0DH, Backspace = 08H, BELL = 07H).
2. String can be written to any pages regardless of active state.
3. Line wrapping and screen scrolling are supported. Screen scrolling is only supported on active page.
4. The color value in Register BL will do X'OR with the content of display memory, if Bit 7 of the register is set in graphics modes.

10.4.21 Function: 1AH

Function: 1AH • Subfunction: 00H — Get Display Combination Code (DCC)

[Entry]

AH = 1AH
AL = 00H (Subfunction)

[Return]

If function supported:
AL = 1AH
BH = Alternate display code
BL = Active display code

[Notes]

1. The index of current DCC entry in DCC table is stored in address [40:8A].
2. Display Combination Code Definition:

Code	Definition
00H	No Display
01H	Monochrome Display Adapter (MDA)
02H	Color Display Adapter (CGA)
03H	Reserved
04H	EGA with Color Monitor (EGA)
05H	EGA with Monochrome Monitor (MEGA)
06H	Professional Graphics Adapter with Color Display (PGA)
07H	Video Graphics Array with Analog Monochrome Monitor (MVGA)
08H	Video Graphics Array with Analog Color Monitor (VGA)

Function: 1AH • Subfunction: 01H — Set Display Combination Code (DCC)

[Entry]

AH = 1AH
AL = 01H (Subfunction)
BH = Alternate display code
BL = Active display code

[Return]

If function supported:
AL = 1AH

[Note]

1. Display Combination Code Definition:

Code	Definition
00H	No Display
01H	Monochrome Display Adapter (MDA)
02H	Color Display Adapter (CGA)
03H	Reserved
04H	EGA with Color Monitor (EGA)
05H	EGA with Monochrome Monitor (MEGA)
06H	Professional Graphics Adapter with Color Display (PGA)
07H	Video Graphics Array with Analog Monochrome Monitor (MVGA)
08H	Video Graphics Array with Analog Color Monitor (VGA)

2. User is responsible for providing correct DCC. There is no physical checking device.

10.4.22 Function: 1BH

Function: 1BH • Collection of Video Information

[Entry]

AH = 1BH
BX = 00H
ES: DI = Pointer points to 128-byte buffer

[Return]

If function supported
AL = 1BH

[Notes]

1. Video information in 128-byte buffer:

Offset	Size	Definition
00H	2 Words	Pointer points to collection of static functionality information
04H	Byte	Current Video Mode
05H	Word	Number of columns (1 base)
07H	Word	Refresh Buffer Length (unit: byte)
09H	Word	The starting address of Refresh Buffer (Offset value relates to start of video memory; default = 0000H)
0BH	8 Words	Cursor Position for each page (maximum eight pages supported)
1BH	Word	Current Cursor Type (High Byte = start scanline, Low Byte = end scanline)
1DH	Byte	Active Video Page
1EH	Word	Base Port Address of CRT Controller (CRTC) (Monochrome = 3BxH, Color = 3DxH)
20H	Byte	Current setting of 3B8H or 3D8H (Mode Control Register)
21H	Byte	Current setting of 3B9H or 3D9H
22H	Byte	Number of rows (1 base)
23H	Word	Character height (1 base; unit: scanline)
25H	Byte	Active Display Code
26H	Byte	Alternate Display Code
27H	Word	Number of displayable colors (1 base; monochrome = 0000H)
29H	Byte	Number of Pages (1 base)
2AH	Byte	Specifier of vertical resolution 00H = 200 scanlines 01H = 350 scanlines 02H = 400 scanlines 03H = 480 scanlines 04H - FFH = Reserved
2BH	Byte	Primary Font Block (00H - 07H)
2CH	Byte	Secondary Font Block (00H - 07H)
2DH	Byte	Flags of Video State: **Bit** **Definition** 7-6 Reserved 0 = Background intensity 1 = Blinking (Default) 4 0 = Cursor Emulation Disable 1 = Cursor Emulation Enable 3 0 = Default Palette Loading Enable 1 = Default Palette Loading Disable 2 0 = Color Monitor Attached 1 = Monochrome Monitor Attached 1 0 = Summing-to-grayshades Disable 1 = Summing-to-grayshades Enable 0 1 = All Modes are active on all displays
2E - 30H	Reserved	
31H	Byte	Specifier of total video RAM 00H = 64K bytes

		01H = 128K bytes 02H = 192K bytes 03H = 256K bytes 04H - FFH = Reserved
32H	Byte	Save pointer state information: Bit Definition 7-6 Reserved 5 1 = Extension of Display Combination Code Active 4 1 = Palette Override Active 3 1 = Graphics Font Override Active 2 1 = Alpha Font Override Active 1 1 = Dynamic Save Area Active 0 1 = 512-character Set Active
33 - 3FH	Reserved	

2. Collection of static functionality information:

Offset	**Size**	**Definition**
00H	Byte	Available video modes if bit set: **Bit** **Video Mode** 0 00H 1 01H 2 02H 3 03H 4 04H 5 05H 6 06H 7 07H
01H	Byte	Available video modes if bit set: **Bit** **Video Mode** 0 08H 1 09H 2 0AH 3 0BH 4 0CH 5 0DH 6 0EH 7 0FH
00H	Byte	Available video modes if bit set: **Bit** **Video Mode** 0 10H 1 11H 2 12H 3 13H 4 - 7 Reserved
03 - 06H	Reserved	
07H	Byte	Number of scanlines available in text modes: (Subfunction 30H, Function 12H)

		Bit **Scanlines (if Bit = 1)**
		0 200
		1 350
		2 400
		3 - 7 Reserved
08H	Byte	Number of active character blocks available in text modes
09H	Byte	Maximum number of character blocks available in text modes
0AH	Byte	Supported functions (No. 1):
		Bit **Function (if Bit = 1)**
		0 All Modes on All Displays
		1 Summing to grayshades
		2 Character fonts Loading
		3 Default Palette Loading
		4 Cursor Emulation
		5 EGA Palettes (Internal Palettes)
		6 Color Palettes (External Palettes/RAMDAC)
		7 Color Paging
0BH	Byte	Supported functions (No. 2):
		Bit **Function (if Bit = 1)**
		0 Reserved
		1 Save/Restore Video State
		2 Background Intensity/Blinking Control
		3 Set Display Combination Code
		4 - 7 Reserved
0C - 0DH	Reserved	
0EH	Save Pointer Functions:	
		Bit **Function (if Bit = 1)**
		0 512-character Set
		1 Dynamic Save Area
		2 Alpha Font Override
		3 Graphics Font Override
		4 Palette Override
		5 Extension of Display Combination Code
		6 - 7 Reserved
0FH	Reserved	

10.4.23 Function: 1CH

Function: 1CH • Subfunction: 00H — Get Buffer Size for Video State

[Entry]

AH = 1CH
AL = 00H (Subfunction)
CX = Requested Video State:

Bit	Video State
0	Hardware State
1	BIOS Data Area
2	Color Registers (External Palettes/RAMDAC)
3 - 15	Reserved

[Return]

If function supported
AL = 1CH
BX = Blocks/Buffer (Unit: 64 Byte/Block)

[Note]

1. This function will report the sufficient size of buffer to save video state. To guarantee Subfunction 01H and 02H are performed successfully, call this subfunction first.

Function: 1CH • Subfunction: 01H — Saving Video State

[Entry]

AH = 1CH
AL = 01H (Subfunction)
CX = Requested Video States:

Bit	Video States
0	Hardware State
1	BIOS Data Area
2	Color Registers (External Palettes/RAMDAC)
3 - 15	Reserved

ES: BX = Pointer points to buffer (Segment: Offset format)

[Return]

If function supported:
AL = 1CH
ES: BX = State information saved in user-supplied buffer

Function: 1CH • Subfunction: 02H — Restore Video State

[Entry]

AH = 1CH

AL = 02H (Subfunction)

CX = Requested Video States:

Bit	Video States
0	Hardware State
1	BIOS Data Area
2	Color Registers (External Palettes/RAMDAC)
3 - 15	Reserved

ES: BX = Pointer points to previous saved buffer (Segment: Offset format)

[Return]

If function supported:

AL = 1CH

10.5 VGA Sleep Mode And Display Switching

The IBM VGA standard supports a Sleep Mode feature to enable/disable CPU addressing of the VGA subsystem video memory and I/O ports. For integrated VGA subsystems on the motherboard, the video subsystem is enabled or disabled by programming a Video Subsystem Enable Register at I/O Port 3C3H. On VGA adapter cards, a control register at I/O Port 46E8H is used. These two separate schemes of enabling/disabling addressing allows two VGAs (driving separate display monitors) to coexist in a system and have the capability to switch active video from one display to another. The IBM standard VGA BIOS supports a set of function calls to select Sleep Mode and display switching features.

The CL-GD543X/'4X VGA controller, depending on the application, can be programmed to respond at either 3C3H or 46E8H I/O Port for enabling/disabling CPU addressing. This allows for full IBM VGA compatibility, whether the design is an integrated motherboard VGA or an adapter card solution.

See Section 10.2 for the power-on initialization sequence.

10.6 Address Maps

The tables on the following pages provide background information regarding the usage of system memory, port address space, and interrupt vectors by DOS and its I/O routines (Planar and Peripheral BIOSes). The areas of interest to video subsystem users and designers are highlighted in bold text.

Table 10-1. MS DOS Memory Map After Loading

FE0000–FFFFFF	128 Kbytes to 'shadow' system ROM BIOS
100000–FDFFFF	15 Mbytes of extended memory in protected mode only
FFFF:000F (I Mbyte)	**Planar BIOS**
F000:0000	**Expansion BIOS (motherboard video BIOS)**
E000:0000	Voice Communication BIOS/LIM EMS page map area
D000:8000	Network BIOS/LIM EMS page map area
D000:0000	LIM EMS page map area
C000:C000	Hard disk BIOS
C000:8000	**EGA/VGA adapter BIOS**
C000:0000	EGA display RAM
B000:C000	CGA display RAM (or HGC mode graphics RAM)
B000:8000	HGC display RAM
B000:4000	MDA/HGC display RAM
B000:0000	**EGA/VGA display RAM**
A000:0000	**Top of system RAM** COMMAND.COM (transient portion), free RAM, COMMAND.COM (resident portion), installable device drivers, file control blocks, disk buffers, DOS tables, DOS kernel (MSDOS.SYS), resident DOS device drivers (IO.SYS)
0000:0600	ROM BIOS data area
0000:0400	Interrupt vectors
0000:0000	

Table 10-2. BIOS Data Area Assignments

0040:0000 WORD		COM1 Port base address
0040:0002 WORD		COM2 Port base address
0040:0004 WORD		COM3 Port base address
0040:0006 WORD		COM4 Port base address
0040:0008 WORD		Printer 1 port base address
0040:000A WORD		Printer 2 port base address
0040:000C WORD		Printer 3 port base address
0040:000E WORD		Printer 4 port base address
0040:0010 WORD	**EQUIPMENT_FLAG**	

Bit	**Definition**		
D15, D14	No. or printer adapters		
D13,D12	reserved		
D11,D10,D9	No. of RS232-C		
D8	reserved		
D7,D6	No. of diskette drives		
D5,D4	Identify the current primary display device:		
	D5	**D4**	**Adapter**
	0	0	EGA (or none)
	0	1	CGA 40 x 25
	1	0	CGA 80 x 25
	1	1	MDA
D3,D2	reserved		
D1	math coprocessor		
D0	IPL diskette		

0040:0012 BYTE		reserved
0040:0013 WORD	USABLE_RAM	Usable memory size in kilobytes
0040:0015 BYTE		reserved
0040:0016 BYTE		reserved
0040:0017 WORD	KBD_CNTRL	stores status of special keys
0040:0019 BYTE	ALT_KBD	alternate keypad entry
0040:001A WORD	KBD_BUF_HD	Points to head of keyboard buffer
0040:001C WORD	KBD_BUF_TL	Points to tail of keyboard buffer
0040:001E 16 WDS	KBD_BUFFER	Circular keyboard buffer
0040:003E BYTE		Diskette drive re-calibrate status
0040:003F BYTE		Diskette drive motor status
0040:0040 BYTE		Diskette drive motor off counter
0040:0041 BYTE		Last diskette driver operation status
0040:0042 7 BYTES		Diskette driver controller status
0040:0049 BYTE	**VIDEO_MODE**	**Current BIOS Video Mode**
0040:004A WORD	**COLUMNS**	**Number of text columns**
0040:004C WORD	**PAGE_LENGTH**	**Length of each page in bytes**
0040:004E WORD	**START_ADDR**	**Start Address Register value for page**
0040:0050 8 WDS	**CURSOR_POS**	**Cursor positions for all eight pages The high byte of each word contains the character row, the low byte the column**
0040:0060 WORD	**CURSOR_TYPE**	**Start and ending lines for text**

		cursor. High byte has start line.
0040:0062 BYTE	**ACTIVE_PAGE**	**Currently displayed page number**
0040:0063 WORD	**ADDR_CRTC**	**I/O Port address of 6845/CRTC address register (3B4 monochrome; 3D4 color)**
0040:0065 BYTE	**CRT_MODE_SET**	**Current value for Mode Control register (3B8 MDA; 3D8 CGA). The EGA and VGA values emulate the MDA/CGA values**
0040:0066 BYTE	**CRT_PALETTE**	**Current value for the CGA color select register (3D9); emulated by EGA/VGA**
0040:0067 DWORD		pointer to MCA PS/2 reset code
0040:006B BYTE		reserved
0040:006C DWORD		Timer counter
0040:0070 BYTE		Timer overflow
0040:0071 BYTE		Break key state
0040:0072 WORD		RESET flag
0040:0074 BYTE		Last hard disk drive operation status
0040:0075 BYTE		No. of hard disk drives attached
0040:0076 BYTE		PC XT hard disk drive control
0040:0077 BYTE		PC XT hard disk drive controller port
0040:0078 BYTE		Printer 1 Time-out value
0040:0079 BYTE		Printer 2 Time-out value
0040:007A BYTE		Printer 3 Time-out value
0040:007B BYTE		Printer 4 Time-out value
0040:007C BYTE		COM1 Time-out value
0040:007D BYTE		COM2 Time-out value
0040:007E BYTE		COM3 Time-out value
0040:007F BYTE		COM4 Time-out value
0040:0080 WORD		Keyboard Buffer Start Offset pointer
0040:0082 WORD		Keyboard Buffer End Offset pointer
0040:0084 BYTE	**ROWS**	**Number of text rows minus 1**
0040:0085 WORD	**CHAR_HEIGHT**	**Bytes-per-character**
0040:0087 BYTE	**INFO_1**	

Bit	**Description**
D7	Equals Bit D7 from AL register on most recent mode select. (A one indicates display memory was not cleared by mode select).
D6, D5	Display memory size (00=64K, 01=128K, 10=192K, 11=256K).
D4	Reserved.
D3	A zero indicates EGA is the primary display.
D2	A one will force the BIOS to wait for Vertical Retrace before memory write.
D1	A one indicates that EGA is in Monochrome Mode.
D0	A zero means that CGA cursor emulation is enabled. The cursor shape will be modified if enhanced text is used.

0040:0088 BYTE	**INFO_3**	
	D4-D7	Feature Control Bits (from Feature Control Register).

	D0-D3	EGA Configuration Switch settings.

0040:0089 BYTE FLAGS Miscellaneous flags

D7	Alphanumeric Scanlines (with Bit 4): **Bit 7 Bit 4** 0 0 350-line Mode 0 1 400-line Mode 1 0 200-line Mode 1 1 (reserved)
D6	1 – display switching is enabled 0 – display switching is disabled
D5	Reserved
D4	(see Bit 7)
D3	1 – default palette loading is disabled 0 – default palette loading is enabled
D2	1 – using monochrome monitor 0 – using color monitor
D1	1 – grayscale summing is enabled 0 – grayscale summing is disabled
D0	1 – VGA active 0 – VGA not active

0040:008A BYTE	Reserved
0040:008B BYTE	Media control
0040:008C BYTE	Hard disk drive controller status
0040:008D BYTE	Hard disk drive error status
0040:008E BYTE	Hard disk drive interrupt control
0040:008F BYTE	Reserved
0040:0090 BYTE	Drive 0 Media state
0040:0091 BYTE	Drive 1 Media state
0040:0092 BYTE	Reserved
0040:0093 BYTE	Reserved
0040:0094 BYTE	Drive 0 Current cylinder
0040:0095 BYTE	Drive 1 Current cylinder
0040:0096 BYTE	Keyboard Mode State and Type flags
0040:0097 BYTE	Keyboard LED Flags
0040:0098 WORD	Address offset to User Wait Complete flag
0040:009A WORD	Segment address to User Wait Complete flag
0040:009C WORD	User wait count – Low word (µsecs)
0040:009E WORD	User wait count – High word (µsecs)
0040:00A0 BYTE	Wait active flag
0040:00A1 BYTE	Reserved
0040:00A2 BYTE	Reserved
0040:00A3 BYTE	Reserved
0040:00A4 BYTE	Reserved
0040:00A5 BYTE	Reserved
0040:00A6 BYTE	Reserved
0040:00A7 BYTE	Reserved

0040:00A8 DWORD SAVE_PTR Pointer to BIOS Save Pointer Table

NOTE: The next 84 bytes from 0040:00A1 to 0040:00FF are reserved.

Table 10-3. I/O Port Assignment for PC XT and AT Computers

Port Usage for PC XT	I/O Address	Port Usage for AT
DMA Controller	000 - 0IF	DMA Controller, Note 1
Interrupt Controller	020 - 03F	Interrupt Controller, Note 1
Timer	040 - 04F	Coprocessor access, Timer
	050 - 05F	Timer
PPI (system configuration)	060 - 063	
	060 - 06F	Keyboard
Reserved	070 - 07F	Real-time Clock
DMA Page Register	080 - 09F	DMA Page Register
NMI Mask Register	0A0 - 0AF	
	0A0 - 0BF	Interrupt Controller, Note 2
Reserved	0B0 - 0FF	
	0C0 - 0DF	DMA Controller, Note 2
	0F0 - 0FF	Math coprocessor
Unusable	100 - 13F	Reserved
Unusable	140 - 14F	Token Ring Adapter, Note 2
Unusable	150 - 15F	Advanced Color Graphics Display
Unusable	160 - 16F	Advanced Mono Graphics Display
Unusable	170 - 177	Fixed-disk Adapter, Note 2
Unusable	1C0 - 1CF	Token Ring Adapter, Note 1
Unusable	1E8 - 1EF	Streaming Tape Drive Adapter
Unusable	IF0 - IF7	Fixed-Disk Adapter, Note 1
Unusable	1F8 - 1FF	Reserved
Game I/O	200 - 20F	Game I/O
Expansion Unit	210 - 217	
Multifunction Card, Note 1	218 - 21F	Multifunction Card, Note 1
Reserved	220 - 24F	
	278 - 27F	Parallel Port 2
Clock Calendar, Note 1	2C0 - 2CF	Clock Calendar, Note 1
	2D0 - 2DF	3278/79 Emulation Adapter, Clock/calender, Note 1
Serial Port 4, Note 1	2E0 - 2E7	
Serial Port 3 or 4, Note 1	2E8 - 2EF	
Reserved	2F0 - 2F7	Interrupt Sharing
Serial Port 2	2F8 - 2FF	Serial Port 2
Prototype Card	300 - 31F	Prototype Card
Fixed Disk	320 - 32F	
	360 - 36F	PC Network
Parallel Port 1	378 - 37F	Parallel Port 1
SDLC	380 - 38F	SDLC, Bisync 2
Bisync	3A0 - 3AF	Bisync 1
MDA and printer adapter	**3B0 - 3BF**	**MDA, EGA/VGA and printer adapter**
EGA/VGA Adapter	**3C0 - 3CF**	**EGA/VGA**
CGA	**3D0 - 3DF**	**CGA, EGA/VGA**
Reserved	3E0 - 3E7	
Serial Port 3, Note 1	3E8 - 3EF	

Table 10-3. I/O Port Assignment for PC XT and AT Computers *(cont.)*

Port Usage for PC XT	I/O Address	Port Usage for AT
Diskette Controller	3F0 - 3F7	Diskette Controller
Serial Port 1	3F8 - 3FF	Serial Port 1
	400 - 43F	Reserved
	440 - 44F	Coprocessor Access
	450 - 50F	Reserved
	510 - 52F	Multi-protocol Adapter
	550 - 557	Coprocessor to main CPU communication
	6F0 - 6F7	Interrupt sharing
	910 - 92F	Multi-protocol Adapter
	D10 - D2F	Extended Monochrome Graphics Display
	E90 - E9F	PSLA
	1230-124F	1st Address range: multi-port async
	2230-224F	2nd Address range: multi-port async
	3230-324F	3rd Address range: multi-port async
	4230-424F	4th Address range: multi-port async
	46E8	**VGA add-in Adapter Sleep Enable**

NOTE: Use of port for this function is common, but not standard.

Table 10-4. Interrupt Vector Assignments

VECTOR TABLE ENTRY	INT NO.	NAME	
0000:0000	0	Divide by zero	
0000:0004	1	Single step	
0000:0008	2	Non-maskable	
0000:000C	3	Break-point	
0000:0010	4	Overflow	
0000:0014	5	Print screen	
0000:0018	6	(Reserved)	
0000:001D	7	(Reserved)	
0000:0020	8	Time	H/W IRQ0
0000:0024	9	Keyboard	H/W IRQ1
0000:0028	A	Network	H/W IRQ2
0000:002C	B	Comm. Port 2	H/W IRQ3
0000:0030	C	Comm. Port 1	H/W IRQ4
0000:0034	D	Hard disk	H/W IRQ5
0000:0038	E	Diskette	H/W IRQ6
0000:003C	F	Printer	H/W IRQ7
0000:0040	**10**	**EGA/VGA BIOS Video Services**	
0000:0044	11	Equipment check	
0000:0048	12	Determine memory size	
0000:004C	13	Diskette/disk	
0000:0050	14	Communications	
0000:0054	15	Cassette (***see*** Notes)	
0000:0058	16	Keyboard	
0000:005C	17	Printer	
0000:0060	18	Resident BASIC	
0000:0064	19	Bootstrap	
0000:0068	1A	Time of day	
0000:006C	1B	Keyboard break	
0000:0070	1C	Timer tick	
0000:0074	**1D**	**Video initialization**	
0000:0078	1E	Diskette parameters	
0000:007C	**1F**	**Optional Pointer to Upper 128 CGA 8 x 8 characters**	

Table 10-4. Interrupt Vector Assignments *(cont.)*

THE FOLLOWING INTERRUPTS ARE RESERVED FOR USE BY DOS:

VECTOR TABLE ENTRY	INT NO.	NAME
0000:0080	20	Program Terminate
0000:0084	21	Function Request
0000:0088	22	Terminate Process Exit Address
0000:008C	23	Control-C Handler Address
0000:0090	24	Critical Error Handler Address
0000:0094	25	Absolute Disk Read
0000:0098	26	Absolute Disk Write
0000:009C	27	Terminate But Stay Resident
0000:00AA-00B8	28-2E	Reserved
0000:00BC	2F	Print Spool Control
0000:00C0-00FC	30-3F	Reserved
0000:0108	**42**	**Old BIOS Video Services**
0000:010C	**43**	**Pointer to CGA 8 x 8 Char Set**

NOTES:

1) The INT 15 interrupt service handler has an additional responsibility in systems with an E000 segment video BIOS; besides cassette service, it will handle video subsystem services.
2) The complete list of interrupt numbers goes to FFH; each vector is a double word so the pointer for INT xH is stored at absolute location 4xH.

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Appendix A1

Connector Pinouts

CONNECTOR PINOUTS

Table A1-1. VGA DB15

Pin Number	Standard VGA	DDC1	DDC2B
1	Analog RED	Analog RED	Analog RED
2	Analog GREEN	Analog GREEN	Analog GREEN
3	Analog BLUE	Analog BLUE	Analog BLUE
4	Monitor ID 2	Monitor ID 2	Monitor ID 2
5	n/c	DDC Return	DDC Return
6	Analog RED Return	Analog RED Return	Analog RED Return
7	Analog GREEN Return	Analog GREEN Return	Analog GREEN Return
8	Analog BLUE Return	Analog BLUE Return	Analog BLUE Return
9	n/c	V_{CC} supply (optional)	V_{CC} supply (optional)
10	Digital Ground	Digital Ground	Digital Ground
11	Monitor ID 0	Monitor ID 0	Monitor ID 0
12	Monitor ID 1	Data from Display	Data: SDA
13	HSYNC	HSYNC	HSYNC
14	VSYNC	VSYNC (VCLK)	VSYNC
15	n/c	n/c	Clock: SCL

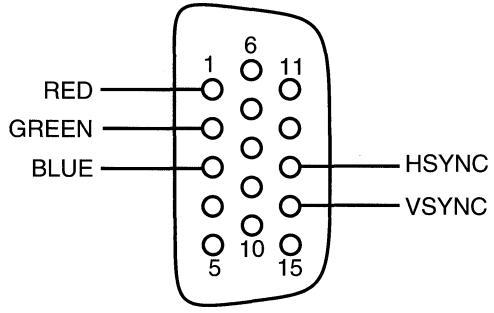
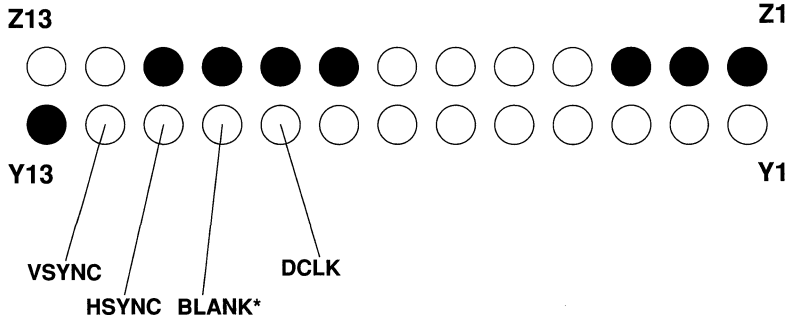


Table A1-2. VESA® Pass-through Connector

Number	Z	Y
1	Ground	P[0]
2	Ground	P[1]
3	Ground	P[2]
4	EVIDEO*	P[3]
5	ESYNC*	P[4]
6	EDCLK*	P[5]
7	+5 V[a]	P[6]
8	Ground	P[7]
9	Ground	DCLK
10	Ground	BLANK*
11	Ground	HSYNC
12	MCLK[a]	VSYNC
13	OVRW*[a]	Ground

a. These connections are assigned by Cirrus Logic for compatibility with VAFC.



View from Component Side

Table A1-3. VESA® Advanced Feature Connector Pinout

Pin	Name	Pin	Name
1	RSRV0	41	GND
2	RSRV1	42	GND
3	GENCLK	43	GND
4	OFFSET0	44	GND
5	OFFSET1	45	GND
6	FSTAT	46	GND
7	VRDY	47	GND
8	GRDY	48	GND
9	BLANK	49	GND
10	VSYNC	50	GND
11	HSYNC	51	GND
12	EGEN*	52	GND
13	VCLK	53	GND
14	RSRV2	54	GND
15	DCLK	55	GND
16	EVIDEO*	56	GND
17	P0	57	P1
18	GND	58	P2
19	P3	59	GND
20	P4	60	P5
21	GND	61	P6
22	P7	62	GND
23	P8	63	P9
24	GND	64	P10
25	P11	65	GND
26	P12	66	P13
27	GND	67	P14
28	P15	68	GND
29	P16	69	P17
30	GND	70	P18
31	P19	71	GND
32	P20	72	P21
33	GND	73	P22
34	P23	74	GND
35	P24	75	P25
36	GND	76	P26
37	P27	77	GND
38	P28	78	P29
39	GND	79	P30
40	P31	80	GND

Table A1-4. ISA Bus (CL-GD5434 Only)

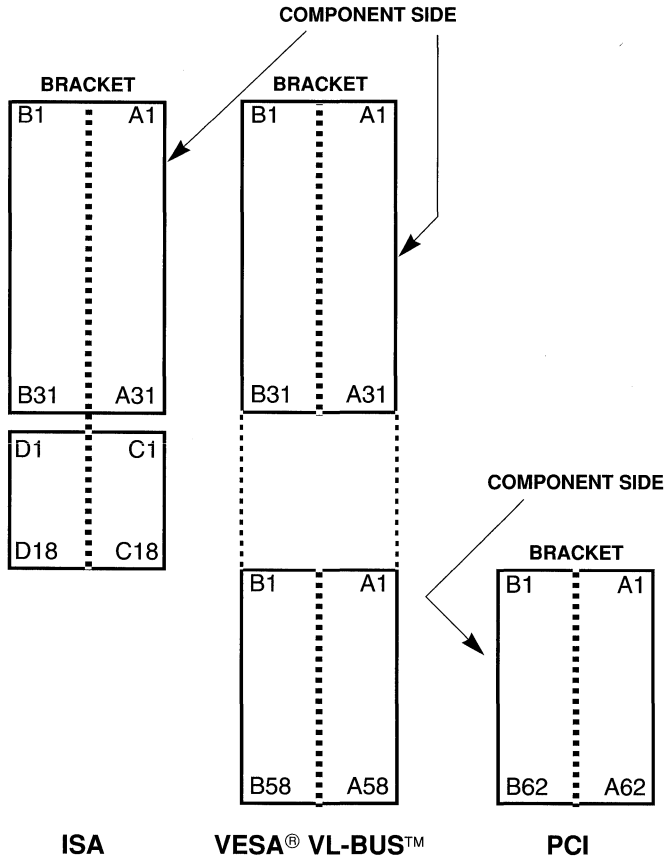
Pin	Component Side A	Solder Side B	Component Side C	Solder Side D
1	IOCHCHK*	Ground	SBHE*	MCS16*
2	SD7	RESET	LA23	IOCS16*
3	SD6	+5 V	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	–5V	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	–12 V	LA18	IRQ14
8	SD1	0WS*	LA17	DACK0*
9	SD0	+12 V	MEMR*	DRQ0
10	IOCHRDY	Ground	MEMW*	DACK5*
11	AEN	SMEMW*	SD8	DRQ5*
12	SA19	SMEMR*	SD9	DACK6*
13	SA18	IOW*	SD10	DRQ6
14	SA17	IOR*	SD11	DACK7*
15	SA16	DACK3*	SD12	DRQ7
16	SA15	DRQ3	SD13	+5 V
17	SA14	DACK1*	SD14	MASTER*
18	SA13	DRQ1	SD15	Ground
19	SA12	REFRESH*		
20	SA11	CLK		
21	SA10	IRQ7		
22	SA9	IRQ6		
23	SA8	IRQ5		
24	SA7	IRQ4		
25	SA6	IRQ3		
26	SA5	DACK2*		
27	SA4	T/C		
28	SA3	BALE		
29	SA2	+5 V		
30	SA1	OSC		
31	SA0	Ground		

Table A1-5. VESA® VL-Bus™

Pin	Solder Side 'B'	Component Side 'A'	Pin	Solder Side 'B'	Component Side 'A'
1	DAT00	DAT01	30	ADR17	ADR16
2	DAT02	DAT03	31	ADR15	ADR14
3	DAT04	GND	32	V_{CC}	ADR12
4	DAT06	DAT05	33	ADR13	ADR10
5	DAT08	DAT07	34	ADR11	ADR08
6	GND	DAT09	35	ADR09	GND
7	DAT10	DAT11	36	ADR07	ADR06
8	DAT12	DAT13	37	ADR05	ADR04
9	V_{CC}	DAT15	38	GND	WBACK# (not used)
10	DAT14	GND	39	ADR03	BE0#
11	DAT16	DAT17	40	ADR02	V_{CC}
12	DAT18	V_{CC}	41	n/c	BE1#
13	DAT20	DAT19	42	RESET# (not used)	BE2#
14	GND	DAT21	43	D/C# (not used)	GND
15	DAT22	DAT23	44	M/IO#	BE3#
16	DAT24	DAT25	45	W/R#	ADS#
17	DAT26	GND	46	Key	Key
18	DAT28	DAT27	47	Key	Key
19	DAT30	DAT29	48	RDYRTN#	LRDY#
20	V_{CC}	DAT31	49	GND	LDEV<X>#
21	ADR31	ADR30	50	IRQ9 (not used)	LREQ<X># (not used)
22	GND	ADR28	51	BRDY# (not used)	GND
23	ADR29	ADR26	52	BLAST# (not used)	LGNT<X>#
24	ADR27	GND	53	ID0 (not used)	V_{CC}
25	ADR25	ADR24	54	ID1 (not used)	ID2 (not used)
26	ADR23	ADR22	55	GND	ID3 (not used)
27	ADR21	V_{CC}	56	LCLK	ID4 (not used)
28	ADR19	ADR20	57	V_{CC}	LKEN# (not used)
29	GND	ADR18	58	LBS16#	LEADS# (not used)

Table A1-6. PCI Bus

Pin	Side B	Side A	Pin	Side B	Side A
1	–12V (not used)	TRKST# (not used)	32	AD[17]	AD[16]
2	TCLK (not used)	+12 V (not used)	33	C/BE[2]#	+3.3 V (not used)
3	Ground	TMS (not used)	34	Ground	FRAME#
4	TDO	TDI (not used)	35	IRDY#	Ground
5	+5 V	+5 V	36	+3.3 V (not used)	TRDY#
6	+5 V	INTA#	37	DEVSEL#	Ground
7	INTB# (not used)	INTC# (not used)	38	Ground	STOP#
8	INTD# (not used)	+5 V	39	LOCK#	+3.3 V (not used)
9	PRSNT1#	Reserved	40	PERR# (not used)	SDONE (not used)
10	Reserved	+5 V (I/O)	41	+3.3 V (not used)	SBO# (not used)
11	PRSNT2#	Reserved	42	SERR# (not used)	Ground
12	Ground	Ground	43	+3.3 V (not used)	PAR
13	Ground	Ground	44	C/BE[1]#	AD[15]
14	Reserved	Reserved	45	AD[14]	+3.3 V (not used)
15	Ground	RST#	46	Ground	AD[13]
16	CLK	+5 V (I/O)	47	AD[12]	AD[11]
17	Ground	GNT# (not used)	48	AD[10]	Ground
18	REQ# (not used)	Ground	49	Ground	AD[09]
19	+5 V (I/O)	Reserved	50	(Connector key)	(Connector key)
20	AD[31]	AD[30]	51	(Connector key)	(Connector key)
21	AD[29]	+3.3 V (not used)	52	AD[08]	C/BE[0]#
22	Ground	AD[28]	53	AD[07]	+3.3V (not used)
23	AD[27]	AD[26]	54	+3.3 V (not used)	AD[06]
24	AD[25]	Ground	55	AD[05]	AD[04]
25	+3.3 V (not used)	AD[24]	56	AD[03]	Ground
26	C/BE[3]#	IDSEL	57	Ground	AD[02]
27	AD[23]	+3.3 V (not used)	58	AD[01]	AD[00]
26	Ground	AD[22]	59	+5 V (I/O)	+5 V (I/O)
29	AD[21]	AD[20]	60	ACK64# (not used)	REQ64# (not used)
30	AD[19]	Ground	61	+5 V	+5 V
31	+3.3 V (not used)	AD[18]	62	+5 V	+5 V



Appendix B1

ISA Bus Schematics

ISA BUS SCHEMATICS

1. INTRODUCTION

This board design is for the CL-GD5434 only. No other CL-GD543X/'4X product has an ISA bus configuration.

The schematic was captured with OrCAD® SDT. This schematic, and associated Gerber files, are available to Cirrus Logic customers. Board design notes are included.

2. ISA-BUS INTERFACE

2.1 Bus Connections

Most bus interface pins on the CL-GD543X/'4X are connected directly to pins on the bus. The following table enumerates pins connected directly to the RESET pin.

Table B1-1. Bus Interface Connections

Pin(s)	Note
RESET	Note Inverter
INTR	Jumper
ZWS*	Jumper
REFRESH*	–
MEMW*/MEMR*	–
IOW*/IOR*	–
BALE	–
MSC16*/IOCS16*	–
SD[15:0]	–
SA[16:0]	–
LA[17:23]	–
BOSC	Note Filter

2.2 VGA BIOS

The VGA BIOS is contained in a single piece of 27C256 (32 Kbytes). The address is taken directly from SA[14:0]. The data is buffered in a single piece of 74ALS244, which is enabled with EROM* directly from the CL-GD5434.

3. DISPLAY MEMORY INTERFACE

3.1 Memory Configurations

The display memory is made up of one to four pieces of 256K × 16 dual-CAS* DRAMs. Table B1-2 indicates memory configurations that are available with this design.

Table B1-2. Display Memory Configurations

Capacity	Configuration
512 Kbyte	n/a
1 Mbyte	Devices one, two
2 Mbyte	Devices one–four
4 Mbyte	n/a

The RAS* inputs on the second Mbyte must be driven with the RAS1* outputs of the CL-GD5434. The configuration that drives these inputs with RAS0* will never be utilized.

3.2 Damping Resistors

The MA lines and all memory control lines from the CL-GD543X/'4X into the display memory array have series resistors to damp reflections from the array and control edge rates. These resistors are shown as 22 Ω. The value may be adjusted based on the number of devices actually populated. Ideally, these lines should be nearly critically damped.

4. MONITOR INTERFACE

4.1 RGB Lines

The RGB lines are terminated in 75 Ω to AGND. This provides half of the nominal 37.5-Ω DC load; the other half is in the monitor.

π filters on each RGB line control edge rates and reduce RFI (radio frequency interference) to an acceptable level. The component values in these filters represent a trade-off. For good crisp video, especially at higher frequencies, the cutoff frequency should be as high as possible. On the other hand, for reduced emissions the cutoff frequency should be fairly low. The values in the schematic represent our best engineering advice as of the time the schematic was captured.

The resistors are located as close as possible to the device. The π filters are located very close to the DB-15 connector. The traces between the device and the π filters are direct with a minimum of vias and no sharp corners. These traces must be designed with a characteristic impedance as close as possible to 75 Ω. The edge rates, especially before the π filter, are fast enough that a trace as short as a few inches will begin to behave as a transmission line.

4.2 Sync Lines

HSYNC and VSYNC are isolated with π RC filters of 33 Ω and 220 pF. The filter outputs connect directly to the DB-15 and VESA connectors.

4.3 Monitor ID

This design supports only heritage monitor ID. The four monitor ID pins can be sensed through the Pixel bus.

5. VESA® CONNECTOR

5.1 Standard VESA® Interface

The VESA connector pins are tied to the corresponding pins on the CL-GD543X/'4X either directly or through an appropriate resistor. Table B1-3 shows the pins on the VESA connector.

Table B1-3. VESA® Connector Pinouts

Pin	Function	Note	Pin	Function	Note
Z1	GND		Y1	P0	
Z2	GND		Y2	P1	
Z3	GND		Y3	P2	
Z4	EVIDEO*	1 KΩ	Y4	P3	
Z5	ESYNC*	1 KΩ	Y5	P4	
Z6	EDCLK*		Y6	P5	
Z7	n/c		Y7	P6	
Z8	GND		Y8	P7	
Z9	GND		Y9	DCLK	
Z10	GND		Y10	BLANK*	
Z11	GND		Y11	HYSNC	Filtered
Z12	MCLK	a	Y12	VSYNC	Filtered
Z13	OVRW*	b	Y13	GND	

a. Z12 is a 'no connect' in the VESA specification. Cirrus Logic uses this pin for a video clock.

b. Z13 is a 'no connect' in the VESA specification. Cirrus Logic uses this pin for OVRW*.

6. POWER DISTRIBUTION AND CONDITIONING

By far, the most common reason for unsatisfactory performance of a video subsystem is the power distribution and conditioning not properly directed. Dedicated power and ground planes are strongly recommended for boards based on all CL-GD543X/'4X products.

6.1 Dedicated Ground Plane

A dedicated ground plane minimizes differential ground offsets and nearly approximates the ideal notion of 'ground'. Additionally, a ground plane is necessary to predict and control the characteristic impedance of traces that must be treated as transmission lines.

The ground plane has cuts to partially isolate the critical analog VSS sections from the relatively noisy digital VSS associated with the DRAM array and the bus interface. On the schematic diagram, there are two ground nodes. The digital ground is designated with a standard ground symbol. The isolated grounds are designated as MCLKVSS, VCLKVSS, and DACVSS.

6.2 Dedicated Power Plane

A dedicated power plane allows low-impedance distribution of VCC, minimizing noise and coupling. A dedicated power plane also behaves as an AC ground, making it possible to predict and control the characteristic impedance of traces above it.

The power plane has regions that are completely isolated from the digital portion of the plane. The power plane beneath the device is isolated and connected to the main section of the power plane with two 1-Ω resistors in parallel. This isolated area is designated as VDD on the schematic diagram. Two areas for the synthesizer power conditioning are further isolated with 33-Ω resistors.

6.3 Power Bypassing

Bypass capacitors are used to minimize power sags caused by current spikes and reduce power distribution impedance. Bulk bypassing is present where power comes onto the board, around the DRAM array, and near the EPROM.

High-frequency bypass capacitors are distributed as needed on the board. Every digital VCC pin on the device has a bypass capacitor located as close as possible to the pin. Each pin is connected to its capacitor – and the isolated VDD section of the power plane – with a short, thick, direct lead. The ground connection of each capacitor is made with a via directly to the ground plane. Each DRAM has a high frequency bypass capacitor located very close to pin 20 (the VCC pin). The VCC pin is also connected with a short, thick, direct lead. The ground connection of the capacitor is made with a via directly to the ground plane.

6.4 Analog Power Conditioning

Two areas on the power plane are further isolated within the VDD section. One is designated MCLKVDD (AVDD4), the other is designated VCLKVDD (AVDD1). Each is connected to VDD through a π RC filter consisting of a 33-Ω resistor and a 10-μF capacitor in parallel with a 0.1-μF capacitor. Each of the capacitors in each filter is returned to its respective cutout of

AGND. Devices with integrated synthesizer filters require the same synthesizer power conditioning.

Power for the DAC (AVDD[3:2]) is taken directly from the VDD section of the power plane. It is bypassed with a 10-µF capacitor in parallel with a 0.1-µF capacitor. Each capacitor is returned to the DAC cutout of the ground plane. Devices with an integrated current reference require the same DAC power filtering.

6.5 Configuration Resistors

The configuration resistors in Table 4 are shown on the schematic. Some are optional.

Table B1-4. Configuration Resistors

MD Pin	CF-	Use (if Installed)
60	12	Disable internal DAC
58	10	Multiple-CAS DRAMs
57	9	Extended RAS timing
56	8	50 MHz MCLK default
51	3	3C3 Sleep Address

6.6 Synthesizer Reference

The 14.3 MHz reference required by the dual-frequency synthesizer is supplied by a crystal oscillator or from the BOSC pin on the ISA bus. For specification in typical ISA motherboards, the oscillator should be used. If the boards are being built for specific motherboards on which the 14.3 MHz is known to be very stable and very clean, the BOSC pin may be usable.

6.7 Synthesizer Filters

Each of the two synthesizer filter pins is connected to a π RC filter. The input capacitor of 0.1 µF is connected in parallel with a section comprising a 75-Ω resistor in series with a nominal 2.2-µF capacitor. Each section of the filter is returned to the respective AGND cutout.

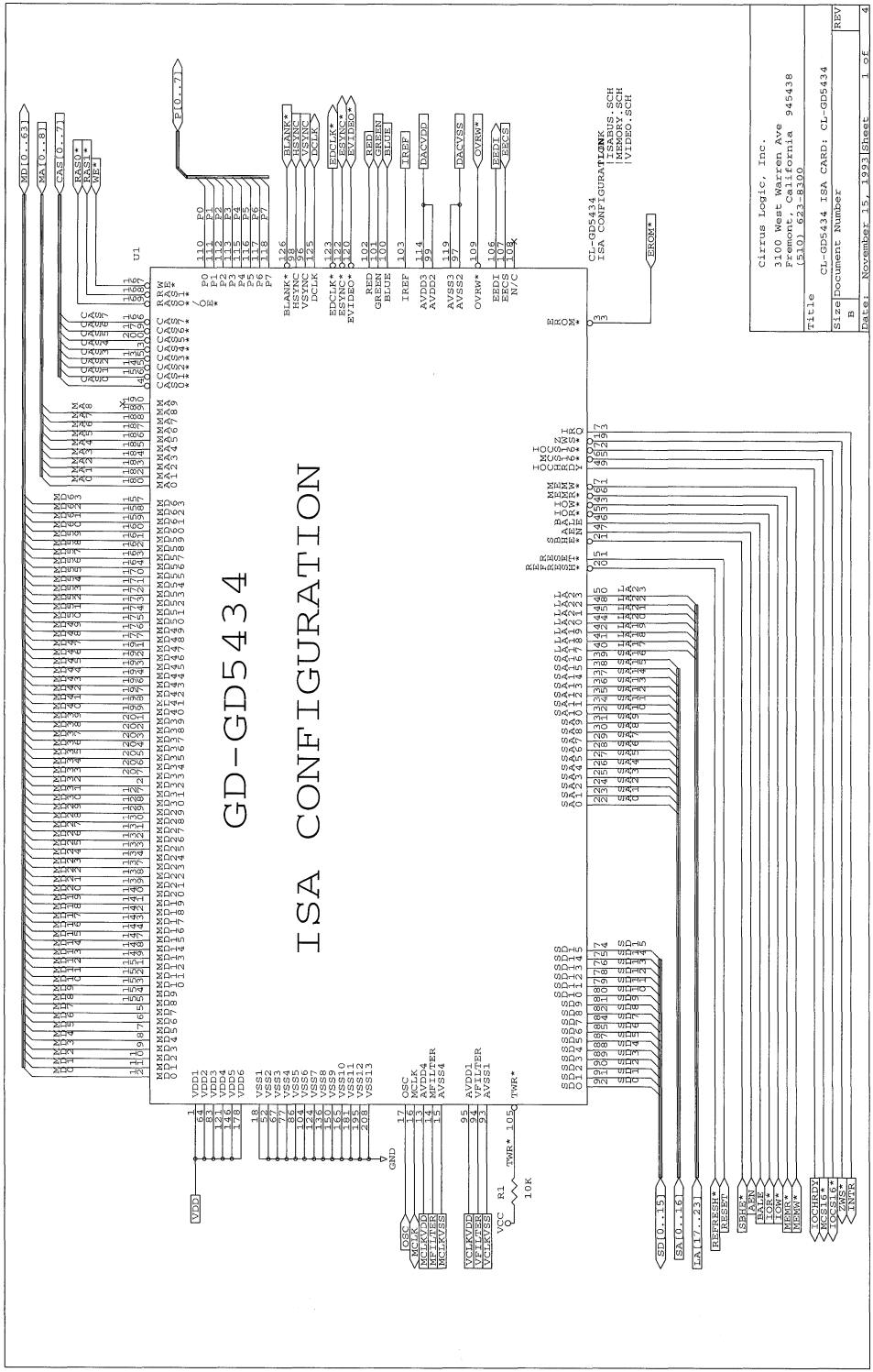
6.8 Current Reference

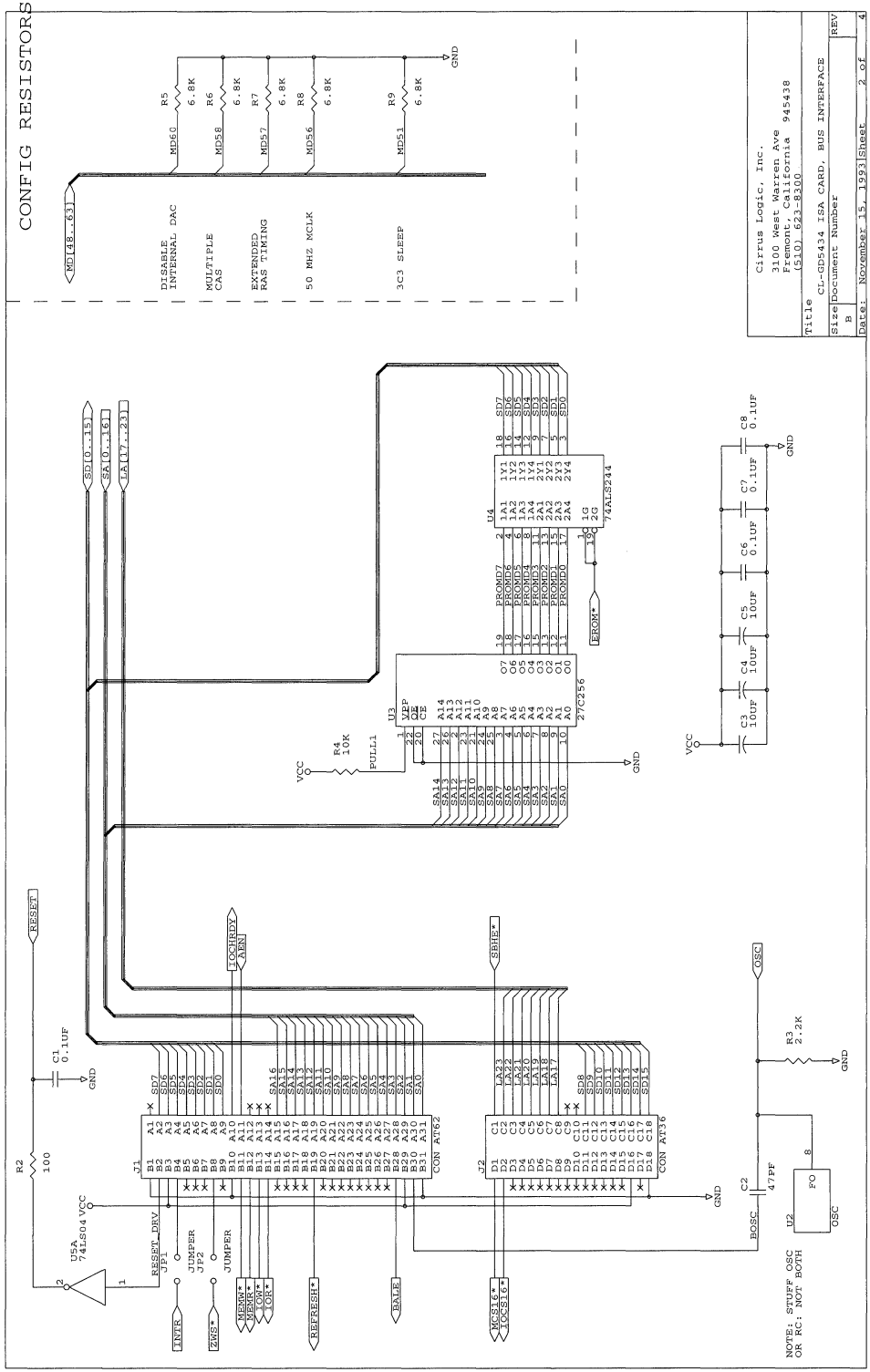
The current reference sets the full-scale current output of the DACs. The circuit based on the LM344 has adequate headroom to allow for minimum VCC conditions for all devices. The two capacitors between the IREF pin and VDD are optional. The decision whether to populate them and what the exact value is are made at the time the design is evaluated.

CL-GD5434 ISA CARD: CL-GD5434 Revised: November 15, 1993
Revision:

Bill Of Materials November 15, 1993 14:43:52 Page 1

Item	Quantity	Reference	Part
1	1	CR1	LM334,,
2	25	C1,C6,C7,C8,C9,C10,C11, C12,C13,C14,C15,C16,C18, C20,C22,C24,C33,C34,C35, C36,C37,C38,C39,C40,C44	0.1UF,,
3	1	C2	47PF,,
4	7	C3,C4,C5,C17,C21,C41,C43	10UF,,
5	3	C19,C23,C45	2.2UF,,
6	6	C25,C26,C27,C28,C29,C30	10PF,,
7	2	C31,C32	220PF,,
8	1	C42	100PF,,
9	1	D1	DIODE,,
10	3	FB1,FB2,FB3	BEAD,,
11	5	JP1,JP2,JP4,JP5,JP6	JUMPER,100MIL,
12	1	JP3	VESA HEADER,13X2X100MIL,
13	1	J1	CON AT62,EDGE CONNECTOR,
14	1	J2	CON AT36,,
15	1	P1	15PIN,DB15_3ROW,
16	2	R1,R4	10K,,
17	1	R2	100,,
18	1	R3	2.2K,,
19	13	R5,R6,R7,R8,R9,R32,R33, R34,R35,R36,R37,R38,R39	6.8K,,
20	14	R10,R11,R12,R13,R14,R15, R16,R17,R18,R19,R20,R43, R45,R46	22,,
21	4	R21,R23,R40,R41	33,,
22	2	R22,R24	75,,
23	4	R25,R26,R27,R44	150,,
24	3	R30,R31,R42	0,,
25	1	U1	CL-GD5434,ISA CONFIGURATION,
26	1	U2	OSC,,
27	1	U3	27C256,,
28	1	U4	74ALS244,,
29	1	U5	74LS04,,
30	4	U6,U7,U8,U9	256KX16,,
31	1	U10	93C46,,




CONFIG RESISTORS
MD[48..63]
DISABLE INTERNAL DAC
MULTIPLE CAS
EXTENDED RAS TIMING
50 MHZ MCLK
3C3 SLEEP
R5 6.8K
R6 6.8K
R7 6.8K
R8 6.8K
R9 6.8K
GND
Cirrus Logic, Inc.
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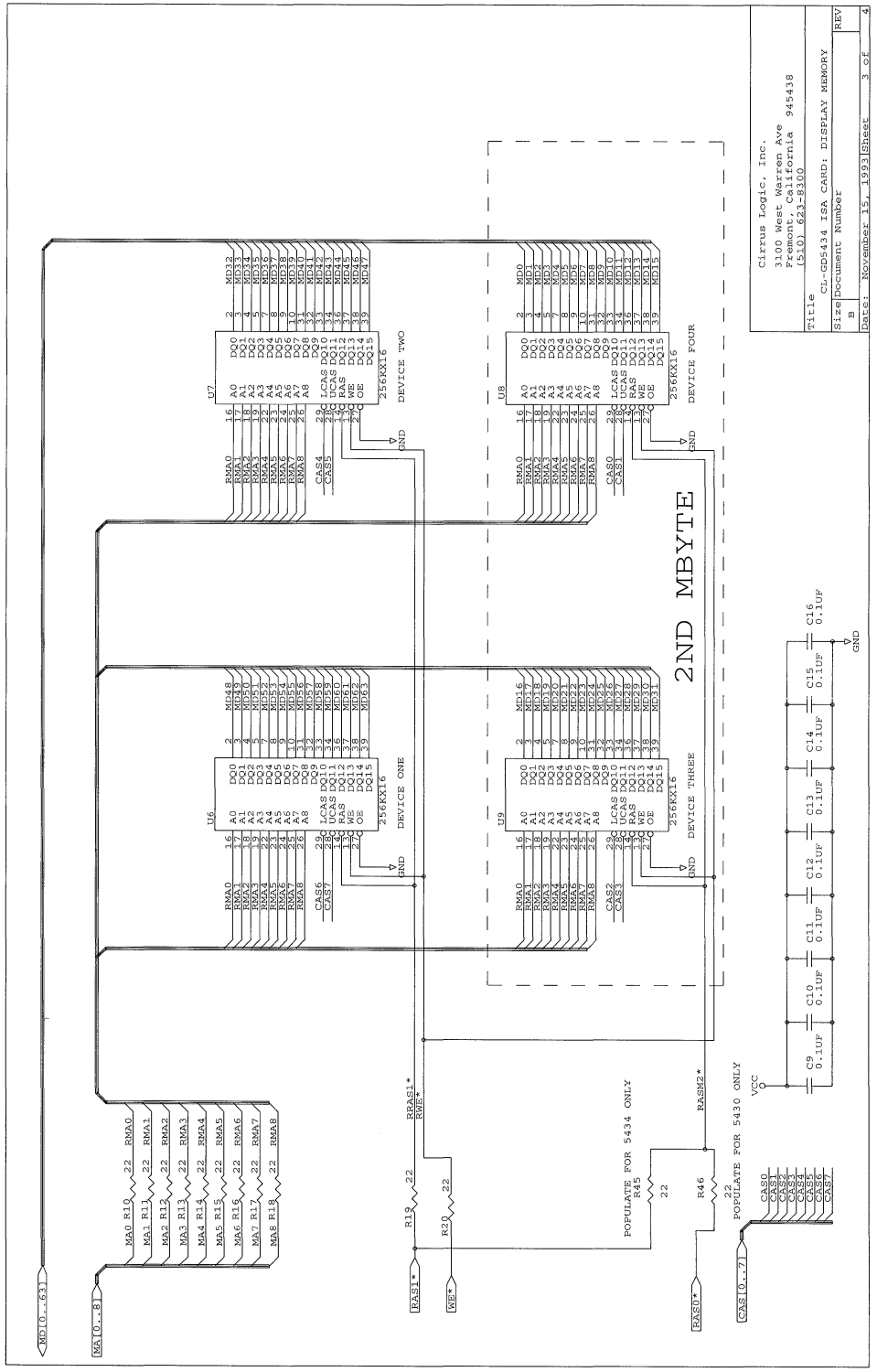
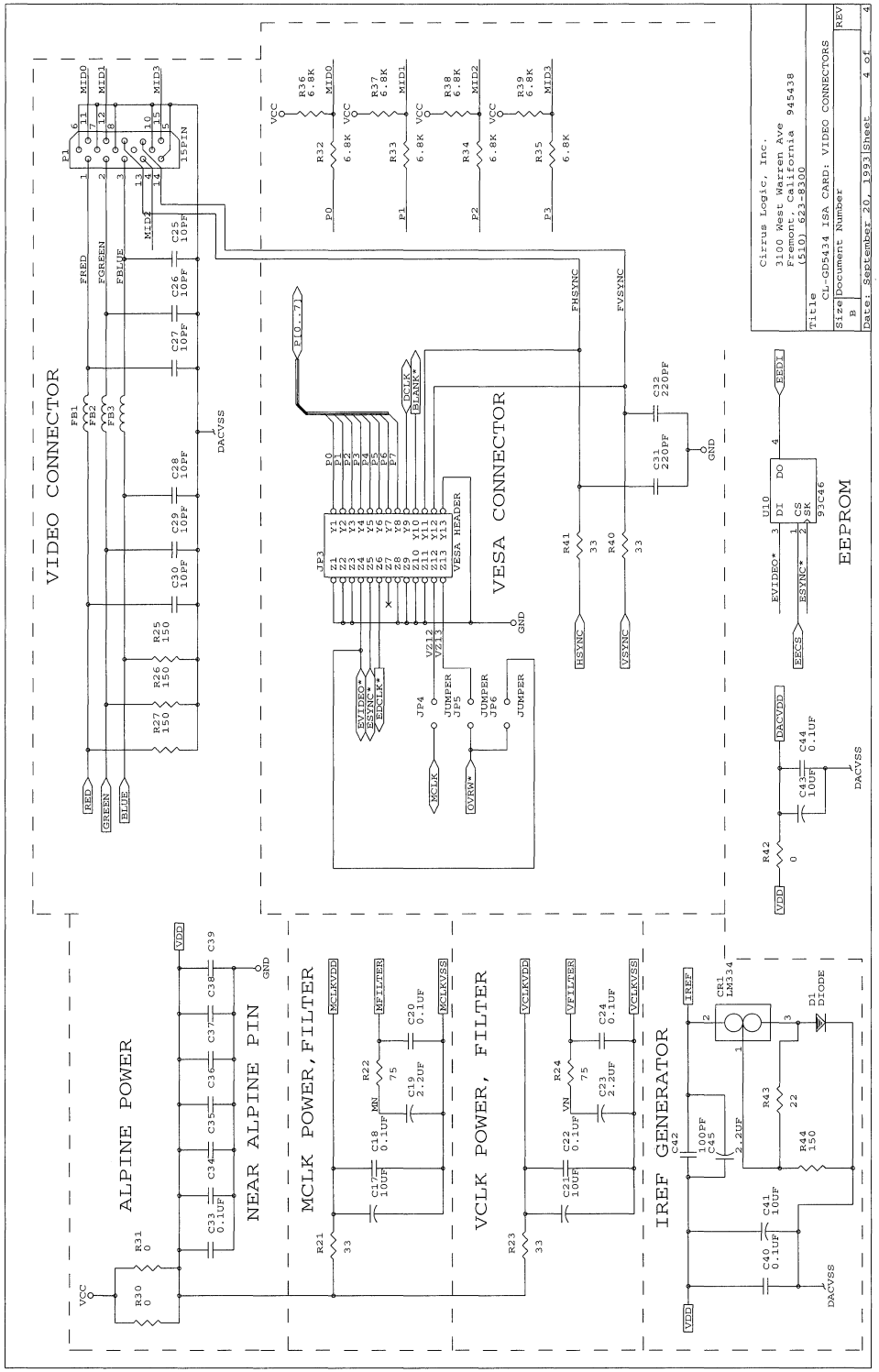
Fremont, California 94538
(510) 623-8300
Title
CL-GD5434 ISA CARD, BUS INTERFACE
Size B
Document Number
REV
Date: November 15, 1993 Sheet 2 of 4
SD[0..15]
SA[0..16]
LA[17..23]
U3 27C256
U4 74ALS244
R4 10K
PULL1
VCC
EROM*
C1 0.1UF
C2 47PF
C3 10UF
C4 10UF
C5 10UF
C6 0.1UF
C7 0.1UF
C8 0.1UF
R2 100
R3 2.2K
U5A 74LS04
U2 OSC
J1 CON AT62
J2 CON AT36
RESET
RESET_DRV
JUMPER
LOCHRDY
SBHE*
OSC
BALE
REFRESH*
MEMW*
MEMR*
IOW*
IOR*
INTR
ZWS*
MCS16*
IOCS16*
NOTE: STUFF OSC OR RC, NOT BOTH




VIDEO CONNECTOR
VESA CONNECTOR
EEPROM
ALPINE POWER
NEAR ALPINE PIN
MCLK POWER, FILTER
VCLK POWER, FILTER
IREF GENERATOR
Cirrus Logic, Inc.
3100 West Warren Ave
Fremont, California 94538
(510) 623-8300
Title
CL-GD5434 ISA CARD: VIDEO CONNECTORS
Size B
Document Number
REV
Date: September 20, 1993 Sheet 4 of 4

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Appendix B2

PCI Bus Schematics

PCI BUS SCHEMATICS

1. INTRODUCTION

This appendix covers the schematics of the CL-GD543X/'4X reference adapter board design for the PCI bus. This board can be populated with any CL-GD543X/'4X device. The board can also be populated with 512 Kbytes to 2 Mbytes of display memory.

The schematic was captured with OrCAD® SDT. This schematic and the associated Gerber files are available to Cirrus Logic customers. Board design notes are included.

2. PCI BUS INTERFACE

2.1 Bus Connections

The CL-GD543X/'4X is designed for a glueless interface to the PCI bus. Pins on the CL-GD543X/'4X are connected directly to similarly named pins on the PCI bus. This is summarized in the following table.

Table B2-1. PCI Bus Connections

Pin Names	Function	Note
AD[31:0]	Address/Data bus	
PAR	Parity	
STOP#	Control	
C/BE[3:0]#	Control	
FRAME#	Control	
IRDY#	Control	
TRDY#	Control	
IDSEL	Control	
CLK	Clock	
RST#	Control	
DEVSEL#	Control	
INTR#	Interrupt Request	Connected with jumper
PRSNT#2	System Control	Grounded
TDI/TDO	System Control	Tied together

The CL-GD543X/'4X is placed within an inch of the PCI connector and is approximately centered on the connector. The pin assignments on the CL-GD543X/'4X are carefully optimized to allow short and direct connections between the bus pins and the CL-GD543X/'4X pins. The CLK trace is laid out first and made wider than others.

2.2 INTR# Pin

The INTR# pin is connected from CL-GD543X/'4X with a jumper. For the CL-GD5430 and some versions of the CL-GD5434, PCI3C[8] will always be '1'. The jumper should be installed for applications that require it.

For the CL-GD5436, CL-GD5440, and some versions of the CL-GD5434, PCI3C[8] can be configured in the chip. If a pull-down resistor is installed on MD[62], PCI3C[8] will be '1' and the jumper may be installed. If a pull-down resistor is not installed on MD[62], PCI3C[8] will be '0' and the jumper must not be installed. This particular board layout does not support the pulldown on MD62; the jumper should not be installed.

2.3 VGA BIOS

The CL-GD543X/'4X is designed to comply with the PCI requirement that a single load appear on each signal. This requirement precludes connecting the BIOS EPROM directly to the bus. Rather, the EPROM is connected only to the CL-GD543X/'4X. The EPROM address inputs are driven with dedicated pins on the CL-GD543X/'4X (BIOSA[14:0]). The EPROM data pins are connected to MD[7:0]; these pins are multiplexed. The EPROM enables are both driven with the CL-GD543X/'4X EROM*.

A 27C256 EPROM contains the 32K VGA BIOS. The address pins are connected directly pin-to-pin; no address bit swapping is used.

3. DISPLAY MEMORY INTERFACE

3.1 Memory Configurations

The display memory is made up of one to four pieces of 256K × 16 dual-CAS* DRAMs. Table B2-2 indicates the memory configurations available with this design.

Table B2-2. Display Memory Configurations

Capacity	Devices	CL-GD5430/'40	CL-GD5434/'36
512 Kbyte	One	✔	
1 Mbyte	One, Two	✔	✔
2 Mbyte	One, Two, Three, Four	✔	✔

The RAS* inputs on the second Mbyte can be driven either from the RAS1* or RAS0* outputs of the CL-GD543X/'4X. RAS0* must be used for a design populated with the CL-GD5430/'40. RAS1* must be used for a design populated with the CL-GD5434/'36.

3.2 Damping Resistors

The MA lines and all memory control lines from the CL-GD543X/'4X into the display memory array have series resistors to damp reflections from the array and to control edge rates. These resistors are shown as 10 Ω. The value may be adjusted based on the number of devices actually populated. Ideally the lines should be nearly critically damped.

4. MONITOR INTERFACE

4.1 RGB Lines

The RGB lines are terminated in 75 Ω to AGND. This provides half of the nominal 37.5-Ω DC load; the other half is in the monitor.

π filters on each RGB line control edge rates and reduce RFI (radio frequency interference) to an acceptable level. The component values in these filters represent a trade-off. For life-like, high-resolution video, especially at higher frequencies, the cutoff frequency should be as high as possible. On the other hand, for reduced emissions the cutoff frequency should be fairly low.

The resistors are located as close as possible to the CL-GD543X/'4X. The filters are located very close to the DB-15 connector. The traces between the CL-GD543X/'4X and the π filters are direct with an absolute minimum of vias and no sharp corners. These traces must be designed with a characteristic impedance as close as possible to 75 Ω. The edge rates, especially before the π filter, are fast enough that a trace as short as a few inches will begin to behave as a transmission line.

4.2 Sync Lines

HSYNC and VSYNC are isolated with π RC filters of 33 Ω and 220 pF. The filter outputs connect directly to the DB-15 and VESA connectors.

4.3 Monitor ID

The BIOS requires information regarding the capability of the connected monitor so that it can program the appropriate refresh rates for the various video modes. In some cases, the monitor capability may be such that higher resolution modes cannot be programmed at all.

The CL-GD543X/'4X supports the DDC1 and DDC2B methods of monitor identification. Additionally, two methods each of DDC1 and DDC2B can be configured, depending on the production level of the CL-GD543X/'4X.

4.3.1 Legacy Monitors

When super VGA monitors were first available there was an attempt to standardize a method of specifying monitor capability that involved the unused pins on the DB-15 connector. These pins are called Monitor ID (MID[3:0]). Each of the four pins was to be pulled-up on the adapter card; the monitor would tie one or more of these pins to digital ground. The BIOS would sense these pins to determine the monitor capability. This attempt at standardization failed for a variety of reasons.

Cirrus Logic reference designs implemented a method of reading all four MID pins for some time; this is no longer supported, either in the board designs or in the BIOS. End users with monitors that are not DDC-compliant should use CLMODE or an equivalent utility to specify to the BIOS the monitor type.

4.3.2 DDC1 Support

DDC1 provides a unidirectional data channel from the monitor to the controller that continuously transmits EDID (Extended Display Identification) information. The EDID is transmitted from the monitor to the controller on MID[1] (DB15 pin 12). MID[1] is connected to Pixel bus bit P1 through a 6.8-KΩ series resistor or to the EEDI pin through a 1-KΩ resistor. Software is able to read P1 or the EEDI pin to determine what the monitor is transmitting.

4.3.3 DDC2B Support

DDC2B is a bidirectional data channel based on the I2C bus. The data clock is on MID[3] (DB15 pin 15) and the bidirectional data is on MID[1] (DB15 pin 12). The schematic diagram shows two implementations of DDC2B. Depending on the capabilities of the device being populated, one or the other should be populated.

DDC2B is an open collector protocol. The logic in the controller has to pull-up each of the two signals (MID[1] and MID[3]) and drive each signal low. In addition, the software has to be able to sense each line (MID[1] and MID[3]).

For boards populated with CL-GD543X/'4X devices without integrated DDC2B support, the components listed in the OLD DDC2B row of page ALP2M4 must be populated. ESYNC* and EVIDEO* drive MID[1] and MID[3], respectively, through the two open collector gates. To prevent the monitor from seeing activity on the lines when the EEPROM is being programmed, the gates are disabled when EECS is high. The pins can be sensed through Pixel bus lines P1 and P3.

For boards populated with CL-GD543X/'4X devices with integrated DDC2B, the components listed in the NEW DDC2B row of sheet 5 must be populated. EECS and EEDI drive MID[3] and MID[1], respectively. The same pins are used to sense the level on the two signals. Table B2-3 indicates the production level of devices that are planned to support integrated DDC2B.

Table B2-3. Integrated DDC2B Support

Product	Production Revision Level
CL-GD5434	Production Revision E
CL-GD5436	Production Revision A
CL-GD5440	Production Revision A

5. VESA® CONNECTOR

5.1 Standard VESA® Interface

The VESA connector pins are tied to the corresponding pins on the CL-GD543X/'4X either directly or through an appropriate resistor. Table B2-4 shows the pins on the VESA connector.

Table B2-4. VESA® Connector Pinouts

Pin	Function	Note	Pin	Function	Note
Z1	GND		Y1	P0	
Z2	GND		Y2	P1	
Z3	GND		Y3	P2	
Z4	EVIDEO*	1 KΩ	Y4	P3	
Z5	ESYNC*	1 KΩ	Y5	P4	
Z6	EDCLK*	1 KΩ	Y6	P5	
Z7	+5V or EEDI	a	Y7	P6	
Z8	GND		Y8	P7	
Z9	GND		Y9	DCLK	
Z10	GND		Y10	BLANK*	
Z11	GND		Y11	HYSNC	Filtered
Z12	MCLK	b	Y12	VSYNC	Filtered
Z13	OVRW* or EECS*	c	Y13	GND	

a. Z7 is a no connect in the VESA specification. Cirrus Logic uses this pin either for a VCC supply for a VAFC adapter card or as one pin of an I2C interface.

b. Z12 is no connect in the VESA specification. Cirrus Logic uses this pin for a video clock.

c. Z13 is a no connect in the VESA specification. Cirrus Logic uses this pin either for OVRW* or as one pin of an I2C interface.

5.2 16-Bit Interface (CL-GD5436)

The 16-bit pixel interface of the CL-GD5436 is not supported in this reference design.

5.3 I2C Interface

The I2C interface allows the host to communicate with devices using the standard TV tuner interface, such as the CL-PX4072. Z7 and Z13 on the VESA connector are used.

6. POWER DISTRIBUTION AND CONDITIONING

6.1 Introduction

By far the most common reason for unsatisfactory performance of a video subsystem is a failure on the part of the board designer to properly direct power distribution and conditioning. Dedicated power and ground planes are very strongly recommended for boards based on all CL-GD543X/'4X devices.

6.2 Dedicated Ground Plane

A dedicated ground plane minimizes differential ground offsets and more nearly approximates the ideal notion of 'ground'. Additionally, a ground plane is necessary to predict and control the characteristic impedance of those traces that must be treated as transmission lines.

The ground plane has cuts to partially isolate the critical analog VSS sections from the relatively noisy digital VSS associated with the DRAM array and the bus interface. These cuts may be studied in the Gerber plots. On the schematic diagram, there are five ground nodes. The digital ground (used by the DRAMs) is designated with a standard ground symbol. The three isolated grounds are designated AVSS, MCLKVSS, and VCLKVSS.

6.3 Dedicated Power Plane

A dedicated power plane allows low impedance distribution of VCC, minimizing noise and coupling. A dedicated power plane also behaves as an AC ground, making it possible to predict and control the characteristic impedance of traces above it.

The power plane has regions that are completely isolated from the digital portion of the plane. The power plane beneath the CL-GD543X/'4X is isolated, and is connected to the main section of the power plane with two 1-Ω resistors in parallel. This isolated area is designated VDD on the schematic diagram.

Two areas for the synthesizer power conditioning are further isolated. The power plane can be studied in the Gerber prints.

6.4 Power Bypassing

Bypass capacitors are used to minimize power sags caused by current spikes and to reduce the power distribution impedance. Bulk bypassing is present in the area where power comes onto the board, around the DRAM array, and near the EPROM.

High-frequency bypass capacitors are distributed as needed on the board. Every digital VCC pin on the CL-GD543X/'4X has a bypass capacitor located as close to the pin as possible. Each pin is connected to its capacitor – and the isolated VDD section of the power plane – with a short, thick, direct lead. The ground connection of each capacitor is made with a via directly to the ground plane. Each DRAM has a high frequency bypass capacitor located very close to pin 20 (the VCC pin). The VCC pin is connected with a short, thick, direct lead. The ground connection of the capacitor is made with a via directly to the ground plane.

6.5 Analog Power Conditioning

Two areas on the power plane are further isolated within the VDD section. One is designated MCLKVDD (AVDD4) and one is designated VCLKVDD (AVDD1). Each is connected to VDD through an RC filter consisting of a 33-Ω resistor and a 10-µF capacitor in parallel with a 0.1-µF capacitor. Each of the capacitors in each filter is returned to its respective cutout on the ground plane. Devices with integrated synthesizer filters require the same synthesizer power conditioning.

Power for the DAC (AVDD[3:2]) is taken from the VDD section of the power plane through a 0-Ω resistor. It is bypassed with a 10-µF capacitor in parallel with a 0.1-µF capacitor. Each capacitor is returned to the DAC cutout of the ground plane. Devices with integrated current reference require the same DAC power filtering.

6.6 Configuration Resistors

The configuration resistors in Table B2-5 are shown in the schematic. Some are optional.

Table B2-5. Configuration Resistors

MD Pin	CF-	Use (if Installed)	Note
MD58	CF10	Dual-CAS* DRAMs	–
MD57	CF9	Extended RAS* timing	–
MD56	CF8	50 MHz MCLK default	CL-GD5430/'34/'40
MD56	CF8	Enable byte swap	CL-GD5436 only
MD[48:47]	CF1, CF0	PCI bus	–

6.7 Synthesizer Reference

The 14.3 MHz reference required by the dual-frequency synthesizer is supplied by a crystal oscillator.

For devices that support integrated synthesizer filters, the crystal oscillator can be replaced with a crystal connected between the BOSC pin and the MFILTER pin. Each pin on the crystal is bypassed to ground with a 27-pF capacitor. The crystal and capacitors are located close to the pins and connected with short, direct leads.

6.8 Synthesizer Filters

Each of the two synthesizer filter pins is connected to an RC filter. A 0.1-µF input capacitor is connected in parallel with a section comprising a 75-Ω resistor in series with a nominal 2.2-µF capacitor. Each section of the filter is returned to the respective AGND cutout.

For devices that support integrated synthesizer filters, MFILTER is optionally connected to one side of a reference crystal, described in the section immediately preceding. VFILTER is optionally connected to a current setting resistor and a parallel capacitor for the integrated current reference, described in the section immediately following.

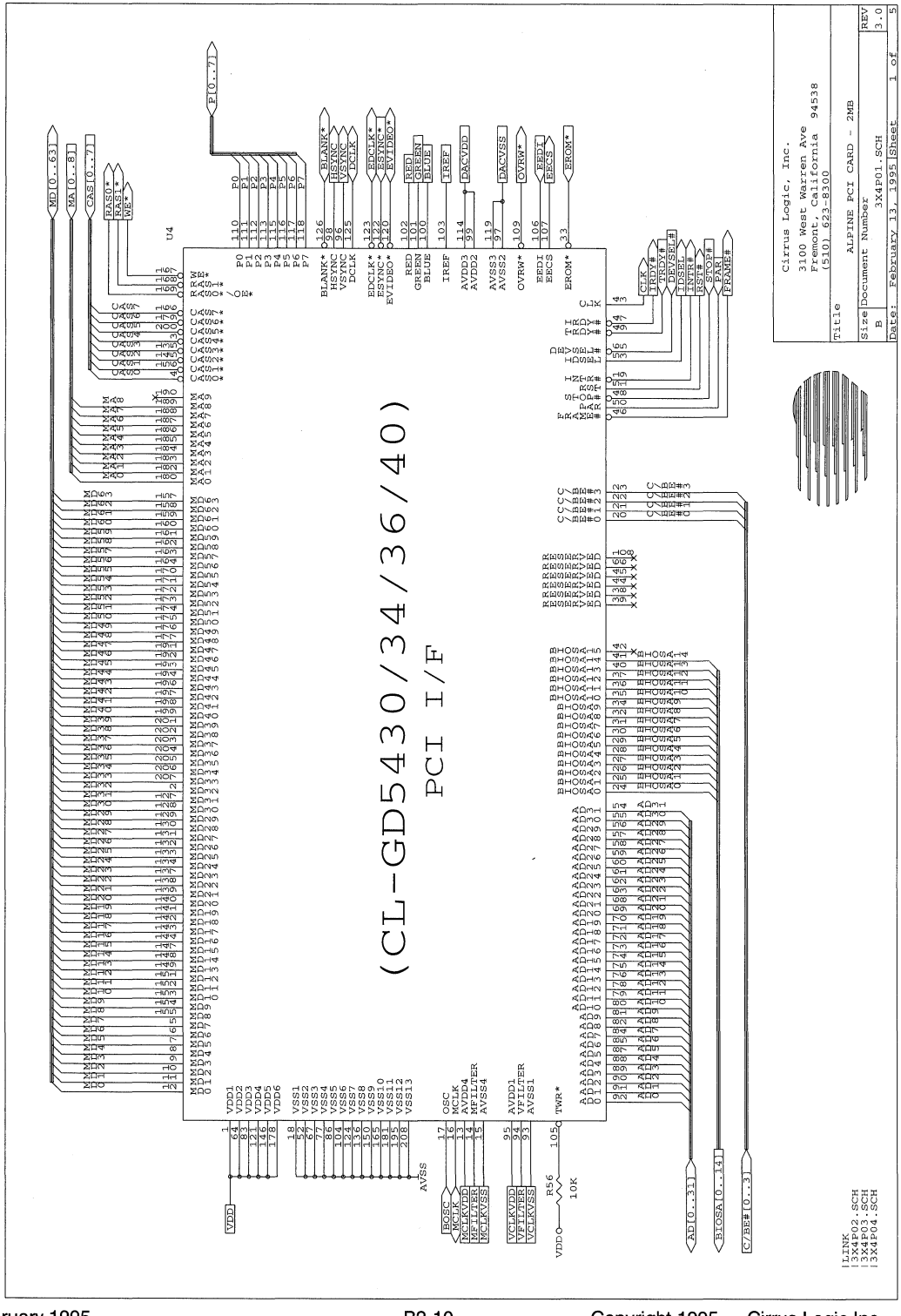
6.9 Current Reference

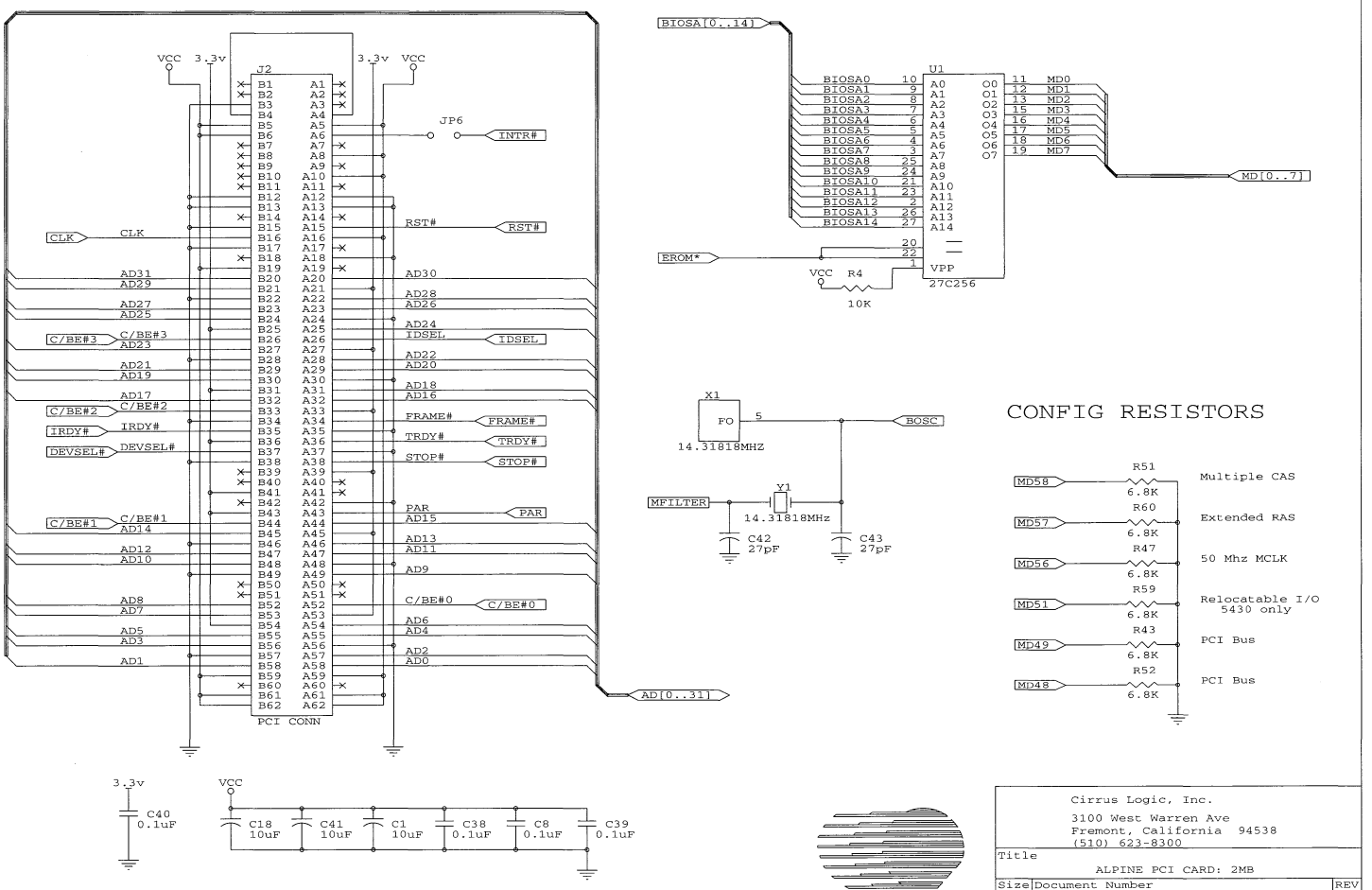
The current reference sets the full-scale current output of the DACs. The circuit based on the LM344 has adequate headroom to allow for minimum VCC conditions for all CL-GD543X/'4X devices. The two capacitors between the IREF pin and VDD are optional. The decisions of whether to populate them and the exact value are made at the time the design is evaluated.

For devices that support integrated current reference, IREF is connected to a capacitor to DACVDD. The pads used for the optional capacitors described in the paragraph above are used for this purpose. See the text on page ALP2M4.

Also for devices that support integrated current reference, VFILTER is connected to a current setting resistor in parallel with a 0.1-µF capacitors. See the text on page ALP2M4. The resistor value can be calculated with the following equation where *Load* is the DC load in ohms, and *VFullScale* is the desired full-scale voltage. The derivation of this equation is given in Appendix B8.

$$RSet = \frac{2.52V \bullet Load}{VFullScale}$$





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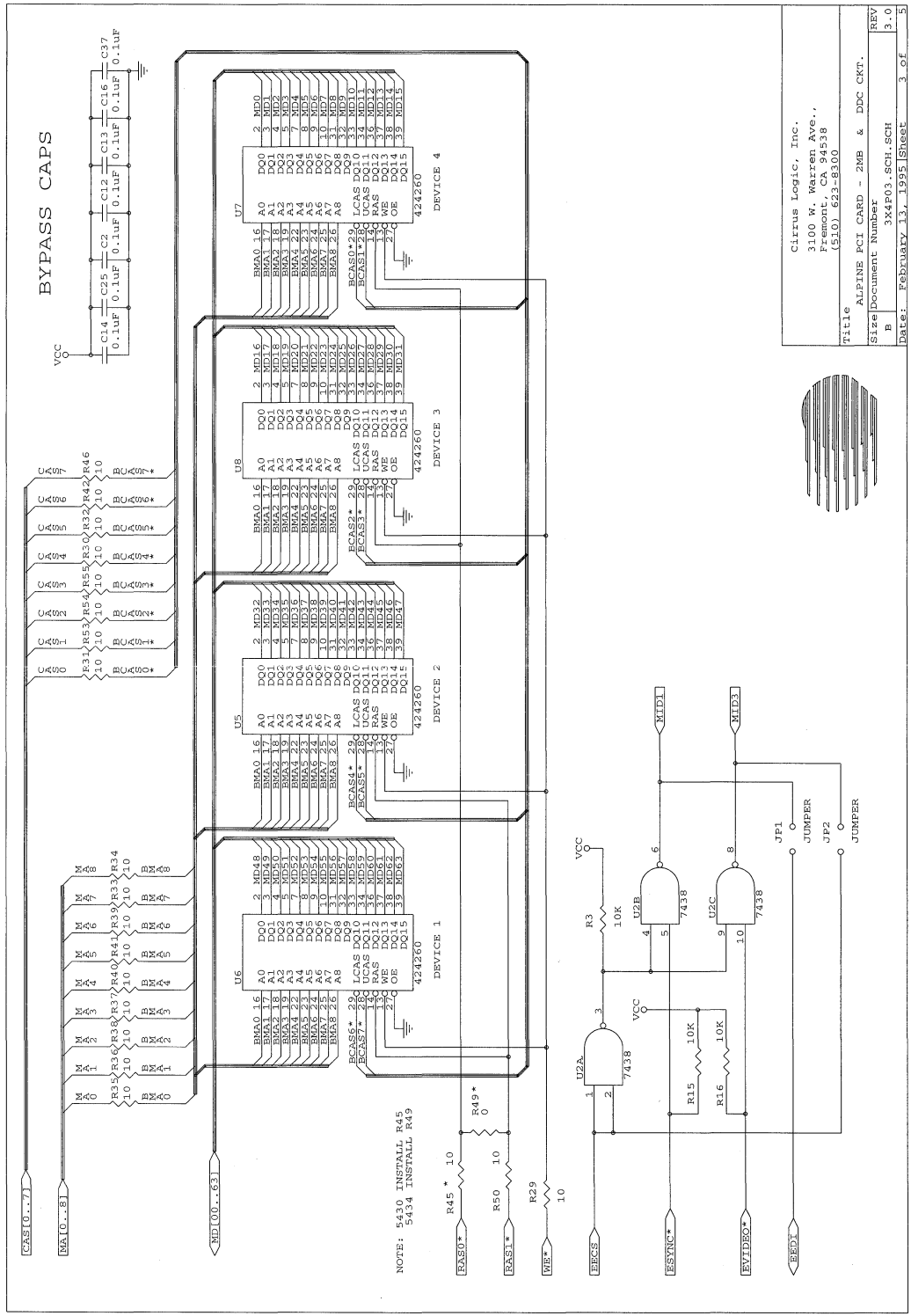
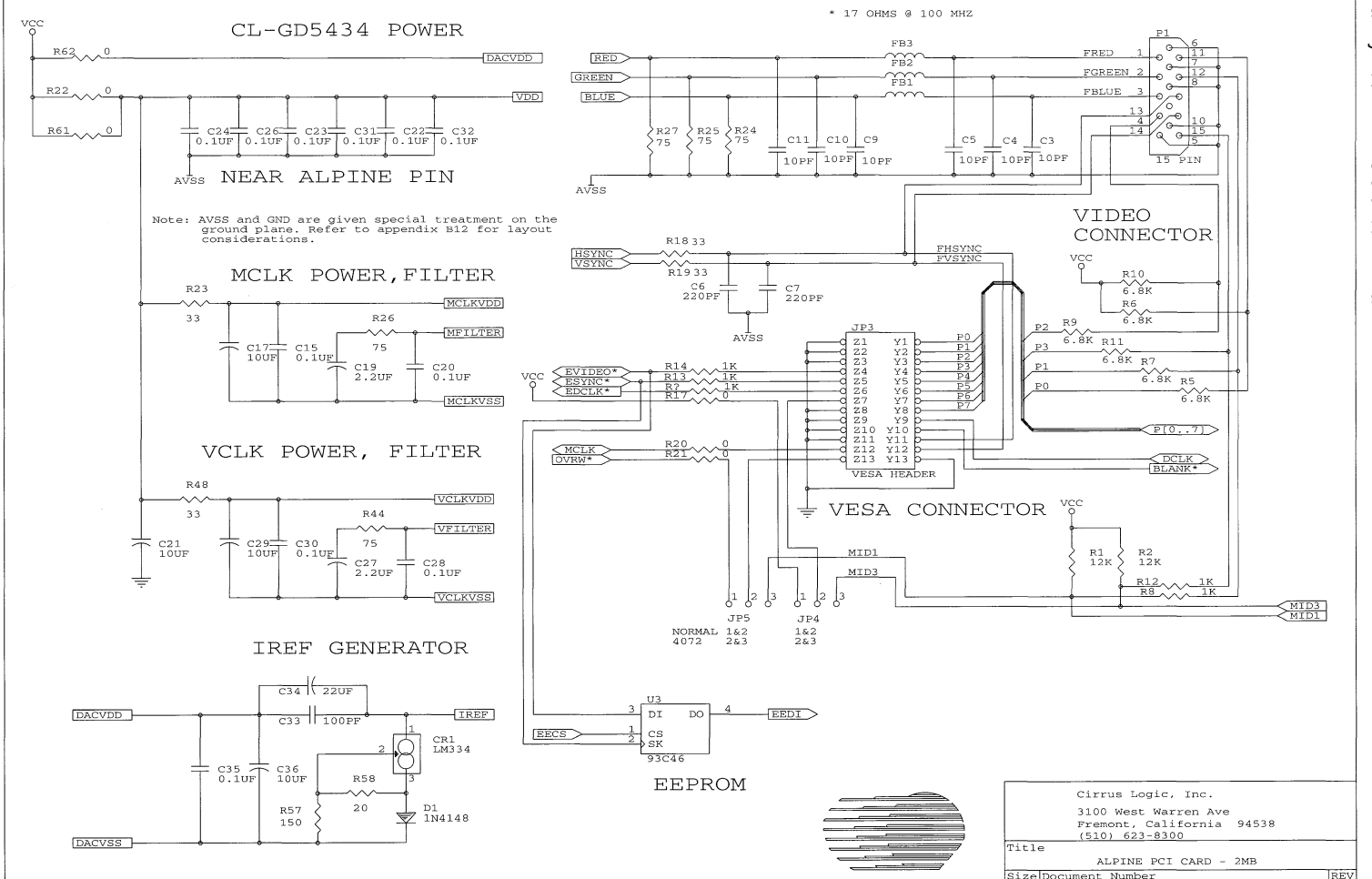
Title ALPINE PCI CARD: 2MB		
Size B	Document Number 3X4P02.SCH	REV 3.0
Date: February 13, 1995	Sheet 2 of 5	





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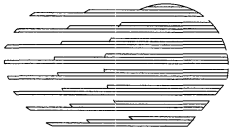
Title		
ALPINE PCI CARD - 2MB		
Size: B	Document Number: 3X4P04.SCH	REV: 3.0
Date: February 13, 1995	Sheet 4 of 5	

BOARD CONFIGURATION OPTIONS: X=INSTALL

	U2	JP1	JP2	R1	R2	R3	R5	R6	R7	R8	R9	R10	R11	R12	R15	R16
OLD DDC1				X					X	X						
NEW DDC1				X						X						
OLD DDC2B	X			X	X	X			X	X			X	X	X	X
NEW DDC2B		X	X	X	X					X				X		

Integrated VFILTER	Do not install C27, C28, R44
Integrated MFILTER	Do not install C19, C20, R26
Integrated IREF (Only if VFILTER is Integrated	Change C19=0 Ohm Res, R44=135 Ohm, C28=0.1uF Do not install C34, R57, R58, D1, CR1
Crystal Option (Only if MFILTER is Integrated)	Install Y1, C42, C43 Do not install X1



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Date: February 10, 1995	Sheet 5 of 5	

Appendix B3

VESA® VL-Bus™ Schematics

VESA® VL-BUS™ SCHEMATICS

1. INTRODUCTION

The schematic was captured with OrCAD® SDT. This schematic and the associated Gerber files are available to Cirrus Logic customers. Board design notes are included. Prints of the layout are included with the schematics.

2. VESA VL-BUS INTERFACE

2.1 Bus Interface Pins

The bus interface pins on the CL-GD543X/'4X are connected directly to the corresponding pins of the VESA VL-Bus. The following table enumerates the pins.

Table B3-1. VESA® VL-Bus™ Interface Pins

Pins	Note
D[31:0]	–
A[21:2]	–
RESET	Note low-pass filter
M/IO# / W/R#	–
RDYR	–
LCLK	–
LRDY	–
LDEV	–
BE[3:0]#	–
A[22:26], A31	HIMEM, LOMEM
INTR	Jumper to ISA B4

2.2 VGA BIOS

The VGA BIOS is contained in a single 27C256 (32 Kbytes). The address is driven directly from the ISA bus SA[15:0] pins. The data is buffered through a single piece of 74LS245. The '245 buffer is enabled with a combination of EROM* and SMEMR*. When they are both low, the buffer will drive the data onto ISA SD[7:0]. The EPROM enables are also controlled with EROM* and SMEMR* to prevent a collision at the BD[7:0] nodes.

3. DISPLAY MEMORY INTERFACE

3.1 Memory Configurations

The display memory is made up of one to four pieces of 256K × 16 dual-CAS* DRAMs. Table B3-2 indicates the memory configurations available with this design.

Table B3-2. Display Memory Configurations

Capacity	CL-GD5430/'40	CL-GD5434/'36
512 Kbyte	✔	
1 Mbyte	✔	✔
2 Mbyte	✔	✔

The RAS* inputs on the second Mbyte can be driven either from the RAS1* or RAS0* outputs of the CL-GD543X/'4X. This node is named BRAS1*. RAS0* must be used for designs populated with the CL-GD5430/'40. RAS1* must be used for designs populated with the CL-GD5434/'36.

3.2 Damping Resistors

The MA lines and all memory control lines from the CL-GD543X/'4X into the display memory array have series resistors to damp reflections from the array and to control edge rates. These resistors are shown as 10 Ω. The value may be adjusted based on the number of devices actually populated. Ideally, the lines should be nearly critically damped.

4. MONITOR INTERFACE

4.1 RGB Lines

The RGB lines are terminated in 75 Ω to AGND. This provides half of the nominal 37.5-Ω DC load; the other half is in the monitor.

π filters on each RGB line control edge rates and reduce RFI to an acceptable level. The component values in these filters represent a trade-off. For good crisp video, especially at higher frequencies, the cutoff frequency should be as high as possible. On the other hand, for reduced emissions the cutoff frequency should be fairly low.

The resistors are located as close as possible to the CL-GD543X/'4X. The filters are located very close to the DB-15 connector. The traces between the CL-GD543X/'4X and the π filters are direct, with a minimum of vias and no sharp corners. These traces must be designed with a characteristic impedance as close as possible to 75 Ω. The edge rates, especially before the π filter, are fast enough that a trace as short as a few inches will begin to behave as a transmission line.

4.2 Sync Lines

HSYNC and VSYNC are isolated with RC filters of 33 Ω and 220 pF. The filter outputs connect directly to the DB-15 connector and to the VESA connector.

4.3 Monitor ID

The BIOS requires information regarding the capability of the connected monitor so that it can program the appropriate refresh rates for the various video modes. In some cases, the monitor capability may be such that higher resolution modes cannot be programmed at all.

The CL-GD543X/'4X supports the DDC1 and DDC2B methods of monitor identification. In addition, two methods each of DDC1 and DDC2B can be configured, depending on the production level of the CL-GD543X/'4X chip. The board configuration option table on sheet 6 of 6 may be used to determine what components are to be populated for any given design.

4.3.1 Heritage Monitors

When super VGA monitors were first available, there was an attempt to standardize on a method of specifying monitor capability that involved unused pins on the DB-15 connector. These pins are called Monitor ID (MID[3:0]). Each of four pins was to be pulled up on the adapter card; the monitor would tie one or more of these pins to digital ground. The BIOS would sense these pins to determine the monitor capability. This attempt at standardization failed for a variety of reasons.

Cirrus Logic reference designs implemented a method of reading all four MID pins for some time; this is no longer supported, either in the board designs or in the BIOS. End users with monitors that are not DDC compliant will use CLMODE or the equivalent to specify the monitor type to the BIOS.

4.3.2 DDC1 Support

DDC1 provides a uni-directional data channel from the monitor to the controller, continuously transmitting Extended Display IDentification, EDID, information. The EDID is transmitted from the monitor to the controller on MID1 (DB15 pin 12). MID1 is connected to Pixel Bus bit P1 via a 6.8 K ohm series resistor, or to the EEDI pin through a 1k resistor. The software is able to read P[1] or the EEDI pin to determine what the monitor is transmitting.

4.3.3 DDC2B Support

DDC2B is a bi-directional data channel based on the I2C bus. The data clock is on MID3 (DB15 pin 15) and the bi-directional data is on MID1 (DB15 pin 12). The schematic diagram shows two implementations of DDC2B. Depending on the capabilities of the CL-GD543X/'4X being populated, one or the other should be populated.

DDC2B is an open collector protocol. The logic in the controller has to pull up each of the two signals (MID1 and MID3), and has to be able to drive each low. In addition, the software has to be able to sense each of the two lines.

For boards populated with CL-GD543X/'4X devices without integrated DDC2B support, the logic labeled **OLD DDC2B** in the table on sheet 6 must be populated. ESYNC* and EVIDEO* drive MID1 and MID3, respectively, through the two open collector gates. The gates are dis-

abled when EECS is high, to prevent the monitor from seeing activity on the lines when the EEPROM is being programmed. The pins can be sensed through Pixel bus lines P1 and P3.

For boards populated with CL-GD543X/'4X devices with integrated DDC2B, the logic labeled **NEW DDC2B** on sheet 6 must be populated. EECS and EEDI drive MID3 and MID1, respectively. The same pins are used to sense the level on the two signals. The following table indicates the production level of devices that are planned to support integrated DDC2B.

Table B3-3. Integrated DDC2B Support

Product	Production Revision Level
CL-GD5434	Production Revision E
CL-GD5436	Production Reversion A
CL-GD5440	Production Revision A

5. VESA® CONNECTOR

5.1 Standard VESA® Interface

The VESA connector pins are tied to the corresponding pins on the CL-GD543X/'4X either directly or through an appropriate resistor. The following table shows the pins on the VESA connector.

Table B3-4. VESA® Connector Pinouts

Pin	Function	Note	Pin	Function	Note
Z1	GND		Y1	P0	
Z2	GND		Y2	P1	
Z3	GND		Y3	P2	
Z4	EVIDEO*	1K Ω	Y4	P3	
Z5	ESYNC*	1K Ω	Y5	P4	
Z6	EDCLK*	1K Ω	Y6	P5	
Z7	+5V or EEDI	a	Y7	P6	
Z8	GND		Y8	P7	
Z9	GND		Y9	DCLK	
Z10	GND		Y10	BLANK*	
Z11	GND		Y11	HYSNC	Filtered
Z12	MCLK	b	Y12	VSYNC	Filtered
Z13	OVRW* or EECS*	c	Y13	GND	

a. Z7 is a no connect in the VESA specification. Cirrus uses this pin either for a VCC supply for a VAFC adapter card or as one pin of an I2C interface.

b. Z12 is no connect in the VESA specification. Cirrus uses this pin for a video clock.

c. Z13 is a no connect in the VESA specification. Cirrus uses this pin either for OVRW* or as one pin of an I2C interface.

5.2 I²C Interface

The I²C interface allows the host to communicate with devices using the standard TV tuner interface, such as the CL-PX4072. Z7 and Z13 on the VESA connector are used.

6. POWER DISTRIBUTION AND CONDITIONING

6.1 Introduction

By far, the most common reason for unsatisfactory performance of a video subsystem is a failure on the part of the board designer to properly handle power distribution and conditioning. Dedicated power and ground planes are very strongly recommended for boards based on all CL-GD543X/'4X products.

6.2 Dedicated Ground Plane

A dedicated ground plane minimizes differential ground offsets and more nearly approximates the ideal notion of "ground". In addition, a ground plane is necessary to predict and control the characteristic impedance of those traces that must be treated as transmission lines.

The ground plane has cuts to partially isolate the critical analog VSS sections from the relatively noisy digital VSS associated with the DRAM array and the bus interface. These cuts may be studied in the Gerber plots. On the schematic diagram, there are four ground nodes. The digital ground is designated with a standard ground symbol. The isolated grounds are designated DACVSS, VCLKVSS, and MCLKVSS.

6.3 Dedicated Power Plane

A dedicated power plane allows low impedance distribution of VCC, minimizing noise and coupling. A dedicated power plane also behaves as an AC ground, making it possible to predict and control the characteristic impedance of traces above it.

The power plane has regions that are completely isolated from the digital portion of the plane. The power plane beneath the CL-GD543X/'4X is isolated, and is connected to the main section of the power plane with two 1-ohm resistors in parallel. This isolated area is designated VDD on the schematic diagram.

Two areas for the synthesizer power conditioning are further isolated. The power plane may be studied in the Gerber plots.

6.4 Power Bypassing

Bypass capacitors are used to minimize power sags caused by current spikes and to reduce the power distribution impedance.

Bulk bypassing is present in the area where power comes onto the board, around the DRAM array, and near the EPROM.

High-frequency bypass capacitor are distributed as needed on the board. Every digital VCC pin on the CL-GD543X/'4X has a bypass capacitor located as close to the pin as possible. Each pin is connected to its capacitor -and the isolated VDD section of the power plane- with a short, thick, direct lead. The ground connection of each capacitor is made with a via directly to the ground plane. Each DRAM has a high frequency bypass capacitor located very close to pin 20 (the VCC pin). The VCC pin is connected with a short, thick, direct lead. The ground connection of the capacitor is made with a via directly to the ground plane.

6.5 Analog Power Conditioning

Two areas on the power plane are further isolated within the VDD section. One is designated MCLKVDD (AVDD4) and one is designated VCLKVDD (AVDD1). Each is connected to VDD via an RC filter consisting of a 33 ohm resistor and a 10-µF capacitor in parallel with a 0.1-µF capacitor. Each of the capacitors in each filter is returned to its respective cutout of ground. Devices with integrated synthesizer filters require the same synthesizer power conditioning.

Power for the DAC (AVDD[3:2]) is taken directly from the VDD section of the power plane. It is bypassed with a 10-µF capacitor in parallel with a 0.1-µF capacitor. Each capacitor is returned to the DAC cutout of the ground plane. Devices with integrated current reference require the same DAC power filtering.

6.6 Configuration Resistors

The configuration resistors in Table B3-5 are shown in the schematic. Some are optional.

Table B3-5. Configuration Resistors

MD Pin	CF-	Use (if Installed)	Note
MD57	CF-9	Extended RAS* timing	
MD58	CF-10	Dual-CAS* DRAMs	
MD56	CF-8	50 MHz MCLK default	Reserved on CL-GD5436
MD54	CF-6	ZWS not supported	Reserved on CL-GD5436
MD48	CF-0	VESA VL-Bus	

6.7 Synthesizer Reference

The 14.3 MHz reference required by the dual-frequency synthesizer is supplied by a crystal oscillator. For devices that support integrated synthesizer filters, the crystal oscillator can be replaced with a crystal connected between the BOSC pin and the MFILTER pin. Each pin on the crystal is bypassed to ground with a 27-pF capacitor. The crystal and capacitors are located close to the pins and connected with short, direct leads.

6.8 Synthesizer Filters

Each of the two synthesizer filter pins is connected to an RC filter. A 0.1-µF input capacitor is connected in parallel with a section comprising a 75-Ω resistor in series with a nominal 2.2-µF capacitor. Each section of the filter is returned to the respective AGND cutout.

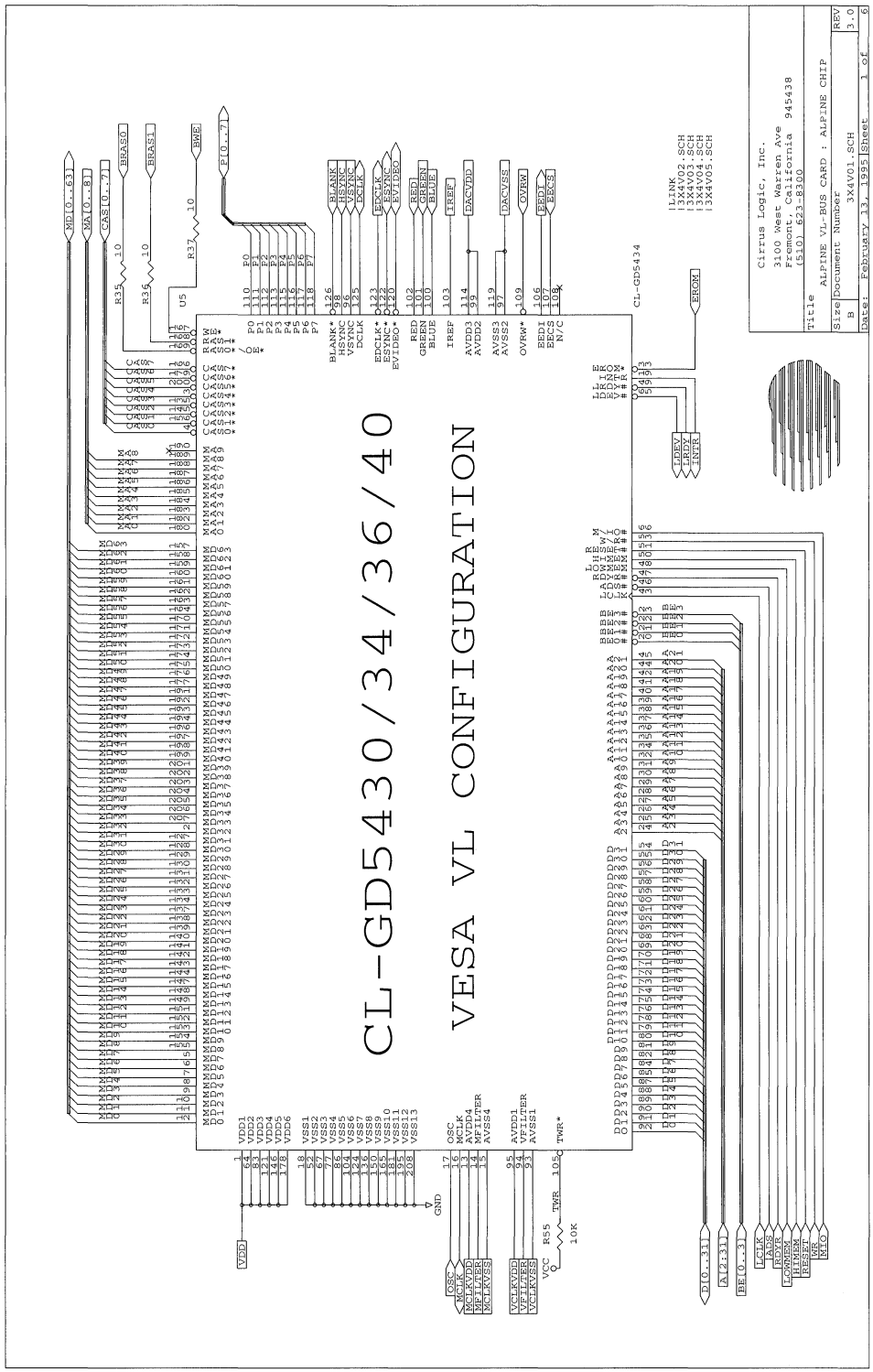
For devices which support integrated synthesizer filters, MFILTER is optionally connected to one side of a reference crystal. VFILTER is optionally connected to a current setting resistor and a parallel capacitor for the integrated current reference. This is described in the "Current Reference" Section.

6.9 Current Reference

The current reference sets the full-scale current output of the DACs. The circuit, based on the LM344, has adequate headroom to allow for minimum VCC conditions for all CL-GD543X/'4X products. The two capacitors between the IREF pin and VDD are optional. The decisions of whether to populate them and the exact value are made at the time the design is evaluated.

For devices that support integrated current reference, IREF is connected to a capacitor to the DAC VDD. VFILTER is connected to a current setting resistor. The resistor value can be calculated with the following equation where *Load* is DC load in ohms, and *VFullScale* is the desired full scale voltage. The derivation of this equation is given in Appendix B8.

$$RSet = \frac{2.52V \bullet Load}{VFullScale}$$


CL-GD5430/34/36/40
VESA VL CONFIGURATION
Cirrus Logic, Inc.
3100 West Warren Ave
Fremont, California 94538
(510) 623-8300
Title
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Size
B
Document Number
3X4V01.SCH
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3.0
Date: February 13, 1995
Sheet 1 of 6
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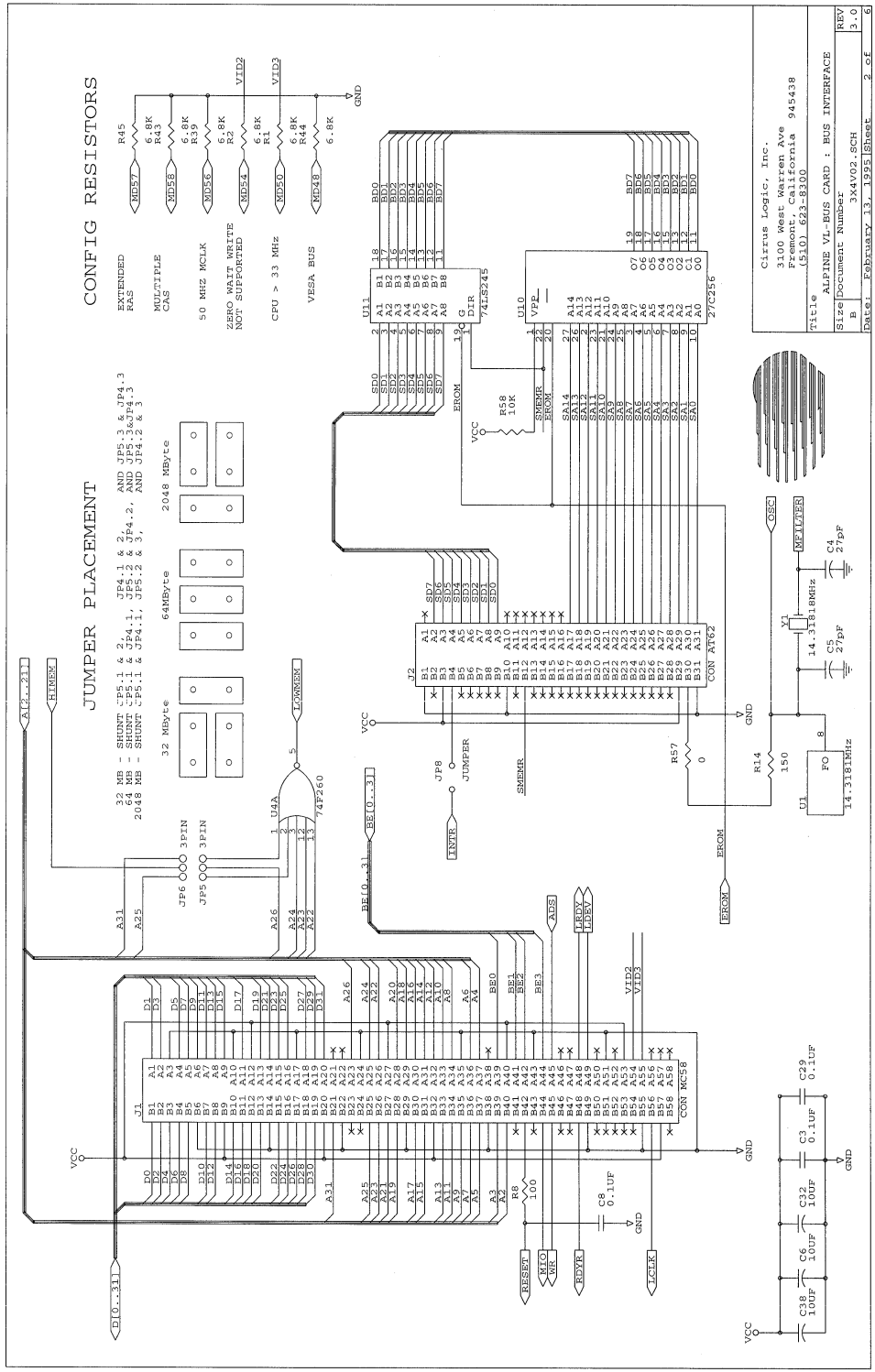
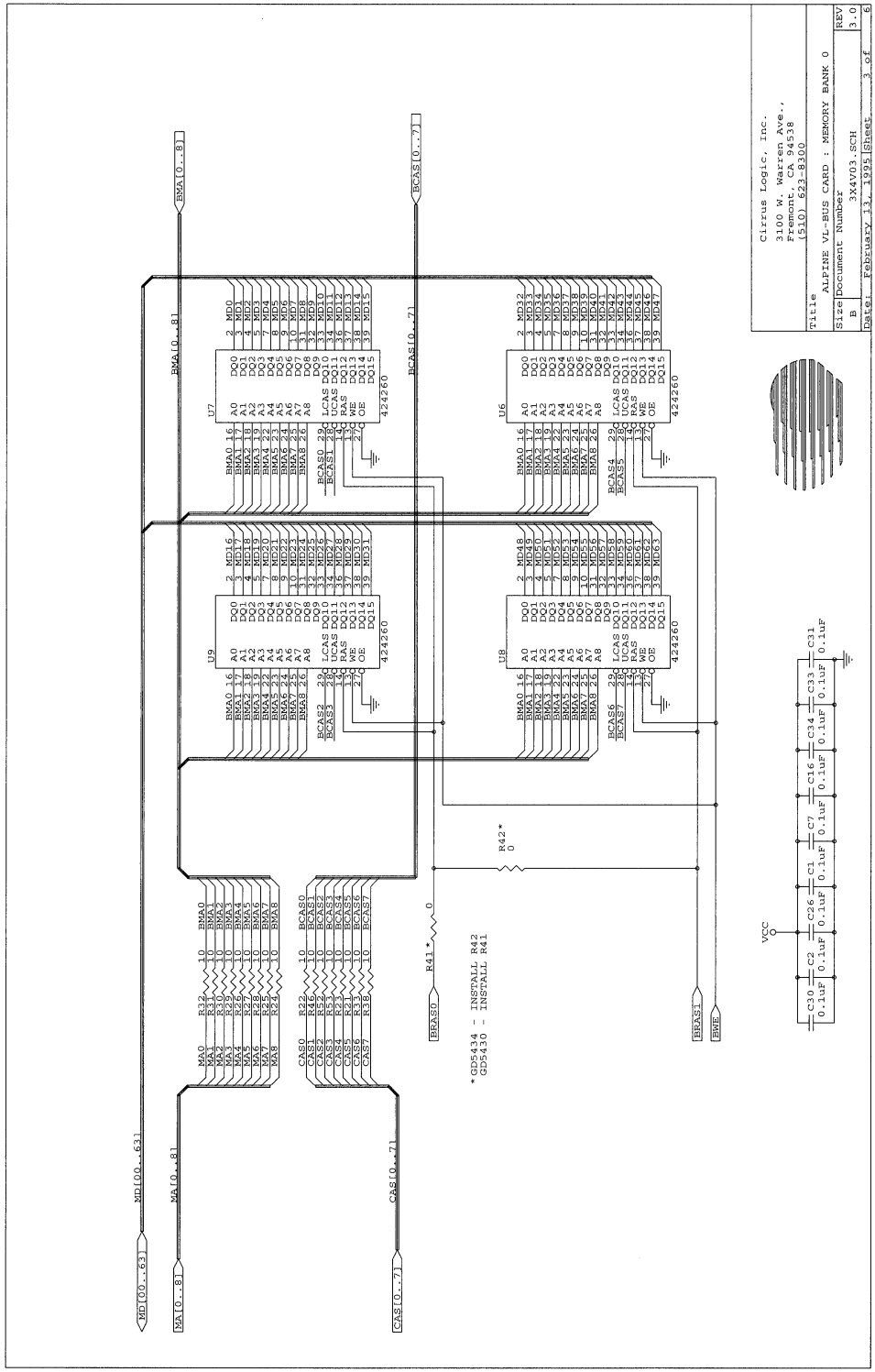
!3X4V05.SCH




Cirrus Logic, Inc.
3100 W. Warren Ave.,
Fremont, CA 94538
(510) 623-8300
Title
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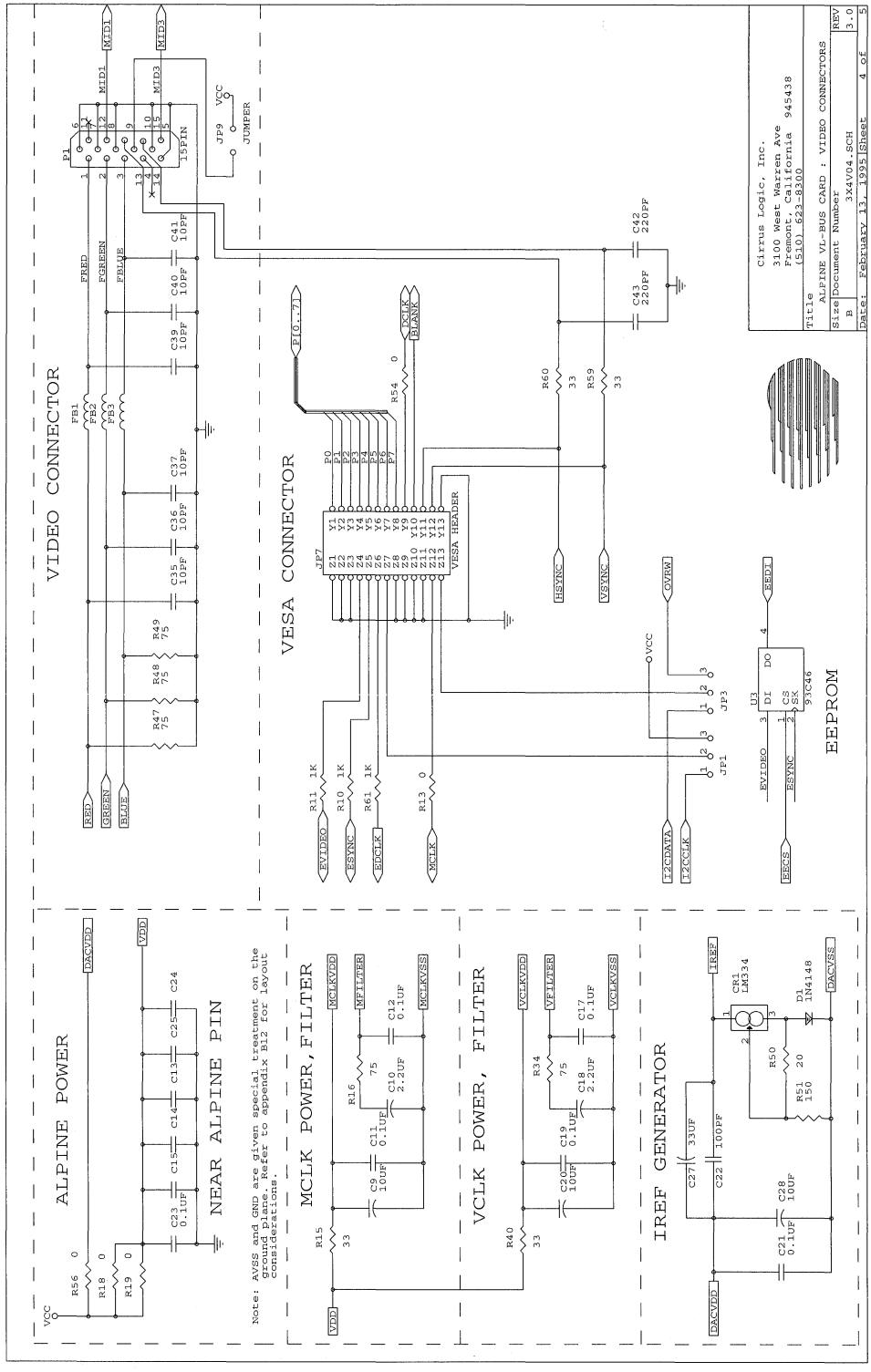
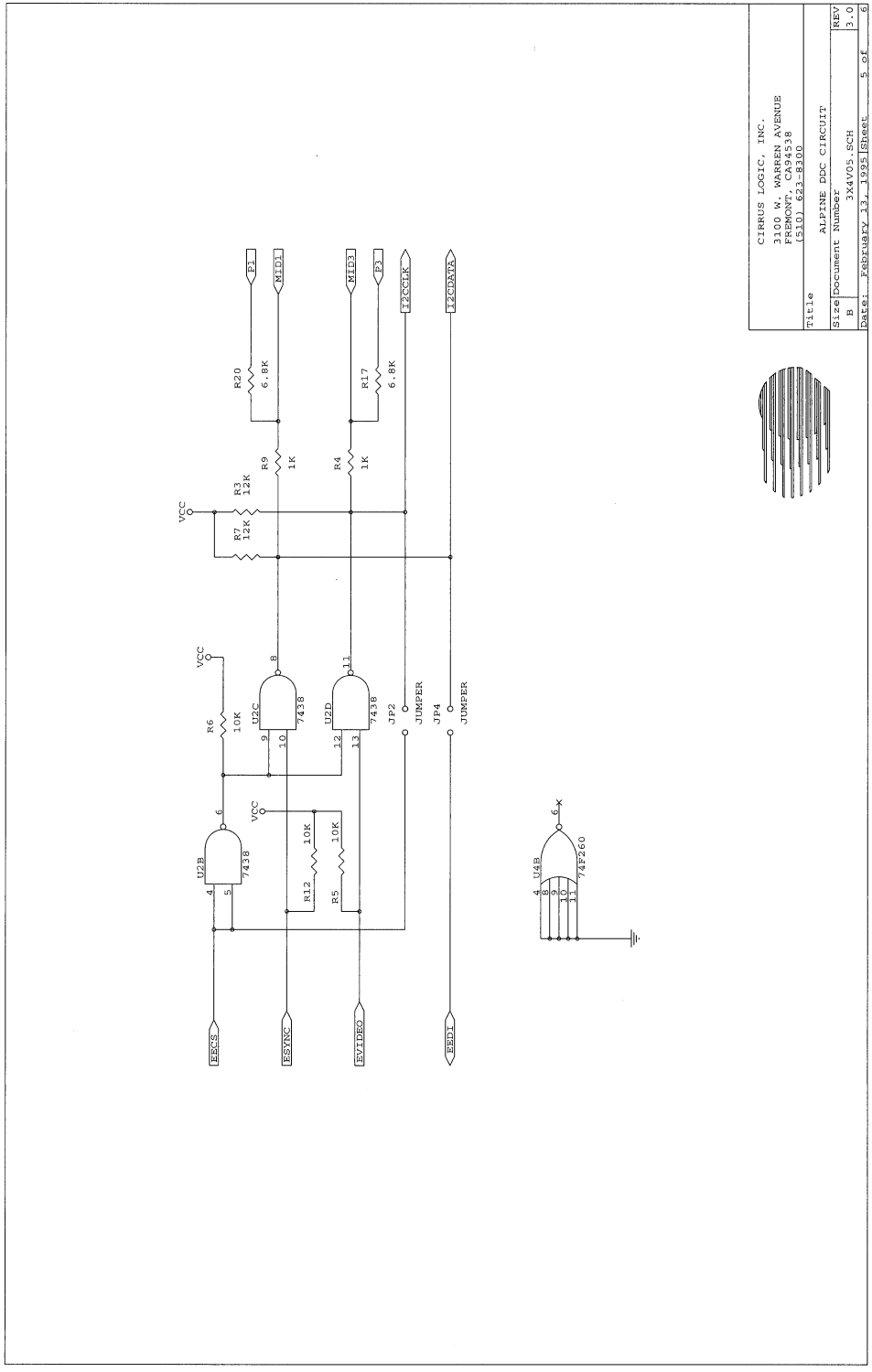
Size
B
Document Number
3X4V03.SCH
REV
3.0
Date: February 13, 1995 Sheet 3 of 6
MD[00..63]
MA[0..8]
CAS[0..7]
BCAS[0..7]
BMA[0..8]
BRAS0
BRAS1
BWE
R41* 0
R42* 0
* GD5434 - INSTALL R42
GD5430 - INSTALL R41
U9
U8
U7
U6
424260
VCC
C30 0.1uF
C2 0.1uF
C26 0.1uF
C1 0.1uF
C7 0.1uF
C16 0.1uF
C34 0.1uF
C33 0.1uF
C31 0.1uF

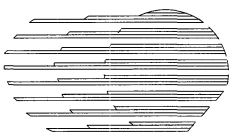



CIRRUS LOGIC, INC.
3100 W. WARREN AVENUE
FREMONT, CA94538
(510) 623-8300
Title ALPINE DDC CIRCUIT
Size B | Document Number 3X4V05.SCH | REV 3.0
Date: February 13, 1995 | Sheet 5 of 6
R20 6.8K
R17 6.8K
R9 1K
R4 1K
R3 12K
R7 12K
R6 10K
R12 10K
R5 10K
U2C 7438
U2D 7438
U2B 7438
U4B 74F260
JP2 JUMPER
JP4 JUMPER
VCC
F1
MID1
MID3
F3
I2CCLK
I2CDATA
EDCS
ESYNC
EVIDEO
EDD1

BOARD CONFIGURATION OPTIONS: X=INSTALL

	U2	JP2	JP4	R3	R4	R5	R6	R7	R9	R12	R17	R20
OLD DDC1								X	X			X
NEW DDC1			X					X	X			
OLD DDC2B	X			X	X	X	X	X	X	X	X	X
NEW DDC2B		X	X	X	X			X	X			

Integrated VFILTER	Do not install C17, C18, R34
Integrated MFILTER	Do not install C10, C12, R16
Integrated IREF (Only if VFILTER is Integrated	Change C18=0 Ohm Res, R34=135 Ohm, C17=0.1uF Do not install R50, R51, D1, CR1
Crystal Option (Only if MFILTER is Integrated)	Install Y1, C4, C5 Do not install U1, R14, R57



Cirrus Logic, Inc.
3100 West Warren Ave
Fremont, CA94538
(510) 623-8300

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Date: February 13, 1995	Sheet 6 of 6	

Appendix B4

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Appendix B5

CL-GD5430 NOTES

CL-GD5430 NOTES

This appendix lists the differences between the CL-GD5430 and CL-GD5434. It is assumed that the reader is familiar with the CL-GD5434.

1. **Video modes/frequencies not supported**
   The CL-GD5430 supports only 2 Mbytes of display memory and a 32-bit memory interface. This restricts the memory modes/refresh frequencies that are supported.

Refer to Appendix B7 for detailed information on RAS* line connections.

2. **32-bit-pixel modes not supported**
   Do *not* program register SR7[3:1] to '100'. Do *not* program register GR30[5:4] to '11'. Registers GR12–GR15 are not present on the CL-GD5430.
3. **ISA bus not supported**
   The CL-GD5430 is a local bus device.
4. **Extension registers are always unlocked**
   SR6 returns the values '12h' or '0fh', depending on the value last written to it. The Extension registers are always unlocked. This is now true of all CL-GD543X/'4X devices.
5. **SRF[7]**
   Bank switching is always enabled on the CL-GD5430. RAS1* connects to the first Mbyte, and RAS0* connects to the second Mbyte of display memory.
6. **CRT FIFO depth control — SRF[5]**
   Programming this bit to a '1' sets the FIFO depth to 20 rather than 32.
7. **MCLK**
   The maximum value that SR1F[5:0] can be programmed is increased from 1Ch to 22h with a maximum MCLK of 60 MHz. This is subject to change with silicon characterization.
8. **SR17[7]**
   The CL-GD5430 does not support this bit (disable DRAM refresh).
9. **Power-management features**
   When register GRE[3] is programmed to a '1' to select Static-Clock mode:
   - MCLK and VCLK are gated off
   - the chip dissipates only static power
   - the RAMDAC is powered off
   - DRAM refresh continues
   - I/O reads and writes may occur (except to the palette) and
   - Memory reads and writes and I/O reads and writes to the palette will not hang the system, but will not product deterministic results.

See Appendix B21, "Power Management".

10. **BLT Destination/Source Start registers**
    The CL-GD5430 supports only 2 Mbytes of display memory. Registers GR2A[5] and GR2E[5] are not used.

11. **BLT destination write mask — GR2F[2:0]**
    If this field is programmed to any value other than '0', then 'n' pixels will not be written on the left edge of each scanline for a color-expanded BLT. See Appendix D8 for more information on the BitBLT engine.
12. **Vertical preset for color-expanded BLT**
    The three low-order bits of the source address select the scanline of source data to be used for the first (or only) scanline. This forces vertical alignment of the pattern. The source must also be aligned.
13. **BLT transparency**
    For color expand with transparency, the CL-GD5430 does not require loading of the Background Color registers. Also, register GR11 need not be programmed for 8 bit-per-pixel color expand with transparency.
14. **Memory-mapped I/O at selectable locations**
    Register SR17[6] selects the address space for memory-mapped I/O.
15. **Overlay/DAC mode switching controls**
    - Internal OVRW* can be chosen for the Switch signal without being fed back as EVIDEO*. See the description of register CR1D[6] in Chapter 9, "Extension Registers".
    - Choosing EVIDEO* AND'ed with OVRW* (CR1A[3:2] = 1, 0) functions as originally intended.
    - Color key compare type is always a logical identity (no arithmetic compares).

See Appendix B14, "Video Overlay and DAC Mode Switching", for a complete description of the overlay functions.

16. **VAFC baseline input**
    Bit 5 of the Hidden DAC register is redefined to support VESA VAFC baseline input. It controls pixel doubling in 16-bit-per-pixel display modes. The VCLK VCO is available on the MCLK pin.
17. **Chip ID updated**
    The device ID in CR27[7:2] and PCI[0] is changed as indicated in the following table:

Product	Device ID
CL-GD5430	101000
CL-GD5434	101010

18. **Configuration options changes**
    The CL-GD5430 supports the MCLK pin source (VCLK VCO on MCLK), but does not support 'disable internal DAC'.
19. **CR1C removed**
    GENLOCK and sync adjust are not present on the CL-GD5430.
20. **Hidden DAC register mode 01xx1010**
    Palette Clock Doubling mode is not supported on the CL-GD5430.
21. **PCI bus relocatable I/O**
    The CL-GD5430 supports relocated I/O addresses for the PCI bus only.

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Appendix B6

Extended Color Modes

EXTENDED COLOR MODES

1. INTRODUCTION

The CL-GD543X/'4X family supports the following extended color modes:

- 8-bit-per-pixel (VGA-standard 256-color Palette mode)
- 8-bit-per-pixel grayscale
- 8-bit-per-pixel (256 color, 3-3-2)
- 8-bit-per-pixel AccuPak™ (CL-GD5440 only)
- 15-bit-per-pixel (32K color, 5-5-5 TARGA™ mode)
- Mix mode: 32K colors (5-5-5 mode) and 256 colors (standard VGA mode)
- 16-bit-per-pixel (64K colors, 5-6-5 XGA™ mode)
- 16-bit-per-pixel YCrCb (CL-GD5440 only)
- 24-bit-per-pixel (16.8M colors, True-color mode)
- 32-bit-per-pixel (16.8M colors, with Alpha Overlay — CL-GD5434/'36 only)

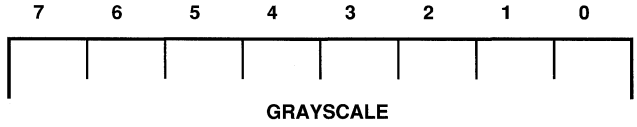
2. VGA COMPATIBILITY (PALETTIZED)

This mode supports the industry-standard 8-bit 256 color palette mode. This mode is selected by writing the value 0 to the HDR (Hidden DAC register). The HDR is forced to '0' at reset time.

Each pixel is represented by one byte in display memory. The value is used as an address into the color palette. The three six-bit color values (one each for Red, Green, and Blue) from the corresponding location in the color palette are passed to the three DACs.

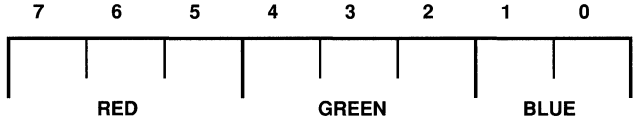
3. 8-BIT GRAYSCALE

Each pixel is represented by one byte. The byte is sent to all three DACs in parallel. The result on the screen is a Gray pixel with brightness corresponding to the value of the byte. The palette is not used in this mode.



4. 3-3-2 MODE with 256 COLORS

Each pixel is represented by one byte. The eight bits are allocated to the three colors as indicated in the diagram below. This provides access to 256 fixed colors. This is useful for some video overlay modes. The palette is not used in this mode.

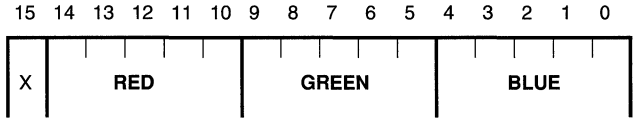


5. 5-5-5 MODE with 32K COLORS

This mode supports the industry-standard 5-5-5 RGB mode with 32,768 colors. This mode is selected by writing the value C0 or E0 to the HDR. Each pixel is represented by 15 bits containing five bits each of Red, Green, and Blue color information. The palette is not used in this mode.

Each pixel is stored as two contiguous bytes on a 2-byte boundary. When pixels are written into display memory using 16- or 32-bit write operations, they can be treated just as shown in the following diagram. If partial pixels are being stored one byte at a time in a little endian machine such as an '86 (80386 and 80486), the byte containing the Blue bits will be stored at the first address and the byte containing the Red bits will be stored at the next higher address.

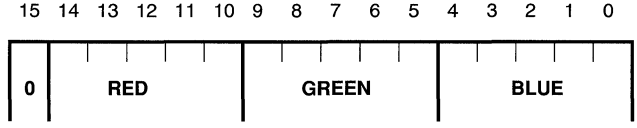
This DAC mode is no longer used by the Cirrus Logic BIOS. 32K color modes now use the 5-5-5 with 256-Color Mix mode. For compatibility, bit 15 of each pixel must be programmed to '0'.



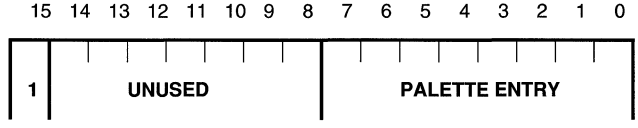
6. 5-5-5 with 256-COLOR MIX MODE

This mode allows the mixing of industry-standard 5-5-5 RGB mode pixels and palette DAC pixels. This mode is selected by writing the value D0 or F0 to the HDR. The interpretation is based on bit 15 of each pixel.

If bit 15 contains a '0', the remaining 15 bits will be interpreted as 5-5-5 video. The palette is not used in this case.



If bit 15 contains a '1', bits 14:8 will be ignored. Bits 7:0 will select an entry in the palette whose contents will be directed to the DACs.

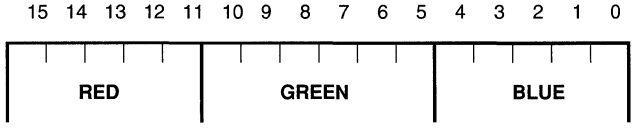


Each pixel is stored as two contiguous bytes on a 2-byte boundary. When pixels are written into display memory using 16- or 32-bit write operations, they can be treated as shown in the diagrams above. If partial pixels are being stored one byte at a time in a little endian machine (such as an '86), the byte containing the Blue bits will be stored at the first address and the byte containing the Red bits will be stored at the next higher address.

7. XGA™ 5-6-5 MODE with 64K COLORS

This mode supports the XGA™ 5-6-5 RGB mode with 65,536 colors. This mode is selected by writing the value C1 or E1 to the HDR. Each pixel is represented by 16 bits containing 5 bits of Red, 6 bits of Green, and 5 bits of Blue color information. The palette is not used in this mode.

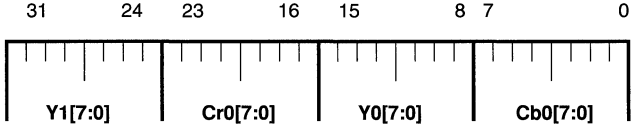
Each pixel is stored as two contiguous bytes on a 2-byte boundary. When pixels are written into display memory using 16- or 32-bit write operations, they can be treated as shown in the following diagram. If partial pixels are being stored, one byte at a time, in a little endian machine such as an '86. The byte containing the Blue bits will be stored at the first address and the byte containing the Red bits will be stored at the next higher address.



8. 16-BIT-PER-PIXEL YCrCb 4:2:2 MODE (CL-GD5440 only)

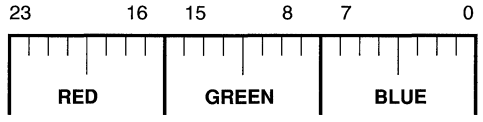
YCrCb is defined in the CCIR (International Radio Consultive Committee) Recommendation CCIR601. The CL-GD5440 supports the YCrCb 4:2:2 format. Each two-pixel unit is stored as one DWORD (doubleword) containing luminance for each of the two pixels and chrominance for alternate pixels. When YCrCb is displayed, the missing chrominance values are generated by interpolation.

YCrCb video can be displayed only within the video window.



9. 8-8-8 MODE with 16.8M COLORS

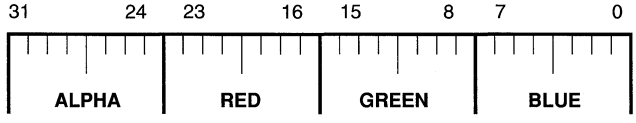
This mode supports the industry-standard 8-8-8 RGB mode with 16,777,216 colors. Each pixel is represented by 24 bits containing 1 byte each of Red, Green, and Blue color information. Each pixel is stored in three contiguous bytes. The Blue value is stored in the lowest-addressed byte, the Green value is stored in the next higher-addressed byte, and the Red value is stored in the next higher-addressed byte. For the 640 × 480 24-bit-per-pixel mode, the Cirrus Logic BIOS sets the Offset register to 2048. A small amount of memory is unused, but the address calculations are simplified somewhat. The palette is not used in this mode. This mode allows 640 × 480 true color with 1 Mbyte of display memory, but requires that the VCLK be programmed to three times the pixel rate. Generally, this mode will be used for systems with only 1 Mbyte of display memory or with the CL-GD5430/'40 that do not support 32-bit-per-pixel mode. The CL-GD5436 supports true Packed-24 modes.



10. 8-8-8-8 MODE with 16.8M COLORS and ALPHA ('34/'36 only)

This mode supports the industry-standard 8-8-8-8 ARGB mode with 16,777,216 colors plus the Alpha Channel. Each pixel is represented by 32 bits containing 1 byte each of Alpha, Red, Green, and Blue color information. Each pixel is stored in four contiguous bytes. The Blue value is stored in the lowest-addressed byte, followed by one byte each of Green, Red, and Alpha in that order. This mode is not supported by the CL-GD5430/'40.

This mode is distinguished from the three-byte-per-pixel mode by the programming of SR7[3:1]. If this field is programmed to '100', Alpha-byte mode is chosen. VCLK is programmed to be equal to the pixel rate. This mode requires a 64-bit DRAM data path, and allows true color with pixel rates above 25 MHz. The Alpha byte can be used for Color Key Compare. For more information refer to Appendix B14, "Video Overlay and DAC Mode Switching".



Appendix B7

Memory Configurations and Timing

MEMORY CONFIGURATIONS AND TIMING

1. INTRODUCTION

This appendix covers three topics related with the selection of DRAMs for the CL-GD543X/'4X: DRAM configuration and connections, DRAM timing requirements, and MCLK requirements for Video modes.

2. DRAM CONFIGURATIONS

The CL-GD543X/'4X supports a number of display memory configurations, from 512 Kbytes to 4 Mbytes, using DRAMs that are organized as:

- **256K × 4**
- **256K × 8 (Each device replaces two pieces of 256K × 4)**
- **256K × 16 — Dual-WE* or Dual-CAS*, Symmetric or Asymmetric Addressing**

The following table indicates the memory configurations that can be used with the CL-GD5430/'40 and the CL-GD5434/'36.

Table B7-1. Configurations for CL-GD5430/'40 and CL-GD5434/'36

DRAM Configuration	CL-GD5430/'40	CL-GD5434/'36
256K × 4	512K–2M	1M–2M
256K × 8	512K–2M	1M–2M
256K × 16: dual-CAS*	512K–2M	1M–4M
256K × 16: dual-WE*	512K–1M	1M–2M

For 256K × 16 devices, the system designer needs to choose between dual-CAS* and dual-WE* devices. Dual-CAS* devices are recommended since that configuration has the least capacitive loading on the CAS* lines, which need to toggle faster than the others. In addition, the maximum capacity using dual-CAS* devices is twice that as compared to dual-WE* devices. For 256K × 4, and 256K × 8 devices, the exclusive use of CAS* steering is recommended.

3. DUAL LAYOUT CONSIDERATIONS

The CL-GD5430 and CL-GD5440 on the one hand, and the CL-GD5434 and CL-GD5436 on the other hand have slightly different DRAM interfaces. If a common PC board is being built for both the CL-GD5430/'40 and the CL-GD5434/'36, the RAS* connection to the second Mbyte requires special treatment. This is because the CL-GD5430/'40 uses RAS0/OE* for the second Mbyte while the CL-GD5434/'36 uses RAS1* for the second Mbyte. An obvious way to treat this is to source RAS* to the second Mbyte from both RAS0/OE* and RAS1* through zero-Ω (or damping) resistors. At manufacturing time, only the appropriate resistor is actually populated.

4. DRAM CONNECTION TABLES

Table B7-2 is an index to the connection tables in this appendix. The memory devices must be wired as indicated in the connection tables. The following may be taken into consideration by the layout artist:

- For all cases, the Control Lines (RAS*, CAS*, WE*, and OE*) must be connected exactly as indicated. It is the control line distribution that defines the memory device numbers in the tables that follow.
- For 256K × 4 or 256K × 8 devices, the Address pins may be interchanged. The Data pins of any device or any two devices sharing common control lines may be interchanged.
- For 256K × 16 symmetric addressed DRAM, the Address pins may be interchanged. The Data pins of any byte may be interchanged.
- For asymmetric 256K × 16 devices, A[7:1] may be interchanged. MA0, MA8, and MA9 must connect as indicated. The Data pins of any byte may be interchanged.

Table B7-2. Connection Tables Overview

DRAM Configuration	Number of DRAMs	Total Memory	Connection Table	Note
256K × 4	4	512 Kbyte	B7-3	CL-GD5430/'40 only
256K × 4	8	1 Mbyte	B7-4	
256K × 4	16	2 Mbyte	B7-5	
256K × 16, dual-CAS*, symmetric	1	512 Kbyte	B7-6	CL-GD5430/'40 only
256K × 16, dual-CAS*, symmetric	2	1 Mbyte	B7-7	
256K × 16, dual-CAS*, symmetric	4	2 Mbyte	B7-8	
256K × 16, dual-CAS*, symmetric	8	4 Mbyte	B7-9	CL-GD5434/'36 only
256K × 16, dual-WE*, asymmetric	1	512 Kbyte	B7-10	CL-GD5430/'40 only
256K × 16, dual-WE*, asymmetric	2	1 Mbyte	B7-11	
256K × 16 dual-WE*, asymmetric	4	2 Mbyte	B7-12	CL-GD5434/'36 only
256K × 16, dual-WE*, symmetric	1	512 Kbyte	B7-13	CL-GD5430/'40 only
256K × 16, dual-WE*, symmetric	2	1 Mbyte	B7-14	
256K × 16 dual-WE*, symmetric	4	2 Mbyte	B7-15	CL-GD5434/'36 only

The following tables show the detailed memory interface connections for every DRAM configuration supported by CL-GD543X/'4X.

Table B7-3. *256K* × *4 DRAMs*: 512-Kbyte Display Memory (CL-GD5430/'40 only)

Memory Device	One	Two	Three	Four
OE*	GND	GND	GND	GND
WE*	WE*	WE*	WE*	WE*
RAS*	RAS1*	RAS1*	RAS1*	RAS1*
CAS*	CAS6*	CAS6*	CAS7*	CAS7*
ADDR	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[55:52]	MD[51:48]	MD[63:60]	MD[59:56]

Table B7-4. *256K* × *4 DRAMs*: 1-Mbyte Display Memory

Memory Device	One	Two	Three	Four	Five	Six	Seven	Eight
OE*	GND	GND	GND	GND	GND	GND	GND	GND
WE*	WE*	WE*	WE*	WE*	WE*	WE*	WE*	WE*
RAS*	RAS1*	RAS1*	RAS1*	RAS1*	RAS1*	RAS1*	RAS1*	RAS1*
CAS*	CAS6*	CAS6*	CAS7*	CAS7*	CAS4*	CAS4*	CAS5*	CAS5*
ADDR	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[55:52]	MD[51:48]	MD[63:60]	MD[59:56]	MD[39:36]	MD35:32]	MD[47:44]	MD[43:40]

Table B7-5. *256K* × *4 DRAMs*: 2-Mbyte Display Memory†

Memory Device	One	Two	Three	Four	Five	Six	Seven	Eight
OE*	GND	GND	GND	GND	GND	GND	GND	GND
WE*	WE*	WE*	WE*	WE*	WE*	WE*	WE*	WE*
RAS*	RAS1*	RAS1*	RAS1*	RAS1*	RAS1*	RAS1*	RAS1*	RAS1*
CAS*	CAS6*	CAS6*	CAS7*	CAS7*	CAS4*	CAS4*	CAS5*	CAS5*
ADDR	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[55:52]	MD[51:48]	MD[63:60]	MD[59:56]	MD[39:36]	MD35:32]	MD[47:44]	MD[43:40]
Memory Device	**Nine**	**Ten**	**Eleven**	**Twelve**	**Thirteen**	**Fourteen**	**Fifteen**	**Sixteen**
OE*	GND	GND	GND	GND	GND	GND	GND	GND
WE*	WE*	WE*	WE*	WE*	WE*	WE*	WE*	WE*
RAS*	RAS1*	RAS1*	RAS1*	RAS1*	RAS1*	RAS1*	RAS1*	RAS1*
CAS*	CAS2*	CAS2*	CAS3*	CAS3*	CAS0*	CAS0*	CAS1*	CAS1*
ADDR	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[23:20]	MD[19:16]	MD[31:28]	MD[27:24]	MD[7:4]	MD[3:0]	MD[15:12]	MD[11:8]

† For compatibility with the CL-GD5430/'40, make provisions to source RAS* to the second Mbyte (devices 9–16) from RAS0*/OE*.

Table B7-6. *256K* × *16 DRAM*: 512-Kbyte Display Memory — Dual-CAS* (CL-GD5430/'40 only)

Memory Device	One
OE*	GND
WE*	WE*
RAS*	RAS1*
UCAS*	CAS7*
LCAS*	CAS6*
ADDR	MA[8:0]
DATA[16:8]	MD[63:56]
DATA[8:1]	MD[55:48]

Table B7-7. *256K* × *16 DRAMs*: 1-Mbyte Display Memory — Dual-CAS*

Memory Device	One	Two
OE*	GND	GND
WE*	WE*	WE*
RAS*	RAS1*	RAS1*
UCAS*	CAS7*	CAS5*
LCAS*	CAS6*	CAS4*
ADDR	MA[8:0]	MA[8:0]
DATA[16:8]	MD[63:56]	MD[47:40]
DATA[8:1]	MD[55:48]	MD[39:32]

Table B7-8. *256K* × *16 DRAMs*: 2-Mbyte Display Memory — Dual-CAS*†

Memory Device	One	Two	Three	Four
OE*	GND	GND	GND	GND
WE*	WE*	WE*	WE*	WE*
RAS*	RAS1*	RAS1*	RAS1*	RAS1*
UCAS*	CAS7*	CAS5*	CAS3*	CAS1*
LCAS*	CAS6*	CAS4*	CAS2*	CAS0*
ADDR	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA[16:8]	MD[63:56]	MD[47:40]	MD[31:24]	MD[15:8]
DATA[8:1]	MD[55:48]	MD[39:32]	MD[23:16]	MD[7:0]

† For compatibility with the CL-GD5430/'40, make provisions to source RAS* to the second Mbyte (devices 3–4) from RAS0*/OE*.

Table B7-9. *256K* × *16 DRAMs*: 4-Mbyte Display Memory — Dual-CAS* (CL-GD5434/'36 only)

Memory Device	One	Two	Three	Four	Five	Six	Seven	Eight
OE*	GND	GND	GND	GND	GND	GND	GND	GND
WE*	WE*	WE*	WE*	WE*	WE*	WE*	WE*	WE*
RAS*	RAS1*	RAS1*	RAS1*	RAS1*	RAS0*	RAS0*	RAS0*	RAS0*
UCAS*	CAS7*	CAS5*	CAS3*	CAS1*	CAS7*	CAS5*	CAS3*	CAS1*
LCAS*	CAS6*	CAS4*	CAS2*	CAS0*	CAS6*	CAS4*	CAS2*	CAS0*
ADDR	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA[15:8]	MD[63:56]	MD[47:40]	MD[31:24]	MD[15:8]	MD[63:56]	MD[47:40]	MD[31:24]	MD[15:8]
DATA[7:0]	MD[55:48]	MD[39:32]	MD[23:16]	MD[7:0]	MD[55:48]	MD[39:32]	MD[23:16]	MD[7:0]

Table B7-10. *256K* × *16 DRAMs*: 512-Kbyte Display Memory — Dual-WE*, Asymmetric (CL-GD5430/'40 only)

Memory Device	One
OE*	OE*
CAS*	WE*
RAS*	RAS1*
WEH*	CAS7*
WEL*	CAS6*
A[9]	MA[9]
A[8]	MA[0]
A[7:1]	MA[7:1]
A[0]	MA[8]
DATA[15:8]	MD[63:56]
DATA[7:0]	MD[55:48]

Table B7-11. *256K* × *16 DRAMs*: 1-Mbyte Display Memory — Dual-WE*, Asymmetric

Memory Device	One	Two
OE*	OE*	OE*
CAS*	WE*	WE*
RAS*	RAS1*	RAS1*
WEH*	CAS7*	CAS5*
WEL*	CAS6*	CAS4*
A[9]	MA[9]	MA[9]
A[8]	MA[0]	MA[0]
A[7:1]	MA[7:1]	A[7:1]
A[0]	MA[8]	MA[8]
DATA[15:8]	MD[63:56]	MD[47:40]
DATA[7:0]	MD[55:48]	MD[39:32]

Table B7-12. *256K* × *16 DRAMs*: 2-Mbyte Display Memory — Dual-WE*, Asymmetric (CL-GD5434/'36 only)

Memory Device	One	Two	Three	Four
OE*	OE*	OE*	OE*	OE*
CAS*	WE*	WE*	WE*	WE*
RAS*	RAS1*	RAS1*	RAS1*	RAS1*
WEH*	CAS7*	CAS5*	CAS3*	CAS1*
WEL*	CAS6*	CAS4*	CAS2*	CAS0*
A[9]	MA[9]	MA[9]	MA[9]	MA[9]
A[8]	MA[0]	MA[0]	MA[0]	MA[0]
A[7:1]	MA[7:1]	MA[7:1]	MA[7:1]	MA[7:1]
A[0]	MA[8]	MA[8]	MA[8]	MA[8]
DATA[15:8]	MD[63:56]	MD[47:40]	MD[31:24]	MD[15:8]
DATA[7:0]	MD[55:48]	MD[39:32]	MD[23:16]	MD[7:0]

Table B7-13. *256K* × *16 DRAM*: 512-Kbyte Display Memory — Dual-WE*, Symmetric (CL-GD5430/'40 only)

Memory Device	One
OE*	OE*
CAS*	WE*
RAS*	RAS1*
WEH*	CAS7*
WEL*	CAS6*
ADDR	MA[8:0]
DATA[16:8]	MD[63:56]
DATA[8:1]	MD[55:48]

Table B7-14. *256K* × *16 DRAMs*: 1-Mbyte Display Memory — Dual-WE*, Symmetric

Memory Device	One	Two
OE*	OE*	OE*
CAS*	WE*	WE*
RAS*	RAS1*	RAS1*
WEH*	CAS7*	CAS5*
WEL*	CAS6*	CAS4*
ADDR	MA[8:0]	MA[8:0]
DATA[16:8]	MD[63:56]	MD[47:40]
DATA[8:1]	MD[55:48]	MD[39:32]

Table B7-15. *256K* × *16 DRAMs*: 2-Mbyte Display Memory — Dual-WE*, Symmetric (CL-GD5434/'36 only)

Memory Device	One	Two	Three	Four
OE*	OE*	OE*	OE*	OE*
CAS*	WE*	WE*	WE*	WE*
RAS*	RAS1*	RAS1*	RAS1*	RAS1*
WEH*	CAS7*	CAS5*	CAS3*	CAS1*
WEL*	CAS6*	CAS4*	CAS2*	CAS0*
ADDR	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA[16:8]	MD[63:56]	MD[47:40]	MD[31:24]	MD[15:8]
DATA[8:1]	MD[55:48]	MD[39:32]	MD[23:16]	MD[7:0]

5. DRAM TIMING REQUIREMENTS

The CL-GD543X/'4X state machine that generates the DRAM timing operates from an internally generated signal called MCLK. As the MCLK frequency is increased, the MCLK period is decreased and the DRAMs have to be faster to keep pace. Increasing MCLK frequency increases performance, at the cost of more expensive DRAM devices.

Not all DRAMs of a given speed grade are the same. There are marked differences in the values of several parameters including t_{RP} and t_{CAP}. This means it is impossible to say with any certainty that a DRAM from *any* vendor with such and such a speed grade can be used with an MCLK of X MHz. A system designer must carefully compare the proposed DRAM data sheet and the timing provided in the CL-GD543X/'4X documentation to determine the maximum permissible MCLK.

The timing flexibility of the CL-GD543X/'4X must also be taken into consideration. There are two timing options, Extended RAS* timing and EDO timing.

5.1 Extended RAS* Timing

With standard RAS* timing a random read or write cycle requires six MCLK periods, and a Fast-page Cycle requires two MCLK periods. If a pull-down resistor is installed on MD57, the DRAM timing will be extended so that a random read or write cycle requires seven MCLK periods. In particular, 1⁄2 additional MCLK is inserted between RAS* and CAS* (increasing the available RAS* access time), and 1⁄2 additional MCLK is inserted in RAS* precharge.

Some DRAMs have Column Address access and CAS* access times that are relatively faster than their Row access times. By using Extended RAS* timing with these devices, the MCLK frequency can be increased without decreasing the RAS* Access and RAS* Precharge times. Depending on how much the MCLK can be increased, this may result in better performance. The only way to be certain is to run the critical benchmarks with both configurations. It should be clear that switching to Extended RAS* without increasing MCLK will certainly result in *decreased* performance.

5.2 EDO Timing (CL-GD5436)

The CL-GD5436 provides EDO support. When GR18[2] is programmed to '1', the timing changes so that a RAS* cycle is eight MCLKs. The device must have been configured for extended RAS* timing (see CF9 in Appendix B9). The following table summarizes the timing equations for the CL-GD5436.

Table B7-16. EDO Timing Equations (CL-GD5436)

Parameter	Description	Normal	Extended	EDO
28-t_5	t_{RCD}	2.5 m[a] – 7.5 ns	3 m	4 m
28-t_6	t_{RAS}	3.5 m	4 m – 1 ns	5 m – 1ns
28-t_7	t_{RP}	2.5 m –2 ns	3 m – 1.5 ns	3 m – 1.5 ns
29-t_3	DRAM access time from RAS*	3.5 m	4 m – 1 ns	5 m
29-t_4	DRAM access time from Column Address	2 m	2 m	3 m
29-t_5	DRAM access time from CAS*	1 m + 3 ns	1 m + 3 ns	2 m
29-t_6	DRAM access time from CAS* precharge	2 m	2 m	3 m

a. m = MCLK

Extended RAS* timing must be configured in order to program EDO timing. This means there are three cases, Standard RAS* timing, Extended RAS* timing, and EDO timing. This is reflected in the timing diagrams and in the two following tables.

5.3 Dram Timing Equations Evaluated

Refer to the timing diagrams for the display memory Interface in the *CL-GD543X/'4X Data Book*, "Electrical Specifications" (Section 7). Most of the timing numbers are provided in terms of MCLK period. For example, 't_1 — t_{ASR}: Address Setup to RAS*' is 1.5m – 9 ns. In that equation, 'm' is the MCLK period. In the following two tables, each of the equations in the timing diagram is evaluated for a number of MCLK frequencies. The parameters are rounded to integers. The numbers given are minimums. The appearance of any frequency in these tables is not to be taken as a guarantee that any Cirrus Logic device will operate at that frequency or that DRAMs are available that will operate with the resulting timings.

Table B7-17. DRAM Timing Parameter Equations Evaluated (Not EDO Timing)

Table/ Parameter	Description	DRAM Timing					
–	SR1F[5:0] (hex)	19	1B	1C	1E	20	22
–	MCLK frequency (MHz)	44.7	48.3	50.1	53.7	57.3	60.9
–	MCLK Period (ns)	22.3	20.7	20.0	18.6	17.5	16.4
25-t_1	t_{ASR}: Address setup to RAS*	25	22	21	19	17	16
25-t_2	t_{RAH}: Row Address hold	29	26	25	23	21	20
25-t_3	t_{ASC}: Address setup to CAS*	19	18	17	16	15	13
25-t_4	t_{CAH}: Column Address hold	22	21	20	19	18	16
25-t_5	t_{RCD}: RAS* to CAS* (Standard RAS*)	48	44	42	39	36	34
25-t_5	t_{RCD}: RAS* to CAS* (Extended RAS*)	67	62	60	56	52	49
25-t_6	t_{RAS}: RAS* pulse width (Standard RAS*)	78	72	70	65	61	58
25-t_6	t_{RAS}: RAS* pulse width (Extended RAS*)	88	82	79	74	69	65
25-t_7	t_{RP}: RAS* precharge (Standard RAS*)	54	50	48	45	42	39
25-t_7	t_{RP}: RAS* precharge (Extended RAS*)	66	61	58	54	51	48
25-t_8	t_{CAS}: CAS* pulse width	25	24	23	22	21	19
25-t_9	t_{CP}: CAS* precharge	16	15	14	13	12	10
25-t_{10}	t_{RC}: Random cycle (Standard RAS*)[a]	134	124	120	112	105	99
25-t_{10}	t_{RC}: Random cycle (Extended RAS*)	156	145	140	130	122	115
25-t_{11}	t_{PC}: Page-mode cycle	45	41	40	37	35	33
26-t_1	Read data setup to CAS* high	0	0	0	0	0	0
26-t_2	Read data hold from CAS* high	10	10	10	10	10	10
26-t_3	RAS* active to data valid (Standard RAS*)	88	82	79	74	69	65
26-t_3	RAS* active to data valid (Extended RAS*)	100	92	89	83	78	73
26-t_4	Column Address valid to data valid	45	41	40	37	35	33
26-t_5	CAS* active to data valid	25	24	23	22	21	19
26-t_6	CAS* precharge to data valid	45	41	40	37	35	33

Table B7-17. DRAM Timing Parameter Equations Evaluated (Not EDO Timing) *(cont.)*

Table/ Parameter	Description	DRAM Timing					
27-t_1	t_{CWL}: WE* setup to CAS*	23	21	21	19	18	17
27-t_2	t_{DS}: Write data setup to CAS*	20	19	18	17	16	14
27-t_3	t_{DH}: Write data hold from CAS*	23	22	21	20	19	17
27-t_4	t_{WCH}: WE* active hold	32	29	28	26	24	23
–	t_T: Transition	2	2	2	2	2	2

a. t_{RC} and t_{PC} are provided for reference only.

Table B7-18. DRAM Timing Evaluated: (EDO Timing – CL-GD5436)

Table/ Parameter	Description	EDO DRAM	
–	SR1F[5:0] (hex)	25	2D
–	MCLK frequency (MHz)	66.2	80.5
–	MCLK period (ns)	15.1	12.4
28-t_1	t_{ASR}: Address setup to RAS*	14	10
28-t_2	t_{RAH}: Row Address hold	18	14
28-t_3	t_{ASC}: Address setup to CAS*	12	9
28-t_4	t_{CAH}: Column Address hold	15	12
28-t_5	t_{RCD}: RAS* to CAS* (EDO timing)	60	50
28-t_6	t_{RAS}: RAS* pulse width (EDO timing)	75	61
28-t_7	t_{RP}: RAS* precharge (EDO timing)	47	39
28-t_8	t_{CAS}: CAS* pulse width	18	15
28-t_9	t_{CP}: CAS* precharge	9	6
28-t_{10}	t_{RC}: Random cycle (EDO timing)[a]	121	99
28-t_{11}	t_{PC}: Page-mode cycle	30	25
28-t_{12}	t_{CAS}: (last CAS* of Page mode read burst)	45	37
29-t_1	Read data setup to CAS* high	1	1
29-t_2	Read data hold from CAS* high	5	5
29-t_3	RAS* active to data valid (EDO timing)	76	62
29-t_4	Column Address valid to data valid (EDO timing)	45	37
29-t_5	CAS* active to data valid (EDO timing)	30	25
29-t_6	CAS* precharge to data valid (EDO timing)	45	37

a. t_{RC} and t_{PC} are provided for reference only.

To determine what MCLK can be programmed for a given DRAM, compare the numbers in the appropriate table above to the corresponding numbers from the DRAM data sheet. The numbers from the DRAM data sheet must be equal to or smaller than the numbers in the table.

6. MCLK vs. VIDEO MODE REQUIREMENTS

The analysis that follows ignores the requirement for CPU and BLT accesses. It assumes that every bit of display memory bandwidth is available for the exclusive purpose of refreshing the screen. Of course, that leaves only blanking time for screen updates, which will probably result in unacceptable performance.

The above disclaimer aside, the relationship between MCLK and Video modes can be simply stated in a single sentence: ***Data must be put into the CRT FIFO faster than it is taken out.*** If this condition is not met, FIFO underflow will occur and the screen will not be properly refreshed.

The maximum rate at which data (in terms of bytes-per-second) is put into the FIFO is the width of the display memory expressed in bytes multiplied by the MCLK divided by two. This is because a Fast-page cycle fetches one memory width worth of bytes and requires two MCLK cycles.

The rate at which data is removed from the FIFO is the effective number of bytes per pixel multiplied by the pixel rate (pixel rate is the rate at which pixels are put onto the screen, which may not be the same as the value programmed into the synthesizer). The effective number of bytes per pixel is divided by two when AccuPak data is being expanded into YCrCb. When interpolation is being used for vertical zoom, the effective number of bytes per pixel is multiplied by two. The following inequality expresses this. *W* is the *width* of the display memory *data path* in bytes. *B* is the effective *number of bytes per pixel*. *PCLK* is the *Pixel clock*.

$$\frac{W \times MCLK}{2} > B \times PCLK$$

The following equation demonstrates rearranging terms to isolate MCLK.

$$MCLK > \frac{B \times PCLK \times 2}{W}$$

For 'acceptable' performance, MCLK should be at least 1.1 times its calculated minimum. MCLK of at least 1.2 times its calculated minimum will result in 'good' performance.

This information can be expressed in tabular form as in the following two tables. These tables are calculated minimums; the actual values should be adjusted as indicated in the previous equations.

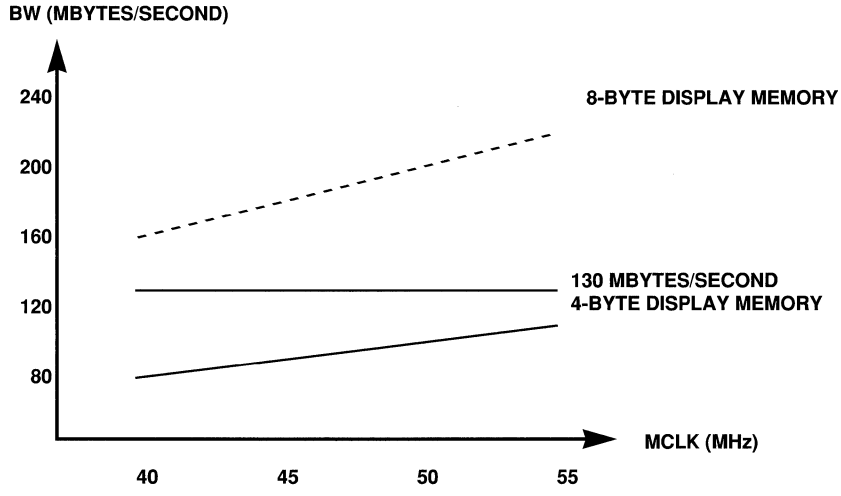
Table B7-19. Minimum MCLK for Text Modes

Display Memory Width	Extended RAS Timing?	Standard 8-Pixel	Standard 9-Pixel	Page Mode 8-Pixel	Page Mode 9-Pixel
32	Yes	.60 VCLK	.54 VCLK	.33 VCLK	.29 VCLK
32	No	.53 VCLK	.48 VCLK	.31 VCLK	.28 VCLK
64	Yes	.30 VCLK	.27 VCLK	.16 VCLK	.15 VCLK
32	No	.27 VCLK	.24 VCLK	.16 VCLK	.14 VCLK

Table B7-20. Minimum MCLK for Graphics Modes

Display Memory Width	4 Bits/Pixel	8 Bits/Pixel	16 Bits/Pixel	24 Bits/Pixel	32 Bits/Pixel
32	.25 VCLK	.50 VCLK	1.0 VCLK	1.5 VCLK	2.0 VCLK
64	.12 VCLK	.25 VCLK	.50 VCLK	.75 VCLK	1.0 VCLK

Consider the case of mode 74 (1024 × 768 × 16 bits/pixel) at 60 Hz refresh. Since the VCLK is 65 MHz and two bytes per pixel are required. The burst rate at which data are removed from the FIFO is 130 Mbytes/second. With a display memory width of 4 bytes, this would require an unlikely MCLK rate of 65 MHz. With a display memory width of 8 bytes, the required MCLK is less than 40 MHz, as shown in the following graph.



7. BANDWIDTH NOTE FOR CL-GD5430/'40 WITH 64-BIT INTERFACE

Although the CL-GD5430/'40 appears to use a 64-bit display memory interface when configured for 2 Mbytes, the bandwidth calculations must be based on a 32-bit interface. This is because the CL-GD5430/'40 has a 32-bit internal bus.

Appendix B8

Dual-Frequency Synthesizer and DAC Current Reference

SYNTHESIZER AND DAC CURRENT REFERENCE

1. INTRODUCTION

This appendix discusses clock options available for CL-GD543X/'4X-based system designs. Additionally, the DAC current reference is covered.

2. MCLK — MEMORY CLOCK

The MCLK synthesizer generates the clock used to drive the display memory state machine, the BitBLT engine, and the host interface state machine. Refer to Appendix B7, "Memory Configurations", to determine an MCLK frequency suitable for specific DRAMs.

2.1 Programming MCLK Frequency

MCLK is directly programmed by writing the value into SR1F[5:0] that most nearly corresponds to the desired frequency.

$$MCLK = SR1F \bullet \left(\frac{Reference}{8} \right)$$

Table B8-1 shows representative examples assuming a reference clock of 14.31818 MHz. Before programming any frequency, check the specification of the specific VGA chip.

Table B8-1. MCLK Programming

SR1F[5:0] (decimal)	SR1F[5:0] (hex)	MCLK Frequency	SR1F[5:0] (decimal)	SR1F[5:0] (hex)	MCLK Frequency
28	1C	50.1 MHz	37	25	66.2 MHz
29	1D	51.9 MHz	38	26	68.0 MHz
30	1E	53.7 MHz	39	27	69.8 MHz
31	1F	55.5 MHz	40	28	71.6 MHz
32	20	57.3 MHz	41	29	73.4 MHz
33	21	59.1 MHz	42	2A	75.2 MHz
34	22	60.9 MHz	43	2B	77.0 MHz
35	23	62.6 MHz	44	2C	78.7 MHz
36	24	64.4 MHz	45	2D	80.5 MHz

2.2 Power-on MCLK Frequency

The CL-GD543X/'4X (excepting the CL-GD5436) has two default MCLK frequencies. At reset, the value on the MD56 is loaded into Configuration register bit 8. See Appendix B9 for information regarding configuration logic. Table B8-2 shows the default frequencies. The default MCLK frequency for the CL-GD5436 is always 50.1 MHz. The MCLK default frequency is immediately overwritten by the Cirrus Logic BIOS at POST time.

Table B8-2. MCLK Default Frequencies

MD56	Pulldown on MD56	Default MCLK (MHz)
0	Yes	50.1
1	No	41.1

3. VCLK — VIDEO CLOCK

3.1 VCLK Source

VCLK is the fundamental video timing clock in the system. The monitor timing signals (HSYNC and VSYNC) as well as the pixel clock are derived from VCLK. The VCLK source is determined by a number of factors, as indicated in Table B8-3.

Table B8-3. VCLK Source

EDCLK (Pin)	SR1F[6]	SR1E[0]	MISC Register 3C2[3:2]	CRTC Dot Clock (Monitor Timing)	DAC Data Clock (Pixel Timing)
1	0	x	0,0	VCLK0	VCLK0
1	0	x	0,1	VCLK1	VCLK1
1	0	x	1,0	VCLK2	VCLK2
1	0	x	1,1	VCLK3	VCLK3
1	1	0	x	MCLK	MCLK
1	1	1	x	MCLK ÷ 2	MCLK ÷ 2
0	0	x	0,0	VCLK0	DCLK pin
0	0	x	0,1	VCLK1	DCLK pin
0	1	0	0,x	MCLK	DCLK pin
0	1	1	0,x	MCLK ÷ 2	DCLK pin
0	x	x	1,x	DCLK pin	DCLK pin

3.2 VCLK Programming

The four internal VCLK sources can be programmed with two registers each, as indicated in Table B8-4. The Numerator is a 7-bit integer, right justified in the corresponding register. The Denominator is a 5- or 6-bit integer, scaled at bit 1 in the corresponding register. The Postscaler is a single bit at bit position 0 of the corresponding register.

Table B8-4. VCLK0–3 Registers

Clock	Numerator	Denominator/ Post Scalar	Usage Note
VCLK0	SRB	SR1B	Nominal 25 MHz
VCLK1	SRC	SR1C	Nominal 28 MHz
VCLK2	SRD	SR1D	Unused
VCLK3	SRE	SR1E	Extended modes

The parameters for each Video clock determines its frequency according to the following two formulae.

$$VCO = Reference \bullet \left(\frac{N}{D}\right)$$ Post Scaler = 0

$$VCO = Reference \bullet \left(\frac{N}{D \bullet 2}\right)$$ Post Scaler = 1

For the CL-GD5434 only, register SR1B bit 7 enables a denominator extension. If bit 7 of SR1B is programmed to a '1', then bit 6 becomes a high-order extension of the Denominator. This allows finer control of VCLK at lower frequencies, such as broadcast TV standards. The extra precision can assist in minimizing the interaction between the Color-burst signal (usually external and asynchronous) and the Pixel clock.

Typically a large number of numerator/denominator values will program a common frequency. The choice among these combinations is made empirically. Generally, better results will be obtained if the pre-scalar is programmed to '1', especially at lower frequencies.

4. USING MCLK AS VCLK

If the two clocks are programmed to frequencies very close to each other (within about 1%) or to frequencies that are nearly multiples of each other, they might interfere with each other. This can show up as screen 'jitter'. The solution is to shut down the VCLK oscillator and use MCLK (or MCLK ÷ 2) as VCLK. See SR1F. Table B8-5 shows the cases where this could be done. This function is currently not used by the Cirrus Logic BIOS.

Table B8-5. When to Use MCLK as VCLK

MCLK	Video Mode	Nominal VCLK	Note
50.1	64, 66 at 60 Hz	25 MHz	Use MCLK ÷ 2
50.1	58, 5C at 72 Hz	50 MHz	Use MCLK

5. DAC CURRENT REFERENCE: RSet

For Cirrus Logic devices that do not have an integrated DAC current reference, the external current references in the schematics should be used. Beginning with the production revisions in Table B8-6, CL-GD543X/'4X controllers are expected to include an internal current reference. This section discusses the selection of the resistor used to set the full-scale current.

Table B8-6. Anticipated Revisions with Integrated Current Reference

Device	First Production Revision	Note
CL-GD5430		
CL-GD5434		
CL-GD5436	Production A	
CL-GD5440	Production A	(Fab. A)

If the standard VGA levels are required (700 mV full-scale across 37.5 Ω), the ideal value for RSet will be 135 Ω. If another value is chosen, the voltage will scale linearly.

For complete generality, the following three equations may be used.

The first equation is part of the chip specification. It specifies the required resistor value in terms of the desired current reference.

$$RSet = \frac{1.2Volts}{IRef}$$

The second equation is also part of the chip specification. It specifies the current reference in terms of the desired full scale current.

$$IRef = \frac{IFullScale}{(63/30)}$$

The third equations comes from Ohm's Law. The required full-scale current is calculated from the load the DACs are looking into and the desired full-scale voltage.

$$IFullScale = \frac{VFullScale}{Load}$$

Combining these equations yields the following.

$$RSet = \frac{2.52V \bullet Load}{VFullScale}$$

By knowing the DAC load and the desired full-scale voltage, the value of the resistor can be calculated.

Appendix B9

Configuration Notes

CONFIGURATION NOTES

1. INTRODUCTION

When RESET is active, the CL-GD543X/'4X loads the levels on MD[63:48] in 16 internal latches. These latches control some fundamental properties of the device, such as the host bus interface and DRAM configuration. These configuration latches are CF[15:0].

2. CONFIGURATION SUMMARY

Each of the MD[63:48] has an internal pull-up resistor (nominally 250 KΩ). The default (if no pull-down resistor is installed) is '1'. If a '0' is to be loaded into the latch associated with a given MD line, an external pull-down resistor (typically 6.8 KΩ) must be installed. Table B9-1 provides an overview of the Configuration bits. The device description columns indicate the configuration if a pull-down resistor is installed for each of the CL-GD543X/'4X family members.

Table B9-1. CL-GD543X/'4X Configuration Bits

MD Bit	CF Bit	CL-GD5430	CL-GD5440	CL-GD5436	CL-GD5434	Readable At
63	15	Enable Pin Scan				–
62	14	Reserved	PCI3C[8] = 1		Reserved	–
61	13	Reserved	Reserved	3C3[0] = 0	Reserved	–
60	12	Select MCLK output pin source			Disable internal DAC	SRF[0]
59	11	Asymmetric DRAM addressing				–
58	10	Multiple-CAS* DRAM interface				–
57	9	Extended-RAS* timing				SRF[2]
56	8	Default MCLK select		PCI byte swap	Default MCLK	SRF[1]
55	7	64K ROM BIOS				–
54	6	No zero wait		Reserved	16-bit ROM/ no zero wait	–
53	5	External MCLK (test only)				–
52	4	Select POS 102 Access				–
51	3	3C3 setup (VESA VL-Bus)/ IO relocation enable (PCI bus)			3C3 setup	–
50	2	System bus select [2]				SR17[5]
49	1	System bus select [1]				SR17[4]
48	0	System bus select [0]				SR17[3]

3. CONFIGURATION DETAILS

Enable Pin Scan (MD[63]): If no pull-down resistor is installed, the CL-GD543X/'4X will not be put into Pin-Scan mode and will function normally. If a pull-down resistor is installed (or if MD63 is driven low by a tester), the CL-GD543X/'4X will be placed into Pin-Scan mode. See Appendix B13, "Pin Scan".

Reserved (MD[62]) (CL-GD5430/'34): The reserved bits are for future expansion. Pull-down resistors should not be installed on these lines.

PCI Interrupt Request Control (MD[62]) (CL-GD5436/'40 only): If no pull-down resistor is installed, PCI3C[8] will be '0'. The PCI interrupt will not be requested and the INTR pin must not be connected. If a pull-down resistor is installed, PCI3C[8] will be '1'. The PCI interrupt will be requested.

Reserved (MD[61]) (CL-GD5430/'34/'40): The reserved bits are for future expansion. Pull-down resistors should not be installed on these lines.

Reset State of 3C3[0] (MD[61]) (CL-GD5436): If no pull-down is installed, 3C3[0] will power-up with the value '1'. If no pull-down is installed, 3C3[0] will power-up with the value '0'. This is interesting only if 3C3 is the setup/enable location (see CF3).

Select MCLK Pin Source (MD[60]) (CL-GD5430/'36/'40 only): If no pull-down resistor is installed, MCLK will appear on the MCLK pin if no pull-down is installed on MD[53]. If a pull-down resistor is installed, the internal VCLK VCO will appear on the MCLK pin. This is the VCO before the prescaler. This allows the internal synthesizer to be fed back into the CL-GD5430/'36/'40 on the DCLK pin. This, in turn, allows the setup and hold times on the P-bus to be predicted more accurately.

Disable Internal DAC (MD[60]) (CL-GD5434 only): If no pull-down resistor is installed, the internal DAC is active and will behave normally. Refer to SR17[0] description. If a pull-down is installed, the internal DAC will be disabled. There will be zero output on the R, G, and B lines. There will be no response at 3C6–3C9 (the DAC Addresses), except for the following:

- All DAC writes will be shadowed (that is, they will actually take place without any acknowledgment so that the internal DAC and palette contents will follow an external DAC)
- Reads from 3C7 (DAC State register) are executed normally
- The EROM* pin (pin 33) will be active for I/O Addresses 3C6-3C9 (except reads from 3C7) in addition to memory reads from the ROM page. This allows EROM* to serve as an external DAC chip select. This occurs only when the CL-GD5434 is configured for the VESA VL-Bus.

Asymmetric DRAM Addressing (MD[59]): If no pull-down resistor is installed, the DRAM Row and Column Addresses will be on MA[8:0]. If a pull-down resistor is installed, the DRAM Row Address will be on MA[9:0] and the DRAM Column Address will be on MA[8:1]. This is for asymmetric 256K × 16 devices. See the DRAM configuration tables in Appendix B7, "Memory Configurations".

Multiple-CAS* DRAM Interface (MD[58]): If no pull-down resistor is installed, the CL-GD543X/'4X will be configured for multiple-WE* DRAMs. This should only be used if dual-WE* 256K × 16 devices are being used. If a pull-down resistor is installed, the CL-GD543X/'4X will be configured for dual-CAS* DRAMs. This should be used for all 256K × 4, 256K × 8, and 256K × 16 devices with dual-CAS* inputs.

Extended-RAS* Timing (MD[57]): If no pull-down is installed, normal DRAM timing will be used. A Random cycle will require six MCLK periods; a Fast-page Mode cycle will require two MCLK periods. If a pull-down resistor is installed, extended DRAM timing will be used. A Random cycle will require seven MCLK periods; a Fast-page Mode cycle will require two MCLK periods. See Appendix B7 for detailed information on DRAM configuration and timing. For the CL-GD5436 only, Extended-RAS* timing must be configured in order to enable EDO timing.

50-MHz MCLK Default (MD[56]) (CL-GD5430/'34/'40): If no pull-down resistor is installed, the power-up MCLK will be 41.2 MHz. If a pull-down resistor is installed, the power-up MCLK will be 50.1 MHz. See Appendix B8 for information regarding other MCLK frequencies. See Appendix B7, "Memory Configurations", for information regarding the DRAM parameters necessary for a particular MCLK. The standard Cirrus Logic BIOS programs the MCLK at POST time and overrides this default. This bit is not supported on the CL-GD5436 and may not be supported in future products.

Enable PCI Byte Swapping (MD[56]) (CL-GD5436 only): If no pull-down resistor is installed, the CL-GD5436 will be configured for a single 4-Mbyte memory aperture. If a pull-down resistor is installed, the CL-GD5436 will be configured for four 4-Mbyte byte swapping apertures. This applies only if the CL-GD5436 is configured for the PCI bus. Byte swapping will take place depending on which 4 Mbyte aperture is accessed.

Table B9-2. PCI Byte Swapping (CL-GD5436 only)

Aperture	Swapping
0	None: Byte transfers and 8 BPP modes
1	Swap bytes within each WORD: for 16-bit transfers: {1,2,3,4} becomes {2,1,4,3}
2	Swap all four bytes within a DWORD: {1,2,3,4} becomes {4,3,2,1}
3	Reserved

64K ROM BIOS (MD[55]): If no pull-down resistor is installed, the CL-GD543X/'4X will make EROM* active for memory reads C000:0–C7FF:F. This is correct for the standard 32K Cirrus Logic BIOS. If a pull-down resistor is installed, the CL-GD543X/'4X will make EROM* active for memory reads C000:0–CFFF:F. This is appropriate for a 64K BIOS. If the CL-GD543X/'4X is configured for the PCI bus, this bit has no effect.

16-Bit ROM BIOS (MD[54]) (CL-GD5434 only): If no pull-down resistor is installed, the CL-GD5434 will not return MCS16* for memory reads in the BIOS space (C000:0–C7FF:F or CFFF:F). This is appropriate for a single 8-bit EPROM. If a pull-down resistor is installed, the CL-GD543X/'4X will return MCS16* for memory reads in the BIOS space. This is appropriate for a 16-bit EPROM or two 8-bit EPROMs. This bit is defined as above only for an ISA adapter (CL-GD5434 only).

No Zero Wait (MD[54]) (CL-GD5430/'34/'40 only): If the CL-GD5430/'34/'40 is configured for VESA VL-Bus, this bit is defined as follows. If no pull-down resistor is installed, zero wait writes are supported by the VESA core logic chip set. If a pull-down resistor is installed, zero wait writes are not supported by the VESA core logic chip set. This has no direct effect on the operation of the device; the Cirrus Logic BIOS uses this information to configure itself. See the schematic diagrams in Appendix B3 for connection information for MD[54]. If the CL-GD5430/'34/'40 is configured for the PCI bus, this bit has no effect.

Reserved (MD[54]) (CL-GD5436 only): The reserved bits are for future expansion. Pull-down resistors should not be installed on these lines.

External MCLK (MD[53]): If no pull-down resistor is installed, the MCLK pin will be an output. The source will be the MCLK VCO or the VCLK VCO (CL-GD5430/'40). If a pull-down resistor is installed, MCLK will be an input and an MCLK must be supplied externally. In addition, DCLK will directly reflect the reference 14.3 MHz. This mode is intended for factory testing only.

Select POS 102 Access (MD[52]): If no pull-down resistor is installed, the CL-GD543X/'4X will not respond to I/O accesses at I/O Port Addresses 102 or 94. Bit 3C3[0] enables the video system. If a pull-down resistor is installed, the CL-GD543X/'4X will respond to I/O Port Address 102 only if I/O Port Address 94[5] = 0, and will always respond to I/O Port Address 94. If CL-GD543X/'4X is configured for 46E8 Video Enable, this bit has no effect; 46E8[4] controls accesses to I/O Port Address 102.

3C3 Setup (MD[51]) (ISA, VESA VL-Bus only): If no pull-down resistor is installed, I/O Port Address 46E8 is the Setup/Video Enable port. The Select POS 102 Access Configuration bit has no effect. I/O Port Address 56E8, 66E8, and 76E8 also respond as 46E8. See the description of 46E8 in Chapter 4, "External and General Registers". If a pull-down resistor is installed, 3C3 is the Video Enable register. See the description of 3C3 in Chapter 4. This definition applies for ISA and VESA VL-Bus configurations only.

I/O Relocation Enable (MD[51]) (CL-GD5430/'40 only – PCI Bus only): If no pull-down is installed, the I/O relocation described for PCI14 will be disabled. PCI14 will always return the value '0'. If a pull-down is installed, the I/O relocation described for PCI14 will be enabled. PCI14 will initially return the value '00000001'.

Table B9-2 summarizes the defined cases of Configuration bits MD[52:48]. A '0' means a pull-down is installed; a '1' means a pull-down is not installed. Reserved cases are not in this table. This table is for ISA and VESA VL-Bus configurations only. PCI has special registers (refer to Chapter 4).

Table B9-3. Configuration Bits MD[52:48] (ISA and VESA® VL-Bus™ only)

MD[52]	MD[51]	MD[50:48]	Video Enable	I/O Port Address 102 Access	Note
0	0	1,1,1	3C3[0] = 1 and 102[0] = 1 and 94[5] = 1	94[5] = 0	ISA motherboard
1	0	1,1,1	3C3[0] = 1	n/a	ISA motherboard
x	1	1,1,1	46E8[3] = 1 and 102[0] = 1 and 46E8[4] = 0	46E8[4] = 1	ISA adapter
0	0	1,1,0	3C3[0] = 1 and 102[0] = 1 and 94[5] = 1	94[5] = 0	VESA VL-Bus motherboard

Table B9-3. Configuration Bits MD[52:48] (ISA and VESA® VL-Bus™ only)

MD[52]	MD[51]	MD[50:48]	Video Enable	I/O Port Address 102 Access	Note
1	0	1,1,0	3C3[0] = 1 and 102[0] = 1 and 94[5] = 1	94[5] = 0	VESA VL-Bus motherboard
x	1	1,1,0	46E8[3] = 1 and 102[0] = 1 and 46E8[4] = 0	46E8[4] = 1	VESA VL-Bus adapter

System Bus Select [2:0] (MD[50:48]): These three Configuration bits specify the host bus that is connected to CL-GD543X/'4X. See the schematics in Appendix B3 for connector information for MD[50].

Table B9-4. Configuration Bits MD[50:48] System Bus Select

MD[50]	MD[49]	MD[48]	CL-GD5430/'36/'40	CL-GD5434
0	0	0	Reserved	Reserved
0	0	1	Reserved	Reserved
0	1	0	VESA VL-Bus at > 33 MHz	VESA VL-Bus at > 33 MHz
0	1	1	Reserved	Reserved
1	0	0	PCI	PCI
1	0	1	Reserved	Reserved
1	1	0	VESA VL-Bus at ≤ 33 MHz	VESA VL-Bus at ≤ 33 MHz
1	1	1	Reserved	ISA

Appendix B10

CL-GD5440 NOTES

CL-GD5440 NOTES

1. INTRODUCTION

This appendix discusses features unique to the CL-GD5440 and is written for the reader who is familiar with the Cirrus Logic CL-GD543X or CL-GD542X family of graphics controllers. Four topics are discussed in this appendix: the hardware video window, video playback from display memory, video playback from the video port, and video capture.

The CL-GD5440 is upward compatible with the CL-GD5430, and supports its overlay functions as described in Appendix B14.

2. HARDWARE VIDEO WINDOW

The CL-GD5440 supports a hardware video window. This is a single, rectangular window intended for displaying video that is live or being played back from a file.

2.1 Position on the Screen

The location and size of the window on the screen is programmed into a number of registers as indicated in Figure B10-1.

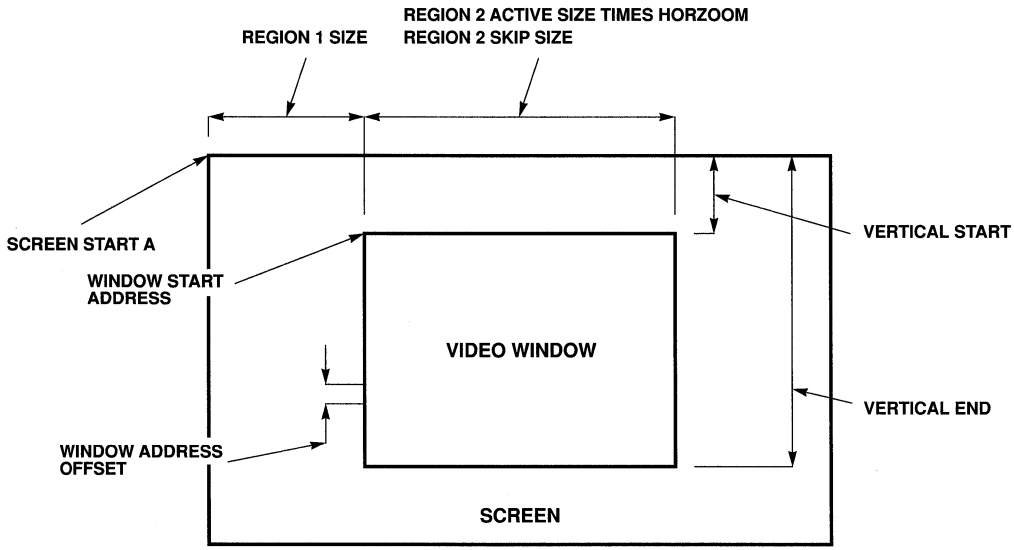


Figure B10-1. Screen Positioning

B7-1 summarizes the programming of the parameters of the window.

Table B10-1. Window Positioning Parameters

Register	Name	Address	Function
Horizontal Region 1 Size	HR1SZ	CR33/36	Screen size to the left of the video window
Horizontal Region 2 Skip Size	HR2SSZ	CR34/36	Offset in display memory for the video window (distance in DWORDs across the window)
Horizontal Region 2 Active Size	HR2ASZ	CR35/36	Size of the video window
Vertical Start	VWVS	CR37/39	First scanline of the video window
Vertical End	VWVE	CR38/39	Last scanline of the video window
Window Start Address	WSA	CR3A/B/C	Address of top left pixel in video window
Window Address Offset	WAO	CR3C/D	Distance in display memory between vertically adjacent pixel within video window

The vertical position and size of the window are programmed in terms of absolute scanline numbers. Vertical Start is programmed to the first scanline of the window and Vertical End is programmed to the last scanline of the window.

The horizontal position and size are programmed in terms of DWORDs fetched from display memory and placed into the CRTC FIFOs. Figure B10-2 shows a typical scanline within a window.

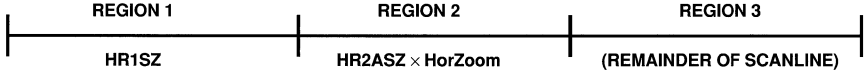


Figure B10-2. Scanline Width

Each scanline in the window begins with a Region 1, at the left of the screen. DWORDs of graphics data are fetched from display memory and placed into the CRT FIFO until HR1SZ has been fetched. The number of pixels filled on the left of the scanline (which is numerically equal to the position of the first pixel in the window) can be calculated with the following formula.

$$Region1Pixels = \left(\frac{32}{R1BitsPerPixel}\right) \bullet HR1SZ$$

Since the hardware counts DWORDs rather than pixels, it is necessary to correct for the number of pixels-per-DWORD. The first element in the equation above does this. This element also places restrictions on the position of the left edge of the window. For example, for the case of 16 bits per pixel, the window can begin only on even-numbered pixels.

If HR1SZ is programmed to '0', there is a zero-width Region 1, and the window begins at the left edge of the screen.

Each scanline in the window continues with a Region 2. The number of pixels occupied by Region 2 depends on HR2ASZ and the horizontal zoom factor.

$$Region2Pixels = \left(\frac{32}{R2BitsPerPixel}\right) \bullet HR2ASZ \bullet HorZoomFactor$$

Since HR2ASZ is a count of DWORDs, it is necessary to correct for the number of pixels in a DWORD. The Horizontal Zoom Factor (see section 2.4 on page 5) can accept values from 1 to 4 inclusive. It is also a factor in the number of pixels in Region 2. As the HorZoomFactor is increased, for example, from 1× to 4×, the actual width of the displayed window on the screen increases proportionally.

At the end of Region 2, the right edge of the window has been reached and background data are again presented. The display memory fetch hardware skips HR2SSZ DWORDs to account for the pixels that are overlaid and begins fetching data for Region 3. Depending on the sizes of Regions 1 and 2, there can be a zero-width Region 3.

For scanlines that are not in the video window, HR1SZ and HR2ASZ are both forced to a zero value and the entire line is treated as Region 3.

2.2 Location in Display Memory

Data for the background is fetched beginning at Screen Start A (CRC/CRD with extensions). At the end of each scanline, the address is incremented by the Offset (CR13 with extensions) as usual. HR2SSZ is the number of DWORDs of background information that was not displayed because it was overlaid.

Data for the window is fetched beginning at Window Start Address (CR3A/B/C). At the end of each scanline, the address is incremented by the Window Address Offset (CR3D with extensions).

2.3 Pixel Format

Since the pixel format for the background and the window are specified separately, they can differ (including the number of bits per pixel).

The pixel format for the background is programmed into the HDR (Hidden DAC register). Only the standard 8- and 16-bit-per-pixel modes can be programmed for the background. The pixel format for the window is specified in CR3E[3:1]. B7-2 shows the formats that can be used.

Table B10-2. Pixel Format in the Window

CR3E[3:1]	Format	Note
000	YCrCb 4:2:2	Excess 128 Cr, Cb
001	AccuPak™	Encoded from YCrCb, Excess 128 Cr, Cb
010	Reserved	
011	RGB AccuPak™	Encoded from RGB
100	RGB 5-5-5	
101	RGB 5-6-5	
110	YCrCb 4:2:2	2's complement Cr, Cb
111	AccuPak™	Encoded from YCrCb, 2's complement Cr, Cb

2.4 ZOOM!

The data in the window can be continuously zoomed from 1× through 4×. Vertical and horizontal zooming are independent. B7-3 summarizes the zoom features of the CL-GD5440. There are some restrictions; see B7-4.

Table B10-3. Zooming: A Summary

Feature	Horizontal	Vertical
Zoom control	CR31	CR32
Zoom factor	1–4×, continuous	1–4×, continuous
Generated display elements	Interpolation	Interpolation or replication
Window size changes with zoom factor	Yes	No

The zoom factor for each axis is calculated as follows.

$$Zoom = \frac{256}{ZoomControl}$$

The horizontal and vertical zoom controls are programmed in CR31 and CR32, respectively. Values in the range 255 through 64 can be programmed, yielding zooms of slightly greater than 1 through 4. A value of 0 sets 1× (zooming is effectively turned off).

Zooming is accomplished by generating pixels or scanlines displayed between those from the source image.

For horizontal zooming, the pixels are generated by interpolation between source pixels. The window width is increased to accommodate generated pixels.

For vertical zooming, scanlines are generated either by interpolation or scanline replication (CR3E[4]). The height of the window is directly programmed into VWVS and VWVE; scanlines at the bottom of the source area are discarded to make room for generated scanlines.

Up to full screen zooming is available for the resolutions shown in B7-4.

Table B10-4. Full Screen Zoom Availability

Resolution	X-Zoom	Y-Zoom	AccuPak™	16-bit RGB	16-bit YCrCb
640 × 480, 256 colors	Interpolation	Interpolation	✔	✔	✔
640 × 480, 64K colors	Interpolation	Rep, Int [a]	✔	✔	✔
800 × 600, 256 colors	Interpolation	Rep, Int [a]	✔	✔	✔
800 × 600, 64K colors	Interpolation	Rep, Int [a]	✔	✔	✔
1024 × 768, 256 colors	Interpolation	Rep, Int [a]	✔		

a. Replication at zoom factor less than 2× (due to limited memory bandwidth), interpolation at or above 2×.

2.5 Additional Window Controls

CR3E[0] is the Master Enable for the hardware video window. If this bit is programmed to a '0', there will be no window. If this bit is programmed to a '1', the window is enabled and is displayed as programmed into the parameter registers.

CR3E[6] is the Window Blank Enabled. If this bit is programmed to a '1', the window is forced to black. If this bit is programmed to a '0', the window displays video normally.

3. VIDEO PLAYBACK

The CL-GD5440 supports AccuPak™ or YCrCb video playback, either stored in memory or directly from the P-bus. This section covers video playback from memory.

If the video data is 15- or 16-bit-per-pixel RGB or YCrCb, the AccuPak decoder is bypassed. The format of the video data is specified in CR3E[3:1], as indicated in B7-5.

Table B10-5. Video Format: CR3E[3:1]

CR3E[3:1]	Format	Note
000	YCrCb 4:2:2	AccuPak™ decoder bypassed, excess 128 Cr, Cb
001	AccuPak™	Use if AccuPak™ is encoded from excess 128 Cr, Cb
010	Reserved	
011	RGB AccuPak™	Use if AccuPak™ is encoded from RGB
100	RGB 5-5-5	AccuPak™ decoder bypassed
101	RGB 5-6-5	AccuPak™ decoder bypassed
110	YCrCb 4:2:2	AccuPak™ decoder bypassed, 2's complement Cr, Cb
111	AccuPak™	Use if AccuPak™ is encoded from 2's complement Cr, Cb

3.1 Chrominance Interpolator

The chrominance interpolator accepts 16-bit YCrCb or RGB pixels from the AccuPak block. For YCrCb pixels, a linear interpolation is performed to generate a 24-bit YCrCb output. RGB pixels are reformatted to produce 24-bit RGB pixels. This block is programmed by CR3E[3:1].

3.2 Y Interpolator

The Y interpolator uses a bi-linear interpolation that picks the weighting that is closest to the "ideal" pixel output. The weighting will be chosen from the following possibilities.

Table B10-6. Vertical Zooming

1	Ln
2	$\left(\frac{3}{4} \bullet Ln\right) + \left(\frac{1}{4} \bullet L(n+1)\right)$
3	$\left(\frac{1}{2} \bullet Ln\right) + \left(\frac{1}{2} \bullet L(n+1)\right)$
4	$\left(\frac{1}{4} \bullet Ln\right) + \left(\frac{3}{4} \bullet L(n+1)\right)$
5	L (n + 1)

3.3 X Interpolator

The X interpolator uses a bi-linear interpolation that picks the weighting that is closest to the "ideal" pixel output. The weighting will be chosen from the following possibilities.

Table B10-7. Horizontal Zooming

1	Pn
2	$\left(\frac{3}{4} \bullet Pn\right) + \left(\frac{1}{4} \bullet P(n+1)\right)$
3	$\left(\frac{1}{2} \bullet Pn\right) + \left(\frac{1}{2} \bullet P(n+1)\right)$
4	$\left(\frac{1}{4} \bullet Pn\right) + \left(\frac{3}{4} \bullet P(n+1)\right)$
5	P(n + 1)

3.4 YCrCb-to-RGB Matrix

The color conversion uses the standard equations for CCIR (International Radio Consultive Committee) 601 YCrCb-to-RGB conversion.

4. VIDEO PORT

This section discusses the CL-GD5440 CDX video port. This feature allows the CL-GD5440 to display video from the existing feature connector at up to 16 bits per pixel. The external device must be synchronized to the CL-GD5440.

4.1 Data Formats

The video port accepts and can display data in the formats shown in B7-8.

Table B10-8. Data Formats

Format	Byte Order	Note
YCrCb	Cb0, Y0, Cr0, Y1...	Pixels 0, 1
RGB 5-6-5	P[7:0] = G[4:2] B[7:3], P[7:0] = R[7:3] G[7:5]	
RGB 5-5-5	P[7:0] = G[5:3] B[7:3], P[7:0] = d/c R[7:3] G[7:6]	
AccuPak™	AP[7:0], AP[15:8], AP[23:16], AP[31:24]	Pixels 0:3

4.2 Video Port Controls

The video port is enabled, and the transfer mode is controlled with bit fields in CR1E. Bits 1 and 0 are used to enable the video port, as shown in B7-9. When the CR1E[1:0] field is programmed to '01', CL-GD5520 video overlay is selected.

Table B10-9. Video Port Configuration: CR1E[1:0]

CR1E[1:0]	Configuration	Handshake	Clock In	Clock Out
00	CL-GD5430–compatible	–	–	–
01	Video Overlay (TV Encoder)	BLANK*	–	DCLK
10	Reserved	–	–	–
11	Video Capture	–	–	–

The transfer mode is controlled with the field in CR1E[3:2]. CR1E[1:0] must be programmed for video overlay ('01' or '10'). Three modes are defined, as shown in B7-10.

Table B10-10. Video Port Transfer Mode: CR1E[3:2]

CR1E[3:2]	Transfer Mode	DCLK Source	VGA Pixel Clock Source	Data Rate Ratio: DCLK ÷ Pixel Rate
00	0	VCLK	VCLK	1
01	1	VCLK/2	VCLK	0.5
10	2	2 X VCLK (VCO before post-scalar)	VCLK (VCO after post-scalar)	2
11	Reserved			

4.3 Video Port Horizontal Zooming

When configured for TV encoder input mode, the video port supports continuous horizontal zooming from 1× to 4×. In some cases the zoom factor must be at least 2×. This is because data cannot be supplied across the P-bus at a high enough rate to supply a complete pixel for each pixel time. B7-11 shows the zoom range for the various resolutions and video data formats.

Some entries have the note 'Hi Freq'. These require that data be transferred to the P-bus at a rate greater than 40 MHz. These modes are not usable with a standard feature connector cable.

Table B10-11. Zoom Factors

Graphics Resolution	Dot Clock (VCLK)	Video Data Format	FC Clock (DCLK)	Transfer Mode CR1E[3:2]	Zoom Range	Note
640 × 480	25 MHz	AccuPak™	25 MHz	0	1–4×	
640 × 480	25 MHz	16-bit RGB or YCC	25 MHz	0	2–4×	
640 × 480	25 MHz	16-bit RGB or YCC	50 MHz	2	1–4×	Hi Freq
800 × 600	40 MHz	AccuPak™	40 MHz	0	1–4×	
800 × 600	40 MHz	16-bit RGB or YCC	40 MHz	0	2–4×	
800 × 600	40 MHz	16-bit RGB or YCC	80 MHz	2	1–4×	Hi Freq
1024 × 768	80 MHz	AccuPak™	40 MHz	1	2–4×	
1024 × 768	80 MHz	16-bit RGB or YCC	40 MHz	1	4×	Hi Freq
1024 × 768	80 MHz	AccuPak™	80 MHz	0	1–4×	Hi Freq
1024 × 768	80 MHz	16-bit RGB or YCC	80 MHz	0	2–4×	Hi Freq

4.4 I/O Pins Used for Video Port

The pins shown in B7-12 are used for video port. They retain their normal usage with the exception of BLANK*, which is redefined as a transfer request.

Table B10-12. Video Port Pins

Pin Name	Direction	Description
HSYNC*	Output	Graphics Horizontal Sync used as a start of line indicator
VSYNC*	Output	Graphics Vertical Sync used as a new frame indicator
BLANK*	Output	Video data request
P[7:0]	Input	Video data from external device
DCLK	Output	Video transfer clock. Depending on transfer mode, can be 1×, ½×, or 2× graphics pixel clock.

4.5 Transfer Protocol

When the video window is enabled (see CR3E) and the video port is enabled by programming CR1E[3:2] to 01b, the CL-GD5440 demands video from the external source with the BLANK* pin. Once the video has been stored in the FIFO, it is processed and displayed by the video pipeline exactly as if it had been read from display memory.

At the beginning of each new video line (when HSYNC* is active), the video FIFO in the CL-GD5440 is cleared. If the scanline is within the video window, the video FIFO is pre-filled during the back porch time. The CL-GD5440 makes BLANK* active-high (see Figure B10-3). When the external device samples BLANK* high on the rising edge of DCLK, it must provide a byte of valid data to be sampled by the CL-GD5440 on the next rising edge (see Figure B10-4). There is no handshaking term from the external device; it is assumed that the data is available and will be presented with the correct setup and hold times.

As bytes are assembled into words, they are stored in the appropriate FIFO in the CL-GD5440. When the FIFO becomes nearly full, BLANK* is asserted low to stop the transfer of video from the external device.

When Region 2 is reached in the scanline (that is, when the window is to begin), video data is taken from the video FIFO. When the FIFO becomes not full, BLANK* is asserted high to demand more video (see Figure B10-3). Depending on the transfer mode and horizontal zoom factor, BLANK* is asserted high as necessary to keep the FIFO nearly full.

The external device must transfer the proper number of bytes for each scanline. The CL-GD5440 requests video whenever the FIFO is not full, and almost always requests data (that it will not use) near the end of the window. These extra bytes are discarded when the FIFO is reset at the beginning of the next scanline.

Table B10-13. Video Port Timing (CL-GD5440 only)

Symbol	Parameter	MIN	Units
t_1	Back Porch	16	Pixel clocks

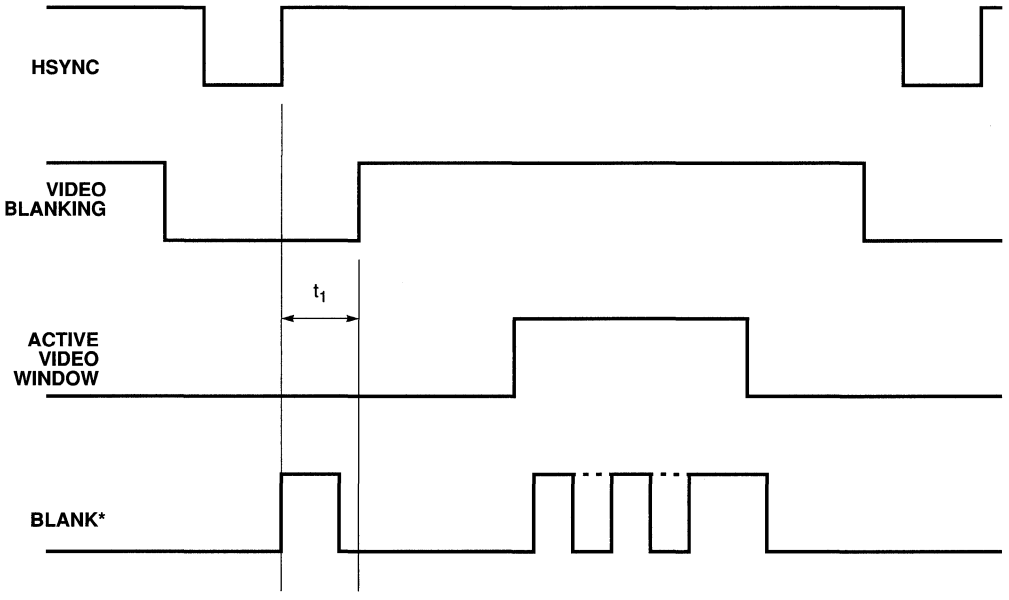


Figure B10-3. Video Port (CL-GD5440 only)

Table B10-14. Video Port Timing: Detail (CL-GD5440 only)

Symbol	Parameter	MIN	MIN	Units
t_1	DCLK period	12	–	ns
t_2	BLANK* delay from DCLK rising edge	–	7	ns
t_3	P[7:0] setup to DCLK rising edge	5	–	ns
t_4	P[7:0] hold from DCLK rising edge	0	–	ns

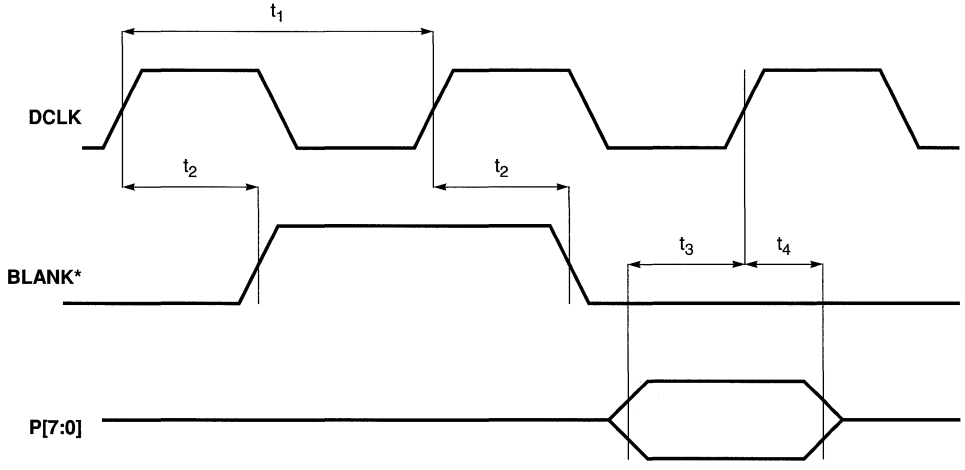


Figure B10-4. Video Port: Detail (CL-GD5440 only)

5. VIDEO CAPTURE

5.1 Features

The CL-GD5440 supports video capture. This feature allows video input on the pixel bus to be written into display memory. The video to be captured can be interlaced or non-interlaced. Closed-caption data may be captured (in non-interlaced mode only).

5.2 Control Bits

The video capture control bits are in register CR1E. A brief definition of the bits involved follows.

7 **Closed Caption Enable:** If video capture is enabled by programming CR1E[1:0] to 1,1, and this bit is programmed to '1', a single scan line of closed caption information is captured at the start of the ODD interlaced field. See section 5.4.3 for additional information.

6 **Interlaced Video:** If video capture is enabled by programming CR1E[1:0] to '1,1', and this bit is programmed to '1', the video capture address controller will operate in interlaced mode. See Memory Addressing.

5 **Field Capture Enable:** If video capture is enabled by programming CR1E[1:0] to '1,1', and this bit is programmed to '1', the field of video data following the next trailing video port vertical sync will be captured. If this bit is programmed to '0', the next field will not be captured.

4 **AccuPak Encode:** If video capture is enabled by programming CR1E[1:0] to '1,1', and this bit is programmed to '1', the data input on P[7:0] will be converted from YUV 4:2:2 to AccuPak format prior to being stored. See Data Formats.

3:2 **Transfer Mode:** If video capture is enabled by programming CR1E[1:0] to '1,1', this field will control the transfer mode for data on P[7:0] with DCLK input.

Table B10-15. Video Capture Transfer Mode

CR1E[3:2]	DCLK Edge(s)	Prescale
00	Rising	Disabled
01	Rising	Enabled
10	Rising and Falling	Disabled
11	Rising and Falling	Enabled

1:0 **Configuration:** This field must be programmed to '1,1' to enable video capture.

In addition, CR3F[7] is a read-only bit that indicates VSYNC* and CR3F[6] can be used to read and control the odd/even field ID.

5.3 I/O Pins Used for Video Capture

The following pins are used for video capture. All except the clock and the pixel bus are re-defined. These pins are all inputs when the CL-GD5440 is programmed for video capture.

Table B10-16. Video Capture Pins

Internal Signal	Pin Name	Pin Number	Description
PIXCLK	DCLK	125	Pixel Clock: Can be programmed as double or single edge.
VSYNC	EDCLK*	123	Active High Vertical Sync
HREF	BLANK*	126	Active High Horizontal Reference: Indicates active video line
VACT	EVIDEO*	120	Active High Video Active: Indicates valid video samples
P[7:0]	P[7:0]	118:115, 113:110	Pixel Data

5.4 Memory Addressing

The address in the display memory is generated by the address controller using the video window start address (CR3A/B/C) and the window address offset (CR3C/D).

5.4.1 Non-interlaced Mode

At the start of each video field, indicated by the leading (rising) edge of the video capture VSYNC input (pin 123), the starting address (CR3A/B/C) is loaded into a start of line address register. This specifies where the captured video will start in display memory.

At the start of each active line, indicated by the first assertion of VACT after a leading edge of HREF, the start of line address is loaded into the video address counter. The start of line address is then incremented by the window address offset (CR3C/D) to point to the start of the next line in display memory. This specifies the distance in display memory between adjacent lines (the PITCH). The video address counter is incremented by one following the transfer of each DWORD of captured data into display memory so that data within any scan line is contiguous.

5.4.2 Interlaced Mode

At the start of each video field, indicated by the leading (rising) edge of the video capture VSYNC input (pin 123), the starting address (CR3A/B/C) is loaded into a start of line address register. For odd fields, the start of line address is incremented by the window address offset (CR3C/D) to point to the second line in the video window. The odd field is indicated by HREF high at the falling edge of VSYNC. This specifies where the captured video will start in display memory.

At the start of each active line, indicated by the first assertion of VACT after a leading edge of HREF, the start of line address is loaded into the address counter. The start of line address is then incremented by two times the window address offset (CR3C/D) to point to the start of next (but one) line in display memory. Thus the data will be captured into every other

scan line of display memory. The video address counter is incremented by one following the transfer of each DWORD of captured data into display memory so that data within any scan line is contiguous.

5.4.3 Closed Caption Mode

The capture of closed caption data is supported for non-interlaced mode only. The closed caption line is assumed to be the first line in the odd video field. The video capture addresses are generated as described above for non-interlaced mode. That is, the video is captured beginning at the window starting address, and each scan line is separated by the window address offset.

When closed caption is enabled, the video display will begin at the second scan line (the window starting address plus the window address offset). This prevents the raw closed caption data from being displayed. When closed caption is enabled, the external NTSC decoder must be programmed to output only odd fields.

5.5 Data Formats

5.5.1 Byte Ordering

The byte ordering for each data type is shown in the following table. Each byte of video data is shown as [msb:lsb].

Table B10-17. Video Capture Data Byte Ordering

Format	Byte Order
RGB 5-5-5	(G0[2:0], B0[4:0]), (d/c, R0[4:0], G0[4:3]), (G1[2:0], B1[4:0]), (d/c, R1[4:0], G1[4:3])
RGB 5-6-5	(G0[2:0], B0[4:0]), (R0[4:0], G0[5:3]), (G1[2:0], B1[4:0]), (R1[4:0], G1[5:3])
YCbCr	(Cb0[7:0]), (Y0[7:]0), (Cr0[7:0]), (Y1[7:0]), (Cb2[7:0]), (Y2[7:]0), (Cr2[7:0]), (Y3[7:0])
AccuPak	(Ap[7:0]), (Ap[15:8]), (Ap[23:16]), (Ap[31:24])

5.6 Transfer Protocol

5.6.1 Single Edge Clocking Mode

Data is sampled on the rising edge of PIXCLK when VACT is HIGH. The beginning of a new line is indicated by HREF going HIGH. VACT is HIGH when valid data is on the pixel bus.

5.6.2 Double Edge Clocking Mode

Data is sampled on the rising edge, and then the immediately following falling edge of PIXCLK when VACT is HIGH. The beginning of a new is indicated by HREF going HIGH. Data must be presented in byte pairs which are sampled on the rising, and then falling, edges of PIXCLK.

5.7 System Notes

The memory sequencer allocates memory cycles with screen refresh as first priority, video capture as second priority, and CPU/BLT cycles as third priority.

The FIFO threshold value in SR16 may have to increase when video capture is enabled, depending on the combination of graphics mode and video capture data rate. CR3C[4] provides for this. Programming guidelines will be provided following characterization of the CL-GD5440.

The video window need not be enabled for video capture to be performed.

Setup and hold times for the video port will be provided following characterization of the CL-GD5440.

HREF setup to PIXCLK

HREF hold from PIXCLK

VACT setup to PIXCLK

HREF hold from PIXCLK

P[7:0] setup to PIXCLK rising edge (single edge clocking mode)

P[7:0] hold from PIXCLK rising edge (single edge clocking mode)

P[7:0] setup to PIXCLK rising edge (double edge clocking mode)

P[7:0] hold from PIXCLK rising edge (double edge clocking mode)

P[7:0] setup to PIXCLK falling edge (double edge clocking mode)

P[7:0] hold from PIXCLK falling edge (double edge clocking mode)

Appendix B11

Signature Generator

SIGNATURE GENERATOR

1. INTRODUCTION

To automatically test the CL-GD543X/'4X display memory and video logic at full speed, Signature Generator logic has been added to the IC. With this feature, it is possible to capture a unique 16-bit signature for any given mode setup and video memory data. An error in the display memory, control logic, or pixel data manipulation logic will produce a signature that will differ from the correct signature. This allows the final test technician to quickly and accurately test a video screen without having to resort to a time-consuming and error-prone visual inspection of the screen. The SG (Signature Generator) is used extensively in the manufacturing test.

To run the SG, register SR18 must be programmed to initialize and arm it. A status bit in SR18 will indicate when the signature is captured and may be read from SR19 and SR1A.

Note that the signature is a function of the displayed pixels, not just the display data. If the display screen includes blinking attributes or a blinking cursor, then the signature will be different for those frames when the pixel is blinked off than when the pixel is blinked on. The SG is intended to be used when blinking is disabled.

2. SR18: SIGNATURE GENERATOR CONTROL

The SG register definitions are as follows:

SR18: Signature Generator Control

D[7:6]	Not associated with the SG
D[5]	Enable Data Generator (factory testing only)
D[4:2]	Pixel Data Select. These three bits select one of the eight Pixel Data bits to use as SG input. 111 = P[7], 110 = P[6]... 000 = P[0]
D[1]	Reset Signature Generator 1 = Reset the SG 0 = Allow the SG to operate
D[0]	Signature Generator Enable/Status 1 = Start generating signature on next VSYNC (write) 0 = SG finished running; signature data ready (read)

NOTE: This bit must be set to start the SG and is automatically cleared when the SG is done.

SR19: Signature Generator Result — low byte

D[7:0] Low byte of the 16-bit result from one video frame of signature data

SR1A: Signature Generator Result — high byte

D[7:0] High byte of the 16-bit result from one video frame of signature data

3. SAMPLE CODE

The following code example in 'C', describes the method a programmer would take to capture eight signatures for any given screen. It is assumed that the screen is already being displayed, and there are no blinking attributes in Text mode.

```
signature_capture ()          /* Capture eight signatures for any mode */
  {
  unsigned int result,i,SR19,SR1A;
  unsigned int SIG [8];

  in.x.ax = 0x0100;           /* shut off the cursor, if in text mode */
  in.x,cx = 0x2000;
  int86x (0x10,&in,&out,&seg);
  outp (0x3c4,6);             /* unlock extended registers */
  outp (0x3c5,0x12);
  for (i = 0;i <= 7; i++) {   /* cycle through all pixel data select bits */
    outp (0x3c4,0x18);        /* arm the SG and set for pixel data bit */
    outp (0x3c5, (2 | (i<<2)));
    outp (0x3c5, (i << 2));
    outp (0x3c4,0x18);
    outp (0x3c5, (1 | (i << 2)));
    result = inp (0x3c5);
    while ((result & 0x01) != 0) {  /* wait until signature is captured */
      outp (0x3c4,0x18);            /* this is actually a requirement*/
      result = inp (0x3c5);
    }
    outp (0x3c4,0x19);        /* get low signature byte */
    SR19 = inp (0x3c5);
    outp (0x3c4,0x1A);        /* get high signature byte */
    SR1A = inp (0x3c5);
    SIG [i] = (SR1A << 8) + SR19;
  }
  }
```

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Appendix B12

Layout Guidelines

LAYOUT GUIDELINES

1. INTRODUCTION

The CL-GD543X/'4X are highly integrated, mixed signal circuits with high operating frequencies. These chips are designed into video subsystems with very high bandwidth buses. Boards based on these controllers will provide a reliable, compact circuit if designed with care.

This appendix distills into a single document the experiences gathered by Cirrus Logic in the course of completing reference designs and in the course of helping customers solve problems.

2. PARTS PLACEMENT AND ADAPTER CARDS

The first consideration is parts placement. This section covers the placement of the Cirrus Logic device. In addition, specific considerations for various adapter cards are covered. Subsequent sections will cover how to place passive devices around the main chip.

2.1 ISA Bus Adapter Card (CL-GD5434 only)

The general parts placement for an ISA adapter should follow the following diagram. The Cirrus Logic device is positioned close to the ISA interface and relatively close to the VGA feature connector.

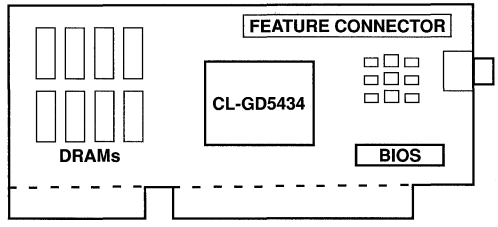


Figure B12-1. ISA Bus Adapter Card Layout

The following considerations apply to adapter boards for ISA bus. RESET and IOCHRDY should be isolated from the system data and system address bus lines to avoid coupling noise into them. This can be done by placing them on the other side of a multi-layer board, or by using ground lines as shields. The layout should provide for an π RC filter on RESET, placed close to the CL-GD5434.

While Cirrus Logic recommends the exclusive use of multilayer boards for all our controllers, it is recognized that economic pressure may drive some vendors to a two-layer board. A layout based on a two-layer board should provide for RC filters for RESET, IOR*, IOW*, MEMR*, and MEMW*. These filters should be close to the CL-GD5434. It may be necessary to provide termination resistors for SD[7:0]. These should be Thevinin equivalents with 330 Ω to VCC and 470 Ω to ground. A single 10-pin SIP contains the eight terminators required for eight data lines.

2.2 VESA® VL-Bus™ Adapter Card

Due to the three inch trace maximum imposed by the VESA VL-Bus specification, there is no choice as to positioning of CL-GD543X/'4X controllers on a VESA VL-Bus adapter card. They will have to be very near the VESA connector, even though this means placement far from the DB15 VGA connector. This is shown in the following diagram.

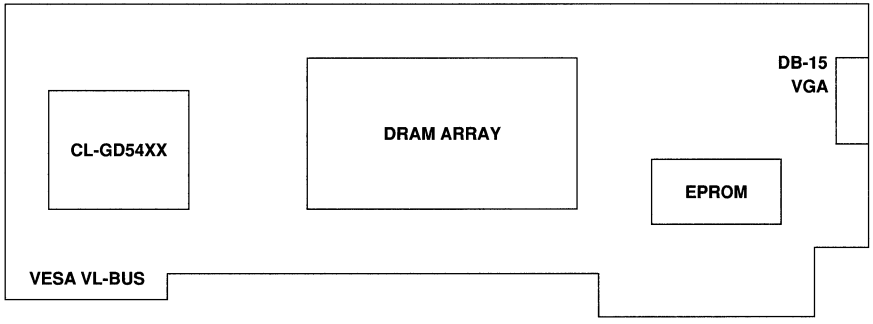


Figure B12-2. VESA® VL-Bus™ Adapter Card Layout

The following considerations apply to adapter boards for the VESA VL-Bus. The CLK signal is critical and special care must be given to its routing. It must be as short as possible and dressed away from other signals that are apt to induce noise. LDEV# is also critical; it must be routed next.

The RGB traces must be designed to have a characteristic impedance of 75 Ω with no vias or sharp turns. These lines must be isolated from the DRAM array, either by being routed around the array or on the other side of the board from the traces going to the array.

For information regarding VESA, please contact:

VESA
2150 North First Street, Suite 440
San Jose, CA, 95131-2029
(408) 435-0333
FAX: (408) 435-8225

2.3 PCI Bus Adapter Card

The requirements of the PCI specification leave little latitude in the placement of the CL-GD543X/'4X. The reference design places the device near the center of the board with the DRAM array in the upper right portion. The PCI board is much smaller that the VESA VL-Bus board, allowing the device to be placed close to the VGA connector. This is shown in the following diagram.

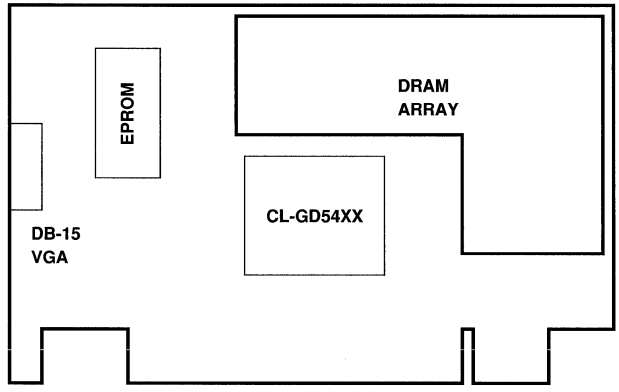


Figure B12-3. PCI Bus Adapter Card Layout

Questions regarding the PCI specification or membership in the PCI Special Interest Group can be forwarded to:

PCI Special Interest Group
M/S HF3-15A
5200 N.E. Elam Young Parkway
Hillsboro, OR, 97124-6497
(503) 696-2000

2.4 Motherboard

Parts placement is as important in a motherboard design as in any adapter card. The Cirrus Logic controller must simultaneously be close to the CPU and the Core Logic, its DRAM array, and the VGA DB15 connector. At the same time, it must be well away from components on the motherboard that could induce noise, such as the main memory, keyboard controller and other peripherals, and the adapter slots.

3. POWER

Cirrus Logic recommends the use of multilayer boards for its components, especially when designed into high performance systems. As frequencies continue to get higher, it becomes less and less likely that one can obtain acceptable results with a two-layer board. One plane must be dedicated exclusively to the distribution of power and one plane must be dedicated exclusively to ground.

There must be cuts in the power plane to completely isolate the three power rails distributed to the Cirrus Logic chip from the VCC on the board and from each other. The following diagram shows how the cuts are made on a typical board.

It can be seen in the following diagram – and in the schematics for the Cirrus Logic Reference designs – that a 1/2-Ω resistor is placed in series between the board VCC and the digital VDD pins of the Cirrus Logic chip (the 1/2-Ω resistor is actually mechanized as two 1-Ω resistors in parallel with each other). This resistor serves as part of an RC filter to isolate the Cirrus chip from noise on the VCC rail, and to provide additional latch-up protection.

Two areas of the power plane must be further isolated. One of these is for AVDD1 (VCLK synthesizer) and one is for AVDD4 (MCLK synthesizer). As shown in the reference designs, these areas are individually further isolated with 33-Ω series resistors that serve as RC filter components.

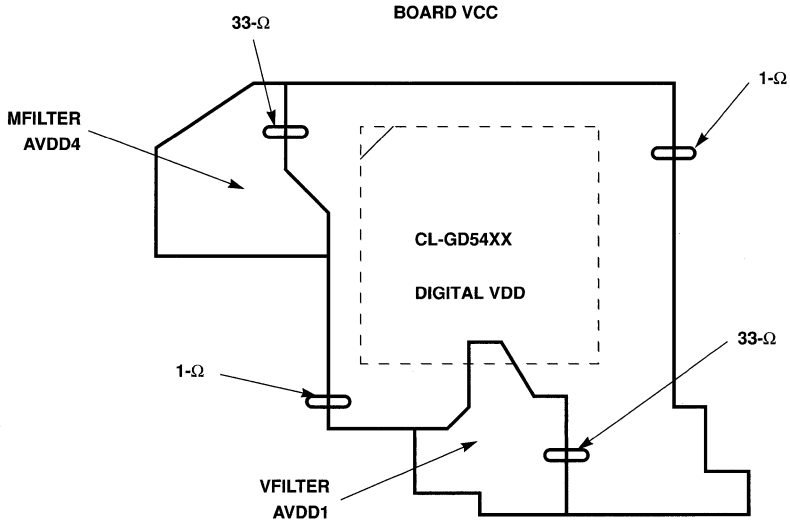


Figure B12-4. Power Plane Layout

4. GROUND

One plane on the board must be dedicated to ground. The ground must have cuts that suppress currents between the various areas (but that do not provide complete isolation). These cuts are shown in the following diagram for a typical reference design.

There is a certain amount of art involved in the exact positioning and size of the cuts in the ground plane and the power plane. Some experimentation may be required to obtain satisfactory results.

The power plane and ground plane cuts must follow each other. It is critical that an isolated ground or power plane not overlay a noisy digital power or ground plane. If such an overlay were allowed, the result would be a capacitor composed of the overlay conductors separated by the relatively thin dielectric between the two pieces of epoxy that make up a four-layer board. Noisy buses (such as data or address) must not be allowed to cross any isolated area.

The ground cuts must not interfere in any way with the return currents between the controller and the DRAM array. Any ground differential between the controller and the DRAM array will directly subtract from the TTL margins.

Cirrus Logic can provide reference designs of adapter cards for various adapter cards which yield satisfactory results and pass FCC Class B emission tests.

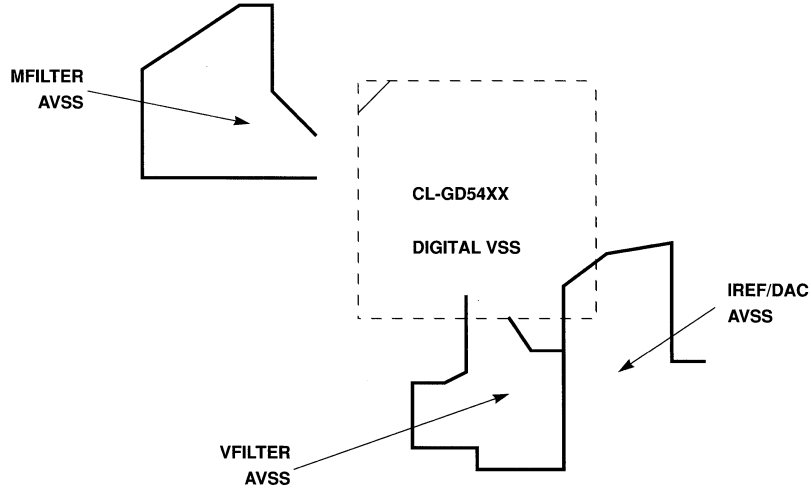


Figure B12-5. Ground Plane Layout

Designers with prior experience using discrete RAMDACs and clock sources may have found that such care with power distribution and isolation was not necessary, especially at relatively low frequencies. The integrated solution available from Cirrus Logic, operating at high frequencies, has changed this, making these precautions necessary.

5. DECOUPLING CAPACITORS

The CL-GD543X/'4X devices operate at high frequencies (up to 135 MHz). Adequate power decoupling is absolutely crucial to a successful design. Each power pin on the device must have a 0.1-μF capacitor returned to the local ground. These capacitors must be placed as closely to the respective power pins as possible. These capacitors must have excellent high frequency characteristics; Cirrus Logic has found the surface mount ceramic chip capacitors perform adequately.

The high frequency capacitors for AVDD must be on the power pin side of the respective 33-Ω resistors, must be as close as possible to the power pin, and must be returned to the appropriate local ground.

The board design must include adequate bulk bypassing. Tantalum capacitors will serve this function. The high frequency characteristics of the bulk bypass capacitors is not as critical as that of the high frequency capacitors.

6. SYNTHESIZER FILTERS

The two synthesizer filter pins, MFILTER and VFILTER, must each be connected to a π RC filter as shown in the reference schematic designs. The filter components, especially the input capacitor and the resistor, must be located as closely to the respective filter pins as possible. The capacitors must be returned to the appropriate AVSS. The traces to the filter pins should be wide (25 mil.).

Some CL-GD543X/'4X controllers have on-chip synthesizer filters. These devices require a resistor from VFILTER to AVSS1. These chips include an on-chip oscillator and so can use a 14.3 MHz crystal as the reference. This crystal is connected between MFILTER and XTAL. The connections to the crystal should be short and direct.

7. IREF CIRCUITRY

The current reference to the DAC (IREF) should be generated using the LM334 circuit shown in the reference designs. The components must be returned to DAC/IREF section of ground plane shown in the previous diagram. A capacitor, on the order of 0.1 μF between IREF and AVDD, may be necessary to suppress noise in some layouts. Provisions should be made for such a capacitor. During system evaluation the decision can be made as to whether to use the capacitor and if so, its exact value.

Some Cirrus Logic controller have an on-chip current reference. These devices require a capacitor from IREF to AVSS[3:2].

8. RGB LINES

The RGB traces are likely to be fairly long, especially on a VESA-VL adapter card. The rise and fall times on these traces are going to be in the order of 2–4 ns, causing them to behave as transmission lines. This means that the characteristic impedance must be controlled and must be close to the nominal monitor termination value of 75 Ω.

There must be π LC filters on each of the RGB lines, as shown in the reference designs. The recommended component values are 10 pF for the capacitors. The inductor is a ferrite bead, with 10–20 Ω impedance at 100 MHz.

There is a trade-off involved in the selection of these component values. Obtaining crisp video on the screen requires that the rise and fall times be as short as possible. However, to obtain acceptable emissions testing results, one would like relatively slow rise and fall times. As the pixel rates get higher and higher, there will be less margin between these two conflicting requirements. The component values recommended above represent our recommendation as of the time of this writing. The filter components must be placed as closely as possible to the VGA DB15 connector.

A 75-Ω resistor to AVSS is specified for each of the RGB lines. These resistors must be placed as closely to the CL-GD543X/'4X as possible.

9. DRAM ARRAY

The DRAMs in display memory typically operate as fast as or faster than those in the system memory. The layout of this array must be given as much consideration as that of the system memory. The following general rules apply.

The devices should be placed close to the CL-GD543X/'4X. In addition, they must be organized so that each individual device is close to the respective MD pins on the controller. The pin-outs on the controller were carefully optimized to allow this.

The control lines must be treated as the fast, heavily loaded lines they are. Relatively wide traces must be used (8 to 10 mil. is typical) and they must be adequately spaced. Placing the traces on 25 mil. centers would be ideal. Avoid long parallel runs.

Provisions should be made for damping resistors to minimize noise in the array. The damping resistors must be placed at the controller end of the lines.

10. DCLK LINE TO FEATURE CONNECTOR

Provisions should be made to insert a resistor or inductor in the DCLK line to the feature connector. This may prove to be very useful in emissions testing.

Appendix B13

Pin Scan

PIN SCAN

1. INTRODUCTION

Pin-Scan testing is a technique for verifying that an IC has been properly soldered to a circuit board. Any IC signal pin that is not connected to the board, or that is shorted to any neighboring pin or trace, can be detected using this technique. The advantage of Pin-Scan testing is that the test patterns to verify full board connectivity are much simpler than would otherwise be possible. The pins are connected sequentially around the IC in a single chain, so that the value on each output pin depends only on the values applied to other pins, rather than the internal state of the VGA processor. In addition, the Pin-Scan logic is strictly combinatorial, so no clock pulses are required.

The first pin in the chain is an input pin; the last pin is an output pin. Each input signal is exclusive-OR'ed (XOR'ed) with the scan data from its lower-numbered neighboring input or output pin. The result of this XOR is passed to its higher-numbered neighbor. Each output pin will be driven with the value passed from its lower-numbered neighbor; that value is inverted and passed to its higher-numbered neighbor.

2. TEST METHOD

In Pin-Scan mode, the test program begins by driving all the input pins to '1', and verifying that the output pins match the values shown in the table that follows. On subsequent cycles, the program drives each input pin, one at a time, to '0' and verifies that all the 'down-stream' outputs match the values shown. In each case, the output is inverted from the value for the all-zeroes case.

If the value applied to an input pin is changed and the 'down-stream' output pins do not change, then that input is shorted or not soldered. If any single output is wrong, then it is either shorted or not soldered.

2.1 Entering Pin-Scan Mode

The CL-GD543X/'4X is placed into Pin-Scan mode by making RESET* low for at least 20 ns while MD63 is low, then making RESET* high.

2.2 Exiting Pin-Scan Mode

The CL-GD543X/'4X is removed from Pin-Scan mode by making RESET* low with MD63 high.

3. PIN SCAN ORDER

In the following table, the pin names are for VESA VL-Bus. The table indicates the pins that are outputs, and indicates the level to be expected for the two cases of 'all inputs = 1' and 'one upstream input = 0'. When the CL-GD543X/'4X is configured for ISA bus or PCI bus, a few pins are no-connects.

Table B13-1. Pin Scan Order

Pin Name	Pin Number	In/Out	All Inputs = 1	1 Input = 0	ISA Note CL-GD5434	PCI Note
BE0#	20	In			RERESH	C/BE0#
BE1#	21	In			SBHE*	C/BE1#
BE2#	22	In			SA0	C/BE2#
BE3#	23	In			SA1	C/BE3#
A2	24	In			SA2	BIOSA0
A3	25	In			SA3	BIOSA1
A4	26	In			SA4	BIOSA2
A5	27	In			SA5	BIOSA3
A6	28	In			SA6	BIOSA4
A7	29	In			SA7	BIOSA5
A8	30	In			SA8	BIOSA6
A9	31	In			SA9	BIOSA7
A10	32	In			SA10	BIOSA8
EROM*	33	Out	0	1		
A11	34	In			SA11	BIOSA9
A12	35	In			SA12	BIOSA10
A13	36	In			SA13	BIOSA11
A14	37	In			SA14	BIOSA12
A15	38	In			SA15	BIOSA13
A16	39	In			LA16	BIOSA14
A17	40	In			LA17	BIOSA15
A18	41	In			LA18	n/c
A19	42	In			LA19	n/c
LCLK	43	In			IOW*	CLK
A20	44	In			LA20	n/c
A21	45	In			LA21	n/c
ADS#	46	In			BALE	FRAME#
RDYR#	47	In			AEN	IRDY#
LOWMEM	48	In			LA22	STOP#
RDY#	49	In			IOCHRDY	TRDY#
HIMEM	50	In			LA23	PAR

Table B13-1. Pin Scan Order *(cont.)*

Pin Name	Pin Number	In/Out	All Inputs = 1	1 Input = 0	ISA Note CL-GD5434	PCI Note
RESET	51	In				RST
W/R#	53	In			IOR*	IDSEL#
D31	54	In			n/c	AD31
D30	55	In			n/c	AD30
D29	56	In			n/c	AD29
D28	57	In			n/c	AD28
D27	58	In			n/c	AD27
D26	59	In			n/c	AD26
D25	60	In			n/c	AD25
D24	61	In			n/c	AD24
D23	62	In			n/c	AD23
D22	63	In			n/c	AD22
LDEV#	65	Out	1	0	MCS16*	DEVSEL#
M/IO#	66	In			MEMR*	LOCK#
D21	68	In			n/c	AD21
D20	69	In			n/c	AD20
D19	70	In			n/c	AD19
D18	71	In			MEMW*	AD18
D17	72	In			IOCS16*	AD17
D16	73	In			IRQ	AD16
D15	74	In			SD15	AD15
D14	75	In			SD14	AD14
D13	76	In			SD13	AD13
D12	78	In			SD12	AD12
D11	79	In			SD11	AD11
D10	80	In			SD10	AD10
D9	81	In			SD9	AD9
D8	82	In			SD8	AD8
D7	84	In			SD7	AD7
D6	85	In			SD6	AD6
D5	87	In			SD5	AD5
D4	88	In			SD4	AD4

Table B13-1. Pin Scan Order *(cont.)*

Pin Name	Pin Number	In/Out	All Inputs = 1	1 Input = 0	ISA Note CL-GD5434	PCI Note
D3	89	In			SD3	AD3
D2	90	In			SD2	AD2
D1	91	In			SD1	AD1
D0	92	In			SD0	AD0
VSYNC	96	In				
HSYNC	98	In				
TWR*	105	In				
EEDI	106	In				
EECS	107	Out	0	1		
OVRW*	109	Out	1	0		
P0	110	In				
P1	111	In				
P2	112	In				
P3	113	In				
P4	115	In				
P5	116	In				
P6	117	In				
P7	118	In				
EVIDEO*	120	In				
ESYNC*	122	In				
EDCLK*	123	In				
DCLK	125	In				
BLANK*	126	In				
MD31	127	In				
MD30	128	In				
MD29	129	In				
MD28	130	In				
MD27	131	In				
MD26	132	In				
MD25	133	In				
MD24	134	In				
CAS3*	135	In				

Table B13-1. Pin Scan Order *(cont.)*

Pin Name	Pin Number	In/Out	All Inputs = 1	1 Input = 0	ISA Note CL-GD5434	PCI Note
MD23	137	In				
MD22	138	In				
MD21	139	In				
MD20	140	In				
MD19	141	In				
MD18	142	In				
MD17	143	In				
MD16	144	In				
CAS2*	145	In				
MD15	147	In				
MD14	148	In				
MD13	149	In				
MD12	151	In				
MD11	152	In				
MD10	153	In				
MD9	154	In				
MD8	155	In				
CAS1*	156	In				
MD63	157	In				
MD62	158	In				
MD61	159	In				
MD60	160	In				
MD59	161	In				
MD58	162	In				
MD57	163	In				
MD56	164	In				
CAS7*	166	In				
WE*	167	In				
RAS1*	168	Out	0	1		
RAS0*/OE*	169	Out	1	0		
MD55	170	In				
MD54	171	In				

Table B13-1. Pin Scan Order *(cont.)*

Pin Name	Pin Number	In/Out	All Inputs = 1	1 Input = 0	ISA Note CL-GD5434	PCI Note
MD53	172	In				
MD52	173	In				
MD51	174	In				
MD50	175	In				
MD49	176	In				
MD48	177	In				
CAS6*	179	In				
MA0	180	Out	1	0		
MA1	182	Out	0	1		
MA2	183	Out	1	0		
MA3	184	Out	0	1		
MA4	185	Out	1	0		
MA5	186	Out	0	1		
MA6	187	Out	1	0		
MA7	188	Out	0	1		
MA8	189	Out	1	0		
MA9	190	Out	0	1		
MD47	191	In				
MD46	192	In				
MD45	193	In				
MD44	194	In				
MD43	196	In				
MD42	197	In				
MD41	198	In				
MD40	199	In				
CAS5*	200	In				
MD39	201	In				
MD38	202	In				
MD37	203	In				
MD36	204	In				
MD35	205	In				
MD34	206	In				

Table B13-1. Pin Scan Order *(cont.)*

Pin Name	Pin Number	In/Out	All Inputs = 1	1 Input = 0	ISA Note CL-GD5434	PCI Note
MD33	207	In				
M32	2	In				
CAS4*	3	In				
CAS0*	4	In				
MD7	5	In				
MD6	6	In				
MD5	7	In				
MD4	8	In				
MD3	9	In				
MD2	10	In				
MD1	11	In				
MD0	12	In				
MCLK	16	in				
INTR	19	Out	1	0	0WS	INTR

A few pins are not accessible in the pin scan; these are listed in the table below. These pins are all analog rather than digital.

Table B13-2. Non-Scanned Pins

Pin Name	Number
MFILTER	14
OSC	17
VFILTER	94
BLUE	100
GREEN	101
RED	102

Appendix B14

Video Overlay and DAC Mode Switching

VIDEO OVERLAY AND DAC MODE SWITCHING

1. INTRODUCTION

This appendix describes the Video Overlay and DAC Mode Switching functions available on the CL-GD543X family. The advanced windowing and video playback features of the CL-GD5440 are covered in Appendix B10.

2. OVERVIEW

Video Overlay and DAC Mode Switching are terms that refer to displaying pixels from an external source in place of pixels in display memory, or to changing the DAC mode (the mode in which data are interpreted in the DAC and displayed), or both.

2.1 Block Diagram

The block diagram in Figure B14-1 may be used to follow the data and control signals through the following descriptions.

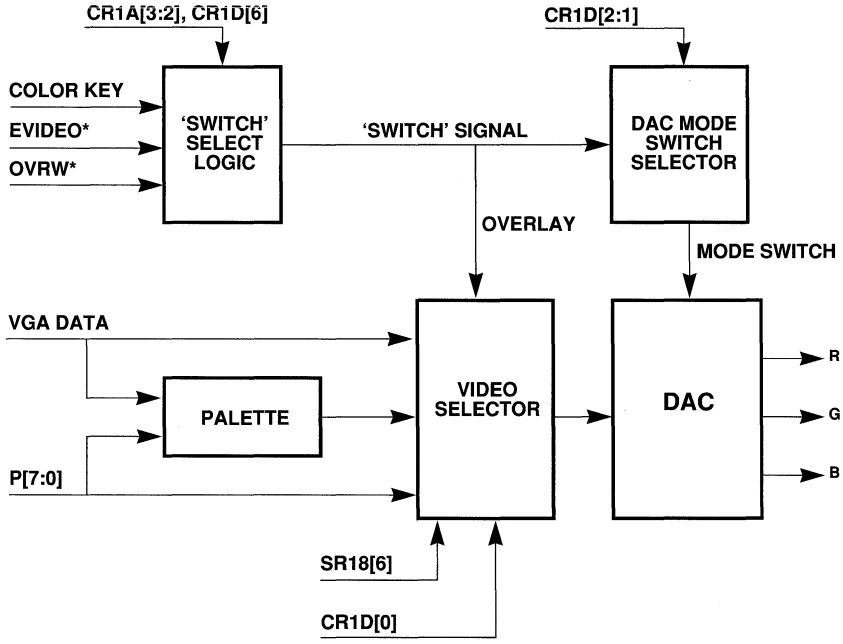


Figure B14-1. Mode Switching

2.2 SWITCH: Which Pixels are chosen

The Switch signal determines which pixels are chosen to be overlayed or to be displayed in an alternate DAC mode. This can take place on a pixel-by-pixel basis. The source of the Switch signal is controlled by register bits CR1A[3:2] and CR1D[6]. There are three major cases.

Timing: The Switch signal can come from the EVIDEO* pin or the internally generated OVRW* signal (for the CL-GD5430/'36/'40 only). This selection method is called *timing*. This method allows pixels to be chosen according to their position on the screen.

Key: The Switch signal can be generated with the Color Key Compare logic. This selection method is called *key*. This method allows pixels to be chosen according to their color without regard to their position on the screen.

Timing AND Key: The Switch signal can be generated with the AND of the timing signal (either EVIDEO* or OVRW*) and the output of the Color Compare logic. This method allows both the color and position of a pixel to be considered.

The following table enumerates the cases that are covered in this appendix.

Table B14-1. Choosing 'Switch'

CR1A[3]	CR1A[2]	CR1D[6]	Source of Switch	EVIDEO*
0	0	X	VGA-compatible Operation: Switch Disabled	Input
0	1	0	EVIDEO* pin	Input
0	1	1	OVRW* signal CL-GD5430/'36/'40 only	Input
1	0	0	EVIDEO* pin AND'ed with Color Key Compare	Input
1	0	1	OVRW* signal AND'ed with Color Key Compare CL-GD5430/'36/'40 only	Input
1	1	X	Color Key Compare	Output

2.3 Video Overlay

Anytime the CR1A[3:2] field is programmed to any value other than '0', the Pixel bus drivers are turned off and the bus becomes an input bus. Pixels for which Switch is active will be replaced on the screen with pixels from the pixel bus. Switch is controlled by register bits CR1A[3:2] and CR1D[6] as shown in the table above. The pixels from the pixel bus may or may not be interpreted differently in the DAC according to how DAC Mode Switching is programmed (see the next section).

If SR18[6] is programmed to '1', data from Display Memory will be used even if the Switch signal is active. This allows DAC Mode Switching without overlay. This is useful for displaying a window of data from the display memory in a mode other than VGA palettized.

2.4 DAC Mode Switching

The RAMDAC Mode can be dynamically changed between standard VGA 8-bit-per-pixel through the palette and another mode (such as 8-, 16-, or 24-bit RGB). DAC Mode switching is controlled by the Switch signal and can take place on a pixel basis.

In every case where DAC Mode Switching is used, one mode will be the standard VGA 8-bit mode through the LUT. The second mode will be the one programmed into the Hidden DAC register (HDR). If DAC Mode Switching is disabled (see below), any desired DAC Mode may be used.

The CL-GD543X can be programmed so that DAC Mode Switching occurs when Switch is active, or when Switch is not active, or not at all. This is shown in the following table.

Table B14-2. Relationship Between Switch and DAC Mode Switching

CR1D[2:1]	DAC Mode Switching
00	Choose Extended DAC Mode on Switch true
01	Choose Extended DAC Mode on Switch false
1x	DAC Switching disabled

3. GENERATING SWITCH: DETAILS

The various methods of generating the Switch signal are covered in the following sections. The programming of CR1A and CR1D are covered, and a block diagram shows how to configure a system to use that mode of generating switch.

Whenever the pixel bus is switched to inputs, the external video generator must always drive the pixel bus to valid CMOS levels. This is true even for the portion of the frame where the Alpine is not actually using the data from the bus. This prevents the bus pins from floating to CMOS threshold and oscillating.

3.1 Switch with EVIDEO*

Switch with EVIDEO* is selected when the CR1A[3,2] field is programmed to '0,1'. For the CL-GD5430/'36/'40 only, CR1D[6] must be programmed to '0. The block diagram in Figure B14-2 indicates how a system might be configured to use this mode. Note that the pixel bus extensions P[15:8] are available only on the CL-GD5436.

The external video source determines which pixels will be chosen. The Alpine simply displays data from the display memory or data from the Pixel bus according to whether EVIDEO* is active (but see SR18[6]). For every pixel that is to be overlayed, the external video source must drive EVIDEO* active and provide either 8- or 16-bit video at the P-bus. Setup and hold time requirements are specified in the timing diagrams in the data book.

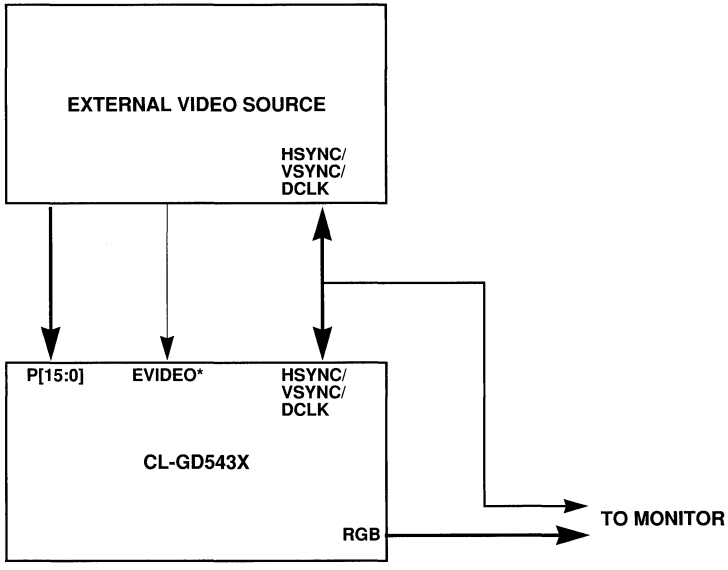


Figure B14-2. Switch with EVIDEO*

The system designer must guarantee that the External Video Source and the CL-GD543X are precisely synthronized. Otherwise the overlayed video will appear at random places on the screen. This is why the sync and DCLK signals have to be available at both blocks. There are two basic approaches. Either the External Video Source has to synchronize itself to the CL-GD543X or the CL-GD5434/'36 (only) has to synchronize itself to the External Video Source. For the latter case, see Appendix B17, *GENLOCK Support*.

3.2 Switch with Color Key

Switch with Color Key is enabled when the CR1A[3:2] field is programmed to '1,1'. In this mode, the choice of pixels to be overlayed is controlled strictly by the contents of display memory. If a VGA pixel compares appropriately with the contents of the Color Key register, Switch will be active. EVIDEO* is a normally LOW output in this mode; it will go HIGH one VCLK period before any pixel is replaced. If horizontally contiguous pixels are to be replaced, EVIDEO* will remain HIGH appropriately.

The comparison that is made is chosen according to CR1D[5:4] as indicated in the following table:

Table B14-3. Color Key Comparison

CR1D[5:4]	Comparison	Note	Availability Note
00	Pixel Byte = Color Key register	Logical	
01	Pixel Byte < Color Key register	Arithmetic	CL-GD5434/'36 only

Table B14-3. Color Key Comparison *(cont.)*

CR1D[5:4]	Comparison	Note	Availability Note
1x	Pixel Byte > Color Key register	Arithmetic	CL-GD5434/'36 only

The matching of the pixel with the Color Key is done under a mask. GRC contains the Color Key; GRD contains the mask. The key is compared with the pixel from display memory only for those bits for which the mask is a '0'. If the values 0xFC through 0xFF are to be used for the key, Register GRC can be loaded with any value in the range 0xFC though 0xFF, and GRD would be loaded with the value 0x03.

In cases where the CL-GD543X is programmed for other than 8-bits-per-pixel, the high-order byte of the pixel will be compared; the others will be ignored. This is shown in Table B14-5.

Table B14-4. Color Key Bytes

Mode	Byte Compared	Note
8 bits per pixel	Every Byte	
16 bits per pixel	High Byte	See CR1D[3] (CL-GD5436/'40 only)
32 bits per pixel	Alpha Byte	CL-GD5434/'36 only

The CL-GD5436/'40 can be programmed for a 16-bit color key compare. If the 16-bit parallel transfer mode is selected by programming the SR7[2:1] field to 1,1, and CR1D[3] is programmed to '1', all 16 bits of each pixel will be compared. The low byte of VGA data will be compared to the value in GRC and the high byte of VGA data will be compared to the value in CRD. No mask is available. This cannot be used when the SR7[2:1] is programmed for 16- or 24-bit serial modes.

The block diagram in Figure B14-3 indicates how a system might be configured to use Color Key compare. Note that EVIDEO* is an output from the Alpine in this case. The external video source can determine which pixels are to be overlayed by monitoring the EVIDEO* output of the CL-GD543X. For every pixel that is to be overlayed, it must provide either 8- or 16-bit video at the P-bus.

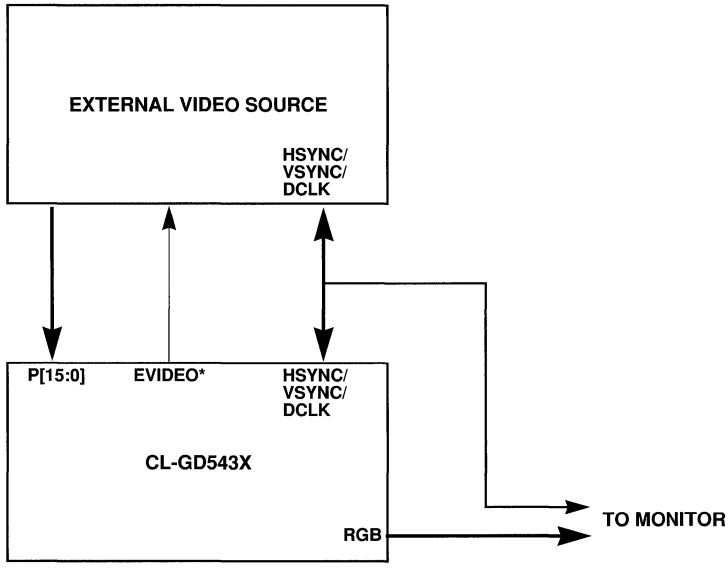


Figure B14-3. Switch with Color Key

3.3 Switch with Color Key ANDed with EVIDEO*

Switch with Color Key ANDed with EVIDEO* is selected when the CR1A[3:2] field is programmed to '1,0'. For the CL-GD5430/'36/'40 only, CR1D[6] must be programmed to a '0'. The Switch signal is the logical 'AND' of the Color Key comparison and EVIDEO* being LOW. EVIDEO* is an input in this mode.

This mode is intended to restrict the Color Key effect to a specified area.

This mode can also be used to mechanize a dynamic window with horizontal resolution finer than an eight-pixel character clock. The coarse horizontal timing would be generated with the on-chip Window Timing Generator as described above, and the fine (pixel resolution) would be controlled by changing either the contents of display memory or the Color Key Mask.

3.4 Switch with Color Key ANDed with OVRW* signal (CL-GD5430/'36/'40)

Switch with Color Key ANDed with OVRW* is selected when the CR1A[3:2] field is programmed to '1,0'. CR1D[6] must be programmed to '1'. The Switch signal is the logical 'AND' of the Color Key comparison and the internal OVRW* signal being active. EVIDEO* is an input in this mode but is not used.

This mode is intended to restrict the Color Key effect to a specified area.

3.5 Switch with OVRW* (CL-GD5430/'36/'40 only)

Switch with OVRW* is selected when the CR1A[3,2] field is programmed to '0,1' and CR1D[6] is programmed to '1'. This mode is available on the CL-GD5430/'36/'40 only. The block diagram in Figure B14-4 indicates how a system might be configured to use this mode.

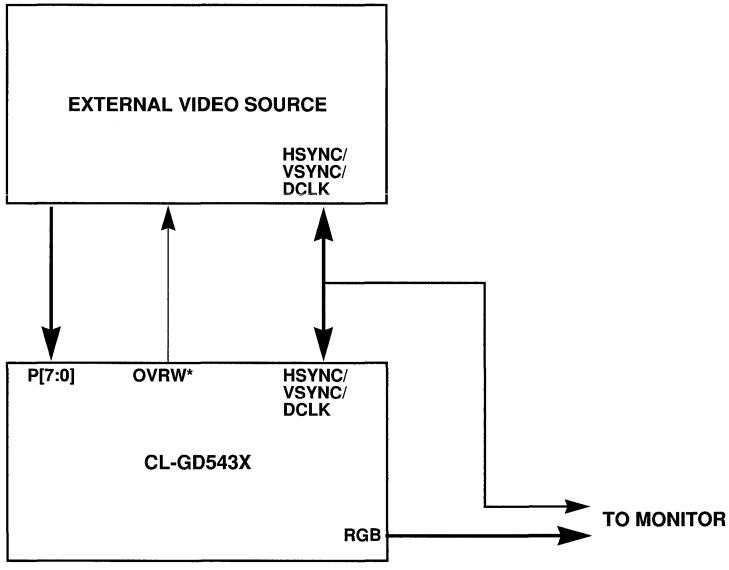


Figure B14-4. Switch with OVRW*

This mode allows the Alpine to generate its own window. This effect can be simulated on the CL-GD5434 by driving the EVIDEO* pin with OVRW*.

The external video source must monitor OVRW* to determine which portion of the screen is to be overlayed with its video. For every pixel that is to be overlayed, either 8- or 16-bit video at the P-bus must be provided.

4. OVRW*: ON-CHIP WINDOW TIMING GENERATOR

The CL-GD543X contains logic to generate timing for a single rectangular window. If this function is enabled, the window timing comes out on OVRW*, which may be fed back into EVIDEO*; the chip specifies its own window. For the CL-GD5430/'36/'40 only, the internal signal is also directly available as the Switch signal.

This mode is chosen by programming CR1B[5] to a '1'. When this is done, the blanking term to the palette DAC comes from Display Enable, and there is no border. This makes the Blank Generator Logic available, which is used as a window generator. The timing diagram in Figure B14-5 shows how the Blank Start and Blank End registers specify either the horizontal or vertical component of the window; the other component is similar. The Horizontal Blank End field is extended to eight bits and the Vertical Blank End is extended to 10 bits.

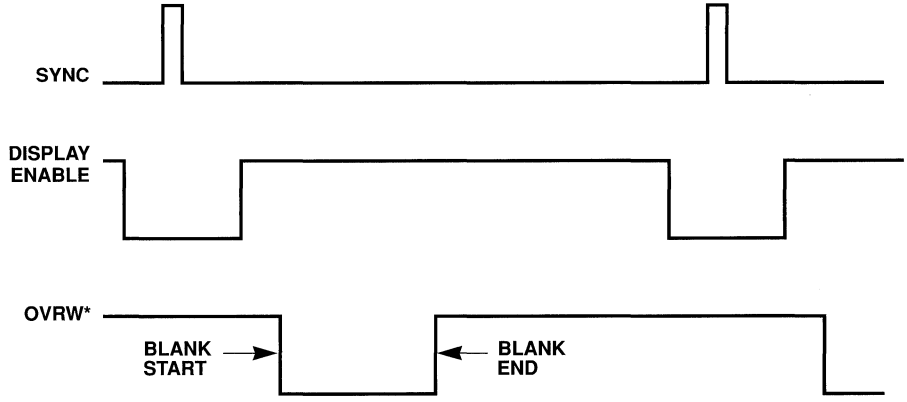


Figure B14-5. Blanking Term Selection

When the vertical timing and the horizontal timing generated coincide, OVRW* will be driven LOW. This indicates the window. OVRW* may be connected directly to EVIDEO* if Dynamic Overlay mode '1,1' (Color Key only) is never going to be chosen. If Dynamic Overlay Mode '1,1' will be chosen, OVRW* must be driven into EVIDEO* with an external three-state buffer to avoid a potential bus collision. This is avoided on the CL-GD5430/'36/'40 by making the term available internally.

This method of generating timing has four restrictions that require consideration. First, since the blank timing generation logic is used for window generation, there can be no border. This is inconsequential since the VESA timing specifications do not include a border. Second, since the Horizontal Counters operate on an eight-pixel character clock, the resolution of the horizontal component of the window is eight pixels. This can be overcome at least in part by using EVIDEO* and Color Key Overlay, as discussed previously. Third, there can only be a single window and it must be rectangular. Finally, the first, third, or subsequent scanline (or group of eight pixels) can be chosen as a window boundary, not the second scanline (or group of eight pixels).

When programming horizontal and vertical blanking, nine registers must be programmed to set the four blank parameters. Five of these registers contain bits related to other functions.

Table B14-5. Programming of Horizontal and Vertical Blanking

Register	Bits	Parameter	Other Bits
CR2	7:0	Horizontal Blank Start [7:0]	–
CR3	4:0	Horizontal Blank End [4:0]	7:5
CR5	7	Horizontal Blank End [5]	6:0
CR7	3	Vertical Blank Start [8]	7:4, 2:0
CR9	5	Vertical Blank Start [9]	7:6, 4:0
CR15	[7:0]	Vertical Blank Start [7:0]	–
CR16	[7:0]	Vertical Blank End [7:0]	–
CR1A	[7:6]	Vertical Blank End [9:8]	3:0
CR1A	[5:4]	Horizontal Blank End [7:6]	3:0

5. CL-GD5436 ENHANCEMENTS

The CL-GD5436 has two major enhancements for Video Overlay. These are described in the next two sections.

5.1 16-bit Pixel Bus (CL-GD5436)

When the CL-GD5436 (only) is configured for PCI bus, it can be programmed for a 16-bit input pixel bus. The following table shows the pins that are used for the upper eight bits.

Table B14-6. Pixel Bus Extension (Input Only)

P-Bit	Pin	(was)
P8	45	Reserved
P9	44	Reserved
P10	40	BIOSA13
P11	39	Reserved
P12	38	Reserved
P13	37	BIOSA12
P14	36	BIOSA11
P15	35	BIOSA10

To enable the pixel bus extension, the CL-GD5436 must be configured for PCI host bus, the

BIOS ROM must be disabled by programming PCI30[0] to '0', and GR18[6] must be programmed to '1'. This makes the following three overlay modes available.

Table B14-7. Overlay Modes with Pixel Bus Extension

VGA Data	Max Pixel Clock	(Modes)	Overlay Data	Overlay Clocking
8-bit LUT	50 MHz	5Ch at 75 Hz	16-bit RGB	Pixel Clock
8-bit LUT	40-80 MHz	60h at 75 Hz	16-bit RGB	Pixel Clock /2 with interpolation
16- bit RGB	50 MHz	60h at 75 Hz	16-bit RGB	Pixel Clock

5.2 Clock Doubling with Interpolation (CL-GD5436)

When the 16-bit Pixel bus extension is enabled, clock-doubling and overlay interpolation can be enabled by programming GR8[5] to '1'. This allows 16-bit RGB to be overlayed onto 8-bit VGA palettized data with a pixel clock of up to 80 MHz.

SR7[3:1] are programmed to '011' so that data is provided to the RAMDAC 16 bits in parallel. VCLK is programmed to 1/2 the actual pixel clock. The RAMDAC will provide a clock doubling function and each 16-bit word will be unpacked and converted at twice the VCLK rate.

The 16-bit RGB overlay data is input at the VLCK frequency (that is, for every other pixel). The pixels in between will be generated in the CL-GD5436 by averaging the two adjacent real pixels. The last pixel to be overlayed will be replicated (since there is no following pixel for interpolation).

6. USING THE INTERNAL CLOCK WITH DCLK AS INPUT

The overlay modes described in this appendix are intended to be used in a configuration where the video clock is provided by the external video source. If the clock were to be provided by the CL-GD543X, the result is a situation of clocking data into a device where the device itself is providing the clock.

For the CL-GD543X family, the VCLK VCO can be sourced onto the MCLK pin and an external buffer can be supplied to drive MCLK (which is the VCLK) into the DCLK pin. This makes both DCLK and the Pixel bus inputs. On the CL-GD5430/'36/'40, this is a configuration option and is selected when a pull-down resister is installed on MD60. On the CL-GD5434, this is a by-product of programming the device for any overlay mode (CR1A[3:2] not equal to '0,0'). The block diagram in Figure B14-6 indicates how a system might be configured to use the buffer to drive MCLK.

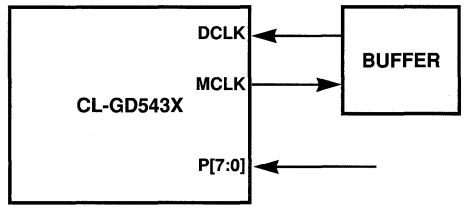


Figure B14-6. Using MCLK as DCLK

7. STATIC OVERLAY

The CL-GD543X supports the standard VESA pass-through function, during which the EVIDEO* pin is statically driven LOW and video is driven into the P-bus. The entire frame is overlayed, and the contents of display memory are ignored. EDCLK* is typically driven LOW so that DCLK as well as the video are supplied externally.

8. VESA® ADVANCED FEATURE CONNECTOR (VAFC)

8.1 Introduction

All members of the CL-GD543X family support VAFC baseline output. The CL-GD5430/'36/ '40 supports VAFC baseline input as well.

8.2 Adapter or Mother board Preparation

To insure that a board will support the functions, ensure that extra pins on the feature connector are wired, via jumpers or zero-Ω resistors, as indicated in Table B14-8.

Table B14-8. Connections to VESA Feature Connector for VAFC

Pin	Jumper to:	Note
Z7	VCC	Power for VAFC/VESA bridge
Z12	MCLK	Will be VCLK VCO
Z13	OVRW*	Internally generated window timing

Install a configuration pulldown resistor to select the VCLK VCO at the MCLK pin. For Alpine, the correct pin is MD60.

8.3 VAFC Adapter Board Description

The attached schematic diagram is a board designed by Cirrus Logic to test the VAFC baseline input. As of the time of this writing, it has not been completely tested because no system capable of driving VAFC is available.

8.3.1 VESA Passthrough Connector

The modified VESA passthrough connector is shown on the left edge of the diagram. Pins are connected and used as indicated in the following table.

Table B14-9. VESA Passthrough Connector Pins

Pin(s)	Direction	Use
P[7:0]	Input	Pixel data into Alpine
EVIDEO*	Output	Overlay Enable (Request)
EDCLK*	Input	Use External DCLK
MCLK	Output	VCLK VCO (prior to post-scalar) drives DCLK pin on VAFC connector
OVRW*	Output	Reserved for overlay enable (currently unused)
DCLK	Input	Pixel Clock
BLANK*	Output	(normal blank signal)
HSYNC/ VSYNC	Outputs	(normal sync signals) Connected to VAFC inputs

8.3.2 VAFC Connector

The VAFC connector is shown on the right edge of the schematic diagram. The pins are connected and used as indicated in the following table.

Table B14-10. VAFC Connector Pins

Pin(s)	Direction	Use
P[15:0]	Output	Pixel data
GRDY	Input	Allow Video
BLANK*	Input	Driven by CL-GD543X/'4X
HSYNC/ VSYNC	Inputs	Driven by CL-GD543X/'4X
VCLK	Output	Video Clock
DCLK	Input	Driven by MCLK on VESA connector (CL-GD543X/'4X VCLK VCO)
EVIDEO*	Output	Overlay enable from video board

8.3.3 17x2 Header

The 17x2 header in the upper center of the schematic diagram is included as part of joint development by MCT, Inc. and Cirrus Logic.

8.3.4 Timing Generation

The basic timing is generated in the Alpine. The VCLK VCO is driven via the MCLK pin onto Z12 of the VESA connector and thence to pin 15 (DCLK) of the VAFC connector. On the video board, DCLK is turned around to become VCLK. VCLK is delayed and shaped in the PAL device on the adapter card to drive DCLK on the VESA connector. VCLK from the VAFC connector is also used to controller the multiplexor.

8.3.5 Data Flow through Adapter Card

The 16-bit pixel data from the VAFC connector is clocked into U1 and U2 at the rising edge of every VCLK (from the VAFC connector). The 16-bit pixels are multiplexed into bytes at twice the DCLK frequency with the three-state bus labeled at P[7:0]. The enable terms for the three-state drivers is a delayed version of VCLK from the VAFC connector.

8.4 Software

The following code fragment can be used to test the adapter board and the CL-GD5430 input logic. This software is used for the CL-GD5430 only.

- Program the MISC register to select VCLK3. Either 2 or 3 may be used, but MISC[3] must be programmed to '1' for the DCLK pin to drive both the DAC and the CRTC counters.

```
mov     dx,03cch;       /*will read from MISC register*/
in      al,dx;          /*current value*/
or      al,0ch;         /*select VCLK3 - also DCLK pin to
                        /*DAC and CRTC counters*/
mov     dx,03c2h;       /*will write MISC register*/
out     dx,al;
```

- Program SR0E/SR1E for the desired pixel clock frequency. In this example, it is programmed for 25.18 MHz. This is the appropriate frequency for 640 x 480 at 60 Hz refresh. Observe that the post-scalar can not be used because the source for the MCLK pin is taken before the post scalar.

```
mov     dx,03c4h;       /*point to the SR registers*/
mov     ax,330dh;       /*numerator*/
out     dx,ax;          /*both index and data at once*/
mov     ax,3a1dh;       /*denominator and post scalar*/
out     dx,ax;
```

- Set Dot Clock divided by two by programming SR1[5] to '1'. The adapter card will double the MCLK frequency prior to feeding it back on the DCLK pin.

```
mov     al,01h;         /*point to SR1*/
out     dx,al;          /*set the index*/
inc     dx;             /*data register port*/
in      al,dx;          /*get the current value of SR1*/
or      al,08h;         /*set bit three*/
out     dx,al;          /*and write it to SR1*/
```


- Set the overlay/DAC mode switch control field in CR1A to 1,1 to select overlay with color key. As a side effect, the EVIDEO* pin will become an output and is used on the adapter board to drive EDCLK* low. This will cause the '30 to use the DCLK pin as the VCLK source.

```
mov     dx,03d4h;       /*assume we are in color mode*/
mov     al,1ah;         /*point to CR1a*/
out     dx,al;          /*set index*/
inc     dx;             /*point to data point*/
in      al,dx;          /*get current CR1A*/
or      al,0ch;         /*CR1A[3:2] = 11*/
out     dx,al;          /*set the value*/
```

- Set blanking control in CR1B[5]. This switches the BLANK* output to display enable. In addition, the OVRW* pin will follow the blanking signal generated by the CRT controller

```
dec     dx;             /*point back to CR index*/
mov     al,1bh;         /*point to CR1B*/
out     dx,al;          /*set the index*/
inc     dx;             /*point to data port*/
in      al,dx;          /*get current CR1B*/
or      al,20;          /*set bit 5*/
out     dx,al;          /*and write it*/
```

- Set the overlay timing signal source to OVRW* by programming CR1D[6] to '1'. This is actually not used since since color key overlay control is being used.
- Set the overlay switching control for DAC mode switching on switch true.

```
dec     dx;             /*point back to CR index*/
mov     al,1dh;         /*point to CR1D*/
out     dx,al;          /*set the index*/
inc     dx;             /*point to data port*/
in      al,dx;          /*get current CR1D*/
or      al,40;          /*set bit 6*/
and     al,f9h;         /*clear bits 3,2*/
out     dx,al;          /*and write it*/
```

- Program the Hidden DAC Register (HDR) to E1h. This selects 5-6-5 as the extended mode and selects clock-doubling.

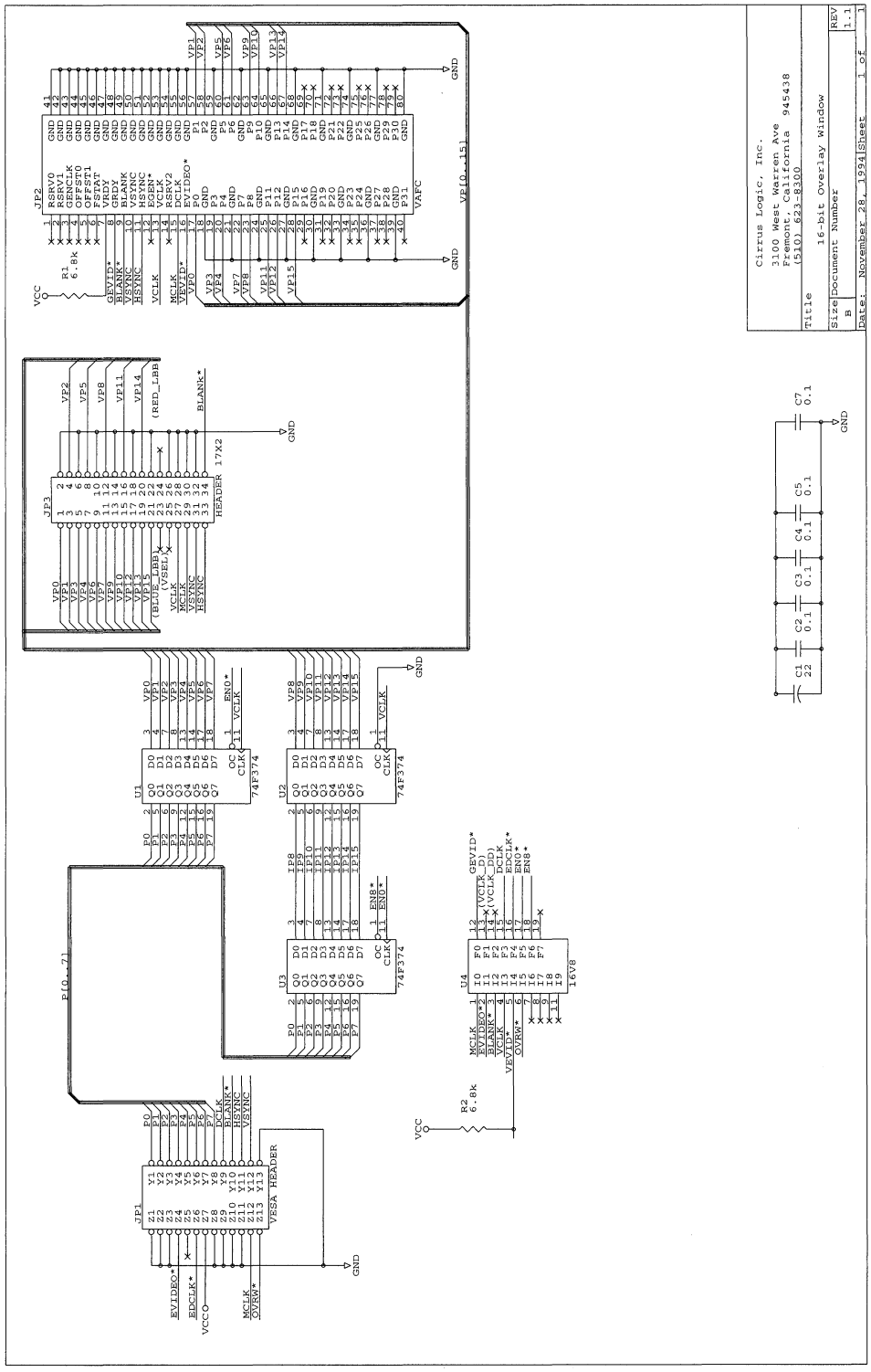
```
mov     dx,3c6h;        /*get ready to access HDR*/
in      al,dx;          /*read pixel mask register*/
in      al,dx;          /*four times*/
in      al,dx;          /*in succession*/
in      al,dx;          /*next access to 3c6 will hit HDR*/
mov     al,e1h;
out     dx,al;          /*write hidden dac register*/
```

- Finally, the color key and color key mask can be selected by programming GRC and GRD. For this example, the key is programmed to ffh and the mask is programmed to 03h. This will cause a match for the pixel value fch, fdh, feh, and ffh.

```
mov     dx,3ceh;        /*point to GR registers*/
mov     ax,ff0ch;       /*ff to color key*/
out     dx,ax;          /*do it*/
mov     ax,o30dh;       /*03 to color key mask*/
out     dx,ax;
```

8.5 PAL Device Equations

```
Name            v0;
Partno          00000;
Date            11/27/94;
Revision        1.00;
Company         Cirrus Logic Inc.;
Assembly        VAFC;
Location        U5;
Device          p1618;
/
*************************************************************************/
/*  This PAL is on the VAFC to feature connector interface module.      */
/
*************************************************************************/
/** Inputs  **/

Pin  1     = mclk;                /* Clock from 5429/30. */
Pin  2   = !evideo;    /* 5429/30 overlay enable signal. */
Pin  3   = !blank;    /* 5429/30 blank signal.*/
Pin  4   = vclk;       /* Clock from video board.*/
Pin  5   = !vevid;/* Overlay enable signal from video board*/
Pin  6   = !ovrw;/* Reserved for 5429/30 overlay enable signal*/

/** Outputs **/
Pin  12 = !gevid;     /* Allow video to start xfer data.*/
Pin  13 = vclk_d;    /* Delay of vclk.              */
Pin  14 = vclk_dd;     /* Delay of vclk_d       */
Pin  15 = dclk;              /* DCLK as external source (DCLK=mclk *2)*/
Pin  16 = !edclk;/* DCLK as external source enable signal.*/
Pin  17 = !en0;              /* Enables V_P[7:0] to P[7:0].*/
Pin  18 = !en8;              /* Enables V_P[15:8] to P[7:0].  */

/** Logic equations **/
vclk_d = vclk;
vclk_dd = vclk_d;

edclk = !vevid & blank & evideo
      # !vevid & edclk & !blank
      # vevid & !evideo;

dclk = (vclk & !vclk_dd) # (!vclk & vclk_dd);
dclk.oe = edclk;

en8 = vclk_dd;
en8.oe = edclk;

en0 = !vclk_dd;
en0.oe = edclk;

gevid = !edclk;
```



Cirrus Logic, Inc.
3100 West Warren Ave
Fremont, California 945438
(510) 623-8300
Title 16-bit Overlay Window
Size B
Document Number
REV 1.1
Date: November 28, 1994 Sheet 1 of 1
JP2
JP3
JP1
U1
U2
U3
U4
74F374
16V8
HEADER 17X2
VESA HEADER
R1 6.8k
R2 6.8k
C1 22
C2 0.1
C3 0.1
C4 0.1
C5 0.1
C7 0.1
VCC
GND

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Appendix B15

EEPROM Interface and Programming

EEPROM INTERFACE AND PROGRAMMING

1. INTRODUCTION

This appendix presents interface and programming details of the optional EEPROM (Electrically Erasable Programmable Read-Only Memory), and provides an overview of Extension register SR8. Timing restrictions imposed by the EEPROM device are included as are examples of writing to and reading the EEPROM.

The EEPROM is used by the Cirrus Logic BIOS to contain system configuration information, such as monitor type and refresh rate. The BIOS uses the first four bytes of the EEPROM; it is possible to use the remainder for other applications.

The programming examples are for the XL93C46 1024-bit device.

2. SR8

The EEPROM interface is controlled through Extension register SR8 (refer to Chapter 9 for details on this register). The SR8 bits are summarized in Table B15-1.

Table B15-1. Extension Register SR8 EEPROM Interface

Bit	Function
7	EEPROM Input Data
6	Disable MCS16* for display memory. (**NOTE**: This bit must be preserved.) For chips that support DDC2B, this bit must be programmed to '0' to enable EEPROM support.
5	Latch ESYNC*/EVIDEO* input state
4	Enable ESYNC*/EVIDEO* as outputs for EEPROM Data and Serial Data clocks (SK)
3	Serial data input (DI) to EEPROM if bit 4 = 1
2	SK to EEPROM if bit 4 = 1
1	Enable EEPROM Data In
0	Chip Select (CS) to EEPROM

3. TIMING CONSIDERATIONS

Serial EEPROMs are inherently slow devices. Software written to control EEPROMs must include timing delays so that signal transitions do not occur too quickly. Consult the data sheet for the particular device. The parameters in Table B15-2 are typical.

Table B15-2. EEPROM Timing Parameters

Parameter	MIN	Units
DI-setup-to-SK-positive transition	1	µS
DI-hold-from-SK-positive transition	1	µS
SK High-pulse Width	2	µS
SK Low-pulse Width	2	µS
DO-delay-from-SK-positive transition	2	µS

The times specified in Table B15-2 are minimum. Longer delays will not damage the device. The EEPROM write operation requires a 10-µs wait after the last bit has been transferred; no other operation is allowed until this time has elapsed.

The XL95C46 EEPROMs are organized as 64 sixteen-bit locations (each with a 6-bit address). Any data transfer, read, or write must transfer all 16 bits for correct operation.

3.1 Write Example

1. Set the CL-GD543X/'4X for EEPROM Control:
   a. Unlock the Extended registers (SR6 = 12h).
   b. Determine the state of SR8[6] and save it for all subsequent writes.
   c. Latch ESYNC* and EVIDEO* inputs (SR8[5] = 1).
   d. Enable EEPROM Interface (SR8[4] = 1, SR8[1] = 1). For all writes to SR8 during this and the following steps (except step 5), bits 5, 4, and 1 must be done uniformly, and bit 6 *must always* be as is determined in step 1b.

2. Enable the EEPROM for writes:
   a. Set the EEPROM Chip Select high (SR8[0] = 1).
   b. Send the Write Enable Command (01000110000) to the EEPROM:
      – write data bit into SR8[3],
      – set SK high (SR8[2] = 1),
      – set SK low (SR8[2] = 0),
      – get the next data bit and repeat the sequence until all 11 bits are sent.
   c. Set the EEPROM Chip Select low (SR8[0] = 0).

3. Write 16 bits of data to the EEPROM location desired:
   a. Set the EEPROM Chip Select high (SR8[0] = 1).
   b. Send the Write Enable Command (01000110000) to the EEPROM:
      – write data bit into SR8[3]
      – set SK high (SR8[2] =1)
      – the bit sequence is 0101 A5..A0 D15..D0
      Where A5..A0 is the 6-bit address and D15..D0 is the data
      – set SK low (SR8[2] = 0)
   c. Set the EEPROM Chip Select low (SR8[0] = 0).

4. Repeat Step 3, if required.

5. Remove the CL-GD543X/'4X from EEPROM Control:
   a. Disable the EEPROM interface (SR8[4] = 0, SR8[1] = 0).
   b. Unlatch ESYNC* and EVIDEO* (SR8[5] = 0).
   c. Lock the Extended registers (SR6 = 0).

3.2 Read Example

1. Set the CL-GD543X/'4X for EEPROM Control:
   a. Unlock the Extended registers (SR[6] = 12h).
   b. Determine the state of SR8[6] and save it for all subsequent writes.
   c. Latch ESYNC* and EVIDEO* inputs (SR8[5] = 1).
   d. Enable EEPROM interface (SR8[4] = 1, SR8[1] = 1). For all writes to SR8 during this and the following steps (except step 5), bits 5, 4, and 1 must be done uniformly, and bit 6 *must always* be as is determined in step 1b.

2. Read the EEPROM:
   a. Set the EEPROM Chip Select high (SR8[0] = 1).
   b. Send the READ Command (0101 A5..A0) to the EEPROM:
      – write data bit into SR8[3]
      – set SK high (SR8[2] = 1)
      – set SK low (SR8[2] = 0)
      – get the next data bit and repeat the sequence until all ten bits are sent
   c. Read EEPROM Data D15..D0.
      – set SK high (SR8[2] = 1)
      – set SK low (SR8[2] = 0)
      – read the data bit at SR8[7]: first bit is D15
      – continue until all 16 bits are read
   d. Set the EEPROM Chip Select low (SR8[0] = 0).

3. Repeat Step 2, if required.

4. Remove the CL-GD543X/'4X from EEPROM Control:
   a. Disable the EEPROM interface (SR8[4] = 0, SR8[1] = 0).
   b. Unlatch ESYNC* and EVIDEO* (SR8[5] = 0).
   c. Lock the Extended registers (SR6 = 0).

Appendix B16

DDC1/2B Support

DDC1/2B SUPPORT

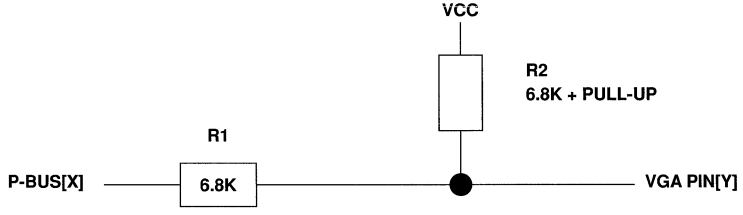
1. INTRODUCTION

The VESA Display Data Channel (DDC) proposal defines a communication channel between a computer display and the host system. The channel may be used to carry configuration information for optimum use of the display as well as carry additional display control information.

This appendix shows how Cirrus Logic recommends that its CL-GD543X chips be configured to support DDC levels 1 and 2B. It will also cover Cirrus' plans for changes in this regard for future versions of the CL-GD543X family. Finally, the I^2C interface for the CL-PX4072 is covered. A schematic diagram fragment illustrates the connections.

2. DDC1 BOARD DESIGN

DDC1 is supported by all Cirrus Logic desktop chip families, beginning with the CL-GD542X True Color VGA Family. Since late 1993, all Cirrus Logic reference designs have included (passive) components that allow software to sense TTL levels on the monitor ID pins on the 15-pin VGA connector. The following diagram indicates how this is mechanized for a typical pin.



If the pin on the VGA connector is open or is being driven to a TTL high by the monitor, a soft-high will appear on the P-bus pin. If the pin on the VGA connector is grounded or is being driven to a TTL LOW by the monitor, a soft low will appear on the P-bus pin. If the overlay control field in CR1A[3:2] is programmed to any value other than '0,0', the P-bus pins will be inputs and their levels can be sensed in the STAT register (3DA or 3BA). The following table shows how the pins are allocated and how they are sensed.

Mon ID Bit	VGA Pin	P-Bus	Program AR12[5:4] to	Sense on STAT[x]	Note	Recommended
MID0	11	P0	00	4		No
MID1	12	P1	10	4	DDC1	Yes
MID2	4	P2	00	5		No
MID3	15	P3	10	5		No

For DDC1, only Mon ID1 needs to be connected. Connecting bits Mon ID0 and Mon ID2 will allow the hardware to support the old method of monitor ID sensing. This is absolutely no longer supported by Cirrus Logic BIOSs and is no longer recommended. Cirrus has previously recommended connecting VGA pin 15; this is no longer recommended since it can cause monitors with DDC2B support to incorrectly enter DDC2B mode.

In the attached schematic fragment, the only components required for a DDC1-only design are R3, R4, and R6.

3. DDC2B BOARD DESIGN: OLD METHOD

Cirrus Logic supports DDC2B for desktop families beginning with Alpine (CL-GD543X/'4X). DDC2B requires that the board drive some monitor ID pins, as well as sense them. They are bidirectional pins and use an open collector protocol. The attached schematic fragment shows how Cirrus Logic recommends that this be mechanized.

Gates B and C drive pins 12 and 15, respectively, of the VGA connector. These are open collector gates and so can drive only low. This is the protocol defined for DDC2B. The levels on these pins, whether they are being driven by the VGA controller or by the monitor, can be sensed on pixel bus pins P[1], and P[3], respectively.

Gate A inverts EECS. When the EEPROM is being accessed, this output will be LOW, preventing gates B and C from turning on. This prevents EEPROM accesses from affecting a DDC monitor.

This circuit will support DDC1 and DDC2B with no hardware changes.

4. DDC2 BOARD DESIGN: NEW METHOD

Future revisions of Cirrus Logic CL-GD5434 and and all versions of the CL-GD5436 and CL-GD5440 will use the EECS and EEDI pins to both drive and read the levels on VGA pins 12 and 15. They will be configurable as open collector outputs with read-back capability. The following table indicates the chip revision that is planned to have this function. See the description of register SR8 in Chapter 9.

Chip	Rev Level
CL-GD5434	Production Revision E
CL-GD5436	Production Revision A
CL-GD5440	Production Revision A

The CL-GD5434, when configured for ISA bus, will not support this change and the circuit previously described can be used.

Jumpers are installed on JP1 and JP2 to connect EECS and EEDI to MID3 and MID1, respectively. U1 is not installed.

5. I²C DEVICE SUPPORT

The DCC2B logic can also be used to relay commands from the host to I²C devices, such as the CL-PX4072 multistandard TV decoder. Two pins on the feature connector are used for this purpose. This is used only for designs that are intended to work with the CL-PX4072.

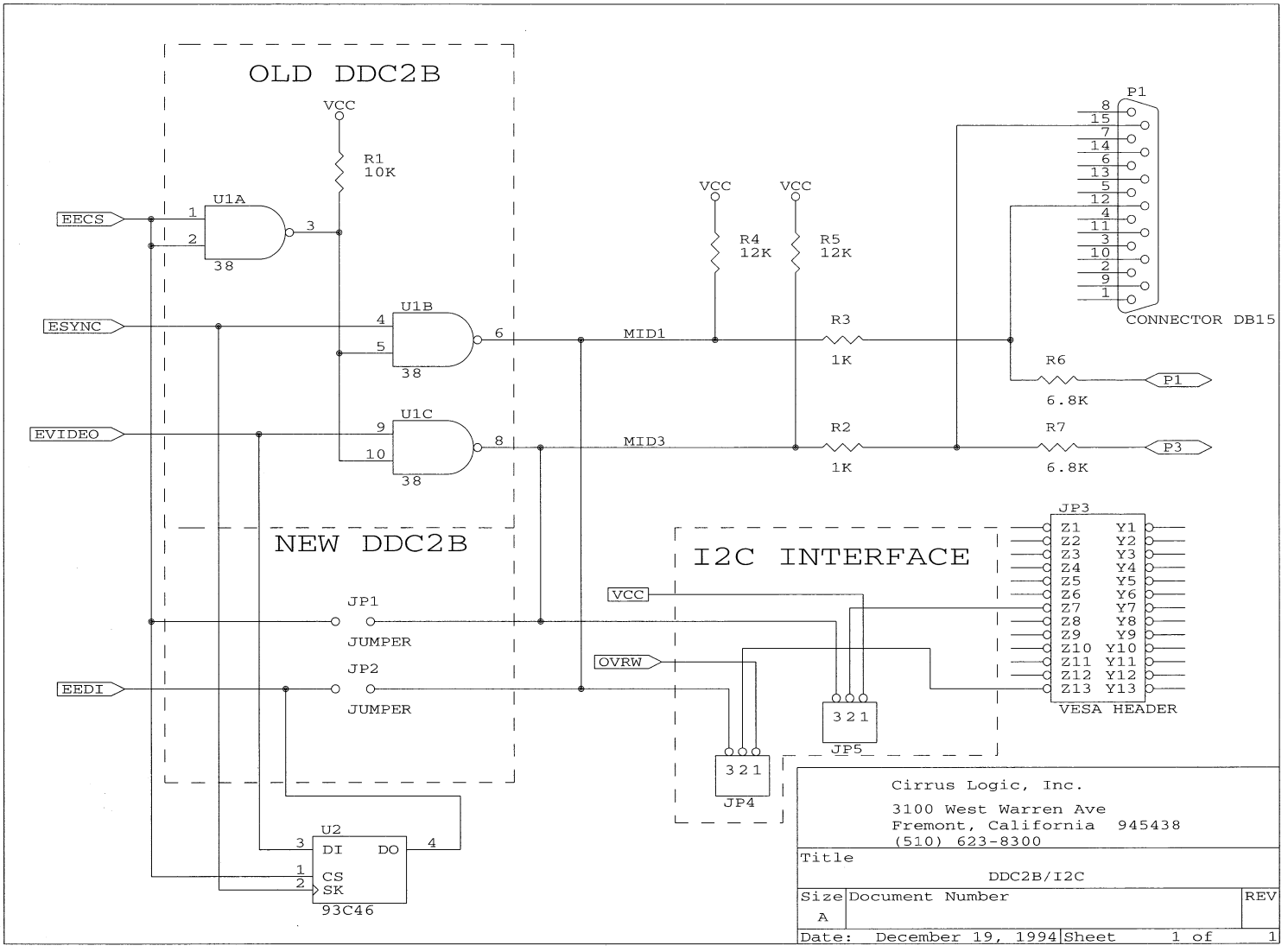
MID3 is connected to the feature connector pin Z7 and MID1 is connected to feature connector pin Z13. Either the old or new method of controlling MID3 and MID1 can be used. Three pin jumpers are used since VCC and OVRW* are connected to the feature connector pins for other applications.

If the I²C interface is not to be used, VCC and OVRW* should be connected to the feature connector with zero-Ω resistors.

6. SUMMARY

The following table summarizes the devices from the attached schematic fragment that must be populated for the various levels of support. For complete generality, the PC board should be designed with locations for all the components.

Case	Populate
Old DDC1	R3, R4, R6
New DDC1	R3, R4
Old DDC2B	U1, R1, R2, R3, R4, R5, R6, R7
New DDC2B	JP1, JP2, R2, R3, R4, R5, R6
I²C Interface (with DDC2B)	Add JP4, JP5



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Appendix B17

GENLOCK Support

CL-GD5434/'36 Only

GENLOCK SUPPORT (CL-GD5434/'36 ONLY)

1. INTRODUCTION

When mixing video from multiple sources onto a single screen, it is necessary to synchronize the sources. This synchronization can be done by using a frame buffer, or it can be done by forcing the multiple video sources into synchronization with each other. In the latter case, one of the sources provides the timing and the others slave themselves to this timing. This is referred to as *GENLOCK*. GENLOCK is supported on the CL-GD5434/'36 only.

2. GENLOCK ON THE CL-GD5434/'36

The CL-GD5434/'36 can GENLOCK to an external VSYNC, an external HSYNC, or both. When using GENLOCK, the CL-GD5434/'36 must be supplied with an external VCLK (it does not recover the pixel clock from HSYNC). The clock is supplied on the DCLK pin, with EDCLK* being held low. 3C2[3:2] must be programmed to '1,X' so that the external clock drives the CRT Controller as well as the DAC.

The external master supplies HSYNC and VSYNC to the display, as well as to the CL-GD5434/'36. The diagram in Figure B17-1 shows the connections that must be made when video is being overlaid via the P[7:0] bus.

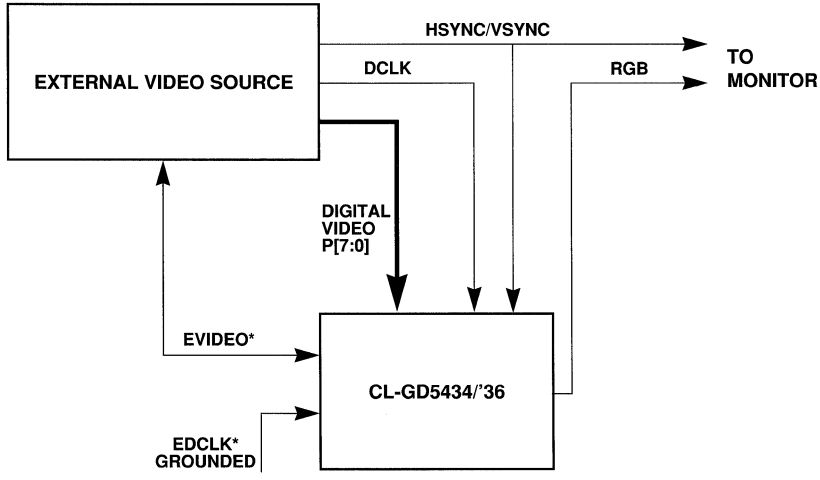

Figure B17-1. Video Overlay Connections

The external source provides all raster timing in the form of DCLK and both SYNCs. EDCLK* on the CL-GD5434/'36 is tied low so that DCLK is an input. The CL-GD5434/'36 is programmed for both VSYNC and HSYNC GENLOCK so both SYNC pins are inputs, preventing a bus crash. The CL-GD5434/'36 is also programmed for overlay mode (see Extension register CR1A) so that its P[7:0] pins are inputs. Depending on the overlay mode, EVIDEO* is an input or an output, as indicated in Table B17-1. See Appendix B14 for additional information regarding video overlay. Also depending on the overlay mode, the Digital Video from the external source may be either 8- or 16-bits per pixel.

Table B17-1. Overlay Mode I/O Indicator

CR1A[3:2]	Overlay Mode	EVIDEO*	Note
01	EVIDEO*	In	External Source provides overlay timing
10	EVIDEO* AND'ed with Color Key	In	External Source timing AND'ed with Color Key
11	Color Key	Out	VGA Data specifies pixels to be overlaid

3. VSYNC GENLOCK PROGRAMMING

If CR1C[7] is programmed to '1', VSYNC GENLOCK is enabled. The VSYNC pin becomes an input. The falling edge of the VSYNC input is synchronized to VCLK, and after two VCLK edges, the vertical counter will be reset on the next HSYNC. The next HSYNC after that will signal the beginning of the first scanline of the next field.

VTOTAL (CR7/CR6) should be programmed so that the external VSYNC will occur before the programmed value is reached. That is, the CRTC timing should be programmed for a somewhat greater than the actual vertical period and then truncated as necessary.

4. HSYNC GENLOCK PROGRAMMING

If CR1C[6] is programmed to '1', HSYNC GENLOCK is enabled. The HSYNC pin becomes an input. The falling edge of the HSYNC input is synchronized to VCLK, and after two VCLK edges, the Character Clock Generator (which is in fact, a VCLK counter) is cleared.

The next character clock (which is now synchronized to HSYNC at a VCLK resolution) will force the Horizontal Timing Generator to the state equivalent to Horizontal Total. The Horizontal Counter is cleared three character clocks later, and display data begins after the video pipeline delays normally present for the current display mode (typically three character clocks plus five VCLKs).

HTOTAL (CR0) should be programmed so that the external HSYNC will occur before the programmed value is reached. That is, the CRTC timing should be programmed for somewhat greater than the actual horizontal period and is then truncated as necessary.

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Appendix B18

Manufacturing Test

MANUFACTURING TEST

1. MANUFACTURING TEST PROGRAM

1.1 Specifications and Operating Instructions

The Manufacturing Test Program (MFGTST.EXE) provides the ability to visually and programmatically verify correct operation of the CL-GD543X/'4X family (as well as being downward compatible with the CL-GD542X and CL-GD540X families). Primary features include: write/read/compare tests of all video register groups, write/read/compare tests of all video RAM, display patterns for visual verification of all primary video modes, as well as a complete set of miscellaneous video tests designed to verify proper operation of the video chip. All RAM and register tests are self-checking to the extent that values will be read and compared to expected values. When a difference is detected, an error message will be generated.

The program detects chip type and automatically configures itself to run all valid tests for the video chip installed in the system. For example, if a CL-GD5430 or CL-GD5434 is installed in the system, the program automatically sets internal menus and external command-line options to run CL-GD5430- or CL-GD5434-specific tests accordingly. In all cases where a particular test is chip-specific, the program senses and records it.

The operating mode of the test program may be selected from display menu options, or may be specified with command-line parameters. This overview details the user interface and operation of the test program.

1.2 Using MFGTST Menu Driven Interface

At the DOS prompt type:

```
MFGTST /m [Enter]
```

When the '/m' option is selected, the user is in Menu mode (after the initial Cirrus Logic logo screen). From these menus, the user may select from a variety of register, display, or miscellaneous video tests. To select a test, use the up, down, left, or right arrow keys to change the currently highlighted selection. When the desired selection is highlighted, press the 'Enter' key to execute the test. The 'ESC' key always terminates a test, as well as the program, when at the main menu. Section 1.2.1 lists and discusses tests available while in Menu mode.

1.2.1 Register Tests

- Memory tests, for current video RAM installed in the video system
- Input Status register 1 test (SYNC bits)
- Sequencer register tests
- CRTC register tests
- Graphics Controller register tests

- Attribute Controller register tests
- Miscellaneous Output register test
- Feature Control register test
- DAC State register test
- PEL Mask register test
- DAC Palette register tests
- Extended register tests
- DAC comprehensive register test

All registers that are both writable and readable are tested by writing bit patterns to the register and then reading the same register. The result of the read operation is compared with the expected result. If a difference is detected, an error message is generated. If reserved bits are defined for a register, they are not included in the write pattern, that is, they are excluded from the compare. An extra test ensures that if ones are written to any reserved bits, they remain set to zeros in the read value.

The test patterns used for the write operation are derived from the loop count. Write values range from 0 to 255 (all possible bit patterns). When an error occurs the loop does not abort, the error bits are recorded and the register test continues. When all bit patterns have been written, the bit errors are analyzed. Information regarding bits that appear to be stuck high or low is included in the error message that is generated.

If multiple compare errors occur on a single register, a count of bad registers is incremented by '1', even though the total number of compare errors is greater than a '1'. For example, if a register has one bit stuck low (0), the bad register count is incremented (to a '1'), and the total number of compare errors will be 128. These statistics will be displayed in a summary, if the verbose mode (option '/v') was specified at the command line at program execution.

In addition to write/read/compare tests, Write-protection register tests are also performed. If Write-protect registers can be modified while locked, an error will be generated. Finally, the display enabled, and Vertical Retrace bits in the Input Status register 1 are verified to ensure that they toggle between active video and retrace states.

First Mbyte Video Memory test performs a write/read/compare loop on the 1st Mbyte of display memory. Before the memory test begins, the video chip is configured for a Packed-pixel mode. Using Write mode 2, all planes are written with a pre-selected test pattern (color). This value is loaded into the Color Compare register. Using Read mode 1, the entire memory address space is read (and compared) against the write value. If all pixels do not compare successfully, an error will be generated. When an error has been detected, RAM locations above the error location are not checked, that is, an error is only generated for the first faulty location. The RAM test verifies 16 different test patterns written to the video memory.

Video Memory test 2 uses Write mode 0 in an appropriate video mode, where the test patterns are written to and read back from video RAM directly. If the write value is different when read back, an error will be generated.

When running MFGTST.EXE from the command line, all tests listed above are run as a complete set (default set). Individual register tests may only be selected while in Menu mode or if the User-defined Script mode (option '/u') is selected from the command line (with script file).

1.3 Display and Miscellaneous Tests

- 80-column Text mode 3 test pattern
- 80-column Text mode 3 test (8 pages)
- 80-column Text mode 7 test pattern
- 40-column Text mode 1 test pattern
- 320 × 200 Graphics mode 4 test pattern
- 640 × 200 Graphics mode 6 test pattern
- 640 × 350 Graphics mode 10H test pattern
- 640 × 480 Graphics mode 12H test pattern
- 640 × 480 Graphics mode 11H test pattern
- 320 × 200 Graphics mode 13H test pattern
- VGA graphics standard 256-color palette test pattern
- Extended Video mode patterns (see summary in inside front cover).
- Rotate DAC test pattern
- Miscellaneous Graphics tests:
  - 512-character Set test
  - Pan and Scroll test
  - Split-screen test
  - 360 × 480 × 256 non-standard VGA mode test pattern
  - Summing-to-grayscale test
  - 12 rows × 80-columns Text mode test
  - Text mode scanline test (200, 350, or 400 scanlines)
  - Reset DAC, display static screens
  - Data Generator output
  - Data Generator tests
  - Hidden DAC register: 8-bit grayscale
  - Hidden DAC register: 3-3-2 RGB
- Hardware Graphics Cursor tests
- Write mode tests, BY8 and BY16 addressing tests, latches
- Signature Generator tests
- Signature Generator output
- BitBLT tests
- Variable VCLK test @ 65 MHz through 95 MHz
- Variable MCLK test @ 37 MHz through 68 MHz
- Memory-mapped I/O BitBLT tests

1.4 Test Descriptions

1. **Rotate DAC Test Pattern:** In this test, the DAC is reset to a color spectrum and then slowly rotated from right to left. The spectrum is rotated on the register-level only. For example, the color in register 1 is loaded into register 0, and the color in register 0 is loaded into register 255, and so on. Once the pattern is first drawn to memory, no other writes to memory are made. The test is run in mode 13H (320 × 200 × 256 colors). If colors seem to stick in place (not rotated) or migrate in an unusual manner, this may indicate a chip-level problem.

2. **512-character Test:** In this test, both a 9 × 16 character set (left side) and 8 × 8 character set (right side) are displayed simultaneously in mode 3. This is accomplished by loading two 256-character sets into Memory Plane 2. Sequencer register 3 is then set to select character sets 0 and 1. This enables Character Attribute bit 3 to select between the first or second set when writing characters to the display.
3. **Pan and Scroll Test:** By setting and continually updating several CRTC Registers, it is possible on a standard VGA to achieve a smooth pan and scroll of the display. The logical width of the display in this case must be larger than the display screen itself to permit horizontal scrolling. The text 'PANNING AND SCROLLING TEST', with normal VGA operation, should pan and scroll from the lower right-hand corner of the screen to the upper left-hand corner of the screen and stop.
4. **Split-screen Test:** In this test, the display is split into two pieces, upper and lower. The upper portion of the screen remains stationary, while the lower portion is slowly scrolled up over the upper, and then scrolled down, out of sight. A split screen on a standard VGA can be achieved by adjusting the Line Compare and Start Address CRTC registers.
5. **360 × 480 × 256 non-standard VGA Mode Test Pattern:** It is possible on standard VGA hardware to create a graphics mode that is 360 × 480 × 256 colors (using only the standard VGA 28-MHz dot clock). This mode is currently supported in many major software packages. This display pattern verifies correct operation of this non-standard VGA mode.
6. **Summing-to-grayscale Test:** Grayscale summing, that is, summing color values to their grayscale equivalents, 256 colors to 64 shades of gray, is verified in this test. The pattern is the same one displayed in the 256-color palette test, only in this case, the colors are summed to grayscale.
7. **12 × 80 Text Mode Test:** It is possible in mode 3, to display an stretched 8 × 16 character (pseudo 8 × 32) by performing the following:
   a) Set character font to 200 scanlines.
   b) Set mode 3, to allow 200 scanline option to take effect.
   c) Set an 8 × 16 character font on.

   This test verifies this hidden standard VGA feature.
8. **Select Scanlines Test:** This test simply displays mode 3 in 200, 350, and 400 scanlines.
9. **Reset DAC, Display Static Screens:** The DAC is reset to a color spectrum in the first screen as well as an RGB gradient in the second screen. Both screens are displayed in VGA mode 13H (320 × 200 × 256 color).
10. **Data Generator Output:** This test requests a video mode from the user. The mode is set, and the signature established by the data generator is displayed.
11. **Data Generator Tests:** The signature for each video mode is generated and compared to the known good signature.
12. **Hidden DAC Register: 8-bit Grayscale:** A test pattern is displayed with the HDR set for 8-bit grayscale.
13. **Hidden DAC Register: 3-3-2 RGB:** A test pattern is displayed with the HDR set for 3-3-2 RGB.
14. **Hardware Graphics Cursor Tests:** The hardware cursor is used in 16-color Planar and 256-color Packed-pixel modes to provide a pointer for GUI (graphical user interfaces). A hardware cursor (mouse pointer) will improve performance because the screen data will not have to be rewritten when the cursor is moved, and it will improve the appearance of the screen by providing a smoothly moving cursor. All hardware cursor tests are presently performed while in VGA mode 12H.
    At the time of this writing, plans are underway to add other hardware cursor tests in all video modes that support a hardware cursor.
    The cursor is a 32 × 32 or 64 × 64 pixel array of two planes. The following tests are performed on both the 32 × 32 and 64 × 64 hardware cursor:

a) **Pattern Address Tests:** The 32 × 32 cursor has space for a possible 64 patterns that can be loaded into video memory and be made available to any graphical application; while the 64 × 64 cursor has a possible space for 16 patterns. This test loads the highest amount of patterns possible into memory, and displays each pattern on screen.

b) **Cursor Attribute Tests:** It is possible, with the hardware cursor to set foreground and background colors for the cursor which are independent of the colors stored in the standard VGA DAC. This test verifies the correct operation of hardware cursor color 0 and 1.

c) **Cursor Attribute Tests (Inverted):** This test verifies the correct operation of the hardware cursor when programmed for inverted mode.

d) **Cursor X/Y Position Test:** In this test the hardware cursor is moved across the screen from top right-hand corner to bottom left-hand corner to verify correct graphics cursor position on screen.

e) **Cursor X/Y Position Test (Mode 5FH/64H/66H/76H):** The cursor is moved across the screen from the top right corner to the bottom left corner after first programming the appropriate extended video mode.

f) **Freestyle Test (Requires mouse driver):** This test first requests that the user specify a video mode. It sets the mode and writes a test pattern. Then the mouse will move the cursor about the screen.

15. **Write Mode Tests:** Write mode 1 as well as Extended Write modes 4 and 5 are tested in BY8 and BY16 addressing, fill, scroll, and color expansion. Tests are also performed on the 4-, 8-, and 16-byte-wide latches. The following tests are available:

a) Write mode 1, standard addressing and latches (mode 5FH) with scroll.

b) Write mode 1, BY8 Addressing, 8-byte-wide data latches (mode 5FH) with scroll.

c) Write mode 4, BY8 Addressing (mode 5FH) Fill test.

d) Write mode 4, BY8 Addressing (mode 5FH) Mask tests (2 screens).

e) Write mode 5, BY8 Addressing (mode 5FH) Mask tests (5 screens).

f) Write mode 4, Text Write test, BY8 addressing (mode 5FH).

g) Write mode 5, Text Write test, BY8 addressing (mode 5FH).

h) Write mode 4 Fill, Write mode 1 Scroll, with 8-byte-wide latches (mode 5FH).

i) Write mode 4 Monochrome Bitmap Conversion test (mode 5FH).

j) Write mode 0, with Raster Op's (GR3), 4 screens in mode 13H.

k) Write mode 0, Data Rotator test (GR3), 8 screens.

l) Write mode 1, 8-byte wide data latches (mode 64H) with scroll.

m) Write mode 4, BY16 Addressing (mode 64H) Fill test.

n) Write mode 4, BY16 Addressing (mode 64H) Mask tests (2 screens).

o) Write mode 5, BY16 Addressing (mode 64H) Mask tests (5 screens).

p) Write mode 4, Text Write test, BY16 Addressing (mode 64H).

q) Write mode 5, Text Write Test, BY16 Addressing (mode 64H).

r) Write mode 4 Fill, Write mode 1 Scroll, with 8-byte-wide latches (mode 64H).

s) Write mode 4 Monochrome Bitmap Conversion test (mode 64H).

NOTE: At the time of this publication, plans are underway to add other Write mode tests, which will include tests for the other CL-GD543X/'4X family-specific features.

16. **Signature Generator Tests:** To automatically test the CL-GD543X/'4X family video output logic at full speed, SG (Signature Generator) logic was added to the IC. The SG uses a 16-bit CCITT-standard CRC (cyclic redundancy check) algorithm, commonly used in data communications to ensure the integrity of large blocks of data. The SG operates on the Pixel Data bus P(7:0) over the active display time of a video frame. In the case of Interlaced modes, the SG operates over

one full video refresh cycle of an odd and an even frame. The data from one-bit-at-a-time of the Pixel Data bus is used by the SG to produce a unique signature for any given mode setup or video memory data.

By storing known, good values, the Manufacturing Test samples signatures from a set of display patterns, and compares the known signatures to the newly sampled signatures. If both match, then the screen is said to be correct. If a mismatch occurs, then a problem may exist in the VGA hardware or firmware. This allows the user to automatically test screen data without having to visually inspect a screen for error (which can become complicated, especially in High Color and True Color modes).

The CCITT CRC is designed to run on a serial-bit stream. The SG has a 3-bit control field to select which bit of the Pixel Data bus to run through the CRC on each frame. Checking the entire Pixel Data bus requires that a signature be taken for each Pixel Data bus bit, or eight-signatures-per-screen. Running one signature per Pixel Data bus bit helps pinpoint the cause of a failure, since seven of the SG runs may be successful and only one failed, isolating the problem to a subset of the IC pins and/or memory.

Using most of the manually viewed screens as input, signatures are captured and compared for possible errors. In operations where eliminating human error and speed in testing is important, signature testing replaces visual inspection of display screens and, in most cases, is the recommended and accurate way to test a video mode.

17. **Signature Generator Output:** This option displays the eight signatures captured for each screen tested. This information can be used to determine where a possible problem may exist within the IC.
18. **BitBLT Tests:** The following BitBLT tests are available that test all the basic BitBLT functions of the CL-GD543X/'4X family.
    a) Screen-to-screen, mode 5FH
    b) Screen-to-screen with Overlap, mode 5FH
    c) Large BitBLT, mode 5FH
    d) Large BitBLT, mode 64H
    e) Large BitBLT, mode 71H
    f) Full-screen BitBLT, mode 5FH
    g) Screen-to-off-screen-to-screen
    h) System-to-screen (9 × 4 boxes)
    i) System-to-screen (160 × 120 boxes)
    j) Pattern Copy, 8-bits (mode 5FH)
    k) Pattern Copy, 16-bits (mode 64H)
    l) Screen-to-system (160 × 120 box)
    m) Pattern Copy with Color Expand, 8-bit
    n) Pattern Copy with Color Expand, 16-bit

    NOTE: At the time of this publication, plans are underway to add other CL-GD543X/'4X family-specific BitBLT tests. These tests will be added in future updates to the manufacturing test and related documentation.
19. **Variable VCLK @ 65 MHz through 95 MHz:** This test allows the user to reset mode 71H from its default dot clock setting of 75 MHz to non-standard values in the range given above. The MHz values are selected by using the left and right arrow keys while the test pattern is visible on screen. When a new value is selected, the dot clock is reprogrammed and the resulting screen is adjusted.

20. **Variable MCLK Test @ 37 MHz through 68 MHz:** This test sets mode 3 and then allows the user to vary MCLK from 37 MHz through 68 MHz. The MHz values are selected by using the left and right arrow keys. When a new value is selected, the memory clock is reprogrammed and the resulting screen is displayed.
21. **Memory-Mapped I/O BitBLT Tests:** These are the same tests as above, except the registers are programmed using Memory-mapped I/O.

3.1 Running MFGTST From The Command Line

Running the manufacturing test with no parameters simply runs all standard tests (default test set order and selection). The following options are available from the command line:

/h	Displays a help screen while in DOS (/? also accepted)... A brief, one-screen list of valid command line options are shown. No tests are run.
/m	Runs the program in Menu Mode, as described above.
/x	Runs all self-checking tests only (register tests)... This option does not display test patterns or miscellaneous tests.
/n	Runs all display pattern tests only... This option does not run self-checking register and video RAM tests.
/d<n>	Maximum time each test pattern is displayed... The default is to wait indefinitely until a key is pressed. If <n> is not specified, default <n> is 1 second. The maximum delay is 9 seconds.
/v	Generates detailed messages on test status... Additional test information in Verbose mode is displayed for self-checking tests. Successful completion messages are generated in addition to any error messages.
/q	Do not display messages to standard output (con:), no test messages will be output to the display in Quiet mode.
/e<n>	Number of errors permitted before program aborts... The maximum number of bad register/RAM locations that will be tolerated before the program terminates (default is 1).The actual number of compare errors (on a single register/RAM location) may be higher than this number.
/w	Pause after error message (until any key pressed)...
/r<n>	Number of test passes; default <n> = 1...
/c<n>	Send message output to com<n>, default <n> = 1... <n> specifies the port to be used, and may range from 1 to 4.
/p<n>	Send message output to lpt<n>, default <n> = 1... LPT1, LPT2, or LPT3 may be selected with <n> set to 1, 2, or 3.

/f<path name>	Send message output to disk file, <path name> name of file, default = ~video.rpt... This is in addition to the screen output, unless the '/q' option has been specified. The file name may be a fully qualified (path) file name. If <path name> is not specified, the default file ~video.rpt is used. This parameter must be the last item on the command line, when several options are grouped together, e.g., /vsf err.rpt.
/+	Runs extended miscellaneous tests along with standard tests... This is a lengthy test set and should only be used when the most comprehensive test suite is desired.
/s	Runs signature testing on selected video screens...
/u	User-defined test scripts option: syntax: C:>mfgtst /u<path script-filename> This option runs the Manufacturing Test from the command line with a user-defined script file, instead of using the default tests and test order. If this option is not used, the normal default tests and order will be used during command line run.

When the script option is active, the following command line options are suppressed: '/s', '/n', and '/x'. A sample script file is available (SCRIPT.MFG) which has all the current test options available in the form of string input to the program. Only one test string may occupy a line in the script file. The script file may have any name, and may be used as many times as needed. Tests may also be in any order. While this option is active, Verbose mode ('/v') is always turned on.

NOTE: Strings in the script file must be written exactly as those shown in the sample script file. If the strings are altered, MFGTST.EXE will not recognize the test and will pass it over and go on to the next test command in the script file.

3.2 Command Line Examples

1.	MFGTST /sv	This execution invokes the self-checking register and RAM tests only. No test patterns or miscellaneous tests are displayed. Verbose mode ('/v') displays messages to the display screen indicating successful test completion.
2.	MFGTST /s /v	Same as example 1.
3.	MFGTST -sv	Same as example 1.
4.	MFGTST /nd	The display patterns are run with a maximum delay of 1 second between each screen, or until a key is pressed. No self-checking tests are run.
5.	MFGTST /f error.rpt	Message output is sent to file error.rpt in addition to the display.
6.	MFGTST /d 3	*ILLEGAL* parameter, this must be specified as /d3, as well as any other command line parameter that has <n> as a sub-parameter.

3.3 Manufacturing Test Updates

The manufacturing test is constantly updated. As more and more products are added to the CL-GD543X/'4X family of graphics controllers, more tests are added to the manufacturing test software to support new functions and features of current and future products. Contact Cirrus Logic for up-to-date manufacturing test software and documentation.

Appendix B19

Power Management

POWER MANAGEMENT

1. INTRODUCTION

The CL-GD543X/'4X family of graphics controllers features comprehensive PC-power-management functions that support compliance with the United States Environmental Protection Agency's Energy Star Computer Program, a voluntary program that promotes energy efficient technology for desktop computers. Compliance with the Energy Star Program will be a qualification for federal government purchases of computers, monitors, and printers.

The purpose of this appendix is to describe the methods used in the CL-GD543X/'4X family to comply with Energy Star.

The specific methods described in this appendix involve programming registers in the CL-GD543X/'4X. If the application program does reprogram registers, it *must* first save the register contents so that it can subsequently restore them. In addition, it may be necessary to unlock the extended registers. All this can be avoided by merely using the BIOS calls.

2. DISPLAY POWER MANAGEMENT SIGNALING – DPMS

The method by which the greatest power savings can be obtained is by putting the monitor into a low-power mode. This requires, of course, that the monitor respond to DPMS.

The Video Electronics Standards Association (VESA) DPMS Proposal defines four levels of Display Power, as shown in the following table.

Table B19-1. VESA® DPMS Proposal States

Name	Definition	HSYNC	VSYNC
On	Full operation	Active	Active
Stand-by	Optional state of minimal power reduction	Inactive	Active
Suspend	Significant reduction of power consumption	Active	Inactive
Off	Lowest level of power consumption	Inactive	Inactive

3. VESA® VBE/PM BIOS FUNCTIONS

The CL-GD545X family is fully compliant with the VESA Display Power Management BIOS Extensions, VBE/PM. The following is a description of these calls.

3.1 Report VBE/PM Capabilities

Input:	AH = 4fh	VESA Extension
	AL = 10h	VBE/PM Services
	BL = 00h	Report VBE/PM Capabilities

	ES:DI		Null pointer, must be 0000:0000h Reserved for future use
Output:	AX =		Status
	BH =		Power saving state signals supported by the controller (Note 1) 1 = supported, 0 = not supported
		bit 0	STAND BY
		Bit 1	SUSPEND
		Bit 2	OFF
		Bit 3	REDUCED ON (intended for flat panel displays)

Note 1: The attached display may not support all the power states that can be signaled by the controller. It is the responsibility of the power management program to determine the power saving states that are offered by the controller. If the controller has a means of determining which power saving state that is implemented in the attached display device, this function reports the power saving states that are supported by both the controller and the display.

3.2 Set Display Power State

Input:	AH = 4fh		VESA Extension
	AL = 10h		VBE/PM Services
	BL = 01h		Set Display Power State
	BH =		Requested Power state
		00h	ON
		01h	STAND BY
		02h	SUSPEND
		04h	OFF
		08h	REDUCED ON (intended for flat panel displays)
Output:	AX =		Status: If the requested state is not available, this function will return AX = 14h to indicate that the function is supported but the call failed. The BH register and Display Power State shall be left unchanged in this case.
	BH =		Unchanged

3.3 Get Display Power State

Input:	AH = 4fh		VESA Extension
	AL = 10h		VBE/PM Services
	BL = 02h		Get Display Power State
Output:	AX =		Status: If this function is not supported by the controller hardware, AL=01 should be returned in the status.
	BH =		Power state currently requested by the controller
		00h	ON
		01h	STAND BY
		02h	SUSPEND
		04h	OFF
		08h	REDUCED ON (intended for flat panel displays)

4. STATIC HSYNC/VSYNC

HSYNC will be static if GRE[1] is programmed to '1'. The sense will be as programmed into MISC[6]. VSYNC will be static if GRE[2] is programmed to a '1'. The sense will be as programmed into MISC[7].

If either GRE[1] or GRE[2] is programmed to '1', the RAMDAC will be powered-down. This satisfies the requirement in the VESA proposal which states, "...host system sets the video image information to the blank level prior to the host transmitting the stand-by/suspend/OFF signal to the display". In addition, this reduces the power in the chip itself.

5. STATIC CLOCK MODE/SYSTEM LEVEL (CL-GD5436 only)

For the CL-GD5436 only, if GRE[3] is programmed to '1', the device is put into Suspend mode. VCLK and MCLK are gated off, reducing the dynamic power dramatically. DRAM refresh continues. In addition, the DAC is set to Power-down mode. This provides system-level power management, which is not part of DPMS. In Static Clock mode display memory and the palette registers cannot be accessed.

If GRE[4] is programmed to '1', host access to display memory and screen refresh are disabled. This bit must be programmed to '1' before GRE[3] is programmed to '1', and must be programmed to '0' only after GRE[3] is programmed to '0'. The MCLK and VLCK VCOs continue to operate at their programmed frequencies, but the device consumes very little power.

GRE[3] and GRE[4] should be used together to minimize power dissipation in the device.

6. VIDEO CLOCK/DISPLAY MEMORY REFRESH (CL-GD5430/'34/'40)

The following procedure may be used to reduce power in the CL-GD5430/'34/'40. This is provided as a substitute for the Static Clock mode/System Level mentioned above.

The Video clock can be reduced to as low as 3.47 MHz, and the DRAM refresh can be reduced to 5 cycles every 4.6 µsec. without losing the contents of display memory. This reduces the power in the DRAM array and also reduces the power in the chip. This provides system-level power management, which is not part of DPMS. When the chip is in Low-power mode, display memory and the palette registers cannot be accessed. The following steps are involved:

1. Divide DCLK by two and select 8 pixels-per-character
   - Program SR1 to 29h
2. Select VCLK0
   - Program MICS[3:2] to 00h
3. Set VCLK0 to 3.47 MHz
   - Program SR0B to 20fh
   - Program SR1B to 3fh
4. Unlock Horizontal Timing and select 5 refresh cycles per scanline
   - Program CR11 to 40h
5. Set Horizontal Total to 14 character clocks
   - Program CR0 to 09h
6. Set other horizontal parameters to be consistent with HTOTAL of 16
   - Program CR1 to 02h

- Program CR4 to 03h
- Program CR5 to 02h

6.1 Memory Clock

MCLK can be reduced to as low as 7.14 MHz. This reduces the power in the chip. To reduce power, program SR1F to 04h.

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Appendix B20

Memory-Mapped I/O

MEMORY-MAPPED I/O

1. INTRODUCTION

The CL-GD543X/'4X allows application programs to access the BLT-control registers as memory locations. This can be up to four times faster than using I/O accesses when multiple registers must be changed at once. The register address is implied in the address rather than being transferred as part of the data (the index field). This doubles the data transfer rate at once. Since DWORD transfers are allowed, the data transfer rate is doubled again.

Memory-mapped I/O is enabled when SR17[2] is programmed to '1'. GR6[3:2] must be programmed to '0,1'. This means that if the CL-GD543X/'4X is not programmed for Linear Addressing, the window into display memory is 64K (A000:0–AFFF:F).

A block of 256 bytes of memory address space is reserved beginning at B800:0 (Address bits 14:8 are 'don't care' so the block is actually aliased at every 256 boundary from B800:0–BFF0:0). This block can be accessed using BYTE, WORD, or DWORD cycles. All registers are write-only with memory-mapped I/O, except GR31 which is read/write. In local bus configurations, the CL-GD543X/'4X will return RDY# if write-only memory-mapped registers are read, but the data are indeterminate. When memory mapped I/O is enabled, ordinary I/O may still be used.

For the CL-GD5430/'36/'40 only, if linear addressing is enabled and SR17[6] is programmed to '1', the memory address space will be at the highest 256 bytes of the linear address space. If linear addressing is not enabled, SR17[6] is a don't care.

Table B20-1 indicates the registers that are accessible using memory-mapped I/O.

Table B20-1. Registers Accessed Using Memory-Mapped I/O

Offset (Hex.)	Register	Description	CL-GD5430/'40
00	GR0	Background Color Byte 0	Yes
01	GR10	Background Color Byte 1	Yes
02	GR12	Background Color Byte 2	No
03	GR14	Background Color Byte 3	No
04	GR1	Foreground Color Byte 0	Yes
05	GR11	Foreground Color Byte 1	Yes
06	GR13	Foreground Color Byte 2	No
07	GR15	Foreground Color Byte 3	No
08	GR20	BLT Width Byte 0	Yes
09	GR21	BLT Width Byte 1	Yes

Table B20-1. Registers Accessed Using Memory-Mapped I/O *(cont.)*

Offset (Hex.)	Register	Description	CL-GD5430/'40
0A	GR22	BLT Height Byte 0	Yes
0B	GR23	BLT Height Byte 1	Yes
0C	GR24	BLT Dest Pitch Byte 0	Yes
0D	GR25	BLT Dest Pitch Byte 1	Yes
0E	GR26	BLT Source Pitch Byte 0	Yes
0F	GR27	BLT Source Pitch Byte 1	Yes
10	GR28	BLT Dest Address Byte 0	Yes
11	GR29	BLT Dest Address Byte 1	Yes
12	GR2A	BLT Dest Address Byte 2	Yes
13	GR2B	Reserved	No
14	GR2C	BLT Source Address Byte 0	Yes
15	GR2D	BLT Source Address Byte 1	Yes
16	GR2E	BLT Source Address Byte 2	Yes
17	GR2F	BLT Destination Write Mask	Yes
18	GR30	BLT Mode	Yes
19	–	Reserved	No
1A	GR32	BLT Raster OP	Yes
1B	GR33	BLT Reserved	No
1C-3F	–	Reserved	No
40	GR31	BLT Start/Status (R/W)	Yes
41-FF	–	Reserved	No

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Appendix C1

Software Support

SOFTWARE SUPPORT

1. INTRODUCTION

The CL-GD543X/'4X family of VGA controllers comes with the CL-GD543X/'4X VGA BIOS and an extensive set of utilities and software drivers. The following sections briefly describe some of the utilities and software drivers available.

To get an up-to-date list of BIOS, utilities, and software drivers supported refer to the latest release of CL-GD543X/'4X VGA BIOS and utilities or the CL-GD543X/'4X Display Drivers Release Kits. These programs also available on the Cirrus Logic BBS (see Appendix D9 for further information on the BBS).

2. CL-GD543X/'4X VGA SOFTWARE UTILITIES

This section describes the software utilities provided with the CL-GD543X/'4X VGA controllers, and explains the function and usage of each.

2.1 CLMODE — A CL-GD543X/'4X Video Mode Configuration Utility

The CL-GD543X/'4X VGA controllers have many more video modes than the original IBM VGA. Some of these are: 132-column Text, 1280 × 1024 × 16/256-color Graphics, 1024 × 768 × 32K/64K Direct Color, and 16.8 million True Color modes. To take advantage of these features, a compatible monitor must be installed, and the proper monitor parameters need to be selected.

The CLMODE utility provides a number of graphics configuration options, all of which are selectable from a menu or by direct keyboard input at the DOS command line. The menu options include:

- Monitor-type selection based on monitor vertical and horizontal sync frequencies
- Selection and setting of CL-GD543X/'4X VGA BIOS Standard and Extended Video modes
- Extended Video mode preview to verify high-resolution modes supported by the video subsystem
- Selection and setting of video refresh rates for each individual video mode resolution (that is, 640 × 480, 800 × 600, 1024 × 768, and 1280 × 1024) to match video refresh rates supported by a monitor

2.2 VGA.EXE — RAMBIOS Utility

This VGA.EXE utility is an executable version of the VGA BIOS EPROM code that can be loaded into DOS memory. VGA.EXE utility allows the VGA BIOS to be executed out of 16- or 32-bit system memory, instead of an 8- or 16-bit bus ROM. This permits for most operations that use the VGA BIOS to run much faster.

The most noticeable performance boost is in text modes where VGA BIOS character-write and text-scrolling functions are used. Common benchmark programs that can be used to demonstrate this increase in performance are PC Bench™ from Ziff-Davis® Publishing Com-

However, most Graphical User Interface (GUI) applications do not use the BIOS heavily, so actual performance increases varies between applications, and in some cases may not be significant.

Many of the newest '386 and later PCs automatically cache (copy into system memory) the VGA BIOS upon booting the machine. This is sometimes called 'Shadow RAM'. In this case, the BIOS is already executing out of 16- or 32-bit memory, and the VGA.EXE utility is not necessary.

The VGA.EXE utility can be executed from the command line or named in the AUTOEXEC.BAT. The utility will then automatically install itself in system memory at the correct address, shortly after power-on or a warm-boot.

The RAMBIOS utility only works with MS-DOS or PC-DOS, and does not work with OS/2™, Unix®, or Xenix®.

2.3 OEM System Integration (OEMSI) Utility

The OEM System Integration (OEMSI) utility enables the Cirrus Logic VGA BIOS to be customized to system requirements. Since OEMSI operates upon the binary (executable) image of the BIOS, source code is no longer necessary for customization. Several different derivative BIOSes can easily be generated from the same core, which reduces maintenance problems and simplifies software-generation control. If OEMSI is used, the RAM BIOS should not be shipped since its use would override the changes.

A wide range of parameters, default values, and tables can easily be modified or replaced using the OEMSI program. The following is a list of components of the Cirrus Logic VGA BIOS that can be modified with the OEMSI program:

Sign-on Message. In addition to the Cirrus Logic copyright notices displayed when the system boots-up, custom copyright messages may be inserted. The positioning of the cursor, after the copyright messages have been displayed, can also be changed.

Monitor-type Configuration. The mechanism for how monitor type is determined can be selected by reading software-configuration switches, or by a Software Interrupt 15H call.

Hardware Configuration Registers. The CL-GD543X/'4X VGA BIOS hardware configuration table includes register values that are programmed at POST. This allows customizing of register values that program video dot clocks, memory clocks, and other programmable settings.

Video Mode Parameter Tables. These tables contain the complete set of register values for each Standard and Extended Video mode. Values for both the Standard VGA registers and Cirrus Logic Extension registers are contained in these tables, and can be customized to configure video refresh rates for individual video mode resolutions.

Font Tables. All fonts used by the Cirrus Logic VGA BIOS can be modified or completely replaced by using the OEMSI utility. A flexible scheme is implemented, whereby font tables can be exported from the binary image of the BIOS or imported to it.

2.4 WINMODE Utility

The WINMODE utility is a Windows application that can be used to conveniently set the resolution and number of colors of the display.

3. CL-GD543X/'4X VGA SOFTWARE DRIVERS

Several text and graphics device drivers are available to enhance the operation of VGA graphics applications.

3.1 Driver Applicability

The CL-GD543X/'4X VGA controller needs no software drivers to run applications in Standard VGA modes. The drivers listed in Table C1-1 are provided as a service to the user for improved resolution and performance to many software packages.

Cirrus Logic recognizes that quality device drivers are an important feature of any video subsystem, and as such our list of available device drivers is continuously expanding. For the latest list of available device drivers, please refer to the CL-GD543X/'4X Software Drivers and Utilities Kit.

Table C1-1. Software Drivers Support

Software Drivers	Resolution Supported[a]	No. of Colors
Microsoft® Windows® v3.1	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600, 1024 × 768	256 65,536 16.8 million
Microsoft® Windows NT™ v3.1	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	16 and 256
Microsoft® Windows NT™ v3.5	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	16 256 65,536
Microsoft® Windows NT™ v3.5 for PowerPC™	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	16 256 65,536
OS/2® v2.1, v2.1.1, v3.0	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480	256 65,536 16.8 million
AutoCAD® v11, v12 Autoshade® v2.0 w/ Renderman, 3D Studio v1, v2	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600, 1024 × 768	16 256 32,768 65,536 16.8 million
WordStar® v5.5–7.0	800 × 600, 1024 × 768	16
SCO[b] UNIX®	640 × 480, 800 × 600, 1024 × 768	16 and 256

[a] All resolutions may not run on all monitor types; 640 × 480 drivers will run on IBM® PS/2®-type monitors. Extended resolutions are dependent upon monitor type and VGA system implementation.

[b] Shipped by Santa Cruz Operations.

Appendix D1

D

Programming Examples

Table of Contents

PROGRAMMING EXAMPLES

1. INTRODUCTION

This appendix comprises software programming examples that demonstrate how to implement the following features of the CL-GD543X/'4X:

- Identifying Cirrus Logic CL-GD543X/'4X Controllers (if no Cirrus Logic BIOS is available)
- Initializing CL-GD543X/'4X Video modes via INT 10H call
- Programming Single-page mapping
- Programming Double-page mapping

2. SUPER VGA DISPLAY MODES

The table on the inside front cover summarizes the CL-GD543X/'4X extended VGA Display modes. A more complete table is given in Table 4-2 of the Data Book, which is reproduced as Chapter 3 of this book.

The pixel formats are covered in Appendix B6. Table D1-1 summarizes the pixel formats as a function of Video mode:

Table D1-1. Extended Modes

Mode Number*	Resolution	Colors	Bits/ Pixel	Memory Organization	Minimum Memory [f]	Pitch [g]
58h, 6Ah	800 × 600	16	4	Planar	512K	
5Ch	800 × 600	256	8	Packed	512K	800
5Dh	1024 × 768	16	4	Planar	512K	
5Eh	640 × 400	256	8	Packed	512K	640
5Fh	640 × 480	256	8	Packed	512K	640
60h	1024 × 768	256	8	Packed	1M	1024
64h	640 × 480	64K	16	RGB[b] (5-6-5) Packed	1M	1280
65h	800 × 600	64K	16	RGB[b] (5-6-5) Packed	1M	1600
66h	640 × 480	32K	15/8	Mixed[c] RGB (5-5-5)/ 256-colors Packed	1M	1280
67h	800 × 600	32K	15/8	Mixed[c] RGB (5-5-5)/ 256-colors Packed	1M	1600
68h	1024 × 768	32K	15/8	Mixed[c] RGB (5-5-5)/ 256-colors Packed	2M	2048

Table D1-1. Extended Modes *(cont.)*

Mode Number*	Resolution	Colors	Bits/ Pixel	Memory Organization	Minimum Memory [f]	Pitch [g]
69h	1280 × 1024	32K	15/8	Mixed[c] RGB (5-5-5)/ 256-colors Packed	4M	2560
6Ch	1280 × 1024	16	4	Planar	1M	
6Dh	1280 × 1024	256	8	Packed	2M	1280
71h	640 × 480	16M	24	RGB[d] (8-8-8) Packed	1M	2048
72h	800 × 600	16M	32	xRGB[e] (8-8-8-8) Packed	2M	3200
73h	1024 × 768	16M	32	xRGB[e] (8-8-8-8) Packed	4M	4096
74h	1024 × 768	64K	16	RGB[b] (5-6-5) Packed	2M	2048
75h	1280 × 1024	64K	16	RGB[b] (5-6-5) Packed	4M	2560
76h	640 × 480	16M	32	xRGB[e] (8-8-8-8) Packed	2M	2560
77h	640 × 400	64K	16	RGB[b] (5-6-5) Packed	1M	1280
	800 × 600	16M	24	RGB[d] (8-8-8) Packed	2M	3072
	1024 × 768	16M	24	RGB[d] (8-8-8) Packed	2M	3072

NOTES:

a) The 32,768 Color Video modes are RGB (5-5-5) packed-pixel modes compatible with industry standards.

b) The 65,536 Color Video modes are RGB (5-6-5) packed-pixel modes compatible with industry standards.

c) The mixed format allows 32,768 Color Video modes RGB (5-5-5) and 256 colors (8 bits-per-pixel) packed format to be combined.

d) The 640 x 480 x 16.8M True Color Video mode with 1024K display memory is RGB (8-8-8) Packed-pixel modes compatible with 24-bit-per-pixel TARGA Truevision® format.

e) With 2048K or 4096K of display memory, some CL-GD5434 16.8M-Direct Color video modes run in 32-bit-per-pixel mode with a high-byte of 32 bits used as 'color key' overlay control (see Appendix B14, *Video Overlay and DAC Mode Switching*). The CL-GD5430 uses 24-bit modes exclusively.

f) The minimum memory configuration for the CL-GD543X/'4X is 512 Kbytes (even though some video modes actually require less). One Mbyte modes typically use a granularity of 4K; 2-, and 4-Mbyte modes must use a granularity of 16K.

g) 'Pitch' is the distance, in bytes, between vertically adjacent pixels. The offset from the beginning of display memory to (the first byte of) any pixel may be calculated with:

$$Offset = X + (Y \times Pitch)$$

3. EXTENDED VIDEO MEMORY ADDRESSING TECHNIQUES

The CL-GD543X/'4X is capable of addressing up to 4 Mbyte of display memory. In the DOS environment, there is 128 Kbytes of memory space at A0000–BFFFF reserved for display memory. Since the VGA may have to share this memory with MDA, Hercules, or CGA, it is left with the single 64-Kbyte segment from A0000 to AFFFF.

The CL-GD543X/'4X supports single- and dual-paging display memory addressing schemes that allow mapping of two 32-Kbyte segments, or one 64-Kbyte segment of display memory into CPU address space.

The CL-GD543X/'4X also supports a linear address mapping scheme that allows the display memory to be mapped to a continuous 4-Mbyte region above the standard DOS address space. This allows application programs to access the full 4 Mbytes of display memory instead of being constrained to a 64-Kbyte window. Linear addressing is discussed in Appendix D2.

3.1 Single-Page Addressing

The single-page addressing scheme allows a 64-Kbyte segment of display memory to be mapped to the A0000–AFFFF of CPU address range. The segment of display memory that is mapped into the CPU address range is selected by programming the Extension register GR9: Offset register 0 (I/O Port Address 3CF, Index = 0 x 09). The detailed interpretation of the contents of GR9 depends on the granularity. See Figure D1-1 below.

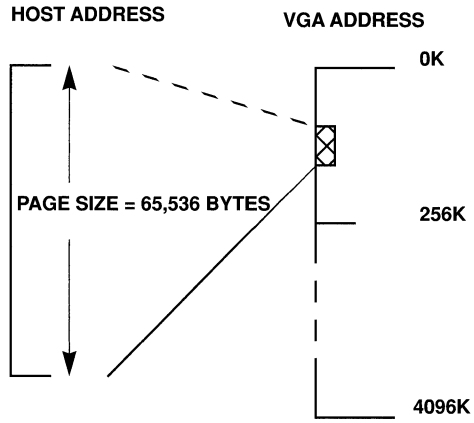


Figure D1-1. Single-Page Mapping Scheme

3.2 Dual-Page Addressing

The dual-page addressing scheme allows two segments of display memory to be mapped into the CPU address range. The two segments are mapped into address range A0000–A7FFF and A8000–AFFFF. The two segments of display memory mapped into the CPU address ranges are set by Offset register 0 (GR9) and Offset register 1 (GRA). The two segments in the display memory may have any relationship, including overlapping. The advantages of dual-page addressing are largely superseded by the BitBLT engine.

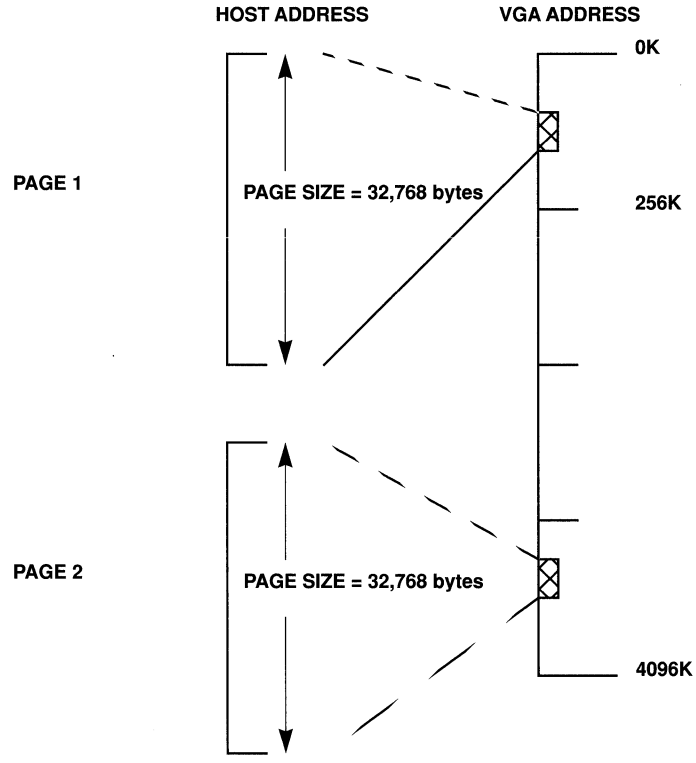


Figure D1-2. Dual-Page Mapping Scheme

3.3 Single Page Remapping with 4-Kbyte Granularity

Figure D1-3 shows how the Offset register (GR9) and the CPU Address bits are added together to generate the Display Memory Address. The low order 12 bits of CPU address directly specify the low order 12 bits of memory address. Bits 15:12 of the CPU address, with four high order zeroes, are added to the 8 bits of offset register contents to form the eight high order bits of memory address. A carry out is possible and is undetected.

This mode allows access to a 64K window beginning on any 4K boundary. This mode allows access to only the first 1 Mbyte of display memory and so would not be applicable for modes requiring more than 1 Mbyte.

GRB[5] is programmed to '0' and GRB[0] is programmed to '0' to select this mode.

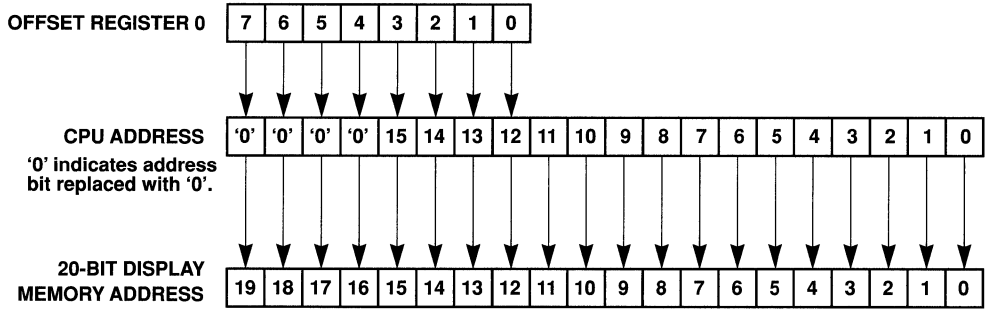


Figure D1-3. Single Page Mode Remapping Adder Alignment with 4-Kbyte Granularity

3.4 Single-Page Mapping with 16-Kbyte Granularity

Figure D1-4 shows how the Offset register (GR9) and the CPU Address bits are added together to generate the Display Memory Address for 16-Kbyte granularity. The low-order 14 bits of CPU address directly specify the low-order 14 bits of memory address. Bits 15 and 14 of the CPU address, with six high-order zeroes, are added to the 8 bits of the offset register contents to form the eight high order bits of memory address. A carry out is possible and is undetected.

This mode allows access to a 64K window on any 16K boundary. This modes allows access to up to four Mbytes of display memory and so can be used for any mode.

GRB[5] is programmed to '1' and GRB[0] is programmed to '0' to select this mode.

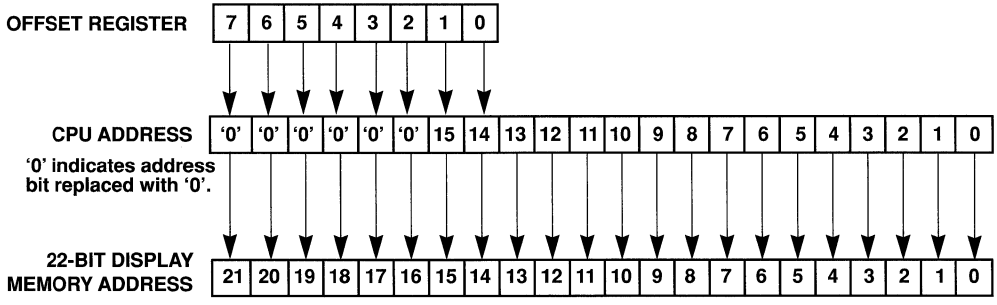


Figure D1-4. Single Page Mode Remapping Adder Alignment with 16-Kbyte Granularity

3.5 Dual-Page Mapping with 4-Kbyte Granularity

Figure D1-5 shows how either one of the two Offset registers (GR9 and GRA) and the CPU Address bits are added together to generate the Display Memory Address. The low-order 12 bits of CPU address directly specify the low-order 12 bits of memory address. Bits 14:12 of the CPU address, with five high-order zeroes, are added to the 8 bits of offset register to form the eight high order bits of memory address. A carry out is possible and is undetected.

CPU address bit 15 is used to choose between Offset register 0 and Offset register 1. Table D1-2 summarizes this.

Table D1-2. Offset Register Addressing

CPU Address 15	Address Range	Offset Register
0	A0000–A7FFF	0 (GR9)
1	A8000–AFFFF	1 (GRA)

This mode allows two 32K windows, each beginning of any 4K boundary. The two windows may have any relationship in display memory. This mode allows access to only the first 1 Mbyte of display memory and so would not be applicable for video modes requiring more than 1 Mbyte.

GRB[5] is programmed to '0' and GRB[0] is programmed to '1' to select this mode.

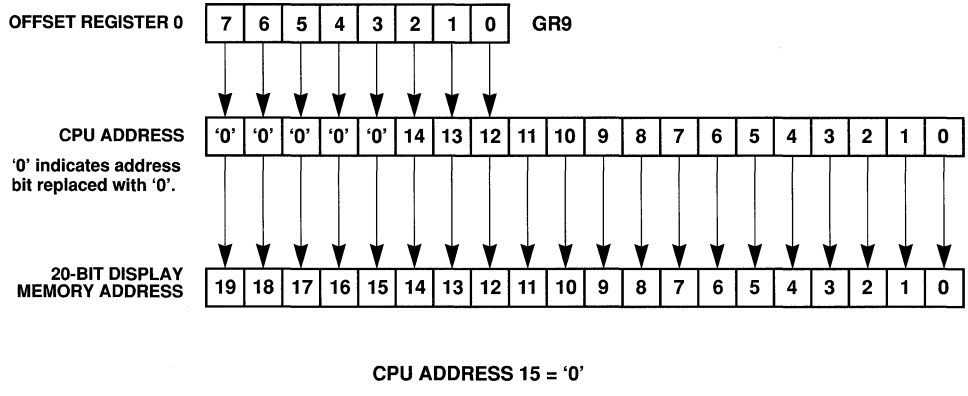


Figure D1-5. Dual-Page Mode Remapping Adder Alignment with 4-Kbyte Granularity

3.6 Dual-Page Mapping with 16-Kbyte Granularity

Figure D1-6 shows how either one of the two Offset registers (GR9 and GRA) and the CPU Address bits are added together to generate the Display Memory Address. The low order 14 bit of CPU address directly specify the low order 14 bits of memory address. Bit 14 of the CPU address, with seven high order zeroes, are added to the 8 bits of offset register to form the eight high order bits of memory address. A carry out is possible and is undetected.

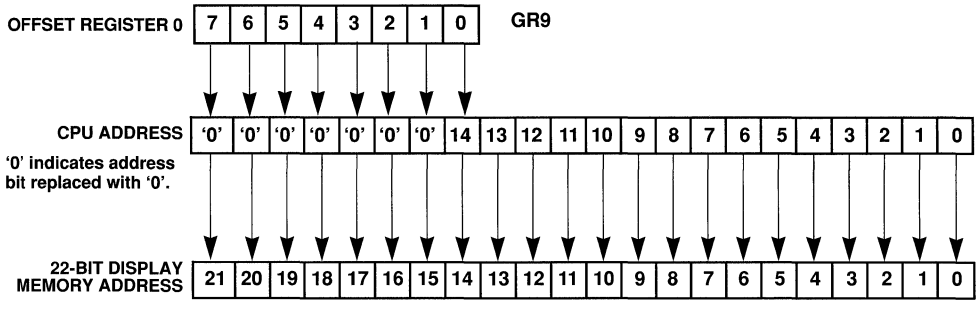
CPU address bit 15 is used to choose between Offset register 0 and Offset register 1. Table D1-3 summarizes this.

Table D1-3. Offset Register Addressing

CPU Address 15	Address Range	Offset Register
0	A0000-A7FFF	0 (GR9)
1	A8000-AFFFF	1 (GRA)

This mode allows two 32K windows, each beginning on any 16K boundary. The two windows may have any relationship in display memory. This modes allows access to up to four Mbytes of display memory and so can be used for any mode.

GRB[5] is programmed to '1' and GRB[0] is programmed to '1' to select this mode.



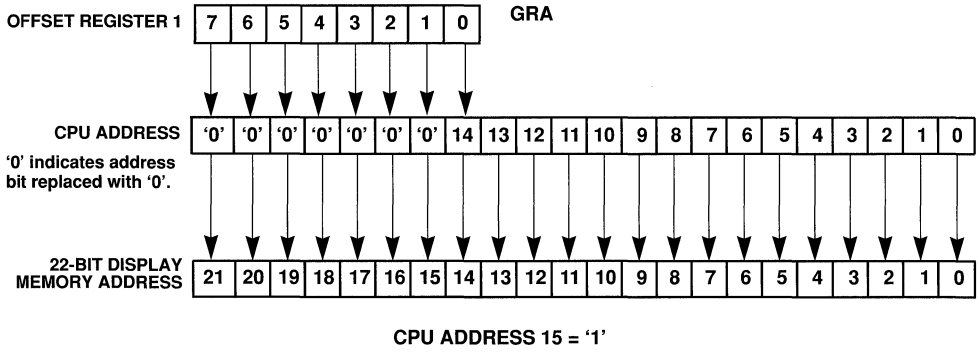


Figure D1-6. Dual-Page Mode Remapping Adder Alignment with 16-Kbyte Granularity

3.7 CL-GD543X/'4X Memory Addressing Registers

The following table lists the CL-GD543X/'4X Extension registers that control the CPU Base Address and display memory mapping functions:

Table D1-4. CL-GD543X/'4X Extension Registers

Function	Register Name	Port	Index	Bit	Value
Single-Page	GRB: Graphics Controller Mode Extensions	3CF	0B	0	0
Dual-Page	GRB: Graphics Controller Mode Extensions	3CF	0B	0	1
4K Granularity	GRB: Graphics Controller Mode Extensions	3CF	0B	5	0
16K Granularity	GRB: Graphics Controller Mode Extensions	3CF	0B	5	1
Linear Addressing	SR7: Graphics Controller Mode Extensions	3C4	07	7:4	15..0
Offset register 0	GR9: Offset register 0	3CF	09	7:0	255..0
Offset register 1	GRA: Offset register 1	3CF	0A	7:0	255..0

Figures D1-7 and D1-8 below show the Extension registers that control the Extended Memory Mapping Functions.

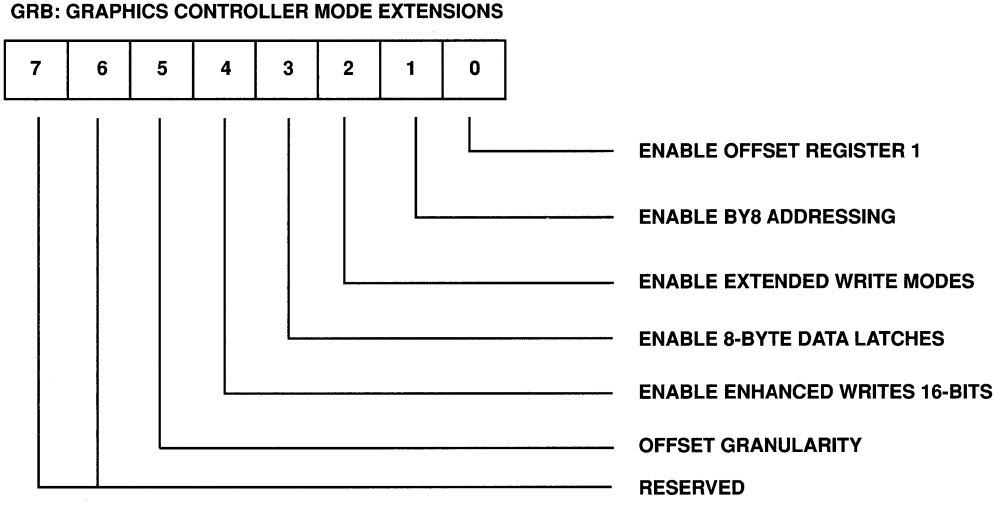


Figure D1-7. Extension Register GRB

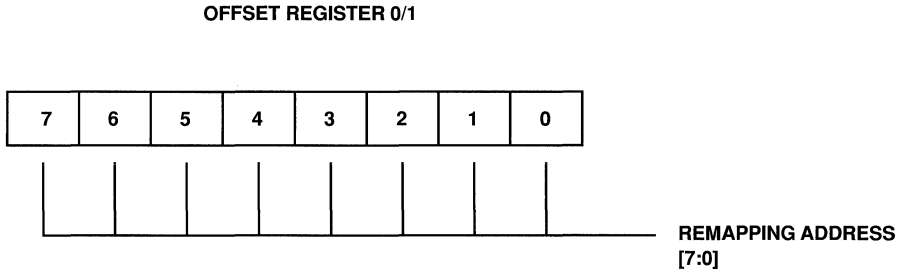


Figure D1-8. Extension Register GR9/GRA

4. VGA PROGRAMMING EXAMPLES

This section provides the software programming examples with source code listing and discussion on the following topics:

- Identifying CL-GD543X/'4X VGA Controllers (when no Cirrus Logic BIOS is available)
- Programming CL-GD543X/'4X Extended Video modes via INT 10H Function Call
- Enabling/disabling Extension register access
- Selecting Single-page Mapping
- Selecting Dual-page Mapping
- Loading Single-page Bank with a new start address
- Loading Dual-page Banks with new start addresses
- Calculating new start address and loading Single-page Bank

4.1 Identifying the CL-GD543X/'4X Controllers (No Cirrus Logic BIOS)

The CL-GD543X/'4X can be identified by calling the Extended VGA BIOS inquiry function via INT 10H (See Appendix E1, "VGA BIOS Specification", for further information). If a VGA BIOS is not available, then the controller can by identified by programming the enable/disable Extension register (SR6) and reading the Chip ID register (CR27). The following code shows the steps to enable/disable CL-GD543X/'4X Extended register access.

The CL-GD5430 and CL-GD5440 implement SR6, and the value read from it will be 12h or 0Fh as decribed in Chapter 9. The extension registers, however, will never be locked.

```
Enable Extension Register Macro:
;           Function:
;           Enabling Extensions
;            Calling Protocol:
;           enable_extensions

            enable_extensions macro
            mov   dx,03c4h              ; select Sequencer Registers i/o port
            mov   al,06h                ; Unlock All Extension register index
            mov   ah,12h                ; load with xxx1x010 to unlock extension
            out   dx,ax                 ; write index and data
            endm

Disable Extension Register Macro:

            ; Function:
            ;     Disabling Extensions

            ; Calling Protocol:
            ;     disable_extensions

            disable_extensions macro
            mov   dx,03c4h              ; select Sequencer Register i/o port
            mov   al,06h                ; Unlock All Extension register index
            mov   ah,00h                ; load with 00 to disable extension
            out   dx,ax                 ; write index and data
            endm
```

4.2 Determining if VGA Controller is a CL-GD543X/'4X

Chip ID register (CR 27) is used to identify the CL-GD543X/'4X. The following sample code shows how to program the Extension registers to read the Chip ID and determine the chip type:

```
;Function: Identify Cirrus Logic CL-GD543X/'4X VGA controller
;Input Parameters:none
;Output Parameters:
;      AL =00h   Cirrus Logic CL-543X/'4X Not present
;      AL =31h   CL-GD5434
;      AL =32h   CL-GD5430
;      AL =34h   CL-GD5440
;      AL =??h   CL-GD5436
; Calling Protocol:
; VGAchip = Id_GD543X4X();

_Id_GD543X4X proc far
      mov       dx,3c4h      ; load Unlock All Extensions I/O port
      mov       ax,1206h     ; load SR6 index and "unlock" data
      out       dx,ax        ; write index and data register
      inc       dx           ;
      in        al,dx        ; read SR6
      cmp       al,12h       ; check SR6 read back value
      jne       fail         ; no SR6 means no Alpine
      mov       dx,3cch      ; MISC: Miscellaneous Output Register
      in        al,dx        ; read CRTC I/O address select (bit 0)
      mov       dx,3b4h      ; monochrome index for CRTC regs
      and       al,1         ; 3CC[bit0]: 1=color(3d4h), 0=mono (3b4h)
      jz        read_id      ;
      mov       dx,3d4h      ; choose color index for CRTC regs
read_id:
      mov       al,27h       ; select CR27 index
      out       dx,al        ; point to CR27
      inc       dx           ;
      in        al,dx        ; read chip id
      and       al,fch       ; drop revision bits
      mov       ah,31h       ;
      cmp       al,a8h       ; check if GD5434
      je        exit         ;
      mov       ah,32h
      cmp       al,a0h       ; check if GD5430
      je        exit
      mov       ah, ??h      ;insert BIOSs code for 36 here
      cmp       al, ach      ;check if GD5436
      je        exit
      mov       ah, 34h
      cmp       al, b0h      ;check if GD5440
      je        exit
fail:
      mov       ah,00h       ; no match, chip id-failed
exit:
      mov       al,ah        ; return in AL the chip id value
      ret
_Id_GD543X4X endp
```


4.3 Initializing CL-GD543X/'4X Super VGA Mode Via INT 10H Call

The following listing is used to initialize the desired video mode by calling the Cirrus Logic VGA BIOS Set Mode function:

```
;Set Video Mode
;set up Extended Video mode supported by CL-GD543X/'4X VGA BIOS
;
;Calling Protocol
; al = desired CL-GD543X/'4X video mode number
;Return
; al = current video mode
;
Set_Video_Mode proc near
      mov ah,0 ; VGA BIOS setmode function 0
      int 10H  ; call VGA BIOS interrupt 10 Hex, al= mode number
      mov ah,0Fh; VGA BIOS get current video mode number
      int 10h  ;
      ret      ; return current video mode number in al so that calling
               ; routine can verify that the mode got set correctly
Set_Video_Mode endp
```

4.4 Programming Single-Page Mapping

The following listing shows the Extension registers that need to be programmed to set up CL-GD543X/'4X Single-page Mapping. Note that this routine does not change the granularity from whatever it may be:

```
; Single Page Mapping
; Setup Single-Page Mapping

; Calling Protocol
;     Set_Single_Page

Set_Single_Page proc near
;setup CPU Base Address Control Register for single page, 64k page size
      mov      dx,03ceh    ; select graphics register i/o port
      mov      al,0bh      ; select GRB register index
      out      dx,al       ; write index register
      inc      dx          ; inc dx to read data port
      in       al,dx       ; read data
      and      al,0feh     ; apply mask to set GRB[0] = 0
      out      dx,al       ; write i/o port with new data
      ret
Set_Single_Pageendp
```

4.5 Programming Dual-Page Mapping

The following listing shows the Extension registers that need to be programmed to set up CL-GD543X/'4X Dual-page Mapping. Note that this routine does not change the granularity from whatever it is:

```
; Dual Page Mapping
;     Setup Dual-Page Mapping
;
; Calling Protocol
;     Set_Dual_Page

Set_Dual_Page proc far

; setup Graphics Controller Mode Extensions Register for dual page size
      mov       dx,03ceh     ; select graphics register i/o port
      mov       al,0bh       ; select GRB index
      out       dx,al        ; write index register
      inc       dx           ; inc dx to read data port
      in        al,dx        ; read data
      or        al,01h       ; data = enable 32k pagesize, dual page
      out       dx,al        ; write i/o port with new data
      ret
Set_Dual_Page  endp
```

4.6 Programming the Address Remapping Registers

The Offset registers contain the eight most-significant bits of the 1-Mbyte address range that can be mapped into the limited CPU address range of A0000–BFFFF. If Single-page Mapping is selected, the page size is 64 Kbytes and the display memory is mapped into CPU address range A0000–AFFFF. The 64-Kbyte segment that is remapped into CPU address range can start at any 4- or 16-Kbyte address boundary of display memory based on programming of offset granularity (bit 5) in GRB register. This means that with 1-Mbyte of display memory and 4-Kbyte granularity, the Remapping registers can select any one of the possible 256 start address locations.

The following examples shows how to select the desired page for Single-page Mapping with 64-Kbyte page size, and Dual-page Mapping with 32 Kbyte page size.

4.7 Single-Page Remapping with a 64-Kbyte Segment Address

The following listing shows how the Extension Offset register 0 needs to be programmed to map a desired page (64 Kbytes) of display memory into CPU address at segment A000:

```
;Function:
;Load the Single Page Offset Register 0 with the new start address
;of a 64K byte segment
; Input:
; bl = 0..255
; page number for start address of desired 64k byte segment
;
; Calling Protocol:
; Select_Single_Page

Select_Single_Page macro
      mov       dx,3CEh      ; load GR09 extension register i/o port
      mov       al,09h       ; load Offset Register 0 index
      mov       ah,bl        ; get page number
      out       dx,ax        ; program selected page
Select_Single_Page endm
```

4.8 Dual-Page Remapping with a 32-Kbyte Segment Bank Address

The following listing shows the Extension registers that need to be programmed to set up Dual-page Remapping Address with a 32-Kbyte Segment Bank Address:

```
;Function:
;Load the Dual Page Remapping Registers with the new star address
;at 32K byte segments

; Input:
;bl = 0..255 page number for segment mapped to A0000 - A7FFF
;bh = 0..255 page number for segment mapped to A8000 - AFFFF

; Calling Protocol:
;Select_Dual_Pages

Select_Dual_Pages macro
mov   dx,3CEh   ; load extension register i/o port
mov   al,09h    ; load CPU Base Addr. Mapping Register A index
mov   ah,bl     ; get page number for A0000-A7FFF mapping
out   dx,ax     ; program selected page
mov   al,0ah    ; load CPU Base Addr. Mapping Register A index
mov   ah,bh     ; get page number for A8000-AFFFF mapping
out   dx,ax     ; program selected page
Select_Dual_Pages endm
```

4.9 Calculating New Start Address and Loading Single Page Offset

```
; Function:
; Setup Graphics controller Mode Extensions Register for single page (64K)
; addressing with 16K granularity
;
; Calling Protocol:
;           Set_Singlepg_16K

Set_Singlepg_16K proc    near
                         mov        dx,3CEh      ; select GR register I/O port
                         mov        al,0Bh       ; select GRB index
                         out        dx,al        ; write index register
                         inc        dx           ; inc dx to read data port
                         in         al,dx        ; read data
                         or         al,20h       ; set 16K bytes granularity
                         and        al,0FEh      ; set single page (64K
                         out        dx,al        ; write I/O port with new data
                         ret
Set_Singlepg_16K endp

; Function:
; Calculate new Start Address and load single page offset.
; This function accepts a long address.  GR9 is loaded with
; an offset so that the address specified is as close to the
; bottom of the window as possible.  That is, the windows
; extends as far as possible above the input address.
; 16K granularity is forced so that all 4 MBytes can be
; addressed.  Single page mapping is used, so the window is
; 64K bytes.
; The low order 14 bits of the input address are returned in DX:AX.
;
; Input:
; AX = A[15:0] Input low address
; DX = A[31:16] Input high address
;
; Output:
; AX = A[15:0] Input low address
; DX = A[31:16] Input high address
;
; Calling Protocol:
;           Set_Addr_16K
Set_Addr_16KPROC
                        push        ax          ;save input low address
                        push        dx          ;save input high address
                        mov         cl,14       ;divide input address by 16K
back:                   shr         dx,1
                        rcr         ax,1
                        loop        back        ; to the right
                        and         ax,0FFh     ;ax  = address / 16K
                        mov         bx,ax       ;save address in bx
```



```
                        mov         dx,3CEh     ;load  register I/O port
                        mov         al,9        ;register 9 index
                        mov         ah,bl       ;load Gr9 with offset
                        out         dx,ax

                        pop         dx          ;get high address from stack
                        pop         ax          ;get low address from stack
                        and         ax,0ffh
                        and         dx,03fh     ;return the bottom 14 bits
                        ret
Set_Addr_16KENDP
```

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Appendix D2

Linear Addressing

LINEAR ADDRESSING

1. INTRODUCTION

The CL-GD543X/'4X family of VGA controllers can be configured to access display memory as a 1-Mbyte (or 2- or 4-Mbytes) linearly addressed string of bytes, rather than using the standard 64K or 128K window based at A000:0.

Byte '0' in display memory will be accessed at the first byte of the linear address space (typically 64 or 2048 Mbytes). Beginning with that address, display memory may be considered an ordered string of bytes. Refer to Appendix D1 to determine the address offset of any particular pixel. Refer to Appendix B10 for special considerations for the CL-GD5440.

For applications or drivers that support linear addressing, address calculations within display memory are simplified. It is not necessary to calculate offsets into a relatively small window, or to test for a crossing of the window boundary.

Since the mechanization of linear addresses varies dramatically among bus configurations, each configuration is treated separately.

2. LINEAR ADDRESSING IN PCI CONFIGURATION

Hardware Connections: The CL-GD543X/'4X Host Interface pins are connected to similarly-named pins on the PCI bus. The PCI bus provides a complete 32-bit address bus, so no external address decoding is required.

System Considerations: If the high order eight bits of the address on the AD pins matches the PCI Base Address register (see Chapter 4, "External and General Registers"), and SR7[7:4] is a non-zero, the CL-GD543X/'4X will be in linear addressing mode. This provides a 16-Mbyte address space.

The bottom of this space is used for Display Memory access and the top 256 bytes can be used for Memory-mapped I/O (for the CL-GD5430/'36/'40 only). The 4-Mbyte region beginning at 8 Mbyte is also used on the CL-GD5440 as the video address space.

For the Windows drivers, the base address of the linear space is retrieved from the Base Address register using a PCI System BIOS INT 1A call. The setting in the SYSTEM.INI is not used.

For the CL-GD5436, the 16-Mbyte space can be set up as four byte-swapping apertures, for Power PC. See the description of CF8 in Appendix B9.

3. LINEAR ADDRESSING IN VESA® CONFIGURATION

Addressing Considerations: The following table shows how CL-GD543X/'4X, when configured for a VESA host, will respond to display memory cycles as a function of the HIMEM and LOMEM inputs.

Table D2-1. CL-GD543X/'4X Memory Addressing: VESA® Configuration

HIMEM	LOMEM	Response	Note
0	0	No response	–
0	1	Standard VGA Map A000:0–BFFF:F	SR7[7:4] = 0
1	0	No response	–
1	1	Linear Display Memory	SR7[7:4] ≠ 0

Finding a location in the address space linear addressing is more difficult for the VESA VL-Bus than for the PCI bus. The reason is that the Cirrus Logic adapter does not decode the entire address bus, nor do most motherboard board core logic chip sets. This can lead to either the CL adapter or the core logic decoding addresses that belong to the other.

Placing the linear address space at 64 Mbytes will work with most motherboards. However, there are two that have a problem. The following table shows the locations that can be used with these boards.

Table D2-2. VESA® VL-Bus™ Motherboards Which Cannot Use 64 Mbyte

Motherboard	Chip Set	Usable Location
EFAR	EC798	32 or 2048 Mbyte
VMC	UM82C491	32 Mbyte

To guarantee compatibility with all motherboards, Cirrus Logic recommends that provisions be made on adapter cards to decode 32 Mbyte, 64 Mbyte, or 2048 Mbyte for the linear address space. One of these locations will be compatible with all known motherboards. The following schematic fragment shows how this might be mechanized with a single piece of F260 and three jumpers.

Alternately, the CL-GD5403 will generate HIMEM and LOMEM at a programmable address.

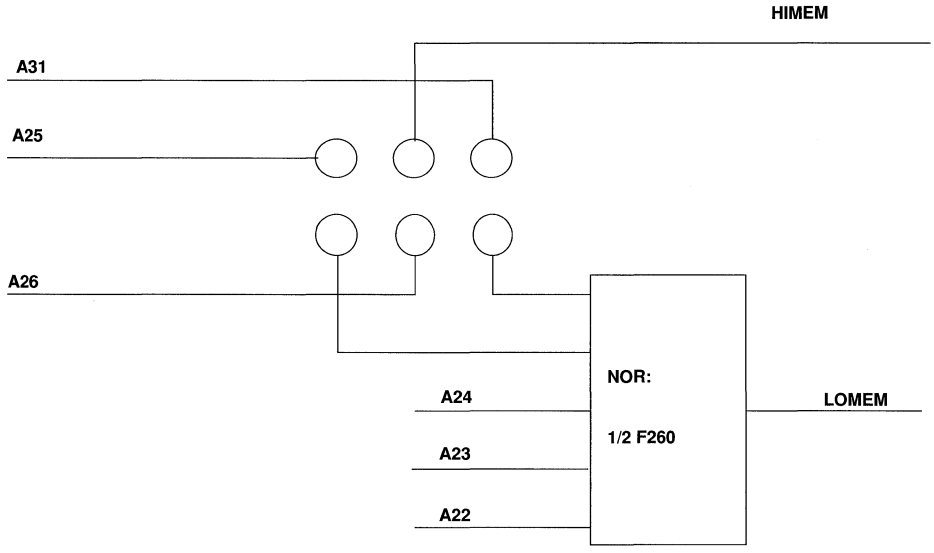
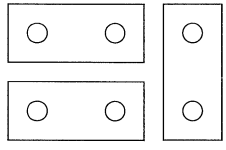
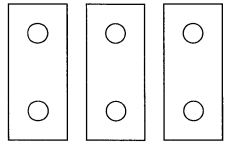
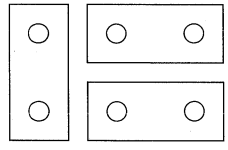


Figure D2-1. Example Schematic Segment

Linear Space	Jumpers	HIMEM	LOMEM
32 Mbyte		A25	A31, A26, A24, A23, A22
64 Mbyte		A26	A31, A25, A24, A23, A22
2048 Mbyte		A31	A26, A25, A24, A23, A22

Software Considerations: For VESA configurations, linear addressing is selected whenever SR7[7:4] is programmed to any value other than '0' (the particular value is unimportant), and HIMEM and LOMEM are both high.

For the Windows drivers, the Base Address is typically put at 64 Mbytes, although this can be changed in the SYSTEM.INI File. Refer to the Windows drivers Install procedure. It will also be necessary to edit the corresponding entry in WINMODE.INI.

4. LINEAR ADDRESSING IN ISA CONFIGURATION (CL-GD5434 only)

Hardware Connections: The CL-GD5434 Address Input pins are connected to similarly-named pins on the ISA bus. There are no HIMEM or LOMEM pins when the CL-GD5434 is configured for ISA bus. MEMR* and MEMW* on the 'B' connector must be used rather than SMEMR* and SMEMW* on the 'A' connector. This is because SMEMR* and SMEMW* are active only for the first 1 Mbyte, while MEMR* and MEMW* are active for the first 16 Mbytes.

Software Considerations: For ISA configurations, linear addressing is selected whenever SR7[7:4] is programmed to any value other than '0'. It will respond to any memory access for which Address Inputs LA[23:20] match the value programmed into SR7[7:4].

If GRB[5] is programmed to '1', the CL-GD5434 will respond to any memory access for which Address Inputs LA[23:21] match SR7[7:5]. SR7[4] must be programmed to '0' in this case. This provides linear addressing for up to 2 Mbytes.

For the linear address space to be accessible in an ISA configuration, the system memory must be limited to 14 Mbytes or less.

For the Windows drivers, the Base Address must be specified in SYSTEM.INI and WINMODE.INI. This will depend on the system configuration; typically 10 Mbytes is used.

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Appendix D3

Hardware Cursor

HARDWARE CURSOR

1. INTRODUCTION

The CL-GD543X/'4X is capable of supporting a 32 × 32 or 64 × 64 hardware cursor (mouse pointer) in 16-color planar, 256-color, 32K, 64K, and 16M Packed-pixel Graphics modes. The hardware cursor cannot be used with 1280 × 1024 resolutions above 87i refresh.

The hardware cursor replaces the software mouse pointer commonly used by GUI (graphical user interface) applications. The hardware cursor eliminates the need for application software to save and restore the screen data as the mouse cursor position changes.

The application software typically initializes the hardware cursor once, and from that point only needs to update cursor (x,y) position to move the cursor on the screen. The hardware cursor offers a smoothly moving mouse pointer, with improved performance as compared to a software cursor.

Multiple hardware cursor patterns can be loaded into the upper display memory area for Stand-alone Alpine modes, allowing application programs to quickly select one of the patterns as the active cursor pattern. The cursor patterns are loaded into the display memory for Extended Mondello modes. The location depends on the memory configuration.

2. CURSOR PROGRAMMING OVERVIEW

The hardware cursor is a pixel array of two planes: Cursor Plane 0 and Cursor Plane 1. The following table shows how the corresponding bits of the two planes determine the displayed state of each cursor pixel. The P-bus output will reflect the cursor state as indicated for 8 BPP modes and for byte serial 16 BPP modes.

Table D3-1. Hardware Cursor Planes

Cursor Plane 1	Cursor Plane 0	Hardware Cursor Pixel Display State	Pixel Bus
0	0	Transparent	Display data
0	1	Inverted VGA display data	Inverted display data
1	0	Cursor Color 0	00h
1	1	Cursor Color 1	FFh

Cursor Color 0 and Cursor Color 1 are supplied by the internal palette DAC extra LUT (look-up table) locations at Index 00H and 0FH. This allows for hardware cursor colors to be independent of the palette DAC table index 00H through FFH. These locations may be accessed by programming SR12[1] to '1'.

The CL-GD543X/'4X Extension SR12: Graphics Cursor Attributes register can be programmed to:

- Select the cursor size
- Enable access to the palette DAC cursor colors
- Enable/disable the cursor

The hardware cursor data is located in the upper 16K of display memory (upper 4K of each logical memory plane). Based on the cursor size selected, 32 × 32 or 64 × 64, the number of cursor patterns that can be loaded in display memory at one time is either 64 or 16. The Graphics Cursor Pattern Address Offset register allows the application to select one of the cursor patterns loaded in display memory to be selected as the active graphics cursor.

The Hardware Cursor position on the screen is controlled by programming the Graphics Cursor X position and Graphics Cursor Y position. The 11-bit Cursor X location and Cursor Y location values are programmed by executing a 16-bit I/O write, where bits 7:5 of the Index register are the least-significant bits of the 11-bit value. The diagram in Figure D3-1 shows the bits.

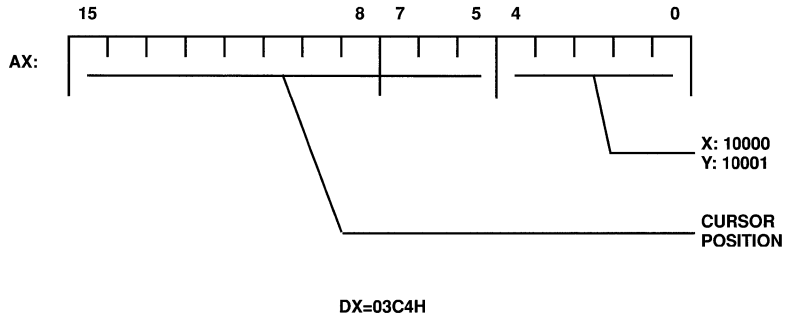

Figure D1-1. Cursor Position Programming

Table D3-2 shows the Extension Register bits for programming the hardware cursor.

Table D3-2. CL-GD543X/'4X Extension Register Bits

Function Description	Extension Register	I/O Port Address	Register Bits	Value
Graphics cursor enable	SR12	3C5	0	1
Access Graphics palette DAC colors	SR12	3C5	1	1
32 × 32 Graphics cursor size	SR12	3C5	2	0
64 × 64 Graphics cursor size	SR12	3C5	2	1
Graphics cursor pattern offset	SR13	3C5	5:0	63..0
Graphics cursor X position	SR10, 30, 50, 70, 90, B0, D0, F0	3C4/3C5	7:5/7:0	2047..0
Graphics cursor Y position	SR11, 31, 51, 71, 91, B1, D1, F1	3C4 /3C5	7:5/7:0	2047..0

3. 32 × 32 HARDWARE CURSOR

For a 32 × 32 cursor size, each cursor pattern requires 256 bytes (128 bytes-per-plane × 2 cursor planes). This allows for 64 cursor patterns to be loaded into hardware cursor data area at the top of display memory. The active graphics cursor pattern is selected by programming the Graphics Cursor Pattern Address register (SR13), bits 5:0.

The hardware cursor pattern data from Cursor Plane 0 and Cursor Plane 1 is loaded into display memory in the following order: the 256 bytes are stored across the four logical Display Memory Planes — 64 bytes per plane, the first 32 bytes of each memory plane are from Cursor Plane 0, and the last 32 bytes are from Cursor Plane 1.

4. 64 × 64 HARDWARE CURSOR

The 64 × 64 cursor size is not available with 16-bit-wide display memory.

For a 64 × 64 cursor size, each cursor pattern requires 1024 bytes (512 bytes per plane × 2 cursor planes). This allows for 16 cursor patterns to be loaded into hardware cursor data area at the top of display memory. The active graphics cursor pattern is selected by programming the Graphics Cursor Pattern Address register (SR13), bits 5:2.

The 64 × 64 Hardware Cursor pattern data from Cursor Plane 0 and Cursor Plane 1 is loaded into display memory one cursor scanline at a time; 8 bytes written across the four logical display planes (2-bytes-per-plane). One cursor scanline is loaded from Cursor Plane 0 followed by one cursor scanline from Cursor Plane 1. This is done until all 64 scanlines from the Cursor Plane 0 and Cursor Plane 1 are loaded into display memory.

5. PROGRAMMING EXAMPLES

The following functions address the hardware cursor. These functions have been tested and debugged, and are declared to be in the public domain.

- Hcursor32_enable — Set cursor size to 32 × 32 and enable
- Hcursor32_disable — Disable cursor
- Hcursor64_enable — Set cursor size to 64 × 64 and enable
- Hcursor64_disable — Set cursor size to 64 × 64 and disable
- Hcursor_set_pattern_32 — Select 32 × 32 cursor pattern
- Hcursor_set_pattern_64 — Select 64 × 64 cursor pattern
- SetXY_Cursor — Set X and Y position of cursor
- HC_load_pattern_32 — Load a pattern for a 32 × 32 hardware cursor
- HC_load_pattern_64 — Load a pattern for a 64 × 64 hardware cursor
- Set_Plane — Select one of four planes of display memory (macro)
- Set_Addr_Offset_Bymem — Set a value for the Address Offset register based on memory size
- Hcursor_color — Set foreground or background color for cursor

```
;Function:
; This function will enable 32x32 hardware cursor
;Calling Protocol:
;           Hcursor32_enable

Hcursor32_enable        proc
            mov         dx,3c4h     ;load sequencer register I/O port
            mov         al,12h      ;select SR12 register index
            out         dx,al       ;write index register
            inc         dx          ;increment dx to read data port
            in          al,dx       ;read data
            or          al,1        ;data = enable graphic cursor
            out         dx,al       ;write I/O port with new data
            ret
Hcursor32_enable        endp

;Function:
; This function will disable 32x32 hardware cursor
;Calling Protocol:
;           Hcursor32_disable

Hcursor32_disable       proc
            mov         dx,3c4h     ;load sequencer register I/O port
            mov         al,12h      ;select SR12 register index
            out         dx,al       ;write index register
            inc         dx          ;increment dx to read data port
            in          al,dx       ;read data
```

```
            and         al,0feh     ;data = disable graphic cursor
            out         dx,al       ;write I/O port with new data
            ret
Hcursor32_disable       endp

;Function:
; This function will enable 64x64 hardware cursor
;Calling Protocol:
;           Hcursor64_enable

Hcursor64_enable        proc
            mov         dx,3c4h     ;load sequencer register I/O port
            mov         al,12h      ;select SR12 register index
            out         dx,al       ;write index register
            inc         dx          ;increment dx to read data port
            in          al,dx       ;read data
            or          al,5        ;data = enable 64x64 graphic cursor
            out         dx,al       ;write I/O port with new data
            ret
Hcursor64_enable        endp

;Function:
; This function will disable 64x64 hardware cursor
;Calling Protocol:
;           Hcursor64_disable

Hcursor64_disable       proc
            mov         dx,3c4h     ;load sequencer register I/O port
            mov         al,12h      ;select SR12 register index
            out         dx,al       ;write index register
            inc         dx          ;increment dx to read data port
            in          al,dx       ;read data
            or          al,4        ;select 64x64 cursor size
            and         al,0feh     ;data = disable graphic cursor
            out         dx,al       ;write I/O port with new data
            ret
Hcursor64_disable       endp

;Function:
; This function select one of the 64-cursor patterns for 32x32 cursor
; stored at the top (highest addressed 16K bytes) of Display Memory.
;
;Input:
; bl = 0..63 cursor patterns number
;
;Calling Protocol:
;           Hcursor_Set_Pattern_32

Hcursor_set_pattern_32  proc
            mov         dx,3c4h     ;load sequencer register I/O port
            mov         al,13h      ;select SR13 register index
```



```
            out         dx,al       ;write index register
            inc         dx          ;increment index to write data port
            mov         al,bl       ;get pattern number
            out         dx,al       ;write I/O port with new data
            ret
Hcursor_set_pattern_32  endp

;Function:
; This function select one of the 16-cursor patterns for 64x64 cursor
; stored at the top (highest addressed 16K bytes) of Display Memory.
;
;Input:
; bl = 0..15 cursor pattern number
;
;Calling Protocol:
;           Hcursor_Set_Pattern_64

Hcursor_set_pattern_64  proc
            mov         dx,3c4h     ;load sequencer register I/O port
            mov         al,13h      ;select SR13 register index
            out         dx,al       ;write index register
            inc         dx          ;increment index to write data port
            mov         al,bl       ;get pattern number
            shl         al,1        ;bit 0 and 1 of SR13 is ignored in
            shl         al,1        ;  64x64 cursor
            out         dx,al       ;write I/O port with new data
            ret
Hcursor_set_pattern_64  endp

;Function:
; This function set the XY Position of the Hardware Cursor.
; For X position register, the data forms the upper-eight bits of the 11-bit
; position.  The offset must be placed in AX[15:5], AX[4:0] must be 10000,
; and DX must be 03C4.
; For Y position register, the data forms the upper-eight bits of the 11-bit
; position.  The offsetmust be placed in AX[15:5], AX[4:0] must be 10001,
; and DX must be 03C4.
;
; Input:
; bx = X position of cursor
; cx = Y position of cursor
;
;Calling Protocol:
;           SETXY

SetXY_Cursor            proc
            PUSH    BP
            MOV     BP,SP
            PUSH    ES
            PUSH    DS
            PUSH    DI
```

```
            PUSH    SI

            mov     dx,3c4h ; X value for Hardware Cursor
            shl     bx,1
            shl     bx,1
            shl     bx,1
            shl     bx,1
            shl     bx,1
            add     bx,10h  ; for index
            mov     ax,bx
            out     dx,ax

            mov     bx,cx   ; Y value for Hardware Cursor
            shl     bx,1
            shl     bx,1
            shl     bx,1
            shl     bx,1
            shl     bx,1
            add     bx,11h  ; for index
            mov     ax,bx
            out     dx,ax

            ;--- Clean up and exit
            POP     SI
            POP     DI
            POP     DS
            POP     ES
            MOV     SP,BP
            POP     BP
            RET
SetXY_Cursor endp

;Function:
; This function select one of the four planes of Display Memory.
;
;Input:
; plane_no: 1,2,4,8  plane 0,1,2,3 of Display Memory
;
;Calling Protocol:
;           Set_Plane

Set_Plane   macro plane_no
            mov         dx,3c4h
            mov         al,2
            out         dx,al       ;select plane mask register
            inc         dx
            mov         al,plane_no
            out         dx,al       ;write to selected plane
ENDM
```



```
;Function:
; This function will load the Hardware Cursor patterns for 32x32
; cursor into memory.
; The 256 bytes cursor pattern are stored across the four logical
; Display Memory Planes - 64 bytes per plane, the first 32 bytes
; of each memory plane are from Cursor Plane 0, and the last 32
; bytes are from Cursor Plane 1.
;
;Protocol:
;           HC_load_patterns_32

HC_load_patterns_32     proc
            push        ds
            push        si
            push        es
            push        di
            push        cx

            call        Set_Addr_Offset_Bymem
            lea         si, CURSOR32            ;SI = offset to the cursor
pattern
            mov         ax,0a000h
            mov         es,ax
            mov         di,0f000h

            mov         cx,64       ;32 scan lines x 2 for 2 planes
write_cur_32:
            Set_Plane 1             ;select memory plane 0 to write pattern
            mov         al,byte ptr cs:[si];read 8 bits of 32 bits cursor pattern
            mov         es:[di],al  ;write 8 bits of cursor pattern
            inc         si          ;move to next 8 bits of 32 bits pattern
            Set_Plane 2             ;select memory plane 1 to write  pattern
            mov         al,byte ptr cs:[si];read 8 bits of 32 bits  pattern
            mov         es:[di],al  ;write 8 bits of cursor pattern
            inc         si          ;move to next 8 bits of 32 bits pattern
            Set_Plane 4                         ;select memory plane 2 to write
cursor pattern
            mov         al,byte ptr cs:[si];read 8 bits of 32 bits  pattern
            mov         es:[di],al  ;write 8 bits of cursor pattern
            inc         si          ;move to next 8 bits of 32 bits pattern
            Set_Plane 8             ;select memory plane 3 to write cursor
pattern
            mov         al,byte ptr cs:[si];read 8 bits of 32 bits  pattern
            mov         es:[di],al  ;write 8 bits of cursor pattern
            inc         si          ;move to next 8 bits of 32 bits pattern
            inc         di          ;move to next address of display memory
            loop        write_cur_32

            pop         cx
            pop         di
            pop         es
```

```
            pop         si
            pop         ds
            ret
HC_load_patterns_32     endp

;Function:
; This function will load the Hardware Cursor patterns for 64x64
; cursor into memory.
; The hardware cursor pattern is loaded into Display Memory one cursor
; scanline at a time.  One cursor scanline is loaded from Cursor Plane
; 0 followed by one cursor scanline from Cursor Plane 1.
;
;Protocol:
;           HC_load_patterns_64

HC_load_patterns_64     proc
            push        ds
            push        si
            push        es
            push        di
            push        cx

            call        Set_Addr_Offset_Bymem

            lea         si,CURSOR64             ;SI = offset to cursor pattern
            mov         ax,0a000h
            mov         es,ax
            mov         di,0f000h

            mov         cx,64       ;64 scan lines per plane
write_cur_64:
            Set_Plane 1             ;select memory plane 0 to write cursor
pattern
            mov         ax,word ptr cs:[si];read 16 bits of 64 bits  pattern
                                           ; from cursor plane 0
            mov         es:[di],ax          ;write 16 bits of  pattern
            mov         ax,word ptr cs:[si+256];read 16 bits from  plane 1
            mov         es:[di+2],ax        ;write 16 bits of  pattern
            inc         si          ;move to next 16 bits of 64 bits pattern
            inc         si
            Set_Plane 2             ;select memory plane 1 to write  pattern
            mov         ax,word ptr cs:[si];read 16 bits of 64 bits  pattern
                                           ; from cursor plane 0
            mov         es:[di],ax          ;write 16 bits of  pattern
            mov         ax,word ptr cs:[si+256];read 16 bits from  plane 1
            mov         es:[di+2],ax        ;write 16 bits of  pattern
            inc         si          ;move to next 16 bits of 64 bits pattern
            inc         si
            Set_Plane 4             ;select memory plane 2 to write  pattern
            mov         ax,word ptr cs:[si];read 16 bits of 64 bits  pattern
                                           ; from cursor plane 0
```



```
            mov         es:[di],ax              ;write 16 bits of  pattern
            mov         ax,word ptr cs:[si+256];read 16 bits from  plane 1
            mov         es:[di+2],ax            ;write 16 bits of  pattern
            inc         si          ;move to next 16 bits of 64 bits pattern
            inc         si
            Set_Plane 8             ;select memory plane 3 to write  patter
            mov         ax,word ptr cs:[si];read 16 bits of 64 bits cursor
                                            ; from cursor plane 0
            mov         es:[di],ax              ;write 16 bits of  pattern
            mov         ax,word ptr cs:[si+256];read 16 bits from  plane 1
            mov         es:[di+2],ax            ;write 16 bits of  pattern
            inc         si          ;move to next 16 bits of 64 bits pattern
            inc         si
            inc         di
            inc         di
            inc         di
            inc         di

            loop        write_cur_64

            pop         cx
            pop         di
            pop         es
            pop         si
            pop         ds
            ret
HC_load_patterns_64     endp

;Function
; This function set value for Address Offset register.
;
;Input:
; BX = total display memory                     BX = 04h - 256KB
;                                                  = 08h - 512KB
;                                                  = 10h - 1MB
;                                                  = 20h - 2MB
;                                                  = 30h - 3MB
;                                                  = 40h - 4MB
;
;Calling Protocol:
;           Set_Addr_Offset_Bymem

Set_Addr_Offset_Bymem   proc
            cmp         bx,4                    ;has 256KB of Display memory?
            jne         @F                      ;no, next memory check
            mov         bl,0                    ;yes, set offset register
            Set_Addr_Offset 0;set offset registers
            jmp         exit
@@:         cmp         bx,8                    ;has 512KB of Display memory?
            jne         @F          ;no, have 1,2,3 or 4MB of display memory
            Set_Addr_Offset 10h;yes, set offset register
```

```
            jmp         exit
@@:
            Set_Addr_Offset 0f0h;set offset register
exit:
            ret
Set_Addr_Offset_Bymem   endp

;Function
; This function set the address offset registers for the next DRAM
; windows.
;
;Input:
; value = number to set offset register
;Calling Protocol:
;           Set_Addr_Offset

Set_Addr_Offsetmacro value
            mov         dx,3c4h
            mov         al,6
            out         dx,al
            inc         dx
            mov         al,12h
            out         dx,al                   ;unlock extened register
            mov         dx,3ceh
            mov         al,9                    ;Offset Register 0 - GR9
            out         dx,al
            inc         dx
            mov         al,value
            out         dx,al
ENDM

;Function
; This function set foreground or background color of hardware
; cursor.
;
;Input:
; bh = color value
;      0h .. 0Eh = background color to set
;       0Fh 1Fh 2Fh .. 0FFh = foreground color to set
; bl = red value
; ch = green value
; cl = blue value
; dh = cursor size
;      0 = 32x32 cursor size
;      1 = 64x64 cursor size
;Calling Protocol:
;           Hcursor_color

proc        Hcursor_color
            mov         dx,3c4h
            mov         al,12h
```



```
            out         dx,al       ;change DAC locations 0&1 to HC colors 0 & 1
            inc         dx
            cmp         dh,1        ;check cursor size type
            je          @F
            mov         al,3        ;bit 1,0: allow access to DAC Ext color
                                    ; and enable HC
            jmp         cont_hcursor
@@:         mov         al,7        ;bit 2,1,0: allow access to DAC Ext
                                    ; color and enable HC 64x64
cont_hcursor:
            out         dx,al
            mov         al,bh       ;get color to set
            mov         dx,3c8h
            out         dx,al       ;specify color entry in LUT of DAC
            mov         dx,3c9h
            mov         al,bl
            out         dx,al       ;write RED value
            mov         al,ch
            out         dx,al       ;write GREEN value
            mov         al,cl
            out         dx,al       ;write BLUE value
            mov         dx,3c4h
            mov         al,12h
            out         dx,al       ;point back to DAC locations
            inc         dx
            mov         al,1        ;enable HC
            out         dx,al
            ret
Hcursor_color endp
```

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Appendix D4

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Appendix D5

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Appendix D6

Color Expansion and Extended Write Modes

COLOR EXPANSION AND EXTENDED WRITE MODES

1. INTRODUCTION

The CL-GD543X/'4X family supports color expansion for faster CPU write performance. This is implemented via two Extended Write modes and the BitBLT engine. Color expansion enhances data transfer efficiency when the host is sending patterns to the display memory that require one or two colors. Rather than sending the entire color description across the bus for each pixel, the colors descriptions are written into registers within the VGA controller. Then each pixel can be defined with a single bit that specifies either one or the other pre-programmed color.

These Extended Write modes operate on eight pixels at a time, in 8- or 16-bits-per-pixel Graphics modes with packed-pixel addressing. Extended Write modes can be used for faster text writes, pattern fill, and block-move operations in Graphics modes. In addition, the BitBLT engine supports color expansion for 8-, 16-, 24-, and 32-bit-per-pixel modes (only the CL-GD5436 supports BitBLT color expansion for 24-bpp modes and only the CL-GD5434/'36 support 32-bit-per-pixel modes).

The following sections cover Extended Write modes from a programming point of view. The basic operation of color expansion is explained and the registers involved described. Finally, the capabilities of the BitBLT engine are also covered.

2. COLOR EXPANSION WITHOUT THE BITBLT ENGINE

The controls that enable the Extended Write modes are in register GRB[4:1], as indicated in Figure D6-1. These bits are described in detail in Chapter 9, "Extension Registers". Briefly, bits 3:1 are programmed to '1's for 8-bit-per-pixel modes, and bits 4:2 are programmed to '1's for 16-bit-per-pixel modes.

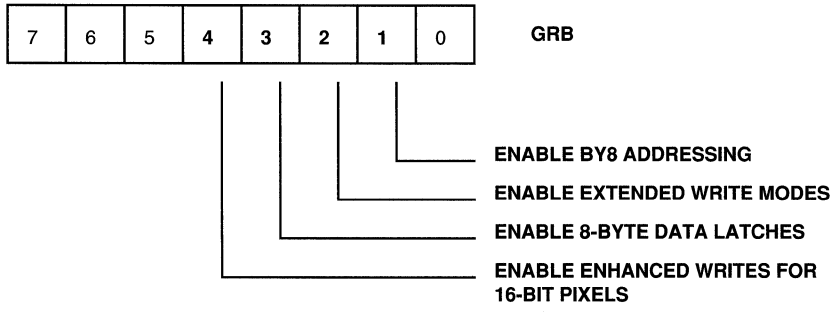

Figure D6-1. Color Expansion Controls

Enable BY8 Addressing shifts the address bits between the host and display memory three bits. This means that each **bit** within the host address space will correspond to a pixel in display memory. The pattern to be expanded is an ordered string of bits, each bit corresponding to a pixel. It can be transferred across the bus with a move string instruction and each bit will be expanded into a complete 8- or 16-bit pixel.

Enable Extended Write Modes can be considered a master enable; it must be programmed to a '1' to turn any of this procedure on.

Enable 8-byte Data Latches allows the use of eight, rather than the standard four data latches at the display memory interface.

Enable Enhanced Write for 16-bit Pixels must be programmed to '1' to use color expansion in 16-bit-per-pixel Video modes. When this bit is programmed to '1', each bit across the host bus still corresponds to a pixel, now a 16-bit pixel. This bit must not be programmed to '1' simultaneously with bit 1. Observe that 32-bit-per-pixel color expansion is supported with the CL-GD5434/'36 BitBLT Engine, *not* with Extended Write modes.

2.1 Extended Write Mode 4

Extended Write mode 4 is enabled when the GR5[2:0] field is programmed to '100', and the Extended Write modes are enabled as described above. In Extended Write mode 4, the foreground color will be written into each pixel for which the corresponding bit on the host bus is '1'. The foreground color will be contained in GR1 and GR11 (for 8-bit pixels GR11 is ignored).

Pixels corresponding to CPU Bus bits that are '0' will not be written in Extended Write mode 4. Extended Write mode 4 is intended for writing text into display memory for which the background is not to be modified. Extended Write mode 4 supports 8- and 16-bits-per-pixel.

2.2 Extended Write Mode 5

Extended Write mode 5 is enabled when the GR5[2:0] field is programmed to '101', and the Extended Write modes are enabled as described above. In Extended Write mode 5, the foreground color will be written into each pixel for which the corresponding bit on the host bus is '1'. The foreground color is contained in GR1 and GR11 (for 8-bit pixels GR11 is ignored). The background color will be written into each pixel for which the corresponding bit on the host bus is '0'. The background color is contained in GR0 and GR10 (for 8-bit pixels GR10 is ignored).

Extended Write mode 5 supports 8- and 16-bits-per-pixel, but does not support 32-bits-per-pixel.

2.3 Special Note for Application Programmers

Extended write modes 4 and 5 are made largely obsolete by the color expansion capabilities of the BitBLT engine. Cirrus Logic does not guarantee the availability of extended write modes 4 and 5. Application programs should be written using the BitBLT engine, rather than extended write modes 4 and 5.

3. COLOR EXPANSION USING BITBLT ENGINE

The BitBLT engine is discussed in detail in Appendix D8. This appendix reviews the information regarding color expansion. The data can be expanded into 8-, 16-, 24, or 32-bits-per-pixel. The CL-GD5430/'40 support 8- and 16-bit-per pixel expansion, but not 32-bit-per-pixel. Only the CL-GD5436 supports 24-bit-per-pixel color expansion.

The data to be expanded will always be a single bit for each pixel. The data can represent text or icons. The data would typically, but not necessarily, be transferred across the host interface. That is, it would typically be sent by a system-to-screen BitBLT operation.

The data could also be a pattern that is to be repeatedly expanded and written into display memory. In this case, the source data must be in display memory (pattern copies are supported only for screen-to-screen BitBLTs).

The Foreground Color registers are GR1, GR11, GR13, and GR15; Background Color registers are GR0, GR10, GR12, and GR14. Tables D6-1 and D6-2 indicate how the registers are allocated to the various colors. Please review the material in Appendix D8, section 5 for notes regarding the use of transparency.

Table D6-1. Background Color Registers

Format	GR0	GR10	GR12: CL-GD5434/'36	GR14: CL-GD5434/'36
8 bits/pixel	Single Byte	Don't care	Don't care	Don't care
16 bits/pixel	Low Byte	High Byte	Don't care	Don't care
32 bits/pixel	Blue Byte	Green Byte	Red Byte	Alpha Byte

Table D6-2. Foreground Color Registers

Format	GR1	GR11	GR13: CL-GD5434 Only	GR15:CL-GD5434 Only
8 bits/pixel	Single Byte	Don't care	Don't care	Don't care
16 bits/pixel	Low Byte	High Byte	Don't care	Don't care
24 bits/pixel (CL-GD5436)	Blue Byte	Green Byte	Red Byte	Don't care
32 bits/pixel	Blue Byte	Green Byte	Red Byte	Alpha Byte

Appendix D7

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Appendix D8

BitBLT Engine

Table of Contents

BITBLT ENGINE

1. INTRODUCTION

Written from a software programmer's standpoint, this appendix describes the CL-GD543X/'4X BitBLT engine. To help establish a common nomenclature, relevant terms are defined. Also included is an example of basic operation. Various methods of modifying the source data before writing it into the destination region are covered, these are: ROPs (raster operations), Color Expansion, and Pattern Fill. Practical considerations covered are: BLT direction, using system memory for either the source or destination, and how to start, suspend, and resume a BLT. This document concludes with a complete summary of the BLT registers, a discussion of memory-mapped I/O, and some practical examples.

2. DEFINITIONS

This section includes a definition of terms.

Source Area: The source area of a BitBLT is the area from which the data are copied. The source area may be in display or system memory; it may be a monochrome image which will be expanded into color; it may be a single 8 pixel × 8 pixel image that will be replicated to fill a larger area. The source area is never written except in special cases where it and the destination area overlap in display memory.

Destination Area: The destination area of a BitBLT is the area into which the data are written. The destination area must be in display memory.

Width: The Width of a BitBLT refers to the number of bytes (not necessarily pixels) of destination that are processed before adding the Pitch values to the Address values. If the destination area is actually or potentially on the screen (that is, if it is a rasterized area that will be displayed), the Width is the number of bytes (not necessarily pixels) to be written in each scan line. If the destination area is off-screen and the source is a rasterized area (and there is no pattern copy or color expansion), the Width is the number of bytes per scan line of source. If neither the destination or source is a rasterized area, Width is simply the number of bytes that are processed before the Pitch values are added to the Address values, and has no special meaning. Width is specified in the register pair GR20 and GR21. The number actually written into this register pair is one less than the actual desired width in bytes. This is a 13-bit value for the CL-GD5434/'36, allowing a maximum width of 8192 bytes. This is an 11-bit value for the CL-GD5430/'40, allowing a maximum width of 2048 bytes.

Height: The Height of a BitBLT refers to the number of times the Pitch values are added to the Address values. If the destination area is actually or potentially on the screen (if it is a rasterized area that will be displayed), the Height is the number of scan lines in that area. If not, Height is simply the number of times the Pitch values are added to the Address values and has no special meaning. In this case, Width and Height are simply two numbers that are multiplied together to define the number of bytes in the destination. Height is specified in the register pair GR22 and GR23. The number actually written into the register pair is one less than the actual desired height. This is a 10-bit value, allowing a maximum height of 1024scan lines. On the CL-GD5436, this is an 11-bit value. The contents of the registers containing the Height are not modified during the operation.

Width and Height are shown for a displayable area in Figure D8-1.

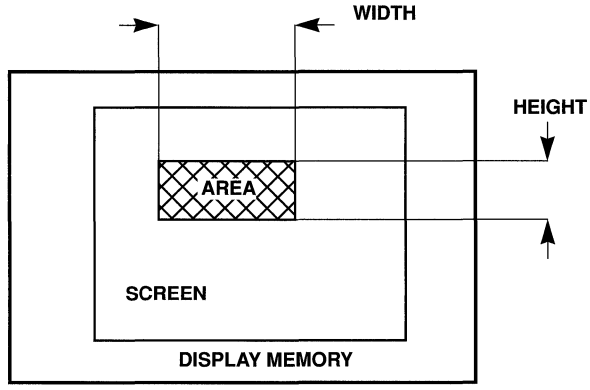

Figure D8-1. Width and Height

Pitch: The destination Pitch and source Pitch are the values that are added to the respective addresses after each *width* bytes of destination have been processed. Destination and source Pitch are specified separately. When an area is a rasterized image, the Pitch will be the number of bytes between vertically adjacent pixels. This is the number of bytes between the (first) pixel of scan line n and the (first) pixel of scan line n+1 (the number that is added to the address to get from one scan line to the next). Sometimes this will the same as the number of bytes in each scan line; sometimes it will be more.

When an area is in off-screen display memory, it will often be stored so that scan lines are adjacent. This minimizes fragmentation. In this case, the respective Pitch would be set equal to the Width (+1). When the source is in system memory, the respective Pitch is unused and is a 'don't care'. When executing BLTs with pattern copy or color expansion, the source area is taken to be linear and the source Pitch is a 'don't care'. The destination Pitch is specified in register pair GR24 and GR25. The source Pitch is specified in register pair GR26 and GR27. These register pairs are both 13-bit values, allowing a Pitch of 8191 bytes. Figure D8-2 shows Pitch for the case of a rasterized image.

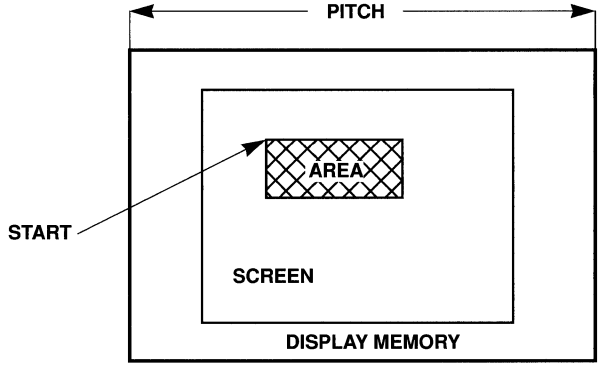

Figure D8-2. Pitch and Start

Start: refers to the address of the first byte of a destination or source area. This is a byte offset from the beginning of display memory. The start address of the destination area is specified in register triplet GR28, GR29, and GD2A. The start address of the source area is specified in register triplet GR2C, GR2D, and GR2E. Each start address is a 22-bit value for the CL-GD5434/'36, allowing up to 4 Mbytes of display memory Each start address is a 21-bit value for the CL-GD5430/'40, allowing up to 2 Mbytes of display memory. The start address is shown in Figure D8-2.

3. AN EXAMPLE: DISPLAY MEMORY TO DISPLAY MEMORY

Table D8-1 shows how the BLT registers would have to be programmed for a very simple BLT operation. This will copy a 128-byte × 64-scan line area in display memory. The CL-GD543X/'4X is assumed to be programmed in Video mode 65 (800 × 600, 16-bits per pixel). Therefore, each 128-byte scan line actually represents 64 pixels. The source begins at location 0, and the destination begins at location 160200 (100 scan lines from the top of the screen, 100 pixels from the left edge).

Table D8-1. Source Copy BLT

Register(s)	Contents (Decimal)	Field	How Calculated
GRB[4,3,1]	0		See Notes in section 10
GR0/GR10/GR12/GR14	Don't care	Background color	Only for Color Expansion
GR1/GR11/GR13/GR15	Don't care	Foreground color	Only for Color Expansion
GR20/GR21	127	Width	(64 × 2) –1
GR22/GR23	63	Height	64 – 1

Table D8-1. Source Copy BLT *(cont.)*

Register(s)	Contents (Decimal)	Field	How Calculated
GR24/GR25	1600	Destination Pitch	800 × 2
GR26/GR27	1600	Source Pitch	800 × 2
GR28/GR29/GR2A	160200	Destination Start	(100 × 1600) + (100 × 2)
GR2C/GR2D/GR2E	0	Source Start	Beginning of display memory
GR2F	Don't care	Write Mask	Only for Color Expansion
GR30	0	Mode	Plain BLT
GR32	0Dh	Raster Op	SRCCOPY
GR33	0	Mode Extension	Unused
GR31	2	Start	Set bit 1

This BLT will be executed as indicated in the following fragment of pseudo-code:

```
sourceAdrs = sourceStartAdrs;
destAdrs = destStartAdrs;
for (i = 0; i < Height; i++)              /*for each scan line*/
    {
    workingSourceAdrs = sourceAdrs
    workingDestAdrs = destAdrs
    for (j =0; j < Width; j++)            /*for each byte*/
         {
         Process one byte of Destination;
         workingDestAdrs++;               /*to next byte*/
         workingSourceAdrs++;
         }
    sourceAdrs = sourceAdrs + sourcePitch; /*next scan line*/
    destAdrs = destAdrs + destPitch;
    }
```

The BLT engine processes *width* bytes of destination, incrementing temporary source and destination addresses after each byte (actually, multiple bytes are processed in parallel). At the end of each *width* bytes, the respective Pitch values are added to the addresses as they were at the beginning of the scan line, moving on to the next scan line. This continues for *height* iterations.

All BLTs are processed in this general manner. There are some variations. For color expansion, the SourceAdrs will be incremented as a bit address rather than a byte address. For pattern copies, the SourceAdrs is incremented modulo some number so that the same 64 pixels are used over and over. If the decrement bit is set, the addresses will be decremented rather than incremented.

4. RASTER OPS

In addition to merely moving bytes from the source area to the destination area, the CL-GD543X/'4X BLT engine can combine the source or pattern bytes with the destination bytes using logical operations. The logical operation is specified by programming GR32. The ROPs are listed in Table D8-2. Observe that the value actually programmed into GR32 is independent of whether a source or pattern is be used; this distinction is made with GR30[6].

Table D8-2. Raster Operations

Source Operation	Microsoft® Name/ Raster Operation	Pattern Operation	Microsoft® Name/ Raster Operation	GR32 (Hex.)
0	BLACKNESS 00000042	0	BLACKNESS 00000042	00
DSon	NOTSRCERASE 001100A6	DPon	– 000500A9	90
DSna	– 00220326	DPna	– 000A0329	50
Sn	NOTSRCCOPY 00330008	Pn	– 000F0001	D0
SDna	SRCERASE 00440328	PDna	– 00500325	09
Dn	DSTINVERT 00550009	Dn	DSTINVERT 00550009	0B
DSx	SRCINVERT 00660046	DPx	PATINVERT 005A0049	59
DSan	– 007700E6	DPan	– 005F00E9	DA
DSa	SRCAND 008800C6	DPa	– 00A000C9	05
DSxn	– 00990066	PDxn	– 00A50065	95
D	– 00AA0029	D	– 00AA0029	06
DSno	MERGEPAINT 00BB0226	DPno	– 00AF0229	D6
S	SRCCOPY 00CC0020	P	PATCOPY 00F00021	0D
SDno	– 00DD0228	PDno	– 00F50225	AD
DSo	SRCPAINT 00EE0086	DPo	– 00FA0089	6D
1	WHITENESS 00FF0062	1	WHITENESS 00FF0062	0E

Table D8-2 emphasizes the compliance of the CL-GD543X/'4X with Microsoft definitions. For those interested in the underlying Boolean logic, Table D8-3 may be helpful.

There are exactly 16 ways in which two bits can be logically combined, these are enumerated in Table D8-3. The first four columns show the logical result for each of the four possible input combinations for each of the 16 cases. For example, in the first row the result is '0' regardless of the inputs. This is called *ZERO* or *BLACKNESS*. For the second row, the result is a '1' when both inputs are zero. This is the logical AND of the inverted inputs.

Table D8-3. 16 Logical Operations

S=1, D=1	S=1, D=0	S=0, D=1	S=0, D=0	Description	GR32 (Hex.)
0	0	0	0	ZERO	00
0	0	0	1	NOT Source AND NOT Destination	90
0	0	1	0	NOT Source AND Destination	50
0	0	1	1	NOT SOURCE	D0
0	1	0	0	Source AND NOT Destination	09
0	1	0	1	NOT Destination	0B
0	1	1	0	Source NEQ Destination (xor)	59
0	1	1	1	NOT Source OR NOT Destination	DA
1	0	0	0	Source AND Destination	05
1	0	0	1	Source EQ Destination (xnor)	95
1	0	1	0	Destination	06
1	0	1	1	NOT Source OR Destination	D6
1	1	0	0	Source	0D
1	1	0	1	Source OR NOT Destination	AD
1	1	1	0	Source OR Destination	6D
1	1	1	1	ONE	0E

5. COLOR EXPANSION

If GR30[7] is programmed to a '1', the source input to the ROP will not be actual data from the source or pattern, but will be *color expanded* data. The source area is a monochrome image. Since the source image is a single bit for each pixel, there are substantial performance benefits, especially if the source is expanded to 16 or more bits per pixel. Color expansion can be used anytime a single foreground color, or a single foreground color and a single background color are to appear in the destination. The following table indicates the color expansion capability of each member of the Alpine family.

Table D8-4. Color Expansion: Bits per pixel

Controller	8 bpp	16 bpp	24 bpp	32 bpp
CL-GD5430	✔	✔		
CL-GD5434	✔	✔		✔
CL-GD5436	✔	✔	✔	✔
CL-GD5440	✔	✔		

The source can be either an 8 × 8 pattern (display memory only), or monochrome data from either display memory or system memory. When the source is in display memory, it must be on a four-byte boundary; when the source is an 8 × 8 pattern, it must be on an eight-byte boundary. In the case of the CL-GD5430/'40, system-to-screen BitBLT with color expansion requires that GR2C be written during the setup even though the register is not used.

Ones in the source area will result in the foreground color being written into the corresponding byte(s) of the destination area. Zeroes in the source area will result in either the background color being written into the corresponding byte(s) of the destination area, or no alteration to the destination area (transparency).

The destination must be Screen Memory and the direction must be 'increment'. Any ROP that uses a source may be used, although SRCCOPY is most common when using color expansion.

For 24-bpp color expansion, transparency *must* be enabled.

For the CL-GD5436, the sense of the monochrome source data can be inverted by programming CR33[1] to '1'. This allows complete foreground/background 24-bpp color expansion in two passes.

The most significant bit of the first source byte will be expanded into the ROP source data for the first pixel of the destination (however, if clipping is enabled, it may not be actually written). Depending on the contents of GR30[5:4], it will be expanded to 1, 2, 3, or 4 bytes (1 or 2 bytes for the CL-GD5430/'40). Tables D8-4 and D8-5 indicate the registers that contain the expansion colors.

Table D8-5. Foreground Expansion ('1' in source)

GR30[5:4]	Width	GR1	GR11	GR13	GR15	Note
00	8-bit	Color	Don't care	Don't care	Don't care	
01	16-bit	Low Byte	High Byte	Don't care	Don't care	
10	24-bit	Blue	Green	Red	Don't care	CL-GD5436
11	32-bit	Blue	Green	Red	Alpha	CL-GD5434/'36

Table D8-6. Background Expansion ('0' in source)

GR30[5:4]	Width	GR0	GR10	GR12	GR14	Note
00	8-bit	Color	Don't care	Don't care	Don't care	
01	16-bit	Low Byte	High Byte	Don't care	Don't care	
10	24-bit	–	–	–	–	Transparency *must* be enabled.
11	32-bit	Blue	Green	Red	Alpha	CL-GD5434/'36

The next bit of source data is processed for the next 1, 2, 3, or 4 bytes of destination, and so on, until *width* bytes of destination have been processed. Unused source bits will be discarded to the end of the current byte. The destination address is modified by the destination Pitch. The source Pitch is ignored since the source is taken to be a linear string of bytes. The next byte of source will be the first eight pixels for the next scan line.

For the CL-GD5436 only, GR33[0] controls the source data granularity for color-expanded system-to-screen BLTs. If GR33[0] is set to '1', unused source data will be discarded to the end of the current DWORD. If GR33[0] is set to '0', unused source data will be discarded to the end of the current byte.

6. COLOR EXPANSION WITH TRANSPARENCY

If GR30[3] is programmed to a '1', the pixels corresponding to '0's in the source area are not written. This is used for a Transparent Write. If GR30[3] is programmed to a '0', the pixels corresponding to '0's in the source area are written with the contents of the background color register(s).

For the CL-GD5430/'36/'40, the Background Color registers are ignored when transparency is enabled. The Foreground Color registers are used as indicated in Table D8-5.

Table D8-7. Color Expansion with Transparency (CL-GD5430/'36/'40)

GR30[5:4]	Width	GR1	GR11	GR13	GR15	Note
00	8-bit	Color	Don't care	Don't care	Don't care	
01	16-bit	Low Byte	High Byte	Don't care	Don't care	
10	24-bit	Blue	Green	Red	Don't care	CL-GD5436
11	32-bit	Blue	Green	Red	Alpha	CL-GD5436

For the CL-GD5434, the Foreground and Background Color registers are used as indicated in the following two tables, when using color expansion with transparency. All four Foreground Color registers must be written; Background Color registers must be written with the inverse value of the corresponding Foreground Color register.

Table D8-8. Color Expansion with Transparency (CL-GD5434)

GR30[5:4	Width	GR1	GR11	GR13	GR15
00	8-bit	Color	Color	Color	Color
01	16-bit	Low byte	High byte	Low byte	High byte
10	(Illegal)	–	–	–	–
11	32-bit	Blue	Green	Red	Alpha

Table D8-9. Color Expansion with Transparency (CL-GD5434)

GR30[5:4]	Width	GR0	GR10	GR12	GR14
00	8-bit	NOT Color	NOT Color	NOT Color	NOT Color
01	16-bit	NOT Low byte	NOT High byte	NOT Low byte	NOT High byte
10	(Illegal)	–	–	–	–
11	32-bit	NOT Blue	NOT Green	NOT Red	NOT Alpha

7. CLIPPING (CL-GD5430/'36/'40 Only)

For the CL-GD5430/'36/'40 only, if GR2F[2:0] are programmed to any value other than zero, the first *n* pixels of each scan line of the destination will not be written. This is typically used in conjunction with pattern fills with or without color expansion. The destination address must point to the first pixel that is skipped and the width must be programmed to include the pixels that are skipped.

Clipping avoids re-aligning the source when it is necessary to begin at other than the first pixel of the color expanded source.

For the CL-GD5436 only, the control field is GR2F is expanded to five bits for Packed-24 modes. In the case, the value is taken as a byte count, rather than a pixel count. This allows skipping up to 31 bytes (seven pixels) of each scan line of destination.

For the CL-GD5436 only, GR2F[6:5] can be used to skip bytes of the source field for system-to-screen BLTs. This allows unaligned source fields to be transferred without the overhead of unaligned bus cycles. The field will select the initial byte of the first DWORD of each scan line. If this field is programmed to a non-zero value for color-expanded system-to-screen BLTs, GR33[0] must be programmed to '1'.

8. PATTERN FILLS

In some cases it is necessary to fill an area with a repeating pattern. The CL-GD543X/'4X BLT engine has provisions for pattern replication with or without color expansion. The pattern size is 8 pixels × 8 pixels, chosen for compatibility with Microsoft Windows.

If GR30[6] is programmed to a '1', the source is taken to be an array of 8 pixels × 8 pixels. The array will be repeatedly copied to the destination area with or without color expansion. For any scan line, the same eight pixels of source data are used repeatedly. The source Pitch will be ignored. The number of bytes in the source pattern is a function of the operating mode, as indicated in Table D8-10.

Table D8-10. Source for Pattern Fills

Operating Mode	Arrangement	Starting Address Boundary	Note
Color Expansion	8 bytes of monochrome data for 64 pixels	8 bytes	
8-bit Pixels	64 bytes of color data for 64 pixels	64 bytes	
16-bit Pixels	128 bytes of color data for 64 pixels	128 bytes	
24-bit Pixels	24 bytes of color data plus 8 bytes of padding for each scan line, repeated 8 times	256 bytes	CL-GD5436
32-bit Pixels	256 bytes of color data for 64 pixels	256 bytes	

9. PATTERN VERTICAL PRESET (CL-GD5430/'36/'40 Only)

The CL-GD5430/'36/'40 supports pattern vertical preset for pattern fill. The low-order three bits of the Source Start Address (GR2C[2:0]) select the scan line to be used for the first, or only, scan line. This is because the pattern must be aligned as shown in the table above. This makes it possible to easily force vertical alignment of the pattern. This vertical alignment is useful for filled rectangles and filled polygons. These patterns are described in the following sections.

10. PATTERNED POLYGON FILLS (CL-GD5430/'36/'40 Only)

The CL-GD5430/'36/'40 has special provisions for patterned polygon fills with color expansion. The polygon to be filled is decomposed into a series of single scan lines, each of which is filled with a single BitBLT. The first such operation will read all eight bytes of monochrome

pattern. Then, as long as no writes to the Source Start Address registers or to the BLT Mode register occur, subsequent operations will use the previously loaded source data (skipping the read cycle). In addition, the Y offset, initially set by the three low-order bits of the Source Start Address (GR2C[2:0]), will be incremented modulo eight at the end of each operation. This results in each scan line starting one byte further into the pattern than the scan line immediately above. The polygon may be filled with a series of single scan line fills that change only the Destination Start Address, left-edge pixel clipping, and Width. The operation should proceed from top to bottom. If the operation goes from bottom to top, the pattern will be vertically flipped.

11. SOLID COLOR FILL *(CL-GD5436 only)*

The CL-GD5436 will perform a solid color fill. GR33[2] is programmed to '1' for this. GR30[7] and GR30[6] must both be programmed to '1' (enable color expansion and enable pattern copy). GR30[3] must be set to '0' (no transparency). GR30[2] must be set to '0'. The contents of the Foreground register(s) will be written to the destination rectangle. Any expansion width can be used. This functions precisely as though the pattern was all 1's, except the pattern isn't read.

This function can be used to implement a full foreground/background color expansion for packed-24 modes. The destination block can be set to the background color, and then the foreground can be written using the monochrome pattern (with transparency enabled).

12. BLT DIRECTION

If the source and destination areas overlay in display memory, the application program must ensure that the operation progresses so that the source area is not overwritten prior to being used. Consider Figure D8-3, if the operation were to begin with the upper left corner of the source and destination, the contents of the overlapped area would be overwritten before being used.

If GR30[0] is programmed to '1', the direction in which the operation progresses will be reversed. The bytes will be processed right-to-left and bottom-to-top. In Figure D8-3 this guarantees that bytes of the source are used prior to being changed. Observe that the start addresses in this case are the highest in the areas, not the lowest. BLTs with color expansion must never be programmed for reverse direction.

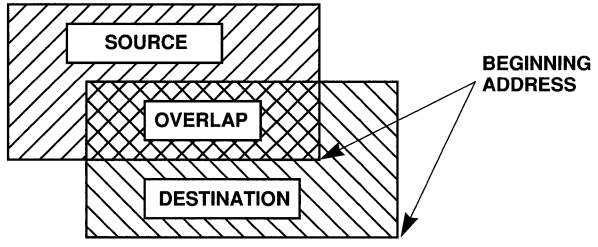

Figure D8-3. Overlapping BLT

13. SYSTEM-TO-SCREEN

If GR30[2] is programmed to '1', the BLT source will be system memory. The CPU must perform the bus transfers; the CL-GD543X/'4X is never a bus master. The address provided by the CPU with such transfers is ignored (except it must be in the range being decoded as display memory).

NOTES:

1. The CPU *must* execute DWORD transfers (even though these would be broken into pairs of WORD transfers for ISA bus).
2. In the case of the CL-GD5430/'40, system-to-screen bitBLT with color expansion requires that GR2C be written during the setup even though the register is not used.
3. SR8[6] *must* be programmed to '0'.

For system-to-screen BitBLTs not involving color expansion, up to three bytes of the last transfer for each scan line will be ignored (depending on Width). The next scan line will begin with the next DWORD transfer.

For system-to-screen BitBLTs which involve color expansion, up to seven bits of the last (partially used) byte will be ignored at the end of each scan line, and unused bytes will be used at the beginning of the next scan line.

For the CL-GD5436, GR33[0] controls how data are skipped at the end of each scan line. If GR33[0] is programmed to '0', the unused bits of the current byte will be skipped as described above. If GR33[0] is programmed to '1', the unused bits of the current DWORD will be skipped at the end of each scan line. That is, up to seven bits of the current byte and the next three whole bytes will be discarded. The next scan line will begin with the first bit of the next DWORD. This is useful is keeping DWORD transfers aligned when the monochrome source image must be clipped.

14. START/PAUSE/RESET CONTROLS

Once the parameters have been loaded into the registers the BitBLT can be started. On the CL-GD5436 only, it is possible to pause any system-to-screen BLT. It is also possible to unconditionally reset the BLT engine. These functions are controlled by bits in GR31.

To start a BLT, register GR31[1] is programmed to '1'. So long as the BLT is in progress, GR31[0] will be '1'. When the BLT has completed, GR31[0] will be '0'. Monitoring GR31[0] is the most straight forward way to synchronize with the BLT engine. While the BLT is in progress, the CL-GD543X/'4X display memory and BLT registers (except GR31) must not be accessed for read or write (except the buffered registers on the CL-GD5436).

If the write buffer is not empty when a BitBLT is started, the BitBLT will not take place properly. This was uncovered by a programming sequence in which the BLT registers were loaded, then a pattern was written to memory, and then the BLT was started immediately. It is recommended that this sequence be reversed so that any necessary writes to the DRAM take place before the registers are loaded. This will allow the write buffer to be emptied before the BLT is started.

14.1 Pause (CL-GD5436)

A system-to-screen BLT can be made to pause on the CL-GD5436 by programming GR31[5] to '1'. Display memory writes will not be directed through the BLT engine but rather will be directed to display memory at the address specified on the bus. Reads are not permitted and will return incorrect data. Programming GR31[5] to '0' will terminate the pause and writes to display memory will be directed to the BLT engine (if a system-to-screen BLT requires additional data to complete).

14.2 Reset

The current operation can be unconditionally stopped, and the entire BLT engine reset by programming GR31[2] to '1'. GR31[3] and GR31[0] will be forced to '0' and the operation will stop after the next write. This may result in partial pixels being written.

15. AUTO-START (CL-GD5436 Only)

The CL-GD5436 includes an auto-start capability and double buffered registers. This allows the parameters for BLT *n+1* to be loaded will BLT *n* is taking place. Furthermore, when BLT *n* completes, BLT *n+1* can begin with no host intervention. This allows a high degree of parallelism between the host and the controller.

Auto-start is enabled by programming GR31[7] to '1'. When GR31[7] is '1', a BLT will start automatically whenever the engine is not busy and a set of parameters is available. A set of parameters is taken to be available if the destination address has been written since the last time a BLT started. The destination address should always be the last registers written.

The host must monitor GR31[4] to determine when the buffered registers are available to be loaded with a new set of parameters. When it is a '0', the registers can be safely loaded. The destination address must be written last to avoid starting a BLT with an incomplete set of parameters. Registers whose contents are not changed from the previous set of parameters do not need to be written.

If GR31[7] is programmed to '0', auto-start will be disabled. BLTs will be manually started by programming GR31[1] to '1' in the normal manner.

16. COMPLETE BLT REGISTER LIST

Table D8-11 lists every register associated with the BLT engine.

Table D8-11. BLT Register List

Name	MM I/O Offset (Hex.)	Used For:	Size (Bits)	Modified?	Note	Double Buffered
GR0	00	Background Color Byte 0	8	No	–	Yes
GR1	04	Foreground Color Byte 0	8	No	–	Yes
GR10	01	Background Color Byte 1	8	No	–	Yes
GR11	05	Foreground Color Byte 1	8	No	–	Yes

Table D8-11. BLT Register List *(cont.)*

Name	MM I/O Offset (Hex.)	Used For:	Size (Bits)	Modified?	Note	Double Buffered
GR12	02	Background Color Byte 2	8	No	CL-GD5434/'36	Yes
GR13	06	Foreground Color Byte 2	8	No	CL-GD5434/'36	Yes
GR14	03	Background Color Byte 3	8	No	CL-GD5434/'36	Yes
GR15	07	Foreground Color Byte 3	8	No	CL-GD5434/'36	Yes
GR20	08	Width Byte 0	8	Yes	–	Yes
GR21	09	Width Byte 1	5	Yes	3 bits on CL-GD5430/'40	Yes
GR22	0A	Height Byte 0	8	No	–	Yes
GR23	0B	Height Byte 1	3	No	–	Yes
GR24	0C	Destination Pitch Byte 0	8	No	–	Yes
GR25	0D	Destination Pitch Byte 1	5	No	–	Yes
GR26	0E	Source Pitch Byte 0	8	No	–	Yes
GR27	0F	Source Pitch Byte 1	5	No	–	Yes
GR28	10	Destination Start Byte 0	8	Yes	–	Yes
GR29	11	Destination Start Byte 1	8	Yes	–	Yes
GR2A	12	Destination Start Byte 2	6	Yes	5 bits on CL-GD5430/'40	Yes
GR2B	13	Reserved	–	–	–	n/a
GR2C	14	Source Start Byte 0	8	Yes	–	Yes
GR2D	15	Source Start Byte 1	8	Yes	–	Yes
GR2E	16	Source Start Byte 2	6	Yes	5 bits on CL-GD5430/'40	Yes
GR2F	17	Write Mask	3	No	CL-GD5430/'36/'40	Yes
GR30	18	BLT mode	8	No	–	Yes
GR31	40	Start/Status	4	–	–	No
GR32	1A	Raster OP	8	No	–	Yes
GR33	1B	BLT Mode Extensions	–	–	CL-GD5436 only	Yes
SR2	–	Plane Mask register	8	No	–	No

17. MEMORY-MAPPED I/O

All the registers listed above, except SR2, can be written as memory locations. This is called *memory-mapped I/O*. This makes it possible to load the registers quickly because they can be written four-per-access.

Memory-mapped I/O is enabled when SR17[2] is programmed to a '1'. The registers are mapped beginning at address B800:0. The CL-GD5430/'36/'40 can be programmed to place the memory-mapped I/O area at the last 256 bytes of the linear address space. GR6[3:2] must be programmed to '01'. When memory-mapped I/O is enabled, only GR31 is accessi-

ble as an I/O location. Appendix B20, "Memory-Mapped I/O", contains a list of registers ordered by offset.

18. OTHER CONSIDERATIONS AND PROGRAMMING NOTES

Protecting Bytes: For 32-bit-per-pixel modes, it may be desirable to avoiding modifying one or more bytes of each pixel during BLTs or ordinary memory writes. This is most likely to apply to the Alpha byte. An easy way to do this is to set GRB[2] to '1'; SR2 will then act as a byte-wise Write Protect for the entire 8-byte data path.

BLT Registers Modified: The source and destination start registers are modified while the BLT is occurring. Therefore, they must be re-written prior to the next BLT even if the initial values are to be the same. On the CL-GD5436, this does not apply when the buffered registers are being used. Note, however, that the destination start address must be written to signal that a new set of parameters are available.

GRB[2] Side Effect: When GRB[2] of any Cirrus Logic VGA Controller with a BitBLT engine is programmed from '1' to '0', the following side effect occurs. GR0[7:4] and GR1[7:4] are cleared to '0'. This does not apply to the CL-GD5436.

GRB Programming: The CL-GD5434 requires that GRB[4,3,1] must be programmed to 0s for any BitBLT.

GR25, GR27 Programming: The CL-GD5434, production version D or earlier, requires that any screen-to-screen BitBLT that does not involve color expansion must have the low order three bits of the Source Pitch (GR27) and the Destination Pitch (GR25) programmed to 000b.

19. EXAMPLE

Text Expansion Example: Using color expansion, a text string is copied from system memory. The monochrome image of the string is arranged in system memory by scan line. The destination area is 150 pixels × 25 scan lines (8-bits-per-pixel); the destination Pitch is 1024 pixels. The registers must be loaded as indicated in Table D8-11. If the background pixels are not to be written, GR30[3] would be set to a '1'.

Table D8-12. Text Expansion BLT

Register(s)	Contents (Decimal)	Field	How Calculated
GRB[4,3,1]	0		See notes in Section 18
GR0/GR10/GR12/GR14	xx	Background color	As desired
GR1/GR11/GR123/GR15	xx	Foreground color	As desired
GR20/GR21	149	Width	150 – 1
GR22/GR23	24	Height	25 – 1
GR24/GR25	1024	Destination Pitch	–
GR26/GR27	n/a	Source Pitch	(System memory)
GR28/GR29/GR2A	xxxxx	Destination Start	–

Table D8-12. Text Expansion BLT *(cont.)*

Register(s)	Contents (Decimal)	Field	How Calculated
GR2C/GR2D/GR2E	n/a	Source Start	(System memory)
GR2F	0	Write Mask	No clipping
GR30	84h	Mode	Color Expansion, System memory source
GR32	0Dh	Raster Op	SRC COPY
GR33	0	Mode Extension	Discard partial bytes
GR31	2	Start	Set bit 1

After the registers are loaded the source bitmap must be transferred. The first DWORD write will transfer the image for pixels 0–31. The second write will transfer the image for pixels 32–63. The third will transfer 64–95, and the fourth will transfer 96–127. The fifth DWORD transfer is special. The data for this transfer is shown in Figure D8-4.

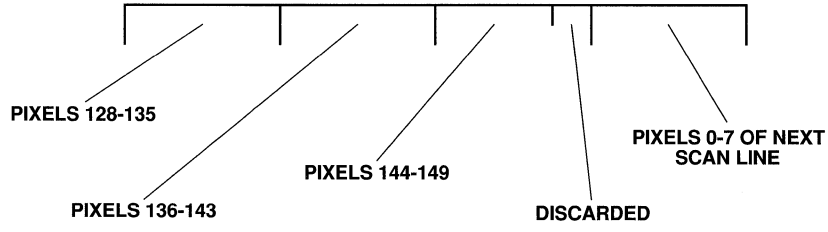

Figure D8-4. Color Expand Transfer

A total of 119 DWORD transfers will be required; the last one byte of the last transfer will be discarded.

Appendix D9

Cirrus Logic Bulletin Board Service

CIRRUS LOGIC BBS

1. INTRODUCTION

This appendix discusses the Cirrus Logic Bulletin Board Service (BBS) which is intended primarily for one-way communication from Cirrus Logic to its OEMs and end users. The latest drivers are available to Cirrus Logic OEMs and end users. Cirrus Logic OEMs can obtain the latest BIOS images, schematics, and other files over the BBS.

Cirrus Logic maintains strict access control to this bulletin board to minimize the possibility of distribution of pirated or virus-ridden software. Only Cirrus Logic employees have upload access to publicly downloadable file areas. An end user or OEM can upload files, but not to a publicly downloadable area.

The software running on this board is Wildcat!™ IM, written by Mustang Software®, Inc. Cirrus Logic operates eight remote nodes and one local node to the BBS.

2. TELEPHONE NUMBER AND COMMUNICATION PARAMETERS

The telephone number of the Cirrus Logic BBS is (510) 440-9080. The communication parameters are:

- 8 data bits
- No parity
- 1 stop bit

The Cirrus Logic BBS line supports up to a 14,400 baud rate. Connections of 300 and 1200 bps will be allowed, as long as phones lines remain available for users with faster modems.

3. FIRST-TIME LOG ON

Upon connection with the bulletin board, a name and password are suggested for a guest account. If the users is merely downloading drivers, demonstration programs, or utilities, it is best to use the guest account. This avoids filling out the questionnaire yet allows access to most files.

If schematic diagrams or BIOS files are required, or if the user is planning to upload files, he should log on with his name (or company name). The system will prompt a password entry and require that the questionnaire be completed. When completed, the name and password chosen is added to the user database and access is the same as a guest log on.

4. UPGRADED ACCESS

If requiring access to BIOS image or schematic diagram files, or if exchanging files with Cirrus Logic personnel on a regular basis, an account upgrade is necessary. Account upgrades are handled through your contact at Cirrus Logic (usually through a sales office). Three to five working days are required for the request to be processed after being received at Cirrus Logic in Fremont, California.

5. ORGANIZATION OF THE BOARD

The Cirrus Logic BBS is organized into 'Product' areas and a 'General Public Messages' area. The Product areas, as of July, 1994, are listed in Table D9–1.

Table D9-1. Product Areas

Area	Name	Note
1	General Public Messages	Non-specific programs, README, etc. Also 510/520, 5320, 5410
5	5401/'02/'20	Software-wise, 5420 is related to 5401/'02
6	5422/'24/'26/'28/'29	
7	5430/'34/'36/'40	Alpine
8	545X	Northstar
9	Spare Desktop	Not yet open
10	610/620	
11	62XX	
12	634X	
13	641X	
14	642X	
15	6440	
16	754X	Nordic
17	Pixel Products	
18	Modems	
19	6710/6720	
20	CL-DD72XX	IDE

The General Public Messages area contains non-specific programs such as PKWare and ID_CHIP. The upload areas also reside in the General Public Messages area. The upload areas are readable only by Cirrus Logic employees.

The other product areas are connected to five file areas each. These file areas are listed in Table D9-2.

Table D9-2. File Areas within Product Areas

File Area	Note	Download Access
Drivers	Driver disks	All
Demonstrations	BLT demo, slide viewers, etc.	All
Utilities	for example, CLMODE	All
BIOS	BIOS images, MFGTST	Integrator, OEM
Schematics	OrCAD schematic diagrams	OEM

Appendix E1

E

BIOS Extensions

BIOS EXTENSIONS

1. INTRODUCTION

This document covers the extensions to the VGA BIOS. The extensions unique to Cirrus Logic are covered in section 2. The VESA charter is reprinted as section 3 and the VESA extensions are covered in section 4.

The Video mode tables are in the Data Book, reprinted as Chapter 3 of this book.

2. CIRRUS LOGIC EXTENSIONS

The Cirrus Logic BIOS supports all standard VGA BIOS Interrupt 10h video service functions. In addition, the BIOS provides extensive support for various features of the Cirrus Logic VGA controller. These functions are available as extended functions under Interrupt 10h.

The standard VGA BIOS Interrupt 10h video service functions are described in Chapter 10 of the TRM.

All extended function calls will preserve the CPU registers, except those used to pass information from the BIOS.

2.1 Function Summary

The following table provides an overview of the extended functions provided by the Cirrus Logic BIOS.

Table E1-1. Function Summary

AH Register	BL Register	Function
12h	80h	Inquire VGA Type
12h	81h	Inquire BIOS Version Number
12h	82h	Inquire Design Revision Code
12h	85h	Return Installed Memory
12h	9Ah	Inquire User Options
12h	A0h	Query Video Mode Availability
12h	A1h	Read Monitor Type and ID
12h	A4h	Set Monitor Type
12h	AEh	Get High Refresh
12h	AFh	Set High Refresh

2.2 Inquire VGA Type

This function provides a mechanism for software to determine the type of Cirrus Logic VGA controller, silicon revision number and its corresponding hardware capabilities. BIOS versions that do not support this family of function will preserve the input value in AL register. The VGA types of particular interest to readers of this manual are in **bold** type.

Input:
AH= 12h
BL= 80h

Output:
AX= Controller type
0= No extended alternate select support
1= Reserved
2= CL-GD510/520
3= CL-GD610/620
4= CL-GD5320
5= CL-GD6410
6= CL-GD5410
7= CL-GD6420
8= CL-GD6412
10h= CL-GD5401
11h= CL-GD5402
12h= CL-GD5420
13h= CL-GD5422
14h= CL-GD5424
15h= CL-GD5426
16h= CL-GD5420r1
17h= CL-GD5402rl
18h= CL-GD5428
19h= CL-GD5429
20h= CL-GD6205
21h= CL-GD6215
22h= CL-GD6225
23h= CL-GD6235
24h= CL-GD6245
31h= CL-GD5434
32h= CL-GD5430
33h= CL-GD5434 rev E & F
35h= CL-GD5440
36h= CL-GD5436
40h= CL-GD6440
41h= CL-GD7542
50h= CL-GD5452

BL= Silicon revision number
0-7Fh= Silicon revision
80h= Silicon revision number not available

2.3 Inquire BIOS Version Number

This function provides a mechanism for software to determine the BIOS version number.

Input: AH= 12h
BL= 81h

Output: AH= Major BIOS version number
AL= Minor BIOS version number

Example: If BIOS version is 1.02, then AH is 01 and AL is 02.

2.4 Inquire Cirrus Logic Design Revision Code

This function provides a mechanism for software to determine the revision of Cirrus Logic silicon.

Input: AH= 12h
BL= 82h

Output: AL= Chip revision

2.5 Return Installed Memory

The function returns the amount of video memory present in 64K units.

Input: AH= 12h
BL= 85h

Output: AL= Amount of video memory present in 64K units.

2.6 Inquire User Options

This function returns the current status of user options. The values of the vertical frequencies and maximum vertical resolution correspond to the values defines as input for functions A4h, Set Monitor Type (Vertical).

Input: AH= 12h
BL= 9Ah

Output: AX= Contains the following options
Bits 13:0= Reserved
Bit 14= Vertical montype 640 x 480 frequency (VGA refresh)
Bit 15= Reserved
BX= Reserved
CX= Contains the following options
Bit 0= Reserved
Bits 3:1= 1280 x 1024 vertical frequency
Bits 7:4= Maximum Vertical Resolution
Bits 11:8= 800 x 600 vertical frequency
Bits 15:12= 1024 x 768 vertical frequency
DX= Reserved

2.7 Query Video Mode Availability

Input:
AH= 12h
AL= Video mode number (0-7fh)
BL= A0h

Output:
AH= Bit 0
0= Video mode not supported
1= Video mode supported

DS:SI: Pointer to standard video parameters, or FFFF:FFFF if standard parameters undefined for this mode
ES:DI: Pointer to supplemental video parameters, or FFFF:FFFF if supplemental parameters undefined for this mode

BX= Offset to BIOS sub-routine that will fix up the parameters pointed to by DS:SI. This routine requires ES:DI points to the proper supplemental video parameters.

2.8 Read Monitor ID/Type

This function uses the analog sense circuitry to detect the type of monitor attached. The digital Monitor ID pins are not used to read the monitor type. The Monitor ID returned in BH is determined by the monitor type sensed (color, monochrome, or none) and may not correspond to the actual digital Monitor ID of the current monitor. This function is typically used as a diagnostic function to test the monitor sense that occurs during POST. The capabilities (refresh rates supported) of the monitor are determined by the parameters passed to function A4h, Set Monitor Type (Vertical).

Input:
AH = 12h
BL = A1h Read monitor ID and type from 15-pin connector

Output:
BH = Monitor ID
0Dh = IBM 8503 or equivalent
0Eh = IBM 8512/8513 or equivalent
0Fh = No monitor
00 thru 0C = reserved

BL = Monitor gender
00 = Color display
01 = Grayscale display
02 = No display

2.9 Set Monitor Type

This function sets the monitor type in terms of vertical timings. The monitor type information is used by the BIOS to determine which frequency to use when selecting an extended mode. It is also used (in conjunction with the amount of display memory available) to determine what extended modes are available. The monitor type can be read back using Function 9A.

To maintain compatibility with previous Cirrus Logic BIOS releases, obsolete frequencies have not been removed from this function. The appearance of any frequency in the description of this BIOS call is no guarantee that any given BIOS will actually support that frequency. In general, the trend is toward supporting higher frequencies and deleting support of lower frequencies.

NOTE: Calls to the obsolete functions 0A2h (Set Monitor Type - Horizontal) and 0A3h (Set Refresh Type) will be converted into this call.

Input:
AH = 012h
BL = 0A4h
AL[3:0] = Maximum Vertical Resolution
- 000h = 480 scanlines
- 001h = 600 scanlines
- 002h = 768 scanlines
- 003h = 1024 scanlines
- 004h - 00Fh = Reserved

AL[4] = 640 x 480 Frequency
- 0h = 60 Hz
- 1h = High Refresh: Refer to Subfunction AEh to select 72 or 75 Hz.

AL[7:5] = Reserved
BH[3:0] = 800 x 600 Frequency
- 000h = 56 Hz
- 001h = 60 Hz
- 002h = 72 Hz
- 003h = 75 Hz
- 004h - 00Fh = Reserved

BH[7:4] = 1024 x 768 Frequency
- 000h = 43i Hz
- 001h = 60 Hz
- 002h = 70 Hz
- 003h = 72 Hz
- 004h = 75 Hz
- 005h - 00Fh = Reserved

CH[3:0] = Reserved
CH[7:4] = 1280 x 1024 Frequency
- 000h = 43i Hz
- 001h = 60 Hz
- 002h = 71.2 Hz (CL-GD5434 Rev E and F)
- 003h = 75 Hz (CL-GD5434 Rev E and F)
- 004h - 00Fh = Reserved

CL = Reserved
DX = Reserved

2.10 Get High Refresh

This function returns the vertical refresh rate of the 640 x 480 high refresh modes.

Input:
AH = 012h
BL = 0AEh

Output:
AL = Bit 0 indicates 640 x 480 high refresh rate
- 0 = 72 Hz
- 1 = 75 Hz

2.11 Set High Refresh

This function sets the vertical refresh rate of the 640 x 480 high refresh modes. The application must call this function after calling Set Monitor Type (Subfunction A4h), specifying 640 x 480 high refresh mode.

Input: AH = 012h
BL = 0AFh
AL = Bit 0 indicates 640 x 480 high refresh rate
0 = 72 Hz
1 = 75 Hz

3. VESA® SUPER VGA STANDARD

Video Electronics Standards Association
2150 N. First Street, Suite 440
San Jose, CA 95131-2020
TEL: (408) 435-0333 FAX:(408) 435-8225

Purpose: To standardize a common software interface to Super VGA video adapters to provide simplified software application access to advanced VGA products.

Summary: The standard provides a set of functions that an application program can use to **a)** obtain information about the capabilities and characteristics of a specific Super VGA implementation, and
b) to control the operation of such hardware in terms of video mode initialization and video memory access. The functions are provided as an extension to the VGA BIOS video services, accessed through Interrupt 10h.

3.1 Goals and Objectives

The purpose of the VESA VGA BIOS Extension is to provide a common software interface for developers to design applications successfully on widely disparate architectures. Being a common software interface to Super VGA graphics products, the primary objective is to enable application and system software to adapt to and exploit the wide range of features available in these VGA extensions.

The VESA BIOS Extension attempts to address the following two main issues:
a) Return information about the video environment to the application, and
b) Assist the application in initializing and programming the hardware.

3.1.1 Video Environment Information

The VESA BIOS Extension provides several functions to return information about the video environment. These functions return system-level information as well as video-mode-specific details. Function 00h returns general system-level information, including an OEM identification string. The function also returns a pointer to the supported video modes. Function 01h may be used by the application to obtain information about each supported video mode. Function 03h returns the current video mode.

3.1.2 Programming Support

The VESA BIOS Extension provides several functions to interface to the different Super VGA hardware implementations. The most important of these is Function 02h, Set Super VGA Video mode. This function isolates the application from the tedious and complicated task of setting up a video mode. Function 05h provides an interface to the underlying mem-

ory-mapping hardware. Function 04h enables an application to save and restore a Super VGA state without determining specifics of the particular implementation.

3.1.3 Compatibility

The primary design objective of the VESA BIOS Extension is to preserve maximum compatibility to the standard VGA environment. In no way should the BIOS extensions compromise compatibility or performance. Another related concern is to minimize the changes necessary to an existing VGA BIOS. RAM- as well as ROM-based implementations of the BIOS extension should be possible.

3.2 Standard VGA BIOS

A primary design goal with the VESA BIOS Extension is to minimize the effects on the standard VGA BIOS. Standard VGA BIOS functions should need to be modified as little as possible. This is important since ROM- as well as RAM-based versions of the extension may be implemented.

Two standard VGA BIOS functions are affected by the VESA extension. These are Function 00h (Set Video Mode) and Function 0Fh (Read current video state). VESA-aware applications will not set the video mode using VGA BIOS Function 00h. Nor will such applications use VGA BIOS Function 0Fh. VESA BIOS Functions 02h (Set Super VGA Mode) and 03h (Get Super VGA Mode) will be used instead.

VESA-unaware applications (such as old Pop-up programs and other TSRs, or the CLS command of MS-DOS), might use VGA BIOS Function 0Fh to get the present video mode. Later it may call VGA BIOS Function 00h to restore/re-initialize the old video mode.

To make such applications run properly, VESA recommends that whatever value returned by VGA BIOS Function 0Fh (it is the OEM's responsibility to define this number), it can be used to re-initialize the video mode through VGA BIOS Function 00h. Thus, the BIOS should record the last Super VGA mode in effect.

It is recommended, but not mandatory, to support output functions (such as TTY-output, scroll, set pixel, etc.) in Super VGA modes. If the BIOS extension doesn't support such output functions, Bit D2 (Output functions supported) of the ModeAttributes field (returned by VESA BIOS Function 01h) should be cleared.

3.3 Super VGA Mode Numbers

Standard VGA mode numbers are 7-bits-wide and presently ranges from 00h to 13h. OEMs have defined extended video modes in the range 14h to 7Fh. Values in the range 80h to FFh cannot be used, since VGA BIOS Function 00h (Set Video Mode) interprets bit 7 as a flag to clear/not clear video memory.

Due to the limitations of 7-bit mode numbers, VESA Video mode numbers are 15-bits-wide. To initialize a Super VGA mode, its number is passed in the BX register to VESA BIOS Function 02h (Set Super VGA Mode).

The format of VESA mode numbers is as follows:

D0-D8 =	Mode number If D8 = 0, this is not a VESA-defined mode If D8 = 1, this is a VESA-defined mode
D9-D14 =	Reserved by VESA for future expansion (= 0)
D15 =	Reserved (= 0)

4. EXTENDED VESA® BIOS FUNCTIONS

Several new BIOS calls have been defined to support Super VGA modes. For maximum compatibility with the standard VGA BIOS, these calls are grouped under one function number. This number is passed in the AH register to the INT 10h handler.

The designated Super VGA extended function number is 4Fh. This function number is presently unused in most, if not all, VGA BIOS implementations. A standard VGA BIOS performs no action when function call 4F is made. Super VGA Standard VS911022 defines subfunctions 00H through 08H. Subfunction numbers 09H through 0FFH are reserved for future use.

4.1 Status Information

Every function returns status information in the AX register. The format of the status word is as follows:

AL =	4Fh:	Function is supported
AL ! =	4Fh:	Function is not supported
AH =	00h:	Function call successful
AH =	01h:	Function call failed

Software should treat a non-zero value in the AH register as a general failure condition. In later versions of the VESA BIOS Extension new error codes might be defined.

4.2 Function 00h — Return Super VGA information

The purpose of this function is to provide information to the calling program about the general capabilities of the Super VGA environment. The function fills an information block structure at the address specified by the caller. The information block size is 256 bytes.

Input: AH = 4Fh Super VGA support
AL= 00h Return Super VGA information
ES:DI= Pointer to buffer

Output: AX = Status
All other registers are preserved.

The information block has the following structure:

```
VgaInfoBlock struc
    VESASignature   db      'VESA'          ; 4 signature bytes
    VESAVersion     dw      ?               ; VESA version number
    OEMStringPtr    dd      ?               ; Pointer to OEM string
    Capabilities    db      4 dup (?)       ; capabilities of the video environment
    VideoModePtr    dd      ?               ; pointer to supported Super VGA Modes
    TotalMemory     dw      ?               ; Number of 64kb memory blocks on board
    Reserved        db      236 dup (?)     ; Remainder of VgaInfoBlock
VgaInfoBlock ends
```

The VESASignature field contains the characters 'VESA' if this is a valid block.

The VESAVersion is a binary field that specifies what level of the VESA standard the Super VGA BIOS conforms to. The higher byte specifies the major version number. The lower byte specifies the minor version number. The current VESA version number is 1.2. Applications written to use the features of a specific version of the VESA BIOS Extension are guaranteed to work in later versions. The VESA BIOS Extension will be fully upwards compatible.

The OEMStringPtr is a far pointer to a null-terminated OEM-defined string. The string may used to identify the video chip, video board, memory configuration, etc., to hardware-specific display drivers. There are no restrictions on the format of the string.

The Capabilities field describes what general features are supported in the video environment. The bits are defined as follows:

D0= DAC is switchable
    0 = DAC is fixed width, with 6-bits per primary color
    1 = DAC width is switchable
D1-31 = Reserved

The VideoModePtr points to a list of supported Super VGA (VESA-defined as well as OEM-specific) mode numbers. Each mode number occupies one word (16 bits). The list of mode numbers is terminated by a -1 (0FFFFh). Please refer to Section 4.3 for a description of VESA mode numbers. The pointer could point into either ROM or RAM, depending on the specific implementation. Either the list would be a static string stored in ROM, or the list would be generated at run-time in the information block (see above) in RAM. It is the applications responsibility to verify the current availability of any mode returned by this Function through the Return Super VGA mode information (Function 1) call. Some of the returned modes may not be available due to the video boards current memory and monitor configuration.

The TotalMemory field indicates the amount of memory installed on the VGA board. Its value represents the number of 64K bytes blocks of memory currently installed.

4.3 Function 01h — Return Super VGA Mode Information

This function returns information about a specific Super VGA Video mode that was returned by Function 0. The function fills a mode information block structure at the address specified by the caller. The mode information block size is maximum 256 bytes.

Some information provided by this function is implicitly defined by the VESA mode number. However, some Super VGA implementations might support other video modes than those defined by VESA. To provide access to these modes, this function also returns various other information about the mode.

Input:	AH =	4Fh	Super VGA support
	AL=	01h	Return Super VGA Mode information
	CX =		Super VGA Video Mode number
	ES:DI =		Pointer to 256 byte buffer
Output:	AX =		Status
	All other registers are preserved.		

The mode information block has the following structure:

```
ModeInfoBlock   struc
; mandatory information

        ModeAttributes          dw      ?       ; mode attributes
        WinAAttributes          db      ?       ; window A attributes
        WinBAttributes          db      ?       ; window B attributes
        WinGranularity          dw      ?       ; window granularity
        WinSize                 dw      ?       ; window size
        WinASegment             dw      ?       ; window A start segment
        WinBSegment             dw      ?       ; window B start segment
        WinFuncPtr              dd      ?       ; pointer to window function
        BytesPerScanLine        dw      ?       ; bytes per scanline extended information

        XResolution             dw      ?       ; horizontal resolution
        YResolution             dw      ?       ; vertical resolution
        XCharSize               db      ?       ; character cell width
        YCharSize               db      ?       ; character cell height
        NumberOfPlanes          db      ?       ; number of memory planes
        BitsPerPixel            db      ?       ; bits per pixel
        NumberOfBanks           db      ?       ; number of banks
        MemoryModel             db      ?       ; memory model type
        BankSize                db      ?       ; bank size in kb
        NumberOfImagePages      db              ?       ; Number of Images
        Reserved                db      1       ; reserved for page function

        RedMaskSize             db      ?       ;size of direct color red mask in bits
        RedFieldPosition        db      ?       ;bit position of lsb of red mask
        GreenMaskSize           db      ?       ;size of direct color green mask in bits
        GreenFieldPosition      db      ?       ;bit position of lsb of green mask
        BlueMaskSize            db      ?       ;size of direct color blue mask in bits
        BlueFieldPosition       db      ?       ;bit position of lsb of blue mask
        RsvdMaskSize            db      ?       ;size of direct color reserved mask in bits
        RsvdFieldPosition       db      ?       ;bit position of lsb of reserved mask
        DirectColorModeInfo     db      ?       ;Direct Color Mode attributes

        Reserved                db      216 dup (?)     ; remainder of ModeInfoBlock
ModeInfoBlock   ends
```

The ModeAttributes field describes certain important characteristics of the video mode. Bit D0 specifies whether this mode can be initialized in the present video configuration. This bit can be used to block access to a video mode if it requires a certain monitor type, and that this monitor is presently not connected. Bit D1 specifies whether extended mode information is available. This information is required in VESA BIOS Extension Ver. 1.2 and later. Bit D2 indicates whether the BIOS have support for output functions such as TTY output, scroll, pixel output, etc., in this mode (it is recommended, but not mandatory, that the BIOS have support for all output functions).

The field is defined as follows:

D0= Mode supported in hardware
    0 = Mode not supported in hardware
    1 = Mode supported in hardware
D1 = Extended information available

0 = Extended Mode information not available
1 = Extended Mode information available
D2 = Output functions supported by BIOS
0 = Output functions not supported by BIOS
1 = Output functions supported by BIOS
D3 = Monochrome/Color Mode (see note below)
0 = Monochrome Mode
1 = Color Mode
D4 = Mode type
0 = Text Mode
1 = Graphics Mode
D5–D15 = Reserved

NOTE: Monochrome modes have their CRTC address at 3B4h. Color modes have their CRTC address at 3D4h. Monochrome modes have attributes in which only Bit 3 (video) and Bit 4 (intensity) of the attribute controller output are significant. Therefore, monochrome text modes have attributes of off, video, high intensity, blink, etc. monochrome graphics modes are two-plane graphics modes and have attributes of off, video, high intensity, and blink. Extended two-color modes that have their CRTC address at 3D4h, are color modes with one bit per pixel and one plane. The standard VGA Modes, 06h and 11h would be classified as color modes, while the standard VGA Modes 07h and 0fh would be classified as monochrome modes.

The BytesPerScanline field specifies how many bytes each logical scanline consists of. The logical scanline could be equal to or larger than the displayed scanline.

The WinAAttributes and WinBAttributes describe the characteristics of the CPU windowing scheme such as whether the windows exist and are read/writable, as follows:

D0 = Window supported
0 = Window is not supported
1 = Window is supported
D1 = Window readable
0 = Window is not readable
1 = Window is readable
D2 = Window writable
0 = Window is not writable
1 = Window is writable
D3–D7 = Reserved

If neither window is supported (bit D0 = 0), then an application can assume that window paging is not supported, and that the display memory buffer resides at the CPU address appropriate for the MemoryModel of the mode.

The WinGranularity specifies the smallest boundary, in kilobytes, on which the window can be placed in the video memory. If WinGranularity equals a '0' then CPU display memory windowing is not supported.

The WinSize specifies the size of the window in kilobytes.

The WinASegment and WinBSegment address specify the segment addresses where the windows are located in the CPU address space.

The WinFuncAddr specifies the address of the CPU video memory windowing function. The windowing function can be invoked either through VESA BIOS Function 05h, or by calling

the function directly. A direct call will provide faster access to the Hardware Paging registers than using INT 10h, and is intended to be used by high-performance applications. If WinFuncPtr is NULL (0000:0000) then CPU display memory windowing is not supported.

The XResolution and YResolution specify the width and height of the video mode. In graphics modes, this resolution is in units of pixels. In text modes this resolution is in units of characters. Note that text mode resolutions, in units of pixels, can be obtained by multiplying XResolution and YResolution by the cell width and height, if the extended information is present.

The XCharSize and YCharSize specify the size of the character cell in pixels.

The NumberOfPlanes field specifies the number of memory planes available to software in that mode. For standard 16-color VGA graphics, this would be set to a four. For standard Packed-pixel modes, the field would be set to a '1'.

The BitsPerPixel field specifies the total number of bits that define the color of one pixel. For example, a standard VGA Four-plane 16-color Graphics mode would have a four in this field and a packed-pixel 256-color Graphics mode would specify a eight in this field. The number of bits per pixel per plane can normally be derived by dividing the BitsPerPixel field by the NumberOfPlanes field.

The MemoryModel field specifies the general type of memory organization used in this mode. The following models have been defined:

00h = Text Mode
01h = CGA graphics
02h = Hercules graphics
03h = Four-plane planar
04h = Packed pixel
05h = Non-chain4, 256 color
06h = Direct Color
07h = YUV
08h–0fh = Reserved, to be defined by VESA
10h–ffh = To be defined by OEM

In Version 1.1 and earlier of the VESA Super VGA BIOS Extension, Direct Color 1:5:5:5, 8:8:8, and 8:8:8:8 are defined as Packed Pixel model with 16, 24, and 32 bits per pixel, respectively. In Version 1.2 and later of the VESA Super VGA BIOS Extension, it is recommended that Direct-color Modes use the Direct-color MemoryModel and use the MaskSize and FieldPosition fields of the ModeInfoBlock to describe the pixel format. BitsPerPixel is always defined to be the total size of the pixel, in bits.

The NumberOfBanks is the number of banks in which the scanlines are grouped. The remainder from dividing the scanline number by the number of banks is the bank that contains the scanline and the quotient is the scanline number within the bank. For example, CGA graphics modes have two banks and Hercules® Graphics Mode has four banks. For modes that don't have scanline banks (such as VGA Modes 0Dh-13h), this field should be set to a '1'.

The BankSize field specifies the size of a bank (group of scanlines) in units of 1K byte. For CGA and Hercules graphics modes this is a eight, as each bank is 8192 bytes in length. For modes that don't have scanline banks (such as VGA Modes 0Dh-13h), this field should be set to a '0'.

The NumberOfImagePages field specifies the number of additional complete display images that will fit into the VGA memory, at one time, in this mode. The application may load more than one image into the VGA memory if this field is a non-zero, and flip the display between the images.

The Reserved field has been defined to support a future VESA BIOS extension feature and will always be set to '1' in this version.

The RedMaskSize, GreenMaskSize, BlueMaskSize, and RsvdMaskSize fields define the size, in bits, of the red, green, and blue components of a Direct-color Pixel. A bit mask can be constructed from the MaskSize fields using simple shift arithmetic. Example MaskSize values for Direct-color 5:6:5 Mode would be 5, 6, 5, and 0, for the red, green, blue, and reserved fields, respectively. The MaskSize fields should be set to a '0' in modes using a MemoryModel that does not have pixels with component fields.

The RedFieldPosition, GreenFieldPosition, BlueFieldPosition, and RsvdFieldPosition fields define the bit position within the Direct-color Pixel or YUV pixel of the least-significant bit of the respective color component. A color value can be aligned with its pixel field by shifting the value left by the FieldPosition. Example FieldPosition values for Direct-color 5:6:5 mode would be 11, 5, 0, and 0, for the red, green, blue, and reserved fields, respectively. The FieldPosition fields should be set to a '0' in modes using a MemoryModel that does not have pixels with component fields.

The DirectColorModeInfo field describes important characteristics of Direct-color modes. Bit D0 specifies whether the color ramp of the DAC is fixed or programmable. If the color ramp is fixed, then it cannot be changed. If the color ramp is programmable, it is assumed that the red, green, and blue lookup tables can be loaded using a standard VGA DAC Color registers BIOS Call (AX = 1012h). Bit D1 specifies whether the Rsvd field of the Direct-color Pixel can be used by the application or is reserved, and thus unusable.

D0 = Color ramp is fixed/programmable
- 0 = Color ramp is fixed
- 1 = Color ramp is programmable

D1 = Rsrvd field is usable/reserved
- 0 = Rsvd field is reserved
- 1 = Rsvd field is usable by the application

The MapFuncAddr specifies the address of the mapping function. The mapping function can be invoked either through VESA BIOS Function 06h, or by calling the function directly. A direct call will provide a faster memory mapping than using INT 10h, and is intended to be used by high-performance applications.

NOTE: Version 1.1 and later VESA BIOS extensions will zero-out all unused fields in the Mode Information Block, always returning exactly 256 bytes. This facilitates upward compatibility with future versions of the standard, as any newly-added fields will be designed such that values of zero will indicate nominal defaults or non-implementation of optional features. (For example, a field containing a bit-mask of extended capabilities would reflect the absence of all such capabilities.) Applications that wish to be backwards-compatible to Version 1.0 VESA BIOS extensions should pre-initialize the 256-byte buffer before calling Return Super VGA mode Information.

4.4 Function 02h — Set Super VGA Video Mode

This function initializes a video mode. The BX register contains the video mode number. The format of VESA Mode numbers is described in Section 2. If the mode cannot be set, the BIOS should leave the video environment unchanged and return a failure error code.

Input:
AH = 4Fh Super VGA support
AL = 02h Set Super VGA Video Mode
BX = Video mode
D0–D14 = Video mode number
D15 = Clear memory flag
0 = Clear video memory
1 = Don't clear video memory

Output:
AX = Status
All other registers are preserved.

4.5 Function 03h — Return Current Video Mode

This function returns the current video mode in BX register. The format of VESA Video Mode numbers is described in Section 2 of this document.

Input:
AH = 4Fh Super VGA support
AL = 03h Return current video mode

Output:
AX = Status
BX = Current video mode number
All other registers are preserved.

NOTE: In a standard VGA BIOS, Function 0Fh (Read current video state) returns the current video mode in the AL register. In D7 of AL register, it also returns the status of the Memory Clear bit (D7 of 40:87). This bit is set if the mode was set without clearing memory. In this Super VGA Function, the Memory Clear Bit will not be returned in BX register since the purpose of the function is to return the video mode only. If an application must obtain the Memory Clear Bit, it should call VGA BIOS Function Fh.

4.6 Function 04h — Save/Restore Super VGA Video State

These functions provide a mechanism to save and restore the Super VGA video state. The functions are a superset of the three Subfunction under standard VGA BIOS Function 1Ch (Save/restore video state). The complete Super VGA video state (except video memory) should be saveable/restorable by setting the requested states mask (in the CX register) to 000Fh.

Input:
AH = 4Fh Super VGA support
AL = 04h Save/Restore Super VGA video state
DL = 00h Return save/restore state buffer size
CX = Requested states
D0 = Save/restore video hardware state
D1 = Save/restore video BIOS data state
D2 = Save/restore video DAC state
D3 = Save/restore Super VGA state

Output:
AX = Status
BX = Number of 64-byte blocks to hold the state buffer
All other registers are preserved.

Input:

AX =	4Fh	Super VGA support
AL =	04h	Save/Restore Super VGA video state
DL =	01h	Save Super VGA video state
CX =		Requested states (see above)
ES:BX =		Pointer to buffer

Output: AX = Status
All other registers are preserved.

Input:

AH =	4Fh	Super VGA support
AL =	04h	Save/Restore Super VGA video state
DL =	02h	Restore Super VGA video state
CX =		Requested states (see above)
ES:BX =		Pointer to buffer

Output: AX = Status
All other registers are preserved.

4.7 Function 05h — CPU Video Memory Window Control

This function sets or gets the position of the specified window in the video memory. The function allows direct access to the Hardware Paging registers. To use this function properly, the software should use VESA BIOS Function 01h (Return Super VGA Mode information) to determine the size, location, and granularity of the windows.

Input:

AH =	4Fh	Super VGA support
AL =	05h	Super VGA video memory window control
BH =	00h	Select super VGA video memory window
BL =		Window number
	0 =	Window A
	1 =	Window B
DX =		Window position in video memory (in window granularity units)

Output: AX = Status
See note below.

Input:

AH =	4Fh	Super VGA support
AL =	05h	Super VGA video memory window control
BH =	01h	Return super VGA video memory window
BL =		Window number
	0 =	Window A
	1 =	Window B

Output:

AX =	Status
DX =	Window position in video memory (in window granularity units)

See note below.

NOTE: This function is also directly accessible through a far call from the application. The address of the BIOS function may be obtained by using VESA BIOS Function 01h, return Super VGA Mode information. A field in the ModeInfoBlock contains the address of this function. Note that this function may be different among video modes in a particular BIOS implementation so the function pointer should be obtained after each set mode.

In the far call version, no status information is returned to the application. Also, in the far call version, the AX and DX registers will be destroyed. Therefore if AX and/or DX register must be preserved, the application must do so prior to making the far call.

The application must load the input arguments in BH, BL, and DX registers (for set window), but does not need to load either AH or AL register to use the far call version of this function.

4.8 Function 06h — Set/Get Logical Scanline Length

This function sets or gets the length of a logical scanline. This function allows an application to set up a logical video memory buffer that is wider than the displayed area. Function 07h then allows the application to set the starting position that is to be displayed.

Input:	AH =	4fh	Super VGA Support
	AL =	06h	Logical Scanline Length
	BL =	00h	Select Scanline Length
	CX =		Desired Width in Pixels
Output:	AX =		Status
	BX =		Bytes Per Scanline
	CX =		Actual Pixels Per Scanline
	DX =		Maximum Number of Scanlines
Input:	AH =	4fh	Super VGA Support
	AL =	06h	Logical Scanline Length
	BL =	01h	Return Scanline Length
Output:	AX =		Status
	BX =		Bytes Per Scanline
	CX =		Actual Pixels Per Scanline
	DX =		Maximum Number of Scanlines

NOTE: The desired width in pixels may not be achievable because of VGA hardware considerations. The next larger value will be selected that will accommodate the desired number of pixels, and the actual number of pixels will be returned in CX register. BX register returns a value that, when added to a pointer into video memory, will point to the next scanline. For example, in a Mode 13h this would be 320, but in Mode 12h this would be 80. DX register returns the number of logical scanlines based upon the new scanline length and the total memory installed and usable in this display mode. This function is also valid in text modes. In text modes, the application should determine the current character cell width through VESA Function 1 (or VGA BIOS Function 1BH), multiply that times the desired number of characters per line, and pass that value in the CX register.

4.9 Function 07h — Set/Get Display Start

This function selects the pixel to be displayed in the upper-left corner of the display from the logical page. This function can be used to pan and scroll around logical screens that are larger than the displayed screen. This function can also be used to rapidly switch between two different displayed screens for double-buffered animation effects.

Input:	AH =	4fh	Super VGA Support
	AL =	07h	Display Start Control
	BH =	00h	Reserved and must be a '0'
	BL =	00h	
	CX =		First Displayed Pixel In Scanline
	DX =		First Displayed Scanline
Output:	AX =	Status	
Input:	AH =	4fh	Super VGA Support
	AL =	07h	Display Start Control
	BL =	01h	Return Display Start
Output:	AX =		Status
	BH =		00h Reserved and will be a '0'
	CX =		First Displayed Pixel In Scanline
	DX =		First Displayed Scanline

NOTE: This function is also valid in text modes. In text modes, the application should find out the current character cell width through VESA Function 1 (or VGA BIOS Function 1BH), multiply that times the desired starting character column, and pass that value in the CX register. It should also multiply the current character cell height times the desired starting character row, and pass that value in the DX register.

4.10 Function 08h — Set/Get DAC Palette Control

This function queries and selects the operating mode of the DAC palette. Some DACs are configurable to provide 6 bits, 8 bits, or more of color definition per red, green, and blue primary color. The DAC palette width is assumed to be reset to standard VGA 6 bits per primary during a standard or VESA Set Super VGA mode (AX=4F02h) call.

Input:	AH=	4fh	Super VGA Support
	AL=	08h	Set/Get DAC Palette Control
	BL =	00h	Set DAC Palette Width
	BH=		Desired number of bits of color per primary (Standard VGA = 6)
Output:	AX=		Status
	BH=		Current number of bits of color per primary (Standard VGA = 6)
Input:	AH=	4fh	Super VGA Support
	AL=	08h	Set/Get DAC Palette Control
	BL =	01h	Get DAC Palette Width
Output:	AX=		Status
	BH=		Current number of bits of color per primary (Standard VGA = 6)

An application can determine if DAC switching is available by querying Bit D0 of the Capabilities field of the VgaInfoBlock structure returned by VESA Return Super VGA Information (AX=4F00h). The application can then attempt to set the DAC palette width to the desired value. If the Super VGA is not capable of selecting the requested palette width, then the next lower value that the Super VGA is capable of selecting. The resulting palette width is returned.

4.10.1 Function 10h — Display Power Management Extensions

The following three functions are defined by VESA as a proposal for VBE/PM which is a software interface to DPMS: Report Display Power Management Capabilities, Set Power State, and Get Power State. These functions are included to specify the Cirrus Logic implementation of display power management. For questions regarding VESA, VBE/PM, or DPMS, please refer to the Video Electronics Standards Association. The contact information is at the beginning of this section.

Report VBE/PM Capabilities

Input:	AH=	4fh Super VGA Support
	AL=	10f VBE/PM Services
	BL=	00h Report VBE/PM Capabilities
	ES:DI=	Null pointer, must be 0000:0000 in version 1.0
Output:	AX=	Status
	BH=	Power saving state signals support by the controller: 1 = supported, 0 = not supported bit 0 STAND BY bit 1 SUSPEND bit 2 OFF bit 3 REDUCED ON (not supported by DPMS 1.0) bit 4-7 reserved
	BL=	VBE/PM Version number bits 7:4 Major Version number bits 3:0 Minor Version number

Set Display Power State

Input:	AH=	4fh Super VGA Support
	AL=	10h VBE/PM Services
	BL=	01h Set Display Power State
	BH=	Requested Power State 00h ON 01h STAND BY 02h SUSPEND 04h OFF 08h REDUCED ON (not supported by DPMS 1.0)
Output:	AX=	Status
	BH=	Unchanged

Get Display Power State

Input:	AH=	4fh Super VGA Support
	AL=	10h VBE/PM Services
	BL=	02h Get Display Power State

Output:

AX=		Status
BH=		Display Power State
	00h	ON
	01h	STAND BY
	02h	SUSPEND
	04h	OFF
	08h	REDUCED ON (not supported by DPMS 1.0)
		bits 7:4 are reserved and should be ignored to ensure upward compatibility.

4.11 Function 15h — Display Identification Extensions

The VESA VBE sub-function 15h is used to implement the VBE/DDC services. The VBE/DDC services are defined below and are not included in the VBE Standard documentation. For questions regarding VESA, or VBE/DDC, please refer to the Video Electronics Standards Association. The contact information is at the beginning of this section.

Report VBE/DDC Capabilities

Input:

AH=	4fh	VESA Extension
AL=	15h	VBE/DDC Services
BL=	00h	Report DDC Capabilities
CX=	00h	Controller unit number (00 = primary controller)
ES:DI=	Null pointer, must be 0000:0000 in version 1.0	

Output:

AX=		Status
BH=		Approx time in seconds, rounded up, to transfer one EDID block (128 bytes)
BL=		DDC level supported by both the display and controller
	bit 0 = 0	DDC1 not supported
	bit 0 = 1	DDC1 supported
	bit 1 = 0	DDC2 not supported
	bit 1 = 1	DDC2 supported
	bit 2 = 0	Screen not blanked during data transfer
	bit 2 = 1	Screen blanked during data transfer (This refers to the behavior of the controller and software
CX=		Unchanged
ES:DI=		Unchanged

All other register contents may be destroyed

Read EDID

Input:

AH=	4fh	VESA Extension
AL=	15h	VBE/DDC Services
BL=	01h	Read EDID
CX=	00h	Controller Unit Number (00 = primary controller)
DX=	00h	EDID block number. Zero is the only valid value in version 1.0
ES:DI=		Pointer to area in which the EDID block (128 bytes) shall be returned

Output:

AX=	Status
BH=	Unchanged
CX=	Unchanged
ES:DI=	Pointer to area in which the EDID block is returned

All other register contents may be destroyed

NOTE: Sub-functions 02 (Read VDIF Block) is not supported.

Appendix F1

Glossary and Bibliography

Glossary

AccuPak™: A video compression method that is proprietary to Cirrus Logic, Inc. See Appendix B10.

Add-in Card, Adapter Card: A circuit board that plugs into a computer motherboard and connects it to some external device, such as a video monitor or storage subsystem.

A.N.: An acronym for Alpha Numeric. Only those patterns defined in the font tables can be displayed. Information can usually be displayed more quickly than is the case with A.P.A. images because fewer bits need to be manipulated by the software. These modes are also referred to as Text Modes.

A.P.A.: An acronym for All Points Addressable. Each pixel on the screen is individually programmable. Any pattern (subject to the resolution of the system) can be displayed. This typically requires that one to two orders of magnitude more information be manipulated than is the case with an A.N. system. These modes are also referred to as Graphics Modes. Nearly all extended modes are A.P.A.

Analog Interface: An interface between a video controller and a video display in which pixel colors are determined by the voltage levels on three output lines (RGB). Theoretically, an unlimited number of colors can be supported by this method (the maximum number anyone talks about is 16,777,216). The voltage level on any line varies between zero volts (for black) to about 700 millivolts (for maximum brightness). The lines are typically terminated in 75 ohms at the monitor end and 150 or 75 ohms at the graphics controller end. In the IBM world, the analog interface is usually mechanized with a 15-pin, 3-row connector (DB15).

Analog Monitor: A video monitor that uses an analog interface. In IBM terms, commonly known as a PS/2 monitor, or a VGA monitor when used in conjunction with a VGA controller. Many modern analog monitors have a switch allowing them to be used as a digital monitor.

Analog: A signal that can assume intermediate levels between on and off. Contrast with Digital.

ASCII: American Standard Code for Information Interchange. This is a 7-bit code used to encode alphanumeric information. In the IBM-compatible world, this is expanded to eight bits to encode a total of 256 alphanumeric (A.N.) and control characters.

AUTOEXEC.BAT: A file used to direct a series of activities that occur during system boot-up.

Auto-Monitor Detect: A feature of Cirrus Logic VGA controllers and BIOS that senses the type of monitor that is connected. This uses a scheme that involves the use of comparators to sense the terminations present on the RGB lines. This is being replaced with DDC1 and DDC2B.

BIOS-Level Compatibility: With regard to a VGA subsystem, this means that the BIOS supplied is in compliance with the IBM VGA standard. This is the minimum level of compatibility necessary to accommodate the majority of standard applications.

BIOS: An acronym for Basic Input Output System. In IBM-compatible personal computers, this is a set of ROM-based firmware routines that control the resources of the system and make them available to application programs in an orderly manner. These routines provide basic input/output services for the operating system and for applications programs that use interrupts to call them. Also called ROM BIOS. The Cirrus Logic BIOS is written in 80386/486 Assembly Language.

Bit: Binary Digit. A single piece of information: on or off, 0 or 1, high or low, closed or open, up or down, in or out, alive or dead, black or white.

BitBLT: An acronym for Bit Boundary Block Transfer. A type of graphics drawing routine that moves a rectangle of data from one area of Display Memory to another or moves data from System Memory to Display Memory. Graphics controllers frequently include varying degrees of hardware to help speed BitBLT operations.

Bitmap: A rectangular array of locations, each of which is associated with a location (pixel) on a monitor. The contents of each location determines the color of the pixel. Often times there are more locations in the bitmap than on the screen, allowing images to be maintained for later presentation.

Block Diagram: A diagram in which blocks are used to represent components or subsystems of a system. Usually the blocks are connected with lines indicating data or control flow.

Byte: A group of eight bits addressed as a unit. Can take any of 256 (2^8) values.

CAS: Column Address Strobe. One of the DRAM control signals.

CGA, Color Graphics Adapter: This was the first color adapter available for the IBM personal computer. It has low resolution, both spatial and color. While CGA is generally considered obsolete, the VGA standard includes the video modes originally designed for CGA.

Character Cell Matrix: In Text Mode, the area of display used to display one character. On the VGA, character cells are either 8, 9, 12, or 16 pixels wide and usually are either 8, 14, or 16 pixels high.

Character Clock: This clock is generated by dividing the VCLK by either eight or nine. The Monitor Timing Signals (HSYNC, VSYNC) are derived by dividing the character clock.

Color Key: The CL-GD543X has the capability of overlaying the computer-generated video, on a pixel-by-pixel basis, with external video. One method of determining whether to overlay a pixel involves comparing it with a specific color or range of colors.

Color Lookup Table (CLUT): Translates color information from the Display Memory into color information for the CRT display. It may be found in a Video DAC.

Color Modes: Uses two, four, eight, or more bits-per-pixel. The following table summarizes the number of colors and the standards for which the colors were first available.

Table F1-1. Color Modes

Bits per Pixel	Number of Colors	Standards
2	4	CGA
4	16	CGA
8	256	VGA
15	32,368	TARGA™
16	65,536	VGA/XGA™
24	16,777,216	Cirrus Logic True Color
32	16,777,216	True Color with Alpha Channel

Color Planes: In planar modes, the display memory is separated into four independent planes of memory, with each plane dedicated to controlling one color component (Red, Green, Blue, and Intensify). Each pixel of the display occupies one bit position in each plane. Planar modes are generally 16 colors. In character modes and packed pixel modes, the data is organized differently.

Comparator: A hardware element that is used to perform an arithmetic or logical comparison between two fields. The two fields are typically the same width. Arithmetic comparisons include equal, greater than, and less than. Logical comparisons are generally identity.

CONFIG.SYS: A file that provides the system with information regarding application requirements. This information may include peripherals that are connected and require special drivers (such as a mouse). Other information that might be specified is the number of files that may be open simultaneously, or the number of disk drives that may be accessed.

CMOS: Complementary Metal Oxide Semiconductor. A digital logic family that is characterized by high density, low-to-medium power, and medium-to-high speeds. All modern VGA controllers are fabricated using CMOS.

CPU, Central Processing Unit: The master computer unit in a system. In the VGA world, this is typically a 80386, 80486, or Pentium™ microprocessor.

CRT, Cathode Ray Tube: An electron beam is generated, accelerated, and made to strike a phosphor coating on the inside of an evacuated glass enclosure. The phosphor glows as a result of the energy imparted by the beam. By precisely controlling the position and intensity of the electron beam, meaningful patterns are made to appear in the phosphor and are visible through the glass.

DAC: An acronym for Digital to Analog Converter. The DACs in a VGA system convert the 6- or 8-digital bits-per-color (RED, GREEN, and BLUE) to analog levels suitable for the Analog Interface.

DCLK: The package pin on which the pixel clock (or a multiple or sub-multiple) is present. See also VCLK.

DDC™: Display Data Channel: A definition of a communication channel between a computer display and the host system. This is a VESA proposal. Cirrus Logic components and software support either DDC1 or DDC2B.

Digital Interface: A type of interface used between video controller and video display in which display color is controlled by digital color control lines switching on and off. The number of colors that can be supported depends on the number of signal lines in the interface, and is generally either 8, 16, or 64. Most digital interfaces are TTL- (Transistor-Transistor Logic) compatible. CGA, MDA, and EGA use digital interfaces. In the IBM world, the digital interface is usually mechanized with a 9-pin connector.

Digital Monitor (TTL): A monitor that receives its input in the form of a digital code. Typical digital monitors can display 8, 16, or 64 colors. Digital monitors are more or less obsolete.

Digital: A method of representing data whereby the individual components are either fully on or fully off.

Digitize: To convert an analog image or signal to a corresponding series of numbers.

Display Memory: The area in the computer memory where the information used to update the screen is kept. In the IBM-compatible world, the range of addresses for this data is A000:0 through BFFF:F.

Display Modes: In the IBM-compatible world, a number of standard display modes have been defined. Video Mode is used interchangeably with Display Mode. In addition to the standard modes enumerated below, there are many Extended Display modes.

Table F1-2. Standard Display Modes

Mode(s)	Colors	Alphanumeric Resolution	Pixel Resolution	A.N./ A.P.A
0,1	16	40 × 25	360 × 400	A.N.
2,3	16	80 × 25	720 × 400	A.N.
4,5	4	40 x25	320 × 200	A.P.A.
6	2	80 × 25	640 × 200	A.P.A.
7	Mono.	80 × 25	720 × 400	A.N.
D	16	40 × 25	320 × 200	A.P.A.
E	16	80 × 25	640 × 200	A.P.A.
F	Mono.	80 × 25	640 × 250	A.P.A.
10	16	80 × 25	640 × 350	A.P.A.
11	2	80 × 30	640 × 480	A.P.A.
12	16	80 × 30	640 × 480	A.P.A.
13	256	40 × 25	320 × 200	A.P.A.

Dithering: To intersperse a pattern of one color (for example, blue) with a pattern of another color (for example, red) to give the subjective effect of a color somewhere between the two colors (blue and red together make magenta). This technique is effective over large surfaces but fails if the area is too small. This technique creates the appearance of more colors at the expense of resolution.

DIP: Dual Inline Package. A method of packaging semiconductor chips that was essentially ubiquitous until the 1980s. It is being replaced with plastic quad flatpack and pin grid arrays for devices with high pin counts, and small outline packages for devices with low or medium pin counts.

DPMS: Display Power Management Signaling: A proposal to standardize on a common definition and methodology in which the display controller sends a signal to the display that enables it to enter various power management states. This is a VESA proposal. The VGA controller can instruct the monitor go enter one of a number of reduced power states. DPMS is supported by current Cirrus Logic desktop products.

DRAM: Dynamic Random Access Memory. A memory technology that is characterized by extreme high density, low power, and low cost. It must be more or less continuously refreshed to avoid loss of data.

Driver: A software module that interfaces a particular display device to an application program to allow operation at higher resolutions than standard VGA.

Dual-Page Mapping: Refers to using both Offset Registers, 0 and 1, as the window into Display Memory. This mode is chosen when GRB[0] is programmed to a '1'. In this mode, SA15 is used to choose between Offset Registers 0 and 1.

EDO: Extended Data Out: A DRAM technology that is characterized by very short Fast Page Mode cycle times. Members of the CL-GD543X/'4X family, beginning in late 1994, are expected to have support for EDO devices.

EEPROM, Electrically Erasable Programmable Read-only Memory: A memory storage device that can be written repeatedly with no special erasure fixture. EEPROMs do not lose their contents when they are powered down. The Cirrus Logic BIOS can use EEPROMs to record information regarding the connected monitor. This is being replaced with DDC.

EGA: Enhanced Graphics Adapter. This was the second color adapter available for IBM-compatible computers. While EGA is generally considered obsolete, the VGA standard includes the modes originally designed for EGA.

Emulation: Simulation of unavailable hardware by available hardware and software. Emulations improve the usefulness of a product by making it compatible with other products. EGA is capable of emulating MDA and sometimes CGA and Hercules. VGA is capable of emulating EGA, CGA, and MDA.

EPROM: Electrically Programmable Read-only Memory: A memory storage device that can be written once (per erasure cycle) and read many times. In the VGA world, it is used for holding the BIOS.

Fast-Page Mode: A read or write mode of DRAMs that is characterized by a decrease in cycle time of about 2–3 times and a corresponding increase in performance. The data accessed in Fast-Page Mode cycles must be adjacent in memory.

Feature Connector: An expansion connector on the VGA that can be used to accept or drive video signals to or from the VGA. This is used in applications involving video overlay. This is also called the VESA Pass-through connector.

FIFO: First In First Out. A memory that can temporarily hold data so that the sending device can send data faster than the receiving device can accept it. The sending and receiving devices typically operate asynchronously.

Fixed-Frequency Monitor: A monitor that can accept a fixed horizontal frequency, usually 31.5 kHz. Such monitors can accommodate different vertical resolutions by operating at different vertical frequencies, usually either 60 or 70 Hz.

Frequency Synthesizer: An electronic circuit that can generate a number of frequencies from a fixed reference frequency. Some frequency synthesizers can generate only a relatively small number of frequencies; others can generate hundreds of different frequencies.

Glue Logic: Additional logic devices required to interconnect the major components of a system.

Graphics Controller: On EGA and VGA, a section of circuitry that can provide hardware assist for graphics drawing algorithms by performing logical functions on data written to Display Memory.

Graphics Mode: (Also A.P.A.) A display mode in which all pixels on the display screen can be controlled independently to draw graphics objects (as opposed to Text mode, in which only a pre-defined set of characters can be displayed).

Hardware: A computing system is normally spoken of as having two major components: hardware and software. Hardware is the portion that executes the step-by-step procedure necessary to perform a particular task as instructed by the software.

HERC, Hercules Graphics Adapter (HGC): The third display format standardized for the PC family of computers, following the MDA and CGA. It provides standard 80-character-by-25-row alphanumeric display, and 720 horizontal by 348 vertical pixels in Monochrome Graphics Mode. It was designed as a replacement for MDA, and provided monochrome A.P.A.

Hex Code, Hexadecimal: A numbering system using base 16. The allowable digits are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F. A base 16 numbering system is useful because conversion to and from base 2 is trivial. Numbers written in base 16 are typically denoted by a prepended '0x' or an appended 'h'.

Interlaced: A graphics system in which the even scanlines are refreshed in one vertical cycle (field), and the odd scanlines are refreshed in another vertical cycle. The advantage is that the video bandwidth is roughly half that required for a non-interlaced system of the same resolution. This results in less costly hardware. It also may make it possible to display a resolution that would otherwise be impossible on given hardware. The disadvantage of an interlaced system is flicker, especially when displaying objects that are only a single scan line high.

ISA: Industry Standard Architecture. In reference to IBM-compatible computers, it was the definition of the standard bus until the introduction of VESA and PCI in the early 1990s.

Mapping: Mapping refers to the definition of memory for storing data used by a particular Video Mode. The range of addresses reserved for video information in IBM-compatible systems is from A000:0 to BFFF:F.

MCGA, Multicolor Graphics Array: A graphics adapter designed for the PS/2 series of personal computers, with similar function to the CGA and downwardly compatible to the CGA at the BIOS, control register, and Display Memory levels. Like the VGA, the MCGA drives either an analog monochrome or analog RGB monitor.

MDA, Monochrome Display Adapter: The original display adapter marketed by IBM for personal computers. MDA has no bit-mapped graphics capability.

Monitor: Another term for a CRT Display.

Monochrome Modes: Uses one bit per pixel. 'Two-color' modes are similar to monochrome modes because they can display two colors; the two colors do not need to be black and white, sometimes they are amber or green with black.

Motherboard: The large printed circuit board in a personal computer into which the adapter boards plug. It contains the CPU and core memory. It may also contain the video controller or a number of other peripheral controllers.

Multiple-FIFO Architecture: A video controller architecture that is characterized by having multiple (two or more) FIFOs or Write Buffers. There is typically one FIFO or Write Buffer at the CPU interface and one or more FIFOs in the screen refresh stream.

Multifrequency Monitor: A monitor that will accommodate a variety of horizontal and vertical synchronization frequencies. This type of monitor accepts inputs from many different video display adapters, and is typically capable of either analog or digital input.

Nibble: A group of four bits, typically contiguous. It can take any of 16 (2^4) values.

Non-interlaced: A video system in which every pixel is refreshed during every vertical scan. A non-interlaced system is normally more expensive than an interlaced system of the same resolution, and is usually said to have a more pleasing appearance.

NTSC: A color encoding scheme used for television. NTSC is used in North America and Japan, as well as some other areas. NTSC is often spoken of as a timing standard; it is an extension of RS-170.

Overlay: The superimposition of video (typically live) onto computer generated graphics.

Overscan: That portion on all four sides of the display between active video and blanking.

Packed Pixel: Color information for a pixel packed into one word of memory data. For a system with few colors, this packed pixel may require only a part of one word of memory; for very elaborate systems, a packed pixel might be several words long. See **Planar**.

PAL: A color encoding scheme used for television. PAL is used in Europe (except France), as well as some other places.

Palette: The range of colors available on the screen, not necessarily simultaneously. For VGA, this is either 16 or 256 simultaneous colors out of 262,144. For CL-GD543X, the palette is extended to 32,768, 65,536, or 16,777,216 simultaneous colors on the screen.

Palette DAC: The triple eight-bit DAC with its associated Lookup Table.

Pixel: An acronym for picture element, and is also called a pel. A pixel is the smallest addressable graphic on a display screen. In RGB systems, the color of a pixel is defined by some Red intensity, some Green intensity, and some Blue intensity.

Planar: In video terms, the pixel color information is stored in four bits across four memory planes. This allows a maximum of 16 colors (2^4). See **Packed Pixel**.

RAM BIOS: The BIOS can be copied from relatively slow ROM into relatively fast RAM. When this is done, it will execute faster, enhancing performance of the subsystem being controlled.

RAM, Random Access Memory: This term has come to mean any semiconductor memory whose write access time is approximately the same as its read access time. This is typically taken to include SRAMs (Static RAMs) and DRAMs (Dynamic RAMs). This definition specifically eliminates memories that cannot be altered at all and memories that require a special fixture for erasing (such as EPROMs).

RAS: Row Address Strobe. A DRAM control signal.

Refresh (Display or Screen Refresh): An image drawn on a CRT display will remain visible only for a few milliseconds (the persistence of the screen phosphor), unless it is redrawn continuously. This process is called display refresh or screen refresh. Different displays use different refresh rates, but display refresh is normally required between 60 and 80 times a second to avoid any visible screen flickering. 75 times a second is a common refresh rate. In general, a higher refresh rate results in more stable appearing display.

Register-Level Compatibility: If a peripheral is compatible at the register level with another peripheral, it means that every bit in every register of the two devices has precisely the same meaning. This implies that application programs can circumvent the BIOS and directly program registers in a peripheral device without functionality problems. The CL-GD543X is register-level-compatible with the IBM VGA standard.

Registers: In a VGA controller, these are the storage elements that contain data relating to the mode or configuration of the device, as opposed to the Display Memory that contains the image. Traditionally, the registers are divided into six groups: General, Sequencer, CRT Controller, Graphics Controllers, Attribute, and Extensions. The VGA registers are accessed by a number of addressing schemes, each involving an index or address register and a data register.

Resolution, Color: The number of simultaneous colors is determined by the number of bits associated with each pixel in the Display Memory. The more colors, the more bits. If n bits-per-pixel are used, 2^n color combinations can be generated. EGA uses from one to four bits-per-pixel, permitting up to 16 (2^4) colors to be displayed on the screen at the same time. The VGA has an added mode that supports eight bits-per-pixel, or 256 (2^8) simultaneous colors. The CL-GD543X has additional modes that support up to 24 bits-per-pixel or 16,777,216 (2^{24}) simultaneous colors. In addition, some modes use a fourth byte, the alpha byte.

Resolution, Spatial: The number of pixels in an area or on the screen. Resolution is typically specified as pixels per scanline and scanlines per frame. Higher resolution images require more processing and greater storage requirements per image. In addition, monitor costs increase with resolution, particularly above about one million pixels. Different applications require different resolutions.

RGB: Used with color displays, an interface that uses three color signals (Red, Green, and Blue), as opposed to an interface used with a monochrome display that requires only a single signal. Both digital and analog RGB interfaces exist.

ROM, Read-only Memory: A type of memory that is characterized by not being alterable (see EPROM). ROMs are typically used to contain low-level programs that do not change, such as BIOS.

Simultaneous Colors: The number of colors in a display system that can be displayed on the screen at one time. This number is limited by the circuitry of the display adapter, and is often much smaller than the number of colors the display device can actually support. The number of simultaneous colors a display adapter will support is normally determined by the number of color planes, or bits per pixel, that it uses. For example, a device with four bits-per-pixel will support 16 simultaneous colors.

Single-Page Mapping: Refers to always using Offset Register 0 (GR9) as the window into Display Memory. The mode is chosen when GRB[0] is programmed to a '0'.

Sleep Mode: A VGA controller can be put to 'sleep' by writing a value to a particular bit of a particular register. The register is normally at address 3C3 or 46E8 in the IBM-compatible world. When a VGA controller is asleep, it will respond to no further commands except a command to wake up or a BIOS read. This allows two VGA controllers to share common addresses, so long as their sleep addresses and BIOS addresses are not the same. PCI uses a different sleep mechanism than do ISA and VESA VL.

Software: A computing system is normally spoken of as having two major components: hardware and software. Software is that portion that instructs the hardware in the step-by-step procedure necessary to perform a particular task.

Super VGA: Graphics adapters that extend the capabilities of the features provided by the original IBM VGA. The first Super VGA provided a 640 x 480 x 256-Color Mode. Also SVGA.

Surface Mount Technology (SMT): A method of mounting devices (such as integrated circuits, resistors, capacitors, and others) on a printed circuit board, characterized by not requiring mounting holes. Rather, the devices are soldered to pads on the printed circuit board. Surface-mount devices are typically smaller than the equivalent through-hole devices.

TTL, Transistor-Transistor Logic: A collection of logic families developed beginning in the 1960s. TTL is gradually being replaced with CMOS for all but the fastest or most cost-sensitive applications.

True-color: 24-or 32-bits-per-pixel color providing photo-realistic image quality.

VCLK: The internal signal operating at the pixel rate.

Vertical Retrace: The time interval immediately following the completion of a complete frame (or field for an interlaced display). The electron beam returns to the top of the display screen in preparation for the next frame or field during this period.

VESA, Video Electronics Standards Association: A consortium of CRT monitor vendors, graphics chip vendors, and graphics software vendors that set hardware and software standards for PC-compatible graphics monitors and software interfaces. Cirrus Logic is an active participant on many of the VESA committees.

VGA, Video Graphics Array: The VGA standard was introduced by IBM in 1987. In the IBM definition, the maximum spatial resolution is 640 x 480 (Modes 11 and 12), and the maximum color resolution is 256 colors (Mode 13). This has been enhanced or extended by third party chip vendors to up to 1280 x 1024 and up to 16,777,216 colors.

VLSI, Very Large Scale Integration: The technology of manufacturing integrated circuits (chips) with thousands of transistors on a single device. The personal computer was made possible because of VLSI technology.

VRAM, Video (Dynamic) Random Access Memory: Memory chips with two ports, one used for random accesses and the other capable of serial accesses. Once the serial port has been initialized (with a transfer cycle), it can operate independently of the random port. This frees the random port for CPU accesses. The result of adding the serial port is a significantly reduced amount of interference from screen refresh. VRAMs cost more per bit than DRAMs.

Wait State: When a system processor is reading or writing a memory or peripheral device that cannot respond fast enough, one or more time intervals (typically on the order of tens of nanoseconds each) are inserted during which the processor does nothing but wait for the slower device. While this has a detrimental effect on system throughput, it is unavoidable. The number of wait states can be reduced using techniques such as CPU-bus caches or write FIFOs.

Word: The amount of memory that a given computer can access in a single cycle. In the IBM-compatible world, this is either 16 or 32 bits.

Write Buffer: A term used in the CL-GD543X literature to denote the buffer that is logically positioned between the CPU interface and the Display Memory.

YCrCb: A color space defined in CCIR601.

YUV: A color space generally associated with color television.

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W–Z

ASCII Character Set: 00-7f

Char	0x	1x	2x	3x	4x	5x	6x	7x
0	NUL	DLE	space	0	@	P	´	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	`	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
a	LF	SUB	*	:	J	Z	j	z
b	VT	ESC	+	;	K	[	k	{
c	FF	FS	,	<	L	\	l	|
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