- **Glueless Interface Between the Peripheral Component Interconnect (PCI) Bus and the TI380C2x† and TI380C3x† Generation of Processors**
- **Compliant With PCI Specification, Revision 2.0‡§**
- **Allows Use of Existing TI2000 Drivers**
- **Includes TI2000 Interface Configuration Register**
- **Supports Bus Master Operations for High Performance**
- **Provides 32-Bit Address-Data Path**
- **Implements Address/Data Parity Checking**
- **Includes Internal Error Checking for Illegal Bus Operations**
- **Supports Direct Memory Access (DMA) Bursts With 64-Byte FIFO**
- **Supports EPROM Interface for Remote Program Load (RPL) Operation**
- **Supports Inter-Integrated Circuit (I^2C) Interface for Optional Serial EEPROM for Configuration Information**
- **Allows Burned-In Address (BIA) to be Implemented in Configuration EEPROM**
- **Includes NAND Tree Structure to Allow for In-Circuit Connectivity Testing**
- **144-Pin JEDEC Plastic Quad Flat Package (PCM Suffix)**
- **Operating Temperature Range 0°C to 70°C**

description

The TI380PCIA provides a glueless interface between a TI380C2x† commprocessor and the PCI bus (see Figure 1). The TI380PCIA transfers information/data between the PCI bus and the TI380C2x† system interface (SIF) using any of these three methods:

- Direct memory access (DMA)
- Direct input/output (DIO)
- Pseudo-direct memory access (PDMA)

DMA (or PDMA) transfers all data between host memory (by way of the PCI local bus) and TI380C2x† local memory. DIO accesses are typically used to load software into TI380C2x† local memory and for initializing the TI380C2x†.

The TI380PCIA conforms to the PCI standards found in “PCI Local Bus Specification,” Revision 2.0.‡§

The TI380PCIA is available in a 144-pin JEDEC plastic quad flat package (PCM suffix) and is rated from 0°C to 70°C. It is a drop-in replacement for the TI380PCI.

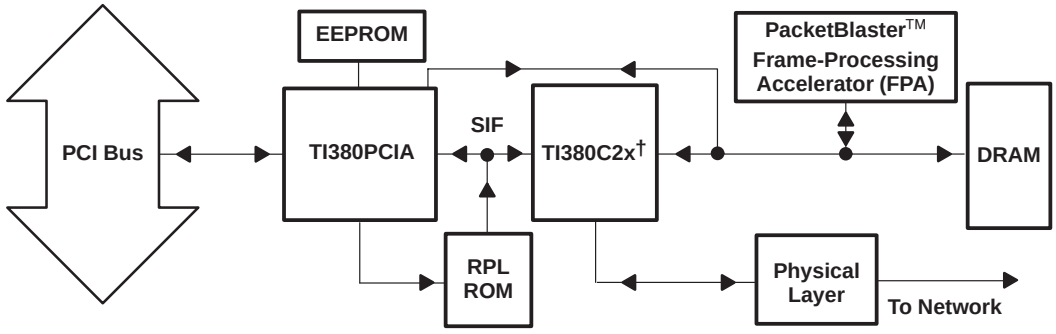

Figure 1. TI380PCIA Applications Diagram

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† TI380C3x devices can be used with TI380PCIA in the same way as TI380C2x devices.
‡ The “PCI Local Bus Specification”, Revision 2.0, and the TI380C2x or TI380C3x series of data sheets (e.g., literature number SPWS012) should be used as references to this document.
§ Exceptions to electrical timing parameters specified in PCI Specification Revision 2.0 are described in Note 8 and Note 10 of the timing requirements section of this document.

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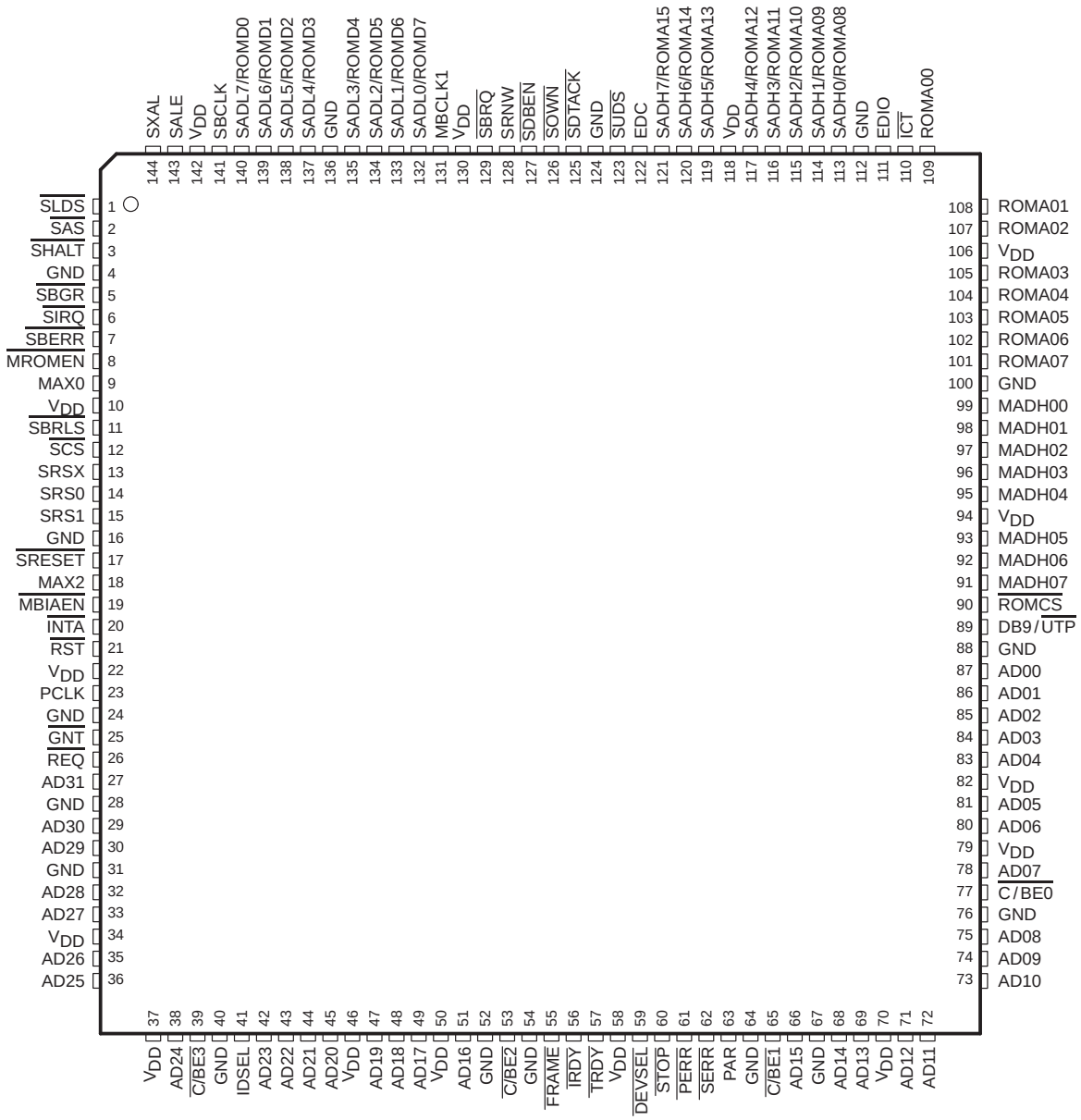
pin assignments

The pin assignments for the TI380PCIA (144-pin plastic quad flat package) are shown below.

PCM PACKAGE
(TOP VIEW)

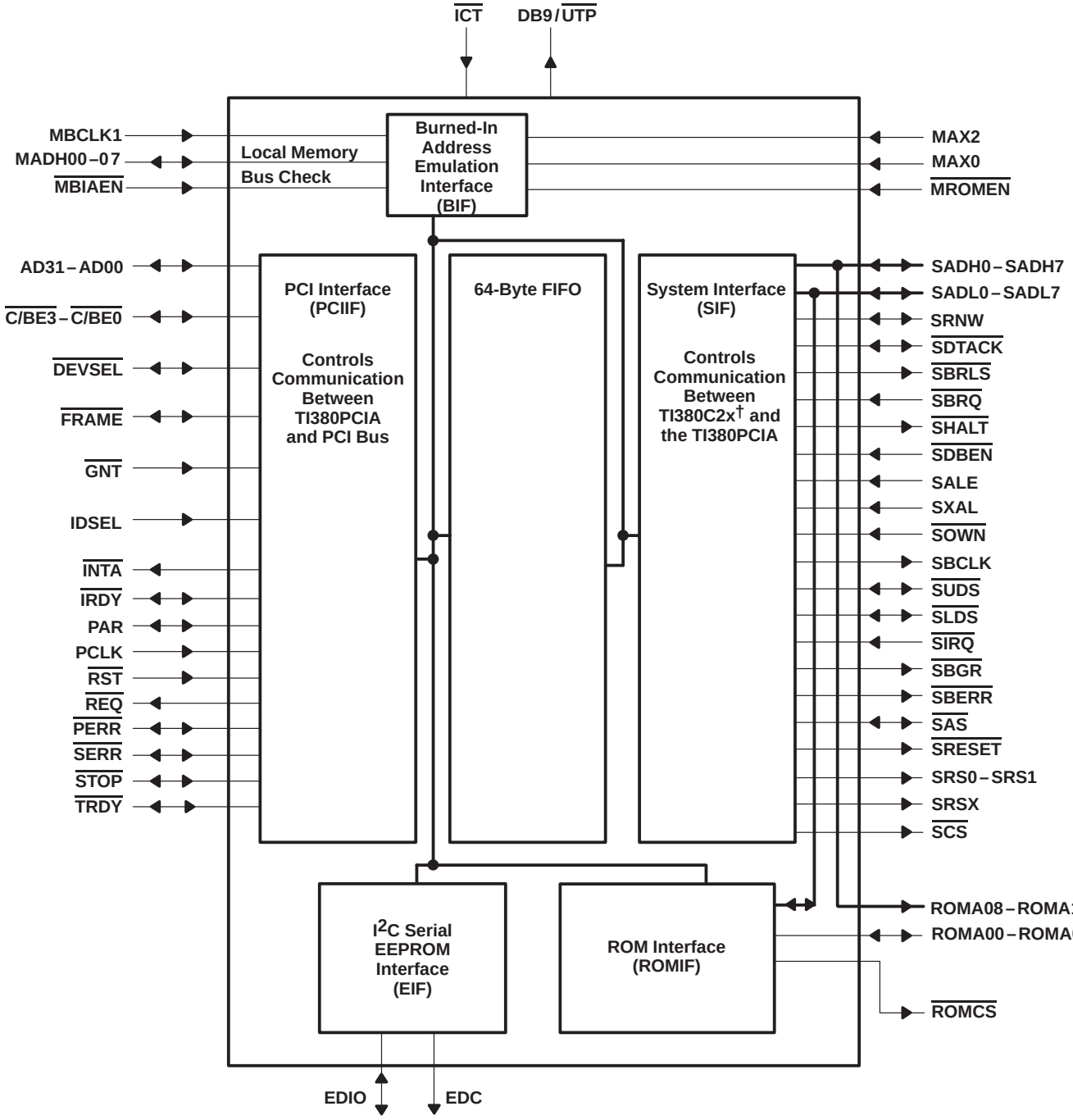


NOTE: Pin 1 is positioned at the upper left corner.

ADVANCE INFORMATION

block diagram

TI380PCIA can connect to up to four devices in a system: the PCI bus, the SIF bus, an optional serial EEPROM, and an optional boot ROM. The major blocks of the TI380PCIA include the PCI Interface (PCIIF), SIF, and ROM Interface (ROMIF) as shown in Figure 2.



† TI380C3x devices can be used with TI380PCIA in the same way as TI380C2x devices.

Figure 2. TI380PCIA Block Diagram

ADVANCE INFORMATION

ADVANCE INFORMATION

Terminal Functions

TERMINAL NAME	NO.	I/O†	DESCRIPTION
DB9/$\overline{\text{UTP}}$	89	O	Connector. The value on DB9/$\overline{\text{UTP}}$ indicates the type of connector in use. Upon reset, the DB9/$\overline{\text{UTP}}$ value is 0. 1 = D-Shell (DB9) 0 = UTP/10BaseT
GND	4 16 24 28 31 40 52 54 64 67 76 88 100 112 124 136	I	Ground. These pins must be attached to the common system ground plane.
$\overline{\text{ICT}}$	110	I	$\overline{\text{ICT}}$ supports in-circuit tests. $\overline{\text{ICT}}$ must be pulled high for normal operation of the TI380PCIA. When pulled along with $\overline{\text{RST}}$ to a steady low state, all bidirectional signals in the TI380PCIA are configured as inputs, and all output pins of the TI380PCIA are in 3-state mode.
ROMA07 ROMA06 ROMA05 ROMA04 ROMA03 ROMA02 ROMA01 ROMA00	101 102 103 104 105 107 108 109	I/O	ROM address. ROMA07 – ROMA00 form the least significant eight bits of the address for the RPL ROM. The most significant bits (MSBs) of the ROM address are multiplexed onto the SADHx lines. When $\overline{\text{RST}}$ is driven high, the value on ROMA07 – ROMA00 is latched into the board configuration register in the TI380PCIA configuration space. The value on ROMA07 – ROMA00 can be provided by pullup and pulldown resistors that do not affect operation after reset. This feature allows designers to support jumpers or board stuffing options that can be sensed by software that reads the board configuration register. If pullup and pulldown resistors are not used, the contents of the board configuration register are undefined after reset.
$\overline{\text{ROMCS}}$	90	O	$\overline{\text{ROMCS}}$ enables the outputs of the ROM when the ROM has been accessed. $\overline{\text{ROMCS}}$-enable allows the data lines from the ROM to be driven.

† I = in, O = out

‡ The TI380PCIA SIF pin names correspond to a subset of the system interface pins on a TI380C2x§. See the TI380C2x§ data sheets for more information on individual pins. Like-named pins on the TI380PCIA and TI380C2x§ system interfaces are intended to be connected to each other.

§ TI380C3x devices can be used with TI380PCIA in the same way as TI380C2x devices.

¶ Typical bit-ordering for Intel™ and Motorola™ processor buses

The signal connecting this pin to the TI380C2x§ also should be connected to a 4.7-kΩ pullup resistor.

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NOTE 1: The TI380PCIA allows driver software to set SBCLK output to a steady high state. This signal is driven to a steady high state during power-down operations.

Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O†	DESCRIPTION
V_{DD}	10 22 34 37 46 50 58 70 79 82 94 106 118 130 142	I	5-V supply. These pins must be attached to the common system power supply plane.
SYSTEM INTERFACE (SIF)‡			
SADH0/ROMA08 SADH1/ROMA09 SADH2/ROMA10 SADH3/ROMA11 SADH4/ROMA12 SADH5/ROMA13 SADH6/ROMA14 SADH7/ROMA15	113 114 115 116 117 119 120 121	I/O	System address/data bus—high byte. These lines make up the most significant byte (MSByte) of each TI380C2x§ address word (32-bit address bus) and data word (16-bit data bus). The most significant bit (MSB) is SADH0, and the least significant bit (LSB) is SADH7. Address-multiplexing bits 31–24 and bits 15–8¶ Data-multiplexing bits 15–8¶ During accesses to the ROM address space from the PCI bus, these lines provide the eight most significant address bits to the ROM.
SADL0/ROMD7 SADL1/ROMD6 SADL2/ROMD5 SADL3/ROMD4 SADL4/ROMD3 SADL5/ROMD2 SADL6/ROMD1 SADL7/ROMD0	132 133 134 135 137 138 139 140	I/O	System address/data bus—low byte. These lines make up the least significant byte (LSByte) of each address word (32-bit address bus) and data word (16-bit data bus). The MSB is SADL0, and the LSB is SADL7. These address lines also make up the ROM address. Address-multiplexing bits 23–16 and bits 7–0¶ Data-multiplexing bits 7–0¶ During accesses to the ROM address space from the PCI bus, these lines transfer data from the ROM to the TI380PCIA.
SALE	143	I	System-address latch-enable. SALE is the enable pulse used to latch the 16 LSBs of the address externally from the SADH0–SADH7 and SADL0–SADL7 buses at the start of the DMA cycle.
$\overline{SAS}$	2	I/O	System-memory address strobe. $\overline{SAS}$ is an active-low address strobe that is an output during DIO and an input during DMA.# H = Address not valid L = Address is valid and a transfer operation is in progress
SBCLK	141	O	SIF bus clock. The TI380C2x§ requires SBCLK to synchronize its bus timings for all DMA transfers (see Note 1).

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‡ The TI380PCIA SIF pin names correspond to a subset of the system interface pins on a TI380C2x§. See the TI380C2x§ data sheets for more information on individual pins. Like-named pins on the TI380PCIA and TI380C2x§ system interfaces are intended to be connected to each other.

§ TI380C3x devices can be used with TI380PCIA in the same way as TI380C2x devices.

¶ Typical bit-ordering for Intel™ and Motorola™ processor buses

The signal connecting this pin to the TI380C2x§ also should be connected to a 4.7-kΩ pullup resistor.

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NOTE 1: The TI380PCIA allows driver software to set SBCLK output to a steady high state. This signal is driven to a steady high state during power-down operations.

ADVANCE INFORMATION

Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O†	DESCRIPTION
SYSTEM INTERFACE (SIF)‡ (CONTINUED)			
$\overline{\text{SBERR}}$	7	O	Bus error. $\overline{\text{SBERR}}$ corresponds to the bus error signal of the 68000 microprocessor. $\overline{\text{SBERR}}$ is driven low during a DMA cycle to indicate to the TI380C2x§ that the cycle must be terminated. See Section 3.4.5.3 of the *TMS380 Second-Generation Token Ring User's Guide* (SPWU005) for more information.
$\overline{\text{SBGR}}$	5	O	System-bus grant. $\overline{\text{SBGR}}$ serves as an active-low bus grant, as defined in the standard 68000 interface. H = System bus not granted L = System bus granted
$\overline{\text{SBRLS}}$	11	O	SIF bus release. $\overline{\text{SBRLS}}$ indicates to the TI380C2x§ that a higher-priority device requires the SIF bus. The value on $\overline{\text{SBRLS}}$ is ignored by the TI380C2x§ when DMA is not performed. H = The TI380C2x§ can hold onto the system bus. L = The TI380C2x§ should release the system bus upon completion of current DMA cycle. If the DMA transfer is not yet complete, the SIF rearbitrates for the SIF bus.
$\overline{\text{SBRQ}}$	129	I	System-bus request. $\overline{\text{SBRQ}}$ is used to request control of the system bus in preparation for a DMA transfer. $\overline{\text{SBRQ}}$ is internally synchronized to SBCLK. H = System bus not requested L = System bus requested
$\overline{\text{SCS}}$	12	O	System chip select. $\overline{\text{SCS}}$ activates the system interface of the TI380C2x§ for a DIO read or write. H = Not selected L = Selected
$\overline{\text{SDBEN}}$	127	I	System data-bus enable. $\overline{\text{SDBEN}}$ causes the TI380PCIA to allow its external data buffers to begin driving data. $\overline{\text{SDBEN}}$ is accepted during both DIO and DMA. H = Keep external data buffers in high-impedance state L = Cause external data buffers to begin driving data
$\overline{\text{SDTACK}}$	125	I/O	System data-transfer acknowledge. The purpose of $\overline{\text{SDTACK}}$ is to indicate to the bus master that a data transfer is complete. $\overline{\text{SDTACK}}$ is internally synchronized to SBCLK by the TI380C2x§. During DMA cycles, it is asserted before the falling edge of SBCLK in state T2 by the TI380PCIA to prevent a wait state. $\overline{\text{SDTACK}}$ is an input when the TI380C2x§ is selected for DIO, and an output otherwise.# H = System bus NOT ready L = Data transfer is complete; system bus is ready.
$\overline{\text{SHALT}}$	3	O	System halt/bus error retry. If $\overline{\text{SHALT}}$ is asserted along with bus error ($\overline{\text{SBERR}}$), the adapter retries the last DMA cycle. This is the rerun operation as defined in the 68000 specification. See Section 3.4.5.3 of the *TMS380 Second-Generation Token Ring User's Guide* (SPWU005) for more information.
$\overline{\text{SIRQ}}$	6	I	System interrupt request. TI380C2x§ drives $\overline{\text{SIRQ}}$ to signal an interrupt request to the host processor. H = No interrupt request L = Interrupt request by TI380C2x§

† I = in, O = out

‡ The TI380PCIA SIF pin names correspond to a subset of the system interface pins on a TI380C2x§. See the TI380C2x§ data sheets for more information on individual pins. Like-named pins on the TI380PCIA and TI380C2x§ system interfaces are intended to be connected to each other.

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¶ Typical bit-ordering for Intel™ and Motorola™ processor buses

The signal connecting this pin to the TI380C2x§ also should be connected to a 4.7-kΩ pullup resistor.

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Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O†	DESCRIPTION
SYSTEM INTERFACE (SIF)‡ (CONTINUED)			
$\overline{\text{SLDS}}$	1	I/O	Lower data strobe. $\overline{\text{SLDS}}$ is an output during DIO and an input during DMA. $\overline{\text{SLDS}}$ serves as the active-low lower data strobe.# H = Not valid data on SADL0–SADL7 lines L = Valid data on SADL0–SADL7 lines
$\overline{\text{SOWN}}$	126	I	SIF bus owned. $\overline{\text{SOWN}}$ signals the TI380PCIA SIF logic to indicate that the TI380C2x§ has control of the SIF bus. L = TI380PCIA does not have control of the SIF bus. H = TI380PCIA has control of the SIF bus.
$\overline{\text{SRESET}}$	17	O	System reset. $\overline{\text{SRESET}}$ is sent to initialize the TI380C2x§. It is set low whenever $\overline{\text{RST}}$ goes low or by a configuration write to the MISCCTRL register. H = No system reset L = System reset
SRNW	128	I/O	System read not write. SRNW serves as a control signal to indicate a read or write cycle. H = Read Cycle L = Write Cycle
SRSX SRS0 SRS1	13 14 15	O	System register select. These outputs are sent to select the word or byte to be transferred during a system DIO access. The most significant bit is SRSX and the least significant bit is SRS1. MSB LSB Registers selected = SRSX SRS0 SRS1
$\overline{\text{SUDS}}$	123	I/O	Upper data strobe. $\overline{\text{SUDS}}$ serves as the active-low upper data strobe. $\overline{\text{SUDS}}$ is an output during DIO and an input during DMA.# H = Not valid data on SADH0–SADH7 lines L = Valid data on SADH0–SADH7 lines
SXAL	144	I	System extended address latch. SXAL provides the enable pulse that externally latches the most significant 16 bits of the 32-bit system address during DMA. SXAL is activated by the TI380C2x§ prior to the first cycle of each block DMA transfer, and thereafter as necessary (whenever an increment of the DMA address counter causes a carryout of the lower 16 bits).

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¶ Typical bit-ordering for Intel™ and Motorola™ processor buses

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ADVANCE INFORMATION

ADVANCE INFORMATION

Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O†	DESCRIPTION
BURNED-IN ADDRESS EMULATION INTERFACE (BIF)‖			
MBCLK1	131	I	Local memory bus clock 1.
MADH00 MADH01 MADH02 MADH03 MADH04 MADH05 MADH06 MADH07	99 98 97 96 95 93 92 91	I/O	Local memory address, data, and status bus — high byte. For the first quarter of the local memory cycle, MADH00 – MADH07 monitor address bits AX4 and A0 to A6; for the second quarter, they monitor status bits, and for the third and fourth quarters, they carry data bits 0 to 7. The most significant bit is MADH00, and the least significant bit is MADH07.
$\overline{\text{MBIAEN}}$	19	I	Burned-in address enable. $\overline{\text{MBIAEN}}$ enables the output of data on the MADHxx lines during BIA accesses.
MAX2	18	I	Local memory extended address bit. For the first quarter of a local memory cycle MAX2 monitors AX2. For quarters two through four, MAX2 monitors A14.
MAX0	9	I	Local memory extended address bit. For the first quarter of a local memory cycle MAX0 monitors AX0. For quarters two through four, MAX0 monitors A12.
$\overline{\text{MROMEN}}$	8	I	$\overline{\text{MROMEN}}$ monitors the local memory bus ROM enable signal.

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¶ Typical bit-ordering for Intel™ and Motorola™ processor buses
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Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O†	DESCRIPTION
PCI INTERFACE			
AD31	27	I/O	PCI address and data. A bus transaction to or from one of these pins consists of an address phase followed by one or more data phases. The address phase is the clock cycle in which $\overline{\text{FRAME}}$ is asserted. During the address phase, AD31–AD00 contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases, AD07–AD00 contain the LSB, and AD31–AD24 contain the MSB. Write data is stable and valid when $\overline{\text{IRDY}}$ is asserted, and read data is stable and valid when $\overline{\text{TRDY}}$ is asserted. Data is transferred during those clocks where both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted.
AD30	29		
AD29	30		
AD28	32		
AD27	33		
AD26	35		
AD25	36		
AD24	38		
AD23	42		
AD22	43		
AD21	44		
AD20	45		
AD19	47		
AD18	48		
AD17	49		
AD16	51		
AD15	66		
AD14	68		
AD13	69		
AD12	71		
AD11	72		
AD10	73		
AD09	74		
AD08	75		
AD07	78		
AD06	80		
AD05	81		
AD04	83		
AD03	84		
AD02	85		
AD01	86		
AD00	87		
$\overline{\text{C/BE3}}$	39	I/O	Bus command and byte-enables. During the address phase of a transaction, $\overline{\text{C/BE3}}$–$\overline{\text{C/BE0}}$ define the bus command. During the data phase, $\overline{\text{C/BE3}}$–$\overline{\text{C/BE0}}$ are used as byte-enables. The byte-enables are valid for the entire data phase and they determine which byte lanes carry meaningful data. $\overline{\text{C/BE0}}$ applies to the LSB and $\overline{\text{C/BE3}}$ applies to the MSB.
$\overline{\text{C/BE2}}$	53		
$\overline{\text{C/BE1}}$	65		
$\overline{\text{C/BE0}}$	77		
$\overline{\text{DEVSEL}}$	59	I/O	Device-select. When $\overline{\text{DEVSEL}}$ is actively driven, it indicates that the driving device has decoded its address as the target of the current access. As an input, $\overline{\text{DEVSEL}}$ indicates if any device on the bus has been selected. If no PCI agent has asserted $\overline{\text{DEVSEL}}$, then the TI380PCIA removes itself as the PCI bus master.

† I = in, O = out

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¶ Typical bit-ordering for Intel™ and Motorola™ processor buses

The signal connecting this pin to the TI380C2x§ also should be connected to a 4.7-kΩ pullup resistor.

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ADVANCE INFORMATION

Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O†	DESCRIPTION
PCI INTERFACE (CONTINUED)			
FRAME	55	I/O	Cycle frame. FRAME is driven by the current master to indicate the beginning and duration of an access. It is asserted to indicate that a bus transaction is beginning. While FRAME is asserted, data transfers continue. When FRAME is deasserted, the transaction is in the final data phase.
GNT	25	I	Grant. GNT indicates to the TI380PCIA that access to the PCI bus has been granted. This is a point-to-point signal.
IDSEL	41	I	Initialization device select. IDSEL is used as a chip-select during configuration read and write transactions.
INTA	20	O	Interrupt A. INTA is used to request an interrupt. The assertion and deassertion of INTA is asynchronous to PCLK.
IRDY	56	I/O	Initiator ready. IRDY indicates that the bus master can complete the current data phase of the transaction. If a data phase is completed on any clock, both IRDY and TRDY are sampled and asserted. During a write, IRDY indicates that valid data is present on AD31 – AD00. During a read, it indicates that the master is prepared to accept data. Wait cycles are inserted until both IRDY and TRDY are asserted together.
PAR	63	I/O	Parity. PAR carries even parity across AD31 – AD00 and C/BE3 – C/BE0. It is driven by the master for address and write data phases; it is driven by the target for read data phases. PAR is valid one clock after the address phase. For data phases, PAR is valid one clock after either IRDY (for a write) or TRDY (for a read) is asserted.
PCLK	23	I	Clock. PCLK provides timing for all transactions on the PCI bus. All other PCI signals, except RST and INTA, are sampled on the rising edge of PCLK. PCLK is used to generate the SBCLK signal that goes to the TI380C2x§.
PERR	61	I/O	Parity error. PERR is for the reporting of data parity errors during all transactions. It is driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR is one clock for each data phase that a data parity error is detected. There are no special conditions when a PERR can be lost or when reporting of an error can be delayed. An agent cannot report a PERR until it has claimed the access by asserting DEVSEL and completing a data phase.
REQ	26	O	Request. REQ indicates to the arbiter that TI380PCIA desires use of the bus. REQ is a point-to-point signal.
RST	21	I	Reset. RST is used to hard-reset the LAN subsystem, including TI380C2x§ and the TI380PCIA. To prevent ADxx, C/BEx, and PAR signals from floating during reset, the central device can drive these lines during reset (bus-parking) but only to a logic-low level; these cannot be driven high.
SERR	62	I/O	System error. SERR, when enabled, reports address parity errors or any other system error where the result is catastrophic. The assertion of SERR is synchronous to the clock and meets the setup and hold times of all PCI signals.
STOP	60	I/O	Stop. STOP indicates that the current slave is requesting the master to stop the current transaction.

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¶ Typical bit-ordering for Intel™ and Motorola™ processor buses

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Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O†	DESCRIPTION
PCI INTERFACE (CONTINUED)			
$\overline{\text{TRDY}}$	57	I/O	Target ready. $\overline{\text{TRDY}}$ indicates the target agent's (that is, the TI380PCIA's) ability to complete the current data phase of the transaction. If a data phase is completed on any clock, both $\overline{\text{TRDY}}$ and $\overline{\text{IRDY}}$ are sample-asserted. During a read, $\overline{\text{TRDY}}$ indicates that valid data is present on AD31–AD00. During a write, $\overline{\text{TRDY}}$ indicates that the target is prepared to accept data. Wait cycles are inserted until both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted together.
SERIAL EEPROM INTERFACE			
EDIO	111	I/O	EEPROM data input/output is a bidirectional signal used to transfer data into or out of the EEPROM memory. Note I^2C memory devices typically require a pullup resistor to V_{CC} on this line. This is an open-drain output. If the optional EEPROM is not present, EDIO should be tied high.
EDC	122	O	EEPROM clock signal used to synchronize all data in and data out of the memory. I^2C memory devices typically require a pullup resistor to V_{CC} on this line. If the optional EEPROM is not present, EDC should be tied low.

† I = in, O = out

‡ The TI380PCIA SIF pin names correspond to a subset of the system interface pins on a TI380C2x§. See the TI380C2x§ data sheets for more information on individual pins. Like-named pins on the TI380PCIA and TI380C2x§ system interfaces are intended to be connected to each other.

§ TI380C3x devices can be used with TI380PCIA in the same way as TI380C2x devices.

¶ Typical bit-ordering for Intel™ and Motorola™ processor buses

The signal connecting this pin to the TI380C2x§ also should be connected to a 4.7-kΩ pullup resistor.

‖ The TI380PCIA BIF pin names correspond to a subset of the local memory bus interface pins on a TI380C2x§. Like-named pins on the two devices are intended to be connected to each other. Consult the TI380C2x§ data sheets for more information on individual pins.

NOTE 1: The TI380PCIA allows driver software to set SBCLK output to a steady high state. This signal is driven to a steady high state during power-down operations.

ADVANCE INFORMATION

architecture

The major blocks of the TI380PCIA, illustrated in Figure 2, include the PCI interface (PCIIF), TI380C2x† interface (SIF), ROM interface (ROMIF), serial EEPROM interface (EIF), and burned-in address emulation interface (BIF). The functionality of each block is described in the following sections.

PCI interface (PCIIF)

The PCIIF block contains all logic needed to interact with the PCI bus and allows the TI380PCIA to assume the role of bus master or slave. This block controls all communication between the TI380PCIA and the PCI bus. All signals entering the PCIIF, as well as signals generated within the PCIIF, are synchronous to the PCLK signal.

The TI380PCIA also checks and generates parity for data presented on the PCI bus at the PCIIF.

The PCIIF generates and responds to the PCI cycles listed in Table 1.

Table 1. PCI Interface Logic

TI380PCIA CAN GENERATE:	TI380PCIA RESPONDS TO:
Memory read line	I/O reads and writes
Memory write and invalidate	Configuration reads and writes
Memory write	All types of memory reads and writes

The TI380PCIA asserts slave-initiated termination, if the initiator exceeds one data-phase transfer.

address decode

The TI380PCIA uses only the most significant 27 address bits present in AD31–AD00 to decode an access directed at the TI380PCIA for a TI380C2x† DIO access, and the most significant 16 bits for a ROM access. The TI380PCIA's base address selects a block of eight contiguous 32-bit memory or I/O locations for DIO access or 64K bytes of address space for ROM access. Access to each register within the selected memory, I/O, or configuration space is uniquely decoded. The decode logic returns $\overline{\text{DEVSEL}}$ as a medium-latency device.

The PCIIF logic generates control signals that propagate either to configuration registers, the SIF, ROMIF, or EIF within the TI380PCIA. The address and command/byte-enables are valid and sustained throughout each PCI cycle. Configuration registers can be accessed through configuration cycles when the TI380PCIA's address is decoded.

address/data-parity checking and generation

The PCIIF checks and generates parity for addresses during bus master operations and for data during master and slave operations. If the PCIIF encounters $\overline{\text{SERR}}$ two PCLKs after the address phase when it is mastering the PCI bus, it terminates its transaction immediately and regains control of the TI380C2x† SIF. If the PCIIF detects any address error (even if not selected) or data parity error (only when selected) while operating as a PCI slave, or if it detects a data parity error while operating as a PCI bus master, it pulses $\overline{\text{PERR}}$ and sets bit 15 in the status register to 1. Bus transactions causing the parity error are otherwise ignored by the LAN subsystem. Any bus-mastering transaction that encounters a parity error is aborted by the TI380PCIA. This detection also prevents future bus master cycles from occuring until a reset occurs.

The TI380PCIA performs a bus master cycle when bus-mastering is enabled and the TI380C2x† requests the SIF bus.

The supported PCI master cycles are:

- Memory write
- Memory read line
- Memory write and invalidate

† TI380C3x devices can be used with TI380PCIA in the same way as TI380C2x devices.

address/data-parity checking and generation (continued)

During PCI master cycles, PCIIF is able to handle the following:

- Master-abort termination: due to no $\overline{\text{DEVSEL}}$ response
- Slave-initiated termination: disconnect/retry and slave-abort
- Parity-error processing

TI380C2x† interface (SIF)

The SIF handles all communications between the TI380C2x† and the TI380PCIA.

The TI2000 software standard‡ requires that the TI380PCIA SIF include a configuration register at I/O address 0xE–0xF. This is the same location as the TI380C2x† DIO DMALEN register; therefore, access to the DIO DMALEN register from the TI380PCIA is masked, and the TI2000 configuration register information is presented instead.

When there is no DIO access pending, the TI380PCIA SIF acknowledges all $\overline{\text{SBRQ}}$ from the TI380C2x† and allows the TI380C2x† to control the SIF bus. If the PCIIF initiates a DIO access while the TI380C2x† is controlling the SIF bus and is performing a DMA access, the SIF signals the TI380C2x† to relinquish control of the SIF bus and let the DIO proceed. On completion of the DIO cycle, the SIF logic again grants the SIF bus to the TI380C2x† if the interrupted DMA sequence is not complete.

The interface between the TI380PCIA and the TI380C2x† operates in Motorola mode. The interface is designed so it can operate with drivers that use 8- or 16-bit I/O instructions on the host. Accesses to the SIFDAT, SIFDAT/INC, and SIFADR registers are ideally made with 16-bit I/O instructions from the host. If a driver has to perform byte-accesses to these registers, then the odd byte must be accessed before the even byte.

Note that on Intel platforms, the “INSTR word” and the “OUTSTR word” 16-bit I/O instructions use a little-endian byte-ordering that does not work without additional byte-swapping when used with the TI380PCIA Motorola-mode big-endian interface. These instructions are typically used only in 16-bit pseudo DMA drivers.

For more information on byte operations between the host and the TI380C2x†, see the description of DIO operations on pages 4-16 and 4-28 of the *TMS380 Second Generation Token Ring User’s Guide* (literature number SPWU005).

interrupt request

interrupting the PCI host

The SIF takes an $\overline{\text{SIRQ}}$ from the TI380C2x†, sends it to the PCIIF, and the PCIIF then translates it into an $\overline{\text{INTA}}$ on the PCI bus. The generation of $\overline{\text{INTA}}$ on the PCI bus is held off until the data in the TI380PCIA FIFO has been emptied. This interrupt is done to ensure data coherency.

clearing the host interrupt request

Driver software running on the host can clear the $\overline{\text{SIRQ}}$ interrupt by writing a 0 to bit 8 (SYSTEM_INTERRUPT) of the SIFCMD register in the TI380C2x†. Writing a 1 to this location has no effect [see Section 4.3.10.1 in the *TMS380 Second Generation Token Ring User’s Guide* (literature number SPWU005)].

ROM interface (ROMIF)

The ROMIF supports remote program load for PCI LAN adapter cards. This interface supports a 64K-byte ROM address range aligned on a 64K-byte boundary. Since the PCI bus can access the ROM in any byte order, the ROMIF reads all 32 bits for each PCI ROM access. This latency is acceptable because the PCI bus does not execute code out of the ROM. The ROM is normally accessed during system configuration when performance is not critical. The ROMIF uses either 14 or 16 bits of the address, depending on the setting of bit 17 in the MISCCTRL register. In 14-bit mode, the ROMIF appends two bits to the most significant end of the address from

† TI380C3x devices can be used with TI380PCIA in the same way as TI380C2x devices.
‡ TI2000 software standard specification is available from the local TI Sales Office.

ROM interface (ROMIF) (continued)

its internal page register. The TI2000 software standard requires that writes to the ROM location increment to the next 16K page and that the ROM pages be cycled through only once until the next reset. Note that $\overline{\text{ROMCS}}$ does not go low when the host attempts to write to the EPROM.

When $\overline{\text{RST}}$ is driven high, the value on ROMA[07:00] is latched into the board configuration register in the TI380PCIA configuration space (DWORD address 0x44). The value on ROMA[07:00] can be provided by pullup and pulldown resistors that do not affect operation after reset. This feature allows designers to support jumpers or board-stuffing options sensed by software that reads the board configuration register. If pullup and pulldown registers are not used, the contents of the board configuration register are undefined after reset.

When the host computer initiates a 32-bit read to the ROMIF, the TI380PCIA fetches four bytes from the ROM and presents the resulting 32-bit DWORD to the PCI bus. The fetches from the ROM start with the least significant byte, byte 0, followed by bytes 1, 2, and 3. The data is presented to the PCI data bus as shown in Figure 3.

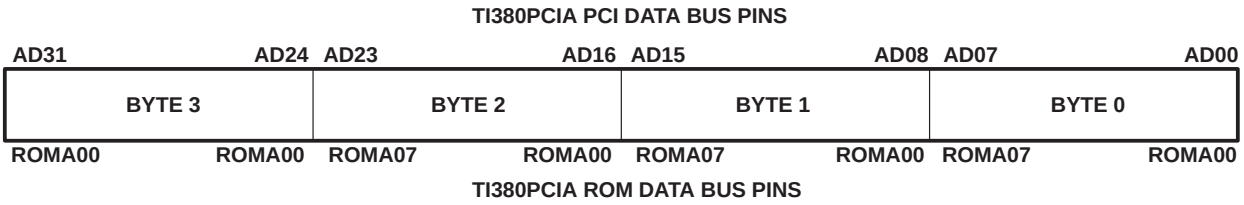

Figure 3. PCI Bus Data

The ROMIF has been designed for operation with EPROM devices with 100-ns access times.

serial EEPROM interface (EIF)

The TI380PCIA includes an interface for an optional I^2C serial EEPROM. The EEPROM contains the following:

- Bytes 0x0 – 0x7 contain eight bytes of PCI configuration information that are automatically loaded into the appropriate PCI configuration register by the TI380PCIA at power-on.
- Byte 0x8 is a checksum calculated on bytes 0–7. This checksum byte is automatically read at power-on by the TI380PCIA. If the checksum read from byte 8 does not agree with the checksum that the TI380PCIA calculated from bytes 0–7, then the TI380PCIA sets the ECRCERR and NEP bits in the EEPROM read/write register in TI380PCIA configuration space.
- Bytes 0x09 – 0x10 contain the six bytes of the BIA and two bytes of the BIA checksum. The TI380PCIA reads these bytes and stores them in an internal register, the contents of which are presented to the TI380C2x† local memory bus when the TI380PCIA detects an access to the BIA. In this way, the TI380PCIA emulates the presence of a BIA ROM on the TI380C2x† local memory bus. The TI380PCIA does not verify the BIA checksum.
- Byte 0x11 is reserved for use by TI2000 drivers. This byte is not read automatically by the TI380PCIA, but it is read by TI2000 drivers that load bit 0 from this byte into the TI380PCIA MISCCTRL register bit 8 and load bit 1 from this byte into TI380PCIA MISCCTRL register bit 9. This byte allows the TI2000 driver to read the network speed and topology from nonvolatile memory before attempting to access the network.
- Bytes 0x12 – 0x20 are reserved for future use by the TI380PCIA.
- Bytes 0x21 – 0xFF are available for user-defined variable storage.

† TI380C3x devices can be used with TI380PCIA in the same way as TI380C2x devices.

serial EEPROM interface (EIF) (continued)

Several copies of the BIA can be programmed into the EEPROM user-defined space as a protection against inadvertent modification of the copy of the BIA at addresses 0x09–0x0E.

In systems that do not use an EEPROM, the EDC pin should be tied low and the EDIO pin should be tied high. This action causes default values to be loaded into the configuration registers as shown in Table 2. EDC and EDIO are sampled at the deassertion of $\overline{\text{RST}}$. If EDC is low and EDIO is high at the deassertion of reset, the TI380PCIA functions as if no EEPROM is present in the system.

Table 2. EIF Configuration Registers

PARAMETER DESCRIPTION	EEPROM BYTE ADDRESS	DEFAULT VALUE
Vendor ID least significant byte	0x00	0x4C
Vendor ID most significant byte	0x01	0x10
Device ID least significant byte	0x02	0x08
Device ID most significant byte	0x03	0x05
Revision ID	0x04	0x01
Sub-class	0x05	0x80
Min_Gnt	0x06	0x01
Max_Lat	0x07	0x00
Checksum	0x08	0x7A
Burned-in address	0x09 0x0A 0x0B 0x0C 0x0D 0x0E 0x0F 0x10	BIA MSbyte BIA byte BIA byte BIA byte BIA byte BIA LSbyte BIA most significant checksum BIA least significant checksum
TI2000 reserved byte	0x11	0x01
Reserved for future use	0x12 ... 0x20	Reserved
User-defined	0x21 ... 0xFF	User-defined

The default values for the parameters stored in the EEPROM can always be accessed by software because copies of these values are stored in a series of hardwired registers in the TI380PCIA configuration space (see Table 3). These registers are read-only and are unaffected by the process of loading data from the optional EEPROM.

Table 3. Hardwired Registers in TI380PCIA Configuration Space

PARAMETER DESCRIPTION	HARDWIRED REGISTER NAME (CONTAINS READ-ONLY COPY OF DEFAULT VALUE)	REGISTER ADDRESS IN TI380PCIA CONFIGURATION SPACE
Vendor ID	Hardwired vendor ID	4C
Device ID	Hardwired device ID	4C
Revision ID	Hardwired revision ID	50
Subclass	Hardwired subclass	50
Min_Gnt	Hardwired Min_Gnt	50
Max_Lat	Hardwired Max_Lat	50

serial EEPROM interface (EIF) (continued)

The algorithm for generating the cyclic-redundancy check (CRC) code placed in the serial EEPROM byte 08 is shown in Figure 5. When the TI380PCIA reads the EEPROM after power up, it checks the CRC in byte 08 to ensure that it was generated with this algorithm. If the CRC from byte 08 of the EEPROM does not match the CRC calculated from EEPROM bytes 00–07, then the TI380PCIA sets the NEP and ECRCERR bits in the EEPROM read/write register. When the NEP and ECRCERR bits are set because of a CRC mismatch on the data read from the EEPROM, the TI380PCIA still continues to load the data read from the EEPROM into the PCI configuration registers. In the event that the EEPROM is unprogrammed, the TI380PCIA configuration registers can be left in an unknown state. In such a case, the EEPROM can be initialized by using PCI BIOS calls to read the hardwired configuration register addresses associated with each PCI slot. The slot containing the TI380PCIA responds with the contents of the hardwired registers. Once the slot containing the TI380PCIA has been identified, the EEPROM can be programmed using the EEPROM register in the PCI configuration space. After the next power cycle, the TI380PCIA loads the contents of the initialized EEPROM.

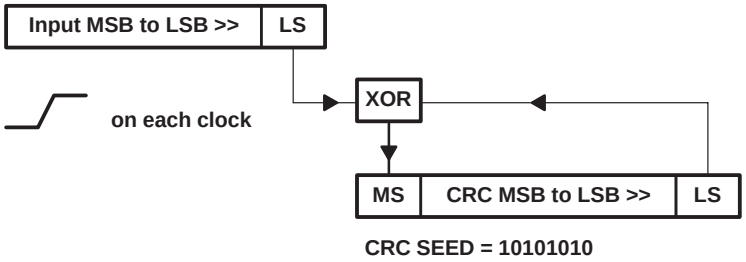

Figure 4. CRC Code Calculation

It is assumed that data in the serial EEPROM is shifted LSB to MSB, consistent with other serial communication streams.

The routine that calculates the serial EEPROM CRC over the first eight bytes of the EEPROM is shown in Figure 5. The resulting value is written to the ninth byte of the EEPROM. The “MSB” argument passed is a copy of the bytes read from the EEPROM and stored in an array. The BIA has its own checksum, which is not verified by the TI380PCIA.

```
unsigned short xor-crc (unsigned short   *msb, int bytes)
{
        BYTE crc=0xaa; // seed
        int i;
        for (i=0; i<bytes; i++)
                crc^=msb[i];
        return (crc);
}
```

Figure 5. EEPROM CRC Calculation Routine

The BIA downloaded from the EEPROM ultimately appears in the adapter RAM at chapter 0, address 0. The high or odd byte of each 16-bit word contains two hexadecimal digits of the 12-digit BIA, the most significant digit first. The last two high bytes of the first eight 16-bit words contain the 16-bit checksum of the BIA. The checksum is calculated as shown below.

serial EEPROM interface (EIF) (continued)

The example that follows is an adapter RAM memory dump for a card with BIA = 0001fafe1093.

example:

Address		Data							
000000	:	0000	0100	fa00	fe00	1000	9300	0b00	9200

Address	Data	Checksum
01	00	0001
03	01	fafe
05	fa	+ 1093
07	fe	_____
09	10	(1) 0b92
0b	93	
0c	0b	
0d	92	

The EEPROM also can be read and written under software control by PCI configuration register 0x48. A typical I^2C EEPROM that can be used with the TI380PCIA is the 24C02. EEPROMs that provide external address pins for identification of several devices on the I^2C bus should have these address pins pulled down to logic 0.

burned-in address interface (BIF)

The BIF logic is designed to connect directly to the local memory bus of the TI380C2x†. The BIF serves two purposes:

- Checks the status cycles on the local memory bus to detect the initialization and completion of DMA transfers from the TI380C2x†
- Detects accesses to the BIA ROM from the TI380C2x†. During a BIA access, the TI380PCIA drives data onto MADH00–07, emulating a BIA programmable read-only memory (PROM). This eliminates the need for a separate BIA PROM.

in-circuit test NAND tree operation

The terminal function table explains how to use the $\overline{\text{ICT}}$ pins on the TI380PCIA to place the output pins of the TI380PCIA in a 3-state mode to allow for in-circuit testing of a printed circuit board.

The TI380PCIA also contains a NAND tree that can be used during the in-circuit testing process to verify the integrity of the solder connections to the TI380PCIA. The NAND tree is activated by latching a control value on the SADL0–7 pins on the rising edge of the signal applied to the $\overline{\text{ICT}}$ pin.

To activate the NAND tree, complete the following steps:

1. Drive and hold $\overline{\text{ICT}}$ low.
2. Drive and hold the MAX0 input low and drive the MAX2 input high. Drive and hold the SADL0–7 pins as shown in Figure 6.
3. While holding the values in step 2, pull the $\overline{\text{ICT}}$ input high to latch the values from step 2.

   The connections to the TI380PCIA can now be tested with the NAND tree. The NAND tree can be deactivated by repeating steps 1 through 3 with the data applied to the SADL0–7 pins in step 2 set as shown in Figure 7.

† TI380C3x devices can be used with TI380PCIA in the same way as TI380C2x devices.

in-circuit test NAND tree operation (continued)

SADL7	SADL6	SADL5	SADL4	SADL3	SADL2	SADL1	SADL0
0	0	0	0	0	0	1	0

Figure 6. SADL0–SADL7 Pins for Activation of NAND Tree

SADL7	SADL6	SADL5	SADL4	SADL3	SADL2	SADL1	SADL0
0	0	0	0	0	0	0	0

Figure 7. SADL0–SADL7 Pins for Deactivation of NAND Tree

TI380PCIA device operation

The TI380PCIA PCIIF functions as both master and slave of the PCI bus.

TI380PCIA behavior as a PCI bus target

The PCIIF in the TI380PCIA acts as an I/O slave to the PCI bus after power up and when the LAN subsystem is not the PCI bus master. It monitors and decodes PCI commands for memory, I/O, and configuration accesses. Enabling of memory and I/O accesses are performed by setting and clearing bits in the command register.

TI380PCIA behavior as a PCI bus master

The TI380PCIA requests that it become a master on the PCI bus after the TI380C2x† initiates a DMA transfer to the TI380PCIA. The TI380C2x† begins a DMA series by asserting $\overline{\text{SBRQ}}$ and requesting its own system interface bus. The TI380PCIA performs a DIO access to the TI380C2x† and reads the DMA length before granting the SIF bus to the TI380C2x†. (The read cycle occurs only on the first transaction of the DMA access.) If the TI380C2x† has requested DMA write access and there is no DIO access from the PCI bus pending, the TI380PCIA acknowledges the request and latches the DMA address and completes the write cycle from the TI380C2x† to start filling the FIFO. Subsequent writes continue to fill the FIFO. When the FIFO contains the smaller of 60 bytes or one cache line of data, the PCIIF logic arbitrates for the PCI bus and transfers the data in a burst sequence.

If the access is a read access, the TI380PCIA acknowledges the request and latches the DMA address. It then initiates a read access on the PCI bus. If the DMA length exceeds the cache line size, as defined by the contents of the TI380PCIA cache line size configuration register, then the read access on the PCI bus is a burst read. As data is available from the PCI bus, it is provided to the TI380C2x†. Since the PCI bus has a higher bandwidth than the TI380C2x† SIF bus, the 64-byte FIFO in the TI380PCIA fills as the burst read continues. If the FIFO fills before the DMA length is reached, the PCI master relinquishes the bus until the FIFO is almost empty.

If a DIO conflict occurs while the DMA is in progress, the TI380PCIA forces the TI380C2x† off the SIF bus to allow the DIO to complete. The DMA operation resumes at the point where it was interrupted and continues until completion.

removal of TI380PCIA as bus master

The TI380PCIA is removed as the PCI bus master under two conditions:

- Target-initiated retry and/or termination
- Master-initiated termination as no PCI agent asserted $\overline{\text{DEVSEL}}$

TI380PCIA behavior on the SIF bus

The TI380PCIA SIF functions as both master and slave of the SIF bus.

† TI380C3x devices can be used with TI380PCIA in the same way as TI380C2x devices.

SIF behavior as a SIF master

The TI380PCIA SIF logic masters the TI380C2x† system interface to translate signals from the PCIIF into TI380C2x† control signals and relays TI380C2x† return signals to the PCIIF.

SIF behavior as a slave

The SIF acts as a slave when the TI380C2x† is engaged in DMA operations. During DMA transfers, other PCI masters can access the TI380C2x† DIO registers. The TI380PCIA retries all accesses from the PCI bus while posting a preempt to the TI380PCIA SIF. When the TI380PCIA SIF receives the preempt, it signals the TI380C2x† to relinquish the SIF bus at the earliest opportunity and does not grant the TI380C2x† the SIF bus until the preempt is removed.

FIFO control

The 64-byte FIFO serves to reduce the bandwidth demand on the PCI bus from the TI380PCIA. It is used only when the TI380C2x† is functioning as a PCI bus master during DMA accesses.

FIFO operation (write cycles)

The TI380PCIA BIF checks the status cycles on the TI380C2x† local bus. When the TI380PCIA detects a status code that indicates the start of a DMA write from the TI380C2x† to the host computer, the TI380PCIA immediately initiates a DIO read of the DMALEN register in the TI380C2x†. When the DMALEN register has been read, the TI380PCIA grants the TI380C2x† control of the SIF bus and the DMA write can proceed.

The DMALEN register is not read again until the next DMA transaction starts. During DMA write cycles from the TI380C2x†, the TI380PCIA stores one cache line or 60 bytes in the FIFO before requesting the PCI bus. It drives data on the PCI bus as long as it has sufficient data in the FIFO or until it loses the PCI bus. The FIFO control requests the PCI bus under the following conditions:

- A full cache line is available for writing and the DMA address is aligned on a cache boundary. The PCI bus cycle is a write-and-invalidate cycle.
- The TI380C2x† relinquishes control of the SIF bus because of completion of a DMA write from the TI380C2x† with DMA data in the TI380PCIA FIFO. If the quantity of data in the TI380PCIA FIFO is greater than or equal to the cache line size and the DMA address is aligned on a cache line boundary, the PCI cycles are write-and-invalidates. If the quantity of data in the TI380PCIA FIFO is less than the cache line size or the DMA address is not aligned on a cache line boundary, the PCI cycles are memory writes.
- A full 32-bit word is available for the PCI bus and the cache line size is zero.

If the host attempts a DIO access during a DMA transfer between the TI380C2x† and the host, the TI380PCIA signals the TI380C2x† to pause the DMA transfer. When the TI380PCIA regains control of the SIF bus, the DIO access from the host is allowed to complete, and then the TI380PCIA allows the DMA transfer to restart and run to completion. The TI380PCIA signals the host to retry the DIO access until the TI380PCIA gains control of the SIF bus and can allow the DIO access to complete. In the case of a DMA write from the TI380C2x† to the host (which is almost complete), the TI380PCIA can give up control of the SIF bus prior to transferring the last data from the FIFO to the host. If the host initiates a DIO access at this time, the DIO access is allowed to complete immediately, that is, before the FIFO empties.

FIFO operation (read cycles)

The TI380PCIA BIF checks the status cycles on the TI380C2x† local bus. When the TI380PCIA detects a status code that indicates the start of a DMA read by the TI380PCIA from the host computer, the TI380PCIA immediately initiates a DIO read of the DMALEN register in the TI380C2x†. When the DMALEN register has been read, the TI380PCIA grants the TI380C2x† control of the SIF bus, and the DMA read can proceed. The DMALEN register is not read again until the next DMA transaction starts. The TI380PCIA then requests the PCI bus and begins filling the FIFO. As data is available, it is provided to the TI380C2x†. The TI380PCIA counts the

† TI380C3x devices can be used with TI380PCIA in the same way as TI380C2x devices.

FIFO operation (read cycles) (continued)

bytes received from the PCI bus and decrements its DMA length counter. If the DMA count is not zero, but the TI380C2x† releases the SIF bus, the TI380PCIA continues to read data from the PCI bus. The TI380PCIA logic terminates the PCI ownership when the DMA count goes to zero.

The TI380PCIA always performs memory-read line commands on the PCI bus regardless of DMA count or address alignment.

BIA interface

On power up, BIA data is loaded from the EEPROM and held in registers inside the TI380PCIA. All the pins on the local bus of the TI380C2x† necessary to sense an access from the TI380C2x† to an attached BIA ROM are connected to the TI380PCIA. When the TI380PCIA senses an access to the BIA ROM, it drives the BIA data onto the MADHxx bus, simulating the presence of a BIA ROM on the TI380C2x† local bus.

TI380PCIA registers

The TI380PCIA supports a number of registers to facilitate communications between the host computer and the token-ring LAN subsystem. It also performs address translation to map TI380C2x† DIO registers into host computer memory or I/O space. Table 4 lists the configuration space registers implemented within the TI380PCIA.

Table 4. Configuration Space Header‡

DWORD ADDRESS	BYTE 3	BYTE 2	BYTE 1	BYTE 0	READ/WRITE
0x00	Device ID		Vendor ID		R
0x04	Status		Command		R/W
0x08	Class Code			Revision ID	R
0x0C	Built-In Self-Test	Header Type	Latency Timer	Cache Line Size	R/W
0x10	Base Address I/O				R/W
0x14	Base Address Memory				R/W
0x18	Reserved (returns 0)				R
0x1C	Reserved (returns 0)				R
0x20	Reserved (returns 0)				R
0x24	Reserved (returns 0)				R
0x28	Reserved (returns 0)				R
0x2C	Reserved (returns 0)				R
0x30	Expansion ROM Base Address				R/W
0x34	Reserved (returns 0)				R
0x38	Reserved (returns 0)				R
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	R/W
0x40	Miscellaneous Control (MISCCTRL) Register				R/W
0x44	Board Configuration Register				R
0x48	Reserved (returns 0)		EEPROM		R/W
0x4C	Hardwired DEVICE ID		Hardwired VENDOR ID		R
0x50	H/W Subclass	H/W Max Lat	H/W Min_Gnt	H/W Revision ID	R
0x54	TI380PCIA Interface Control Register				R
0x58–0xFF	Reserved (returns 0 when read)				

‡ Shading denotes registers that are autoloaded from an external serial EEPROM at power up.

† TI380C3x devices can be used with TI380PCIA in the same way as TI380C2x devices.

device identification

The TI380PCIA contains the device identification information in its configuration space as shown in Table 5.

Table 5. Device Identification

REGISTER	HEX VALUE
Vendor ID	104Ch†
Device ID	0508h†
Revision ID	01
Class code	028000
Header type	00

† These values are defaults and can be overwritten by the contents of the optional EEPROM.

command register—configuration space DWORD address (0x04)

Figure 8 shows the command register layout.

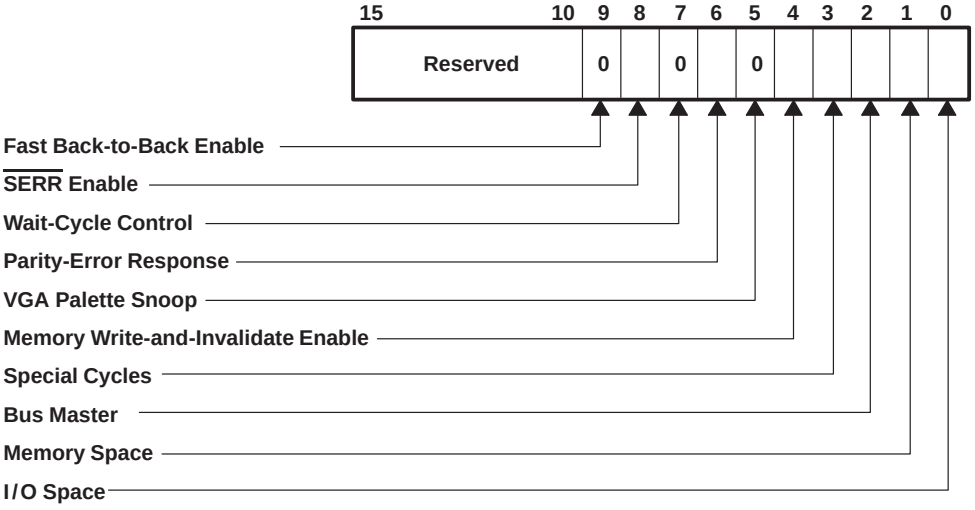

Figure 8. Command Register Layout

The command register provides coarse control over the TI380PCIA's ability to generate and to respond to PCI cycles. When 0 is written to this register, the device is logically disconnected from the PCI bus for all accesses except configuration accesses.

The command register is set to 0 at power up and after hardware reset.

Bit 00: I/O space. Controls the TI380PCIA's response to I/O space accesses. A value of 0 disables the TI380PCIA's response. A value of 1 allows the TI380PCIA to respond to I/O space accesses.

Bit 01: Memory space. Controls the TI380PCIA's response to memory space accesses. A value of 0 disables the TI380PCIA's response. A value of 1 allows the TI380PCIA to respond to memory space accesses.

Bit 02: Bus master. Controls the TI380PCIA's ability to act as a master on the PCI bus. A value of 0 disables TI380PCIA from generating PCI accesses. A value of 1 allows the TI380PCIA to behave as a bus master. If the automatic software-reset bit in the TI380PCIA interface control register (0x54) is set to a one, then the action of clearing the bus master bit of the TI380PCIA command register from one to zero also resets the TI380PCIA.

command register—configuration space DWORD address (0x04) (continued)

Bit 03: Special cycles. Allows the LAN subsystem to enter low-power mode following a shutdown broadcast. All other special-cycle messages are ignored. Device drivers must reinitialize and download microcode to the LAN subsystem when the subsystem exits low-power mode.

Bit 04: Memory write-and-invalidate enable. Controls memory write-and-invalidate cycles. A value of 1 enables the TI380PCIA to generate memory write-and-invalidate cycles. When this bit is 0, the memory-write command must be used instead.

Bit 05: VGA palette snoop. Applies to video graphics adapter (VGA) subsystems and is hardwired to 0

Bit 06: Parity error response. This bit controls the TI380PCIA response to parity errors. When this bit is set to 1, the TI380PCIA takes its normal action when a parity error is detected. When this bit is reset to 0, the TI380PCIA ignores any parity errors that it detects and continues normal operation. This bit is set to 0 after reset.

Bit 07: Wait-cycle control. This bit is hardwired to 0 because the TI380PCIA does not support address/data-stepping.

Bit 08: $\overline{\text{SERR}}$ enable. This bit is an enable bit for the $\overline{\text{SERR}}$ driver. A value of 0 disables the $\overline{\text{SERR}}$ driver and a value of 1 enables it. The state of this bit after $\overline{\text{RST}}$ is 0.

Bit 09: Fast back-to-back enable. This bit is hardwired to 0 because the TI380PCIA does not support fast back-to-back transactions to different devices.

Bits 10–15: Reserved. These reserved bits are read as 0.

status register—configuration space DWORD address (0x04)

Figure 9 shows the status register layout.

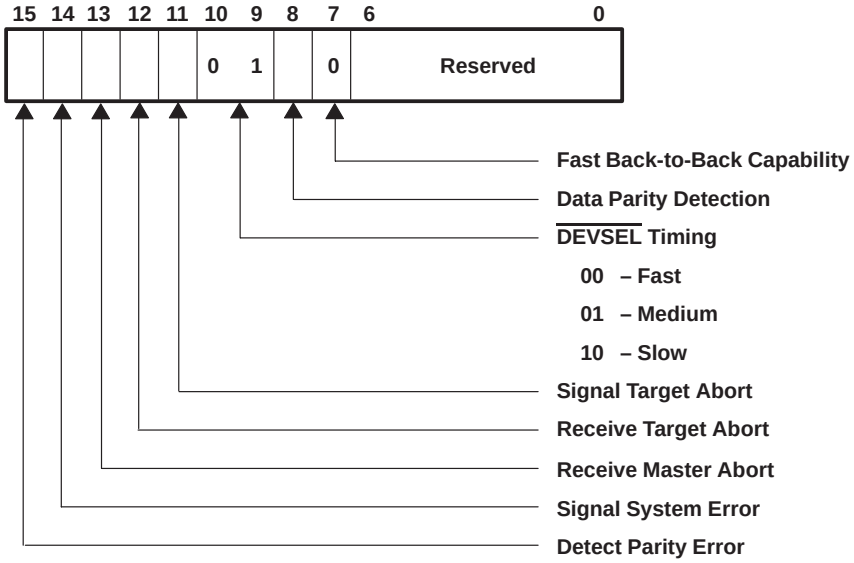

Figure 9. Status Register Layout

The status register records status information for PCI bus-related events. Reads from this register behave normally. Writes are slightly different in that bits can be reset to 0, but not set to 1. A bit is reset whenever data is written to the register and the corresponding bit of the written data contains a 1.

status register—configuration space DWORD address (0x04) (continued)

Bits 00–06: Reserved

Bit 07: Fast back-to-back capability. This bit is hardwired to 0 because the TI380PCIA does not support fast back-to-back cycles as a slave.

Bit 08: Data-parity detection. This bit is set to 1 when three conditions are met: 1) the PCI device asserted $\overline{\text{PERR}}$ itself or observed $\overline{\text{PERR}}$ asserted; 2) the device setting the bit acted as the bus master for the operation in which the error occurred; 3) the parity error response bit (in the command register) is set.

Bits 09–10: $\overline{\text{DEVSEL}}$ timing. $\overline{\text{DEVSEL}}$ timing for the TI380PCIA is set to 01 (medium).

Bit 11: Signal target abort. This bit is set to 1 whenever TI380PCIA terminates a transaction with slave abort.

Bit 12: Receive target abort. This bit is set to 1 whenever a transaction from the TI380PCIA is terminated with slave abort.

Bit 13: Receive master abort. This bit is set to 1 whenever a transaction from the TI380PCIA is terminated with master abort.

Bit 14: Signal system error. This bit is set whenever TI380PCIA asserts $\overline{\text{SERR}}$.

Bit 15: Detect parity error. This bit is set by TI380PCIA whenever it detects a parity error, even if parity-error handling is disabled (as controlled by the parity error response bit in the command register).

miscellaneous functions

cache line size (CLS)—configuration space DWORD address (0x0C)

The CLS register is loaded with the host system data cache line size. On reset, it is set to 0. The value in this register controls the TI380PCIA FIFO fill/flush algorithm. The value in this register should be a power of two that is greater than or equal to 4, or a sum of those powers of two.

latency timer (LT)—configuration space DWORD address (0x0C)

The TI380PCIA supports burst data transfer on the PCI bus; therefore, a latency timer register is needed as defined in the PCI specification.

header type — configuration space DWORD address (0x0C)

This register defines the layout of DWORD addresses 0x10–0x3C in the configuration space header. The TI380PCIA supports only header type 0x00; therefore, contents of the header type register are read as 0.

built-in self-test (BIST)—configuration space DWORD address (0x0C)

The TI380PCIA does not support built-in self-test and returns 0 when the BIST register is read.

base address I/O register (BASE0)—configuration space DWORD address (0x10)

Figure 10 shows the I/O base address register (BASE0) layout.

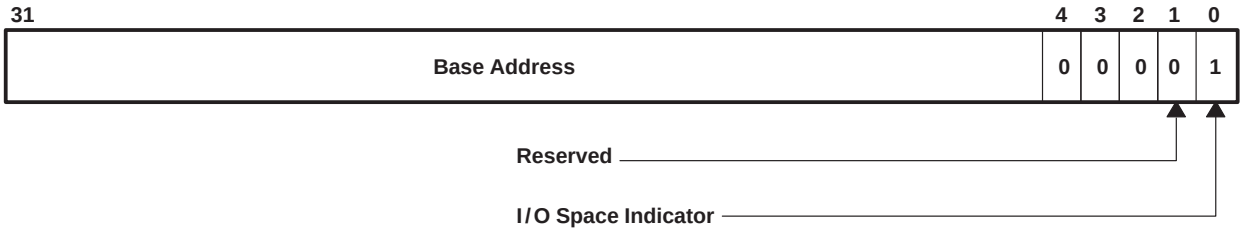

Figure 10. Base Address Register for I/O

The TI380PCIA supports only one I/O address range decoded down to eight contiguous 32-bit locations. After reset, the value of the address map is set to 0x1. Bits 0–4 are read-only and contain 0x1. The LAN subsystem is expected to reside in I/O space under normal operations for conformance with the TI2000 software specification.

base address memory register (BASE1)—configuration space DWORD address (0x14)

Figure 11 shows the memory base address register (BASE1) layout.

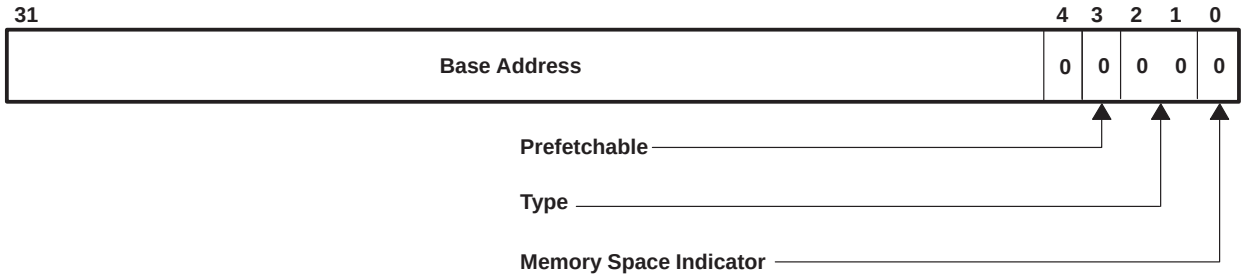

Figure 11. Base Address Register for Memory

The TI380PCIA supports only one memory address range decoded down to eight contiguous 32-bit locations. After reset, the value of the address map is set to 0x0. Bits 0–4 are read-only and contain 0x0. The LAN subsystem is expected to reside in I/O space under normal operations for conformance with the TI2000 software specification; therefore, this register is not used.

expansion ROM base address register (BASEROM)—configuration space DWORD address (0x30)

Figure 12 shows the layout of the expansion ROM base address register.

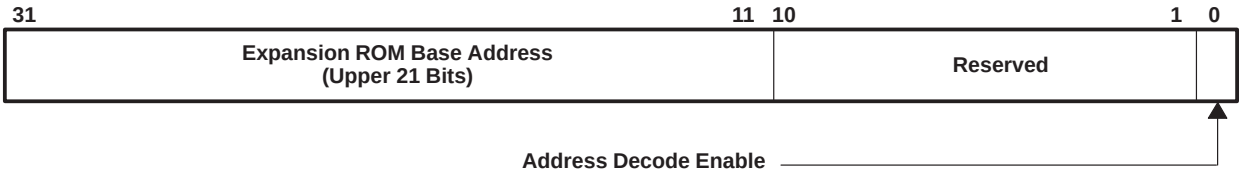

Figure 12. Expansion ROM Base Address Register Layout

The TI380PCIA supports an RPL expansion ROM on a PCI bus add-in card. This register is used to configure the location of the expansion ROM. The BASEROM supports address alignment on a 64K-byte boundary. Bits 16–31 and bit 0 of BASEROM are read/write. Bits 1–15 are read-only and are read as 0x0. Bit 0 is set by the host. The TI380PCIA supports 64K-byte ROM devices.

interrupt line—configuration space DWORD address (0x3C)

TI380PCIA uses a PCI bus interrupt so this register is implemented as an 8-bit read/write register. The value after reset is 0x00. The least significant four bits are passed to the MISCCTRL register and the TI2000 configuration register.

interrupt pin—configuration space DWORD address (0x3C)

This is hardwired to 0x01 to indicate that $\overline{\text{INTA}}$ is used as the interrupt pin.

minimum grant (Min_Gnt)—configuration space DWORD address (0x3C)

This register is loaded with a value from the EEPROM. If no EEPROM is present, the register is loaded with 0x01.

maximum latency (Max_Lat)—configuration space DWORD address (0x3C)

The TI380C2x† uses a buffer that is larger than 1K byte to store network data; therefore, at the maximum network data rate of 16 Mbps, the TI380C2x† can be serviced at intervals greater than 64 µs. This register is loaded with a value from the EEPROM. If no EEPROM is present, the register is loaded with 0x00.

subsystem-specific registers

The TI380PCIA contains the following registers in addition to the PCI-prescribed registers:

- Miscellaneous control register
- Board configuration register
- EEPROM read/write register
- TI380PCIA interface control register
- TI2000 configuration register

These registers are described in this section.

† TI380C3x devices can be used with TI380PCIA in the same way as TI380C2x devices.

miscellaneous control register (MISCCTRL) — configuration space DWORD address (0x40)

Figure 13 shows the layout of the miscellaneous control register.

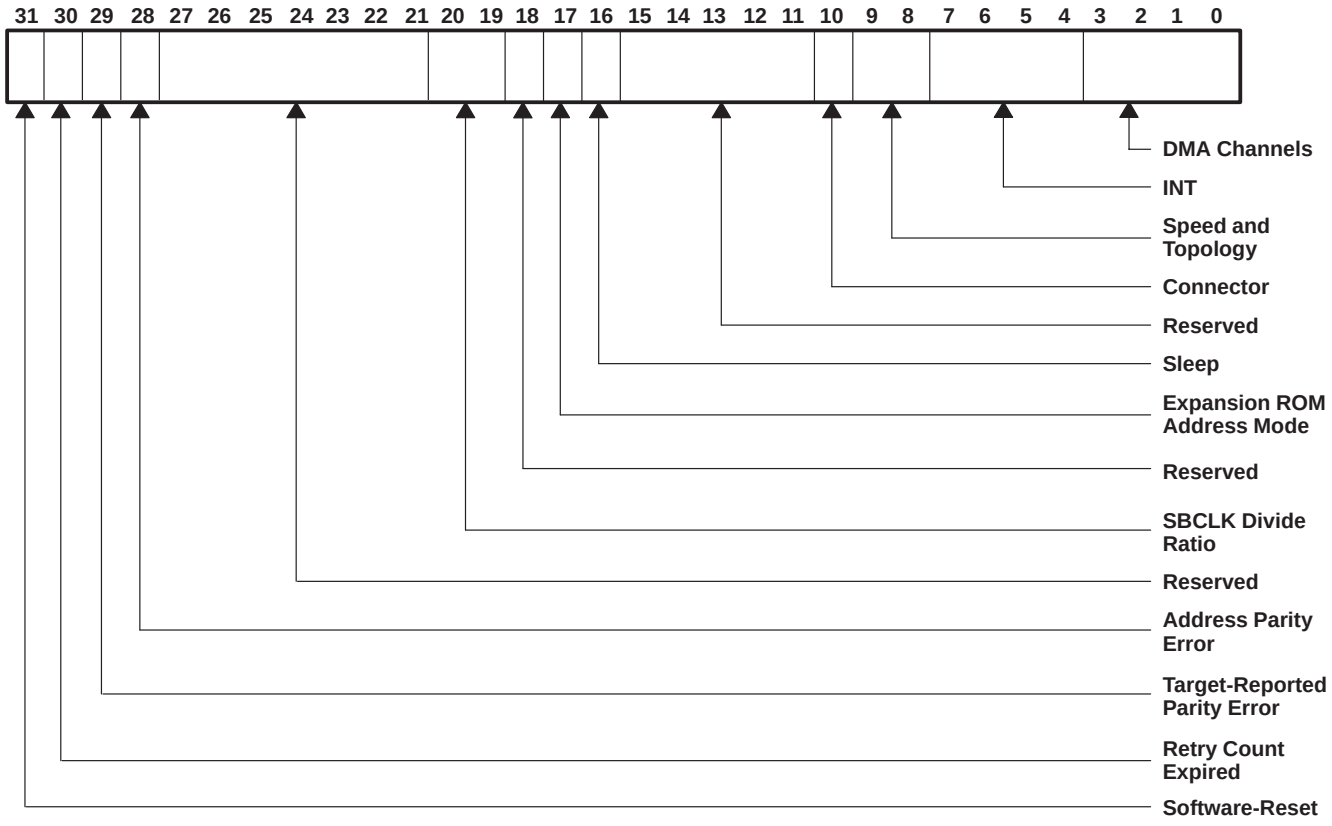

Figure 13. Miscellaneous Control Register Layout

The MISCCTRL is a collection of LAN subsystem control functions. The value of the bit fields in this register after reset are as indicated.

Bits 00–03: DMA channels. DMA channel has no meaning in a PCI context. These four bits also appear in the TI2000 configuration register where they select between bus master DMA operation and pseudo-DMA operation as defined by the TI2000 software specification. When this field has the value of 0xF, a TI2000 driver operates in pseudo-DMA mode. For all other values, TI2000 drivers operate in bus master DMA mode.

Bits 04–07: INT. The four INT bits indicate the interrupt level. At reset, these bits are set to 0x0. They are read-only bits and they echo the least significant four bits of the interrupt line register.

Bits 08–09: Speed and topology. These bits are echoed in bits 8–9 of the TI2000 configuration register (see Table 6). At reset, these bits are set to 0x1 (Token Ring 16 Mbps).

Table 6. Speed and Topology Bits

SPEED BIT 9	TOPOLOGY BIT 8	DESCRIPTION
0	0	Full-duplex Ethernet®
1	0	Ethernet
0	1	Token Ring 16 Mbps
1	1	Token Ring 4 Mbps

Ethernet is a registered trademark of Xerox Corporation.

miscellaneous control register (MISCCTRL) — configuration space DWORD address (0x40) (continued)

Bit 10: Connector. The Connector bit indicates the type of connector in use. The value of this bit is present on pin DB9/$\overline{\text{UTP}}$ of the TI380PCIA. TI2000 drivers do not use this bit currently. However, it must always be read as 0 if it is not implemented in adapter logic. Upon reset, this bit is 0.

1 = D-Shell (DB9)
0 = UTP/10BaseT

Bits 11–15: Reserved. These bits are read as 0x09.

Bit 16: Sleep. Setting this bit to a 1 causes the SBCLK output from the TI380PCIA to be driven to a steady high state. The TI380PCIA's SBCLK output is used as the SBCLK input to the TI380C2x†. Holding the sleep bit high causes the TI380C2x† to suspend operations and go into power-saving mode. When this bit changes from a 1 to 0, the SBCLK returns to normal operation. This bit is set to 0 on reset.

Bit 17: Expansion ROM address mode, 14/$\overline{\text{16}}$. This bit indicates to the ROMIF that it should either use full 16-bit addressing or support the TI2000 paging protocol. When using TI2000 paging, the ROMIF uses the least significant 14 bits of the 16-bit ROM address, and the most significant two bits are provided by an internal TI380PCIA page register. This bit is set to 0x0 after reset, indicating full 16-bit mode.

Bit 18: Reserved. This bit is reserved and is set to zero during reset by the TI380PCIA. This bit is read as zero and must always be zero.

Bits 19–20: SBCLK divide ratio. These bits specify the relationship between the PCI clock and the TI380C2x† SBCLK (see Table 7). After reset, these bits are set to 0x1 (PCLK/2).

Table 7. SBCLK Divide-Ratio Bits

BIT 20	BIT 19	SBCLK FREQUENCY
0	0	PCLK/1
0	1	PCLK/2
1	0	PCLK/3
1	1	PCLK/4

Bits 21–27: Reserved

Bit 28: Address parity error. The address parity error bit is set to 1 when the TI380PCIA detects an address-parity error when acting as a PCI slave. This bit is set to 0 after reset.

Bit 29: Target-reported parity error. The target-reported parity error bit is set to 1 when the TI380PCIA receives a data-parity error (that is, it receives $\overline{\text{PERR}}$ during a master write and/or it detects a parity error during master read). This bit is set to 0 after reset.

Bit 30: Retry count expired. The retry count expired bit is set to 1 when the TI380PCIA has exceeded the maximum retry count with a master transaction. This bit is set to 0 after reset.

Bit 31: Software reset. Software reset is a programmable reset. Setting this bit to a 1 causes the $\overline{\text{SRESET}}$ output to pulse low for a minimum of 14 μs and results in a hard reset to the LAN subsystem. (This function is provided primarily for hardware and driver-software debug purposes.) This bit is set to 0 after reset. When set to 1, this bit resets itself to 0 after four PCI clock cycles.

ADVANCE INFORMATION

† TI380C3x devices can be used with TI380PCIA in the same way as TI380C2x devices.

board configuration register (board config)—configuration space DWORD address (0x44)

Figure 14 shows the board configuration register layout.

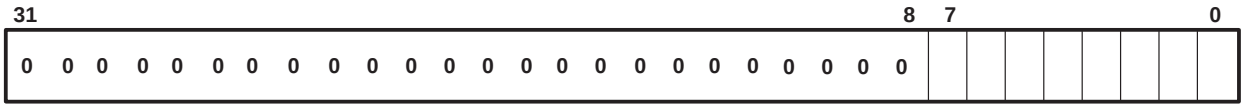

Figure 14. Board Configuration Register Layout

Bits 00–07: When $\overline{\text{RST}}$ is driven high, the value on ROMA[07:00] is latched into the board configuration register in the TI380PCIA configuration space. The value on ROMA[07:00] can be provided by pullup and pulldown resistors that do not affect operation after reset. This feature allows designers to support jumpers or board-stuffing options that can be sensed by software that reads the board configuration register. If pullup and pulldown resistors are not used, the contents of the board configuration register are undefined after reset.

Bits 08–31: These bits must read as 0.

EEPROM read/write register — configuration space DWORD address (0x48)

Figure 15 shows the layout of the EEPROM read/write register. Table 8 describes bits 4 through 8 of this register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	rsvd	rsvd	rsvd	ECR-CERR	NEP	ECLK	EEN	EDATA	rsvd	rsvd	rsvd	rsvd

rsvd = reserved

Figure 15. EEPROM Read/Write Register Layout

Table 8. EEPROM Read/Write Register Bit Descriptions

BIT NO.	BIT NAME	DESCRIPTION
8	ECRCERR	EEPROM CRC error detected. ECRCERR is normally 0 but is set to 1 if an error is detected in the CRC read from the EEPROM at power up. If this bit is set, the TI380PCIA also sets bit 7, the NEP bit.
7	NEP	EEPROM not present. NEP indicates that the EEPROM interface was disabled either by a pulldown resistor on the EDIO pin or by the detection of an error in the checksum during the EEPROM download process.
6	ECLK	EEPROM serial I/O (SIO) clock. ECLK controls the state of the EDC pin. 1 = pin high 0 = pin low
5	EEN	EEPROM enable. EEN controls the direction of the EDIO pin. When this bit is set to a 1, the EDIO pin is driven with a value in the EDATA bit.
4	EDATA	EEPROM data. EDATA is used to read or write the EDIO data pin on the EEPROM. When bit 5 is a 1, the EEPROM data pin (EDIO) is driven with the value of this bit. If bit 5 is a 0, this bit becomes a 1 because EDIO is an open-drain output.

TI380PCIA interface control register—configuration space DWORD address (0x54)

Figure 16 shows the layout of the interface control register.

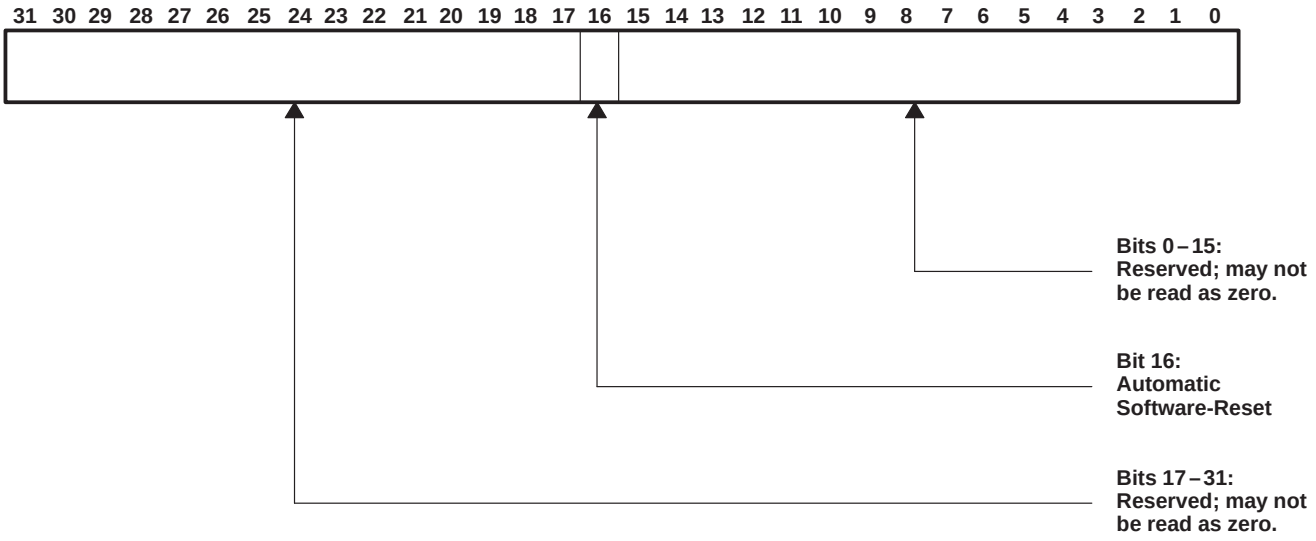

Figure 16. Interface Control Register Layout

Bits 00–15: Reserved; may not be read as zero

Bit 16: Automatic software-reset. The automatic software-reset controls the impact of writing a zero to the bus master bit (bit 2) in the TI380PCIA command register of DWORD address 0x04. When this bit is set to zero, the TI380PCIA resets itself if the host processor causes a transition from one to zero of the bus master bit. When bit 16 is set to one, the TI380PCIA does not reset itself when the host processor causes a transition from one to zero of the bus master bit.

Typically, in personal computer (PC) systems, the TI380PCIA automatic software-reset bit is set to a default value of zero. In a PC system, when a CTRL-ALT-DEL is issued from the keyboard, the PCI bus does not receive a reset. A TI380PCIA bus master in the middle of a DMA transaction when the CTRL-ALT-DEL is issued can be left in an unknown state. In this condition, the bus master could perform unexpected memory accesses to the host after the TI380PCIA device is enabled by the PCI BIOS during the boot process.

To eliminate this problem, the automatic software-reset bit must be left set to the default value of zero. The action of clearing the bus master bit in the TI380PCIA control register (which is a direct consequence of issuing the CTRL-ALT-DEL) also automatically resets the TI380PCIA and clears any pending DMA transactions. The reset induced by clearing the TI380PCIA bus master bit is the same as the software-reset that takes place when bit 31 of the TI380PCIA MISCCTRL register is set to a one.

Bits 17–31: Reserved; may not be read as zero

TI2000 configuration register

The configuration register is defined in I/O space at offset 0xE–0xF from the I/O base address (given in BASE0).

Figure 17 shows the layout of the TI2000 configuration register.

15	14	13	12	11	10	9	8	7 – 4	3 – 0
Config	rsvd	rsvd	DEDMACTL	INST8	Connector	Speed	Topology	INT	DMA

rsvd = reserved

Figure 17. TI2000 Configuration Register Layout

TI2000 configuration register (continued)

This is a read-only register with the following functions:

Bits 00–03: DMA. The four DMA bits indicate the DMA channel. At reset, these bits are 0x0. They are used by TI2000-compatible software. The channel number has no meaning in terms of PCI bus DMA. However, TI2000 drivers read this field. If it is set to 0xF, they operate in pseudo-DMA mode (see Table 9). Any other value allows TI2000 drivers to use PCI DMA operation.

Table 9. DMA Bit Indicating DMA Channel Selection

3	2	1	0	DMA CHANNEL
0	0	0	0	DMA bus master
0	0	0	1	DMA bus master
0	0	1	0	DMA bus master
.	.	.	.	DMA bus master
1	1	1	1	Pseudo-DMA operation

Bits 04–07: INT. The four INT bits indicate the interrupt level as shown in Table 10. At reset, these bits are set to 0x0. These bits echo the four LSBs of the interrupt line register.

Table 10. Interrupt Level of INT Bits 4–7

7	6	5	4	INTERRUPT LEVEL
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
.	.	.	.	...
1	1	1	1	15

Bit 08: Topology. Indicates whether the driver must initialize token-ring or Ethernet operation.

TI2000 drivers interpret the speed and topology bits together to determine whether to initialize the adapter under 4- or 16-Mbps token-ring, or 10-Mbps Ethernet operation (see Table 11).

Bit 09: Speed. Indicates whether the driver must initialize 4- or 16-Mbps Token-Ring Network™ operation. See topology bit (bit 8).

These two bits echo bits 8 and 9 in the MISCCTRL register.

Table 11. Token-Ring/Ethernet Initialization

SPEED BIT 9	TOPOLOGY BIT 8	DESCRIPTION
0	0	Reserved
1	0	Ethernet
0	1	Token Ring, 16 Mbps
1	1	Token Ring, 4 Mbps

Bit 10: Connector. The Connector bit indicates the type of connector in use. TI2000 drivers do not currently use this bit; however, it must always be read as 0 if it is not implemented in adapter logic. The value of this bit is presented on pin DB9/$\overline{\text{UTP}}$ of the TI380PCIA. Upon reset, this bit is 0. This bit echoes bit 10 of the MISCCTRL register.

1 = D-Shell (DB9)
0 = UTP/10BaseT

Token-Ring Network is a trademark of International Business Machines Corporation.

TI2000 configuration register (continued)

Bit 11: INST8. This bit indicates whether the driver can use 16-bit instructions to access adapter registers. It is hardwired to 0 because PCI-based machines are able to perform 16-bit instructions.

1 = The TI2000 driver must use 8-bit instructions to access the LAN adapter registers.
0 = The TI2000 driver can use 16-bit instructions to access the LAN adapter registers.

Bit 12: DEDMACTL. The Don't Enable ISA DMA Controller (DEDMACTL) bit indicates whether the TI2000 driver must enable the ISA DMA controller (see Table 12). The ISA DMA controller is not used to control operations on the PCI bus. To allow the TI2000 software specification to be expanded to comprehend the PCI bus, this bit is hardwired to a 1 to indicate that a TI2000 driver controlling a PCI-based network interface card should not enable an ISA DMA controller. (The setting of this bit does not affect DMA on the PCI bus.)

Table 12. ISA DMA Controller Settings

DMA MODE	DEDMACTL BIT VALUE
DMA	1 = Driver must NOT enable ISA DMA controller
DMA	0 = Driver must enable ISA DMA controller
PDMA	x = Driver must NOT enable ISA DMA controller

Bits 13–14: Reserved. These bits must be read as 0.

Bit 15: Config. The MSB of the configuration register, when set, indicates the existence of the configuration register. This bit is hardwired to 1 to indicate the presence of a configuration register.

CONFIG = 1 There is a configuration register.
CONFIG = 0 There is no configuration register.

silicon errata

A description of known silicon errata for TI380PCIA devices stamped with the identifier "TI380PCIAPCM" follows.

ID 380PCI20001—description

When the TI380PCIA is DMAing data to or from host memory, there is a very narrow window during which back-to-back DIO reads or writes initiated by the host may conflict with the DMA. When the TI380PCIA is DMAing data between host memory and the TI380C2x†, if the host initiates a DIO access to the TI380PCIA, then the TI380PCIA issues a retry to the host. The TI380PCIA then halts the DMA transfer between the TI380C2x† and the TI380PCIA. When the host retries the DIO access, it is allowed to complete successfully and the TI380PCIA then permits the pending DMA to restart. If the host attempts a second DIO access within one PCI cycle of completion of the successful DIO access (that is, if the host asserts the PCI bus $\overline{\text{FRAME}}$ signal one PCI cycle after the completion of the previous successful DIO), then the second DIO access conflicts with the restarting of the DMA, resulting in a data corruption of the DIO. In such a case, the second DIO read or write data is replaced with the DMA address. Note that after the conflict, the DMA resumes successfully.

ID 380PCI20001—work-arounds

- Establish a handshake within driver software such that DIO accesses cannot take place during DMA transfers.

or

- Ensure that back-to-back DIO accesses never take place within one PCI clock cycle.

† TI380C3x devices can be used with TI380PCIA in the same way as TI380C2x devices.

ID 380PCI20002—description

When the TI380PCIA is requesting mastership of the PCI bus for a multicycle access prior to gaining control of the PCI bus, the TI380PCIA may misinterpret assertion of the PCI $\overline{\text{STOP}}$ signal, destined for another target on the PCI bus, and temporarily deassert its PCI $\overline{\text{REQ}}$ signal. The TI380PCIA reasserts the $\overline{\text{REQ}}$ signal when $\overline{\text{STOP}}$ is deasserted. The deassertion of the $\overline{\text{REQ}}$ signal does not impact data integrity, but may slightly increase the time taken for the TI380PCIA to achieve master control of the PCI bus. (After the TI380PCIA gains control of the PCI bus, the master transaction completes without further disruption.) The impact of this behavior is system-specific and depends upon the level of activity on the PCI bus $\overline{\text{STOP}}$ signal.

ID 380PCI20003—description

If the TI380PCIA experiences a soft reset due to a one-to-zero transition on the bus master bit (bit 2 of the command register), or setting the software reset bit in the MISCCTRL register, the contents of the MIN_GNT or MAX_LAT configuration registers are reset from the values loaded in from the serial EEPROM to the hardwired default values for these registers. Note that host software can read the values for the MIN_GNT and MAX_LAT registers that are stored in the EEPROM by means of the EEPROM interface register in TI380PCIA configuration space, but these values cannot be written into the MIN_GNT and MAX_LAT registers by the host because the two registers are defined as read-only configuration registers. Certain PCI BIOS software may cause the TI380PCIA to perform a soft reset after power-up during the operating system boot process. In the systems, the values in the MIN_GNT and MAX_LAT registers always appear to be the hardwired default values.

ID 380PCI20003—work-arounds

The contents of the MIN_GNT and MAX_LAT registers can be restored by asserting the TI380PCIA's PCI reset pin ($\overline{\text{RST}}$), which causes the TI380PCIA to reload the contents of the EEPROM.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 2) . . . . . 7 V
Input voltage range (see Note 2) . . . . . – 0.3 V to 20 V
Output voltage range . . . . . – 2 V to 7 V
Power dissipation . . . . . 0.8 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	High-level DC input voltage (TTL)‡	2		V_{CC}	V
V_{IL}	Low-level DC input voltage (TTL)‡	0		0.8	V
t_t	Input transitions (t_r and t_f, 10% to 90%)	0		25	ns
V_O	Output voltage§	0		V_{CC}	V
T_A	Operating free-air temperature range	0		70	°C

‡ Applies for external input buffers without hysteresis
§ Applies for external output buffers

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS (SEE NOTE 3)	MIN	MAX	UNIT
V_{OH}	High-level output voltage, TTL-level signal (see Note 4)	V_{DD} = MIN, I_{OH} = MAX	2.4		V
V_{OL}	Low-level output voltage, TTL-level signal	V_{DD} = MIN, I_{OL} = MAX		0.6	V
I_{OZ}	High-impedance output current	V_{DD} = MAX, V_O = 2.4 V V_{DD} = MAX, V_O = 0.4 V		20 –20	µA
I_I	Input current, any input or input/output pin	V_I = V_{SS} to V_{DD}		± 20	µA
I_{DD}	Supply current	V_{DD} = MAX		200	mA
C_i	Input capacitance, any input	f = 1 MHz, other pins at 0 V		15	pF
C_o	Output capacitance, any output or input /output	f = 1 MHz, other pins at 0 V		15	pF

NOTES: 3. For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions.
4. The following signals require an external pullup resistor: $\overline{SAS}$, $\overline{SDTACK}$, $\overline{SUDS}$, $\overline{SLDS}$.

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PARAMETER MEASUREMENT INFORMATION

Outputs are driven to a minimum high-logic level of 2.4 V and to a maximum low-logic level of 0.6 V. These levels are compatible with TTL devices.

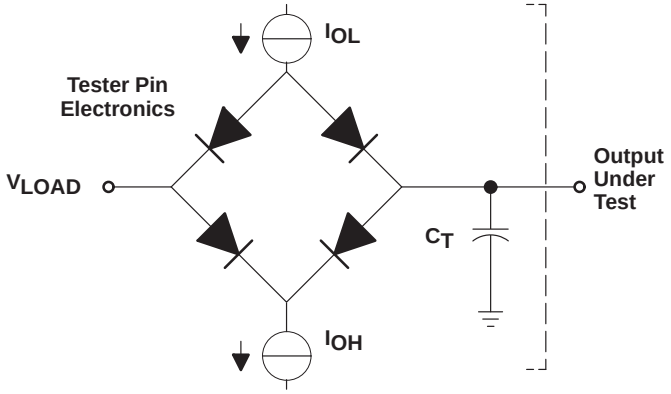
Output transition times are specified as follows: For a high-to-low transition on either an input or output signal, the level at which the signal is said to be no longer high is 2 V, and the level at which the signal is said to be low is 0.8 V. For a low-to-high transition, the level at which the signal is said to be no longer low is 0.8 V, and the level at which the signal is said to be high is 2 V, as shown in Figure 18.

The rise and fall times are not specified but are assumed to be those of standard TTL devices, which are typically 1.5 ns.

Figure 18. Output Transition Levels

test measurement

The test load circuit shown in Figure 19 represents the programmable load of the tester pin electronics used to verify timing parameters of TI380PCIA output signals.



Where: I_{OL} = 2.0 mA DC-level verification (all outputs)
I_{OH} = 400 µA (all outputs)
V_{LOAD} = 1.5 V typical DC-level verification
0.7 V typical timing verification
C_T = 65 pF typical load circuit capacitance and includes probe and jig capacitance

Figure 19. Test Load Circuit

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PARAMETER MEASUREMENT INFORMATION

measure and test condition parameters (see Figure 20 and Figure 21)

SYMBOL	5-V SIGNALING	UNITS
V_{th}	2.4	V
V_{tl}	0.4	V
V_{test}	1.5	V
V_{max}	2.0	V
Input signal edge rate	1	V/ns

timing requirements (5-V signaling environment) (see Figure 20 and Figure 21)

		MIN	MAX	UNIT
t_{val}	CLK to signal valid delay-bused signals (see Notes 5, 6, 7, 8)	2	11	ns
$t_{val(ptp)}$	CLK to signal valid delay-point-to-point (see Notes 5, 6, 7)	2	12	ns
t_{on}	Float-to-active delay (see Note 5)	2		ns
t_{off}	Active-to-float delay (see Note 5)		28	ns
t_{su}	Input setup time to CLK-bused signals (see Notes 7, 9)	7		ns
$t_{su(ptp)}$	Input setup time to CLK-point-to-point (see Notes 7, 9)	10		ns
t_h	Input hold time from CLK (see Notes 9, 10)	3		ns
t_{rst}	Reset active time after power stable (see Note 11)	1		ms
$t_{rst-clk}$	Reset active time after CLK stable (see Note 9)	100		µs
$t_{rst-off}$	Reset active to output float delay (see Notes 9, 12)		40	ns

NOTES:
5. See timing measurement conditions in the Output Timing Measurement Conditions diagram of the PCI Specification 2.0.
6. Minimum times are measured with 0 pF equivalent load; maximum times are measured with 50 pF equivalent load. Actual test capacitance can vary, but results should be correlated to these specifications.
7. $\overline{REQ}$ and $\overline{GNT}$ are point-to-point signals and have different output valid delay and input setup times, respectively, than do bused signals. $\overline{GNT}$ has a setup time of 10 ns; $\overline{REQ}$ has an output valid delay time of 12 ns. All other signals are bused.
8. The maximum value of t_{val} for the $\overline{STOP}$ signal is 12 ns. PCI Specification Revision 2.0 defines a maximum value of 11 ns. No system-related problems have been attributed to this exception to electrical timing defined in the PCI Specification.
9. See timing measurement conditions in the Input Timing Measurement Conditions diagram of the PCI Specification 2.0.
10. The minimum hold time for all TI380PCIA inputs is 3 ns. PCI Specification Revision 2.0 defines a minimum input hold time of 0 ns. No system-related problems have been attributed to this exception to electrical timing defined in the PCI Specification.
11. $\overline{RST}$ is asserted and deasserted asynchronously with respect to CLK. Refer to PCI Specifications 2.0 for more information.
12. All output drivers must be floated when $\overline{RST}$ is active.

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PARAMETER MEASUREMENT INFORMATION (CONTINUED)

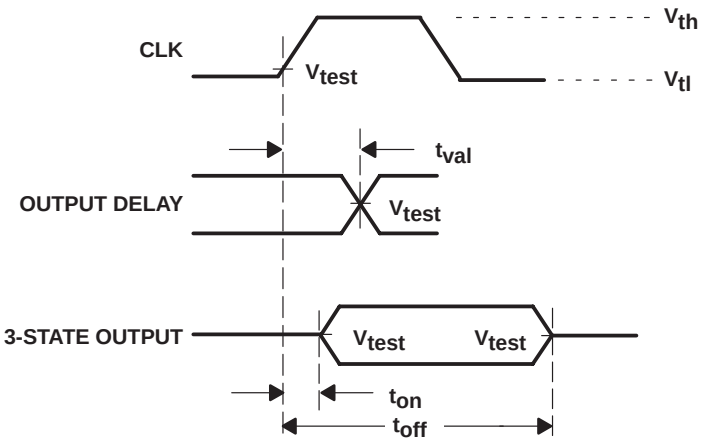

Figure 20. Output Timing Measurement Conditions

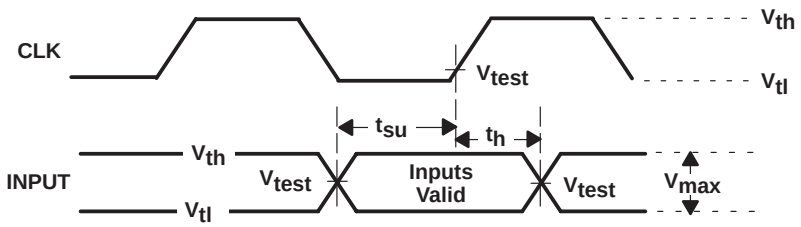

Figure 21. Input Timing Measurement Conditions

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ac characteristics for serial EEPROM interface over recommended ranges of supply voltage and operating free-air temperature (see Figure 22)

PARAMETER		ALT	MIN	MAX	UNIT
t_{CH1CH2}	Rise time, clock	t_R		1	µs
t_{CL1CL2}	Fall time, clock	t_F		300	ns
t_{DH1DH2}	Rise time, input	t_R		1	µs
t_{DL1DL2}	Fall time, input	t_F		300	ns
t_{CHDX}	Setup time, clock high to input transition (see Note 13)	$t_{SU:STA}$	4.7		µs
t_{CHCL}	Pulse duration, clock high	t_{-HIGH}	4		µs
t_{DLCL}	Input low to clock low (START)	$t_{HD:STA}$	4		µs
t_{CLDX}	Clock low to input transition	$t_{HD:DAT}$	0		µs
t_{CLCH}	Pulse duration, clock low	t_{LOW}	4.7		µs
t_{DXCX}	Input transition to clock transition	$t_{SU:DAT}$	250		ns
t_{CHDH}	Clock high to input high (STOP)	$t_{SU:STO}$	4.7		µs
t_{DHDL}	Input high to input low (bus-free)	t_{BUF}	4.7		µs
t_{CLQV}	Clock low to output valid	t_{AA}	0.3	3.5	µs
t_{CLQX}	Clock high to output transition	t_{DH}	300		ns
f_C	Clock frequency	f_{SCL}		100	kHz
t_{LPF}	Input low pass first order filter time constant (SCL and SDA inputs)	T_I		100	ns
t_W	Write time (see Note 14)	t_{WR}		10	ms

NOTES: 13. For a restart condition, or following a write cycle
14. In the multibyte write mode only, if accessed bytes are on two consecutive rows (upper 5 MSB must not change), the maximum programming time is doubled to 20 ms.

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PARAMETER MEASUREMENT INFORMATION

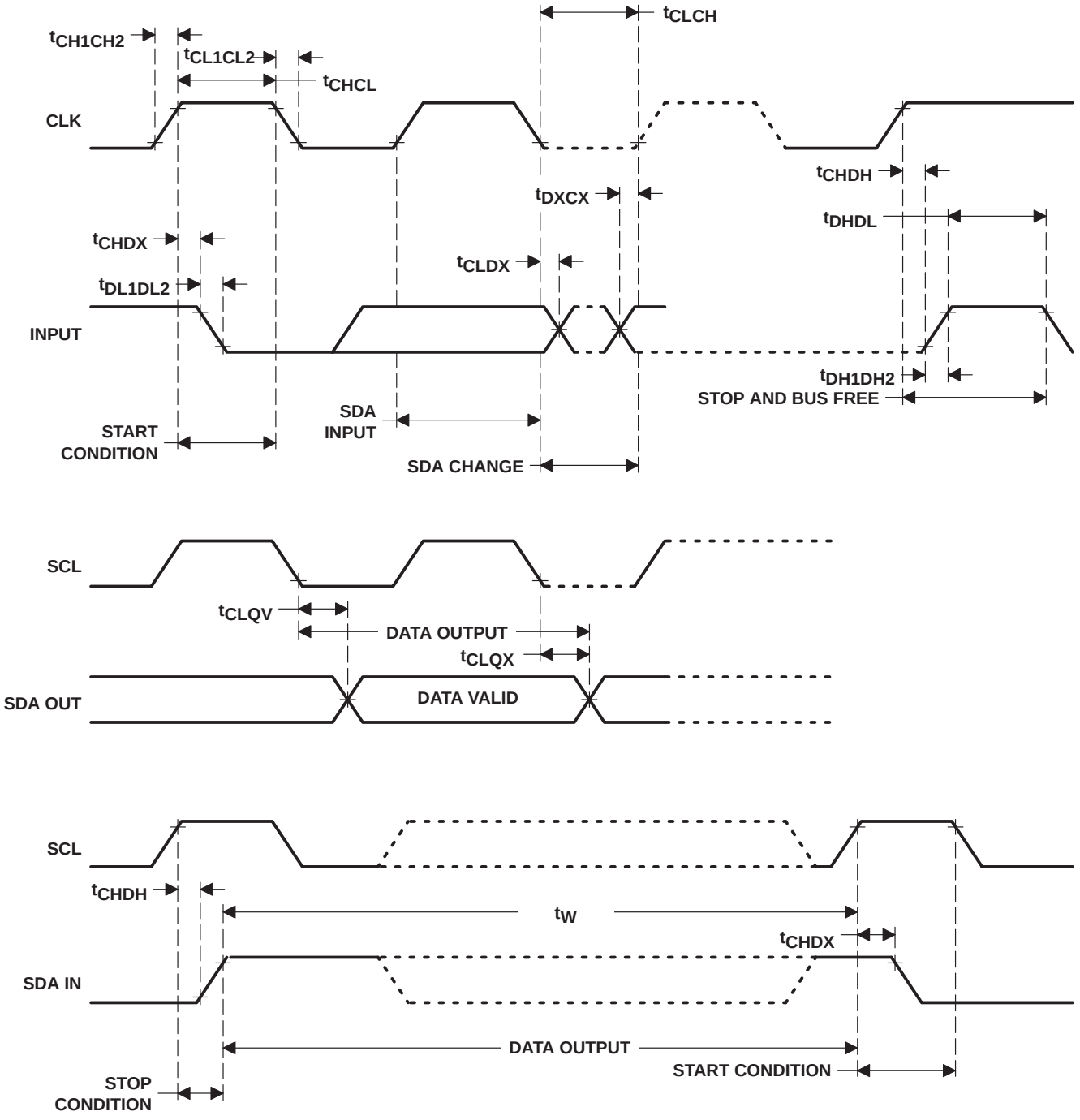
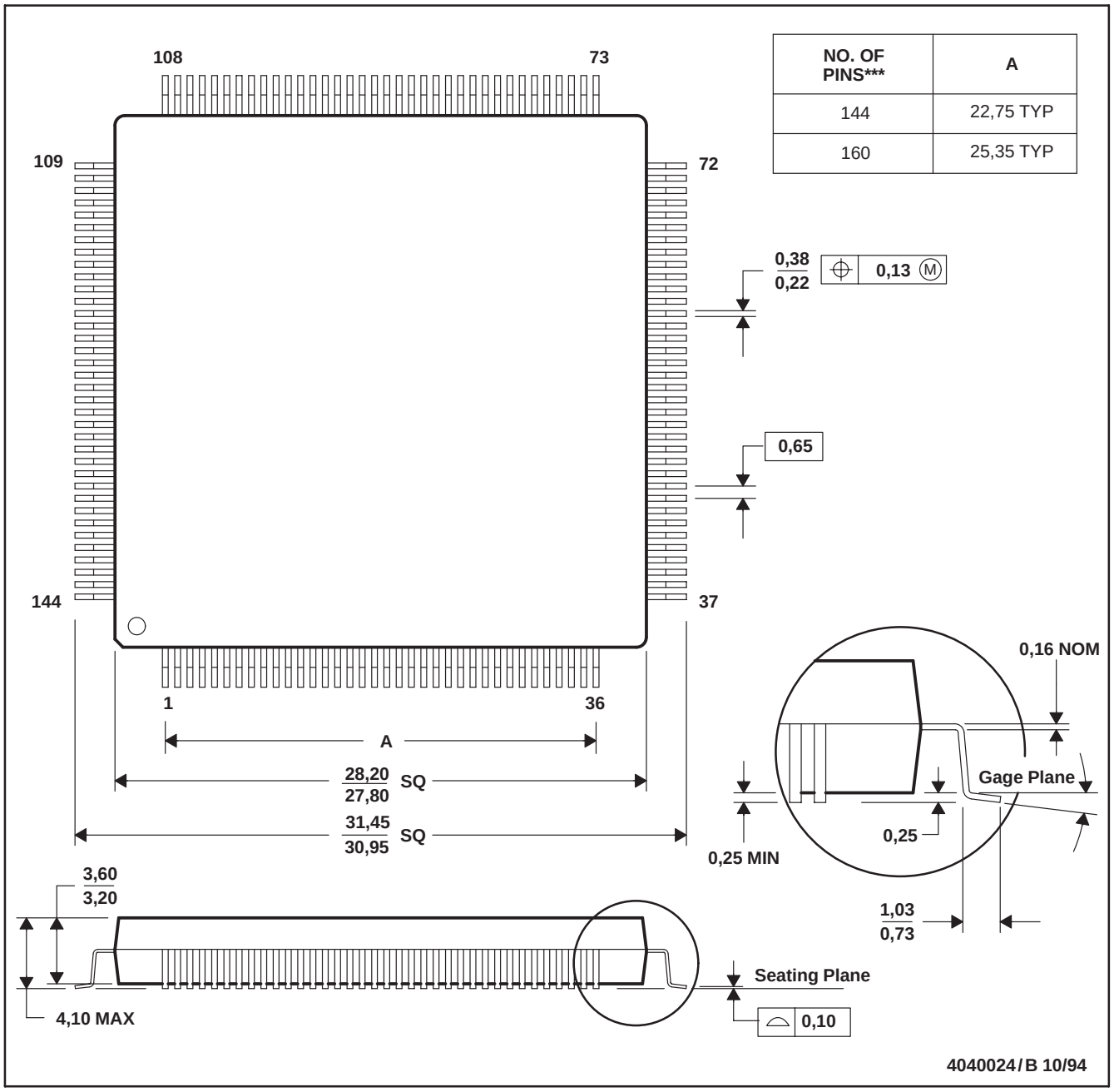


Figure 22. AC Waveforms for Serial EEPROM Interface

MECHANICAL DATA

PCM (S-PQFP-G*)** **PLASTIC QUAD FLATPACK**

144 PIN SHOWN



NO. OF PINS***	A
144	22,75 TYP
160	25,35 TYP

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-022
D. The 144 PCM is identical to the 160 PCM except that four leads per corner are removed.

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