System Engineering Notes
No. 896
Differences Between the SYM53C896 and SYM53C895
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SYMBIOS LOGIC

Functional Differences

This section describes differences in the functionality between the SYM53C896 and the SYM53C895.

Multi_channel

The SYM53C896 has two wide Ultra2 SCSI channels in a single package, each functioning like the SYM53C895. Channel A and Channel B each has its own register set, an independent 944 byte DMA FIFO, its own interrupt signals and a separate internal 8KB SCRIPTS RAM. Each function has its own separate PCI configuration space.

Phase Mismatch Handling

The SYM53C896 can handle phase mismatches due to drive disconnects without having to interrupt the host processor. The primary goal of this logic is to completely eliminate the need for CPU intervention during an IO disconnect/reselect sequence. Storing the appropriate information to later restart the IO can be done through SCRIPTS, eliminating the need for processor intervention during an IO disconnect/reselect sequence. Calculations are performed such that the appropriate information is available to Scripts so that an IO's state can be properly stored for restart later. The logic powers up disabled and can be enabled by setting the Phase Mismatch Jump Enable bit (ENPMJ, bit 7 in the CCNTL0 register). By utilizing the information supplied in the Phase Mismatch registers, which are described later in this document, all overhead involved in a disconnect/reselect sequence can be handled with a modest amount of Script instructions.

64-bit Operation

The SYM53C896 has a 64 bit PCI interface which provides 64-bit address and data capability in the initiator mode. The chip can also respond to 64-bit addressing in the target mode. DACs (Dual Address Cycle) can be generated for all SCRIPTS operations. There are six selector registers that hold the upper dword of a 64-bit address. All but two of these are static and require manual loading via a CPU access, a load/store instruction, or a memory move instruction. The DBMS (Dynamic Block Move Selector) register is dynamic and is used during 64-bit direct block moves only. The SFS (Script Fetch Selector) will be reloaded when a 64-bit jump is executed. All selectors will default to zero, meaning the 896 will power up in a state where only SACs (Single Address Cycles) will be generated. When any of the selector registers are written to a non-zero value, DACs will be generated. Direct, table indirect and indirect block moves, memory to memory moves, load/stores, and jumps are all instructions with 64-bit address capability. Crossing the 4GB boundary on any one SCRIPTS operation is not permitted and S/W needs to take care that any given SCRIPTS operation will not cross the 4GB boundary.

8K SCRIPTS RAM For Each SCSI Channel

The SYM53C896 contains an 8KB internal SCRIPTS RAM for each SCSI channel.

32 Bit ISTAT Register

The SYM53C896 has a 32 bit ISTAT register. The SYM53C895 has one byte in the ISTAT register. In ISTAT1, bit 0 provides a means to disable the interrupt for either channel while SCRIPTS are running. Bit 1 indicates if SCRIPTS are running, and bit 2 allows monitoring if the chip is currently flushing data. Additionally, there are two mailbox bytes, MBOX0 and MBOX1, that contain general purpose bits that can be read from or written to by either the system CPU or the SCRIPTS engine while SCRIPTS are running. The mailbox bits are one way only per byte lane. If reading MBOX1, bit 0, do not write to MBOX1, bit 4. The host and the SCRIPTS processor (53C896) could potentially attempt to access a mailbox byte at the same time. Using one mailbox register as a read only and the other as a write only will prevent this type of conflict from occurring.

JTAG

The SYM53C896 has JTAG boundary scan testing which complies with the IEEE 1149.1 standard.

H/W Control of Activity LED

The SYM53C896 has the ability to control a LED through the GPIO_0 pin to indicate that it is connected to the SCSI bus. Formerly this function was done by a S/W driver. When bit 5 (LED_CNTL) in the General Purpose Control (GPCNTL) register is set, and bit 6 (Fetch Enable) in the GPCNTL register is cleared, and the 53C896 is not performing an EEPROM auto-download, then bit 3 (CON) in the ISTAT register will be presented at the GPIO_0 pin. The CON (Connected) bit in ISTAT0 will be set anytime the 53C896 is connected to the SCSI bus either as the initiator or the target. This will happen after the 53C896 has successfully completed a selection or when it has successfully responded to a selection or reselection. It will also be set when the 53C896 wins arbitration in the low level mode.

PC97 Power Management

The SYM53C896 will support PC97 Power Management, including Subsystem Vendor ID/Subsystem ID Download and PCI Power Management.

The Subsystem Vendor ID/Subsystem ID Auto-download is used to differentiate board vendors from silicon vendors. Downloading from a serial EEPROM is the recommended implementation. Values must be populated before the system OS or BIOS accesses the PCI Configuration Space.

PCI Power Management levels are defined by bus and device class. These are supported through the Extended Capabilities Register at offset 34h. This register contains a pointer to a linked list that resides at address 40h and contains information on the chip's power management states. See the configuration space register descriptions for more information.

Alternate Interrupt Routing

The SYM53C896 supports an alternate interrupt signal for each SCSI function so that function A has INTA and ALT_INTA interrupt output pins and function B has INTB and ALT_INTB interrupt output

pins. The interrupt direction pin, INT_DIR, will allow all interrupts through when high, or will allow only alternate interrupts through when it is low. The alternate interrupts can be routed away from the PCI bus to be handled by another processor, i.e., i960. The INT_DIR pin is pulled high internally.

All four interrupt outputs can be routed to the INTA pin if the MAD4 pin is pulled up external to the chip. If this is the case, SCSI function B interrupt requests will appear on the INTA pin instead of on the INTB pin. Another result of the MAD4 pin being pulled high is that the SCSI function B Interrupt Pin register in PCI configuration space will contain 01h instead of 02h. When MAD4 is allowed to be pulled low internally, the default mode, SCSI function A interrupts are routed to the INTA pin and SCSI function B interrupts are routed to the INTB pin.

One possible way to implement the interrupt routing follows:

1) MAD4: no connections (pulled down internally).
This will allow interrupts from SCSI channel A to be routed to INTA/ (ALT_INTA/) while interrupts from SCSI channel B are routed to INTB/ (ALT_INTB/).

2) INT_DIR: connect to TDI of the RAID upgradable PCI slot (no other connections to this signal).
This will allow INTA/ and INTB/ to be disabled when a RAID upgrade card is present in the RAID upgradable PCI slot. An internal pull-up on INT_DIR keeps INTA/ and INTB/ enabled when a RAID upgrade card is not present. This assumes that TDI is pulled low on the RAID upgrade card.

3) INTA/: connect to the INTC/ of all PCI slots except the RAID upgradable PCI slot.

4) INTB/: connect to the INTD/ of all PCI slots except the RAID upgradable PCI slot.
When a RAID upgrade card is not present, INTA/ and INTB/ are enabled, so connections 3 and 4 will allow these interrupts to be serviced by the host CPU. When an upgrade card is present, INTA/ and INTB/ are disabled.

5) ALT_INTA/: connect to INTC/ of the RAID upgradable PCI slot (no other connections to this signal).

6) ALT_INTB/: connect to INTD/ of the RAID upgradable PCI slot (no other connections to this signal).
When a RAID upgrade card is present, these connections will allow interrupts from the SYM53C896 to be routed to the RAID upgrade card.

This scheme would allow a Symbios HBA to take over the baseboard SCSI channels. The upgradable PCI slot, if not populated with a RAID upgrade, remains available to receive a generic PCI card whose PCI interrupt resource needs are limited to INTA/ and INTB/.

Duplicate REQ/ACK Pair

The SYM53C896 supplies a duplicate SCSI REQ/ACK pair for each SCSI channel. These are enabled when the MAD6 and MAD5 pins are pulled high external to the chip. Duplicate SREQ/ and SACK/ may be used to provide extra drive for backplane applications.

Improved PCI Caching Ability

The SYM53C896 contains an improved cache block which replaces the cache block that was used in the SYM53C895. The new cache block design results in improved PCI bus efficiency by reducing the

number of times the SCSI processor gets on and off the bus for alignment. With the new cache block design, no cache alignment is done during PCI read cycles, but a determination of the appropriate cache read command is done based on the programmed burst size, current address, cache line size and data transfer length. PCI reads are not throttled, but are always a full burst length as programmed in the DMODE register, with the appropriate Read command (Memory Read, Memory Read Multiple or Memory Read Line) being generated. Writes are still aligned in order to issue Write and Invalidate commands, but the alignment will be one burst length in size until the end of any given data transfer. While the data transfer is continuing, Write and Invalidate commands will continue until the byte count is below a Write and Invalidate threshold. Then a single write burst will be issued to complete the data transfer. The general pattern is: single data alignment write, multiple Write and Invalidates, a single data residual write.

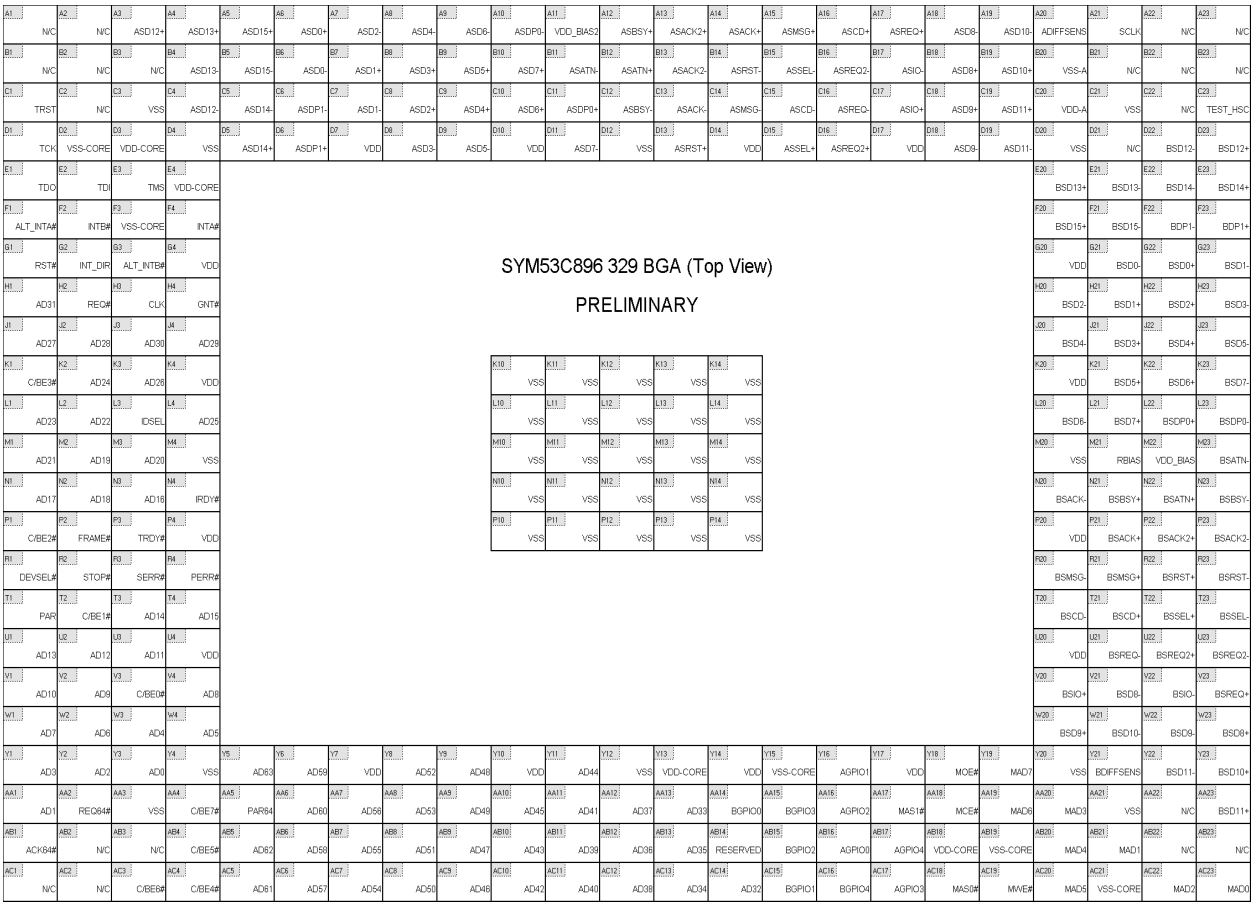
Memory to Memory moves are also supported by the PCI cache commands described above, with one limitation: Write and Invalidate on Memory to Memory move writes are only supported if the source and destination address are quad word aligned. If source and destination addresses are not quad word aligned, where source address 2-0 = destination address 2-0, no write aligning is performed, nor will Write and Invalidate commands be issued.

The new cache block also supports issuing cache commands while pre-fetching SCRIPTS instructions. However, burst opcode on normal non-burst SCRIPTS fetches are not supported with cache commands. Only standard PCI reads will be issued.

Existing enable bits in the SCSI core are still used to control cache alignment operations and issuing the various PCI commands.

Rerouting of SCRIPTS RAM Load/Store Data

Load/Store data transfers to or from SCRIPTS RAM remain internal to the SYM53C896 and will not generate PCI cycles. While a Load/Store transfer to or from SCRIPTS RAM is occurring, any external (PCI) slave cycles that occur to the SCSI core are retried on the PCI bus. This feature can be disabled by setting the DISINTLS bit in CCNTL1.



SYM53C896 Pin Diagram (329 BGA)

Operating Register/Bit Differences

The register differences between the SYM53C896 and the SYM53C895 are related to the new features available in the SYM53C896. SCSI operating registers are not accessible through the PCI Configuration Space.

ISTAT1 (15h) - Interrupt Status 1

Bit 2 FLUSHING

Reading this bit monitors if the chip is currently flushing data. If set, the chip is flushing data from the DMA FIFO. If cleared, no flush is occurring. This bit is read only.

Bit 1 SCRIPTS RUNNING

Reading this bit monitors if the SCRIPTS engine is currently fetching and executing instructions. If set, the SCRIPTS engine is active. If cleared, the SCRIPTS engine is not currently active. This bit is read only.

Bit 0 SYNC_IRQD

Setting this bit disables the INTA/ pin for Function A and the INTB/ pin for Function B. Clearing this bit enables normal operation of the INTA/ (or INTB/) pin. The function of this bit is nearly identical to bit 1 of DCNTL (Reg 3B) except that if INTA/ (or INTB/) is already asserted and this bit is set, the INT will remain asserted until the interrupt is serviced. At this point the INT line will be blocked for future interrupts until this bit is cleared. In addition, this bit may be read from and written to while SCRIPTS are executing.

MBOX0 (16h) - MAILBOX 0

Bits 7-0 MAILBOX

These are general purpose bits that may be read or written while SCRIPTS are running. They also may be read or written by the SCRIPTS processor.

MBOX1 (17h) - MAILBOX 1

Bits 7-0 MAILBOX

These are general purpose bits that may be read or written while SCRIPTS are running. They also may be read or written by the SCRIPTS processor.

Note: Mailbox bits are one way only per byte lane. For example, if reading MBOX1, bit 0, do not attempt to write to MBOX1, bit 4 at the same time. The host and SCRIPTS processors could potentially attempt to access a mailbox byte at the same time. It is suggested to use one mailbox register as a read only and the other as a write only to prevent this type of conflict from occurring.

CTEST0 (18h) - Chip Test 0

Bits 7-0 FMT7-0 (Byte empty in DMA FIFO)

These bits identify the bottom bytes in the DMA FIFO that are empty. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is empty, then FMT3 will be set. Since the FMT flags indicate the status of bytes at the bottom of the FIFO, if all FMT bits are set, the DMA FIFO is empty.

CTEST1 (19h) - Chip Test 1

Bits 7-0 FFL7-0 (Byte full in DMA FIFO)

These status bits identify the top bytes in the DMA FIFO that are full. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is full then FFL3 will be set. Since the FFL flags indicate the status of bytes at the top of the FIFO, if all FFL bits are set, the DMA FIFO is full.

CTEST2 (1Ah) - Chip Test 2

Bit 3 PCICFGEN (PCI Configuration Info Enable)

This bit controls the shadowing of the PCI RAM base address, PCI Memory register base address, PCI Device ID, and PCI Revision ID into the SCRATCHA, MMRS, SCRATCHB, MMWS, and SFS registers. When it is set, MMWS contains bits 63-32 and SCRATCHB contains bits 31-0 of the RAM base address value from the PCI configuration RAM Base Address register. This is the base address for the internal 8 KB internal RAM. MMRS contains bits 63-32 and SCRATCHA contains bits 31-0 of the memory-mapped operating register base address. Bits 23-16 of SFS contain the PCI Revision

ID Register value and bits 15-0 contain the PCI Device ID register value. When this bit is set, only reads to these registers are affected. Writes will pass through normally. When this bit is clear, the SCRATCHA, MMRS, SCRATCHB, MMWS, and SFS registers return to normal operation.

Note: Bit 3 is the only writable bit in this register. All other bits are read only. When modifying this register, all other bits must be written to zero. Do not execute a Read-Modify-Write to this register.

CTEST4 (21h) - Chip Test 4

Bit 6 FBL3 (FIFO Byte Lane 3)

See the definition of FBL(2-0) in bits (2-0) of CTEST4.

Bit 2-0 FBL2-FBL0 (FIFO Byte Lane Control)

FBL3 (bit 6)	FBL2	FBL1	FBL0	DMA FIFO Byte lane	Pins
0	X	X	X	Disabled	n/a
1	0	0	0	0	D(7-0)
1	0	0	1	1	D(15-8)
1	0	1	0	2	D(23-16)
1	0	1	1	3	D(31-24)
1	1	0	0	4	D(39-32)
1	1	0	1	5	D(47-40)
1	1	1	0	6	D(53-48)
1	1	1	1	7	D(63-54)

These bits steer the contents of the CTEST6 register to the appropriate byte lane of the 64-bit DMA FIFO. If the FBL3 bit is set, then FBL2, FBL1 and FBL0 determine which of eight byte lanes can be read or written. When FBL3 is cleared, the byte lane read or write is determined by the current contents of the DNAD and DBC registers. Each of the eight bytes that make up the 64-bit DMA FIFO can be accessed by writing these bits to the proper value. For normal operation, FBL3 must equal zero.

CTEST5 (22h) - Chip Test 5

Bit 5 DFS (DMA FIFO Size)

This bit controls the size of the DMA FIFO. When this bit is cleared, the DMA FIFO will appear to be only 112 bytes deep. When set, the DMA FIFO size will increase to 944 bytes. Using a 112-byte FIFO allows software written for other SYM53C8XX family chips to be backward compatible and properly calculate the number of bytes residing in the chip after a target disconnect.

SCRATCHA (34h-37h) - Scratch A

This is a general purpose, user-definable scratch pad register. Apart from CPU access, only Register Read/Write and Memory Moves into the SCRATCH register will alter its contents. The power-up value of this register is indeterminate.

A special mode of this register can be enabled by setting the PCICFGEN bit in the CTEST2 register. If this bit is set, the SCRATCH A register returns bits 31-10 of the memory mapped operating register PCI base address in bits 31-10 of the SCRATCH A register when read, bits 9-0 of SCRATCH A will always

return zeros in this mode. Writes to the SCRATCH A register are unaffected. Resetting the PCICFGEN bit causes the SCRATCH A register to return to normal operation.

CTYPE (46h) - Chip Type

Bits 7-4 TYP3-0 (Chip Type)

These bits identify the chip type for software purposes.

NOTE: These bits no longer uniquely identify a 8XX device. These bits have been set to a value of Fh to indicate that the device should be uniquely identified by setting the PCICFGEN bit in the CTEST2 register and using the PCI Revision ID and PCI Device ID which will be shadowed in the SFS register. Any devices that contain the value Fh in this register should use this mechanism to uniquely identify the device.

Bit 3-0 Reserved

GPCNTL (47h) - General Purpose Control

Bit 5 LED_CNTL

The internally connected signal (bit 3 of the ISTAT register) will be presented on GPIO0 if this bit is set and bit 6 of GPCNTL is cleared and the chip is not in progress of performing an EEPROM auto-download. This will happen regardless of the state of Bit 0 (GPIO0_EN). This provides a hardware solution to driving a SCSI activity LED in many implementations of SYMBIOS Logic SCSI chips.

CCNTL0 (56h) - Chip Control 0

ENPMJ	PMJCTL	ENDNJ	DISFC	Reserved	Reserved	DISINTLS	DISPREQ
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 ENPMJ (Enable phase mismatch jump)

Upon setting this bit, any phase mismatches do not interrupt, but force a jump to an alternate location to handle the phase mismatch. Prior to actually taking the jump, the appropriate remaining byte counts and addresses will be calculated such that they can be easily stored to the appropriate memory location with SCRIPTS Store instruction.

In the case of a SCSI send, any data in the part will be automatically cleared after being accounted for. In the case of a SCSI receive, all data will be flushed out of the part and accounted for prior to taking the jump. However, this feature does not cover the byte that may appear in SWIDE. This byte must be flushed manually.

Bit 6 PMJCTL (Jump Control)

This bit controls which decision mechanism is used when jumping on phase mismatch. When this bit is cleared, the part will use jump address one PMJAD1 when the WSR bit is cleared, and jump address two PMJAD2 when the WSR bit is set. When this bit is set, the part will use jump address one PMJAD1 on data out (data out, command, message out) transfers and jump address two PMJAD2 on data in (data in, status, message in) transfers. Note that the phase referred to here is the

phase encoded in the block move script instruction, not the phase on the SCSI bus that caused the phase mismatch.

Bit 5 ENNDJ (Enable Jump on non-data phase mismatches)

This bit controls whether or not a jump is taken during a non data phase mismatch, i.e., message in, message out, status, or command. When this bit is cleared, jumps will only be taken on data in or data out phases and a phase mismatch interrupt will be generated for all other phases. When this bit is set, jumps will be taken regardless of the phase in the block move. Note that the phase referred to here is the phase encoded in the block move script instruction, not the phase on the SCSI bus that caused the phase mismatch.

Bit 4 DISFC (Disable Auto FIFO clear)

This bit controls whether or not the FIFO is automatically cleared during a data out phase mismatch. When set, data in the DMA FIFO as well as data in the SODL and SODR register will not be cleared after calculations on them are complete. When cleared, the DMA FIFO and SODL and SODR will automatically be cleared. This bit is for testing purposes only and should not be used during normal operation.

Bits 3-2 Reserved

Bit 1 DISINTLS (Disable Internal Load/Store)

This bit controls whether or not load/store data transfers in which the source/destination is located in SCRIPT RAM generate external PCI cycles. If cleared, load/store data transfers of this type will not generate PCI cycles, but will stay internal to the chip. If set, load/store data transfers of this type will generate PCI cycles.

Bit 0 DISPREQ (Disable Pipe Req)

This bit controls whether or not overlapped arbitration on the PCI bus is performed by asserting PCI Req/ for one SCSI function while the other SCSI function is executing a PCI cycle. If set, overlapped arbitration will be disabled and PCI Req/ will not assert during a PCI master cycle being executed by this chip.

CCNTL1 (57h) - Chip Control 1

ZMOD	Reserved	Reserved	Reserved	DISABLE_ DAC	64TIMOD	EN64TIBMV	EN64DBMV
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 ZMOD (High Impedance Mode)

Setting this bit causes the 53C896 SCSI function to place all output and bi-directional pins except MOE/_TESTOUT, into a high-impedance state. When this bit is set, the MOE/_TESTOUT pin becomes the output pin for the connectivity test of the 53C896 signals in the “AND-tree” test mode. In order to read data out of the 53C896 SCSI function, this bit must be cleared. This bit is intended for board-level testing only. Do not set this bit during normal system operation.

Bits 6-4 Reserved

Bit 3 DISABLE_DAC (Disable Dual Address Cycle)

When this bit is set, all 64-bit addressing as a master will be disabled. No Dual Address Cycles will be generated by the part. When this bit is cleared, the part will generate Dual Address Cycles based on the master operation being performed and the value of its associated selector register.

Bit 2 64TIMOD (64-bit Table Indirect indexing mode)

When this bit is cleared, bits 24-28 of the first table entry dword will select one of 22 possible selectors to be used in a BMOV operation. When this bit is set, bits 24-31 of the first table entry dword will be copied directly into DNAD64 to provide 40-bit addressing capability. This bit will only function if the EN64TIBMV bit is set.

Index Mode 0 (64TIMOD clear) table entry format:

31 29	28 24	23 0
Rsvd.	Sel Index	Byte Count
Source/Destination Address(31-0)		

Index Mode 1 (64TIMOD set) table entry format:

31 24	23 0
Src/Dest Addr(39-32)	Byte Count
Source/Destination Address(31-0)	

Bit 1 EN64TIBMV (Enable 64-bit Table Indirect BMOV)

Setting this bit enables 64-bit addressing for Table Indirect BMOVs using the upper byte (bits 24-31) of the first dword of the table entry. When this bit is clear table indirect BMOVs will use the SBMS register to obtain the upper 32 bits of the data address.

Bit 0 EN64DBMV (Enable 64-bit Direct BMOV)

Setting this bit enables the 64-bit version of a direct BMOV. When this bit is cleared, direct BMOVs will use the SBMS register to obtain the upper 32 bits of the data address.

SCRATCHC-SCRATCHR (60h-9Fh) - Scratch Registers C-R

These are general purpose user definable scratch pad registers. Apart from CPU access, only Register Read/Write, Memory Moves and Load/Stores directed at a SCRATCH register will alter its contents. The power-up values are indeterminate.

64-bit Script Selectors (A0h-BCh)

The following registers are used to hold the upper 32-bit addresses for various Script operations. When a particular type of Script operation is performed, one of the 6 selector registers below will be used to generate a 64-bit address.

If the selector for a particular device operation is zero, then a standard 32-bit address cycle will be generated. If the selector value is non-zero, then a DAC will be issued with the entire 64-bit address.

All selectors default to 0 (zero) with the exception of the 16 scratch registers, these power up in an indeterminate state and should be initialized before they are used.

All selectors can be Read/Written via Load/Store Script instructions, Memory to Memory Moves, Read/Write Script instructions, or CPU w/ SCRIPTS not running.

Crossing of selector boundaries in one memory operation is not supported.

MMRS (A0h) - Memory Move Read Selector - Read/Write

Supplies AD(63-32) during data read operations for Memory to Memory moves and Absolute address LOAD operations.

MMWS (A4h) - Memory Move Write Selector - Read/Write

Supplies AD(63-32) during data write operations during Memory to Memory moves and Absolute address STORE operations.

SFS (A8h) - Script Fetch Selector - Read/Write

Supplies AD(63-32) during Script fetches and Indirect fetches (excluding Table Indirect fetches). When PCICFGEN (bit 3 in CTEST2) is set, bits 15-0 are DeviceID, bits 23-16 are RevisionID, bits 31-24 are reserved. This register will be reloaded automatically when a 64-bit jump instruction is executed.

DRS (ACh) - DSA Relative Selector - Read/Write

Supplies AD(63-32) during Table Indirect fetches and Load/Store DSA relative operations.

SBMS (B0h) - Static Block Move Selector - Read/Write

Supplies AD(63-32) during block move operations, reads or writes. This register is static and will not be changed when a 64-bit direct BMOV is used.

DBMS (B4h) - Dynamic Block Move Selector - Read/Write

Supplies AD(63-32) during block move operations, reads or writes. This register is used only during 64-bit direct BMOV instructions and will be reloaded with the upper 32-bit data address upon execution of a 64-bit direct BMOV.

DNAD64 (B8h) - DMA Next Address 64- Read/Write

This register holds the current selector being used in a given host transaction. The appropriate selector is copied to this register prior to beginning a host transaction.

Reserved (BCh)

Phase Mismatch Jump Registers (C0h - DFh)

Eight 32-bit registers contain the byte count and addressing information required to update, direct, indirect, or table indirect BMOV instructions with new byte counts and addresses. The eight registers are described below.

All registers can be Read/Written via Load/Store Script instructions, Memory to Memory Moves, Read/Write Script instructions, or CPU w/ SCRIPTS not running.

PMJAD1 (C0h) - Phase Mismatch Jump Address 1 - Read/Write

This register contains the 32-bit address that will be jumped to upon a phase mismatch. Depending upon the state of the PMJCTL bit this address will either be used during an out bound (data out, command, message out) phase mismatch (PMJCTL = 1) or when the WSR bit is cleared (PMJCTL = 0). It should be loaded with an address of a Script routine that will handle the updating of memory data structures of the BMOV that was executing when the phase mismatch occurred.

PMJAD2 (C4h) - Phase Mismatch Jump Address 2 - Read/Write

This register contains the 32-bit address that will be jumped to upon a phase mismatch. Depending upon the state of the PMJCTL bit, this address will either be used during an in bound (data in, status, message in) phase mismatch (PMJCTL=1) or when the WSR bit is set (PMJCTL = 0). It should be loaded with an address of a Script routine that will handle the updating of memory data structures of the BMOV that was executing when the phase mismatch occurred.

RBC (C8h) - Remaining Byte Count - Read/Write

This register contains the byte count that remains for the BMOV that was executing when the phase mismatch occurred. In the case of direct or indirect BMOV instructions, the upper byte of this register will also contain the opcode of the BMOV that was executing. In the case of a table indirect BMOV instruction, the upper byte will contain the upper byte of the table indirect entry that was fetched.

In the case of a SCSI data receive, this byte count WILL reflect ALL data received from the SCSI bus, including any byte in SWIDE. There will be no data remaining in the part that must be flushed to memory with the exception of a possible byte in the SWIDE register. That byte must be flushed to memory manually in SCRIPTS.

In the case of a SCSI data send, this byte count will reflect all data sent out onto the SCSI bus. Any data left in the part from the phase mismatch will be ignored and automatically cleared from the FIFOs.

UA (CCh) - Updated Address - Read/Write

This register will contain the updated data address for the BMOV that was executing when the phase mismatch occurred.

In the case of a SCSI data receive, if there is a byte in the SWIDE register then this address will point to the location where that byte must be stored. The SWIDE byte must be manually written to memory and this address must be incremented prior to updating any Scatter Gather entry.

In the case of a SCSI data receive, if there is not a byte in the SWIDE register, then this address will be the next location that should be written to when this IO restarts. No manual flushing will be necessary.

In the case of a SCSI data send, all data sent to the SCSI bus will be accounted for and any data left in the part will be ignored and will be automatically cleared from the FIFOs.

ESA (D0h) - Entry Storage Address - Read/Write

This register's value depends on the type of BMOV being executed. The three types of BMOVs are listed below.

Direct BMOV:

In the case of a direct BMOV, this register will contain the address the BMOV was fetched from when the phase mismatch occurred.

Indirect BMOV:

In the case of an indirect BMOV, this register will contain the address the BMOV was fetched from when the phase mismatch occurred.

Table Indirect BMOV:

In the case of a table indirect BMOV, this register will contain the address of the table indirect entry being used when the phase mismatch occurred.

IA (D4h) - Instruction Address - Read/Write

This register always contains the address of the BMOV instruction that was executing when the phase mismatch occurred. This value will always match the value in the ESA except in the case of a table indirect BMOV, in which case the ESA will have the address of the table indirect entry and this register will point to the address of the BMOV instruction.

SBC (D8h) - SCSI Byte Count - Read only

This register contains the count of the number of bytes transferred to or from the SCSI bus during any given BMOV. This value is used in calculating the information placed into the RBC and UA register and should not need to be used in normal operations. There are two conditions in which this byte count will not match the number of bytes transferred exactly. If a BMOV is executed to transfer an odd number of bytes across a wide bus, then the byte count at the end of the BMOV will be greater than the number of bytes sent by one. This will also happen in an odd byte count wide receive case. Also, in the case of a wide send in which there is a chain byte from a previous transfer, the count will not reflect the chain byte sent across the bus during that BMOV. The reason for this is due to the fact that to determine the correct address to start fetching data from after a phase mismatch, this byte cannot be counted for this BMOV as it was actually part of the byte count for the previous BMOV.

CSBC (DCh) - Cumulative SCSI Byte Count - Read/Write

This loadable register contains a cumulative count of the actual number of bytes that have been transferred across the SCSI bus during data phases, i.e., it will not count bytes sent in Command, Status, Message In or Message Out phases. It will count bytes as long as the phase mismatch enable (ENPMJ) is

set. Unlike the SBC this count will not be reset on each BMOV instruction, but will continue to count across multiple BMOV instructions. This register can be loaded with any arbitrary start value.

PCI Configuration Register Differences

The PCI configuration registers in the SYM53C896 are accessed by performing a configuration read/write to the device with its IDSEL pin asserted and the appropriate value in AD(10-8) during the address phase of the transaction.

Device ID (02-03h)

15-0
Device ID

Default >>>

000Bh

The PCI device ID for the SYM53C896 is 000Bh.

Base Address Register One 63-0 (memory) (14-1Bh)

63-0
Base Address Register One

Default >>>

0000000000000004h

This base address register is used to map the operating register set into memory space. This device will require 1024 bytes of address space. This register has bits 9-0 hardwired to 0000000100b respectively. Detailed information on the operation of this register may be found in the PCI 2.1 specification.

Base Address Register Two 63-0 (SCRIPTS RAM) (1C-23h)

63-0
Base Address Register Two

Default >>>

0000000000000004h

This base address register is used to map the SCRIPTS RAM into memory space. This device will require 8192 bytes of address space. This register has bits 12-0 hardwired to 0000000000100b respectively. Detailed information on the operation of this register can be found in the PCI 2.1 specification.

Subsystem Vendor ID Register (2Ch-2Dh)

15-0
Subsystem Vendor ID

Default >>>

1000h if EEPROM download not enabled; EEPROM value or 0000h if EEPROM download enabled.

This register is used to uniquely identify the vendor of the add-in board or subsystem where this PCI device resides. It provides a mechanism for an add-in card vendor to distinguish its cards from another vendor's cards even if the cards have the same PCI controller installed on them (and therefore the same Vendor ID and Device ID). If the external serial EEPROM interface is enabled, then this register is automatically loaded at power-up from the external serial EEPROM. If an auto-download fails for some reason, the value defaults to 0000h. If the auto-download interface is disabled, this register returns a value of 1000h. The 16-bit value stored in the external serial EEPROM for this register is the vendor's PCI Vendor ID and is obtained from the PCI Special Interest Group.

Subsystem ID Register (2Eh-2Fh)

15-0
Subsystem ID

Default >>>

1000h if EEPROM download not enabled; EEPROM value or 0000h if EEPROM download enabled.

This register is used to uniquely identify the add-in board or subsystem where this PCI device resides. It provides a mechanism for an add-in card vendor to distinguish its cards from one another even if the cards have the same PCI controller installed on them (and therefore the same Vendor ID and Device ID). If the external serial EEPROM interface is enabled, then this register is automatically loaded at power-up from the external serial EEPROM. If an auto-download fails for some reason, the value defaults to 0000h. If the auto-download interface is disabled, this register returns a value of 1000h. The 16-bit value stored in the external serial EEPROM for this register is vendor-specific.

Capabilities Pointer (34h), Read Only

7-0
CP

Default >>>

40h

Bits 7-0 Capabilities Pointer

This register provides an offset into the function's PCI configuration space for the location of the first item in the capabilities linked list.

Capability ID (40h), Read Only

7-0
CID 7-0

Default >>>

01h

Bits 7-0 Cap_I (CI)

This register indicates the current data structure is for PCI power management.

Next Item Pointer (41h), Read Only

7-0
NP 7-0

Default >>>

00h

Bits 7-0 Next_Item_Ptr (NP)

Contains the offset location of the next item in the function's capabilities list. The 53C896 has these bits set to zero indicating no further capability registers exist.

Power Management Capabilities (42-43h), Read Only

15-11	10	9	8-6	5	4	3	2-0
PMES	D2S	D1S	Res	DSI	APS	PMEC	VER

Default >>>

00000	1	1	000	0	0	0	001

Bits 15-11 PME_Support (PMES)

Defines the Power Management states in which the 53C896 will assert the PME pin. These bits are set to zero.

Bit 10 D2_Support (D2S)

When set to one, this bit indicates support for power management state D2.

Bit 9 D1_Support (D1S)

When set to one, this bit indicates support for power management state D1.

Bits 8-6 Reserved

Bit 5 Device Specific Initialization (DSI)

This is a device specific initialization bit and is set to zero to indicate that no special initialization is required.

Bit 4 Auxiliary Power Source (APS)

This bit is set to zero and indicates that an auxiliary power source is not needed for the 53C896.

Bit 3 PME Clock (PMEC)

This bit is set to zero and indicates that no PCI clock is required to assert the PME pin.

Bits 2-0 Version (VER)

These bits indicate the version of the PCI Power Management Specification the 53C896 complies to (version 1.0).

Power Management Control/Status (PMCSR) (44-45h), Read/Write

15	14-13	12-9	8	7-2	1-0
PST	DSCL	DSLT	PEN	Res	PWS
Default >>>					
0	00	0000	0	000000	00

Bit 15 PME_Status (PST)

This bit indicates if the 53C896 has generated a Power Management Event. It will default to zero since D3cold is not supported.

Bits 14-13 Data_Scale (DSCL)

Not used in the SYM53C896.

Bits 12-9 Data_Select (DSLT)

Not used in the SYM53C896.

Bit 8 PME_Enable (PEN)

Not used in the SYM53C896.

Bits 7-2 Reserved

Bits 1-0 Power State (PWS)

These two bits determines the current power state of the 53C896 and is used to place the 53C896 into a new power state. (00b = D0, 01b = D1, 10b = D2, 11b = D3hot)

Bridge Support Extensions (46h), Read Only

7-0
BSE
Default >>>
00h

Bits 7-0 Bridge Support Extensions (BSE)

Not used and will return 00h if read.

Data (47h), Read Only

7-0
DATA
Default >>>
00h

Bits 7-0 Data (DATA)

Not used and will return 00h if read.

Programming Differences

MAD Bus Programming

The MAD(7-0) pins, in addition to serving as the address/data bus for the local memory interface, also may be used to program power-up options for the 53C896. A particular option is programmed by allowing the internal pull-down current sink to pull the pin low at reset or by connecting a 4.7 KΩ resistor between the appropriate MAD(x) pin and VDD. The programming resistors require that HC or

HCT external components be used for the memory interface. The MAD(7-0) pins are sensed by internal circuitry three PCI clock cycles after RST/ is deasserted.

MAD(7) Serial EEPROM programmable option. When allowed to be pulled low by the internal pull-down current sink, the automatic subsystem data download is enabled. When pulled high by an external resistor, the automatic subsystem data download is disabled. Please refer to the Serial EEPROM Interface and Subsystem ID / Subsystem Vendor ID Operating Modes section of this document for details.

MAD(6) Enable B duplicate SCSI REQ/ and ACK/ signals. When allowed to be pulled low by the internal pull-down current sink, the duplicate SCSI REQ/ and ACK/ signals for channel B are disabled. When pulled high by an external resistor, the duplicate SCSI REQ/ and ACK/ signals for channel B are enabled.

MAD(5) Enable A duplicate SCSI REQ/ and ACK/ signals. When allowed to be pulled low by the internal pull-down current sink, the duplicate SCSI REQ/ and ACK/ signals for channel A are disabled. When pulled high by an external resistor, the duplicate SCSI REQ/ and ACK/ signals for channel A are enabled.

MAD(4) INTA/ routing enable. Placing a pull-up resistor on this pin causes SCSI Function B interrupt requests to appear on the INTA/ pin, along with SCSI Function A interrupt request, instead of on INTB/. Placing a pull-up resistor on this pin also causes the SCSI Function B Interrupt Pin register (3Dh) in the PCI configuration space to be programmed to 01h instead of 02h. Placing no resistor on this pin causes SCSI Function B interrupt requests to appear on the INTB/ pin. Placing no resistor on this pin also causes the SCSI Function B Interrupt Pin register (3Dh) in the PCI configuration space to be programmed to 02h.

The **MAD(3-1)** pins are used to set the size of the external expansion ROM device attached. Encoding for these pins is listed in the following table (0 indicates pulled down through internal current sink, 1 indicates an external pull-up resistor is attached).

External Memory Support

MAD(3-1)	Available Memory Space
000	16 KB
001	32 KB
010	64 KB
011	128 KB
100	256 KB
101	512 KB
110	1024 KB
111	no external memory present

The **MAD(0)** pin is the slow ROM pin. When pulled up, it enables two extra cycles of data access time to allow use of slower memory devices.

Serial EEPROM Interface and Subsystem ID/Subsystem Vendor ID Operating Modes

The SYM53C896 implements an interface which allows attachment of a serial EEPROM device to the GPIO0 and GPIO1 pins for each SCSI function. There are two modes of operation relating to the Serial EEPROM and the Subsystem ID and Subsystem Vendor ID PCI configuration registers. They are programmable through the MAD7 pin. This pin is sampled at power-up or hard reset. Note that the SYM53C895 required an external pullup resistor while the SYM53C896 utilizes an internal pulldown to achieve the enable condition.

No pullup on MAD7 (pulled down internally)

In this mode of operation, GPIO0 is the serial data signal (SDA) and GPIO1 is the serial clock signal (SCL). When allowed to be pulled low by the internal pull-down current sink, the automatic data download is enabled.

Certain data in the serial EEPROM is automatically loaded into chip registers at power-up or hard reset. The format of the serial EEPROM data is defined below. If the download is enabled and an EEPROM is not present or the Checksum fails, the Subsystem Vendor ID and Subsystem ID read back all zeroes. At power-up or hard reset, only five bytes are loaded into the chip from locations FBh through FFh.

The Subsystem ID register and Subsystem Vendor ID register are read-only, per the PCI specification. Its value defaults to all zeros if the automatic subsystem download fails. It will default to 1000h if the automatic subsystem download is not enabled.

Serial EEPROM data format

Byte	Name	Description
FBh	SVID(0)	Subsystem Vendor ID, LSB. This byte is loaded into the least significant byte of the Subsystem Vendor ID register in the appropriate PCI configuration space at chip power-up or hard reset.
FCh	SVID(1)	Subsystem Vendor ID, MSB. This byte is loaded into the most significant byte of the Subsystem Vendor ID register in the appropriate PCI configuration space at chip power-up or hard reset.
FDh	SID(0)	Subsystem ID, LSB. This byte is loaded into the least significant byte of the Subsystem ID register in the appropriate PCI configuration space at chip power-up or hard reset.
FEh	SID(1)	Subsystem ID, MSB. This byte is loaded into the most significant byte of the Subsystem ID register in the appropriate PCI configuration space at chip power-up or hard reset.
FFh	CKSUM	Checksum. This 8-bit checksum is formed by adding, byte-wise, each byte contained in locations 00h-03h to the seed value 55h, and then taking the 2s complement of the result.
100h-EOM	UD	User Data

4.7K pullup on MAD7

When pulled high by an external resistor, the automatic data download is disabled. No data is automatically loaded into chip registers at power-up or hard reset.

The Subsystem ID register and Subsystem Vendor ID register are read-only, per the PCI specification, with default values of 1000h and 1000h respectively. (Note: There is an internal pull-down on the MAD 7 pin.)