LSI LOGIC®

Differences between the SYM53C1010-33 and the SYM53C896

Systems Engineering Note

S11009
Version 1.3

This SEN is divided into sections. The first section briefly describes the differences in functionality between the SYM53C1010-33 and the SYM53C896. The second section describes the Operating Register/Bit Differences. The last section describes the Programming Differences.

1 Signal Differences

The signal differences between the SYM53C896 and the SYM53C1010-33 are listed in Table 1.1.

Note: The SYM53C896 power and ground signals, V_{DD} and V_{SS}, were renamed in the SYM53C1010-33 to V_{DD-IO} and V_{SS-IO}. As the signal description is unaltered, signals affected by this naming change are not noted in Table 1.1.

Table 1.1 SYM53C896 / SYM53C1010-33 Signal Differences

BGA Pos.	SYM53C896 Signal Name	SYM53C1010-33 Signal Name	SYM53C1010-33 Signal Description
A2	NC	TEST_PD	Test Power Down. This signal is for LSI Logic test purposes only. It is pulled LOW internally and can cause a full chip reset.
A13	A_SACK2+	NC	Reserved or No Connection.
A22	NC	V_{SS}_CORE	Ground for Core Logic.
AA22	NC	V_{SS}_CORE	Ground for Core Logic.
AB2	NC	V_{SS}_CORE	Ground for Core Logic.
AB3	NC	V_{DD}_CORE	Power for Core Logic.
AB23	NC	V_{DD}_CORE	Power for Core Logic.
AC1	NC	V_{DD}_CORE	Power for Core Logic.
AC2	NC	V_{SS}_CORE	Ground for Core Logic.
B2	NC	V_{DD}_A	Power for Analog Cells
B13	A_SACK2-	NC	Reserved or No Connection.
B16	A_SREQ2-	NC	Reserved or No Connection.
B22	NC	V_{DD}_CORE	Power for Core Logic.
B23	NC	V_{DD}_CORE	Power for Core Logic.
C2	NC	V_{SS}_A	Ground for Analog Cells.
C22	NC	SCAN_MODE	Scan Mode. This signal is for LSI Logic test purposes only. This signal has a static pull down.
D16	A_SREQ2+	NC	Reserved or No Connection.
D21	NC	V_{SS}_CORE	Ground for Core Logic.
P22	B_SACK2+	NC	Reserved or No Connection.
P23	B_SACK2-	NC	Reserved or No Connection.
U22	B_SREQ2+	NC	Reserved or No Connection.
U23	B_SREQ2-	NC	Reserved or No Connection.

2 Functionality Differences

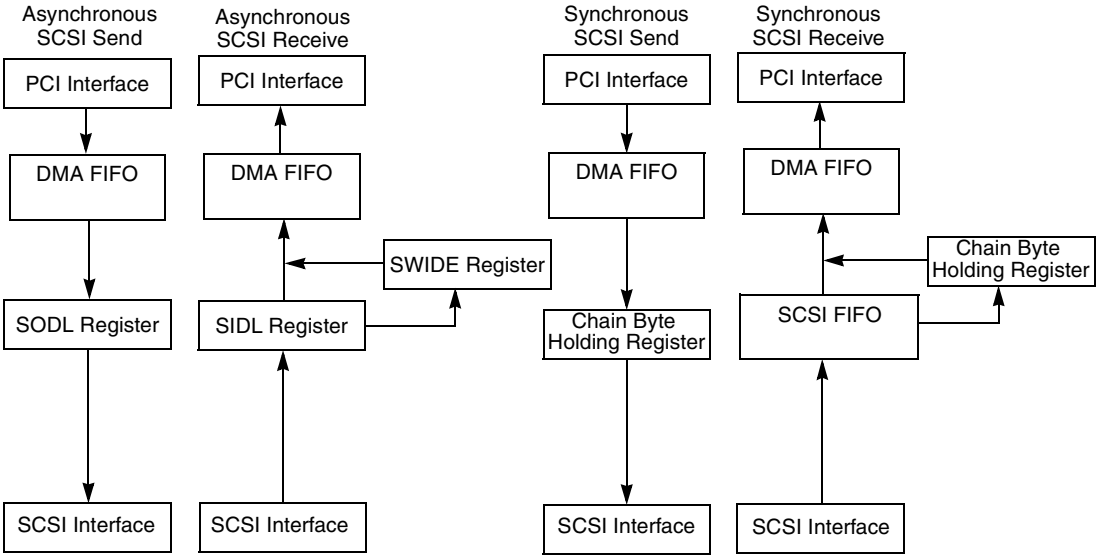
2.1 Ultra3 SCSI

The SYM53C1010 has two Wide Ultra3 SCSI channels in a single package.

2.1.1 SCSI Data Paths

The data path through the SYM53C1010 is dependent on whether data is moved into or out of the chip and whether SCSI transfer is asynchronous or synchronous. Figure 2.1 illustrates how data is moved to and from the SCSI bus in each of the different modes. The following sections determine if any bytes remain in the data path when the device halts an operation.

Figure 2.1 SYM53C1010 Host Interface SCSI Data Paths



2.1.1.1 Asynchronous SCSI Send

To determine the number of bytes remaining in the DMA FIFO when a phase mismatch occurs, read the DMA FIFO Byte Count (DFBC) register. This 16 bit read-only register contains the actual number of

bytes remaining in the DMA FIFO. In addition the SCSI Output Data Latch (SODL) register must be checked to determine if any bytes remain in it. If bit 5 (OLF) in the SCSI Status Zero (SSTAT0) register is set, then the least significant byte in the SODL register contains data. If bit 5 (OLF1) in the SCSI Status Two (SSTAT2) register is set, the most significant byte in the SODL register contains data. Checking these bits also reveals bytes left in the SODL register from a Chained Move operation with an odd byte count. To recover from all other error conditions the DMA FIFO should be cleared by setting bit 2 (CLF) in Chip Test Three (CTEST3) and retrying the I/O.

If the Wide SCSI Send (WSS) bit in the SCSI Control Two (SCNTL2) register is set when a phase mismatch occurs, adjustments must be made to the previous block move, not the current block move loaded into DCMD/DBC. To recover the byte of chain data in the SODL register the previous block move byte count should be set to 1 and the address set to the last data address for that block move.

2.1.1.2 Synchronous SCSI Send

The DMA FIFO is the only location where data can reside when a phase mismatch occurs during a synchronous SCSI send transfer. To determine the number of bytes remaining in the DMA FIFO read the DMA FIFO Byte Count (DFBC) register. This 16 bit, read-only register contains the actual number of bytes remaining in the DMA FIFO. To recover from all other error conditions the DMA FIFO should be cleared by setting bit 2 (CLF) in Chip Test Three (CTEST3) and retrying the I/O.

If the Wide SCSI Send (WSS) bit in the SCSI Control Two (SCNTL2) register is set when a phase mismatch occurs, adjustments must be made to the previous block move, not the current block move loaded into DCMD/DBC. To recover the byte of chain data in the outbound chain byte holding register, the previous block move byte count should be set to one and the address set to the last data address for that block move.

2.1.1.3 Asynchronous SCSI Receive

When a phase mismatch occurs during an asynchronous SCSI receive the only data that may remain in the device is a potential wide residue byte in the SWIDE register. If bit 0 (WSR) in SCSI Control Two (SCNTL2) is set, the SWIDE register contains a residual byte. This byte can be flushed by executing a block move instruction with a byte count of one.

To recover from all other error conditions the DMA FIFO should be cleared by setting bit 2 (CLF) in Chip Test Three (CTEST3) and retry the I/O.

2.1.1.4 Synchronous SCSI Receive

When a phase mismatch occurs during a synchronous SCSI receive transfer no data recovery operation is necessary. All data, including chain bytes from chained block moves, are flushed from the device prior to the phase mismatch occurring. To recover from all other error conditions the DMA FIFO is cleared by setting bit 2 (CLF) in Chip Test Three (CTEST3). The SCSI FIFO is cleared by setting bit 1 (CSF) in SCSI Test Three (STEST3) and retrying the I/O.

2.2 Protocol Changes

Ultra3 SCSI implements double transition (DT) clocking to provide speeds up to 80 mega-transfers per second (MT/s). In double transition clocking the data is sampled on both the asserting and de-asserting edge of REQ/ACK. Double transition clocking can only be implemented using a LVD SCSI bus.

2.2.1 New phases on SCSI bus

In order to support double transition clocking, there are two new phases for the SCSI bus. The old Data-In and Data-Out phases are now called single transition (ST) Data-In and ST Data-Out. The new phases are DT Data-In and DT Data-Out. The use of DT and ST phases implies that the SCRIPTS engine may use a different jump point for DT or ST. The following table illustrates SCSI signal configuration for these phases.

Table 2.2 New Phases on SCSI Bus

Phase	MSG	C/D	I/O	Description
ST Data-Out	0	0	0	
ST Data-In	0	0	1	
DT Data-Out	1	0	0	Previously reserved
DT Data-In	1	0	1	Previously reserved

To indicate DT or ST mode, a bit is set in the current “selection” data reserved byte. BMOVE instructions identify the current BMOVE as either DT or ST through the phase bits.

2.2.2 Parallel Protocol Request

CRC, Sync/Wide, DT, QAS, and “information units” are negotiated with a new SCSI extended message:

Byte 0	0x01	Extended message
Byte 1	0x06	Length
Byte 2	0x04	Parallel Protocol Request (PPR)
Byte 3	0xXX	Transfer Period Factor
Byte 4	0x00	Reserved
Byte 5	0xXX	Req/Ack Offset
Byte 6	0xXX	Transfer Width Exponent
Byte 7	0x0X	Protocol options

2.2.3 Transfer Period

Transfer Period Factor (Byte 3) – Transfer Period Factor is the old Synchronous Period value. These are the same with one addition for 80MT/s rate:

0x09 = 12.5 ns (Ultra3 SCSI) only valid when using DT

0x0A = 25 ns (Ultra2 SCSI)

0x0B = 30.3 ns

0x0C = 50 ns (Ultra SCSI)

0x0D - 0xFF = $value \times 4 = Period$ in ns

The transfer period is related to the data transfer speed, NOT the clock period. So, in DT mode, 0x09 dictates 12.5 ns between clock edges which really means a 25 ns clock period. In DT mode, 0x0A dictates a clock period of 50 ns but a data rate of 40 MT/s (25 ns). In ST mode, 0x0A dictates a clock period of 25 ns and a data rate of 40 MT/s.

Req/Ack Offset (Byte 5) – Req/Ack Offset is the maximum SCSI offset.

Transfer Width Exponent (Byte 6) – Transfer Width Exponent is the old width value. It is set to 0 (8 bit SCSI width) or 1 (16 bit SCSI width).

Note:: For DT mode or when the Protocol Options field is non-zero, the Transfer Width Exponent must be one (1) indicating a SCSI width of 16 bits.

Note:: The Table Indirect data (used during selection/reselection) must be updated to enable certain control bits in the SCNTL4 register. Specific bits to look at include: bit 7, U3EN (Ultra3 Transfer Enable); bit 6, AIPEN (Asynchronous Information Protection Enable); and bits [3:0] (extra clock setup/hold).

Protocol Options (Byte 7) –

OAS_REQ	DT_REQ	IU_REQ	Description
0	0	0	Use ST Data-In and ST Data-Out phase to transfer data
0	1	0	Use DT Data-In and DT Data-Out phase to transfer data with CRC
0	1	1	Use DT Data-In and DT Data-Out phase to transfer data with information units
1	1	0	Use DT Data-In and DT Data-Out phase to transfer data with CRC and use the QAS method for arbitration
1	1	1	Use DT Data-In and DT Data-Out phase to transfer data with information units and use the QAS method for arbitration

A bus or device reset, power cycle, or change between LVD/SE modes invalidate these settings. A re-negotiation resets the Protocol Options.

2.3 Error handling of new negotiation

If the target does not support the selected "Protocol Option" setting, it clears as many bits as required to set the protocol option field to a legal value. For target initiated negotiations, the target must cycle between all

possible protocol options to determine what transfer rates the initiator can handle.

Parity errors during PPR negotiation invalidate the negotiation. The initiator sends the "message parity error" message to the target to indicate it detected an error.

2.4 Asynchronous Information Protection (AIP)

The Asynchronous Information Protection (AIP) feature provides error checking for asynchronous, non-data phases through BCH encoding. During the command, status, and message in/out phases, the BCH code is sent on the upper SCSI data bus. For details on the BCH code, see T10 119 document "Protection for the Asynchronous Phases".

The AIP error status and the live AIP code values are captured in the AIPCNTL1 register for debug purposes. AIP checking and generation is enabled by setting bit 6 in the SCNTL4 register.

The sequence ID is reset on any phase change, chip reset, bus free, or synchronous phase. It is also reset by writing the RSQAIP bit in the AIPCNTL0 register. The AIP sequence value can be read via the SEQAIP bit of this register.

All AIP errors are treated in the same fashion as parity errors. Bit 0 of the SIST0 register indicates if SCSI parity, CRC, or AIP errors are present. The LAIPERR bit in the AIPCNTL1 register indicates if the error is an AIP error.

2.5 CRC

Cyclic Redundancy Check is the error detecting code used in Ultra3 SCSI. Four bytes are transferred with data to increase the reliability of data transfers. CRC is used in the DT Data-In and DT Data-Out phases only. Because CRC is implied with DT mode and only works with DT mode, the DT setting can be used for CRC.

2.6 Parity/CRC/AIP Options

The SYM53C1010 implements a flexible parity scheme that permits control of the parity sense, allows parity checking to be turned on or off, and can deliberately send a bad parity byte over the SCSI bus. Table 2.3

defines the bits that are involved in parity control and observation. Table 2.4 describes the parity control function of the Enable Parity Checking and Assert SCSI Even Parity bits in the SCSI Control One (SCNTL1) register, bit 2. Table 2.4 describes the options available when a parity error occurs.

The SYM53C1010 supports CRC checking and generation in Double Transition (DT) phases and during DT Data Transfers.

The new CRC registers and bits are:

CRCPAD;
CRCCNTL0;
CRCCNTL1;
CRCDATA;
SCNTL0: bit 3, EPC (Enable parity/CRC/AIP checking),
bit 1, AAP (Assert SATN/ on parity/CRC/AIP error);
SCNTL1,bit 5, DHP (Disable Halt on Parity/CRC/AIP Error or ATN);
SIEN0, bit 0, (SCSI Parity/CRC/AIP Error).

The new AIP registers are:

SCNTL0;
AIPCNTL0;
AIPCNTRL1

Table 2.3 Bits Used for Parity/CRC/AIP Control and Generation

Bit Name	Location	Description
AAP (Assert SATN/ on Parity/CRC/AIP Errors)	SCSI Control Zero (SCNTL0), Bit 1	When this bit is set, the SYM53C1010 SCSI function asserts the SATN/ signal upon detection of a parity, CRC, or AIP error. SATN/ is only asserted in initiator mode.
EPC (Enable Parity/CRC/AIP Checking)	SCSI Control Zero (SCNTL0), Bit 3	When set, this bit enables parity checking on the SYM53C1010. The SYM53C1010 checks for odd parity.
Assert Even SCSI Parity	SCSI Control One (SCNTL1), Bit 2	When set, this bit forces a SCSI parity error on each byte sent to the SCSI bus from the SYM53C1010.
Disable Halt on SATN/ or Parity/CRC/AIP Error (Target Mode Only)	SCSI Control One (SCNTL1), Bit 5	Determines if the SYM53C1010 halts operations when a parity error is detected. This bit is only defined for the target mode.
Enable Parity/CRC/AIP Error Interrupt	SCSI Interrupt Enable Zero (SIEN0), Bit 0	Determines whether the SYM53C1010 generates an interrupt when it detects a SCSI parity/CRC/AIP error.

Table 2.3 Bits Used for Parity/CRC/AIP Control and Generation

Bit Name	Location	Description
Parity Error	SCSI Interrupt Status Zero (SIST0), Bit 0	This status bit is set whenever the SYM53C1010 detects a parity/CRC/AIP error on the SCSI bus.
Status of SCSI Parity Signal	SCSI Status Zero (SSTAT0), Bit 0	This status bit represents the active high current state of the SCSI SDP0 parity signal.
SCSI SDP1 Signal	SCSI Status Two (SSTAT2), Bit 0	This bit represents the active high current state of the SCSI SDP1 parity signal.
Latched SCSI Parity	SCSI Status Two (SSTAT2), Bit 3 SCSI Status One (SSTAT1), Bit 3	These bits reflect the SCSI odd parity signal corresponding to the data latched into the SCSI Input Data Latch (SIDL) register.
Master Parity Error Enable	Chip Test Four (CTEST4), Bit 3	Enables parity checking during PCI master data phases.
Master Data Parity Error	DMA Status (DSTAT), Bit 6	Set when the SYM53C1010, as a PCI master, detects a target device signaling a data phase parity error.
Master Data Parity Error Interrupt Enable	DMA Interrupt Enable (DIEN), Bit 6	By clearing this bit, a Master Data Parity Error does not cause assertion of INTA/ (or INTB/). The status bit is set in the DMA Status (DSTAT) register.
AIP Checking	SCSI Control Four (SCNTL4), Bit 6	Setting this bit enables the AIP checking and generation of the upper byte lane of protection information during command, status, and message phases.
CRC Request Pending	SCSI Control Zero (SCNTL0), Bit 2	This bit indicates it is acceptable to force a CRC request. This bit clears only when a CRC request is sent and no data is transferred since the request. This bit is prevents back to back CRC conditions.
Disable CRC Checking	CRC Control Zero (CRCCNTL0), Bit 7	This bit is set to cause internal logic not to check or report CRC errors during Ultra3 transfers.
Disable CRC Protocol Checking	CRC Control Zero (CRCCNTL0), Bit 6	This bit causes the device to not check for a CRC request prior to a SCSI bus phase change. This condition causes a SCSI gross error. Setting this bit makes the SYM53C1010 noncompliant to the SPI-3 specification. This bit should not be set during normal operation.
CRC Reset Counter (Target Mode Only)	CRC Control Zero (CRCCNTL0), Bit 5	When set, this bit resets the internal CRC interval counter to zero. This bit is self clearing.
CRC Interval Counter (Target Mode Only)	CRC Control Zero (CRCCNTL0), Bits [3:0]	These bits determine when a CRC request is sent out by the device. The interval is only applicable when the device is operating in target mode and transferring data in DT Data In or DT Data Out phases. The intervals are provided, in bytes, as: 0x0 = disabled; 0x1 = 128; 0x2 = 256; 0x3 = 512; ... ; 0x9 = 32768; 0xA = 65536; 0xB - 0xF = Reserved.

Table 2.4 SCSI Parity Errors and Interrupts

DHP[1]	PAR[2]	Description
0	0	Halts when a parity error occurs in the target or initiator mode and does NOT generate an interrupt.
0	1	Halts when a parity error occurs in the target mode and generates an interrupt in the target or initiator mode.
1	0	Does not halt in target mode when a parity error occurs until the end of the transfer. An interrupt is not generated.
1	1	Does not halt in target mode when a parity error occurs until the end of the transfer. An interrupt is generated.

1. DHP = Disable Halt on SATN/ or Parity Error (bit 5 SCSI Control One (SCNTL1))
2. PAR = Parity Error (bit 0 SCSI Interrupt Enable One (SIEN1))

2.7 Domain validation

Domain validation is a procedure where a host queries a device to determine its ability to communicate at the negotiated Ultra3 data rate. In software, the following steps are performed to ensure the selected device can successfully transfer data at the negotiated speed.

Step 1. Select a device.

Step 2. Issue Inquiry command.

Step 3. Issue Parallel Protocol Request (PPR) message.

Step 4. Issue Write Buffer command.

Step 5. Issue Read Buffer command.

Step 6. Examine the data pattern to ensure validity.

If the negotiated speed is valid, the commands complete successfully with no CRC errors, bus hangs, or data pattern errors.

2.7.1 Error Handling of Domain Validation

If an error occurs while performing the above domain validation procedure, do the following:

1. Bus Hang

Before step 3 start a handshake to handshake timer. If the timer expires assume the SCSI bus is hung. Several methods could be used to recover from the SCSI bus hang.

- Reset the SCSI bus (noting which SCSI ID hung the bus).
- Issue repeated “ACK” signals until the data phase of the SCSI bus changes.
- Restart with the knowledge that the negotiation must be redone with either pad or timing changes.

2. CRC or Pattern Error

   Restart with the knowledge that the negotiation must be redone with either pad or timing changes.

The 53C1010 allows the use of two options to assist in validation of the SCSI domain. These options are:

1. SCSI LVD Pad drive level changes

   The 53C1010 permits the user to modify the level of the LVD pad drivers. This feature is intended to give the user the ability to test the SCSI environment for margin. This is done by completing a PPR negotiation and then setting the LVD pad drivers to a 20% decrease in level and retrying the PPR negotiation. If the second negotiation completes without error the user can assume the nominal drive strength has an acceptable amount of margin. The LVD Drive strength select bits are located in Chip Control3 (0x5B).

   NOTE: This feature is intended for use in Ultra3 SCSI Domain Validation testing environments only and must not be set during normal data transfer operations.

2. REQ/ACK to data skew

This feature enables the control of the relative skew between the SCSI Req/Ack signal and the data signals. Bits 3:2 in the Chip Control 3 register (0x5B) control the amount of skew between the SCSI Req/Ack signal and the SCSI data signals. These bits are intended to be used for Ultra3 SCSI Domain Validation only and should not be set during normal data transfer operations. The table below gives the skew for each setting of these two bits. The settings are such that negative skew numbers provide less data setup and more data hold and positive skew numbers provide more data setup and less data hold.

These bits only control the skew if the ENDSKEW bit is set (bit 5 Chip Control 3 register (0x5B)).

2.7.2 Synchronous Operation

The SYM53C1010 can transfer synchronous SCSI data in both the initiator and target modes. The SYM53C1010's SCLK input must connect to a 40 MHz oscillator. The SCSI Transfer (SXFER) register controls the synchronous offset and the SCNTL3 register controls the synchronous clock converters. These registers may be loaded by the CPU with a Table Indirect I/O instruction or with a Read-Modify-Write instruction. The load occurs before SCRIPTS execution begins and from within SCRIPTS.

The SYM53C1010 can receive data from the SCSI bus at a synchronous transfer period as short as 12.5 ns, regardless of the transfer period used to send data. The SYM53C1010 can receive data at one-fourth of the divided SCLK frequency. Depending on the SCLK frequency, the negotiated transfer period, and the synchronous clock divider, the SYM53C1010 can send synchronous data at intervals as short as 12.5 ns for Ultra3 SCSI, 25 ns for Ultra2 SCSI, 50 ns for Ultra SCSI, 100 ns for Fast SCSI and 200 ns for SCSI1.

2.7.2.1 Determining the Data Transfer Rate

Synchronous data transfer rates are controlled by bits in two different registers of the SYM53C1010. Following is a brief description of these bits.

2.7.2.2 SCSI Control Three (SCNTL3) Register, bits [6:4] (SCF[2:0])

The SCF[2:0] bits select the factor by which the frequency of SCLK is divided before its presentation to the synchronous SCSI control logic.

The synchronous transfer speed is determined by the combination of the divided clock and the setting of the XCLKS_ST, XCLKS_DT, XCLKH_ST, and XCLKH_DT bits in the SCSI Control Four (SCNTL4) register. The table below gives the clock dividers available. Refer to the Table 4.4, "Double Transition Transfer Rates" and Table 4.5, "Single Transition Transfer Rates", located in the SCSI Control Four (SCNTL4) register description, for a full list of available synchronous transfer rates.

The SCF Divisor values are provided in the following table.

Table 2.5 SCF Divisor Values

SCF2	SCF1	SCF0	SCLK Divisor
0	0	0	SCLK/3
0	0	1	SCLK/1
0	1	0	SCLK/1.5
0	1	1	SCLK/2
1	0	0	SCLK/3
1	0	1	SCLK/4
1	1	0	SCLK/6
1	1	1	SCLK/8

2.7.2.3 SCSI Control Four (SCNTL4) Register, bits [3:0]

The following extra clock bits add an extra clock of setup or hold to a ST or DT transaction.

Bit 3, XCLKH_DT (Extra Clock of Data Hold on DT transfer edge), adds a clock of data hold to synchronous DT SCSI transfers on the DT edge. This bit only impacts DT transfers as it only affects data hold to the DT edge. Setting this bit reduces the synchronous transfer send rate but will not reduce the rate at which the SYM53C1010 receives outbound REQs, ACKs, or data.

Bit 2, XCLKH_ST (Extra Clock of Data Hold on ST transfer edge), adds a clock of data hold to synchronous DT or ST SCSI transfers on the ST edge. This bit impacts DT and ST transfers as it affects data hold to the ST edge. Setting this bit reduces the synchronous transfer send rate but will not reduce the rate at which the SYM53C1010 receives outbound REQs, ACKs, or data.

Bit 1, XCLKS_DT (Extra Clock of Data Setup on DT transfer edge), adds a clock of data setup to synchronous DT SCSI transfers on the DT edge. This bit only impacts DT transfers as it only affects data hold to the DT edge. Setting this bit reduces the synchronous transfer send rate but will

not reduce the rate at which the SYM53C1010 receives outbound REQs, ACKs, or data.

Bit 0, XCLKS_ST (Extra Clock of Data Setup on ST transfer edge), adds a clock of data setup to synchronous DT or ST SCSI transfers on the ST edge. This bit impacts DT and ST transfers as it affects data hold to the ST edge. Setting this bit reduces the synchronous transfer send rate but will not reduce the rate at which the SYM53C1010 receives outbound REQs, ACKs, or data.

The synchronous receive rate can be calculated using the following formula:

$$\text{Receive Rate (DT)} = \frac{\text{Input Clock Rate}}{(\text{SCF Divisor} \times 2)} \quad \text{(MT/sec)}$$

$$\text{Receive Rate (ST)} = \frac{\text{Input Clock Rate}}{(\text{SCF Divisor} \times 4)} \quad \text{(MT/sec)}$$

Note : The receive rate is independent of the settings of the XCLKS_DT, XCLKS_ST, XCLKH_DT, XCLKH_ST bits.

The synchronous send rate, in units of (MT/sec), can be calculated using the following formula:

$$\text{Send Rate (DT)} = \frac{\text{Input Clock Rate}}{\text{SCF Divisor} \times \left(2 + \frac{\text{XCLKS\_DT+XCLKS\_ST+XCLKH\_DT+XCLKH\_ST}}{2}\right)}$$

$$\text{Send Rate (ST)} = \frac{\text{Input Clock Rate}}{\text{SCF Divisor} \times (4 + \text{XCLKS\_ST+XCLKH\_ST})}$$

To configure the SYM53C1010 for Ultra3 DT transfers, perform the following steps:

Step 1. Enable the SCSI Clock Quadrupler -- The SYM53C1010 can quadruple the frequency of a 40 MHz SCSI clock, allowing the system to perform Ultra3 SCSI transfers. This option is user-selectable through bit settings in the SCSI Test One (STEST1) register. At power up or reset, the quadrupler is disabled and powered down. Follow the steps in the bit description to enable the clock quadrupler.

Step 2. Program the Transfer Rate -- Using SCNTL3 and SCNTL4, program the register to 160 MB/sec transfer rate.

Step 3. Program the Maximum SCSI Offset -- Using SXFER, program the maximum SCSI DT Synchronous offset to 0x3E.

Step 4. Enable TolerANT -- Set the TolerANT Enable bit, SCSI Test Three (STEST3), bit 7. Active negation must be enabled for the SYM53C1010 to perform Ultra3 SCSI transfers.

An example of configuring the Ultra3 SCSI transfer speed is:

1. Set SCNTL3 to 0x18.
2. Set SXFER to 0x3E.
3. Set SCNTL4 to 0x80.

These settings program the SYM53C1010 SCSI clocks to send and receive at 160 MHz with a synchronous SCSI offset of 0x3E.

2.8 High Voltage Differential signaling

The 53C1010 does not support HVD.

2.9 66MHz PCI

The SYM53C1010-33 does not support 66 MHz PCI operation. If 66 MHz PCI operation is required, refer to the SYM53C1010-66 documentation.

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3 Operating Register/Bit Differences

There are two sets of PCI configuration registers, one for each SCSI channel. The register sets are identical with the exception of the Interrupt Pin register.

For full details on PCI configuration register space please refer to the PCI 2.2 Specification.

This document describes all the registers that have been changed from SYM53C896 to SYM53C1010 as well as any new registers that have been added in SYM53C1010. For any particular register, only the bits that have changed are described here.

3.1 PCI Configuration Registers

Register: 0x02–0x03
Device ID
Read Only

15							8	7							0
DID															
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

DID **Device ID** **[15:0]**
This 16 bit register identifies the particular device. The SYM53C1010-33 Device ID is 0x0020.

Register: 0x06–0x07
Status
Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3			0
DPE	SSE	RMA	RTA	R	DT[1:0]		DPR	FBBC	R	66C	NC	R			
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Reads to this register behave normally. Writes are slightly different in that bits can be cleared, but not set. A bit is cleared whenever the register is written, and the data in the corresponding bit location is a one. For example, to clear bit 15 and not affect any other bits, write the value 0x8000 to the register.

FBBC **Fast Back to Back Capable** **7**
This bit is zero.

66C **Reserved** **5**
This bit is always set to zero.

Register: 0x3F

Max_Lat (ML)

Read Only

7							0
ML							
0	0	0	1	0	0	1	0

ML **Max_Lat** **[7:0]**

This register is used to specify the desired settings for latency timer values. Max_Lat is used to specify how often the device needs to gain access to the PCI bus. The value specified in this register is in units of 0.25 microseconds. The SYM53C1010 SCSI function sets this register to 0x12 indicating it needs the bus every 4.5 µs to maintain a data stream of 160 Mbytes/sec.

3.2 SCSI Registers

The SCSI operating registers are identical for both channels of this device. SYM53C1010 registers with implementation differences from the SYM53C896 are documented here. If a register is not mentioned, its implementation is unchanged from the SYM53C896. Complete register descriptions are presented in the respective Technical Manuals.

Register: 0x00
SCSI Control Zero (SCNTL0)
Read/Write

7	6	5	4	3	2	1	0
ARB[1:0]		START	WATN	EPC	CRCRP	AAP	TRG
1	1	0	0	0	x	0	0

EPC **Enable Parity/CRC/AIP Checking** **3**
When this bit is set, the SCSI functions transfers are either asynchronous or ST synchronous. The SCSI data bus is checked for odd parity when data is received from the SCSI bus in either the initiator or the target mode. If a parity error is detected, bit 0 of the SCSI Interrupt Status Zero (SIST0) register is set and an interrupt may be generated.

When SCSI transfers are DT synchronous, the CRC is checked when the target requests a CRC transfer via the DP0 signal on the SCSI bus. If a CRC error is detected, bit 0 of the SCSI Interrupt Status Zero (SIST0) register is set and an interrupt may be generated.

If the 53C1010 SCSI function is operating in the initiator mode and a parity error or CRC error is detected, SATN/ can optionally be asserted, but the transfer continues until the target changes phase or the errant block move completes. When this bit is clear, parity and CRC errors are not reported.

CRCRP **CRC Request Pending** **2**
When this bit is set, the SYM53C1010 SCSI function has an outstanding CRC request pending. When this bit is set and the SYM53C1010 is in target mode, a Block Move of zero should not be issued. If a Block Move of zero is

issued, back to back CRC requests are issued. Back to back CRC requests are illegal.

AAP **Assert SATN/ on Parity/CRC/AIP Error** **1**

When this bit is set, the SYM53C1010 SCSI function automatically asserts the SATN/ signal upon detection of a parity error or CRC error. SATN/ is only asserted in the initiator mode. The SATN/ signal is asserted before deasserting SACK/ during the byte transfer with the parity error. Also set the Enable Parity/CRC/AIP Checking bit for the SYM53C1010 SCSI function to assert SATN/ in this manner. A parity error or CRC error is detected on data received from the SCSI bus.

If the Assert SATN/ on Parity/CRC/AIP Error bit is cleared or the Enable Parity/CRC/AIP Checking bit is cleared, SATN/ is not automatically asserted on the SCSI bus when a Parity/CRC/AIP error is received.

Register: 0x01

SCSI Control One (SCNTL1)
Read/Write

7	6	5	4	3	2	1	0
R	ADB	DHP	CON	RST	AESP	IARB	R
0	0	0	0	0	0	0	0

R **Reserved** **7**

This bit was previously the extra clock cycle for the data setup. This is now controlled by the Extra Clock of Data Setup (XCLKS) bit in the SCSI Control 4 (SCNTL4) register.

R **Reserved** **0**

Bit 0 is now reserved. This bit was previously the Start SCSI Transfer (SST) bit.

Register: 0x02

SCSI Control Two (SCNTL2)

Read/Write

7	6	5	4	3	2	1	0
SDU	CHM	R		WSS	VUE0	VUE1	WSR
0	0	0	0	0	0	0	0

R **Reserved** **[5:4]**

Bits [5:4] were previously the SLPAR Mode (SLPMD) and SLPAR High Byte Enable (SLPHBEN) bits, respectively. These bits are now reserved.

Register: 0x03

SCSI Control Three (SCNTL3)

Read/Write

7	6		4	3	2		0
R	SCF[2:0]			EWS	R		
0	0	0	0	0	0	0	0

R **Reserved** **7**

This bit was previously Ultra SCSI Enable. This function is now automatically handled based on the settings of the clock dividers, the clock quadrupler, and the U3EN bit in the SCSI Control 4 (SCNTL4) register.

SCF[2:0] **Synchronous Clock Conversion Factor** **[6:4]**

These bits select a factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. The synchronous transfer speed is determined by the combination of the divided clock and the setting of the XCLKS and XCLKH bits in the SCSI Control 4 (SCNTL4) register. The table below shows the clock dividers that are available. See the table in the SCSI Control 4 (SCNTL4) register description for a full list of available transfer rates.

SCF2	SCF1	SCF0	Factor Frequency
0	0	0	SCLK/3
0	0	1	SCLK/1
0	1	0	SCLK/1.5
0	1	1	SCLK/2
1	0	0	SCLK/3
1	0	1	SCLK/4
1	1	0	SCLK/6
1	1	1	SCLK/8

EWS **Enable Wide SCSI** **3**

When is cleared, all information transfer phases are assumed to be eight bits, transmitted on SD[7:0]/ and SDP0/. When this bit is asserted, data transfers are performed 16 bits at a time; the least significant byte is on SD[7:0]/ and SDP0/, and the most significant byte is on SD[15:8]/, SDP1/. Command, Status, and Message phases are not affected by this bit. Because Ultra3 DT SCSI transfers are always wide this bit must be set. If it is not set, a SGE interrupt will occur.

R **Reserved** **[2:0]**

These bits were previously the CCF value. Due to the fact that this device is limited to a 40 MHz SCSI clock, these bits are no longer being used and the clock divider is no longer fixed at divide by 2 or divide by 8 depending upon whether the clock quadrupler is enabled or not.

Register: 0x05
SCSI Transfer (SXFER)
Read/Write

7	6	5					0
R		MO[5:0]					
0	0	0	0	0	0	0	0

This register is automatically loaded when a Table Indirect Select or Reselect SCRIPTS instruction is executed.

R **Reserved** **[7:6]**
These bits were previously defined as SCSI Synchronous Transfer Period (TP[2:1]) and were used to determine the synchronous transfer rates. This function is now controlled by a combination of the SCF clock divider setting, the clock quadrupler setting and the setting of the XCLKS and XCLKH bits in the SCSI Control 4 (SCNTL4) register.

MO[5:0] **Max SCSI Synchronous Offset** **[5:0]**
These bits describe the maximum SCSI synchronous offset used by the SYM53C1010 SCSI function when transferring synchronous SCSI data in either the initiator or target mode. The following table describes the possible combinations and their relationship to the synchronous data offset used by the SYM53C1010 SCSI function. These bits determine the SYM53C1010 SCSI function's method of transfer for ST/DT Data-In and ST/DT Data-Out phases only; all other information transfers occur asynchronously. Please note that the SCSI offset for Ultra3 transfers is counted as the maximum number of data transfers allowed to be outstanding, not the maximum REQ pulses allowed to be outstanding.

During ST Data-In or ST Data-Out transfers the maximum supported offset is 31 (MO[5:0] = 0x1F).

During DT Data-In or DT Data-Out transfers the maximum supported offset is 62 (MO[5:0] = 0x3E).

Setting offset values outside the allowable range will result in data corruption.

A value of 0 in these bits program the device to perform asynchronous transfers. A value of 1 during DT transfers is illegal and will result in data corruption.

Table 3.6 Maximum Synchronous Offset

MO5	MO4	MO3	MO2	MO1	MO0	Synchronous Offset
0	0	0	0	0	0	0-Asynchronous
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
...	...	...	...	...	...	...
...	...	...	...	...	...	...
...	...	...	...	...	...	...
1	1	1	0	0	1	57
1	1	1	0	1	0	58
1	1	1	0	1	1	59
1	1	1	1	0	0	60
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	Reserved

Register: 0x0D

SCSI Status Zero (SSTAT0)
Read Only

7	6	5	4	3	2	1	0
ILF	R	OLF	ARBIP	LOA	WOA	RST	SDP0
0	0	0	0	0	0	0	0

R **Reserved** **6**
Bit 6 was previously the SODR Least Significant Byte Full (ORF). This bit is now reserved.

Register: 0x0E

SCSI Status One (SSTAT1)
Read Only

7			4	3	2	1	0
R				SDPOL	MSG	C_D	I_O
0	0	0	0	x	x	x	x

R **Reserved** **[7:4]**
Bits [7:4] were previously the FIFO Flag (FF[3:0]) bits. These bits are now reserved.

Register: 0x0F
SCSI Status Two (SSTAT2)
Read Only

7	6	5	4	3	2	1	0
ILF1	R	OLF1	R	SPL1	R	LDSC	SDP1
0	0	0	0	x	0	1	x

R **Reserved** **6**
This bit was previously the SODR Most Significant Byte Full bit. This bit is now reserved.

R **Reserved** **4**
This bit was previously the FIFO Flags bit. This bit is now reserved.

R **Reserved** **2**
This bit was previously the DIFFSENS Mismatch bit. The HVD mode is not supported in the SYM53C1010 and this bit now reserved.

Register: 0x14
Interrupt Status Zero (ISTAT0)
Read/Write

7	6	5	4	3	2	1	0
ABRT	SRST	SIGP	SEM	CON	INTF	SIP	DIP
0	0	0	0	0	0	0	0

This is the only register that is accessible by the host CPU while a SYM53C1010 SCSI function is executing SCRIPTS (without interfering in the operation of the function). It is used to poll for interrupts if hardware interrupts are disabled. Read this register after servicing an interrupt to check for stacked interrupts.

SRST **Software Reset** **6**
Setting this bit resets the SYM53C1010 SCSI function. All operating registers are cleared to their respective default values and all SCSI signals are deasserted. Setting this bit does not assert the SCSI RST/ signal. This reset does not clear the ID Mode bit or any of the PCI configuration registers. This bit is not self-clearing; it must be cleared

to clear the reset condition (a hardware reset also clears this bit).

NOTE: If SCRIPTS are running, then ABRT bit 7 must be set prior to setting the SRST bit.

Register: 0x1A

Chip Test Two (CTEST2)
Read Only (bit 3 write)

7	6	5	4	3	2		0
R	SIGP	CIO	CM	PCICIE	R		
x	0	x	x	0	x	x	x

R **Reserved** **[7]**
This bit was previously the Data Transfer Direction bit. This bit is no longer used.

R **Reserved** **[2]**
This bit was previously the SCSI True End of Process bit. This bit is no longer used.

R **Reserved** **[1]**
This bit was previously the Data Request Status bit. This bit is no longer used.

R **Reserved** **[0]**
This bit was previously the Data Acknowledge Status bit. This diagnostic bit is no longer used.

Register: 0x1B

Chip Test Three (CTEST3)
Read/Write

7			4	3	2	1	0
R				FLF	CLF	R	WRIE
0	0	0	0	0	0	0	0

R **Reserved** **[7:4]**
These bits were previously the Chip Revision Level bits. They are no longer used. The chip revision can be obtained by setting the PCICIE bit (bit 3) in the CTEST2 register and checking the SFS register bits [23:16].

R **Reserved** **[1]**
This bit was previously the Fetch Pin Mode bit. This bit is no longer used.

Register: 0x20
Reserved

This register was previously DMA FIFO register. It is no longer used.

Register: 0x21
Chip Test Four (CTEST4)
Read/Write

7	6	5	4	3	2		0
R	FBL3	R	SRTM	MPEE	FBL[2:0]		
0	0	0	0	0	0	0	0

R **Reserved** **[7]**
This bit was previously the burst disable bit. This bit is no longer used. Bursting is always enabled in the chip.

R **Reserved** **[5]**
This bit was previously the SCSI Data High Impedance Mode bit. This bit is no longer used.

Register: 0x22
Chip Test Five (CTEST5)
Read/Write

7	6	5		3	2	1	0
ADCK	BBCK	R			BL2	R	
0	0	0	0	0	0	0	0

R **Reserved** **[5]**
This bit was previously the DMA FIFO Size bit. This bit is no longer used.

R **Reserved** **[4]**
This bit was previously the Master Control for Set or Reset Pulses. This bit is no longer used.

R **Reserved** **[3]**
This bit was previously the DMA Direction bit. This bit is no longer used.

R **Reserved** **[1:0]**
These bits were previously the DMA FIFO Byte Offset Counter bits. These bits are no longer used.

Register: 0x38

DMA Mode (DMODE)
Read/Write

7	6	5	4	3	2	1	0
BL[1:0]		SIOM	DIOM	ERL	ERMP	BOF	MAN
0	0	0	0	0	0	0	0

BL[1:0] **Burst Length** **[7:6]**
These bits control the maximum number of dwords transferred per bus ownership, regardless of whether the transfers are back-to-back, burst, or a combination of both. This value is also independent of the width (64 or 32 bits) of the data transfer on the PCI bus. The SYM53C1010 SCSI function asserts the Bus Request (PCIREQ/) output when the DMA FIFO can accommodate a transfer of at least one burst threshold of data. Bus Request (PCIREQ/) is also asserted during start-of-transfer and end-of-transfer cleanup and alignment, even if less than a full burst of transfers is performed. The SYM53C1010 SCSI function inserts a “fairness delay” of four CLKs between burst transfers (set in BL[2:0]) during normal operation. The fairness delay is not inserted during PCI retry cycles. This gives the CPU and other bus master devices the opportunity to access the PCI bus between bursts.

BL2 (CTEST5 bit 2)	BL1	BL0	Number of 64 bit Transfers	Number of 32 bit Transfers
0	0	0	2	4
0	0	1	4	8
0	1	0	8	16
0	1	1	16	32
1	0	0	32	64
1	0	1	64	128
1	1	0	64	128
1	1	1	Reserved	Reserved

Register: 0x3B

DMA Control (DCNTL)
Read/Write

7	6	5	4	3	2	1	0
CLSE	PFF	PFEN	SSM	IRQM	STD	R	COM
0	0	0	0	0	0	0	0

R **Reserved** **1**
This bit was previously the INTA, INTB Disable bit. This bit is no longer used.

Register: 0x40

SCSI Interrupt Enable Zero (SIEN0)
Read/Write

7	6	5	4	3	2	1	0
M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
0	0	0	0	0	0	0	0

PAR **SCSI Parity/CRC/AIP Error** **0**
This bit indicates the SYM53C1010 SCSI function detected a Parity/CRC/AIP error while receiving or sending SCSI data. See the Disable Halt on Parity/CRC/AIP error or SATN/ Condition bits in the SCNTL1 register for more information about when this condition is raised.

Register: 0x42

SCSI Interrupt Status Zero (SIST0)
Read Only

7	6	5	4	3	2	1	0
M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
0	0	0	0	0	0	0	0

PAR **Parity/CRC/AIP Error** **0**

This bit indicates the SYM53C1010 SCSI function detected a Parity/CRC/AIP error while receiving or sending SCSI data. See the Disable Halt on Parity/CRC/AIP error or SATN/ Condition bits in the SCNTL1 register for more information about when this condition will actually be raised.

Register: 0x44

Reserved

This register was previously the SCSI Longitudinal Parity (SLPAR) register. This function is no longer supported in 53C1010.

Register: 0x46

Reserved

7							0
Reserved							
X	X	X	X	X	X	X	X

This register was previously the Chip Type (CTYPE) register. This register is no longer used. The PCI Device ID and Revision ID should be used to identify the device. They can be read by setting the PCICIE bit in the CCTEST2 register and then reading the SFS register.

Register : 0x49
SCSI Timer One (STIME1)
Read/Write

7	6	5	4	3			0
R	HTHBA	GENSF	HTHSF	GEN[3:0]			
x	0	0	0	0	0	0	0

GENSF **General Purpose Timer Scale Factor** **5**
Setting this bit causes this timer to shift by a factor of 16. Refer to the SCSI Timer Zero (STIME0) register description for details.

HTH 7-4, SEL 3-0, GEN 3-0	Minimum Time-out	
	HTHSF = 0, GENSF = 0	HTHSF = 1, GENSF = 1
0000	Disabled	Disabled
0001	125 µs	2 ms
0010	250 µs	4 ms
0011	500 µs	8 ms
0100	1 µs	16 ms
0101	2 ms	32 ms
0110	4 ms	64 ms
0111	8 ms	128 ms
1000	16 ms	256 ms
1001	32 ms	512 ms
1010	64 ms	1 sec
1011	128 ms	2 sec
1100	256 ms	4.1 sec
1101	512 ms	8.2 sec
1110	1.024 sec	16.4 sec
1111	2.048 sec	32.8 sec

Register: 0x4D
SCSI Test One (STEST1)
Read/Write

7	6	5	4	3	2	1	0
R		DOSGE	DISGE	QEN	QSEL	IRM[1:0]	
0	0	0	0	0	0	0	0

R **Reserved** **[7]**
This bit was previously the SCSI Clock bit. This bit is now used for internal testing only.

R **Reserved** **[6]**
This bit was previously the SCSI Isolation Mode bit. This bit is no longer used.

DOSGE **Disable Outbound SCSI Gross Errors** **[5]**
This bit disables all SCSI gross errors related to outbound data transfers.

DISGE **Disable Inbound SCSI Gross Errors** **[4]**
This bit disables all SCSI gross errors related to inbound data transfers.

Register: 0x4E
SCSI Test Two (STEST2)
Read/Write

7	6	5	4	3	2	1	0
SCE	ROF	R		SZM	R		LOW
0	0	0	0	0	0	0	0

R **Reserved** **[5]**
This bit was previously HVD or SD/LVD. This bit is no longer used. The SYM53C1010 does not support the HVD mode.

R **Reserved** **[4]**
This bit was previously the SCSI Loopback Mode bit. This bit is no longer used.

R **Reserved** **[2]**
This bit was previously the Always Wide SCSI bit. This bit is no longer used.

R **Reserved** **[1]**
This bit was previously the Extend SREQ/SACK Filtering bit. This bit is no longer used.

Register: 0x4F
SCSI Test Three (STEST3)
Read/Write

7	6	5	4	3	2	1	0
TE	R	HSC	DSI	R	TTM	CSF	R
0	0	0	0	0	0	0	0

R **Reserved** **[6]**
This bit was previously the SCSI FIFO Test Read bit. This bit is no longer used.

R **Reserved** **[3]**
This bit was previously the 16-bit System bit. This bit is no longer used.

R **Reserved** **[0]**
This bit was previously the SCSI FIFO Test Write bit. This bit is no longer used.

Register: 0x52
SCSI Test Four (STEST4)
Read Only

7	6	5					0
SMODE[1:0]		R					
X	X	0	0	0	0	0	0

R **Reserved** **[5]**
This bit was previously the Frequency Lock bit. In order to ensure locking of the quadrupler, a delay should be used after the quadrupler enable bit has been set. This bit is no longer used.

Register: 0x53
Current Inbound SCSI Offset (CSO)
Read Only

7	6	5	4	3	2	1	0
R		CSO5	CSO4	CSO3	CSO2	CSO1	CSO0
0	0	0	0	0	0	0	0

This register was previously reserved. It is now the Current Inbound SCSI Offset (CSO) register.

R **Reserved** **[7:6]**

CSO **Current SCSI Offset** **[5:0]**
These bits indicate the SCSI offset for synchronous inbound transfers. This also represents the number of data bytes in the SCSI FIFO in narrow transfer modes and half the number of bytes in wide transfer mode. This does not include any CRC or PAD bytes that may be in the FIFO.

Register: 0x56
Chip Control Zero (CCNTL0)
Read/Write

7	6	5	4	3	2	1	0
ENPMJ	PMJCTL	ENNDJ	DISFC	R		DISRC	DPR
0	0	0	0	x	x	0	0

DISRC **Disable Internal SCRIPTS RAM Cycles** **1**
This bit controls whether or not data transfers, for which the source/destination is located in SCRIPT RAM, generate external PCI cycles.

If clear, data transfers of this type do NOT generate PCI cycles, but stay internal to the chip. If set, data transfers of this type generate PCI cycles. This does not affect SCRIPTS Fetch operations from SCRIPTS RAM, including Table Indirect and Indirect opcode fetches.

Register: 0x57

Chip Control One (CCNTL1)
Read/Write

7	6	5	4	3	2	1	0
PULLDIS	PULLEN	DIS64MAS	DIS64SLV	DDAC	64TIMOD	EN64TIBMV	EN64DBMV
0	0	0	0	x	x	0	0

PULLDIS **Pull Disable** **7**
Setting this bit causes all internal pulls to be disabled on all pins. This bit is intended for manufacturing test only and should NOT be set for normal operation.

PULLEN **Pull Enable** **6**
Setting this bit causes all internal pulls to be enabled on all pins. This bit is intended for manufacturing test only and should NOT be set for normal operation.

DIS64MAS **Disable 64 bit Master Operation** **5**
Setting this bit causes the SYM53C1010 to no longer request 64 bit master data transfers. If this bit is set by either SCSI channel, 64 bit data transfers will be disabled for all master transactions.

DIS64SLV **Disable 64 bit Slave Cycles** **4**
Setting this bit disables 64 bit slave data transfers to the SCRIPT RAM. This causes only 32 bit data transfers to occur.

Register : 0x5B

Chip Control Three (CCNTL3)
Read/Write

7		5	4	3	2	1	0
R			ENDSKEW	DSKEW[1:0]		LVDDL[1:0]	
0	0	0	0	0	0	0	0

R **Reserved** **[7:5]**

ENDSKEW **Enable REQ/ACK to Data Skew Control** **4**
Setting this bit enables the control of the relative skew between the SCSI REQ/ACK signals and the data sig-

nals. The actual amount of skew time is controlled by DSKEW[1:0] in this register.

DSKEW[1:0] Data Skew Control [3:2]
These bits control the amount of skew between the SCSI REQ/ACK signal and the SCSI data signals. The skew is affected only if the ENDSKEW bit is set.

Note:: These bits are used for Ultra3 SCSI Domain Validation only and should not be set during normal data transfer operations.

LVDDL[1:0] LVD Drive Strength Select [1:0]
These bits control the drive level of the LVD pad drivers.

Note:: This feature is for Ultra3 SCSI Domain Validation testing environments only and should not be set during normal data transfer operations.

The table below shows the relative strength increase or decrease based on the LVDDL values.

LVDDL	Drive Level
00	Nominal
01	-20% Nominal
10	+20% Nominal
11	Reserved

Note:: If one of the LVDDL [1:0] bits are set on either channel, both channels are affected.

Register: 0xBC

SCSI Control Four (SCNTL4)
Read/Write

7	6	5	4	3	2	1	0
U3EN	AIPEN	R		XCLKH_DT	XCLKH_ST	XCLKS_DT	XCLKS_ST
0	0	0	0	0	0	0	0

This register is automatically loaded when a Table Indirect Select or Reselect SCRIPT instruction is executed.

U3EN **Ultra3 Transfer Enable** **7**
Setting this bit enables Ultra3 transfers. This bit will force all SCSI Block Move SCRIPTS instructions for ST Data-In or ST Data-Out phases to become DT Data-In or DT Data-Out phases.

AIPEN **Asynchronous Information Protection Enable** **6**
Setting this bit enables the AIP checking and generation of the upper byte lane of protection information during Command, Status, and Message phases.

R **Reserved** **[5:4]**

XCLKH_DT **Extra Clock of Data Hold on DT Transfer Edge** **3**
Setting this bit adds a clock of data hold to synchronous DT SCSI transfers on the DT edge. This bit only impacts DT transfers as it affects data hold to the DT edge. Setting this bit reduces the synchronous transfer send rate, but does not reduce the transfer rate that the SYM53C1010 can receive inbound REQs, ACKs or data. Refer to Table 0.3 and Table 0.4 for a summary of available transfer rates and to Figure 0.1 through Figure 0.3 for examples of how the XCLKH bits function.

Note: This bit does not affect CRC timings.

XCLKH_ST **Extra Clock of Data Hold on ST Transfer Edge** **2**
Setting this bit adds a clock of data hold to synchronous DT or ST SCSI transfers on the ST edge. This bit impacts both ST and DT transfers as it affects data hold to the ST edge. Setting this bit reduces the synchronous send transfer rate but does not reduce the transfer rate that the SYM53C1010 can receive inbound REQs, ACKs or data. Refer to Table 0.3 and Table 0.4 for a summary of available transfer rates and to Figure 0.1 through Figure 0.3 for examples of how the XCLKH bits function.

Note: This bit does not affect CRC timings.

XCLKS_DT **Extra Clock of Data Setup on DT Transfer Edge** **1**
Setting this bit adds a clock of data setup to synchronous DT SCSI transfers on the DT edge. This bit only impacts DT transfers as it only affects data setup to the DT edge. Setting this bit reduces the synchronous transfer send

rate, but does not reduce the transfer rate that the SYM53C1010 can receive inbound REQs, ACKs or data. Refer to Table 0.3 and Table 0.4 for a summary of available transfer rates and to Figure 0.1 through Figure 0.3 for examples of how the XCLKS bits function.

Note: This bit does not affect CRC timings.

XCLKS_ST **Extra Clock of Data Setup on ST Transfer Edge** **0**
Setting this bit adds a clock of data setup to synchronous DT or ST SCSI transfers on the ST edge. This bit impacts both ST and DT transfers as it affects data setup to the ST edge. Setting this bit reduces the synchronous send transfer rate but does not reduce the transfer rate that the SYM53C1010 can receive inbound REQs, ACKs or data. Refer to Table 0.3 and Table 0.4 for a summary of available transfer rates and to Figure 0.1 through Figure 0.3 for examples of how the XCLKS bits function.

Note: This bit does not affect CRC timings.

Synchronous Receive Rate Calculation
The synchronous receive rate, in mega transfers per second (MT/s), can be calculated using the following formulas:

$$\text{Receive Rate (DT)} = \frac{\text{Input Clock Rate}}{\text{SCF Divisor} \times 2}$$

$$\text{Receive Rate (ST)} = \frac{\text{Input Clock Rate}}{\text{SCF Divisor} \times 4}$$

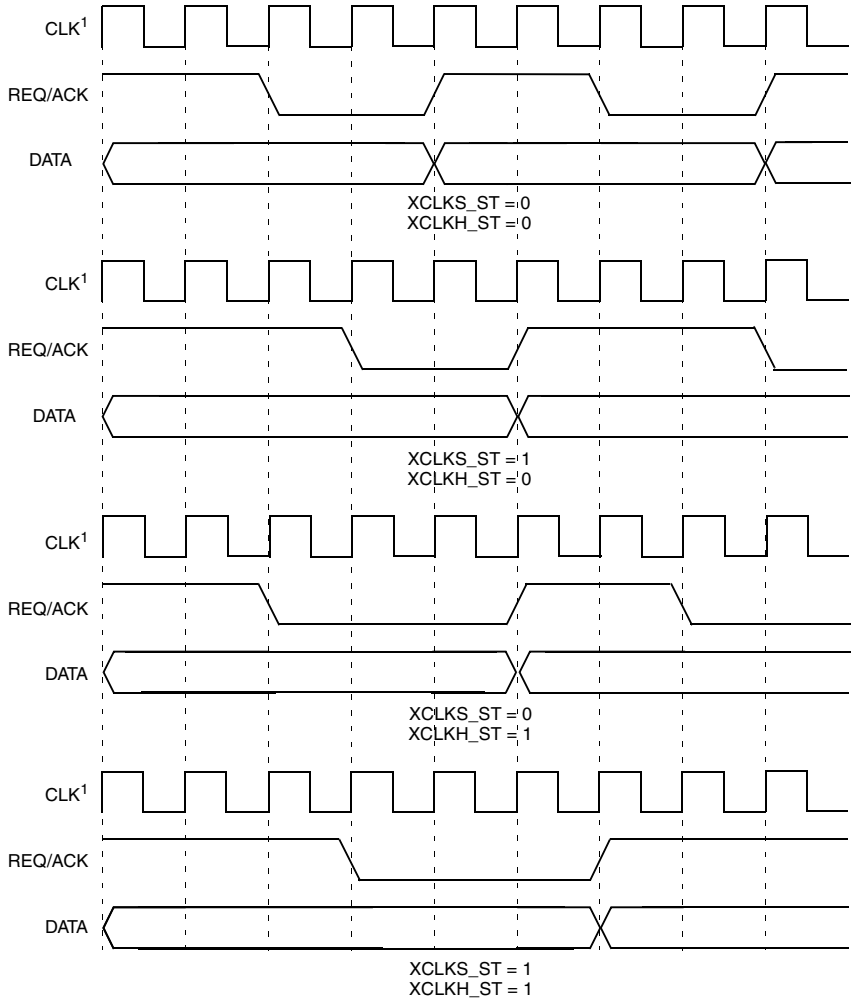
Note:: The receive rate is independent of the settings of the XCLKS_DT, XCLKS_ST, XCLKH_DT, and XCLKH_ST bits.

Synchronous Send Rate Calculation
The synchronous send rate, in mega transfers per second (MT/s), can be calculated using the following formulas:

$$\text{Send Rate (DT)} = \frac{\text{Input Clock Rate}}{\left(\text{SCFDivisor} \times \left(2 + \frac{\text{XCLKS\_DT} + \text{XCLKS\_ST} + \text{XCLKH\_DT} + \text{XCLKH\_ST}}{2}\right)\right)}$$

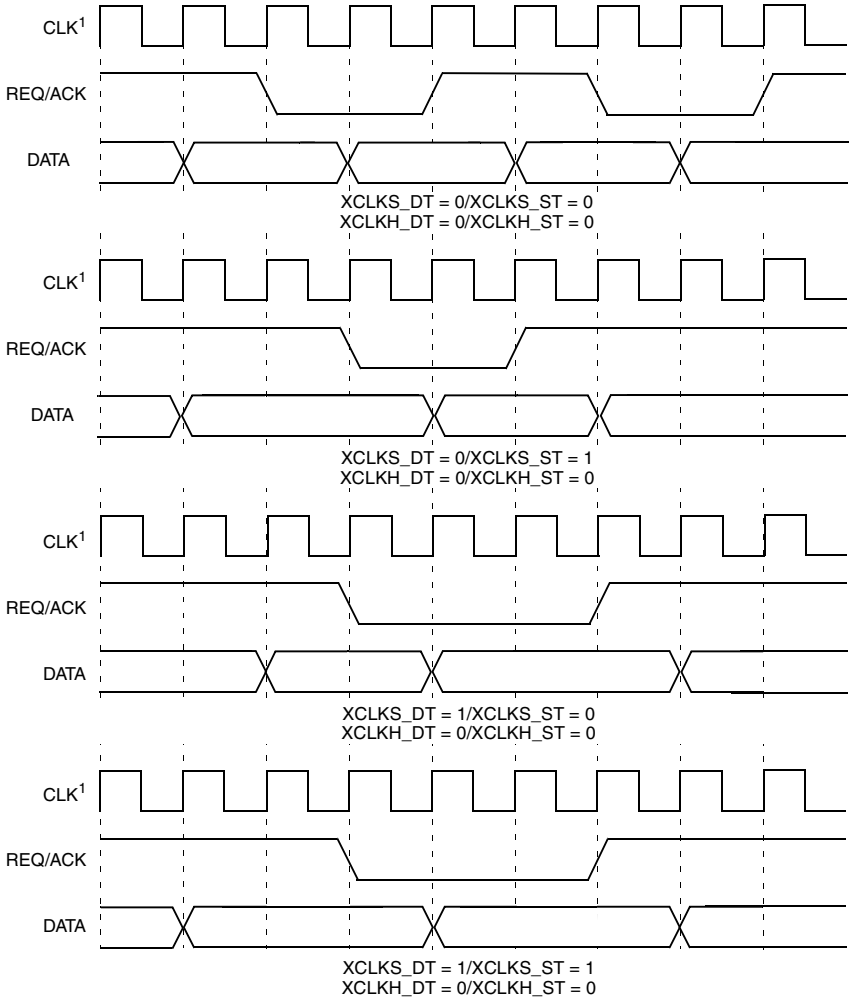
$$\text{Send Rate (ST)} = \frac{\text{Input Clock Rate}}{\text{SCFDivisor} \times (4 + \text{XCLKS\_ST} + \text{XCLKH\_ST})}$$

Figure 3.2 Single Transition Transfer Waveforms



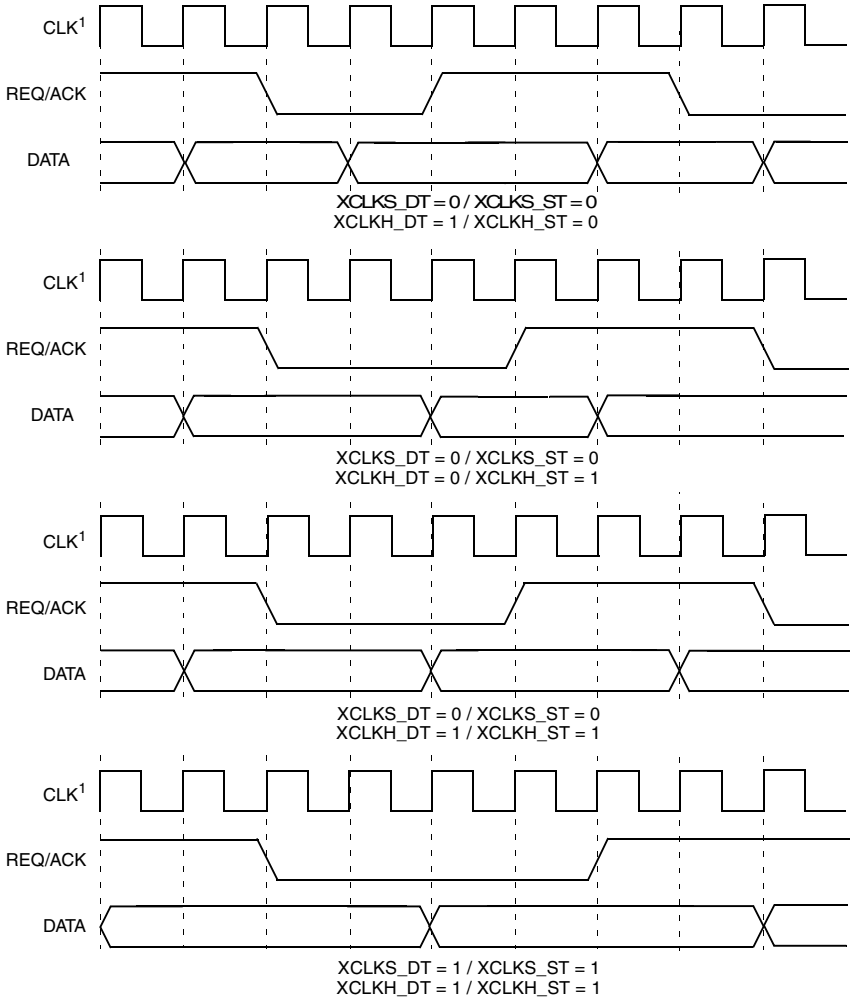
1. CLK = SCLK/SCF Divisor

Figure 3.3 Double Transition Transfer Waveforms (XCLKS Examples)



1. CLK = SCLK/SCF Divisor

Figure 3.4 Double Transition Transfer Waveforms (XCLKH Examples)



1. CLK = SCLK/SCF Divisor

Table 3.7 Double Transition Transfer Rates

Clock (MHz)	Divisor	Number Xclk's[1]	Base Period (ns)	Rcv. Rate (MT/s)	Send Rate (MT/s)
160	**1**	**0**	**6.25**	**80.00**	**80.00**
160	1	1	6.25	80.00	64.00
160	1	2	6.25	80.00	53.33
160	1	3	6.25	80.00	45.71
160	1	4	6.25	80.00	40.00
160	**1.5**	**0**	**9.38**	**53.33**	**53.33**
160	1.5	1	9.38	53.33	42.67
160	1.5	2	9.38	53.33	35.56
160	1.5	3	9.38	53.33	30.48
160	1.5	4	9.38	53.33	26.67
160	**2**	**0**	**12.50**	**40.00**	**40.00**
160	2	1	12.50	40.00	32.00
160	2	2	12.50	40.00	26.67
160	2	3	12.50	40.00	22.86
160	2	4	12.50	40.00	20.00
160	**3**	**0**	**18.75**	**26.67**	**26.67**
160	3	1	18.75	26.67	21.33
160	3	2	18.75	26.67	17.78
160	3	3	18.75	26.67	15.24
160	3	4	18.75	26.67	13.33
160	**4**	**0**	**25.00**	**20.00**	**20.00**
160	4	1	25.00	20.00	16.00
160	4	2	25.00	20.00	13.33
160	4	3	25.00	20.00	11.43
160	4	4	25.00	20.00	10.00
160	**6**	**0**	**37.50**	**13.33**	**13.33**
160	6	1	37.50	13.33	10.67
160	6	2	37.50	13.33	8.89
160	6	3	37.50	13.33	7.62
160	6	4	37.50	13.33	6.67
160	**8**	**0**	**50.00**	**10.00**	**10.00**
160	8	1	50.00	10.00	8.00
160	8	2	50.00	10.00	6.67
160	8	3	50.00	10.00	5.71
160	8	4	50.00	10.00	5.00
40	**1**	**0**	**25.00**	**20.00**	**20.00**
40	1	1	25.00	20.00	16.00
40	1	2	25.00	20.00	13.33
40	1	3	25.00	20.00	11.43
40	1	4	25.00	20.00	10.00
40	**1.5**	**0**	**37.50**	**13.33**	**13.33**
40	1.5	1	37.50	13.33	10.67
40	1.5	2	37.50	13.33	8.89

Table 3.7 Double Transition Transfer Rates (Cont.)

Clock (MHz)	Divisor	Number Xclk's[1]	Base Period (ns)	Rcv. Rate (MT/s)	Send Rate (MT/s)
40	1.5	3	37.50	13.33	7.62
40	1.5	4	37.50	13.33	6.67
40	**2**	**0**	**50.00**	**10.00**	**10.00**
40	2	1	50.00	10.00	8.00
40	2	2	50.00	10.00	6.67
40	2	3	50.00	10.00	5.71
40	2	4	50.00	10.00	5.00
40	**3**	**0**	**75.00**	**6.67**	**6.67**
40	3	1	75.00	6.67	5.33
40	3	2	75.00	6.67	4.44
40	3	3	75.00	6.67	3.81
40	3	4	75.00	6.67	3.33
40	**4**	**0**	**100.00**	**5.00**	**5.00**
40	4	1	100.00	5.00	4.00
40	4	2	100.00	5.00	3.33
40	4	3	100.00	5.00	2.86
40	4	4	100.00	5.00	2.50
40	**8**	**0**	**200.00**	**2.50**	**2.50**
40	8	1	200.00	2.50	2.00
40	8	2	200.00	2.50	1.67
40	8	3	200.00	2.50	1.43
40	8	4	200.00	2.50	1.25

1. Number Xclk's = XCLKS_DT + XCLKS_ST + XCLKH_DT + XCLKH_ST

Table 3.8 Single Transition Transfer Rates

Clock (MHz)	Divisor	Number Xclk's[1]	Base Period (ns)	Rcv. Rate (MT/s)	Send Rate (MT/s)
160	**1**	**0**	**6.25**	**40.00**	**40.00**
160	1	1	6.25	40.00	32.00
160	1	2	6.25	40.00	26.67
160	**1.5**	**0**	**9.38**	**26.67**	**26.67**
160	1.5	1	9.38	26.67	21.33
160	1.5	2	9.38	26.67	17.78
160	**2**	**0**	**12.50**	**20.00**	**20.00**
160	2	1	12.50	20.00	16.00
160	2	2	12.50	20.00	13.33
160	**3**	**0**	**18.75**	**13.33**	**13.33**
160	3	1	18.75	13.33	10.67
160	3	2	18.75	13.33	8.89
160	**4**	**0**	**25.00**	**10.00**	**10.00**
160	4	1	25.00	10.00	8.00

Table 3.8 Single Transition Transfer Rates (Cont.)

Clock (MHz)	Divisor	Number Xclk's[1]	Base Period (ns)	Rcv. Rate (MT/s)	Send Rate (MT/s)
160	4	2	25.00	10.00	6.67
160	**6**	**0**	**37.50**	**6.67**	**6.67**
160	6	1	37.50	6.67	5.33
160	6	2	37.50	6.67	4.44
160	**8**	**0**	**50.00**	**5.00**	**5.00**
160	8	1	50.00	5.00	4.00
160	8	2	50.00	5.00	3.33
40	**1**	**0**	**25.00**	**10.00**	**10.00**
40	1	1	25.00	10.00	8.00
40	1	2	25.00	10.00	6.67
40	**1.5**	**0**	**37.50**	**6.67**	**6.67**
40	1.5	1	37.50	6.67	5.33
40	1.5	2	37.50	6.67	4.44
40	**2**	**0**	**50.00**	**5.00**	**5.00**
40	2	1	50.00	5.00	4.00
40	2	2	50.00	5.00	3.33
40	**3**	**0**	**75.00**	**3.33**	**3.33**
40	3	1	75.00	3.33	2.67
40	3	2	75.00	3.33	2.22
40	**4**	**0**	**100.00**	**2.50**	**2.50**
40	4	1	100.00	2.50	2.00
40	4	2	100.00	2.50	1.67
40	**6**	**0**	**150.00**	**1.67**	**1.67**
40	6	1	150.00	1.67	1.33
40	6	2	150.00	1.67	1.11
40	**8**	**0**	**200.00**	**1.25**	**1.25**
40	8	1	200.00	1.25	1.00
40	8	2	200.00	1.25	0.83

1. Number Xclk's = XCLKS_ST + XCLKH_ST

Register: 0xBE

AIP Control Zero (AIPCNTL0)
Read/Write

7	6	5	4	3	2	1	0
FBAIP	RSQAIP	SEQAIP		R			
0	0	0		0	0	0	0

FBAIP **Force Bad AIP value** **7**
Setting this bit causes bad AIP values to be sent over the SCSI bus.

RSQAIP **Reset AIP Sequence value** **6**
Setting this bit causes the sequence value used in the calculation of the protection code to reset.

SEQAIP **AIP Sequence value** **[5:4]**
These two bits contain the current AIP sequence value. The SEQAIP bits are read only and should only be accessed for diagnostic purposes. The sequence value is automatically reset on every phase change.

R **Reserved** **[3:0]**

Register: 0xBF

AIP Control One (AIPCNTL1)
Read/Write

7	6	5					0
AIPERR	LAIPERR	AIPV					
0	0	0	0	0	0	0	0

AIPERR **AIP Error Status** **7**
This bit represents the live value of the error status for the AIP checking logic. This bit may indicate false errors and should not be used except for diagnostic purposes.

LAIPERR **Latched AIP Error Status** **6**
This bit represents the latched version of the error status for the AIP checking logic. This bit accurately reflects the fact that an AIP error was detected. This bit will be cleared when the Parity/CRC/AIP error bit is cleared in the SIST0 register.

AIPV **AIP Value** **[5:0]**
This value represents the current calculated value of the protection code. This value is based off of the eight SCSI data bits, the three phase signals, the two SCSI Reserved signals, and the Sequence value.

Register: 0xE0-0xE1
CRC Pad Byte Value (CRCPAD)
Read/Write

15							8	7							0
CRCPBV															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CRCPBV **CRC Pad Byte Value** **[15:0]**
This register contains the value placed onto the bus for the CRC pad bytes.

Register: 0xE2
CRC Control Zero (CRCCNTL0)
Read/Write

7	6	5	4	3			0
DCRCC	DCRCPC	RCRCIC	R	CRCRI[3:0]			
0	0	0	0	0	0	0	0

DCRCC **Disable CRC Checking** **7**
Setting this bit causes the internal logic to neither check or report CRC errors during Ultra3 transfers. The SYM53C1010 continues to calculate and send CRCs as requested by the target according to the SPI-3 specification.

DCRCPC **Disable CRC Protocol Checking** **6**
Setting this bit causes the internal logic to neither check or report CRC protocol errors during Ultra3 transfers. The SYM53C1010 continues to calculate and send CRCs as requested by the target according to the SPI-3 specification but does not set a SGE interrupt if a CRC protocol error occurs.

RCRCIC **Reset CRC Interval Counter (Target Mode Only)** **5**
Setting this bit resets the internal CRC interval counter to zero. This bit is self clearing.

R **Reserved** **4**

CRCRI[3:0] **CRC Request Interval (Target Mode Only)** **[3:0]**
These bits determine when a CRC request is to be sent by the device when operating in the target mode and transferring data in the DT Data-In or DT Data-Out phases. The interval is independent of individual block moves, allowing consistent CRC requests across multiple block moves of varying byte counts as in scatter gather types of operations. The following table defines the valid CRC request intervals. A setting of zero will disable the automatic CRC request interval and the device will not request a CRC at any time. The SPI-3 specification states that all DT Data-In and DT Data-Out phases must end with a CRC transfer. Thus, to maintain compliance with the SPI-3 specification it is necessary to manually request a CRC by executing a force CRC Block Move instruction.

CRCRI	Interval (Bytes)
0x0	Disabled
0x1	128
0x2	256
0x3	512
0x4	1024
0x5	2048
0x6	4096
0x7	8192
0x8	16384
0x9	32768
0xA	65536
0xB	Reserved
0xC	Reserved
0xD	Reserved
0xE	Reserved
0xF	Reserved

Register: 0xE3

CRC Control One (CRCCTNL1)
Read/Write

7	6	5	4	3	2	1	0
CRCERR	R	ENAS	TSTSD	TSTCHK	TSTADD	CRCDSEL	
0	0	0	0	0	0	0	0

CRCERR **CRC Error** **7**
This bit indicates whether or not a CRC error has been detected during a DT Data-In SCSI transfer. This bit is set independent of the DISCRCCHK bit. To clear this condition, either write this bit to a 1 or read the SIST0 and SIST1 registers. When CRC Checking and the Parity/CRC/AIP Error Interrupt are enabled, this error condition is also indicated as a Parity/CRC/AIP error (bit 0 of the SIST0 register).

R **Reserved** **6**

ENAS **Enable CRC Auto Seed** **5**
Setting this bit causes the CRC logic to automatically re-seed after every CRC check performed during DT Data-In SCSI transfers. When this bit is clear, the SCSI control logic controls when the re-seeding occurs.

TSTSD **Test CRC Seed** **4**
Setting this bit causes the CRC logic to immediately re-seed itself. This bit should never be set during normal operation as it causes corrupt CRCs to be generated.

TSTCHK **Test CRC Check** **3**
Setting this bit causes the CRC logic to initiate a CRC check. This bit should never be set during normal operation as it results in spurious CRC errors.

TSTADD **Test CRC Accumulate** **2**
Setting this bit causes the CRC block to take the value in its input register and add it into the current CRC calculation, resulting in a new output CRC value. This bit should not be set during normal operation as it results in corrupt CRC values.

CRCDSEL **CRC Data Register Selector** **[1:0]**
These bits control the data that is visible in the CRC Data (CRCDATA) register.

Register: 0xE4-0xE7
CRC Data (CRCD)
Read/Write

31	24	23	16	15	8	7	0
CRCD							
If CRCDSEL is 0b00, 0b01, 0b10, or 0b11:							
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x							

CRCD **CRC Data** **[31:0]**
The value in this register is dependent upon the value of the CRCDSEL[1:0] bits in the CRC Control One (CRCCTNL1) register.

If CRCDSEL = 0b00, this register represents the Current CRC Value and is the current value of the CRC calculation. After sending data during the DT Data-Out phase this register contains the CRC calculation, if no CRC request occurred during the transfer. In this mode, this register is read only.

If CRCDSEL = 0b01, this register represents the CRC Input Register and contains its current value. It contains the SCSI data transferred to or from the SCSI bus during a DT transfer phase. In this mode this register can be written to manually alter the input data used for CRC calculation. For normal operations, this register should never be written to.

If CRCDSEL = 0b10, this register represents the CRC Accumulator and contains its current value. In this mode this register can be written to in order to manually modify the value in the accumulator. This register should not be written to during normal operation as corrupt CRC values result.

If CRCDSEL = 0b11, this register represents the Bad CRC Saved and contains the saved CRC value that was calculated when a CRC error was detected. After a CRC error is detected this register is not be over-written until the error condition is cleared.

Register: 0xF0-0xF1
DMA FIFO Byte Count (DFBC)
Read Only

15							8	7							0
DFBC															
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

DFBC **DMA FIFO Byte Count** **[15:0]**
This 16 bit read only register contains the actual number of bytes contained in the DMA FIFO. This register is not stable while data is actually being transferred. This register can be used during error recovery.

3.3 Shadowed Registers

Note: For more information concerning shadow registers, refer to the Chip Test Four (CTEST4), Scratch Register A (SCRATCHA), Scratch Register B (SCRATCHB), Memory Move Read Selector (MMRS), Memory Move Write Selector (MMWS), and SCRIPT Fetch Selector (SFS) register descriptions.

Registers: 0x34–0x37
Shadowed Scratch Register A (SCRATCHA)
Read/Write

31								24	23							16	15							8	7							0
SCRATCHA																																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCRATCHA **Scratch Register A** **[31:0]**

Register: 0x42

Shadowed SCSI SGE Status 0
Read/Write

7	6	5	4	3	2	1	0
R	R	RD	PCO	OO	OU	DO	DU
0	0	0	0	0	0	0	0

This register contains the individual status bits which cause a SGE SCSI interrupt. These bits correspond to the SGE conditions described in the SIST0 register description. Unlike the other registers in the device, these bits are write '1' to clear. This register is shadowed behind the SIST registers. Setting bit 4 (STRM) in the Chip Test Four (CTEST4) register, enables access to this register.

R	**Reserved**	**[7:6]**
RD	**Residual Data in SCSI FIFO**	**5**
PCO	**Phase Change with outstanding Offset**	**4**
OO	**Offset Overflow**	**3**
OU	**Offset Underflow**	**2**
DO	**Data Overflow**	**1**
DU	**Data Underflow**	**0**

Register: 0x43

Shadowed SCSI Interrupt Status One (SIST1)
Read Only

7		5	4	3	2	1	0
R	R	PNCRC	FCRC	DTST	NFCRC	MCRC	R
0	0	0	0	0	0	0	0

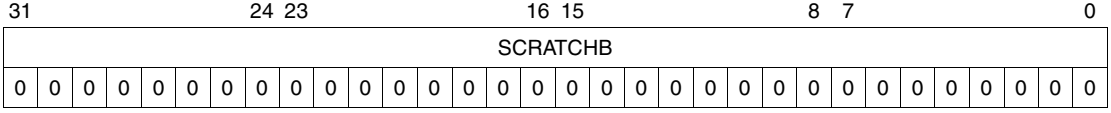
This register contains the individual status bits which cause a SGE SCSI interrupt. These bits correspond to the SGE conditions described in the SIST0 register description. Unlike the other registers in the device, these

bits are write “1” to clear. This register is shadowed behind the SIST registers. Setting bit 4 (STRM) in the Chip Test Four (CTEST4) register, enables access to this register.

R	**Reserved**	**[7:6]**
PNCRC	**Pad Request with no CRC Request Following**	**5**
FCRC	**Force CRC**	**4**
DTST	**Switch from DT to ST timings during a transfer**	**3**
NFCRC	**Phase Change with no final CRC Request**	**2**
HTH	**Multiple CRC Requests with the same offset**	**1**
R	**Reserved**	**0**

Registers: 0x5C–0x5F

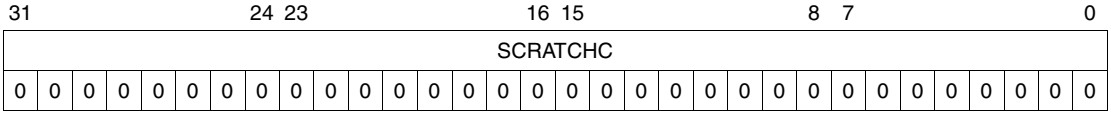
Shadowed Scratch Register B (SCRATCHB)
Read/Write



SCRATCHB	**Scratch Register B**	**[31:0]**

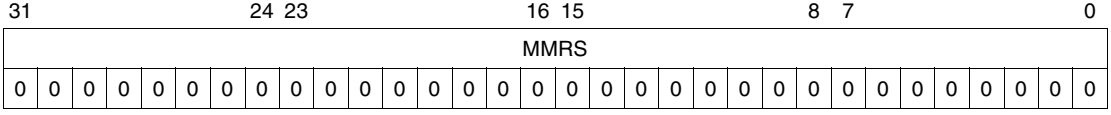
Registers: 0x60–0x9F

Shadowed Scratch Registers C–R (SCRATCHC–SCRATCHR)
Read/Write



Register: 0xA0–0xA3

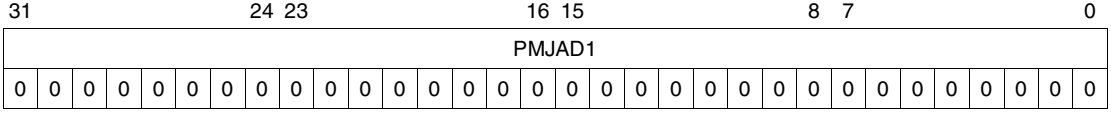
Shadowed Memory Move Read Selector (MMRS)
Read/Write



MMRS **Shadowed Memory Move Read Selector** **[31:0]**

Register: 0xA4–0xA7

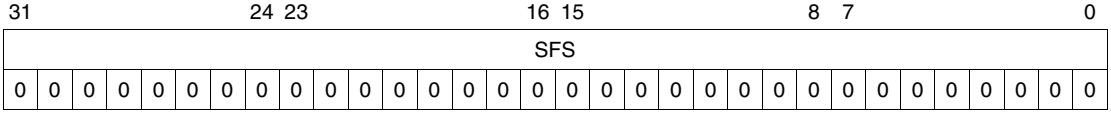
Shadowed Memory Move Write Selector (MMWS)
Read/Write



MMWS **Shadowed Memory Move Write Selector** **[31:0]**

Register: 0xA8–0xAB

Shadowed SCRIPT Fetch Selector (SFS)
Read/Write



SFS **Shadowed SCRIPT Fetch Selector** **[31:0]**