Integrating BIOS and 1030 Firmware into the System BIOS

Systems Engineering Note

SEN S11056 Version 1.0

1 Revision Record

Revision	Date	Remarks
Version 1.0	01/2004	Initial release of document

2 Downloading the Firmware

Firmware download boot is utilized by patching offset 0x40 into the MPT option ROM image. The system BIOS stores the physical 32-bit address of the 1030 firmware into the memory location at offset 0x40 from the start of the BIOS image in RAM. The system BIOS must somehow make a copy of the 1030 firmware available at a memory location that is addressable in physical memory by a 32-bit physical memory address. The image can be in system RAM, or it could be a flash part mapped into the 32-bit memory address space.

The patch must occur before the option ROM is executed. The checksum of the original ROM image can be verified before adding the patch to the ROM image. The process of patching the ROM image is described in detail below:

1. The system BIOS moves the LSI option ROM BIOS image into memory (usually at C800:0000–C800:FFFF) The memory can still be read or written.

   The system BIOS knows how much memory space is required.

2. Edit the option ROM resident in memory to place the 32-bit memory address location of the FW image into offset 0x40 (usually C800:0040). Firmware download boot requires that the firmware image reside in the lower 4 Gbytes of memory and that it be contained entirely in it.

3. (Optional) Re-compute the LSI option ROM BIOS checksum after patching memory address 0x40. If the checksum is not re-computed, the system BIOS must check the checksum prior to the 0x40 address patch.

   Verifying the checksum after the patch without recalculation may result in an 'Adapter Malfunction Error' when the BIOS loads, or the system BIOS may report an error and refuse to initialize the option ROM.

4. After patching and executing the option ROM, the SCSI option ROM BIOS checks the bad flash bit of each 1020/1030 device in a system. If the bit is set, it downloads the firmware to each device.

3 Updating the checksum

To update the checksum, update the end of the code, last address or size minus 1 with the new checksum:

The normal operation is to retrieve the last byte, add the 4 bytes at 0040–0043 (ignoring overflow), complement it, and add it to the previous last byte. 0040–0043 were 00 00 00 00 and last byte = 00

- 0040–0043 change to 80 00 FF FE (FEFF0080)
- 0040–0043 byte add = 27D = 7D
- Complement 7D = 83
- 83 plus last byte (pretend it was 00 to start with) = 83
- Re-checksum the image (all the other bytes add to 00) plus 83 plus 27D = 300 = 00 and the checksum is good.

4 Additional Considerations

If a 1020/1030 device with a flash part is placed in the system, the system firmware will not be loaded onto it. Instead, the firmware from its flash is used.

The patched option ROM must be run first. If a non-patched option ROM is executed first (for example, loaded from the flash memory on a HAB installed in the system), the firmware download boot process does not

occur. Hence, the onboard 1030 fails and the ‘Adapter Malfunction Error’ occurs when the BIOS attempts to run.

The sizes for the option ROM are currently ~64 Kbytes. Its runtime code size is around 15 Kbytes for code and 5140 bytes maximum for data (1200 bytes is a more normal size). The chip uses approximately 2–4 Kbytes of EBDA area memory if it is available within the system. All of the data area is left in the EBDA.

The IM firmware is at 64 Kbytes today. The non-IM firmware is slightly smaller in binary image size. There is currently a hard limit at 96 Kbytes.

The 1020/1030 requires an SEEPROM for storage of persistent data.

Connections to the ICE pins must be made available either with a header or vias. Providing ICE connections allows LSI Logic to debug the 53C1030 firmware if necessary.

Provide access to the GPIO and MAD bus pins to allow for setting up the Test MUX capabilities of the 53C1030. This allows LSI Logic to debug any suspect hardware issues.

Notes

Headquarters

LSI Logic Corporation
North American Headquarters
Milpitas CA
Tel: 408.433.8000

LSI Logic Europe Ltd
European Headquarters
Bracknell England
Tel: 44.1344.413200
Fax: 44.1344.413254

LSI Logic K.K.
Headquarters
Tokyo Japan
Tel: 81.3.5463.7821
Fax: 81.3.5463.7820

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