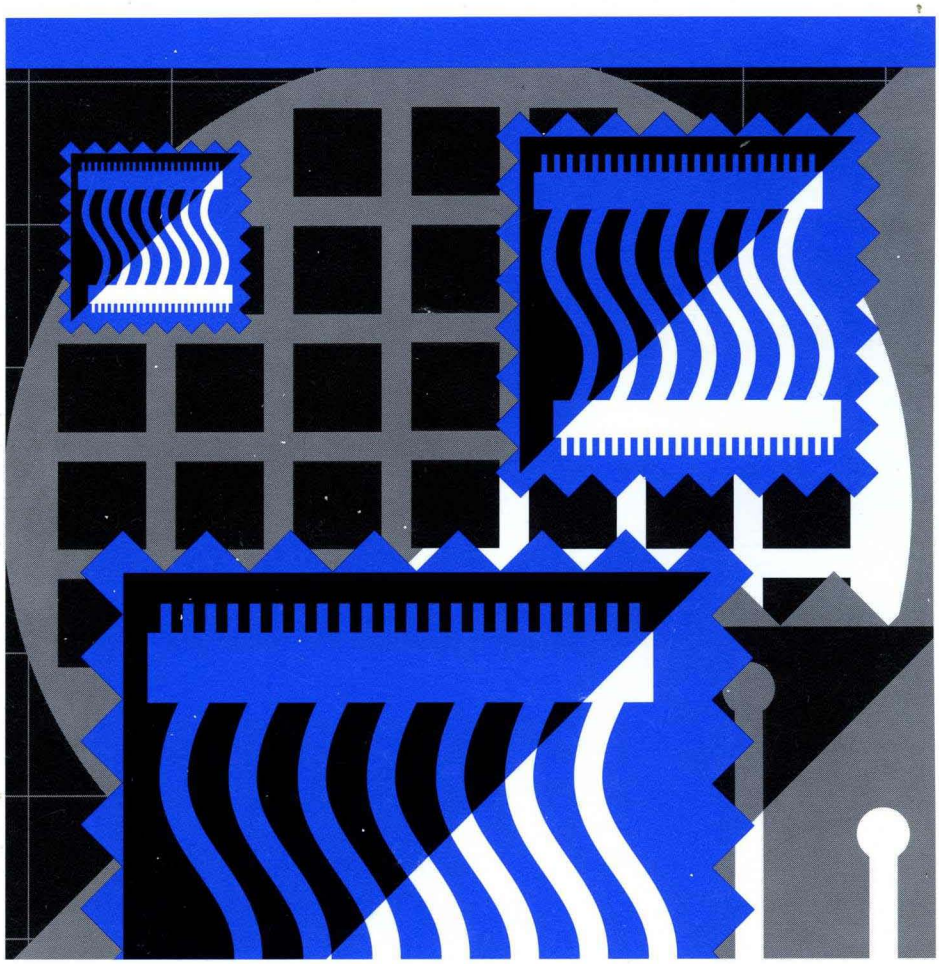
NCR 53C810
PCI-SCSI I/O Processor



Data Manual

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PCI-SCSI I/O Processor

NCR

Data Manual

INCREASING SCSI RELIABILITY
TolerANT
ACTIVE NEGATION TECHNOLOGY

Revision Record

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n/a	10/92	Second Draft
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Preface

SCSI and PCI Reference Information

This manual assumes some prior knowledge of current and proposed SCSI and PCI standards. For background information, please contact:

ANSI
11 West 42nd Street
New York, NY 10036
(212) 642-4900
Ask for document number X3.131-1986 (SCSI-1)

Global Engineering Documents
2805 McGaw
Irvine, CA 92714
(800)-854-7179 or (714) 261-1455
Ask for document number X3.131-199X (SCSI-2)

ENDL Publications
14426 Black Walnut Court
Saratoga, CA 95070
(408) 867-6642
Document names: *SCSI Bench Reference, SCSI Encyclopedia*

Prentice Hall
Englewood Cliffs, NJ 07632
(201) 767-5937
Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

NCR Microelectronic Products Division Electronic Bulletin Board
(719) 596-1649

SCSI Electronic Bulletin Board
(719) 574-0424

PCI Special Interest Group
C/O Intel Corporation
52000 NE Elam Young Parkway, HF 3-15
Hillsboro, OR 97123
(503) 696-2000

Table of Contents

Chapter Three

PCI Functional Description

Chapter Four

Signal Descriptions

Chapter One
SCSI I/O Processor Description

General Description

The NCR 53C810 PCI-SCSI I/O Processor is based on the NCR 53C7XX I/O Processor architecture with a Peripheral Component Interconnect (PCI) front end. The NCR 53C810 integrates a high-performance SCSI core and a PCI bus master DMA core with a SCSI SCRIPTS™ processor to accommodate the flexibility requirements of not only SCSI-1 and SCSI-2, but future SCSI standards as well. The NCR 53C810 solves the protocol overhead problems that have plagued previous intelligent and non-intelligent adapter designs.

The NCR 53C810 has been designed to "gluelessly" connect to the emerging industry standard PCI Bus. An entire SCSI solution, including a SCSI oscillator (40MHz), termination electronics, and an external connector, is illustrated in Figure 1-1. This design can be implemented on less than four square inches of space on the motherboard. In addition to the required PCI pins, the NCR 53C810 provides three other signals useful in adapter plug-in card designs.

The chip is fully supported by NCR SCSI Device Management System (SDMS™) software, that supports the Advanced SCSI Protocol Interface (ASPI) and the ANSI Common Access Method (CAM). The NCR 53C810 is packaged in a 100-pin PQFP package, operates the SCSI bus at 5 MB/s asynchronously or 10 MB/s synchronously, and bursts data to the host at full PCI speeds.

The NCR 53C810 is designed to implement multi-threaded I/O algorithms with a minimum of processor intervention. The NCR 53C810 provides automatic relocation of SCRIPTS by using Table Indirect and Relative addressing. All of the SCRIPTS code may be placed in PROM. The NCR 53C810 allows easy firmware upgrades and is supported by advanced SCRIPTS commands.

NCR TolerANT Technology

The NCR 53C810 features NCR TolerANT® technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation causes the SCSI Request, Acknowledge, Data, and Parity signals to be actively driven high. Active negation is enabled by setting bit 7 in the STEST3 register.

TolerANT receiver technology improves data integrity in unreliable cabling environments, where other devices would be subject to data corruption. TolerANT receivers filter the SCSI bus signals to eliminate unwanted transitions without the long signal delay associated with RC-type input filters. This improved driver and receiver technology helps eliminate the double clocking of data, the single biggest reliability issue with SCSI operations. TolerANT input signal filtering is a built in feature of the NCR 53C810 and all NCR fast SCSI devices. On the NCR 53C810, the filtering period is user-selectable at 30 or 60 ns, with bit 1 in the STEST2 register.

The benefits of TolerANT include increased immunity to noise when the signal is going high, increased performance due to balanced duty cycles, and improved fast SCSI transfer rates. TolerANT is compatible with both the Alternative One and Alternative Two termination schemes proposed by the American National Standards Institute.

NCR 53C810 Benefits Summary

Performance

- Supports variable block size and scatter/gather data transfers.
- Supports 32-bit word data bursts with variable burst lengths
- Performs sustained memory-to-memory DMA transfers in excess of 47 MB/s (@ 33 MHz)
- Zero wait-state bus master data bursts in excess of 110 MB/s (@ 33 MHz)
- Minimizes SCSI I/O start latency
- Performs complex bus sequences without interrupts, including restore data pointers
- Unique interrupt status reporting method reduces ISR overhead
- Performs high-speed async/sync single-ended SCSI bus transfers
  - 5 MB/s asynchronous
  - 10 MB/s synchronous
- 64-byte DMA FIFO

Integration

- Full 32-bit PCI DMA bus master
- Optionally can be used as a third-party PCI bus DMA controller by using the Memory to Memory Move instructions.
- High performance SCSI core
- Integrated SCRIPTS processor
- 100-pin PQFP reduces board space requirements

Ease of Use

- Direct PCI-to-SCSI connection
- Reduces SCSI development effort
- Easily adapted to the Advanced SCSI Protocol Interface (ASPI) or Common Access Method (CAM)
- Compiler-compatible with existing NCR 53C7X0 SCRIPTS
- Direct connection to PCI and single-ended SCSI buses
- Development tools and SCSI SCRIPTS available
- All interrupts are maskable and pollable
- Three programmable SCSI timers: Select/ Reselect, Handshake-to-Handshake, and General Purpose. The time-out period is programmable from 100 µs to greater than 1.6 seconds
- Fully supported by NCR SDMS software for complex PC-based operating system support

Flexibility

- High level programming interface (SCSI SCRIPTS)
- Allows tailored SCSI sequences to be executed from main memory
- Flexible sequences to tune I/O performance or to adapt to unique SCSI devices
- Accommodates changes in the logical I/O interface definition
- Low level access to all registers and all SCSI bus signals
- Allows a target to disconnect and later reselect with no interrupt to the system processor
- Allows a multi-threaded I/O algorithm to be executed in SCSI SCRIPTS with fast I/O context switching

- Allows relative jumps
- Fetch, Master, and Memory Access control pins
- Allows indirect fetching of DMA address and byte counts so that SCRIPTS can be placed in a PROM
- Separate SCSI and system clocks

Reliability

- 2 K volts ESD protection on SCSI signals
- Typical 300 mV SCSI bus hysteresis
- Protection against bus reflections due to impedance mismatches
- Controlled bus assertion times (reduces RFI, improves reliability, and eases FCC certification)
- Latch-up protection greater than 150 mA
- Voltage feed through protection (minimum leakage current through SCSI pads)
- 25% of pins are power and ground
- Power and ground isolation of I/O pads and internal chip logic
- NCR TolerANT technology provides:
  - Active negation of SCSI Data, Parity, Request, and Acknowledge signals for improved fast SCSI transfer rates.
  - Input signal filtering on SCSI receivers; improves data integrity, even in noisy cabling environments.

Testability

- All SCSI signals accessible through programmed I/O
- SCSI loopback diagnostics
- SCSI bus signal continuity checking
- Supports single-step mode operation
- Test mode (AND tree) to check pin continuity to the board

Figure 1-1. SCSI Port Logic

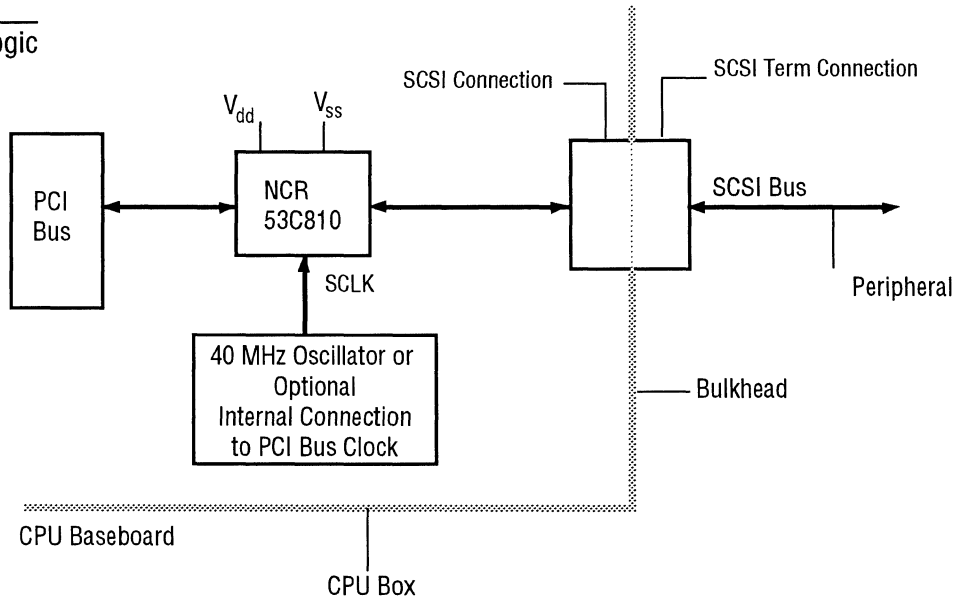
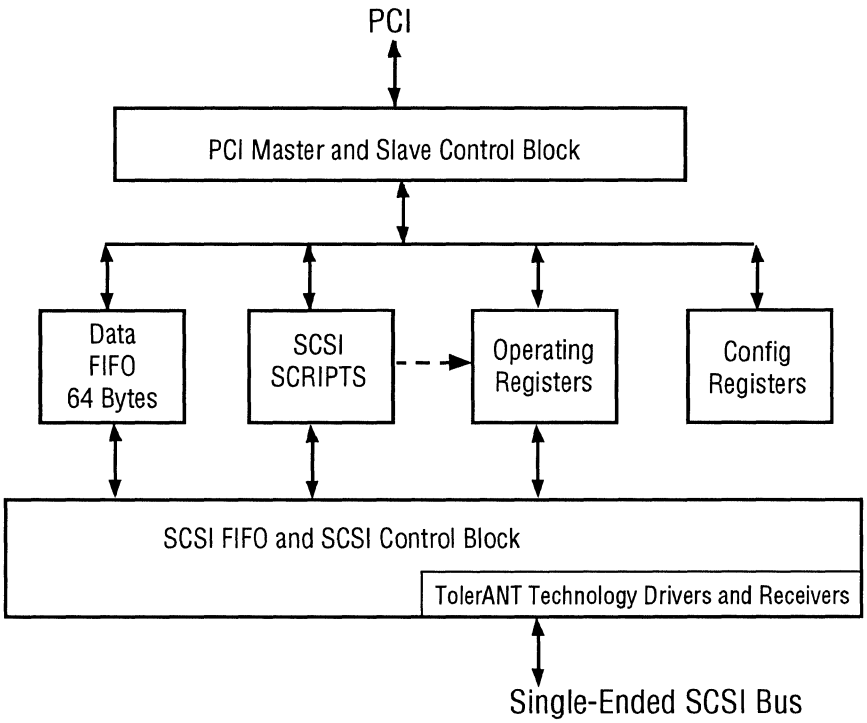


Figure 1-2. NCR 53C810 Block Diagram



Chapter Two

Functional Description

The NCR 53C810 is composed of three functional blocks: the SCSI Core, the DMA Core, and the SCRIPTS Processor. The NCR 53C810 is fully supported by the SCSI Device Management System (SDMS), a complete software package that supports the NCR product line of SCSI processors and controllers.

SCSI Core

The SCSI core supports the SCSI-2, 8-bit bus. It supports synchronous transfer rates up to 10 MB/s, and asynchronous transfer rates up to 5 MB/s. The programmable SCSI interface makes it easy to "fine tune" the system for specific mass storage devices or SCSI-2 requirements.

The SCSI core offers low-level register access or a high-level control interface. Like first generation SCSI devices, the NCR 53C810 SCSI core can be accessed as a register-oriented device. The ability to sample and/or assert any signal on the SCSI bus can be used in error recovery and diagnostic procedures. In support of loopback diagnostics, the SCSI core may perform a self-selection and operate as both an initiator and a target. The NCR 53C810 can test the SCSI pins for physical connection to the board or the SCSI bus.

The NCR 53C810 SCSI core can be controlled by the integrated SCRIPTS processor through a high-level logical interface. Commands controlling the SCSI core are fetched out of the main host memory or local memory. These commands instruct the SCSI core to Select, Reselect, Disconnect, Wait for a Disconnect, Transfer Information, Change Bus Phases and in general, implement all aspects of the SCSI protocol. The SCRIPTS processor is a special high-speed processor optimized for SCSI protocol.

DMA Core

The DMA core is a bus master DMA device that is made to attach directly to the industry standard PCI Bus. The DMA core is tightly coupled to the SCSI core through the SCRIPTS processor, which supports uninterrupted scatter/gather memory operations.

The NCR 53C810 supports 32-bit memory and automatically supports misaligned DMA transfers. A 64-byte FIFO allows the NCR 53C810 to support two, four, eight, or sixteen longword bursts across the PCI bus interface.

SCRIPTS Processor

The SCSI SCRIPTS processor allows both DMA and SCSI instructions to be fetched from host memory. Algorithms written in SCSI SCRIPTS control the actions of the SCSI and DMA cores and are executed from 32-bit system memory. Complex SCSI bus sequences are executed independently of the host CPU.

The SCRIPTS processor can begin a SCSI I/O operation in approximately 500 ns. This compares with 2-8 ms required for traditional intelligent host adapters. Algorithms may be designed to tune SCSI bus performance, to adjust to new bus device types (i.e., scanners, communication gateways, etc.), or to incorporate changes in the SCSI-2 or SCSI-3 logical bus definitions without sacrificing I/O performance. SCSI SCRIPTS are independent of the type of CPU or system bus in use.

The NCR 53C810 can be programmed with advanced SCSI SCRIPTS. A complete set of development tools is available for writing custom drivers with SCSI SCRIPTS. For more information on SCSI SCRIPTS commands supported by the NCR 53C810, see Chapter Six, "Instruction Set of the I/O Processor."

SDMS: The Total SCSI Solution

For users who do not need to develop custom drivers, NCR provides a total SCSI solution in PC environments with the NCR SCSI Device Management System (SDMS). SDMS provides BIOS driver support for hard disk, tape, and removable media peripherals for the DOS, Windows, and Novell operating environments.

The SDMS includes a SCSI BIOS, resident in the SCSI controller or processor, to manage all SCSI functions related to the device. SDMS also provides a series of SCSI device drivers that support most major operating systems. SDMS supports a multi-threaded I/O application programming interface (API) for user-developed SCSI applications.

Loopback Mode

The NCR 53C810 loopback mode allows testing of both initiator and target functions and, in effect, lets the chip communicate with itself. When the Loopback Enable bit is set in the STEST1 register, the NCR 53C810 allows control of all SCSI signals, whether the NCR 53C810 is operating in initiator or target mode.

Parity Options

The NCR 53C810 implements a flexible parity scheme that allows control of the parity sense, allows parity checking to be turned on or off, and has the ability to deliberately send a byte with bad parity over the SCSI bus to test parity error recovery procedures. The following bits are involved in parity control and observation:

1) Assert SATN/ on Parity Errors – Bit 1 in the SCNTL0 register. This bit causes the NCR 53C810 to automatically assert SCSI SATN/ when it detects a parity error while operating as an initiator.

2) Enable Parity Checking – Bit 3 in the SCNTL0 register. This bit enables the NCR 53C810 to check for parity errors. The NCR 53C810 checks for odd parity.

3) Assert Even SCSI Parity – Bit 2 in the SCNTL1 register. This bit determines the SCSI parity sense generated by the NCR 53C810 to the SCSI bus.

4) Disable Halt on SATN/ or a Parity Error (Target Mode Only) – Bit 5 in the SCNTL1 register. This bit causes the NCR 53C810 to halt operations when a parity error is detected in target mode.

5) Enable Parity Error Interrupt – Bit 0 in the SIEN0 register. This bit determines whether the NCR 53C810 will generate an interrupt when it detects a SCSI parity error.

6) Parity Error – Bit 0 in the SIST0 register. This status bit is set whenever the NCR 53C810 has detected a parity error on the SCSI bus.

7) Status of SCSI Parity Signal – Bit 0 in the SSTAT0 register. This status bit represents the live SCSI Parity Signal (SDP).

8) Latched SCSI Parity Signal – Bit 3 in the SSTAT1 register.

9) Master Parity Error Enable – Bit 3 in the CTEST4 register. Setting this bit enables parity checking during master data phases.

10) Master Data Parity Error – Bit 6 in the DSTAT register. This bit is set when the NCR 53C810 as a master detects that a target device has signalled a parity error during a data phase.

11) Master Data Parity Error Interrupt Enable – Bit 6 in the DIEN register. By clearing this bit, a Master Data Parity Error will not cause IRQ/ to be asserted, but the status bit will be set in the DSTAT register.

Table 2-1. SCSI Parity Control

EPC	ASEP	Description
0	0	Will not check for parity errors. Parity is generated when sending SCSI data. Asserts odd parity when sending SCSI data.
0	1	Will not check for parity errors. Parity is generated when sending SCSI data. As serts even parity when sending SCSI data.
1	0	Checks for odd parity on SCSI data received. Parity is generated when sending SCSI data. Asserts odd parity when sending SCSI data.
1	1	Checks for odd parity on SCSI data received. Parity is generated when sending SCSI data. Asserts even parity when sending SCSI data.

Key: *EPC = Enable Parity Checking (bit 3 SCNTL0)*
ASEP = Assert SCSI Even Parity (bit 2 SCNTL1)

Table 2-2. SCSI Parity Errors and Interrupts

This table describes the options available when a parity error occurs. This table only applies when the Enable Parity Checking bit is set.

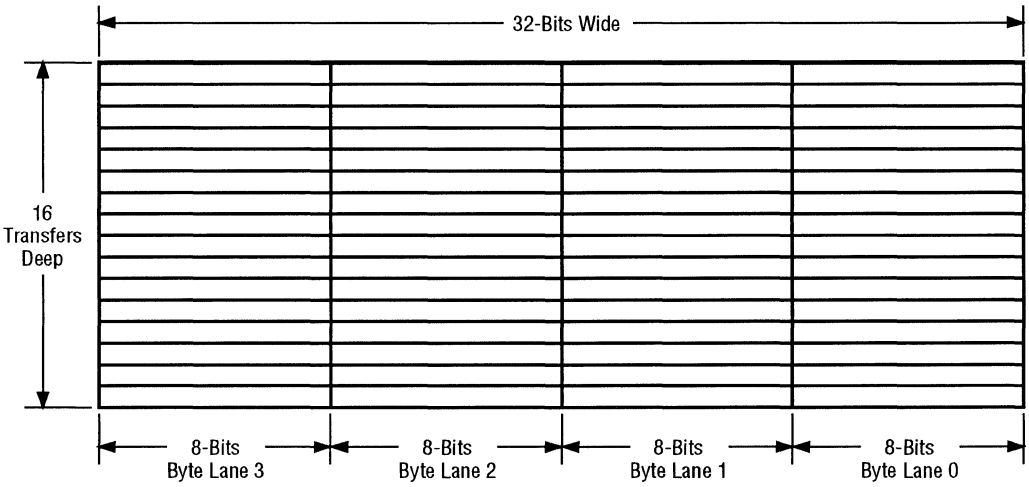
DHP	PAR	Description
0	0	Will halt when a parity error occurs in target or initiator mode and will NOT generate an interrupt.
0	1	Will halt when a parity error occurs in target mode and will generate an interrupt in target or initiator mode.
1	0	Will not halt in target mode when a parity error occurs until the end of the transfer. An interrupt will not be generated.
1	1	Will not halt in target mode when a parity error occurs until the end of the transfer. An interrupt will be generated.

Key: *DHP = Disable Halt on SATN/ or Parity Error (bit 5 SCNTL1)*
PAR = Parity Error (bit 0 SIEN0)

DMA FIFO

The DMA FIFO is 32 bit by 16 transfers deep. It is divided into 4 sections, each 8 bits wide and 16 transfers deep.

Figure 2-1. DMA FIFO Sections



Data Paths

The data path through the NCR 53C810 is dependent on whether data is being moved into or out of the chip, and whether SCSI data is being transferred asynchronously or synchronously.

Figure 2-2 shows how data is moved to/from the SCSI bus in each of the different modes.

The following steps will determine if any bytes remain in the data path when the chip halts an operation:

Asynchronous SCSI Send:

1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between zero and 64.
2) Read bit 5 in the SSTAT0 register to determine if a byte is left in the SODL register. If bit 5 is set in SSTAT0, then the SODL register is full.

Synchronous SCSI Send:

1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between zero and 64.
2) Read bit 5 in the SSTAT0 register to determine if a byte is left in the SODL register. If bit 5 is set in the SSTAT0, then the SODL register is full.
3) Read bit 6 in the SSTAT0 register to determine if any bytes are left in the SODR register. If bit 6 is set in SSTAT0, then the SODR register is full.

Asynchronous SCSI Receive:

1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between 0 and 64.

2) Read bit 7 in the SSTAT0 register to determine if a byte is left in the SIDL register. If bit 7 is set in SSTAT0, then the SIDL register is full.

Synchronous SCSI Receive:

1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between 0 and 64.

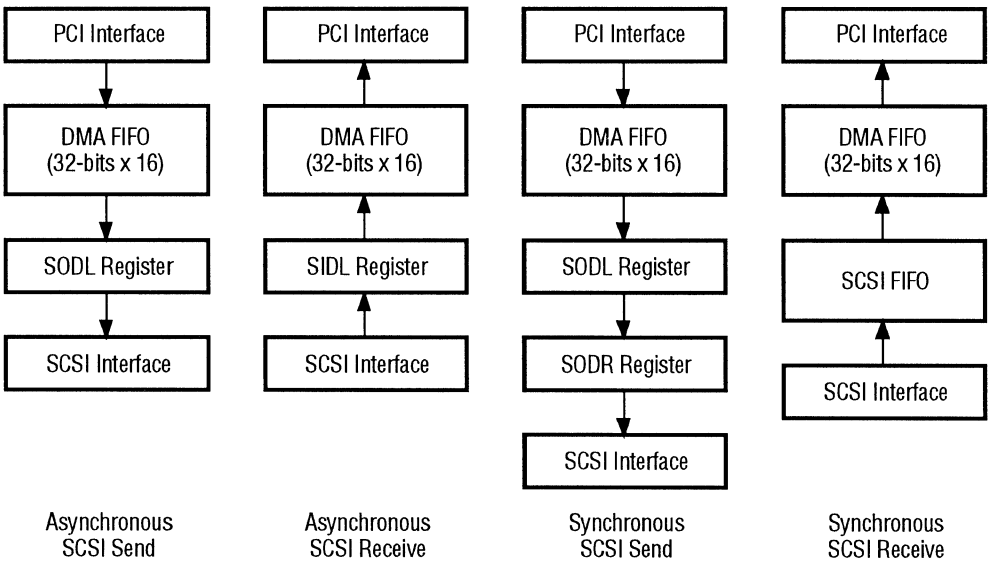
2) Read the SSTAT1 register and examine bits 7-4, the binary representation of the number of valid bytes in the SCSI FIFO, to determine if any bytes are left in the SCSI FIFO.

SCSI Bus Interface

The NCR 53C810 is intended for use in single-ended applications and does not support differential operation.

All SCSI signals are active low. The NCR 53C810 contains the single ended output drivers and can be connected directly to the SCSI bus. Each output is isolated from the power supply to ensure that a powered-down NCR 53C810 has no effect on an active SCSI bus (CMOS "voltage feed-through" phenomena). NCR TolerANT technology provides signal filtering at the inputs of SREQ/ and SACK/ to increase immunity to signal reflections.

Figure 2-2. NCR 53C810 Host Interface Data Paths



Terminator Networks

The terminator networks provide the biasing needed to pull signals to an inactive voltage level, and to match the impedance at the end of the cable with the characteristic impedance of the cable. Terminators must be installed at the extreme ends of the SCSI cable, and only at the ends; no system should ever have more or less than two terminators installed and active. SCSI host adapters should provide a means of accommodating terminators. The terminators should be socketed, or have a means of disabling them with software, so they can be removed if not needed.

Single-ended cables can use a 220 Ω pullup to the terminator power supply (Term-Power) line and a 330 Ω pull-down to Ground. Because of the high-performance nature of the NCR 53C810, Alternative Two termination (defined in the ANSI SCSI-2 standard) is recommended. This method employs a 2.85 volt regulator and 110 Ω pullup resistors (no pull-down). Figure 2-3 shows the schematics for Alternative Two termination. For additional information, refer to the SCSI-2 Specification. TolerANT active negation can be used with either termination network.

(Re)Select During (Re)Selection

In multi-threaded SCSI I/O environments, it is not uncommon to be selected or reselected while trying to perform selection/reselection. This situation may occur when a SCSI controller (operating in initiator mode) tries to select a target and is reselected by another. The SELECT SCRIPT instruction has an alternate address to which the SCRIPTS will jump when this situation occurs. The analogous situation for target devices is being selected while trying to perform a reselection.

Once a change in operating mode occurs, the initiator SCRIPTS should start with a SET INITIATOR instruction or the target SCRIPTS should start with a SET TARGET instruction. It should be noted that the Selection and Reselection Enable bits (SCID bits 5 and 6, respectively) should both be asserted so that the NCR 53C810 may respond as an initiator or as a target. If only selection is enabled, the NCR 53C810 cannot be reselected as an initiator. There are also status and interrupt bits in the SIST0 and SIEN0 registers, respectively, indicating if the NCR 53C810 has been selected (bit 5) and reselected (bit 4).

Synchronous Operation

The NCR 53C810 can transfer synchronous SCSI data in both initiator and target modes. The SXFER register controls both the synchronous offset and the transfer period, and may be loaded by the CPU before SCRIPTS execution begins, from within SCRIPTS via a table indirect I/O instruction, or with a read-modify-write instruction.

The NCR 53C810 can receive data from the SCSI bus at a synchronous transfer period as short as 80 ns or 160 ns (with a 50 MHz clock), regardless of the transfer period used to send data. Then NCR 53C810 can receive data at four times the SCLK period. Depending on the SCLK frequency, the negotiated transfer period, and the synchronous clock divider, the NCR 53C810 can send synchronous data at intervals as short as 100 ns for fast SCSI and 200 ns for slow SCSI.

Determining the Data Transfer Rate

Synchronous data transfer rates are controlled by bits in two different registers of the NCR 53C810. A brief description of the bits is provided below. Figure 2-3 illustrates the clock division factors used in each register, and the relationship between the registers in determining the transfer rate.

Register 03 (00) SCSI Control 3 (SCNTL3) - bits 6 (SCF2), 5 (SCF1), 4 (SCF0)

SCF2-0 bits selects the factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. The output from this divider must not exceed 50 MHz.

Register 03 (00) SCSI Control 3 (SCNTL3) - bits 2 (CCF2), 1 (CCF1), 0 (CCF0)

CCF2-0 bits selects the factor by which the frequency of SCLK is divided before being presented to the asynchronous SCSI core logic. This divider must be set according to the input clock frequency in the table.

Register 05 (06) SCSI Transfer (SXFER) - bits 7 (TP2), 6 (TP1), 5 (TP0)

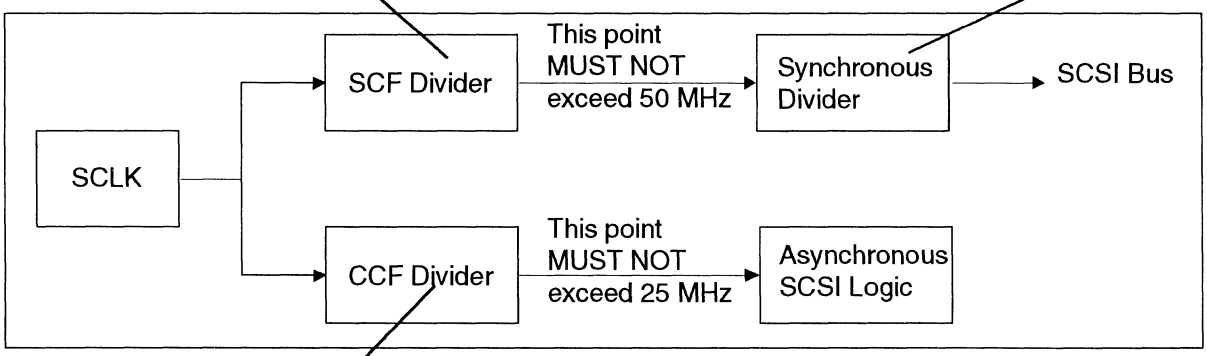
TP2-0 determines the SCSI synchronous transfer period when sending synchronous SCSI data in either initiator or target mode.

These bits control the programmable dividers in the chip. Following are tables of these bits and the division factors they produce. The illustration shows how the chip uses the divisors.

Figure 2-3. Determining the NCR 53C810 Transfer Rate

SCF2	SCF1	SCF0	SCF Divisor
0	0	1	1
0	1	0	1.5
0	1	1	2
1	0	0	3
0	0	0	3

TP2	TP1	TP0	XFERP Divisor
0	0	0	4
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	11



CCF2	CCF1	CCF0	CCF Divisor
0	0	1	1
0	1	0	1.5
0	1	1	2
1	0	0	3
0	0	0	3

SCLK (SCSI Clock) Frequency	Example:
16.667 - 25.00 MHz	SCLK=40 MHz, SCF=1, XFERP=4,
25.01 - 37.50 MHz	SCSI transfer rate=10 MHz, CCF=2
37.51 - 50.00 MHz	(40 MHz÷1=synchronous core rate)
50.01 - 75.00 MHz	(40 MHz÷4=10 MHz synchronous rate=10mB/sec.)

Interrupt Handling

The SCRIPTS processor in the NCR 53C810 performs most functions independently of the host microprocessor. However, certain interrupt situations must be handled by the external microprocessor. This section explains all aspects of interrupts as they apply to the NCR 53C810.

Polling vs. Hardware Interrupts

The external microprocessor can be informed of an interrupt condition by polling or hardware interrupts. Polling means that the microprocessor must continually loop and read a register until it detects a bit set that indicates an interrupt. This method is the fastest, but it wastes CPU time that could be used by other system tasks. The preferred method of detecting interrupts in most systems is hardware interrupts. In this case, the NCR 53C810 will assert the Interrupt Request (IRQ/) line that will interrupt the microprocessor, causing the microprocessor to execute an interrupt service routine. A hybrid approach would use hardware interrupts for long waits, and use polling for short waits.

Registers

The registers in the NCR 53C810 that are used for detecting or defining interrupts are the ISTAT, SIST0, SIST1, DSTAT, SIEN0, SIEN1, and DIEN.

The ISTAT is the only register that can be accessed as a slave during SCRIPTS operation, therefore it is the register that is polled when polled interrupts are used. It is also the first register that should be read when the IRQ/ pin has been asserted in association with a hardware interrupt. The INTF (Interrupt on the Fly) bit should be the first interrupt serviced. It must be written to one to be cleared. This interrupt must be cleared before servicing any other interrupts. If the SIP bit in the ISTAT register is set, then a SCSI-type interrupt has occurred and the SIST0 and SIST1 registers should be read. If the DIP bit in the ISTAT register is set, then a DMA-type interrupt has occurred and the DSTAT register should be read. SCSI-type and DMA-type interrupts may occur simultaneously, so in some cases both SIP and DIP may be set.

The SIST0 and SIST1 registers contain the SCSI-type interrupt bits. Reading these registers will determine which condition or conditions caused the SCSI-type interrupt, and will clear that SCSI interrupt condition. If the NCR 53C810 is receiving data from the SCSI bus and a fatal interrupt condition occurs, the NCR 53C810 will attempt to send the contents of the DMA FIFO to memory before generating the interrupt. If the NCR 53C810 is sending data to the SCSI bus and a fatal SCSI interrupt condition occurs, data could be left in the DMA FIFO. Because of this the DFE bit in DSTAT should be checked. If this bit is clear, set the CLF (Clear DMA FIFO) and CSF (Clear SCSI FIFO) bits before continuing. The CLF bit is bit 2 in CTEST3. The FLF bit is bit 3 in CTEST3. The CSF bit is bit 1 in STEST3.

The DSTAT register contains the DMA-type interrupt bits. Reading this register will determine which condition or conditions caused the DMA-type interrupt, and will clear that DMA interrupt condition. Bit 7 in DSTAT, DFE (DMA FIFO Empty), is purely a status bit; it will not generate an interrupt under any circumstances and will not be cleared when read. DMA interrupts will flush neither the DMA nor SCSI FIFOs before generating the interrupt, so the DFE bit in the DSTAT register should be checked after any DMA interrupt. If the DFE bit is clear, then the FIFOs must be cleared by setting the CLF (Clear DMA FIFO) and CSF (Clear SCSI FIFO) bits, or flushed by setting the FLF (Flush DMA FIFO) bit.

The SIEN0 and SIEN1 registers are the interrupt enable registers for the SCSI interrupts in SIST0 and SIST1.

The DIEN register is the interrupt enable register for DMA interrupts in DSTAT.

Fatal vs. Non-Fatal Interrupts

A fatal interrupt, as the name implies, always causes SCRIPTS to stop running. A non-fatal interrupt will cause SCRIPTS to stop running only if it is not masked. Masking will be discussed later in this section. All DMA interrupts (indicated by the DIP bit in ISTAT and one or more bits in DSTAT being set) are fatal.

Some SCSI interrupts (indicated by the SIP bit in the ISTAT and one or more bits in SIST0 or SIST1 being set) are non-fatal. When the NCR 53C810 is operating in Initiator mode, only the CMP (Function Complete), SEL (Selected), RSL (Reselected), GEN (General Purpose Timer Expired), and HTH (Handshake to Handshake Timer Expired) interrupts are non-fatal. When operating in Target mode CMP, SEL, RSL, GEN, and HTH, and M/A (Target mode: SATN/ active) are non-fatal. Refer to the description for the DHP (Disable Halt on a Parity Error or SATN/ active (Target Mode Only)) bit in the SCNTL1 register to configure the chip's behavior when the SATN/ interrupt is enabled during Target mode operation. The Interrupt on the Fly interrupt is also non-fatal, since SCRIPTS can continue when it occurs.

The reason for non-fatal interrupts is to prevent SCRIPTS from stopping when an interrupt occurs that does not require service from the CPU. This prevents an interrupt when arbitration is complete (CMP set), when the NCR 53C810 has been selected or reselected (SEL or RSL set), when the initiator has asserted ATN (target mode: SATN/ active) or when the General Purpose or Handshake to Handshake timers expire. These interrupts are not needed for events that occur during high-level SCRIPTS operation.

Masking

Masking an interrupt means disabling or ignoring that interrupt. Interrupts can be masked by clearing bits in the SIEN0 and SIEN1 (for SCSI interrupts) register or DIEN (for DMA interrupts) register. How the chip will respond to masked interrupts depends on: whether polling or hardware interrupts are being used; whether the interrupt is fatal or non-fatal; and whether the chip is operating in Initiator or Target mode.

If a non-fatal interrupt is masked and that condition occurs, SCRIPTS **will not** stop, the appropriate bit in the SIST0 or SIST1 **will** still be set, the SIP bit in the ISTAT **will not** be set, and the IRQ/ pin **will not** be asserted. See the section on non-fatal vs. fatal interrupts for a list of the non-fatal interrupts.

If a fatal interrupt is masked and that condition occurs, then SCRIPTS **will** stop, the appropriate bit in the DSTAT, SIST0, or SIST1 register **will** be set, the SIP or DIP bits in the ISTAT **will** be set, and the IRQ/ pin **will not** be asserted.

When the chip is initialized, enable **all** fatal interrupts if you are using hardware interrupts. If a fatal interrupt is disabled and that interrupt condition occurs, SCRIPTS will halt and the system will never know it unless it times out and checks the ISTAT after a certain period of inactivity.

If you are polling the ISTAT instead of using hardware interrupts, then masking a fatal interrupt will make no difference since the SIP and DIP bits in the ISTAT inform the system of interrupts, not the IRQ/ pin.

Masking an interrupt after IRQ/ is asserted will not cause IRQ/ to be deasserted.

Stacked Interrupts

The NCR 53C810 has the ability to stack interrupts if they occur one after the other. If the SIP or DIP bits in the ISTAT register are set (first level), then there is already at least one pending interrupt and any future interrupts will be stacked in extra registers behind the SIST0, SIST1, and DSTAT registers (second level). When two interrupts have occurred and the two levels of the stack are full, any further interrupts will set additional bits in the extra registers behind SIST0, SIST1, and DSTAT. When the first level of interrupts are cleared, all the interrupts that came in afterward will move into the SIST0, SIST1, and DSTAT. After the first interrupt is cleared by reading the appropriate register, the IRQ/ pin will be deasserted for a minimum of three CLKs; the stacked interrupt(s) will move into the SIST0, SIST1, or DSTAT; and the IRQ/ pin will be asserted once again.

Since a masked non-fatal interrupt will not set the SIP or DIP bits, interrupt stacking will not occur as a result of a masked, non-fatal interrupt. A masked, non-fatal interrupt will still post the interrupt in SIST0, but will not assert the IRQ/ pin. Since no interrupt is generated, future interrupts will move right into the SIST0 or SIST1 instead of being stacked behind another interrupt. When another condition occurs that generates an interrupt, the bit corresponding to the earlier masked non-fatal interrupt will still be set.

A related situation to interrupt stacking is when two interrupts occur simultaneously. Since stacking does not occur until the SIP or DIP bits are set, there is a small timing window in which multiple interrupts can occur but will not be stacked. These could be multiple SCSI interrupts (SIP set), multiple DMA interrupts (DIP set), or multiple SCSI and multiple DMA interrupts (both SIP and DIP set).

As previously mentioned, DMA interrupts will not attempt to flush the FIFOs before generating the interrupt. It is important to set either the CLF (Clear DMA FIFO) and CSF (Clear SCSI FIFO) bits if a DMA interrupt occurs and the DFE (DMA FIFO Empty) bit is not set. This is because any future SCSI interrupts will not be posted until the DMA FIFO is clear of data. These 'locked out' SCSI interrupts will be posted as soon as the DMA FIFO is empty.

Halting in an Orderly Fashion

When an interrupt occurs, the NCR 53C810 will attempt to halt in an orderly fashion.

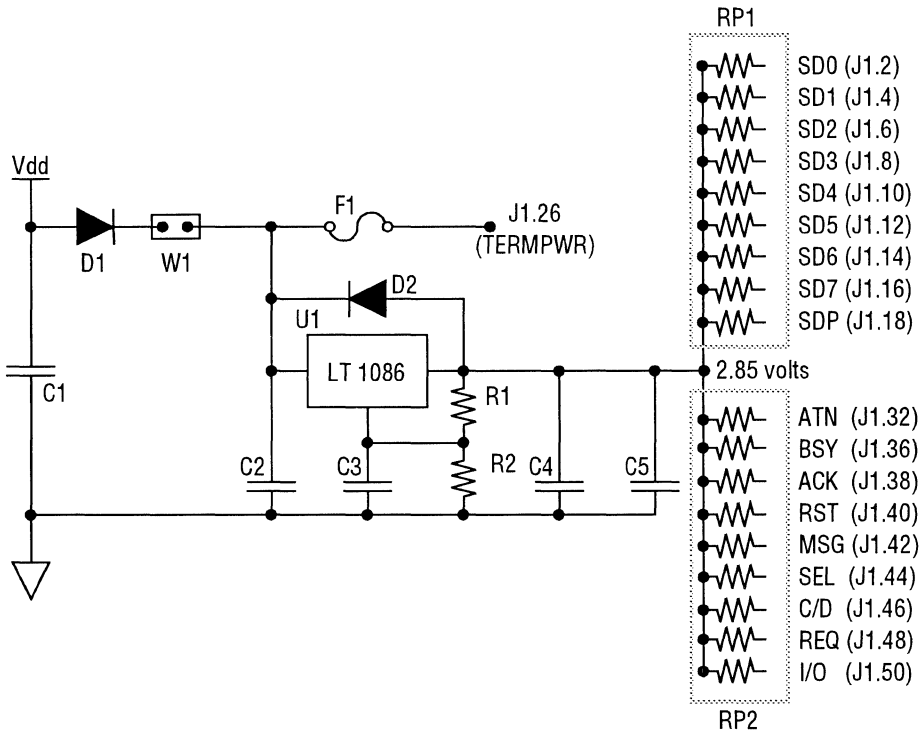
- If in the middle of an instruction fetch, the fetch will be completed, except in the case of a Bus Fault. Execution will not begin, but the DSP will point to the next instruction since it is updated when the current Script is fetched.
- If the DMA direction is a write to memory and a SCSI interrupt occurs, the 53C810 will attempt to flush the DMA FIFO to memory before halting. Under any other circumstances only the current cycle will be completed before halting, so the DFE bit in DSTAT should be checked to see if any data remains in the DMA FIFO.
- SREQ/SACK handshakes that have begun will be completed before halting.
- The 53C810 will attempt to clean up any outstanding synchronous offset before halting.
- In the case of Transfer Control Instructions, once instruction execution begins it will continue to completion before halting.
- If the instruction is a JUMP/CALL WHEN/IF <phase>, the DSP will be updated to the transfer address before halting.
- All other instructions may halt before completion.

Sample Interrupt Service Routine

The following is a sample of an interrupt service routine for the NCR 53C810. It can be repeated if polling is used, or should be called when the IRQ/ pin is asserted if hardware interrupts are used.

1. Read ISTAT.
2. If the INTF bit is set, it must be written to a one to clear this status.
3. If only the SIP bit is set, read SIST0 and SIST1 to clear the SCSI interrupt condition and get the SCSI interrupt status. The bits in the SIST0 and SIST1 tell which SCSI interrupt(s) occurred and determine what action is required to service the interrupt(s).
4. If only the DIP bit is set, read the DSTAT to clear the interrupt condition and get the DMA interrupt status. The bits in the DSTAT will tell which DMA interrupt(s) occurred and determine what action is required to service the interrupt(s).
5. If both the SIP and DIP bits are set, read SIST0, SIST1, and DSTAT to clear the SCSI and DMA interrupt condition and get the interrupt status. If using 8-bit reads of the SIST0, SIST1, and DSTAT registers to clear interrupts, insert a 12 CLK delay between the consecutive reads to ensure that the interrupts clear properly. Both the SCSI and DMA interrupt conditions should be handled before leaving the ISR. It is recommended that the DMA interrupt be serviced before the SCSI interrupt because a serious DMA interrupt condition could influence how the SCSI interrupt is acted upon.
6. When using polled interrupts, go back to step 1 before leaving the interrupt service routine, in case any stacked interrupts moved in when the first interrupt was cleared. When using hardware interrupts, the IRQ/ pin will be asserted again if there are any stacked interrupts. This should cause the system to re-enter the interrupt service routine.

Figure 2-4. NCR 53C810 Alternative Two Termination



Key:

C1	4.7 µF tantalum, SMT
C2, C3	1.0 µF tantalum, SMT
C4	22 µF tantalum, SMT
C5	0.1 µF ceramic, SMT
D1-D2	Schottky diode, 1N5817
F1	1.5 Amp fuse, socketed, 2AG
J1	50-pin dual row header, male SCSI connector
RP1-RP2	110 x 9 (1%) pullups, 1% SIP-10
U1	Voltage Regulator, LT 1086, TO-39
W1	2-position header
R1	121 Ω, 1%
R2	154 Ω, 1%

Chapter Three
PCI Functional Description

PCI Addressing

There are three types of PCI-defined address space:

- Configuration space
- Memory space
- I/O space

Configuration space is a contiguous 256 8-bit set of addresses dedicated to each "slot" or "stub" on the bus. A decode of C_BE/(3-0) determines if this PCI cycle is intended to access configuration register space. The IDSEL bus signal is a "chip select" that allows access to the configuration register space only. A configuration read/write cycle without IDSEL will be ignored. The eight lower order addresses are used to select a specific 8-bit register. The host uses this configuration space to initialize the NCR 53C810.

The lower 128 bytes of the NCR 53C810 256-byte configuration space holds system parameters while the upper 128 bytes map into the NCR 53C810 operating registers. For all PCI cycles except configuration cycles, the NCR 53C810 registers are located on the 256-byte block boundary defined by the base address assigned through the configured register. The NCR 53C810 operating registers will be available in both the upper and lower 128-byte portions of the 256-byte space selected.

Table 3-1. PCI Bus Commands and Encoding Types

CBE/(3-0)	Command Type	Supported as Master	Supported as Slave
0000	Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read Cycle	Yes	Yes
0011	I/O Write Cycle	Yes	Yes
0100	Reserved	n/a	
0101	Reserved	n/a	
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	n/a	
1001	Reserved	n/a	
1010	Configuration Read	No	Yes
1011	Configuration Write	No	Yes
1100	Memory Read Multiple	No	No (defaults to 0110)
1101	Dual Address Cycle	No	No
1110	Memory Read Line	Yes*	No (defaults to 0110)
1111	Memory Write and Invalidate	No	No (defaults to 0111)

* *This operation is selectable by bit 3 in the DMODE register*

At initialization time, each PCI device is assigned a base address (in the case of the NCR 53C810, the upper 24 bits of the address are selected) for memory accesses and I/O accesses. On every access, the NCR 53C810 compares its assigned base adresses with the value on the Address/Data bus during the PCI address phase. If there is a match of the upper 24 bits, the access is for the NCR 53C810 and the low order eight bits define the register to be accessed. A decode of the C_BE/ (3-0) determines which registers and what type of access is to be performed.

PCI defines memory space as a contiguous 32-bit memory address that is shared by all system resources, including the NCR 53C810. Base Address Register one determines which 256-byte memory area this device will occupy.

PCI defines I/O space as a contiguous 32-bit I/O address that is shared by all system resources, including the NCR 53C810. Base Address Register zero determines which 256-byte I/O area this device will occupy.

PCI Bus Commands and Functions Supported

Bus commands indicate to the target the type of transaction the master is requesting. Bus commands are encoded on the C_BE/(3-0) lines during the address phase. PCI bus command encoding and types appear in Table 3-1.

The I/O Read command is used to read data from an agent mapped in I/O address space. All 32 address bits are decoded.

The I/O Write command is used to write data to an agent when mapped in I/O address space. All 32 address bits are decoded.

The Memory Read and Memory Read Line commands are used to read data from an agent mapped in memory address space. All 32 address bits are decoded.

The Memory Write command is used to write data to an agent when mapped in memory address space. All 32 address bits are decoded.

The NCR 53C810 responds to Memory Read Multiple, Memory Read Line, and Memory Write and Invalidate commands by treating them similar to standard Memory Read and Memory Write commands. The NCR 53C810 will not respond to reserved commands, special cycle, or interrupt acknowledge commands.

Configuration Registers

The Configuration registers are accessible only by system BIOS during PCI configuration cycles, and are not available to the user at any time. No other cycles, including SCRIPTS operations, can access these registers.

The lower 128 bytes hold configuration data while the upper 128 bytes hold the NCR 53C810 operating registers, which are described in Chapter Five, "Operating Registers." These registers can be accessed by SCRIPTS or the host processor.

Note: The configuration register descriptions are provided for general information only, to indicate which PCI configuration addresses are supported in the NCR 53C810. For detailed information, refer to the *PCI Specification.*

Table 3-2 shows the PCI configuration registers implemented by the NCR 53C810. Note that addresses 40h through 7Fh are not defined.

All PCI-compliant devices, such as the NCR 53C810, must support the Vendor ID, Device ID, Command, and Status Registers. Support of other PCI-compliant registers is optional. In the NCR 53C810, registers that are not supported are not writable and will return all zeroes when read. Only those registers and bits that are currently supported by the NCR 53C810 are described in this chapter. For more detailed information on PCI registers, please see the *PCI Specification.*

Table 3-2. PCI Configuration Registers Implemented in the NCR 53C810

31 16	15 0	Config
Device ID = 0001h	Vendor ID = 1000h	00h
Status	Command	04h
Class Code = 000000	Rev ID = 01h	08h
Not Supported / Header Type	Latency Timer / Not Supported	0Ch
Base Address Zero (I/O)*		10h
Base Address One (Mem)**		14h
Not Supported		18h
Not Supported		1Ch
Not Supported		20h
Not Supported		24h
Reserved		28h
Reserved		2Ch
Not Supported		30h
Reserved		34h
Reserved		38h
Max_Lat / Min_Gnt	Interrupt Pin / Interrupt Line	3Ch

*I/O Base is supported
**Memory Base is supported

Note: Addresses 40h to 7Fh are not defined. All unsupported registers are not writable and will return all zeroes when read. Reserved registers will also return all zeroes when read.

Vendor ID Register (00h)
Read Only

This field identifies the manufacturer of the device. NCR Microelectronic Products Vendor ID is 1000h.

Device ID (02h)
Read Only

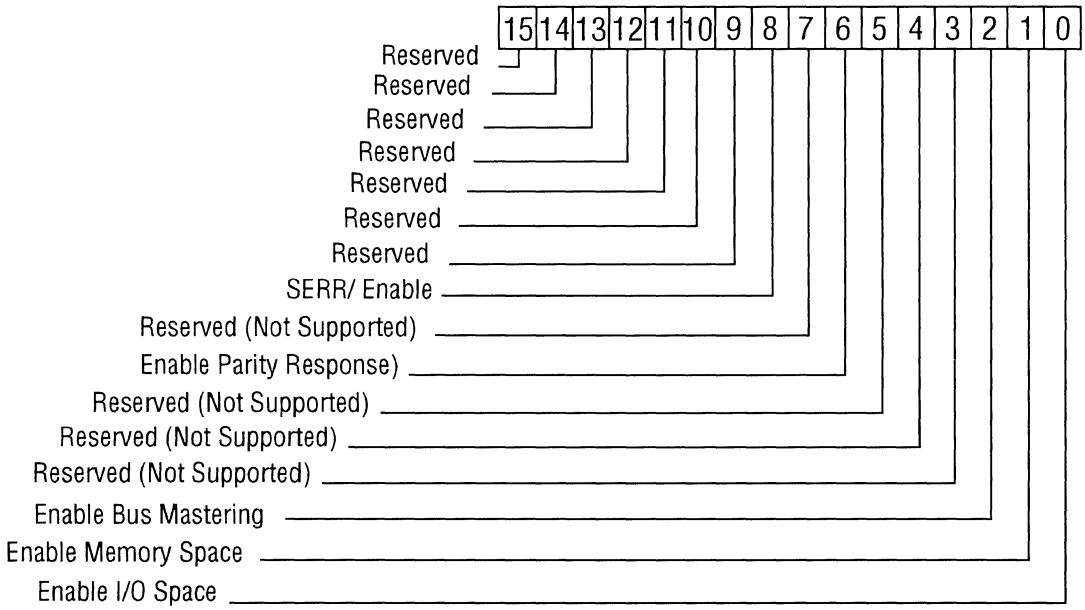
This field identifies the particular device. The NCR 53C810 Device ID is 0001h.

Command Register (04h)
Read/Write

The Command Register, illustrated in Figure 3-1, provides coarse control over a device's ability to generate and respond to PCI cycles. When a zero is written to this register, the NCR 53C810 is logically disconnected from the PCI bus for all accesses except configuration accesses.

In the NCR 53C810, bits 3 through 5 and bits 7 through 8 are not implemented. Bits 9 through 15 are reserved. The NCR 53C810 does implement I/O space and thus implements a writable element at bit location (0) of the Command Register.

Figure 3-1. Command Register Layout



Bits 15-9 Reserved

Bit 8 SERR/ Enable
This bit enables the SERR/ driver. SERR/ is disabled when this bit is clear. The default value of this bit is zero. This bit and bit 6 must be set to report address parity errors.

Bit 7 Reserved

Bit 6 Enable Parity Error Response
This bit allows the NCR 53C810 to detect parity errors on the PCI bus and report these errors to the system. Only data parity checking is enabled. The NCR 53C810 always generates parity for the PCI bus.

Bits 5-3 Reserved

Bit 2 Enable Bus Mastering
This bit controls the NCR 53C810's ability to act as a master on the PCI bus. A value of zero disables the device from generating PCI bus master accesses. A value of one allows the NCR 53C810 to behave as a bus master. The NCR 53C810 must be a bus master in order to fetch SCRIPTS instructions and transfer data.

Bit 1 Enable Memory Space
This bit controls the NCR 53C810's response to Memory Space accesses. A value of zero disables the device response. A value of one allows the NCR 53C810 to respond to Memory Space accesses at the address specified by Base Address 1.

Bit 0 Enable I/O Space
This bit controls the NCR 53C810's response to I/O space accesses. A value of zero disables the response. A value of one allows the NCR 53C810 to respond to I/O space accesses at the address specified in Base Address 0.

Status Register (06h) Read/Write

The Status Register, illustrated in Figure 3-2, is used to record status information for PCI bus-related events.

In the NCR 53C810, bits 0 through 8 are reserved and bits 11 and 14 are not implemented by the NCR 53C810.

Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a one. For instance, to clear bit 15 and not affect any other bits, write the value 8000h to the register.

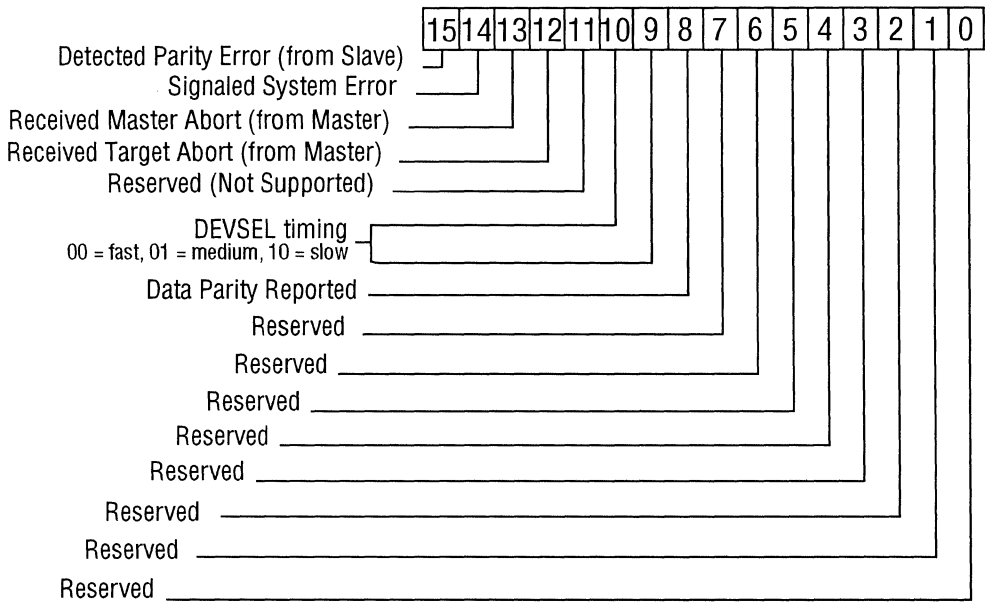
Bit 15 Detected Parity Error (from Slave)
This bit will be set by the device whenever the device detects a data parity error. This bit is disabled when parity error handling is disabled. Devices with a Revision ID register value of 00h do not check or report parity errors if bit 6 is set to 0.

Bit 14 Signaled System Error
This bit should be set whenever a device asserts the SERR/ signal.

Bit 13 Master Abort (from Master)
This bit should be set by a master device whenever its transaction (except for Special Cyle) is terminated with master-abort. All master devices should implement this bit.

Bit 12 Received Target Abort (from Master)
This bit should be set by a master device whenever its transaction is terminated with target-abort. All master devices should implement this bit.

Figure 3-2. Status Register Layout



Bit 11 Reserved

Bits 10-9 DEVSEL/ Timing

These bits encode the timing of DEVSEL/. These are encoded as 00b for fast, 01b for medium, 10b for slow with 11b reserved. These bits are read-only and should indicate the slowest time that a device asserts DEVSEL/ for any bus command except Configuration Read and Configuration Write. In the NCR 53C810, 01b is supported.

Bit 8 Data Parity Reported

This bit is set when the following three conditions are met: 1) The bus agent asserted PERR/ itself or observed PERR/ asserted; 2) The agent setting this bit acted as the bus master for the operation in which the error occurred; 3) The Parity Error Response bit in the Command register is set.

Bits 7-0 Reserved

Revision ID Register (08h)
Read Only

This register specifies a device specific revision identifier. This manual applies to devices that have this register set to 01h.

Class Code Register (09h)
Read Only

This register is used to identify the generic function of the device. The upper byte of this register is a base class code, the middle byte is a subclass code, and the lower byte identifies a specific register-level programming interface. The value of this register is 000000h

Latency Timer Register (0Dh)
Read/Write

The Latency Timer Register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. The NCR 53C810 supports this timer. All eight bits are writable, allowing latency values of 0-255 PCI clocks. Use the following equation to calculate an optimum latency value for the NCR 53C810:

Latency = 2 + (Burst Size * (typical wait states +1))

Values greater than the optimum are also acceptable.

Header Type Register (0Eh)
Read Only

This register identifies the layout of bytes 10h through 3Fh in configuration space and also whether or not the device contains multiple functions. The value of this register is 00h.

Base Address 0 (I/O) (10h)
Read/Write

This 32-bit register has bit zero hardwired to one. Bit 1 is reserved and must return a zero on all reads, and the other bits are used to map the device into I/O space.

Base Address 1 (Memory) (14h)
Read/Write

This register has bit 0 hardwired to zero. For detailed information on the operation of this register, refer to the *PCI Specification.*

Interrupt Line Register (3Ch)
Read/Write

This register is used to communicate interrupt line routing information. POST software will write the routing information into this register as it initiates and configures the system. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin has been connected to. Values in this register are specified by system architecture.

Interrupt Pin Register (3Dh)
Read Only

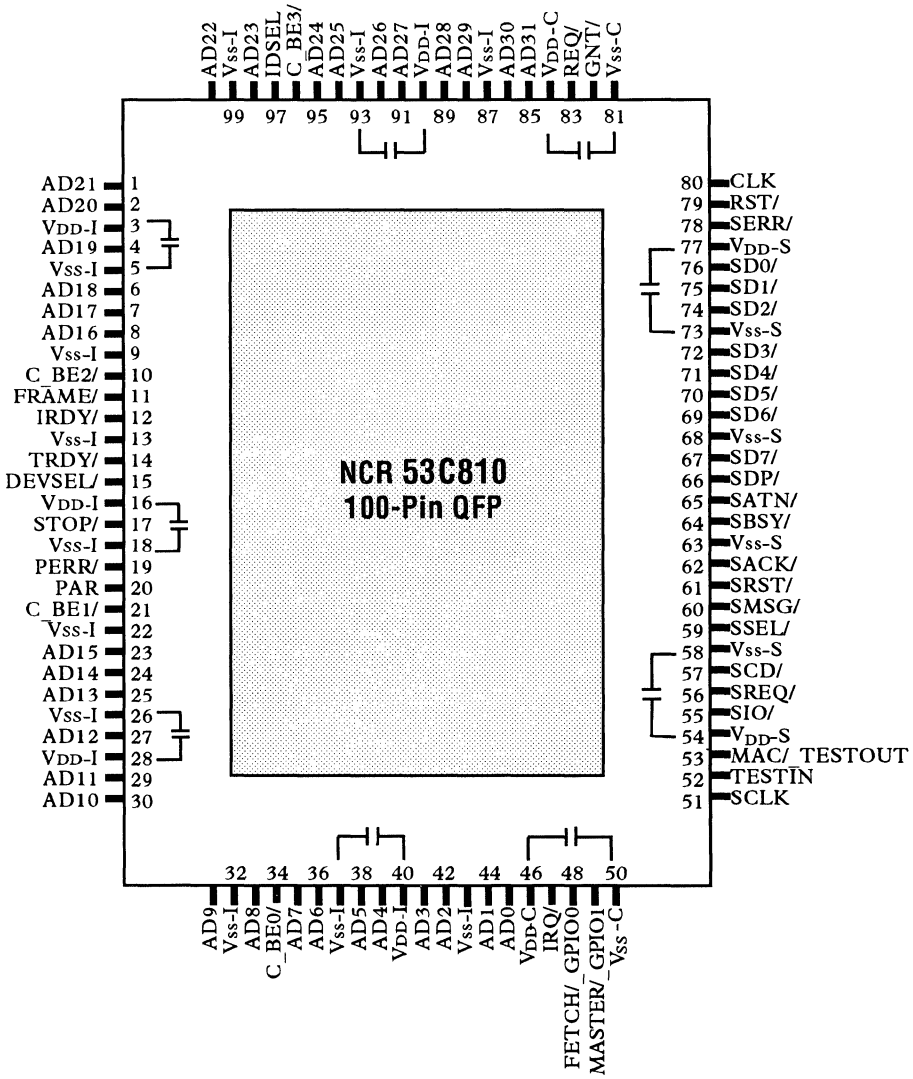
This register tells which interrupt pin the device uses. Its value is set to 01h, for the INTA/ signal.

Min_Gnt Register (3Eh)
Max_Lat Register (3Fh)
Read Only

These registers are used to specify the desired settings for Latency Timer values. Min_GNT is used to specify how long a burst period the device needs. Max_Latency is used to specify how often the device needs to gain access to the PCI bus. The value specified in these registers is in units of 0.25 microseconds. Values of zero indicate that the device has no major requirements for the settings of Latency Timers.

Chapter Four
Signal Descriptions

Figure 4-1. NCR 53C810 Pin Diagram



Note: The decoupling capacitor arrangement shown above is recommended to maximize the benefits of the internal split ground system. Capacitor values between 0.01 and 0.1µF should provide adequate noise isolation. Because of the number of high current drivers on the NCR 53C810, a multi-layer PC board with power and ground planes is required.

The PCI/SCSI pin definitions are organized into the following functional groups: system, address/data, interface control, arbitration, error reporting, SCSI, and optional interface. A slash (/) at the end of the signal name indicates that the active state occurs when the signal is at a low voltage. When absent, the signal is active at a high voltage.

There are four signal type definitions:

I Input, a standard input-only signal

O Totem Pole Output, a standard output driver

T/S Tri-state, a bi-directional, tri-state input/output pin

S/T/S Sustained Tri-state, an active low tri-state signal owned and driven by one and only one agent at a time.

Power and Ground Pins

Symbol	Pin No	Description
V_{SS}-I	5, 9, 13, 18, 22, 26 32, 37, 43, 87, 93, 99	Power supplies to the PCI I/O pins
V_{DD}-I	3, 16, 28, 40, 90	Power supplies to the PCI I/O pins
V_{SS} -S	58, 63, 68, 73	Power supplies to the SCSI bus I/O pins
V_{DD}-S	54, 77	Power supplies to the SCSI bus I/O pins
V_{SS}-C	50, 81	Power supplies to the internal logic core
V_{DD}-C	46, 84	Power supplies to the internal logic core

System Pins

Symbol	Pin No.	Type	Description
CLK	80	I	Clock provides timing for all transactions on the PCI bus and is an input to every PCI device. All other PCI signals are sampled on the rising edge of CLK, and other timing parameters are defined with respect to this edge. This clock can be optionally used as the SCSI core clock; however, fast SCSI transfer rates may not be achieved.
RST/	79	I	Reset forces the PCI sequencer of each device to a known state. All t/s and s/t/s signals are forced to a high impedance state, and all internal logic is reset. The RST/ input is synchronized internally to the rising edge of CLK. The CLK input must be active while RST/ is active to properly reset the device.

Address and Data Pins

Symbol	Pin No.	Type	Description
AD(31-0)	85, 86, 88, 89, 91, 92, 94,95, 98, 100, 1, 2, 4, 6, 7,8, 23, 24, 25, 27, 29, 30, 31, 33, 35, 36, 38, 39, 41, 42, 44, 45	T/S	Physical longword address and data are multiplexed on the same PCI pins. During the first clock of a transaction AD (31-0) contain a physical byte address. During subsequent clocks, AD(31-0) contain data. A bus transaction consists of an address phase, followed by one or more data phases. PCI supports both read and write bursts. Little Endian byte ordering is used. AD(7-0) define the least significant byte, and AD(31-24) the most significant byte.
C_BE/(3-0)	96, 10, 21, 34	T/S	Bus command and byte enables are multiplexed on the same PCI pins. During the address phase of a transaction, C_BE/(3-0) define the bus command. During the data phase, C_BE/(3-0) are used as byte enables. The byte enables determine which byte lanes carry meaningful data. C_BE/(0) applies to byte 0, and C_BE/(3) to byte 3.
PAR	20	T/S	Parity is the even parity bit that protects the AD(31-0) and C_BE/(3-0) lines. During address phase, both the address and command bits are covered. During data phase, both data and byte enables are covered.

Interface Control Pins

Symbol	Pin No.	Type	Description
FRAME/	11	S/T/S	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME/ is asserted to indicate a bus transaction is beginning. While FRAME/ is asserted, data transfers continue. When FRAME/ is deasserted, the transaction is in the final data phase or while the bus is idle.
TRDY/	14	S/T/S	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY/ is used with IRDY/. A data phase is completed on any clock when both TRDY/ and IRDY/ are sampled asserted. During a read, TRDY/ indicates that valid data is present on AD(31-0). During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY/ and TRDY/ are asserted together.
IRDY/	12	S/T/S	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. This signal is used with TRDY/. A data phase is completed on any clock when both IRDY/ and TRDY/ are sampled asserted. During a write, IRDY/ indicates that valid data is present on AD(31-0). During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY/ and TRDY/ are asserted together.
STOP/	17	S/T/S	Stop indicates the selected target is requesting the master to stop the current transaction.
DEVSEL/	15	S/T/S	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, it indicates to a master whether any device on the bus has been selected.
IDSEL	97	I	Initialization Device Select is used as a chip select in lieu of the upper 24 address lines during configuration read and write transactions.

Arbitration Pins

Symbol	Pin No.	Type	Description
REQ/	83	O	Request indicates to the arbiter that this agent desires use of the PCI bus. This is a point-to point signal. Every master has its own REQ/.
GNT/	82	I	Grant indicates to the agent that access to the PCI bus has been granted. This is a point-to-point signal. Every master has its own GNT/.

Error Reporting Pins

Symbol	Pin No.	Type	Description
PERR/	19	S/T/S	Error may be pulsed active by an agent that detects a parity error. PERR/ can be used by any agent to signal data corruptions. However, on detection of an PERR/ pulse, the central resource may generate a nonmaskable interrupt to the host CPU, which often implies the system will be unable to continue operation once error processing is complete.
SERR/	78	O	This open drain output pin is used to report address parity errors.

SCSI Signals

Symbol	Pin No.	Type	Description
SCLK	51	I	SCLK is used to derive all SCSI-related timings. The speed of this clock is determined by the application's requirements; in some applications SCLK may be sourced internally from the PCI bus clock (CLK). If SCLK is internally sourced, then the SCLK pin should be tied low.
SD/ (7-0) SDP	67, 69,70, 71, 72, 74 75, 76, 66	I/O	SCSI Data includes the following data lines and parity signals: SD7-0 (8-bit SCSI data bus), SDP(SCSI data parity bit).
SCTRL/	55, 56, 57 59, 60, 61 62, 64, 65	I/O	SCSI Control includes the following signals: SC_D/ SCSI phase line, command/data SI_O/ SCSI phase line, input/output SMSG/ SCSI phase line, message SREQ/ Data handshake signal from target device SACK/ Data handshake signal from initiator device SBSY/ SCSI bus arbitration signal, busy SATN/ Attention, the initiator is requesting a message-out phase SRST/ SCSI bus reset SSEL/ SCSI bus arbitration signal, select device

Additional Interface Pins

Symbol	Pin No.	Type	Description
TESTIN/	52	I	Test In. When this pin is driven low, the NCR 53C810 connects all inputs and outputs to an "AND tree." The SCSI control signals and data lines are not connected to the "AND tree." The output of the "AND tree" is connected to the Test Out pin. This allows manufacturers to verify chip connectivity to the board and to determine exactly which pins are not properly attached. When the TESTIN pin is driven low, internal pullups are enabled on all input, output, and bidirectional pins, all outputs and bidirectional signals will be tri-stated, and the MAC/_TESTOUT pin will be enabled. Connectivity can be tested by driving one of the NCR 53C810 pins low. The MAC/_TESTOUT pin should respond by driving low, respectively.
GPIO1_0 FETCH/	48	I/O	General Purpose I/O pin. Optionally, when driven low indicates that the next bus request will be for an Op Code fetch.
GPIO0_1 MASTER/	51	I/O	General purpose I/O pin. Optionally, when driven low indicates that the NCR 53C810 is bus master.
MAC/_ TESTOUT	53	T/S	Memory Access Control. This pin can be programmed to indicate local or system memory accesses (non-PCI applications). It is also used to test the connectivity of the NCR 53C810 signals using an "AND tree" scheme. The MAC/_TESTOUT pin is only driven as the Test Out function when the TESTIN/ pin is driven low.
IRQ/	47	0	Interrupt. This signal, when asserted low, indicates that an interrupting condition has occurred and that service is required from the host CPU. The output drive of this pin is programmed as either open drain with an internal weak pullup or optionally as a totem pole driver. Refer to the description of DCNTL Register, Bit 3, for additional information.

Chapter Five
Operating Registers

This section contains descriptions of all NCR 53C810 operating registers. Table 5-1 summarizes the NCR 53C810 operating register set. Figure 5-1, the register map, lists registers by operating and configuration addresses. The terms "set" and "assert" are used to refer to bits that are programmed to a binary one. Similarly, the terms "deassert," "clear" and "reset" are used to refer to bits that are programmed to a binary zero. Any bits marked as reserved should always be written to zero; mask all information read from them. Reserved bit functions may be changed at any time. Unless otherwise indicated, all bits in registers are active high, that is, the feature is enabled by setting the bit. The bottom line of every register diagram shows the default register values, which are enabled after the chip is powered on or reset.

The only register that the host CPU can access while the NCR 53C810 is executing SCRIPTS is the ISTAT register; attempts to access other registers will interfere with the operation of the chip. However, all operating registers are accessible via SCRIPTS. All read data is synchronized and stable when presented to the PCI bus.

Table 5-1. Operating Register Addresses and Descriptions

Memory or I/O	Config Mem/I/O	Read/ Write	Label	Description
00	80	R/W	SCNTL0	SCSI Control 0
01	81	R/W	SCNTL1	SCSI Control 1
02	82	R/W	SCNTL2	SCSI Control 2
03	83	R/W	SCNTL3	SCSI Control 3
04	84	R/W	SCID	SCSI Chip ID
05	85	R/W	SXFER	SCSI Transfer
06	86	R/W	SDID	SCSI Destination ID
07	87	R/W	GPREG	General Purpose Bits
08	88	R/W	SFBR	SCSI First Byte Received
09	89	R/W	SOCL	SCSI Output Control Latch
0A	8A	R	SSID	SCSI Selector ID
0B	8B	R/W	SBCL	SCSI Bus Control Lines
0C	8C	R	DSTAT	DMA Status
0D	8D	R	SSTAT0	SCSI Status 0
0E	8E	R	SSTAT1	SCSI Status 1
0F	8F	R	SSTAT2	SCSI Status 2
10-13	90-93	R/W	DSA	Data Structure Address
14	94	R/W	ISTAT	Interrupt Status
18	98	R/W	CTEST0	Chip Test 0
19	99	R	CTEST1	Chip Test 1
1A	9A	R	CTEST2	Chip Test 2
1B	9B	R	CTEST3	Chip Test 3
1C-1F	9C-9F	R/W	TEMP	Temporary Stack

Table 5-1. Operating Register Addresses and Descriptions (Continued)

Memory or I/O	Config Mem/I/O	Read/ Write	Label	Description
20	A0	R/W	DFIFO	DMA FIFO
21	A1	R/W	CTEST4	Chip Test 4
22	A2	R/W	CTEST5	Chip Test 5
23	A3	R/W	CTEST6	Chip Test 6
24-26	A4-A6	R/W	DBC	DMA Byte Counter
27	A7	R/W	DCMD	DMA Command
28-2B	A8-AB	R/W	DNAD	DMA Next Address for Data
2C-2F	AC-AF	R/W	DSP	DMA SCRIPTS Pointer
30-33	B0-B3	R/W	DSPS	DMA SCRIPTS Pointer Save
34-37	B4-B7	R/W	SCRATCH A	General Purpose Scratch Pad A
38	B8	R/W	DMODE	DMA Mode
39	B9	R/W	DIEN	DMA Interrupt Enable
3A	BA	R/W	DWT	DMA Watchdog Timer
3B	BB	R/W	DCNTL	DMA Control
3C-3F	BC-BF	R	ADDER	Sum output of internal adder
40	C0	R/W	SIEN0	SCSI Interrupt Enable 0
41	C1	R/W	SIEN1	SCSI Interrupt Enable 1
42	C2	R	SIST0	SCSI Interrupt Status 0
43	C3	R	SIST1	SCSI Interrupt Status 1
44	C4	R/W	SLPAR	SCSI Longitudinal Parity
45	C5		Reserved	
46	C6	R/W	MACNTL	Memory Access Control
47	C7	R/W	GPCNTL	General Purpose Control
48	C8	R/W	STIME0	SCSI Timer 0
49	C9	R/W	STIME1	SCSI Timer 1
4A	CA	R/W	RESPID	Response ID
4B	C7		Reserved	
4C	CC	R	STEST0	SCSI Test 0
4D	CD	R	STEST1	SCSI Test 1
4E	CE	R/W	STEST2	SCSI Test 2
4F	CF	R/W	STEST3	SCSI Test 3
50	D0	R	SIDL	SCSI Input Data Latch
51-53	D1-D3		Reserved	
54	D4	R/W	SODL	SCSI Output Data Latch
55-57	D5-D7		Reserved	
58	D8	R	SBDL	SCSI Bus Data Lines
59-5B	D9-DB		Reserved	
5C-5F	DC-DF	R/W	SCRATCH B	General Purpose Scratch Pad B

Figure 5-1. Register Address Map

				Mem I/O	Config Mem I/O
SCNTL3	SCNTL2	SCNTL1	SCNTL0	00	80
GPREG	SDID	SXFER	SCID	04	84
SBCL	SSID	SOCL	SFBR	08	88
SSTAT2	SSTAT1	SSTAT0	DSTAT	0C	8C
DSA				10	90
RESERVED			ISTAT	14	94
CTEST3	CTEST2	CTEST1	CTEST0	18	98
TEMP				1C	9C
CTEST6	CTEST5	CTEST4	DFIFO	20	A0
DCMD	DBC			24	A4
DNAD				28	A8
DSP				2C	AC
DSPS				30	B0
SCRATCH A				34	B4
DCNTL	DWT	DIEN	DMODE	38	B8
ADDER				3C	BC
SIST1	SIST0	SIEN1	SIEN0	40	C0
GPCNTL	MACNTL	RESERVED	SLPAR	44	C4
RESERVED	RESPID	STIME1	STIME0	48	C8
STEST3	STEST2	STEST1	STEST0	4C	CC
RESERVED			SIDL	50	D0
RESERVED			SODL	54	D4
RESERVED			SBDL	58	D8
SCRATCH B				5C	DC

Register 00 (80)
SCSI Control Zero (SCNTL0)
Read/Write

ARB1	ARB0	START	WATN	EPC	RES	AAP	TRG
7	6	5	4	3	2	1	0
Default>>>							
1	1	0	0	0	X	0	0

Bit 7 ARB1 (Arbitration mode bit 1)
Bit 6 ARB0 (Arbitration mode bit 0)

ARB1	ARB0	Arbitration Mode
0	0	Simple arbitration
0	1	Reserved
1	0	Reserved
1	1	Full arbitration, selection or reselection

Simple Arbitration

1) The NCR 53C810 waits for a bus free condition to occur.
2) It asserts SBSY/ and its SCSI ID (contained in the SCID register) onto the SCSI bus. If the SSEL/ signal is asserted by another SCSI device, the NCR 53C810 will deassert SBSY/, deassert its ID and set the Lost Arbitration bit (bit 3) in the SSTAT0 register.
3) After an arbitration delay, the CPU should read the SBDL register to check if a higher priority SCSI ID is present. If no higher priority ID bit is set, and the Lost Arbitration bit is not set, the NCR 53C810 has won arbitration.
4) Once the NCR 53C810 has won arbitration, SSEL/ must be asserted via the SOCL for a bus clear plus a bus settle delay (1.2 µs) before a low level selection can be performed.

Full Arbitration, Selection/Reselection

1) The NCR 53C810 waits for a bus free condition.
2) It asserts SBSY/ and its SCSI ID (the highest priority ID stored in the SCID register) onto the SCSI bus.
3) If the SSEL/ signal is asserted by another SCSI device or if the NCR 53C810 detects a higher priority ID, the NCR 53C810 will deassert BSY, deassert its ID, and wait until the next bus free state to try arbitration again.
4) The NCR 53C810 repeats arbitration until it wins control of the SCSI bus. When it has won, the Won Arbitration bit is set in the SSTAT0 register, bit 2.
5) The NCR 53C810 performs selection by asserting the following onto the SCSI bus: SSEL/, the target's ID (stored in the SDID register) and the NCR 53C810's ID (the highest priority ID stored in the SCID register).
6) After a selection is complete, the Function Complete bit is set in the SIST0 register, bit 6.
7) If a selection time-out occurs, the Selection Time-out bit is set in the SIST1 register, bit 2.

Bit 5 START (Start sequence)

When this bit is set, the NCR 53C810 will start the arbitration sequence indicated by the Arbitration Mode bits. The Start Sequence bit is accessed directly in low-level mode; during SCSI SCRIPTS operations, this bit is controlled by the SCRIPTS processor. An arbitration sequence should not be started if the connected (CON) bit in the SCNTL1 register, bit 4, indicates that the NCR 53C810 is already connected to the SCSI bus. This bit is automatically cleared when the arbitration sequence is complete. If a se-

quence is aborted, bit 4 in the SCNTL1 register should be checked to verify that the NCR 53C810 did not connect to the SCSI bus.

Bit 4 WATN (Select with SATN/ on a start sequence)
When this bit is set and the NCR 53C810 is in initiator mode, the SATN/ signal will be asserted during NCR 53C810 selection of a SCSI target device. This is to inform the target that the NCR 53C810 has a message to send. If a selection time-out occurs while attempting to select a target device, SATN/ will be deasserted at the same time SSEL/ is deasserted. When this bit is clear, the SATN/ signal will not be asserted during selection. When executing SCSI SCRIPTS, this bit is controlled by the SCRIPTS processor, but it may be set manually in low level mode.

Bit 3 EPC (Enable parity checking)
When this bit is set, the SCSI data bus is checked for odd parity when data is received from the SCSI bus in either initiator or target mode. If a parity error is detected, bit 0 of the SIST0 register is set and an interrupt may be generated.

If the NCR 53C810 is operating in initiator mode and a parity error is detected, SATN/ can optionally be asserted, but the transfer continues until the target changes phase. When this bit is cleared, parity errors are not reported.

Bit 2 Reserved

Bit 1 AAP (Assert SATN/ on parity error)
When this bit is set, the NCR 53C810 automatically asserts the SCSI ATN/ signal upon detection of a parity error. SATN/ is only asserted in initiator mode. The SATN/ signal is asserted before deasserting SACK/ during the byte transfer with the parity error. The Enable Parity Checking bit must also be set for the NCR 53C810 to assert SATN/ in this manner. The following parity errors can occur:

1) A parity error detected on data received from the SCSI bus.
2) A parity error detected on data transferred to the NCR 53C810 from the host data bus.

If the Assert SATN/ on Parity Error bit is cleared or the Enable Parity Checking bit is cleared, SATN/ will not be automatically asserted on the SCSI bus when a parity error is received.

Bit 0 TRG (Target mode)
This bit determines the default operating mode of the NCR 53C810. The user must manually set target or initiator mode. This can be done using the SCRIPTS language (SET TARGET or CLEAR TARGET). When this bit is set, the chip is a target device by default. When this bit is cleared, the NCR 53C810 is an initiator device by default.

CAUTION: Writing this register while not connected may cause the loss of a selection or reselection due to the changing of target or initiator modes.

Register 01 (81)
SCSI Control One (SCNTL1)
Read/Write

EXC	ADB	DHP	CON	RST	AESP	IARB	SST
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 EXC (Extra clock cycle of data setup)
When this bit is set, an extra clock period of data setup is added to each SCSI data transfer. The extra data setup time can provide additional system design margin, though it will affect the SCSI transfer rates. Clearing this bit disables the extra clock cycle of data setup time. Setting this bit will only affect SCSI send operations.

Bit 6 ADB (Assert SCSI data bus)
When this bit is set, the NCR 53C810 drives the contents of the SCSI Output Data Latch Register (SODL) onto the SCSI data bus. When the NCR 53C810 is an initiator, the SCSI I/O signal must be inactive to assert the SODL contents onto the SCSI bus. When the NCR 53C810 is a target, the SCSI I/O signal must be active for the SODL contents to be asserted onto the SCSI bus. The contents of the SODL register can be asserted at any time, even before the NCR 53C810 is connected to the SCSI bus. This bit should be cleared when executing SCSI SCRIPTS. It is normally used only for diagnostics testing or operation in low level mode.

Bit 5 DHP (Disable Halt on Parity Error or ATN) (Target Only)
The DHP bit is only defined for target mode. When this bit is cleared, the NCR 53C810 halts the SCSI data transfer when a parity error is detected or when the SATN/ signal is asserted. If SATN/ or a parity error is received in the middle of a data transfer, the NCR 53C810 may transfer up to three additional bytes before halting to synchronize between internal core cells. During synchronous operation, the NCR 53C810 transfers data until there are no outstanding synchronous offsets. If the NCR 53C810 is receiving data, any data residing in the DMA FIFO is sent to memory before halting.

When this bit is set, the NCR 53C810 does not halt the SCSI transfer when SATN/ or a parity error is received.

Bit 4 CON (Connected)
This bit is automatically set any time the NCR 53C810 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing arbitration or when the NCR 53C810 has responded to a bus initiated selection or reselection. It will also be set after successfully completing simple arbitration when operating in low level mode. When this bit is clear, the NCR 53C810 is not connected to the SCSI bus.

The CPU can force a connected or disconnected condition by setting or clearing this bit. This feature would be used primarily during loopback mode.

Bit 3 RST (Assert SCSI RST/ signal)
Setting this bit asserts the SCSI RST/ signal. The SRST/ output remains asserted until this bit is cleared. The 25 µs minimum assertion time defined in the SCSI specification must be timed out by the controlling microprocessor or a SCRIPTS loop.

Bit 2 AESP (Assert even SCSI parity (force bad parity))
When this bit is set , the NCR 53C810 asserts even parity. It forces a SCSI parity error on each byte sent to the SCSI bus from the NCR 53C810. If parity checking is enabled, then the NCR 53C810 checks data received for odd parity. This bit is used for diagnostic testing and should be clear for normal operation. It can be used to generate parity errors to test error handling functions.

Bit 1 IARB (Immediate Arbitration)

Setting this bit will cause the SCSI core to immediately begin arbitration once a Bus Free phase is detected following an expected SCSI disconnect. This bit is useful for multi-threaded applications. The ARB1-0 bits in SCNTL0 should be set for full arbitration and selection before setting this bit.

Arbitration will be re-tried until won. At that point, the NCR 53C810 will hold BSY and SEL asserted, and wait for a select or reselect sequence to be requested. The Immediate Arbitration bit will be reset automatically when the selection or reselection sequence is completed, or times out.

An unexpected disconnect condition will clear IARB without attempting arbitration. See the SCSI Disconnect Unexpected bit (SCNTL2, bit 7) for more information on expected versus unexpected disconnects.

An immediate arbitration sequence can be aborted. First, the Abort bit in the ISTAT register should be set. Then one of two things will eventually happen:

1) The Won Arbitration bit (SSTAT0 bit 2) will be asserted. In this case, the Immediate Arbitration bit needs to be reset. This will complete the abort sequence and disconnect the NCR 53C810 from the SCSI bus. If it is not acceptable to go to Bus Free phase immediately following the arbitration phase, a low level selection may instead be performed.

2) The abort will complete because the NCR 53C810 loses arbitration. This can be detected by the Immediate Arbitration bit being deasserted. The Lost Arbitration bit (SSTAT0 bit 3) should not be used to detect this condition. No further action needs to be taken in this case.

Bit 0 SST (Start SCSI Transfer)

This bit is automatically set during SCRIPTS execution, and should not be used. It causes the SCSI core to begin a SCSI transfer, including SREQ/SACK handshaking. The determination of whether the transfer is a send or receive is made according to the value written to the I/O bit in SOCL. This bit is self-resetting. This bit should not be set for low level operation.

CAUTION: Writing to this register while not connected may cause the loss of a selection/ reselection by resetting the Connected bit.

Register 02 (82)
SCSI Control Register Two (SCNTL2)
Read/Write

SDU			RESERVED				
7	6	5	4	3	2	1	0
Default>>>							
0	X	X	X	X	X	X	X

Bit 7 SDU (SCSI Disconnect Unexpected)
This bit is valid in initiator mode only. When this bit is set, the SCSI core is not expecting the SCSI bus to enter the Bus Free phase. If it does, an unexpected disconnect error will be generated (see the Unexpected Disconnect bit in the SIST0 register, bit 2). During normal SCRIPTS mode operation, this bit is set automatically whenever the SCSI core is reselected, or successfully selects another SCSI device. The SDU bit should be reset with a register write (MOVE 0X00 TO SCNTL2) before the SCSI core expects a disconnect to occur, normally prior to sending an Abort, Abort Tag, Bus Device Reset, Clear Queue or Release Recovery message, or before deasserting SACK/ after receiving a Disconnect command or Command Complete message.

Bits 6-0 Reserved

Register 03 (83)
SCSI Control Three (SCNTL3)
Read/Write

RES		SCF2-0		RES		CCF2-0	
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	0	X	0	0	0

Bit 7 Reserved

Bits 6-4 SCF2-0 (Synchronous Clock Conversion Factor)
These bits select a factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. They should be written to the same value as the Clock Conversion Factor bits below unless fast SCSI operation is desired. See the SXFER register for examples of how the SCF bits are used to calculate synchronous transfer periods. See the table under the description of bits 7-5 of the SCSI Transfer register for the valid combinations.

Note: For additional information on how the synchronous transfer rate is determined, refer to Chapter Two, "Functional Description."

Bit 3 Reserved

Bits 2-0 CCF2-0 (Clock Conversion Factor)
These bits select a factor by which the frequency of SCLK is divided before being presented to the SCSI core. The bits are encoded as follows. All other combinations are reserved and should never be used. Also note that the synchronous portion of the SCSI core can be run at a different clock rate for fast SCSI, using the synchronous clock conversion factor bits.

SCF2 CCF2	SCF1 CCF1	SCF0 CCF0	Factor Frequency	SCSI Clock (MHz)
0	0	0	SCLK / 3	50.01-66
0	0	1	SCLK / 1	16.67-25
0	1	0	SCLK/1.5	25.01-37.5
0	1	1	SCLK / 2	37.51-50
1	0	0	SCLK / 3	50.01-66
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

Note: It is important that these bits be set to the proper values to guarantee that the NCR 53C810 meets the SCSI timings as defined by the ANSI specification.

Note: For additional information on how the synchronous transfer rate is determined, refer to Chapter Two, "Functional Description."

Register 04 (84)
SCSI Chip ID (SCID)
Read/Write

RES 7	RRE 6	SRE 5	RES 4	RES 3	ENC 2	ENC 1	ENC 0
Default>>>							
X	0	0	X	X	0	0	0

Bit 7 Reserved

Bit 6 RRE (Enable Response to Reselection)
When this bit is set, the NCR 53C810 is enabled to respond to bus-initiated reselection at the chip ID in the RESPID register. Note that the NCR 53C810 will not automatically reconfigure itself to initiator mode as a result of being reselected.

Bit 5 SRE (Enable Response to Selection)
When this bit is set, the NCR 53C810 is able to respond to bus-initiated selection at the chip ID in the RESPID register. Note that the NCR 53C810 will not automatically reconfigure itself to target mode as a result of being selected.

Bits 4-3 Reserved

Bits 2-0 Encoded NCR 53C810 Chip SCSI ID, bits 2-0
These bits are used to store the NCR 53C810 encoded SCSI ID. This is the ID which the chip will assert when arbitrating for the SCSI bus. The IDs that the NCR 53C810 will respond to when being selected or reselcted are configured in the RESPID resgiter. The priority of the eight possible IDs, in descending order is:

Highest							Lowest
7	6	5	4	3	2	1	0

Register 05 (85)
SCSI Transfer (SXFER)
Read/Write

	TP2-0		RES		MO3-MO0		
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	X	0	0	0	0

Note: When using Table Indirect I/O commands, bits 7-0 of this register will be loaded from the I/O data structure.

Note: For additional information on how the synchronous transfer rate is determined, refer to Chapter Two, "Functional Description."

Bits 7-5 TP2-0 (SCSI Synchronous Transfer Period)

These bits determine the SCSI synchronous transfer period used by the NCR 53C810 when sending synchronous SCSI data in either initiator or target mode. These bits control the programmable dividers in the chip.

TP2	TP1	TP0	XFERP
0	0	0	4
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	11

The synchronous transfer period the NCR 53C810 should use when transferring SCSI data is found as in the following example: The NCR 53C810 is interfaced to a hard disk which can transfer data at 10 MB/s synchronously. The NCR 53C810's SCLK is running at 40 MHz. The synchronous transfer period (SXFERP) is found as follows:

SXFERP = Period/SSCP + ExtCC

Period = 1 ÷ Frequency = 1 ÷ 10 MB/s = 100 ns

SSCP = 1 ÷SSCF = 1 ÷ 40 MHz = 25 ns

(This SCSI synchronous core clock is determined in SCNTL3 bits 6-4).

ExtCC = 1 if SCNTL1 bit 7 is asserted and the NCR 53C810 is sending data.

(ExtCC = 0 if the NCR 53C810 is receiving data.)

SXFERP = 100 ÷ 25 = 4

Key: *SXFERP = Synchronous transfer period*
SSCP = SCSI Synchronous core period
SSCF = SCSI Synchronous core frequency
ExtCC = Extra clock cycle of data setup

Examples of synchronous transfer periods for SCSI-1 transfer rates.

CLK (MHz)	SCSI CLK ÷ SCNTL3 bits 6-4	XFERP	Synch Transfer Period (ns)	Synch Transfer Rate (MB/S)
66.67	÷ 3	4	180	5.55
66.67	÷ 3	5	225	4.44
50	÷ 2	4	160	6.25
50	÷ 2	5	200	5
40	÷ 2	4	200	5
37.50	÷ 1.5	4	160	6.25
33.33	÷ 1.5	4	180	5.55
25	÷ 1	4	160	6.25
20	÷ 1	4	200	5
16.67	÷ 1	4	240	4.17

Example transfer periods for fast SCSI-2 transfer rates.

CLK (MHz)	SCSI CLK ÷ SCNTL3 bits 6-4	XFERP	Synch Transfer Period (ns)	Synch Transfer Rate (MB/S)
66.67	÷ 1.5	4	90	11.11
66.67	÷ 1.5	5	112.5	8.88
50	÷ 1	4	80	12.5
50	÷ 1	5	100	10.0
40	÷ 1	4	100	10.0
37.50	÷ 1	4	106.67	9.375
33.33	÷ 1	4	120	8.33
25	÷ 1	4	160	6.25
20	÷ 1	4	200	5
16.67	÷ 1	4	240	4.17

Bit 4 Reserved

Bits 3-0 MO3-MO0 (Max SCSI synchronous offset)

These bits describe the maximum SCSI synchronous offset used by the NCR 53C810 when transferring synchronous SCSI data in either initiator or target mode. The following table describes the possible combinations and their relationship to the synchronous data offset used by the NCR 53C810. These bits determine the NCR 53C810's method of transfer for Data In and Data Out phases only; all other information transfers will occur asynchronously.

MO3	MO2	MO1	MO0	Synchronous Offset
0	0	0	0	0 – Asynchronous
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	X	X	1	Reserved
1	X	1	X	Reserved
1	1	X	X	Reserved

Register 06 (86)
SCSI Destination ID (SDID)
Read/Write

RESERVED					ENC2-0		
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	0	0	0

Bits 7-3 Reserved

Bits 2-0 Encoded destination SCSI ID

Writing these bits sets the SCSI ID of the intended initiator or target during SCSI reselection or selection phases respectively. When executing SCSI SCRIPTS, the SCRIPTS processor writes the destination SCSI ID to this register. The SCSI ID is defined by the user in a SCSI SCRIPTS SELECT or RESELECT instruction. The value written should be the binary-encoded ID value. The priority of the eight possible IDs, in descending order, is:

Highest							Lowest
7	6	5	4	3	2	1	0

Register 07 (87)
General Purpose (GPREG)
Read/Write

RESERVED						GPIO1	GPIO0
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	X	X	X

Bits 7-2 Reserved

Bits 1-0 GPIO1-GPIO0 (General Purpose)
These bits can be programmed through the GPCNTL Register to become inputs, outputs or special functions. As an output, these pins can be used to enable or disable external terminators. These signals can also be programmed as live inputs and sensed through a SCRIPTS Register to Register Move Instruction. These bits default as inputs and are pulled up internally.

Register 08 (88)
SCSI First Byte Received (SFBR)
Read/Write

1B7	1B6	1B5	1B4	1B3	1B2	1B1	1B0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

This register contains the first byte received in any asynchronous information transfer phase. For example, when the NCR 53C810 is operating in initiator mode, this register contains the first byte received in Message In, Status Phase, Reserved In and Data In.

When a Block Move Instruction is executed for a particular phase, the first byte received is stored in this register - even if the present phase is the same as the last phase. The first byte-received value for a particular input phase is not valid until after a MOVE instruction is executed.

This register is also the accumulator for register read-modify-writes with the SFBR as the destination. This allows bit testing after an operation.

The SFBR is not writable via the CPU, and therefore not by a Memory Move. However, it can be loaded via SCRIPTS Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate NCR 53C810 register (such as the SCRATCH register), and then to the SFBR.

This register will also contain the state of the SCSI data bus during the selection phase if the COM bit in the DCNTL register is clear.

Register 09 (89)
SCSI Output Control Latch (SOCL)
Read /Write

REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 REQ (Assert SCSI REQ/ signal)

Bit 6 ACK (Assert SCSI ACK/ signal)

Bit 5 BSY (Assert SCSI BSY/ signal)

Bit 4 SEL (Assert SCSI SEL/ signal)

Bit 3 ATN (Assert SCSI ATN/ signal)

Bit 2 MSG (Assert SCSI MSG/ signal)

Bit 1 C/D (Assert SCSI C_D/ signal)

Bit 0 I/O (Assert SCSI I_O/ signal)

This register is used primarily for diagnostic testing or programmed I/O operation. It is controlled by the SCRIPTS processor when executing SCSI SCRIPTS. SOCL should only be used when transferring data via programmed I/O. Some bits are set (1) or reset (0) when executing SCSI SCRIPTS. Do not write to the register once the NCR 53C810 starts executing normal SCSI SCRIPTS.

Register 0A (09)
SCSI Selector ID Register (SSID)
Read Only

VAL	RESERVED				ENCID2-0		
7	6	5	4	3	2	1	0
Default>>>							
0	X	X	X	X	0	0	0

Bit 7 VAL (SCSI Valid Bit)

If VAL is asserted, the two SCSI IDs were detected on the bus during a bus-initiated selection or reselection, and the encoded destination SCSI ID bits below are valid. If VAL is deasserted, only one ID was present and the contents of the encoded destination ID are meaningless.

Bits 6-3 Reserved

Bits 2-0 Encoded Destination SCSI ID

Reading the SSID register immediately after the NCR 53C810 has been selected or reselected returns the binary-encoded SCSI ID of the device which performed the operation. These bits are invalid for targets that are selected under the single initiator option of the SCSI-1 specification. This condition can be detected by examining the VAL bit above.

Register 0B (8B)
SCSI Bus Control Lines (SBCL)
Read Only

REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	X	X	X

Bit 7 REQ (SREQ/ status)
Bit 6 ACK (SACK/ status)
Bit 5 BSY (SBSY/ status)
Bit 4 SEL (SSEL/ status)
Bit 3 ATN (SATN/ status)
Bit 2 MSG (SMSG/ status)
Bit 1 C/D (SC_D/ status)
Bit 0 I/O (SI_O/ status)

When read, this register returns the SCSI control line status. A bit will be set when the corresponding SCSI control line is asserted. These bits are not latched; they are a true representation of what is on the SCSI bus at the time the register is read. The resulting read data is synchronized before being presented to the PCI bus to prevent parity errors from being passed to the system. This register can be used for diagnostics testing or operation in low level mode.

Register 0C (8C)
DMA Status (DSTAT)
Read Only

DFE	MDPE	BF	ABRT	SSI	SIR	RES	IID
7	6	5	4	3	2	1	0
Default>>>							
1	0	0	0	0	0	X	0

Reading this register will clear any bits that are set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the NCR 53C810 stacks interrupts). The DIP bit in the ISTAT register will also be cleared. DMA interrupt conditions may be individually masked through the DIEN register.

When performing consecutive 8-bit reads of the DSTAT, SIST0 and SIST1 registers (in any order), insert a delay equivalent to 12 CLK periods between the reads to ensure that the interrupts clear properly. See Chapter Two, "Functional Description," for more information on interrupts.

Bit 7 DFE (DMA FIFO empty)
This status bit is set when the DMA FIFO is empty. It may be used to determine if any data resides in the FIFO when an error occurs and an interrupt is generated. This bit is a pure status bit and will not cause an interrupt.

Bit 6 MDPE (Master Data Parity Error)
This bit is set when the NCR 53C810 as a master detects that a target device has signalled a parity error during a data phase. This bit is completely disabled by Master Parity Error Enable (bit 3 of CTEST4).

Bit 5 BF (Bus fault)
This bit is set when a PCI bus fault condition is detected. A PCI bus fault can only occur when the NCR 53C810 is bus master, and is defined as a cycle that ends with a Bad Address or Target Abort Condition.

Bit 4 ABRT (Aborted)
This bit is set when an abort condition occurs. An abort condition occurs when a software abort command is issued by setting bit 7 of the ISTAT register.

Bit 3 SSI (Single step interrupt)
If the Single-Step Mode bit in the DCNTL register is set, this bit will be set and an interrupt generated after successful execution of each SCRIPTS instruction.

Bit 2 SIR (SCRIPTS interrupt instruction received)
This status bit is set whenever an Interrupt instruction is evaluated as true.

Bit 1 Reserved

Bit 0 IID (Illegal instruction detected)
This status bit will be set any time an illegal instruction is detected, whether the NCR 53C810 is operating in single-step mode or automatically executing SCSI SCRIPTS. This bit will also be set if the NCR 53C810 is executing a Wait Disconnect instruction and the SCSI REQ line is asserted without a disconnect occurring.

Register 0D (8D)
SCSI Status Zero (SSTAT0)
Read Only

ILF	ORF	OLF	AIP	LOA	WOA	RST	SDP
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 ILF (SIDL full)
This bit is set when the SCSI Input Data Latch register (SIDL) contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch register before being sent to the DMA FIFO and then to the host bus. The SIDL register contains SCSI data received asynchronously. Synchronous data received does not flow through this register.

Bit 6 ORF (SODR full)
This bit is set when the SCSI Output Data Register (SODR, a hidden buffer register) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It is not accessible to the user (cannot be read or written). This bit can be used to determine how many bytes reside in the chip when an interrupt occurs.

Bit 5 OLF (SODL full)
This bit is set when the SCSI Output Data Latch (SODL) contains data. The SODL register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. This bit can be used to determine how many bytes reside in the chip when an error occurs.

Bit 4 AIP (Arbitration in progress)
Arbitration in Progress (AIP = 1) indicates that the NCR 53C810 has detected a bus free condition, asserted BSY and asserted its SCSI ID onto the SCSI bus.

Bit 3 LOA (Lost arbitration)
When set, LOA indicates that the NCR 53C810 has detected a bus free condition, arbitrated for the SCSI bus, and lost arbitration due to another SCSI device asserting the SSEL/ signal.

Bit 2 WOA (Won arbitration)
When set, WOA indicates that the NCR 53C810 has detected a bus free condition, arbitrated for the SCSI bus, and won arbitration. The arbitration mode selected in the SCNTL0 register must be full arbitration and selection for this bit to be set.

Bit 1 RST (SCSI reset signal)
This bit reports the current status of the SRST/ signal, and the SRST signal bit (bit 6) in the ISTAT register.

Bit 0 SDP (SCSI parity signal)
This bit represents the active high current status of the SCSI SDP/ parity signal.

Register 0E (8E)
SCSI Status One (SSTAT1)
Read Only

FF3	FF2	FF1	FF0	SDPL	MSG	C/D	I/O
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	X	X	X	X

Bits 7-4 FF3-FF0 (FIFO flags)

FF3	FF2	FF1	FF0	Bytes or Words in the SCSI FIFO
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

These four bits define the number of bytes that currently reside in the NCR 53C810's SCSI synchronous data FIFO. These bits are not latched and they will change as data moves through the FIFO. Because the FIFO is only 9 bytes deep, values over nine will not occur.

Bit 3 SDPL (Latched SCSI parity)
This bit reflects the SCSI parity signal (SDP/), corresponding to the data latched in the SCSI Input Data Latch register (SIDL). It changes when a new byte is latched into the least significant byte of the SIDL register. This bit is active high, in other words, it is set when the parity signal is active.

Bit 2 MSG (SCSI MSG/ signal)

Bit 1 C/D (SCSI C_D/ signal)

Bit 0 I/O (SCSI I_O/ signal)
These SCSI phase status bits are latched on the asserting edge of SREQ/ when operating in either initiator or target mode. These bits are set when the corresponding signal is active. They are useful when operating in low level mode.

Register 0F (8F)
SCSI Status Two (SSTAT2)
(Read Only)

RESERVED						LDSC	RES
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	X	1	X

Bits 7-2 Reserved

Bit 1 LDSC (Last Disconnect)

Used in conjunction with the Connected (CON) bit in SCNTL1, this status bit allows the user to detect the case in which a target device disconnects, and then some SCSI device selects or reselects the NCR 53C810. If the CON bit is asserted and the LDSC bit is asserted, a disconnect has occurred.

Bit 0 Reserved

Registers 10-13 (90-93)
Data Structure Address (DSA)
Read/Write

This 32-bit register contains the base address used for all table indirect calculations. The DSA register is usually loaded prior to starting an I/O, but it is possible for a SCRIPTS Memory Move to load the DSA during the I/O.

During any Memory-to-Memory Move operation, the contents of this register are preserved. The power-up value of this register is indeterminate.

Register 14 (94)
Interrupt Status (ISTAT)
(Read/Write)

ABRT	SRST	SIGP	SEM	CON	INTF	SIP	DIP
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

This is the only register that can be accessed by the host CPU while the NCR 53C810 is executing SCRIPTS (without interfering in the operation of the NCR 53C810). It may be used to poll for interrupts if interrupts are disabled. There may be stacked interrupts pending; read this register after servicing an interrupt to check for stacked interrupts. For more information on interrupt handling refer to Chapter Two, "Functional Description."

Bit 7 ABRT (Abort operation)
Setting this bit aborts the current operation being executed by the NCR 53C810. If this bit is set and an interrupt is received, reset this bit before reading the DSTAT register to prevent further aborted interrupts from being generated. The sequence to abort any operation is:

1) Set this bit.
2) Wait for an interrupt.
3) Read the ISTAT register.
4) If the SCSI Interrupt Pending bit is set, then read the SIST0 or SIST1 register to determine the cause of the SCSI Interrupt and go back to Step 2.
5) If the SCSI Interrupt Pending bit is clear, and the DMA Interrupt Pending bit is set, then write 00h value to this register.
6) Read the DSTAT register to verify the aborted interrupt and to see if any other interrupting conditions have occurred.

Bit 6 SRST (Software reset)
Setting this bit resets the NCR 53C810. All operating registers are cleared to their respective default values and all SCSI signals are deasserted. Setting this bit does not cause the SCSI RST/ signal to be asserted. This reset will not clear the ID Mode bit or any of the PCI configuration registers. This bit is not self-clearing; it must be cleared to clear the reset condition (a hardware reset will also clear this bit).

Bit 5 SIGP (Signal process)
SIGP is a R/W bit that can be written at any time, and polled and reset via CTEST2. The SIGP bit can be used in various ways to pass a flag to or from a running SCRIPTS.

The only SCRIPTS instruction directly affected by the SIGP bit is Wait For Selection/ Reselection. Setting this bit causes that instruction to jump to the alternate address immediately. The instructions at the alternate jump address should check the status of SIGP to determine the cause of the jump. The SIGP bit may be used at any time and is not restricted to the wait for selection/ reselection condition.

Bit 4 SEM (Semaphore)
This bit can be set by the SCRIPTS processor using a SCRIPTS register write instruction. The bit may also be set by an external processor while the NCR 53C810 is executing a SCRIPTS operation. This bit enables the NCR 53C810 to notify an external processor of a predefined condition while SCRIPTS are running. The external processor may also notify the NCR 53C810 of a predefined condition and the SCRIPTS processor may take action while SCRIPTS are executing.

Bit 3 CON (Connected)
This bit is automatically set any time the NCR 53C810 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing selection or when the NCR 53C810 has responded to a bus-initiated selection or reselection. It will also be set after successfully completing arbitration when operating in low level mode. When this bit is clear, the NCR 53C810 is not connected to the SCSI bus.

Bit 2 INTF (Interrupt on the Fly)

This bit is asserted by an INTFLY instruction during SCRIPTS execution. SCRIPTS programs will not halt when the interrupt occurs. This bit can be used to notify a service routine, running on the main processor while the SCRIPTS processor is still executing a SCRIPTS program. If this bit is set, when the ISTAT register is read it will not automatically be cleared. To clear this bit, it must be written to a one. The reset operation is self-clearing.

Note: If the INTF bit is set but SIP or DIP is not set, do not attempt to read the other chip status registers. An interrupt-on-the-fly interrupt must be cleared before servicing any other interrupts indicated by SIP or DIP.

Note: This bit must be written to one in order to clear it after it has been set.

Bit 1 SIP (SCSI interrupt pending)

This status bit is set when an interrupt condition is detected in the SCSI portion of the NCR 53C810. The following conditions will cause a SCSI interrupt to occur:

- A phase mismatch (initiator mode) or SATN/ becomes active (target mode)
- An arbitration sequence complete
- A selection or reselection time-out occurs
- The NCR 53C810 was selected
- The NCR 53C810 was reselected
- A SCSI gross error occurs
- An unexpected disconnect occurs
- A SCSI reset occurs
- A parity error is detected
- A selection/reselection time-out occurs
- The handshake-to-handshake timer is expired
- The general purpose timer is expired.

To determine exactly which condition(s) caused the interrupt, the SIST0 and SIST1 registers should be read.

Bit 0 DIP (DMA interrupt pending)

This status bit is set when an interrupt condition is detected in the DMA portion of the NCR 53C810. The following conditions will cause a DMA interrupt to occur:

- A PCI parity error is detected
- A bus fault is detected
- An abort condition is detected
- A SCRIPTS instruction is executed in single-step mode
- A SCRIPTS interrupt instruction is executed
- An illegal instruction is detected.

To determine exactly which condition(s) caused the interrupt, the DSTAT register should be read.

Register 18 (98)
Chip Test Zero (CTEST0)
Read/Write

CTEST0 is a general purpose, user-definable read/write register. Apart from CPU access, only Register Read/Write and Memory Moves into this register will alter its contents. The default value of this register is zero.

Register 19 (91)
Chip Test One (CTEST1)
Read Only

FMT3	FMT2	FMT1	FMT0	FFL3	FFL2	FFL1	FFL0
7	6	5	4	3	2	1	0
Default >>>							
1	1	1	1	0	0	0	0

Bits 7-4 FMT3-0 (Byte Empty in DMA FIFO)

These bits identify the bottom bytes in the DMA FIFO that are empty. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is empty, then FMT3 will be set. Since the FMT flags indicate the status of bytes at the bottom of the FIFO, if all FMT bits are set, the DMA FIFO is empty.

Bits 3-0 FFL3-0 (Byte Full in DMA FIFO)

These status bits identify the top bytes in the DMA FIFO that are full. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is full then FFL3 will be set. Since the FFL flags indicate the status of bytes at the top of the FIFO, if all FFL bits are set, the DMA FIFO is full.

Register 1A (9A)
Chip Test Two (CTEST2)
Read Only

DDIR	SIGP	CIO	CM	RES	TEOP	DREQ	DACK
7	6	5	4	3	2	1	0
Default>>>							
0	0	X	X	0	0	0	1

Bit 7 DDIR (Data Transfer Direction)
This status bit indicates which direction data is being transferred. When this bit is set, the data will be transferred from the SCSI bus to the host bus. When this bit is clear, the data will be transferred from the host bus to the SCSI bus.

Bit 6 SIGP (Signal process)
This bit is a copy of the SIGP bit in the ISTAT register (bit 5). The SIGP bit is used to signal a running SCRIPTS instruction. When this register is read, the SIGP bit in the ISTAT register is cleared.

Bit 5 CIO (Configured as I/O)
This bit is defined as the Configuration I/O Enable Status bit. This read-only bit indicates if the chip is currently enabled as I/O space.
Note: both bits 4 and 5 may be set if the chip is dual-mapped.

Bit 4 CM (Configured as Memory)
This bit is defined as the Configuration Memory enable status bit. This read-only bit indicates if the chip is currently enabled as memory space.
Note: both bits 4 and 5 may be set if the chip is dual-mapped.

Bit 3 Reserved

Bit 2 TEOP (SCSI true end of process)
This bit indicates the status of the NCR 53C810's internal TEOP signal. The TEOP signal acknowledges the completion of a transfer through the SCSI portion of the NCR 53C810. When this bit is set, TEOP is active. When this bit is clear, TEOP is inactive.

Bit 1 DREQ (Data request status)
This bit indicates the status of the NCR 53C810's internal Data Request signal (DREQ). When this bit is set, DREQ is active. When this bit is clear, DREQ is inactive.

Bit 0 DACK (Data acknowledge status)
This bit indicates the status of the NCR 53C810's internal Data Acknowledge signal (DACK/). When this bit is set, DACK/ is inactive. When this bit is clear, DACK/ is active.

Register 1B (9B)
Chip Test Three (CTEST3)
Read/Write

V3	V2	V1	V0	FLF	CLF	FM	RES
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	1	0	0	0	X

Bits 7-4 V3-V0 (Chip revision level)
These bits identify the chip revision level for software purposes. This data manual applies to devices that have these bits set to 01h.

Bit 3 FLF (Flush DMA FIFO)
When this bit is set, data residing in the DMA FIFO is transferred to memory, starting at the address in the DNAD register. The internal DMAWR signal, controlled by the CTEST5 register, determines the direction of the transfer. This bit is not self clearing; once the NCR 53C810 has successfully transferred the data, this bit should be reset.

Note: Polling of FIFO flags is allowed during flush operations.

Bit 2 CLF (Clear DMA FIFO)
When this bit is set, all data pointers for the DMA FIFO are cleared. Any data in the FIFO is lost. This bit automatically resets after the NCR 53C810 has successfully cleared the appropriate FIFO pointers and registers.

Note: This bit does not clear the data visible at the bottom of the FIFO.

Bit 1 FM (Fetch pin mode)
When set, this bit causes the FETCH/ pin to deassert during indirect and table indirect read operations. FETCH/ will only be active during the op code portion of an instruction fetch. This allows SCRIPTS to be stored in a PROM while data tables are stored in RAM.

If this bit is not set, FETCH/ will be asserted for all bus cycles during instruction fetches.

Bit 0 Reserved

Registers 1C-1F (9C-9F)
Temporary Stack (TEMP)
Read/Write

This 32-bit register stores the Return instruction address pointer from the Call instruction. The address pointer stored in this register is loaded into the DSP register when a Return instruction is executed. This address points to the next instruction to be executed. Do not write to this register while the NCR 53C810 is executing SCRIPTS.

During any Memory-to-Memory Move operation, the contents of this register are preserved. The power-up value of this register is indeterminate.

Register 20 (A0)
DMA FIFO (DFIFO)
Read/Write

RES	BO6	BO5	BO4	BO3	BO2	BO1	BO0
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	0	0	0	0	0

Bit 7 Reserved

Bits 6-0 BO6-BO0 (Byte offset counter)
These six bits indicate the amount of data transferred between the SCSI core and the DMA core. It may be used to determine the number of bytes in the DMA FIFO when an interrupt occurs. These bits are unstable while data is being transferred between the two cores; once the chip has stopped transferring data, these bits are stable.

Since the DFIFO register counts the number of bytes transferred between the DMA core and the SCSI core, and the DBC register counts the number of bytes transferred across the host bus, the difference between these two counters represents the number of bytes remaining in the DMA FIFO.

The following steps will determine how many bytes are left in the DMA FIFO when an error occurs, regardless of the direction of the transfer:

1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register

2) AND the result with 7Fh for a byte count between zero and 64

Note: If trying to calculate the total number of bytes in both the DMA FIFO and SCSI logic, see the section on Data Paths in Chapter Two, "Functional Description."

Register 21 (A1)
Chip Test Four (CTEST4)
Read/Write

BDIS	ZMOD	ZSD	SRTM	MPEE	FBL2	FBL1	FBL0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 BDIS (Burst Disable)
When set, this bit will cause the NCR 53C810 to perform back to back cycles for all transfers. When reset, the NCR 53C810 will perform back to back transfers for op code fetches and burst transfers for data moves.

Bit 6 ZMOD (High impedance mode)
Setting this bit causes the NCR 53C810 to place all output and bidirectional pins into a high-impedance state. In order to read data out of the NCR 53C810, this bit must be cleared. This bit is intended for board-level testing only. Do not set this bit during normal system operation.

Bit 5 ZSD (SCSI Data High Impedance)
Setting this bit causes the NCR 53C810 to place the SCSI data bus SD and the parity line SDP in a high-impedance state. In order to transfer data on the SCSI bus, this bit must be cleared.

Bit 4 SRTM (Shadow Register Test Mode)
Asserting this bit allows access to the shadow registers used by memory-to-memory Move operations. When this bit is set, register accesses to the TEMP and DSA registers are directed to the shadow copies STEMP (Shadow TEMP) and SDSA (Shadow DSA). The registers are shadowed to prevent them from being overwritten during a Memory-to-Memory Move operation. The DSA and TEMP registers contain the base address used for table indirect calculations, and the address pointer for a call or return instruction, respectively. This bit is intended for manufacturing diagnostics only and should not be set during normal operations.

Bit 3 MPEE (Master Parity Error Enable)
Asserting this bit enables parity checking during master data phases. A parity error during a bus master read is detected by the NCR 53C810. A parity error during a bus master write is detected by the target, and the NCR 53C810 is informed of the error by the PERR/ pin being asserted by the target. When this bit is reset, the NCR 53C810 will not interrupt if a master parity error occurs. This bit is reset at power up.

Bits 2-0 FBL2-FBL0 (FIFO byte control)

FBL2	FBL1	FBL0	DMA FIFO Byte Lane	Pins
0	X	X	Disabled	n/a
1	0	0	0	D(7-0)
1	0	1	1	D(15-8)
1	1	0	2	D(23-16)
1	1	1	3	D(31-24)

These bits steer the contents of the CTEST6 register to the appropriate byte lane of the 32-bit DMA FIFO. If the FBL2 bit is set, then FBL1 and FBL0 determine which of four byte lanes can be read or written. When cleared, the byte lane read or written is determined by the current contents of the DNAD and DBC registers. Each of the four bytes that make up the 32-bit DMA FIFO can be accessed by writing these bits to the proper value. For normal operation, FBL2 must equal zero.

Register 22 (A2)
Chip Test Five (CTEST5)
Read/Write

ADCK	BBCK	RES	MASR	DDIR	RESERVED		
7	6	5	4	3	2	1	0
Default>>>							
0	0	X	0	0	X	X	X

Bit 7 ADCK (Clock address incrementor)
Setting this bit increments the address pointer contained in the DNAD register. The DNAD register is incremented based on the DNAD contents and the current DBC value. This bit automatically clears itself after incrementing the DNAD register.

Bit 6 BBCK (Clock byte counter)
Setting this bit decrements the byte count contained in the 24-bit DBC register. It is decremented based on the DBC contents and the current DNAD value. This bit automatically clears itself after decrementing the DBC register.

Bit 5 Reserved

Bit 4 MASR (Master control for set or reset pulses)
This bit controls the operation of bit 3. When this bit is set, bit 3 asserts the corresponding signals. When this bit is reset, bit 3 deasserts the corresponding signals. This bit and bit 3 should not be changed in the same write cycle.

Bit 3 DDIR (DMA direction)
Setting this bit either asserts or deasserts the internal DMA Write (DMAWR) direction signal depending on the current status of the MASR bit in this register. Asserting the DMAWR signal indicates that data will be transferred from the SCSI bus to the host bus. Deasserting the DMAWR signal transfers data from the host bus to the SCSI bus.

Bits 2-0 Reserved

Register 23 (A3)
Chip Test Six (CTEST6)
Read/Write

DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bits 7-0 DF7-DF0 (DMA FIFO)

Writing to this register writes data to the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Reading this register unloads data from the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Data written to the FIFO is loaded into the top of the FIFO. Data read out of the FIFO is taken from the bottom. To prevent DMA data from being corrupted, this register should not be accessed before starting or restarting SCRIPTS operation. This register should only be written when testing the DMA FIFO using the CTEST4 register. Writes to this register while the test mode is not enabled will have unexpected results.

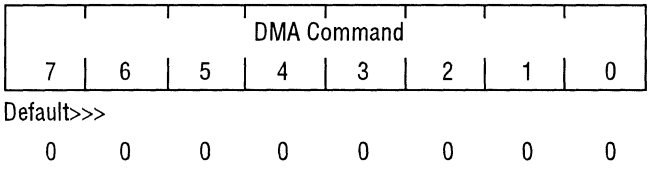
Registers 24-26 (A4-A6)
DMA Byte Counter (DBC)
Read/Write

This 24-bit register determines the number of bytes to be transferred in a Block Move instruction. While sending data to the SCSI bus, the counter is decremented as data is moved into the DMA FIFO from memory. While receiving data from the SCSI bus, the counter is decremented as data is written to memory from the NCR 53C810. The DBC counter is decremented each time that data is transferred on the PCI bus. It is decremented by an amount equal to the number of bytes that were transferred.

The maximum number of bytes that can be transferred in any one Block Move command is 16,777,215 bytes. The maximum value that can be loaded into the DBC register is FFFFFFh. If the instruction is a Block Move and a value of 000000h is loaded into the DBC register, an illegal instruction interrupt will occur if the NCR 53C810 is not in target mode Command phase.

The DBC register is also used to hold the least significant 24 bits of the first longword of a SCRIPT fetch, and to hold the offset value during table indirect I/O SCRIPTS. For a complete description, see Chapter Six, "Instruction Set of the I/O Processor." The power-up value of this register is indeterminate.

Register 27 (A7)
DMA Command (DCMD)
Read/Write



This 8-bit register determines the instruction for the NCR 53C810 to execute. This register has a different format for each instruction. For a complete description, see Chapter Six, "Instruction Set of the I/O Processor."

Registers 28-2B (A8-AB)
DMA Next Data Address (DNAD)
Read/Write

This 32-bit register contains the general purpose address pointer. At the start of some SCRIPTS operations, its value is copied from the DSPS register. Its value may not be valid except in certain abort conditions. The default value of this register is zero.

Registers 2C-2F (AC-AF) DMA SCRIPTS Pointer (DSP) Read/Write

To execute SCSI SCRIPTS, the address of the first SCRIPTS instruction must be written to this register. In normal SCRIPTS operation, once the starting address of the SCRIPT is written to this register, SCRIPTS are automatically fetched and executed until an interrupt condition occurs.

In single-step mode, there is a single step interrupt after each instruction is executed. The DSP register does not need to be written with the next address, but the Start DMA bit (bit 2, DCNTL register) must be set each time the step interrupt occurs to fetch and execute the next SCRIPTS command. When writing this register eight bits at a time, writing the upper eight bits begins execution of the SCSI SCRIPTS. The default value of this register is zero.

Registers 30-33 (B0-B3) DMA SCRIPTS Pointer Save (DSPS) Read/Write

This register contains the second longword of a SCRIPTS instruction. It is overwritten each time a SCRIPTS instruction is fetched. When a SCRIPTS interrupt instruction is executed, this register holds the interrupt vector. The power-up value of this register is indeterminate.

Registers 34-37 (B4-B7)
Scratch Register A (SCRATCH A)
Read/Write

This is a general purpose user-definable scratch pad register. Apart from CPU access, only Register Read/Write and Memory Moves into the SCRATCH register will alter its contents. The power-up value of this register is indeterminate.

Register 38 (B8)
DMA Mode (DMODE)
Read/Write

BL1	BL0	SIOM	DIOM	ER	RES		MAN
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	X	X	0

Bit 7-6 BL1-BL0 (Burst length)

BL1	BL0	Burst Length
0	0	2- transfer burst
0	1	4- transfer burst
1	0	8-transfer burst
1	1	16-transfer burst

These bits control the maximum number of transfers performed per bus ownership. The NCR 53C810 asserts the Bus Request (REQ/) output when the DMA FIFO can accommodate a transfer of at least one burst size of data. Bus Request (REQ/) is also asserted during start-of-transfer and end-of-transfer cleanup and alignment, even though less than a full burst of transfers may be performed. The NCR 53C810 inserts a "fairness delay" of four CLKs between burst-length transfers (as set in BL1-0) during normal operation. The fairness delay is not inserted during PCI retry cycles. This gives the CPU and other bus master devices the opportunity to access memory between bursts. This is the maximum possible number of transfers per bus ownership regardless of whether the transfers are back-to-back, burst, or a combination of both.

Bit 5 SIOM (Source I/O-Memory Enable)

This bit is defined as an I/O Memory Enable bit for the source address of a Memory Move or Block Move Command. If this bit is set, then the source address is in I/O space; and if reset, then the source address is in memory space.

This function is useful for register-to-memory operations using the Memory Move instruction when the NCR 53C810 is I/O mapped. Bits 4 and 5 of the CTEST2 register can be used to determine the configuration status of the NCR 53C810.

Bit 4 DIOM (Destination I/O-Memory Enable)
This bit is defined as an I/O Memory Enable bit for the destination address of a Memory Move or Block Move Command. If this bit is set, then the destination address is in I/O space; and if reset, then the destination address is in memory space.

This function is useful for memory to register operations using the Memory Move instruction when the NCR 53C810 is I/O mapped. Bits 4 and 5 of the CTEST2 register can be used to determine the configuration status of the NCR 53C810.

Bit 3 ERL (Enable Read Line)
This bit enables a read line command. If this bit is set and the chip is about to execute a read cycle other than an op code fetch, then the command will be 1110.

The PCI Cache Line Size register is not supported in the NCR 53C810 and does not affect the execution of the read transfers. The only difference in NCR 53C810 read cycle operation is the command type.

Bits 2-1 Reserved

Bit 0 MAN (Manual Start Mode)
Setting this bit prevents the NCR 53C810 from automatically fetching and executing SCSI SCRIPTS when the DSP register is written. When this bit is set, the Start DMA bit in the DCNTL register must be set to begin SCRIPTS execution. Clearing this bit causes the NCR 53C810 to automatically begin fetching and executing SCSI SCRIPTS when the DSP register is written. This bit normally is not used for SCSI SCRIPTS operations.

Register 39 (B9)
DMA Interrupt Enable (DIEN)
Read/Write

RES	MDPE	BF	ABRT	SSI	SIR	RES	IID
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	0	0	0	X	0

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the DSTAT register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the DSTAT register. Masking an interrupt will not prevent the ISTAT DIP from being set. All DMA interrupts are considered fatal, therefore SCRIPTS will stop running when this condition occurs, whether or not the interrupt is masked. Setting a mask bit enables the assertion of IRQ/ for the corresponding interrupt. (A masked non-fatal interrupt will not prevent un-masked or fatal interrupts from getting through; interrupt stacking does not begin until either the ISTAT SIP or DIP bit is set.)

The NCR 53C810 IRQ/ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted.

For more information on interrupts, see Chapter Two, "Functional Description."

Bit 7 Reserved

Bit 6 MDPE (Master Data Parity Error)

Bit 5 BF (Bus fault)

Bit 4 ABRT (Aborted)

Bit 3 SSI (Single step interrupt)

Bit 2 SIR (SCRIPTS interrupt instruction received)

Bit 1 Reserved

Bit 0 IID (Illegal instruction detected)

Register 3A (BA)
DMA Watchdog Timer (DWT)
Read/Write

This is a general purpose register. Apart from CPU access, only Register Read/Write and Memory Moves into this register will alter its contents. The default value of this register is zero.

Register 3B (BB)
DMA Control (DCNTL)
Read/Write

RESERVED			SSM	IRQM	STD	RES	COM
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	0	0	0	X	0

Bits 7-5 Reserved

Bit 4 SSM (Single-step mode)
Setting this bit causes the NCR 53C810 to stop after executing each SCRIPTS instruction, and generate a single step interrupt. When this bit is clear the NCR 53C810 will not stop after each instruction; instead it continues fetching and executing instructions until an interrupt condition occurs. For normal SCSI SCRIPTS operation, this bit should be clear. To restart the NCR 53C810 after it generates a SCRIPTS Step interrupt, the ISTAT and DSTAT registers should be read to clear the interrupt and then the START DMA bit in this register should be set.

Bit 3 IRQM (IRQ Mode)
When set, this bit will enable a totem pole driver for the IRQ pin. When reset, this bit will enable an open drain driver for the IRQ pin with a internal weak pullup. This bit is reset at power up.

Bit 2 STD (Start DMA operation)
The NCR 53C810 fetches a SCSI SCRIPTS instruction from the address contained in the DSP register when this bit is set. This bit is required if the NCR 53C810 is in one of the following modes:

1) *Manual start mode* – Bit 0 in the DMODE register is set
2) *Single-step mode* – Bit 4 in the DCNTL register is set

When the NCR 53C810 is executing SCRIPTS in manual start mode, the Start DMA bit needs to be set to start instruction fetches, but does not need to be set again until an interrupt occurs. When the NCR 53C810 is in single-step mode, the Start DMA bit needs to be set to restart execution of SCRIPTS after a single-step interrupt.

Bit 1 Reserved

Bit 0 COM (53C700 compatibility)
When this bit is clear, the NCR 53C810 will behave in a manner compatible with the 53C700; selection/reselection IDs will be stored in both the SSID and SFBR registers.

When this bit is set, the ID will be stored only in the SSID register, protecting the SFBR from being overwritten should a selection/ reselection occur during a DMA register-to-register operation.

Register 3C-3F (BC-BF) Adder Sum Output (ADDER) Read Only

This register contains the output of the internal adder, and is used primarily for test purposes. The power-up value for this register is indeterminate.

Register 40 (C0)
SCSI Interrupt Enable Zero (SIEN0)
Read/Write

M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the SIST0 register. An interrupt is masked by clearing the appropriate mask bit.

For more information on interrupts, see Chapter 2, "Functional Description."

Bit 7 M/A (SCSI Phase Mismatch - Initiator Mode; SCSI ATN Condition - Target Mode)
In initiator mode, the SCSI phase asserted by the target and sampled during REQ does not match the expected phase in the SOCL register. This expected phase is automatically written by the SCSI SCRIPTS. In target mode, the initiator has asserted SATN/. See the Disable Halt on Parity Error or ATN Condition bit in the SCNTL1 register for more information on when this status is actually raised.

Bit 6 CMP (Function Complete)
Full arbitration and selection sequence has completed.

Bit 5 SEL (Selected)
The NCR 53C810 has been selected by a SCSI target device. The Enable Response to Selection bit in the SCID register must be set for this to occur.

Bit 4 RSL (Reselected)
The NCR 53C810 has been reselected by a SCSI initiator device. The Enable Response to Reselection bit in the SCID register must be set for this to occur.

Bit 3 SGE (SCSI Gross Error)
The following conditions are considered SCSI Gross Errors:

1) Data underflow - the SCSI FIFO was read when no data was present.
2) Data overflow - the SCSI FIFO was written to while full.
3) Offset underflow - in target mode, an ACK pulse was received before the corresponding REQ was sent.
4) Offset overflow - in initiator mode, a REQ pulse was received which caused the maximum offset (Defined by the MO3-0 bits in the SXFER register) to be exceeded.
5) In initiator mode, a phase change occurred with an outstanding SREQ/SACK offset.
6) Residual data in SCSI FIFO - a transfer other than synchronous data receive was started with data left in the SCSI synchronous receive FIFO.

Bit 2 UDC (Unexpected Disconnect)
This condition only occurs in initiator mode. It happens when the target to which the NCR 53C810 is connected disconnects from the SCSI bus unexpectedly. See the SCSI Disconnect Unexpected bit in the SCNTL2 register for more information on expected versus unexpected disconnects. Any disconnect in low level mode causes this condition.

Bit 1 RST (SCSI Reset Condition)
The SRST/ signal has been asserted by the NCR 53C810 or any other SCSI device. Note that this condition is edge-triggered so that multiple interrupts cannot occur because of a single SRST/ pulse.

Bit 0 PAR (SCSI Parity Error)
The NCR 53C810 detected a parity error while receiving or sending SCSI data. See the Disable Halt on Parity Error or ATN Condition bits in the SCNTL1 register for more information on when this condition will actually be raised.

Register 41 (C1)
SCSI Interrupt Enable One
(SIEN1)
Read/Write

RESERVED					STO	GEN	HTH
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	0	0	0

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the SIST1 register. An interrupt is masked by clearing the appropriate mask bit. See Chapter 2, "Functional Description," for a detailed explanation of interrupts.

Bits 7-3 Reserved

Bit 2 STO (Selection or Reselection Time-out)
The SCSI device which the NCR 53C810 was attempting to select or reselect did not respond within the programmed time-out period. See the description of the STIME0 register bits 3-0 for more information on the time-out timer.

Bit 1 GEN (General Purpose Timer Expired)
The general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the STIME1 register, bits 3-0, for more information on the general purpose timer.

Bit 0 HTH (Handshake to Handshake timer Expired)
The handshake-to-handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the STIME0 register, bits 7-4, for more information on the handshake-to-handshake timer.

Register 42 (C2)
SCSI Interrupt Status Zero
(SIST0)
Read Only

M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Reading the SIST0 register returns the status of the various interrupt conditions, whether they are enabled in the SIEN0 register or not. Each bit set indicates that the corresponding condition has occurred. Reading the SIST0 will clear the interrupt status.

Reading this register will clear any bits that are set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the NCR 53C810 stacks interrupts). SCSI interrupt conditions may be individually masked through the SIEN0 register.

When performing consecutive 8-bit reads of the DSTAT, SIST0, and SIST1 registers (in any order), insert a delay equivalent to 12 CLK periods between the reads to ensure the interrupts clear properly. Also, if reading the registers when both the ISTAT SIP and DIP bits may not be set, the SIST0 and SIST1 registers should be read before the DSTAT register to avoid missing a SCSI interrupt.

Bit 7 M/A (Initiator Mode: Phase Mismatch; Target Mode: SATN/ Active)
In initiator mode, this bit is set if the SCSI phase asserted by the target does not match the instruction. The phase is sampled when SREQ/ is asserted by the target. In target mode, this bit is set when the SATN/ signal is asserted by the initiator.

Bit 6 CMP (Function Complete)
This bit is set when an arbitration only or full arbitration sequence has completed.

Bit 5 SEL (Selected)
This bit is set when the NCR 53C810 is selected by another SCSI device. The Enable Response to Selection bit must have been set in the SCID register (and the RESPID register must hold the chip's ID) for the NCR 53C810 to respond to selection attempts.

Bit 4 RSL (Reselected)
This bit is set when the NCR 53C810 is reselected by another SCSI device. The Enable Response to Reselection bit must have been set in the SCID register (and the RESPID register must hold the chip's ID) for the NCR 53C810 to respond to reselection attempts.

Bit 3 SGE (SCSI Gross Error)
This bit is set when the NCR 53C810 encounters a SCSI Gross Error Condition. The following conditions can result in a SCSI Gross Error Condition:

1) Data Underflow - the SCSI FIFO register was read when no data was present.
2) Data Overflow - too many bytes were written to the SCSI FIFO or the synchronous offset caused the SCSI FIFO to be overwritten.
3) Offset Underflow - the NCR 53C810 is operating in target mode and a SACK/ pulse is received when the outstanding offset is zero.
4) Offset Overflow - the other SCSI device sent a SREQ/ or SACK/ pulse with data which exceeded the maximum synchronous offset defined by the SXFER register.
5) A phase change occurred with an outstanding synchronous offset when the NCR 53C810 was operating as an initiator.
6) Residual data in the Synchronous data FIFO - a transfer other than synchronous data receive was started with data left in the synchronous data FIFO.

Bit 2 UDC (Unexpected Disconnect)
This bit is set when the NCR 53C810 is operating in initiator mode and the target device unexpectedly disconnects from the SCSI bus. This bit is only valid when the NCR 53C810 operates in the initiator mode. When the NCR 53C810 operates in low level mode, any disconnect will cause an interrupt, even a valid SCSI disconnect. This bit will also be set if a selection time-out occurs (it may occur before, at the same time, or stacked after the STO interrupt, since this is not considered an expected disconnect).

Bit 1 RST (SCSI RST/ Received)
This bit is set when the NCR 53C810 detects an active SRST/ signal, whether the reset was generated external to the chip or caused by the Assert SRST/ bit in the SCNTL1 register. This NCR 53C810 SCSI reset detection logic is edge-sensitive, so that multiple interrupts will not be generated for a single assertion of the SRST/ signal.

Bit 0 PAR (Parity Error)
This bit is set when the NCR 53C810 detects a parity error while receiving or sending SCSI data. The Enable Parity Checking bit (bit 3 in the SCNTL0 register) must be set for this bit to become active. A parity error can occur when receiving data from the SCSI bus or when receiving data from the host bus. From the host bus, parity is checked as it is transferred from the DMA FIFO to the SODL register.

A parity error can occur from the host bus only if Pass Through parity is enabled (bit 3 in the SCNTL0 register = 1, bit 2 in the SCNTL0 register = 0).

Register 43 (C3)
SCSI Interrupt Status One (SIST1)
Read Only

RESERVED					STO	GEN	HTH
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	0	0	0

Reading the SIST1 register returns the status of the various interrupt conditions, whether they are enabled in the SIEN1 register or not. Each bit that is set indicates the corresponding condition has occurred.

Reading the SIST1 will clear the interrupt condition.

Bits 7-3 Reserved

Bit 2 STO (Selection or Reselection Time-out)
The SCSI device which the NCR 53C810 was attempting to select or reselect did not respond within the programmed time-out period. See the description of the STIME0 register, bits 3-0, for more information on the time-out timer.

Bit 1 GEN (General Purpose Timer Expired)
The general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the STIME1 register, bits 3-0, for more information on the general purpose timer.

Bit 0 HTH (Handshake-to-Handshake Timer Expired)
The handshake-to-handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the STIME0 register, bits 7-4, for more information on the handshake-to-handshake timer.

Register 44 (C4)
SCSI Longitudinal Parity (SLPAR)
Read/Write

This register performs a bytewise longitudinal parity check on all SCSI data received or sent through the SCSI core. If one of the bytes received or sent (usually the last) is the set of correct even parity bits, SLPAR should go to zero (assuming it started at zero). As an example, suppose that the following three data bytes and one check byte are received from the SCSI bus (all signals are shown active high):

Data Bytes	Running SLPAR
—	00000000
1. 11001100	11001100 (XOR of word 1)
2. 01010101	10011001 (XOR of word 1 and 2)
3. 00001111	10010110 (XOR of word 1, 2 and 3)
	Even Parity >>>10010110
4. 10010110	00000000

A one in any bit position of the final SLPAR value would indicate a transmission error.

The SLPAR register can also be used to generate the check bytes for SCSI send operations. If the SLPAR register contains all zeros prior to sending a block move, it will contain the appropriate check byte at the end of the block move. This byte must then be sent across the SCSI bus.

Note: Writing any value to this register resets it to zero.

The longitudinal parity checks are meant to provide an added measure of SCSI data integrity and are entirely optional. This register does not latch SCSI selection/reselection IDs under any circumstances. The default value of this register is zero.

Register 46 (C6)
Memory Access Control (MACNTL)
Read/Write

TYP3	TYP2	TYP1	TYP0	DWR	DRD	PSCPT	SCPTS
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bits 7-4 TYP3-0 (Chip Type)
These bits identify the chip type for software purposes. This data manual applies to devices that have these bits set to 00h.

Bits 3-0 of this register are used to determine if an external bus master access is to local or far memory. When bits 3 through 0 are set, the corresponding access is considered local. When these bits are clear, the corresponding access is to far memory.

Bit 3 DWR (DataWR)
This bit is used to define if a data write is considered local memory access.

Bit 2 DRD (DataRD)
This bit is used to define if a data read is considered local memory access.

Bit 1 PSCPT (Pointer SCRIPTS)
This bit is used to define if a pointer to a SCRIPTS direct or table indirect fetch is considered local memory access.

Bit 0 SCPTS (SCRIPTS)
This bit is used to define if a SCRIPTS fetch is considered local memory access.

Register 47 (C7)
General Purpose Pin Control (GPCNTL)
Read/Write

ME	FE	RESERVED				GPIO1	GPIO0
7	6	5	4	3	2	1	0
Default>>>							
0	0	X	X	X	X	1	1

This register is used to determine if the pins controlled by the General Purpose register (GPREG) are inputs or outputs. Bits 1-0 in GPCNTL correspond to bits in the GPREG register. When the bits are enabled as inputs, an internal pull-up is also enabled.

Bit 7 Master Enable
The internal bus master signal will be presented on GPIO1 if this bit is set, regardless of the state of Bit 1 (GPIO1_EN).

Bit 6 Fetch Enable
The internal Op code Fetch signal will be presented on GPIO0 if this bit is set, regardless of the state of Bit 0 (GPIO0_EN).

Bits 5-2 Reserved

Bit 1 GPIO1_EN (GPIO1 Enable)
This bit powers up set, causing the GPIO1 to become an input. Resetting this bit causes GPIO1 to become an output.

Bit 0 GPIO0_EN (GPIO0 Enable)
This bit powers up set, causing the GPIO0 to become an input. Resetting this bit causes GPIO0 to become an output.

Register 48 (C8)
SCSI Timer Register Zero (STIME0)
Read /Write

	HTH					SEL		
	7	6	5	4	3	2	1	0
Default>>>	0	0	0	0	0	0	0	0

Bits 7-4 HTH (Handshake-to-Handshake Timer Period)
These bits select Handshake-to-Handshake time-out Period, the maximum time between SCSI handshakes (SREQ/ to SREQ/ in target mode, or SACK/ to SACK/ in initiator mode). When this timing is exceeded, the HTH bit in the SIST1 register is set. The following table contains time-out periods for the Handshake-to-Handshake Timer, the Selection/Reselection Timer (bits 3-0), and the General Purpose Timer (STIME1 bits 3-0).

HTH 7-4, SEL 3-0, GEN 3-0	Minimum Time-out
0000	Disabled
0001	100 µs
0010	200 µs
0011	400 µs
0100	800 µs
0101	1.6 ms
0110	3.2 ms
0111	6.4 ms
1000	12.8 ms
1001	25.6 ms
1010	51.2 ms
1011	102.4 ms
1100	204.8 ms
1101	409.6 ms
1110	819.2 ms
1111	1.6+ sec

Bits 3-0 SEL (Selection Time-Out)
These bits select the SCSI selection/reselection time-out period. When this timing (plus the 200 µs selection abort time) is exceeded, the STO bit in the SIST1 register is set. An interrupt is optionally generated, if bit 2 in the SIEN1 register is set. See Chapter 2, "Functional Description," for an explanation of how interrupts are generated when the timers expire.

Register 49 (C9)
SCSI Timer Register One
(STIME1)
Read/Write

	RESERVED			GEN3	GEN2	GEN1	GEN0
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	0	0	0	0

Bits 7-4 Reserved

Bits 3-0 GEN3-0 (General Purpose Timer Period)

These bits select the period of the general purpose timer. The time measured is the time between enabling and disabling of the timer. When this timing is exceeded, the GEN bit in the SIST1 register is set . Refer to the table under STIME0, bits 3-0, for the available time-out periods. See Chapter 2, "Functional Description," for an explanation of how interrupts are generated when the timers expire.

Note: to reset a timer before it has expired and obtain repeatable delays, the time value must be written to zero first, and then written back to the desired value. This is also required when changing from one time value to another.

Register 4A (CA)
Response ID (RESPID)
Read/Write

ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

This register contains the selection or reselection IDs. This register contains the ID that the chip responds to on the SCSI bus. Each bit represents one possible ID with the most significant bit representing ID 7 and the least significant bit representing ID0. The NCR 53C810 can respond to more than one ID because more than one bit can be set in the RESPID register. However, the NCR 53C810 will arbitrate with only the ID value in the SCID register.

Register 4C (CC)
SCSI Test Register Zero (STEST0)
Read Only

	RESERVED			SLT	ART	SOZ	SOM
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	0	X	1	1

Bits 7-4 Reserved

Bit 3 SLT (Selection Response Logic Test)
This bit is asserted when the NCR 53C810 is ready to be selected or reselected. This does not take into account the bus settle delay of 400 ns. This bit is used for functional test and fault purposes.

Bit 2 ART (Arbitration Priority Encoder Test)
This bit will always be asserted when the NCR 53C810 exhibits the highest priority ID asserted on the SCSI bus during arbitration. It is primarily used for chip level testing, but it may be used during low level mode operation to determine if the NCR 53C810 has won arbitration.

Bit 1 SOZ (SCSI Synchronous Offset Zero)
This bit indicates that the current synchronous SREQ/SACK offset is zero. This bit is not latched and may change at any time. It is used in low level synchronous SCSI operations. When this bit is set, the NCR 53C810, as an initiator, is waiting for the target to request data transfers. If the NCR 53C810 is a target, then the initiator has sent the offset number of acknowledges.

Bit 0 SOM (SCSI Synchronous Offset Maximum)
This bit indicates that the current synchronous SREQ/ACK offset is the maximum specified by bits 3-0 in the SCSI Transfer register. This bit is not latched and may change at any time. It is used in low level synchronous SCSI operations. When this bit is set, the NCR 53C810, as a target, is waiting for the initiator to acknowledge the data transfers. If the NCR 53C810 is an initiator, then the target has sent the offset number of requests.

Register 4D (CD)
SCSI Test Register One (STEST1)
Read Only

SCLK	RESERVED						
7	6	5	4	3	2	1	0
Default>>>							
0	X	X	X	X	X	X	X

Bit 7 SCLK
This bit, when set, will disable the external SCLK (SCSI Clock) pin, and the chip will use the DMA clock as the internal SCSI clock. If a transfer rate of 10 MB/s is to be achieved on the SCSI bus, this bit must be reset and at least a 40 MHz external SCLK must be provided.

Bits 6-0 Reserved

Register 4E (CE)
SCSI Test Register Two (STEST2)
Read/Write

SCE	ROF	RES	SLB	SZM	RES	EXT	LOW
7	6	5	4	3	2	1	0
Default>>>							
0	0	X	0	0	0	0	0

Bit 7 SCE (SCSI Control Enable)
This bit, when set, allows all SCSI control and data lines to be asserted through the SOCL and SODL registers regardless of whether the NCR 53C810 is configured as a target or initiator.

Note: This bit should not be set during normal operation, since it could cause contention on the SCSI bus. It is included for diagnostic purposes only.

Bit 6 ROF (Reset SCSI Offset)
Setting this bit clears any outstanding synchronous SREQ/SACK offset. This bit should be set if a SCSI gross error condition occurs, to clear the offset when a synchronous transfer does not complete successfully. The bit automatically clears itself after resetting the synchronous offset.

Bit 5 Reserved

Bit 4 SLB (SCSI Loopback Mode)
Setting this bit allows the NCR 53C810 to perform SCSI loopback diagnostics. That is, it enables the SCSI core to simultaneously perform as both initiator and target.

Bit 3 SZM (SCSI High-Impedance Mode)
Setting this bit places all the open-drain 48 mA SCSI drivers into a high-impedance state. This is to allow internal loopback mode operation without affecting the SCSI bus.

Bit 2 Reserved

Bit 1 EXT (Extend SREQ/SACK Filtering)
NCR TolerANT SCSI receiver technology includes a special digital filter on the SREQ/ and SACK/ pins which will cause glitches on

deasserting edges to be disregarded. Setting this bit will increase the filtering period from 30ns to 60ns on the deasserting edge of the SREQ/ and SACK/ signals.

Note: This bit must never be set during fast SCSI (greater than 5M transfers per second) operations, because a valid assertion could be treated as a glitch.

Bit 0 LOW (SCSI Low level Mode)
Setting this bit places the NCR 53C810 in low level mode. In this mode, no DMA operations occur, and no SCRIPTS execute. Arbitration and selection may be performed by setting the start sequence bit as described in the SCNTL0 register. SCSI bus transfers are performed by manually asserting and polling SCSI signals. Clearing this bit allows instructions to be executed in SCSI SCRIPTS mode.

Note: It is not necessary to set this bit for access to the SCSI bit-level registers (SODL, SBCL, and input registers)

Register 4F (CF)
SCSI Test Register Three
(STEST3)
Read/Write

TE	STR	HSC	DSI	RES	TTM	CSF	STW
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	X	0	0	0

Bit 7 TE (TolerANT Enable)
Setting this bit enables the active negation portion of NCR TolerANT technology. Active negation causes the SCSI Request, Acknowledge, Data, and Parity signals to be actively deasserted, instead of relying on external pull-ups, when the NCR 53C810 is driving these signals. Active deassertion of these signals will occur only when the NCR 53C810 is in an information transfer phase. When operating in a differential environment or at fast SCSI timings, TolerANT Active negation should be enabled to improve setup and deassertion times. Active negation is disabled after reset or when this bit is cleared. For more information on NCR TolerANT technology, refer to Chapter One, "Introduction."

Bit 6 STR (SCSI FIFO Test Read)
Setting this bit places the SCSI core into a test mode in which the SCSI FIFO can be easily read. Reading the SODL register will cause the FIFO to unload.

Bit 5 HSC (Halt SCSI Clock)
Asserting this bit causes the internal divided SCSI clock to come to a stop in a glitchless manner. This bit may be used for test purposes or to lower I_{DD} during a power down mode.

Bit 4 DSI (Disable Single Initiator Response)
If this bit is set, the NCR 53C810 will ignore all bus-initiated selection attempts that employ the single-initiator option from SCSI-1. In order to select the NCR 53C810 while this bit is set, the NCR 53C810's SCSI ID and

the initiator's SCSI ID must both be asserted. This bit should be asserted in SCSI-2 systems so that a single bit error on the SCSI bus will not be interpreted as a single initiator response.

Bit 3 Reserved

Bit 2 TTM (Timer Test Mode)
Asserting this bit facilitates testing of the selection time-out, general purpose, and handshake-to-handshake timers by greatly reducing all three time-out periods. Setting this bit starts all three timers and if the respective bits in the SIEN1 register are asserted, the NCR 53C810 will generate interrupts at time-out. This bit is intended for internal manufacturing diagnosis and should not be used.

Bit 1 CSF (Clear SCSI FIFO)
Setting this bit will cause the "full flags" for the SCSI FIFO to be cleared. This empties the FIFO. This bit is self-resetting. In addition to the SCSI FIFO pointers, the SIDL, SODL, and SODR full bits in the SSTAT0 and SSTAT2 are cleared.

Bit 0 STW (SCSI FIFO Test Write)
Setting this bit places the SCSI core FIFO into a test mode in which the SCSI FIFO can easily be written. While this bit is set, writes to the SODL register will cause the byte contained in this register to be loaded into the FIFO.

Register 50 (D0)
SCSI Input Data Latch (SIDL)
Read Only

This register is used primarily for diagnostic testing, programmed I/O operation or error recovery. Data received from the SCSI bus can be read from this register. Data can be written to the SODL register and then read back into the NCR 53C810 by reading this register to allow loopback testing. When receiving SCSI data, the data will flow into this register and out to the host FIFO. This register differs from the SBDL register; SIDL contains latched data and the SBDL always contains exactly what is currently on the SCSI data bus. Reading this register causes the SCSI parity bit to be checked, and will cause a parity error interrupt if the data is not valid. The power-up values are indeterminate.

Register 54 (D4)
SCSI Output Data Latch (SODL)
Read/Write

This register is used primarily for diagnostic testing or programmed I/O operation. Data written to this register is asserted onto the SCSI data bus by setting the Assert Data Bus bit in the SCNTL1 register. This register is used to send data via programmed I/O. Data flows through this register when sending data in any mode. It is also used to write to the synchronous data FIFO when testing the chip. The power-up value of this register is indeterminate.

Registers 58 (D8)
SCSI Bus Data Lines (SBDL)
Read Only

This register contains the SCSI data bus status. Even though the SCSI data bus is active low, these bits are active high. The signal status is not latched and is a true representation of exactly what is on the data bus at the time the register is read. This register is used when receiving data via programmed I/O. This register can also be used for diagnostic testing or in low level mode. The power-up value of this register is indeterminate.

Registers 5C-5F (DC-DF) Scratch Register B (SCRATCHB) (Read/Write)

This is a general purpose user definable scratch pad register. Apart from CPU access, only Register Read/Write and Memory Moves directed at the SCRATCH register will alter its contents. The power-up values are indeterminate.

Chapter Six

Instruction Set of the I/O Processor

SCSI SCRIPTS

After power up and initialization of the NCR 53C810, the chip may be operated in one of two modes:

1) Low level register interface; or

2) SCSI SCRIPTS mode.

In the low level register interface, the user has access to the DMA control logic and the SCSI bus control logic. The chip may be operated much like an NCR 53C80. An external processor has access to the SCSI bus signals and the low level DMA signals, which allows creation of complicated board level test algorithms. The low level interface is useful for backward compatibility with SCSI devices that require certain unique timings or bus sequences to operate properly. Another feature allowed at the low level is loopback testing. In loopback mode, the SCSI core can be directed to talk to the DMA core to test internal data paths all the way out to the chip's pins.

To operate in the SCSI SCRIPTS mode, the NCR 53C810 requires only a SCRIPTS start address. The start address must be at a longword (4 byte) boundary, which will align all the following SCRIPTS at a longword boundary since all SCRIPTS are 8 or 12 bytes long. All commands are fetched from external memory. The NCR 53C810 fetches and executes its own instructions by becoming a bus master on the host bus and fetching two or three 32-bit words into its registers. Commands are fetched until an interrupt command is encountered, or until an unexpected event (such as a hardware error) causes an interrupt to the external processor.

Once an interrupt is generated, the NCR 53C810 halts all operations until the interrupt is serviced. Then, the start address of the next SCRIPTS instruction may be written to the DMA SCRIPTS Pointer register to restart the automatic fetching and execution of instructions.

The SCSI SCRIPTS mode of execution allows the NCR 53C810 to make decisions based on the status of the SCSI bus, which off-loads the microprocessor from servicing the numerous interrupts inherent in I/O operations.

Given the rich set of SCSI-oriented features included in the command set, and the ability to re-enter the SCSI algorithm at any point, this high level interface is all that is required for both normal and exception conditions. Therefore, switching to low level mode for error recovery should never be required.

Four types of SCRIPTS instructions are implemented in the NCR 53C810:

- Block Move - used to move data between the SCSI bus and memory
- I/O or Read/Write - causes the NCR 53C810 to trigger common SCSI h/w sequences, or to move registers
- Transfer Control
- Memory Move

Each instruction consists of two or three 32-bit words. The first 32-bit word is always loaded into the DCMD and DBC registers, the second into the DSPS register. The third word, used only by Memory Move instructions, is loaded into the TEMP shadow register. In an indirect I/O or Move instruction, the first two 32-bit op code fetches will be followed by one or two more 32-bit fetch cycles. These cycles are executed with a separate bus ownership request.

Sample Operation

The following example describes execution of a SCRIPTS instruction. This sample operation is for a Block Move instruction.

1) The host CPU, through programmed I/O, gives the DMA SCRIPTS Pointer (DSP) register (in the Operating Register file) the starting address in main memory that points to a SCSI SCRIPTS program for execution.

2) Loading the DSP register causes the NCR 53C810 to request use of the PCI bus to fetch its first instruction from main memory at the address just loaded.

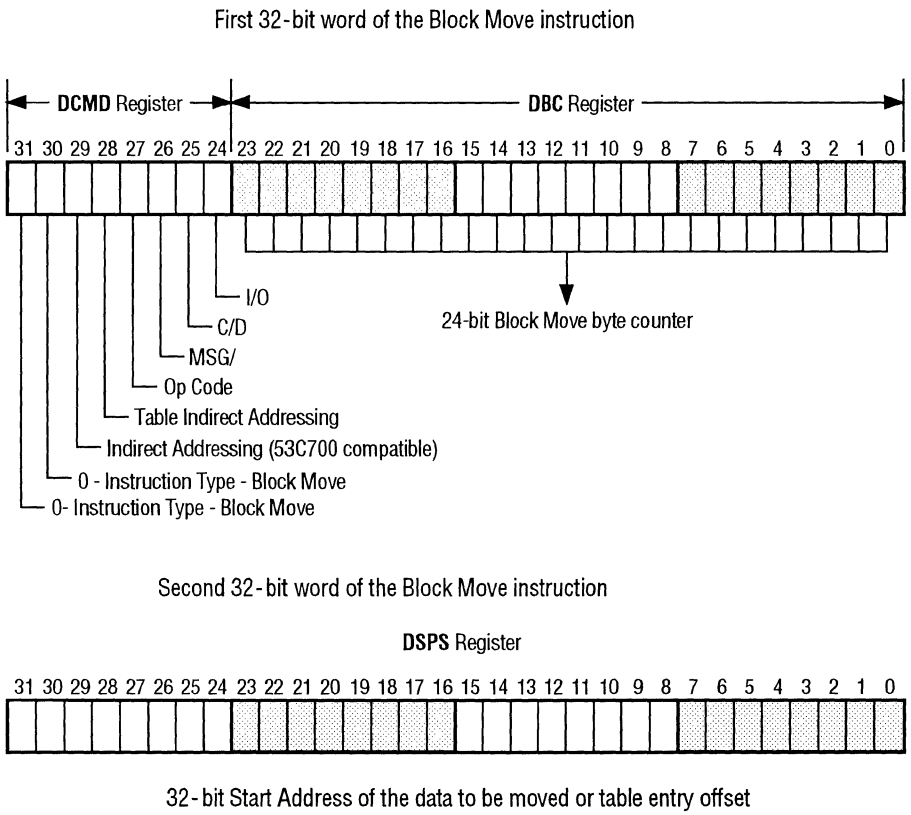
3) When the NCR 53C810 is granted the PCI bus, it typically fetches two longwords (64 bits), releases the PCI bus, and decodes the high order byte of the first longword as a SCRIPTS instruction. If the instruction is a Block Move, the lower three bytes of the first longword are stored and interpreted as the number of bytes to be moved. The second longword is stored and interpreted as the 32-bit beginning address in main memory to which the move is directed.

4) For a SCSI send operation, the NCR 53C810 waits until there is enough space in the DMA FIFO to transfer a programmable size block of data. For a SCSI receive operation, it waits until enough data is collected in the DMA FIFO for transfer to memory. At this point, the NCR 53C810 requests use of the PCI bus again, this time for data transfers.

5) When the NCR 53C810 is again granted the PCI bus, it will execute (as a bus master) a burst transfer (programmable size) of data, decrement the internally stored remaining byte count, increment the address pointer, and then release the PCI bus. The NCR 53C810 stays off the PCI bus until the FIFO can again hold (for a write) or has collected (for a read) enough data to repeat the process.

The process repeats until the internally stored byte count has reached zero. The NCR 53C810 releases the PCI bus and then requests use of the PCI bus again for another SCRIPTS instruction fetch cycle, using the incremented stored address maintained in the DMA SCRIPTS Pointer register. Execution of SCRIPTS instructions continues until an error condition occurs or an interrupt SCRIPTS instruction is received. At this point, the NCR 53C810 interrupts the host CPU and waits for further servicing by the host system. It can execute independent Block Move instructions specifying new byte counts and starting locations in main memory. In this manner, the NCR 53C810 performs scatter/gather operations on data without requiring help from the host program, generating a host interrupt, or requiring an external DMA controller to be programmed.

Figure 6-1. Block Move Instruction Register



Block Move Instructions

For Block Move commands, bits 5 and 4 (SIOM and DIOM) in the DMODE register determine whether the source/destination address resides in memory or I/O space. When data is being moved onto the SCSI bus, SIOM controls whether that data comes from I/O or memory space. When data is being moved off of the SCSI bus, DIOM controls whether that data goes to I/O or memory space.

Bits 31-30 Instruction Type-Block Move

Bit 29 Indirect Addressing

When this bit is cleared, user data is moved to or from the 32-bit data start address for the Block Move instruction. The value is loaded into the chip's address register and incremented as data is transferred.

When set, the 32-bit user data start address for the Block Move is the address of a pointer to the actual data buffer address. The value at the 32-bit start address is loaded into the chip's DNAD register via a third longword fetch (4-byte transfer across the host computer bus).

Direct: The byte count and absolute address are as follows:

Command	Byte Count
Address of Data	

Indirect: Use the fetched byte count, but fetch the data address from the address in the command.

Command	Byte Count
Address of Pointer to Data	

Once the data pointer address is loaded, it is executed as when the chip operates in the direct mode. This indirect feature allows a table of data buffer addresses to be specified. Using the NCR SCSI SCRIPTS compiler, the table offset is placed in the script at compile time. Then at the actual data transfer time, the offsets are added to the base address of the data address table by the external processor. The logical I/O driver builds a structure of addresses for an I/O rather than treating each address individually. This feature makes it possible to locate SCSI SCRIPTS in a PROM.

Bit 28 Table Indirect

When this bit is set, the 24-bit signed value in the start address of the move is treated as a relative displacement from the value in the DSA register. Both the transfer count and the source/destination address are fetched from this address.

Table Indirect: Use the signed integer offset in bits 23-0 of the second four bytes of the instruction, added to the value in the DSA register, to fetch first the byte count and then the data address. The signed value is combined with the data structure base address to generate the physical address used to fetch values from the data structure. Sign-extended values of all ones for negative values are allowed, but bits 31-24 are ignored.

Command	Not Used
Don't Care	Table Offset

Prior to the start of an I/O, the Data Structure Base Address register (DSA) should be loaded with the base address of the I/O data structure. The address may be any address on a long word boundary.

After a Table Indirect op code is fetched, the DSA is added to the 24-bit signed offset value from the op code to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from that address brings the data values into the chip.

For a MOVE command, the 24-bit byte count is fetched from system memory. Then the 32-bit physical address is brought into the NCR 53C810. Execution of the move begins at this point.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and may cross system segment boundaries.

There are two restrictions on the placement of pointer data in system memory: the eight bytes of data in the MOVE command must be contiguous, as shown below; and indirect data fetches are not available during execution of a Memory-to-Memory DMA operation.

(00)	Byte Count
Physical Data Address	

Bit 27 Op Code

This 1-bit field defines the instruction to be executed as a block move (MOVE).

Target Mode

OPC	Instruction Defined
0	MOVE
1	Reserved

1) The NCR 53C810 verifies that it is connected to the SCSI bus as a target before executing this instruction.
2) The NCR 53C810 asserts the SCSI phase signals (SMSG/, SC_D/, & SI_O/) as defined by the Phase Field bits in the instruction.
3) If the instruction is for the command phase, the NCR 53C810 receives the first command byte and decodes its SCSI Group Code.
   a) If the SCSI Group Code is either Group 0, Group 1, Group 2, or Group 5, then the NCR 53C810 overwrites the DBC register with the length of the Command Descriptor Block: 6, 10, or 12 bytes.
   b) If any other Group Code is received, the DBC register is not modified and the NCR 53C810 will request the number of bytes specified in the DBC register. If the DBC register contains 000000h, an illegal instruction interrupt is generated.
4) The NCR 53C810 transfers the number of bytes specified in the DBC register starting at the address specified in the DNAD register.
5) If the SATN/ signal is asserted by the initiator or a parity error occurred during the transfer, the transfer can optionally be halted and an interrupt generated. The Disable Halt on Parity Error or ATN bit in the SCNTL1 register controls whether an interrupt will be generated.

Initiator Mode

OPC	Instruction Defined
0	Reserved
1	MOVE

1) The NCR 53C810 verifies that it is connected to the SCSI bus as an initiator before executing this instruction.
2) The NCR 53C810 waits for an unserviced phase to occur. An unserviced phase is defined as any phase (with SREQ/ asserted) for which the NCR 53C810 has not yet transferred data by responding with an SACK/

3) The NCR 53C810 compares the SCSI phase bits in the DCMD register with the latched SCSI phase lines stored in the SSTAT1 register. These phase lines are latched when SREQ/ is asserted.

4) If the SCSI phase bits match the value stored in the SSTAT1 register, the NCR 53C810 will transfer the number of bytes specified in the DBC register starting at the address pointed to by the DNAD register.

5) If the SCSI phase bits do not match the value stored in the SSTAT1 register, the NCR 53C810 generates a phase mismatch interrupt and the command is not executed.

Bits 26-24 SCSI Phase

This 3-bit field defines the desired SCSI information transfer phase. When the NCR 53C810 operates in initiator mode, these bits are compared with the latched SCSI phase bits in the SSTAT1 register. When the NCR 53C810 operates in target mode, the NCR 53C810 asserts the phase defined in this field. The following table describes the possible combinations and the corresponding SCSI phase.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data out
0	0	1	Data in
0	1	0	Command
0	1	1	Status
1	0	0	Reserved out
1	0	1	Reserved in
1	1	0	Message out
1	1	1	Message in

Bits 23-0 Transfer Counter

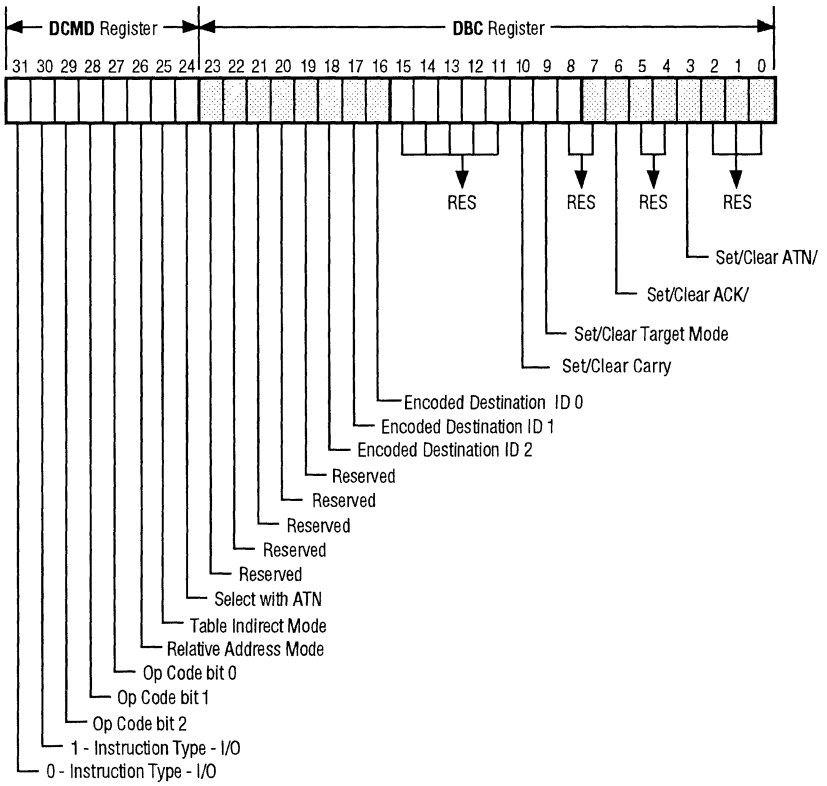
This 24-bit field specifies the number of data bytes to be moved between the NCR 53C810 and system memory. The field is stored in the DBC register. When the NCR 53C810 transfers data to/from memory, the DBC register is decremented by the number of bytes transferred. In addition, the DNAD register is incremented by the number of bytes transferred. This process is repeated until the DBC register has been decremented to zero. At that time, the NCR 53C810 fetches the next instruction.

Bits 31-0 Start Address

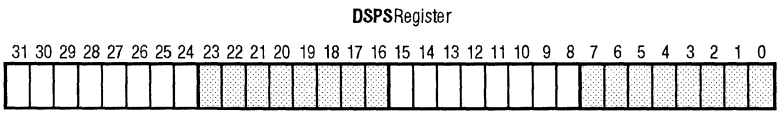
This 32-bit field specifies the starting address of the data to be moved to/from memory. This field is copied to the DNAD register. When the NCR 53C810 transfers data to or from memory, the DNAD register is incremented by the number of bytes transferred.

Figure 6-2. I/O Instruction Register

First 32-bit word of the I/O instruction



Second 32-bit word of the I/O instruction



32-bit Jump Address

I/O Instructions

Bits 31-30 Instruction Type - I/O Instruction

Bits 29-27 Op Code

The following Op Code bits have different meanings, depending on whether the NCR 53C810 is operating in initiator or target mode. **Note:** Op Code selections 101-111 are considered Read/Write instructions, and are described in that section.

Target Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Reselect
0	0	1	Disconnect
0	1	0	Wait Select
0	1	1	Set
1	0	0	Clear

Reselect Instruction

1) The NCR 53C810 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCID register. If the NCR 53C810 loses arbitration, then it tries again during the next available arbitration cycle without reporting any lost arbitration status.

2) If the NCR 53C810 wins arbitration, it attempts to reselect the SCSI device whose ID is defined in the destination ID field of the instruction. Once the NCR 53C810 has won arbitration, it fetches the next instruction from the address pointed to by the DSP register. Therefore, the SCRIPTS can move on to the next instructions before the reselection has completed. It will continue executing SCRIPTS until a SCRIPT that requires a response from the initiator is encountered.

3) If the NCR 53C810 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The NCR 53C810 should manually be set to initiator mode if it is reselected, or to target mode if it is selected.

Disconnect Instruction

The NCR 53C810 disconnects from the SCSI bus by deasserting all SCSI signal outputs.

Wait Select Instruction

1) If the NCR 53C810 is selected, it fetches the next instruction from the address pointed to by the DSP register.

2) If reselected, the NCR 53C810 fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The NCR 53C810 should manually be set to initiator mode when reselected.

3) If the CPU sets the SIGP bit in the ISTAT register, the NCR 53C810 will abort the Wait Select instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register.

Set Instruction

When the SACK/ or SATN/ bits are set, the corresponding bits in the SOCL register are set. SACK/ or SATN/ should not be set except for testing purposes. When the target bit is set, the corresponding bit in the SCNTL0 register is also set. When the carry bit is set, the corresponding bit in the Arithmetic Logic Unit (ALU) is set.

Note: None of the signals are set on the SCSI bus in target mode.

Clear Instruction

When the SACK/ or SATN/ bits are set, the corresponding bits are cleared in the SOCL register. SACK/ or SATN/ should not be set except for testing purposes. When the target bit is cleared, the corresponding bit in the SCNTL0 register is cleared. When the carry bit is cleared, the corresponding bit in the ALU is cleared.

Note: None of the signals are reset on the SCSI bus in target mode.

Initiator Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Select
0	0	1	Wait Disconnect
0	1	0	Wait Reselect
0	1	1	Set
1	0	0	Clear

Select Instruction

1) The NCR 53C810 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCID register. If the NCR 53C810 loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.
2) If the NCR 53C810 wins arbitration, it attempts to select the SCSI device whose ID is defined in the destination ID field of the instruction. Once the NCR 53C810 has won arbitration, it fetches the next instruction from the address pointed to by the DSP register. Therefore, the SCRIPTS can move to the next instruction before the selection has completed. It will continue executing SCRIPTS until a SCRIPT that requires a response from the target is encountered.
3) If the NCR 53C810 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The NCR 53C810 should manually be set to initiator mode if it is reselected, or to target mode if it is selected.
4) If the Select with SATN/ field is set, the SATN/ signal is asserted during the selection phase.

Wait Disconnect Instruction

1) The NCR 53C810 waits for the target to perform a "legal" disconnect from the SCSI bus. A "legal" disconnect occurs when SBSY/ and SSEL/ are inactive for a minimum of one Bus Free delay (400 ns), after the NCR 53C810 has received a Disconnect Message or a Command Complete Message.

Wait Reselect Instruction

1) If the NCR 53C810 is selected before being reselected, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The NCR 53C810 should be manually set to target mode when selected.
2) If the NCR 53C810 is reselected, it fetches the next instruction from the address pointed to by the DSP register.
3) If the CPU sets the SIGP bit in the ISTAT register, the NCR 53C810 will abort the Wait Reselect instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register.

Set Instruction

When the SACK/ or SATN/ bits are set, the corresponding bits in the SOCL register are set. When the target bit is set, the corresponding bit in the SCNTL0 register is also set. When the carry bit is set, the corresponding bit in the ALU is set.

Clear Instruction

When the SACK/or SATN/ bits are set, the corresponding bits are cleared in the SOCL register. When the Target bit is cleared, the corresponding bit in the SCNTL0 register is cleared. When the carry bit is cleared, the corresponding bit in the ALU is cleared.

Bit 26 Relative Addressing Mode

When this bit is set, the 24-bit signed value in the DNAD register is used as a relative displacement from the current DSP address. This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. The Select and Reselect instructions can contain an absolute alternate jump address or a relative transfer address.

Bit 25 Table Indirect Mode

When this bit is set, the 24-bit signed value in the DBC register is added to the value in the DSA register, used as an offset relative to the value in the Data Structure Base Address (DSA) register. The SCNTL3 register value, SCSI ID, synchronous offset and synchronous period are loaded from this address. Prior to the start of an I/O, the DSA should be loaded with the base address of the I/O data structure. The address may be any address on a longword boundary. After a Table Indirect op code is fetched, the DSA is added to the 24-bit signed offset value from the op code to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from that address brings the data values into the chip.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and may cross system segment boundaries. There are two restrictions on the placement of data in system memory:

1) The I/O data structure must lie within the 8 MB above or below the base address.

2) An I/O command structure must have all four bytes contiguous in system memory, as shown below. The offset/period bits are ordered as in the SXFER register. The configuration bits are ordered as in the SCNTL3 register.

SCNTL3	ID	Offset/period	(00)

This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. Bits 25 and 26 may be set individually or in combination:

	Bit 25	Bit 26
Direct	0	0
Table Indirect	0	1
Relative	1	0
Table Relative	1	1

Direct – Uses the device ID and physical address in the command.

Command	ID	Not Used	Not Used
Absolute Alternate Address			

Table Indirect – Uses the physical jump address, but fetches data using the table indirect method.

Command	Table Offset
Absolute Alternate Address	

Relative – Uses the device ID in the command, but treats the alternate address as a relative jump

Command	ID	Not Used	Not Used
	Alternate Jump Offset		

Table Relative – Treats the alternate jump address as a relative jump and fetches the device ID, synchronous offset, and synchronous period indirectly. Adds the value in bits 23-0 of the first four bytes of the SCRIPTS instruction to the data structure base address to form the fetch address.

Command	Table Offset
	Alternate Jump Offset

Bit 24 Select with SATN/
This bit specifies whether SATN/ will be asserted during the selection phase when the NCR 53C810 is executing a Select instruction. When operating in initiator mode, set this bit for the Select instruction. If this bit is set on any other I/O instruction, an illegal instruction interrupt is generated.

Bit 23-19 Reserved

Bits 18-16 Encoded SCSI Destination ID
This 3-bit field specifies the destination SCSI ID for an I/O instruction.

Bit 10 Set/Clear Carry
This bit is used in conjunction with a Set or Clear command to set or clear the Carry bit. Setting this bit with a Set command asserts the Carry bit in the ALU. Clearing this bit with a Set command deasserts the Carry bit in the ALU.

Bit 9 Set/Clear Target Mode
This bit is used in conjunction with a Set or Clear command to set or clear target mode. Setting this bit with a Set command configures the NCR 53C810 as a target device (this sets bit 0 of the SCNTL0 register). Setting this bit with a Clear command configures the NCR 53C810 as an initiator device (this clears bit 0 of the SCNTL0 register).

Bit 6 Set/Clear SACK/

Bit 3 Set/Clear SATN/
These two bits are used in conjunction with a Set or Clear command to assert or deassert the corresponding SCSI control signal. Bit 6 controls the SCSI SACK/ signal; bit 3 controls the SCSI SATN/ signal.

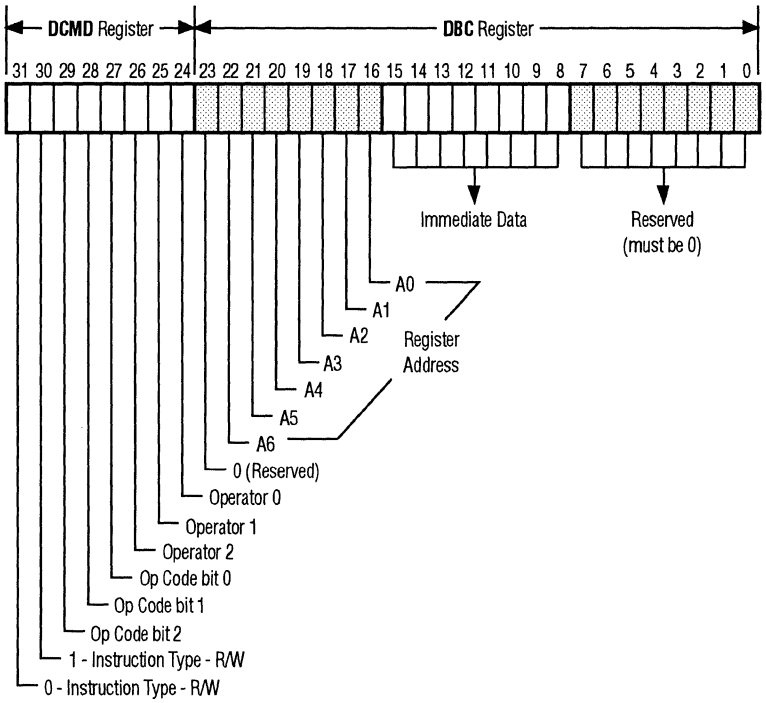
Setting either of these bits will set or reset the corresponding bit in the SOCL register, depending on the command used. The Set command is used to assert SACK/ and/or SATN/ on the SCSI bus. The Clear command is used to deassert SACK/ and/or SATN/ on the SCSI bus.

Since SACK/ and SATN/ are initiator signals, they will not be asserted on the SCSI bus unless the NCR 53C810 is operating as an initiator or the SCSI Loopback Enable bit is set in the STEST2 register.

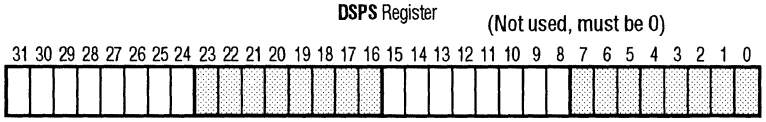
The Set/Clear SCSI ACK/ATN instruction would be used after message phase Block Move operations to give the initiator the opportunity to assert attention before acknowledging the last message byte. For example, if the initiator wishes to reject a message, an Assert SCSI ATN instruction would be issued before a Clear SCSI ACK instruction.

Figure 6-3. Read/Write Register Instruction

First 32-bit word of the Read/Write instruction



Second 32-bit word of the Read/Write instruction



Read/Write Instructions

Bits 31-30 Instruction Type - Read/Write Instruction
The Read/Write instruction uses operator bits 26 through 24 in conjunction with the op code bits to determine which instruction is currently selected.

Bits 29-27 Op Code
The combinations of these bits determine if the instruction is a Read/Write or an I/O instruction. Op Codes 000 through 100 are considered I/O instructions.

Bits 26-24 Operator
These bits are used in conjunction with the op code bits to determine which instruction is currently selected. Refer to table 6-1 for field definitions.

Bits 22-16 Register Address - A(6-0)
Register values may be changed from SCRIPTS in read-modify-write cycles or move to/from SFBR cycles. A(6-0) select an 8-bit source/destination register within the NCR 53C810.

Read-Modify-Write Cycles

During these cycles the register is read, the selected operation is performed, and the result is written back to the source register.

The Add operation can be used to increment or decrement register values (or memory values if used in conjunction with a Memory-to-Register Move operation) for use as loop counters.

Move to/from SFBR Cycles

All operations are read-modify-writes. However, two registers are involved, one of which is always the SFBR. The possible functions of this command are:

- Write one byte (value contained within the SCRIPTS instruction) into any chip register.
- Move to/from the SFBR from/to any other register.
- Alter the value of a register with AND/OR/ ADD operators.
- After moving values to the SFBR, the compare and jump, call, or similar commands may be used to check the value.
- A Move-to-SFBR followed by a Move-from-SFBR can be used to perform a register to register move.

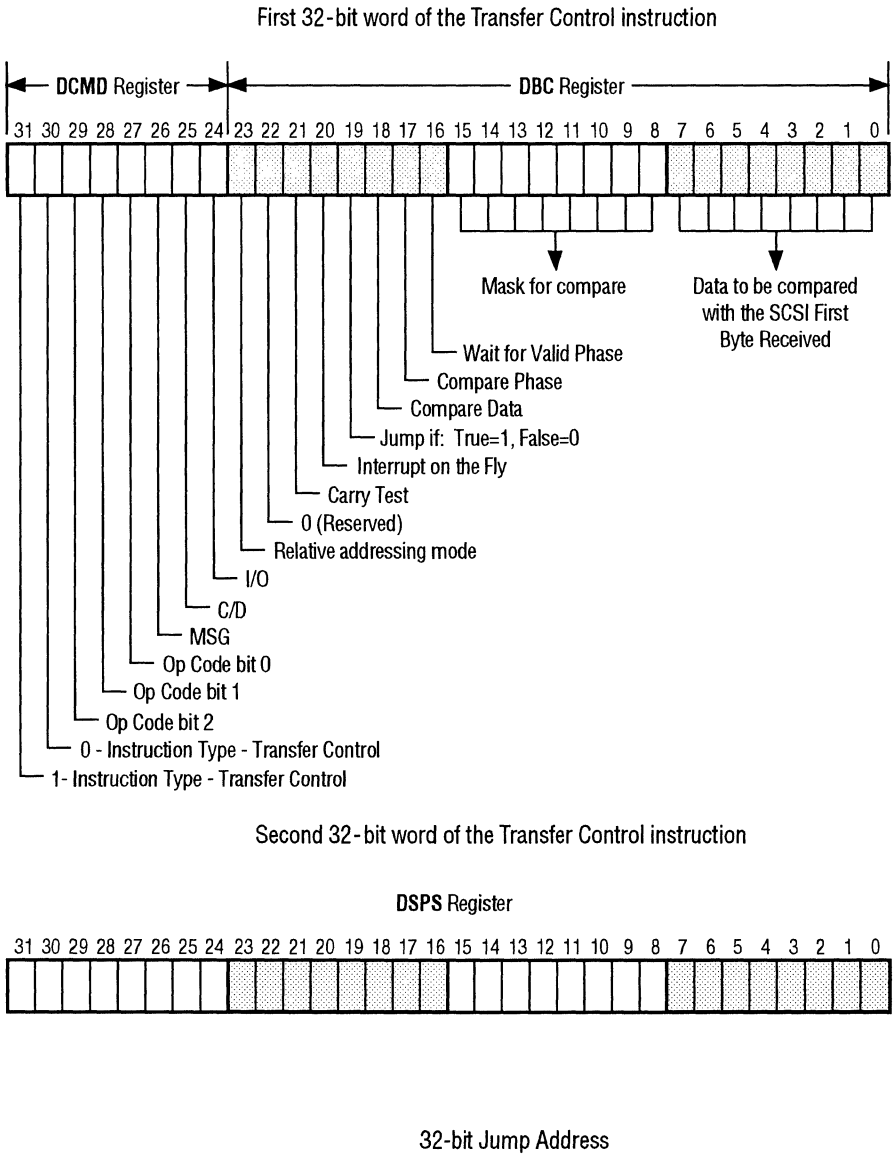
Table 6-1. Read/Write Instructions

Operator	Opcode 111 Read Modify Write	Opcode 110 Move to SFBR	Opcode 101 Move From SFBR
000	Move data into register. Syntax: "Move data8 to RegA"	Move data into SFBR register. Syntax: "Move data8 to SFBR"	Move data into register. Syntax: "Move data8 to RegA"
001*	Shift register one bit to the left and place the result in the same register. Syntax: "Move RegA SHL RegA"	Shift register one bit to the left and place the result in the SFBR register. Syntax: "Move RegA SHL SFBR"	Shift the SFBR register one bit to the left and place the result in the register. Syntax: "Move SFBR SHL RegA"
010	OR data with register and place the result in the same register. Syntax: "Move RegA | data8 to RegA"	OR data with register and place the result in the SFBR register. Syntax: "Move RegA | data8 to SFBR"	OR data with SFBR and place the result in the register. Syntax: "Move SFBR | data8 to RegA"
011	XOR data with register and place the result in the same register. Syntax: "Move RegA XOR data8 to RegA"	XOR data with register and place the result in the SFBR register. Syntax: "Move RegA XOR data8 to SFBR"	XOR data with SFBR and place the result in the register. Syntax: "Move SFBR XOR data8 to RegA"
100	AND data with register and place the result in the same register. Syntax: "Move RegA & data8 to RegA"	AND data with register and place the result in the SFBR register. Syntax: "Move RegA & data8 to SFBR"	AND data with SFBR and place the result in the register. Syntax: "Move SFBR & data8 to RegA"
101*	Shift register one bit to the right and place the result in the same register. Syntax: "Move RegA SHR RegA"	Shift register one bit to the right and place the result in the SFBR register. Syntax: "Move RegA SHR SFBR"	Shift the SFBR register one bit to the right and place the result in the register. Syntax: "Move SFBR SHR RegA"
110	Add data to register without carry and place the result in the same register. Syntax: "Move RegA + data8 to RegA"	Add data to register without carry and place the result in the SFBR register. Syntax: "Move RegA + data8 to SFBR"	Add data to SFBR without carry and place the result in the register. Syntax: "Move SFBR + data8 to RegA "
111	Add data to register with carry and place the result in the same register. Syntax: "Move RegA + data8 to RegA with carry"	Add data to register with carry and place the result in the SFBR register. Syntax: "Move RegA + data8 to SFBR with carry"	Add data to SFBR with carry and place the result in the register. Syntax: "Move SFBR + data8 to RegA with carry"

Notes: 1) *Substitute the desired register name or address for "RegA" in the syntax examples.*
2) *data8 indicates eight bits of data*

* *Data is shifted through the Carry bit and the Carry bit is shifted into the data byte*

Figure 6-4. Transfer Control Instruction



Transfer Control Instructions

Bits 31-30 Instruction Type - Transfer Control Instruction

Bits 29-27 Op Code

This 3-bit field specifies the type of transfer control instruction to be executed. All transfer control instructions can be conditional. They can be dependent on a true/false comparison of the ALU Carry bit or a comparison of the SCSI information transfer phase with the Phase field, and/or a comparison of the First Byte Received with the Data Compare field. Each instruction can operate in initiator or target mode.

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Jump
0	0	1	Call
0	1	0	Return
0	1	1	Interrupt
1	X	X	Reserved

Jump Instruction

1) The NCR 53C810 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare and True/False bit fields. If the comparisons are true, the NCR 53C810 loads the DSP register with the contents of the DSPS register. The DSP register now contains the address of the next instruction.

2) If the comparisons are false, the NCR 53C810 fetches the next instruction from the address pointed to by the DSP register, leaving the instruction pointer unchanged.

Call Instruction

1) The NCR 53C810 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, the NCR 53C810 loads the DSP register with the contents of the DSPS register and that address value becomes the address of the next instruction.

   When the NCR 53C810 executes a Call instruction, the instruction pointer contained in the DSP register is stored in the TEMP register. Since the TEMP register is not a stack and can only hold one longword, only one call is possible at once.

   2) If the comparisons are false, the NCR 53C810 fetches the next instruction from the address pointed to by the DSP register and the instruction pointer is not modified.

Return Instruction

1) The NCR 53C810 can do a true/false comparison of the ALU bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the NCR 53C810 loads the DSP register with the contents of the DSPS register. That address value becomes the address of the next instruction.

   When a Return instruction is executed, the value stored in the TEMP register is returned to the DSP register. The NCR 53C810 does not check to see whether the Call instruction has already been executed. It will not generate an interrupt if a Return instruction is executed without previously executing a Call instruction.

2) If the comparisons are false, then the NCR 53C810 fetches the next instruction from the address pointed to by the DSP register and the instruction pointer will not be modified.

Interrupt Instructions

Interrupt

a) The NCR 53C810 can do a true/false comparison of the ALU bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the NCR 53C810 generates an interrupt by asserting the IRQ/ signal.

b) The 32-bit address field stored in the DSPS register (not DNAD as in 53C700) can contain a unique interrupt service vector. When servicing the interrupt, this unique status code allows the ISR to quickly identify the point at which the interrupt occurred.

c) The NCR 53C810 halts and the DSP register must be written to start any further operation.

Interrupt on-the-Fly

a) The NCR 53C810 can do a true/false comparison of the ALU carry bit or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, the NCR 53C810 will assert the Interrupt on the fly bit (ISTAT bit 2).

Bits 26-24 SCSI Phase

This 3-bit field corresponds to the three SCSI bus phase signals which are compared with the phase lines latched when SREQ/ is asserted. Comparisons can be performed to determine the SCSI phase actually being driven on the SCSI bus. The following table describes the possible combinations and their corresponding SCSI phase. These bits are only valid when the NCR 53C810 is operating in initiator mode; when the NCR 53C810 is operating in the target mode, these bits should be cleared.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data out
0	0	1	Data in
0	1	0	Command
0	1	1	Status
1	0	0	Reserved out
1	0	1	Reserved in
1	1	0	Message out
1	1	1	Message in

Bit 23 Relative Addressing Mode

When this bit is set, the 24-bit signed value in the DSPS register is used as a relative offset from the current DSP address (which is pointing to the next instruction, not the one currently executing). Relative mode does not apply to Return and Interrupt SCRIPTS.

Jump/Call an Absolute Address – Start execution at the new absolute address.

Command	Condition Codes
Absolute Alternate Address	

Jump/Call a Relative Address – Start execution at the current address plus (or minus) the relative offset.

Command	Condition Codes
Don't Care	Alternate Jump Offset

The SCRIPTS program counter is a 32-bit value pointing to the SCRIPT currently being executed by the NCR 53C810. The next address is formed by adding the 32-bit program counter to the 24-bit signed value of the last 24 bits of the Jump or Call instruction. Because it is signed (twos compliment), the jump can be forward or backward.

A relative transfer can be to any address within a 16-MB segment. The program counter is combined with the 24-bit signed offset (using addition or subtraction) to form the new execution address.

SCRIPTS programs may contain a mixture of direct jumps and relative jumps to provide maximum versatility when writing SCRIPTS. For example, major sections of code can be accessed with far calls using the 32-bit physical address, then local labels can be called using relative transfers. If a SCRIPT is written using only relative transfers it would not require any run time alteration of physical addresses, and could be stored in and executed from a PROM.

Bit 21 Carry Test

When this bit is set, decisions based on the ALU carry bit can be made. True/False comparisons are legal, but Data Compare and Phase Compare are illegal.

Bit 20 Interrupt on the Fly

When this bit is set, the interrupt instruction will not halt the SCRIPTS processor. Once the interrupt occurs, the Interrupt on the Fly bit (ISTAT bit 2) will be asserted.

Bit 19 Jump If True/False

This bit determines whether the NCR 53C810 should branch when a comparison is true or when a comparison is false. This bit applies to Phase Compares, Data Compares, and Carry Tests. If both the Phase Compare and Data Compare bits are set, then both compares must be true to branch on a true condition. Both compares must be false to branch on a false condition.

Bit 19	Result of Compare	Action
0	False	Jump Taken
0	True	No Jump
1	False	No Jump
1	True	Jump Taken

Bit 18 Compare Data

When this bit is set, then the first byte received from the SCSI data bus (contained in SFBR register) is compared with the Data to be Compared Field in the Transfer Control instruction. The Wait for Valid Phase bit controls when this compare will occur. The Jump if True/False bit determines the condition (true or false) to branch on.

Bit 17 Compare Phase

When the NCR 53C810 is in initiator mode, this bit controls phase compare operations. When this bit is set, the SCSI phase signals (latched by SREQ/) are compared to the Phase Field in the Transfer Control instruction; if they match, then the comparison is true. The Wait for Valid Phase bit controls when the compare will occur. When the NCR 53C810 is operating in target mode this bit, when set, tests for an active SCSI SATN/ signal.

Bit 16 Wait For Valid Phase

If the Wait for Valid Phase bit is set, then the NCR 53C810 waits for a previously unserviced phase before comparing the SCSI phase and data.

If the Wait for Valid Phase bit is clear, then the NCR 53C810 compares the SCSI phase and data immediately.

Bits 15-8 Data Compare Mask

The Data Compare Mask allows a SCRIPT to test certain bits within a data byte. During the data compare, any mask bits that are set cause the corresponding bit in the SFBR data byte to be ignored. For instance, a mask of 01111111b and data compare value of 1XXXXXXXb allows the SCRIPTS processor to determine whether or not the high order bit is on while ignoring the remaining bits.

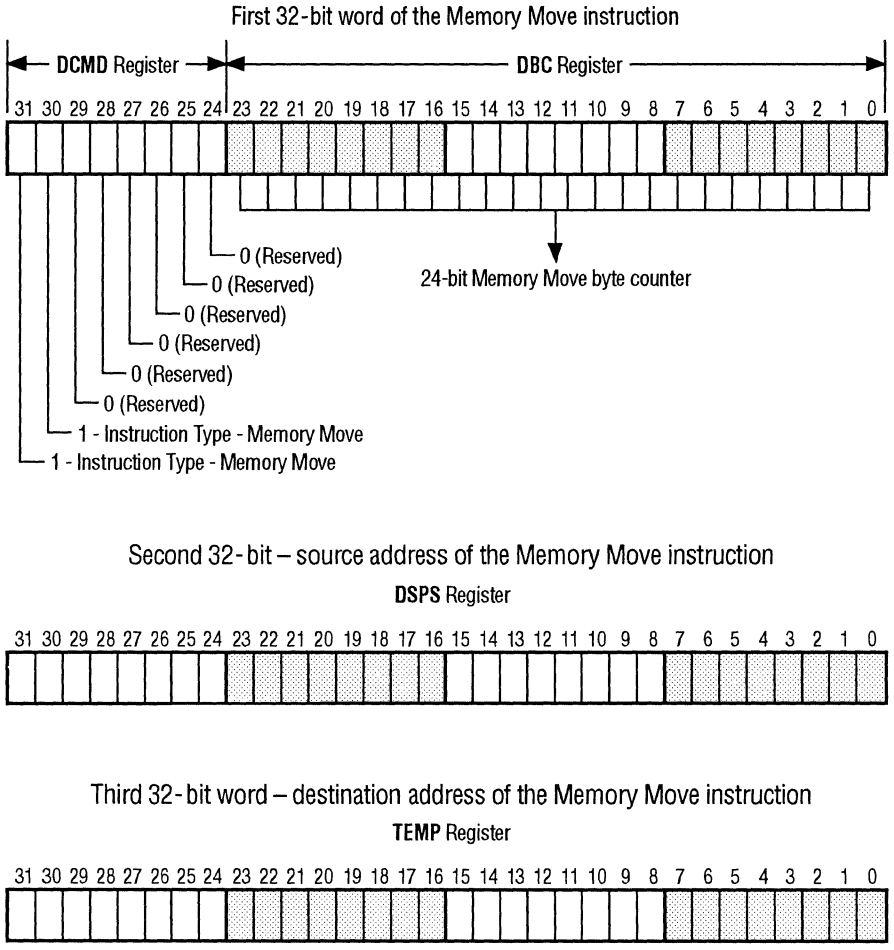
Bits 7-0 Data Compare Value

This 8-bit field is the data to be compared against the SCSI First Byte Received (SFBR) register. These bits are used in conjunction with the Data Compare Mask Field to test for a particular data value.

Bits 31-0 Jump Address

This 32-bit field contains the address of the next instruction to fetch when a jump is taken. Once the NCR 53C810 has fetched the instruction from the address pointed to by these 32 bits, this address is incremented by 4, loaded into the DSP register and becomes the current instruction pointer.

Figure 6-5. Memory Move Instructions



Memory Move Instructions

For Memory Move commands, bits 5 and 4 (SIOM and DIOM) in the DMODE register determine whether the source or destination addresses reside in memory or I/O space. By setting these bits appropriately, data may be moved within memory space, within I/O space, or between the two address spaces.

The Memory Move instruction is used to copy the specified number of bytes from the source address to the destination address.

Allowing the NCR 53C810 to perform memory moves frees the system processor for other tasks and moves data at higher speeds than available from current DMA controllers. Up to 16 MB may be transferred with one instruction. There are two restrictions:

1) Both the source and destination addresses must start with the same address alignment (A(1-0) must be the same). If source and destination are not aligned, then an illegal instruction interrupt will occur.
2) Indirect addresses are not allowed.

A burst of data is fetched from the source address, put into the DMA FIFO and then written out to the destination address. The move continues until the byte count decrements to zero, then another SCRIPT is fetched from system memory.

The DSPS and DSA registers are additional holding registers used during the Memory Move; however, the contents of the DSA register are preserved.

Bits 29-24 Reserved

These bits are reserved and must be zero. If any of these bits is set, an illegal instruction interrupt will occur.

Bits 23-0 Transfer Count

The number of bytes to be transferred is stored in the lower 24 bits of the first instruction word.

Read/Write System Memory from a Script

By using the Memory Move instruction, single or multiple register values may be transferred to or from system memory.

Because the NCR 53C810 will respond to addresses as defined in the Base I/O or Base Memory registers, it could be accessed during a Memory Move operation if the source or destination address decodes to within the chip's register space. If this occurs, the register indicated by the lower seven bits of the address is taken to be the data source or destination. In this way, register values can be saved to system memory and later restored, and SCRIPTS can make decisions based on data values in system memory.

The SFBR is not writable via the CPU, and therefore not by a Memory Move. However, it can be loaded via SCRIPTS Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate NCR 53C810 register (for example, a SCRATCH register), and then to the SFBR.

The same address alignment restrictions apply to register access operations as to normal memory-to-memory transfers.

Chapter Seven
Electrical Characteristics

DC Electrical Characteristics

Absolute Maximum Stress Ratings

Symbol	Parameter	Min	Max	Unit	Test Conditions
T_{STG}	Storage temperature	-55	150	°C	-
V_{DD}	Supply voltage	-0.5	7.0	V	-
V_{IN}	Input Voltage	V_{SS} - 0.5	V_{DD} + 0.5	V	-
I_{LP}*	Latch-up current	± 200	-	mA	-
ESD**	Electrostatic discharge	-	2K	V	MIL-STD 883C, Method 3015.7

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or at any other conditions beyond those indicated in the Operating Conditions section of this manual is not implied.

* *-2V < VPIN < 8V*

** *SCSI pins only*

Operating Conditions

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{DD}	Supply voltage	4.75	5.25	V	-
I_{DD}	Supply current	-	130	mA	-
T_A	Operating free air	0	70	°C	-
Θ_{JA}	Thermal Resistance (junction ambient)	-	67	°C/W	-

* *Conditions that exceed the operating limits may cause the device to function incorrectly*

SCSI Signals - SD (7-0)/, SDP/, REQ/, ACK/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} + 0.5	V	-
V_{IL}	Input low voltage	V_{SS} - 0.5	0.8	V	-
V_{OH}*	Output high voltage	2.5	3.5	V	2.5 mA
V_{OL}	Output low voltage	V_{SS}	0.5	V	48 mA
I_{IN}	Input leakage	-10	10	µA	-
I_{OZ}	Tristate leakage	-10	10	µA	-

* TolerANT active negation enabled

SCSI Signals - SMSG/, SI_O/, SC_D/, SATN/, SBSY/, SSEL/, SRST/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} + 0.5	V	-
V_{IL}	Input low voltage	V_{SS} - 0.5	0.8	V	-
V_{OL}	Output low voltage	V_{SS}	0.5	V	48 mA
I_{IN}	Input leakage	-10	10	µA	-
	SCSI RST/ only	-500	-50	µA	-
I_{OZ}	Tristate leakage	-10	10	µA	-

Input Signals - CLK, SCLK, GNT/, IDSEL, RST/, TESTIN

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} + 0.5	V	-
V_{IL}	Input low voltage	V_{SS} - 0.5	0.8	V	-
I_{IN}	Input leakage	-1.0	1.0	µA	-

Note: *CLK, SCLK, GNT/, and IDSEL have 100 µA pull-ups that are enabled when TESTIN is low. TESTIN has a 100 µA pull-up that is always enabled.*

Capacitance

Symbol	Parameter	Min	Max	Unit	Test Conditions
C_I	Input capacitance of input pads	-	7	pF	-
C_{IO}	Input capacitance of I/O pads	-	10	pF	-

Output Signal - MAC/_TESTOUT

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	-16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{OH}	Output high current	-8	-	mA	V_{DD} - .5 V
I_{OL}	Output low current	16	-	mA	0.4 V
I_{OZ}	Tristate leakage	-10	10	µA	-

Output Signal - IRQ/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	-8 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	8 mA
I_{OH}	Output high current	-4	-	mA	V_{DD} - .5 V
I_{OL}	Output low current	8	-	mA	0.4 V
I_{OZ}	Tristate leakage	-10	10	µA	-

Note: *IRQ/ has a 100 µA pull-up that is enabled when TESTIN is low. IRQ/ can be enabled with a register bit as an open drain output with an internal 100 µA pull-up.*

Output Signal - REQ/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	TBD	TBD	V	-
V_{OL}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{OH}	Output high current	-8	-	mA	2.4 V
I_{OL}	Output low current	16	-	mA	0.4 V

Note: REQ/ has a 100 µA pull-up that is enabled when TESTIN is low.

Output Signal - SERR/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OL}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{OL}	Output low current	16	-	mA	0.4 V
I_{OZ}	Tristate leakage	-10	10	µA	-

Bidirectional Signals - AD (31-0), C_BE (3-0)/, FRAME/, IRDY/, TRDY/, DEVSEL/, STOP/, PERR/, PAR

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} + 0.5	V	-
V_{IL}	Input low voltage	V_{SS} - 0.5	0.8	V	-
V_{OH}	Output high voltage	2.4	V_{DD}	V	16mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{OH}	Output high current	-8	-	mA	V_{DD} -0.5
I_{OL}	Output low current	16	-	mA	0.4V
I_{IN}	Input leakage	-10	10	µA	$V_{SS} < V_{IN} < V_{DD}$
I_{OZ}	Tristate leakage	-10	10	µA	-

Note: All the signals in this table have 100 µA pull-ups that are enabled when TESTIN is low.

Bidirectional Signals - GPIO0_FETCH/, GPIO1_MASTER/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} + 0.5	V	-
V_{IL}	Input low voltage	V_{SS} - 0.5	0.8	V	-
V_{OH}	Output high voltage	2.4	V_{DD}	V	-16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{OH}	Output high current	-8	-	mA	2.4V
I_{OL}	Output low current	16	-	mA	0.4V
I_{IN}	Input leakage	-10	10	µA	-
I_{OZ}	Tristate leakage	-10	10	µA	-

Note: All the signals in this table have 100 µA pull-ups that are enabled when TESTIN is low.

NCR TolerANT Active Negation Technology Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{OH} [1]	Output high voltage	I_{OH}= 2.5 mA	2.5	3.1	3.5	V
V_{OL}	Output low voltage	I_{OL} = 48 mA	0.1	0.2	0.5	V
V_{IH}	Input high voltage		2.0	-	7.0	V
V_{IL}	Input low voltage	Referenced to V_{SS}	-0.5	-	0.8	V
V_{IK}	Input clamp voltage	V_{DD}= 4.75; I_I= -20mA	-0.66	-0.74	-0.77	V
V_{TH}	Threshold, high to low		1.1	1.2	1.3	V
V_{TL}	Threshold, low to high		1.5	1.6	1.7	V
V_{TH} - V_{TL}	Hysteresis		200	300	400	mV
I_{OH} [1]	Output high current	V_{OH} = 2.5 Volts	2.5	15	24	mA
I_{OL}	Output low current	V_{OL} = 0.5 Volts	100	150	200	mA
I_{OSH} [1]	Short-circuit output high current	Output driving low, pin shorted to V_{DD} supply[2]	-	-	625	mA
I_{OSL}	Short-circuit output low current	Output driving high, pin shorted to V_{SS} supply	-	-	95	mA
I_{LH}	Input high leakage	-0.5 < V_{DD} < 5.25 V_{PIN} = 2.7 V	-	0.05	10	µA
I_{LL}	Input low leakage	-0.5 < V_{DD} < 5.25 V_{PIN} = 0.5V	-	-0.05	-10	µA
R_I	Input resistance	SCSI pins [3]	-	20	-	MΩ
C_P	Capacitance per pin	PQFP	-	8	10	pF
t_R [1]	Rise time, 10% to 90 %	Figure 7-1	9.7	15.0	18.5	ns
t_F	Fall time, 90% to 10%	Figure 7-1	5.2	8.1	14.7	ns
dV_H/dt	Slew rate, low to high	Figure 7-1	0.15	0.23	0.49	V/ns
dV_L/dt	Slew rate, high to low	Figure 7-1	0.19	0.37	0.67	V/ns

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
	Electrostatic Discharge	MIL-STD-883C; 3015-7	2	-	-	KV
	Latch-up		100	-	-	mA
	Filter Delay	Figure 7-2	20	25	30	ns
	Extended FIlter Delay	Figure 7-2	40	50	60	ns

Note: *These values are guaranteed by periodic characterization; they are not 100% tested on every device.*

[1] Active Negation outputs only: Data, Parity, REQ, ACK

[2] Single pin only; irreversible damage may occur if sustained for 1 second

[3] *SCSI RESET* pin has 10kΩ pull-up resistor

Figure 7-1. Rise and Fall Time Test Conditions

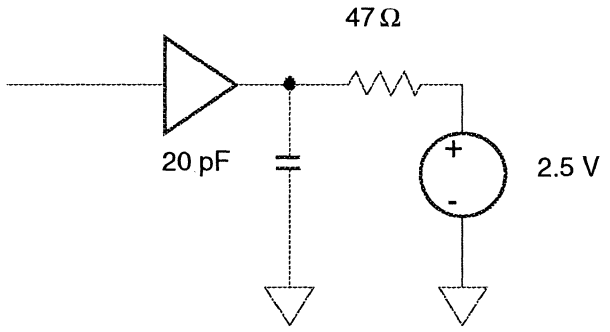


Figure 7-2. SCSI Input Filtering

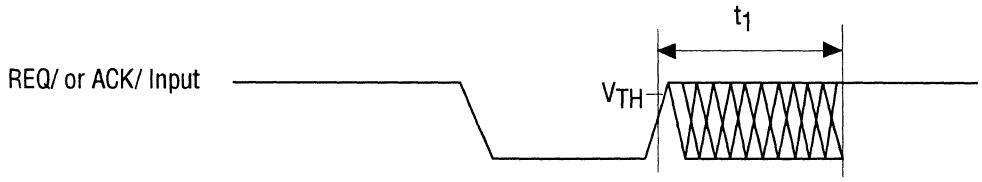


Figure 7-3. Hysteresis of SCSI Receiver

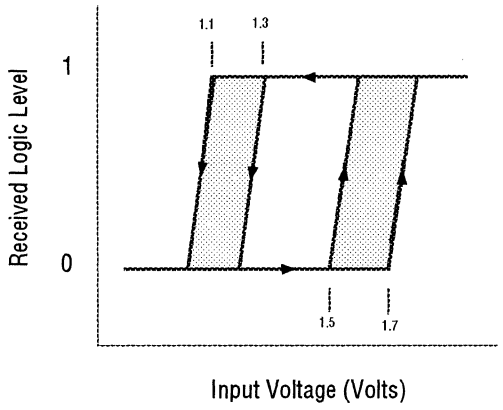


Figure 7-4 Input Current as a Function of Input Voltage

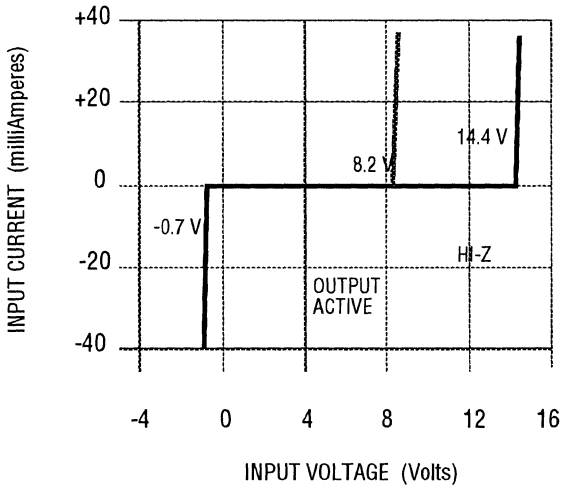
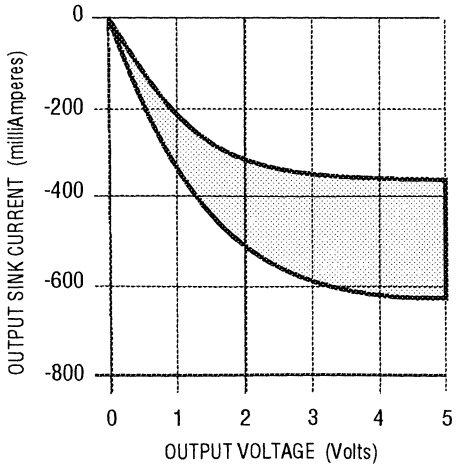
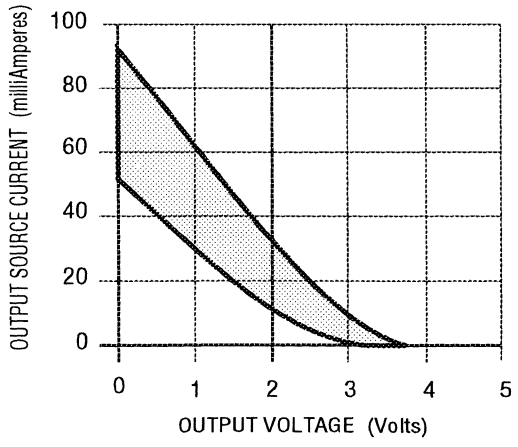


Figure 7-5. Output Current as a Function of Output Voltage



Output Sink Current as a Function of Output Voltage (I_{OL})

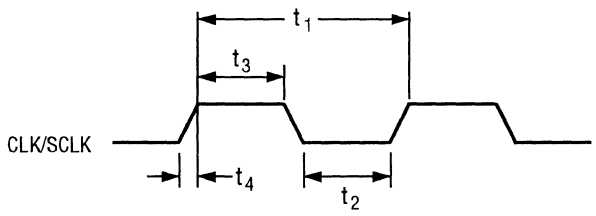


Output Source Current as a Function of Output Voltage (I_{OH})

AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to the *DC Characteristics* section). Chip timings are based on simulation at worst case voltage, temperature, and processing.

Figure 7-6. Clock Timing

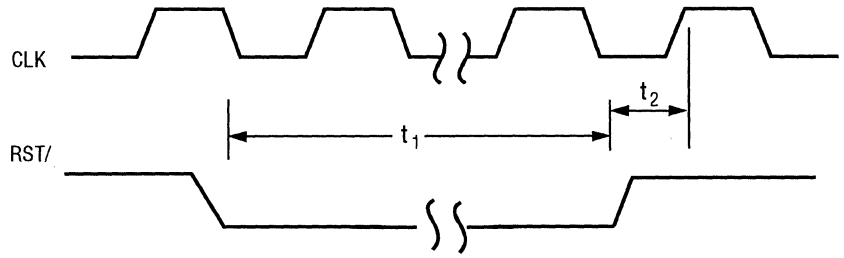


Parameter	Symbol	Min	Max	Units
Bus clock cycle time (CLK)	t_1	30	DC	ns
SCSI clock cycle time (SCLK)*		15	60	ns
CLK low time**	t_2	12	-	ns
SCLK low time**		6	33	ns
CLK high time**	t_3	12	-	ns
SCLK high time**		6	33	ns
CLK slew rate	t_4	1	-	V/ns
SCLK slew rate		1	-	V/ns

* *This parameter must be met to insure SCSI timings are within specification.*

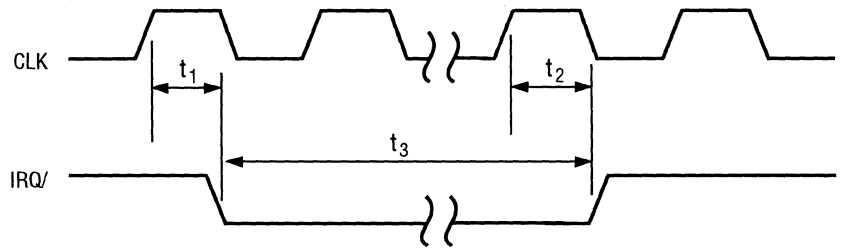
** *Duty cycle not to exceed 60/40.*

Figure 7-7. Reset Input



Parameter	Symbol	Min	Max	Units
Reset pulse width	t_1	10	-	t_{CLK}
Reset deasserted setup to CLK high	t_2	0	-	ns

Figure 7-8. Interrupt Output



Parameter	Symbol	Min	Max	Units
CLK high to IRQ/ low	t_1	TBD	-	ns
CLK high to IRQ/ high	t_2	TBD	-	ns
IRQ/ deassertion time	t_3	3	-	CLKS

Figure 7-9. Configuration Register Read

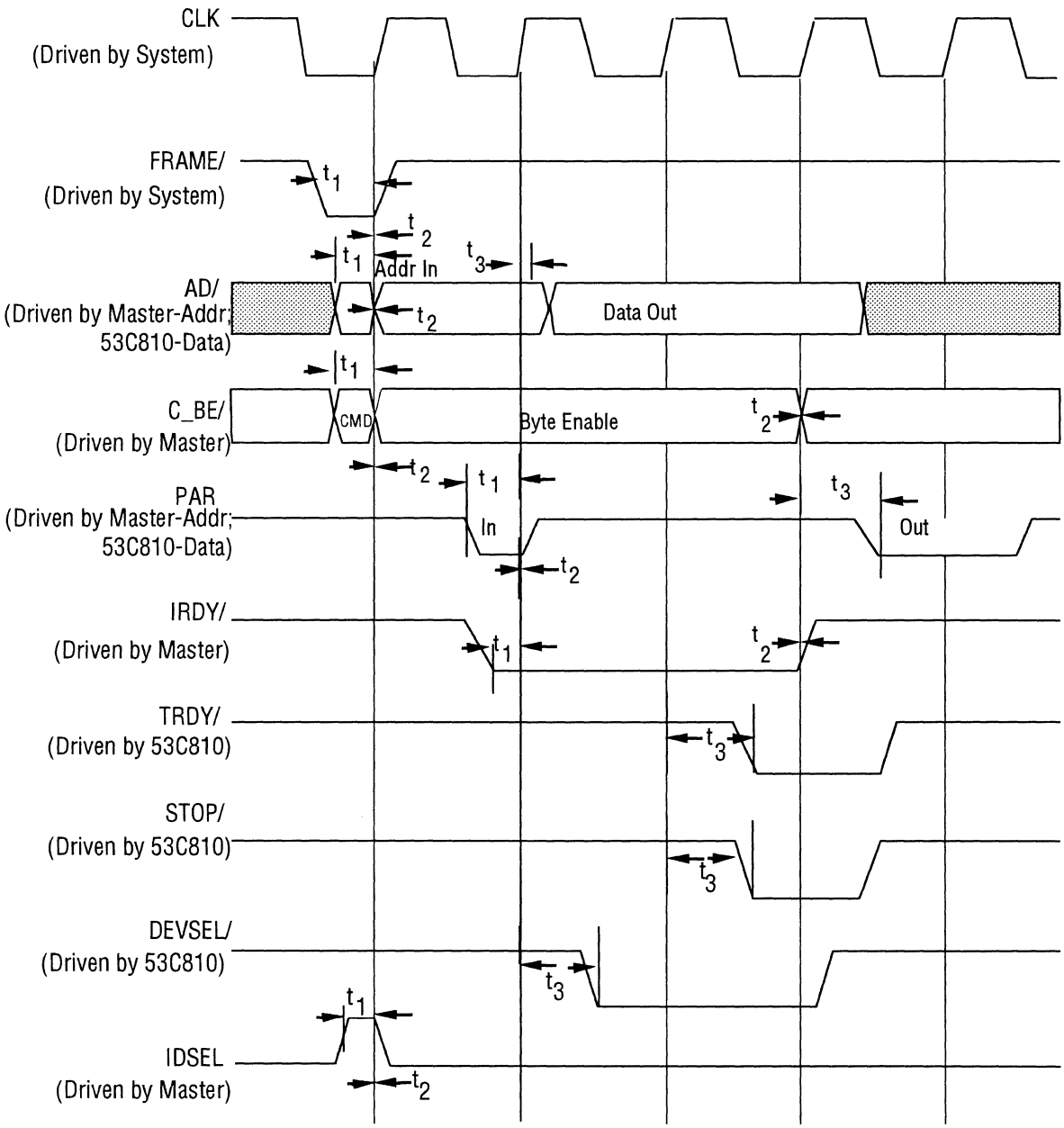


Figure 7-10. Configuration Register Write

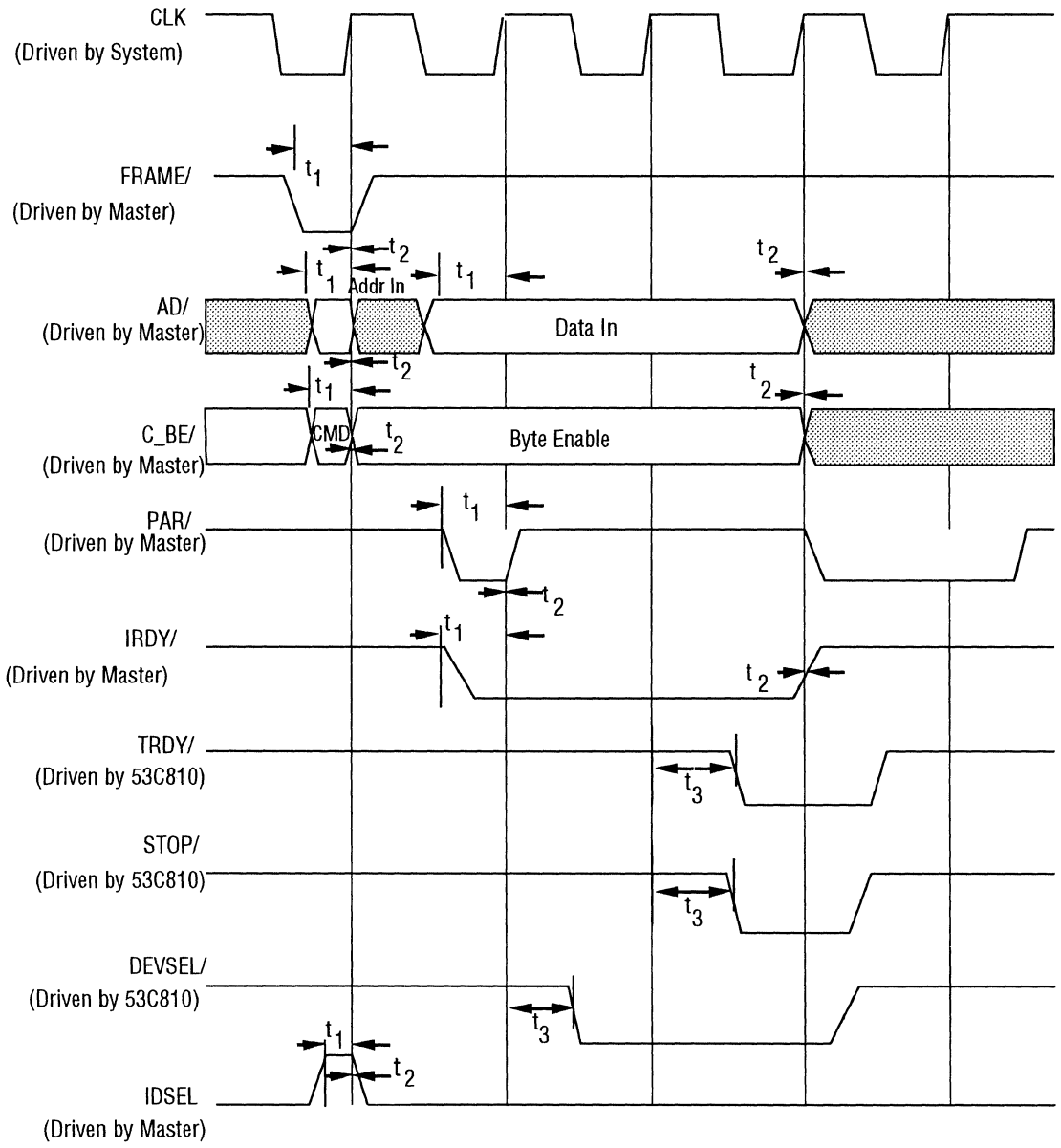


Figure 7-11. Target Read

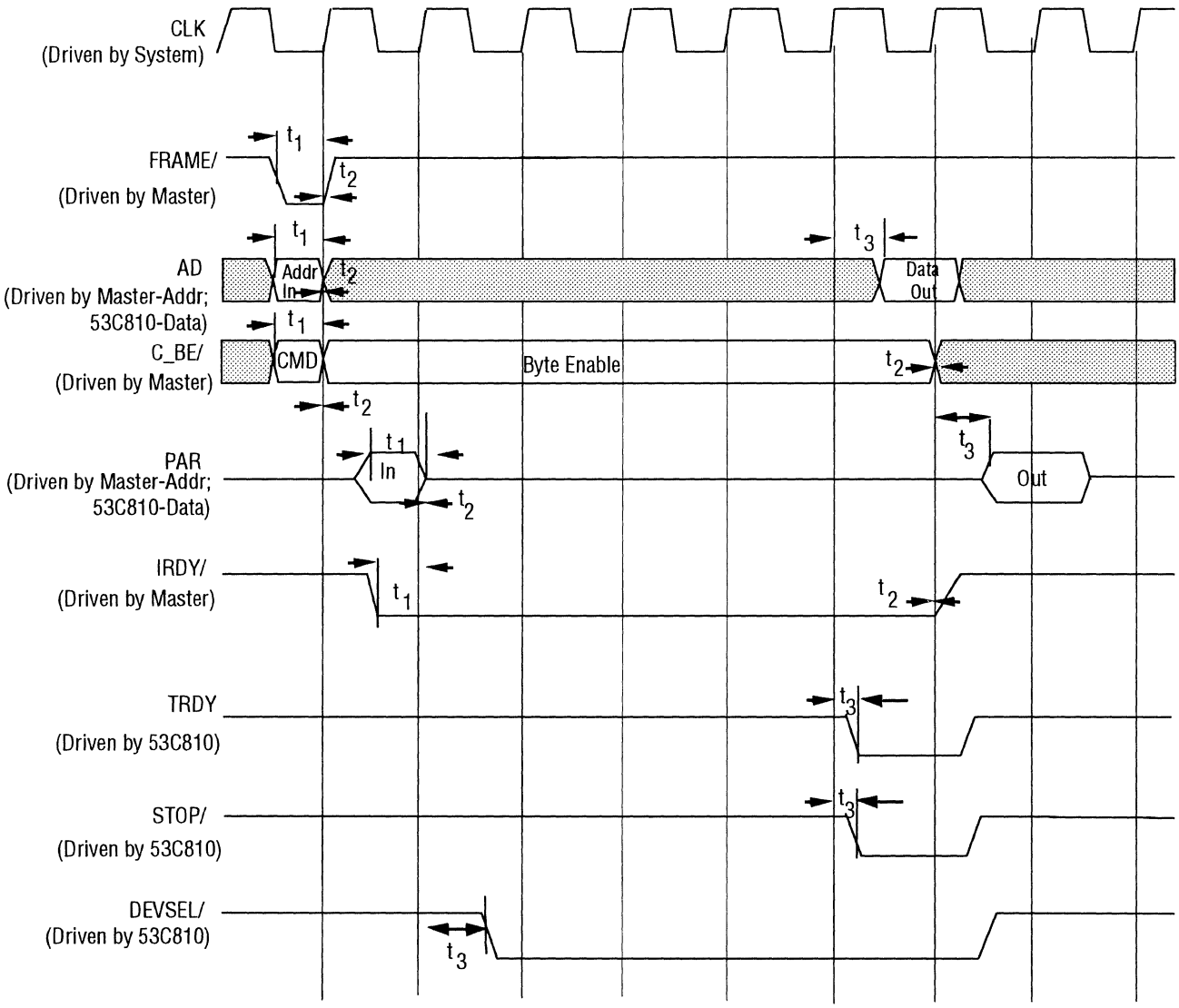


Figure 7-12. Target Write

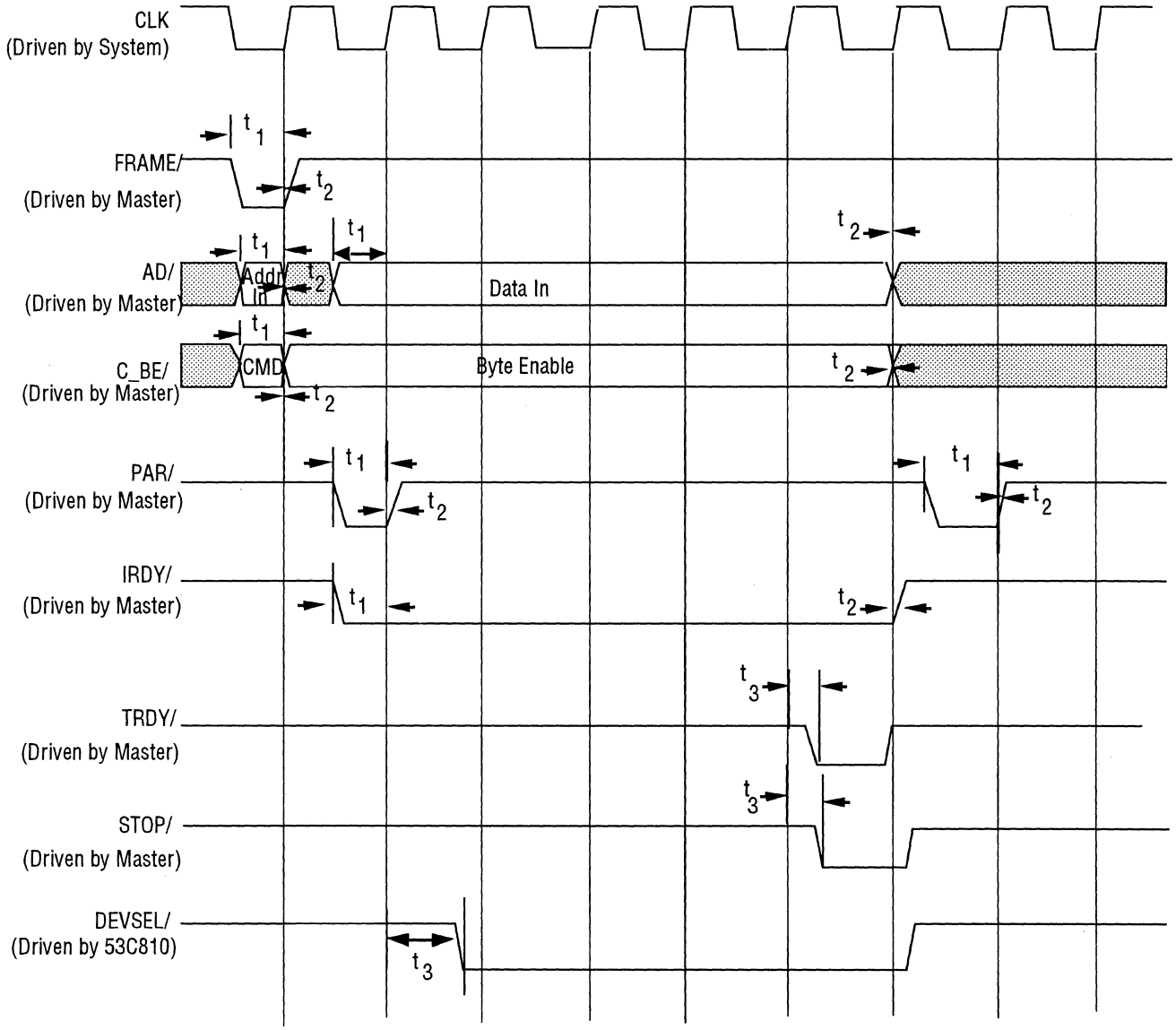
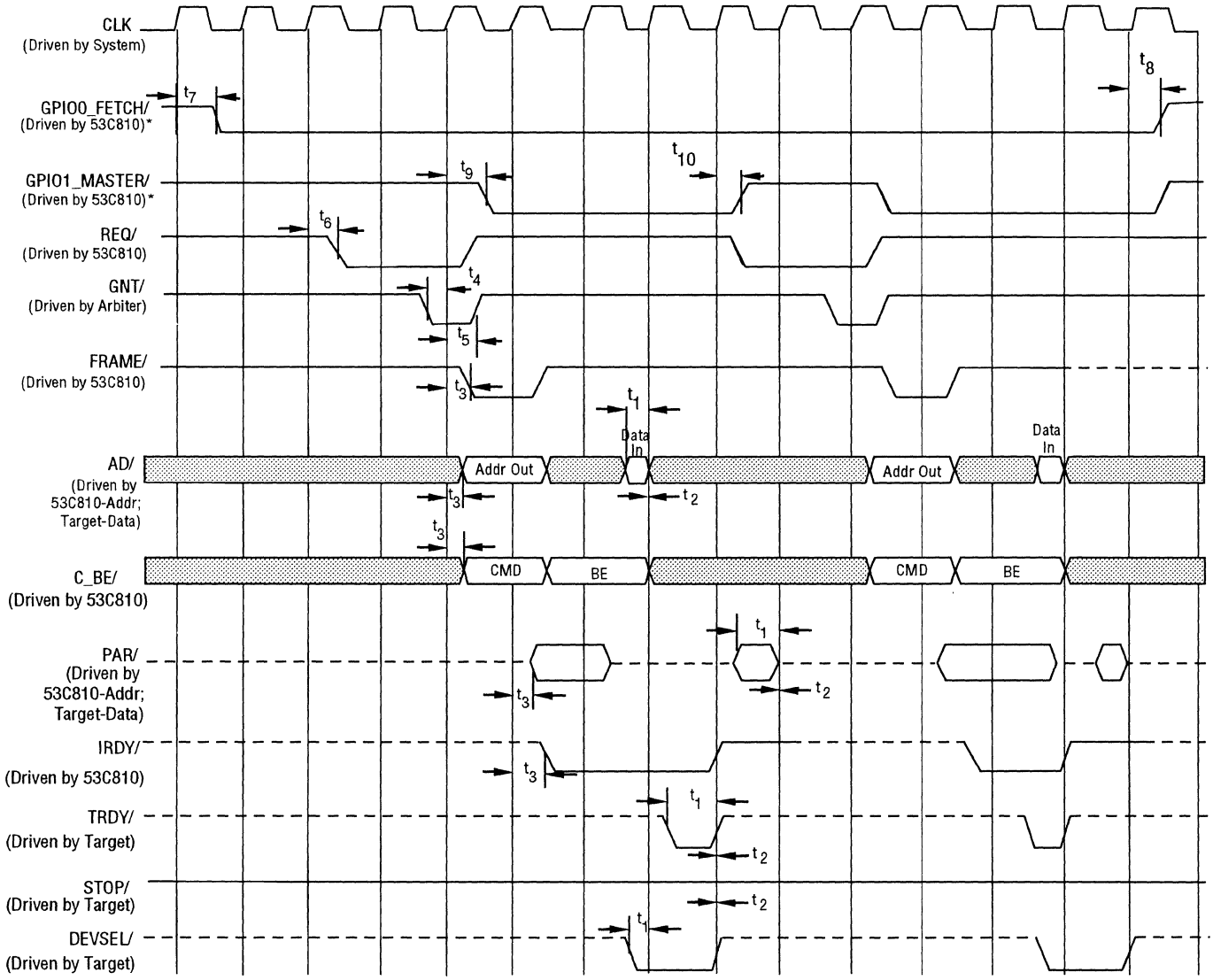
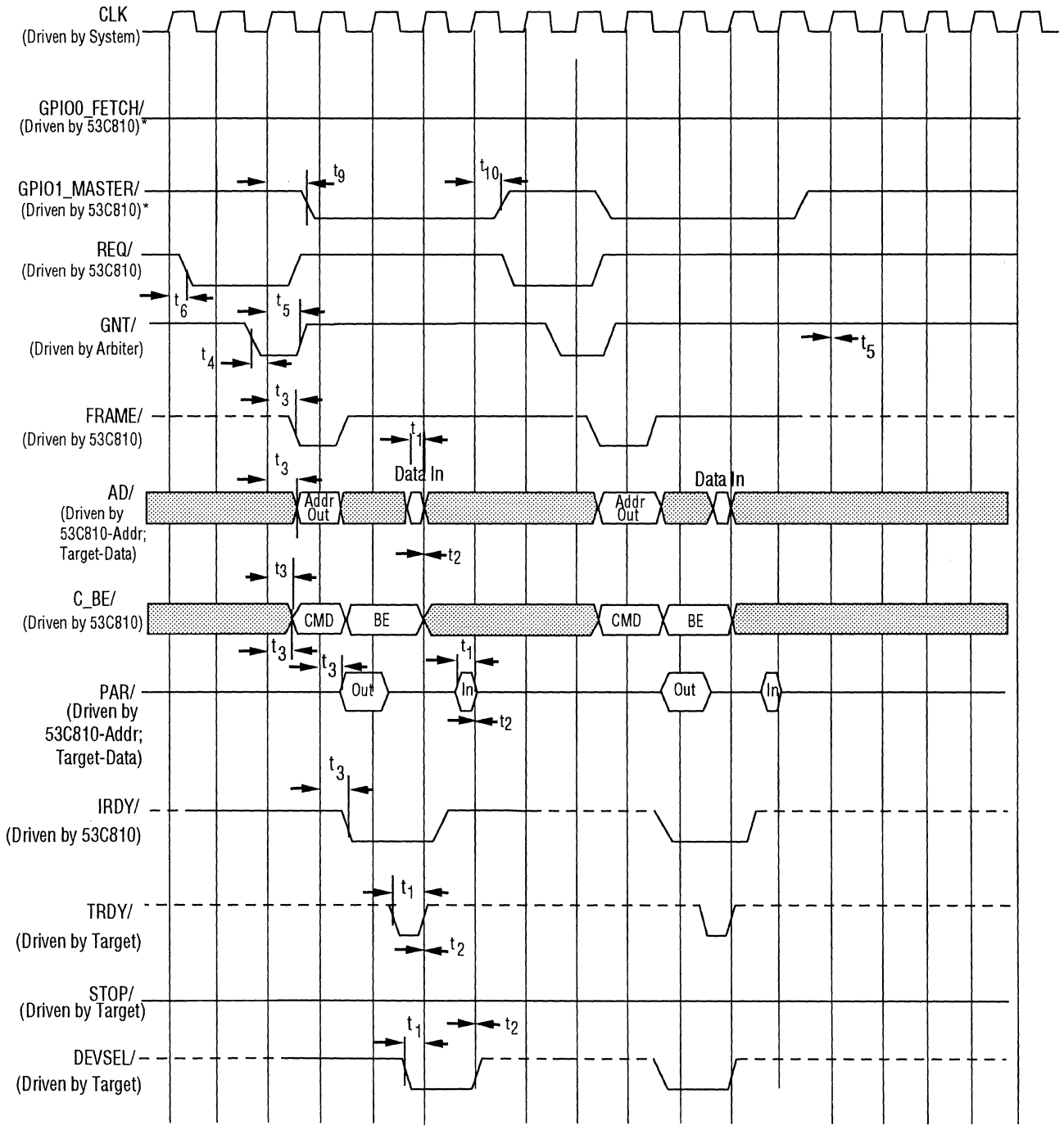


Figure 7-13. Op Code Fetch



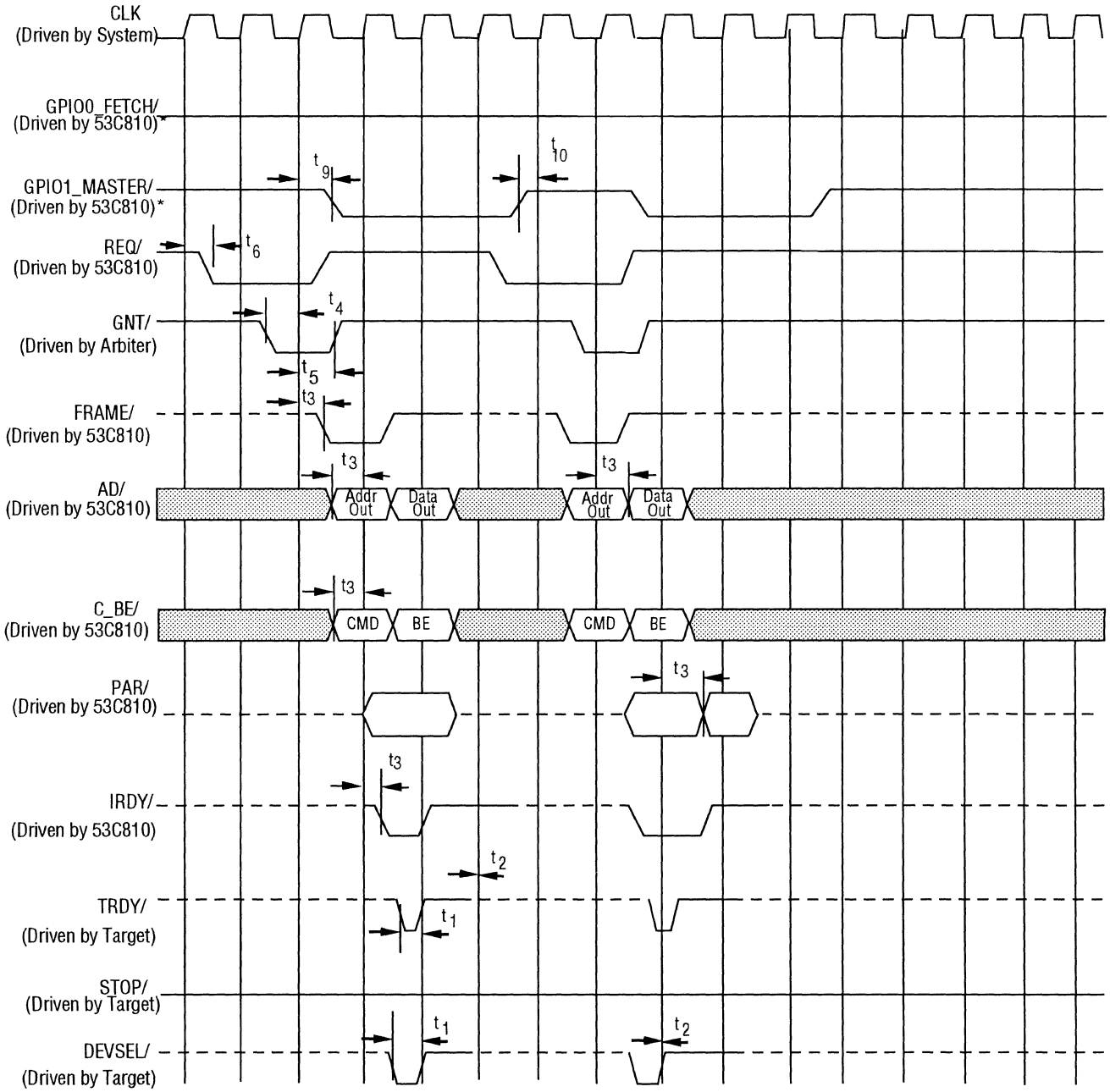
**When enabled*

Figure 7-14. Back-to-Back Read



**When enabled*

Figure 7-15. Back-to-Back Write



**When enabled*

Figure 7-16. Burst Read

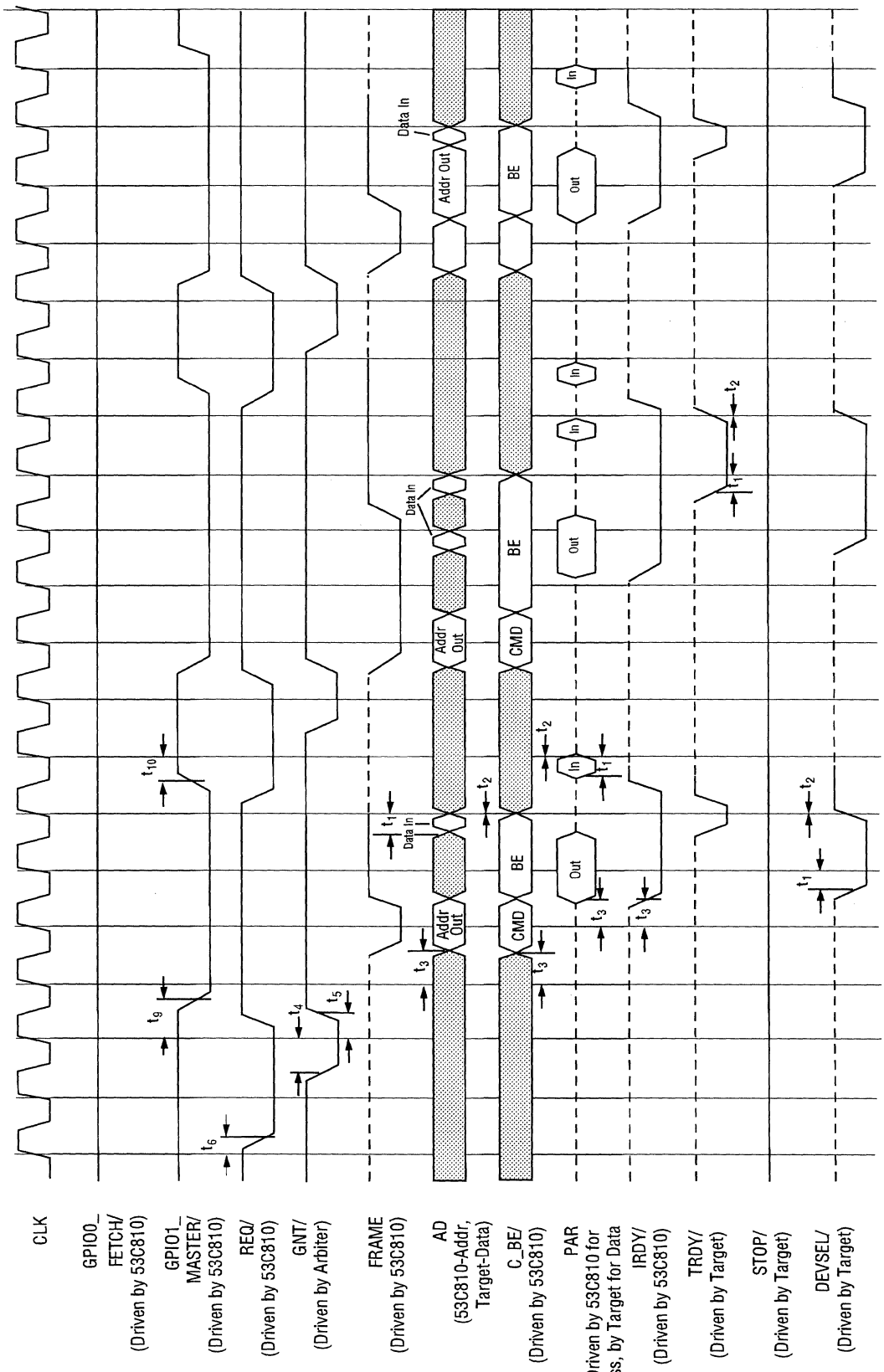
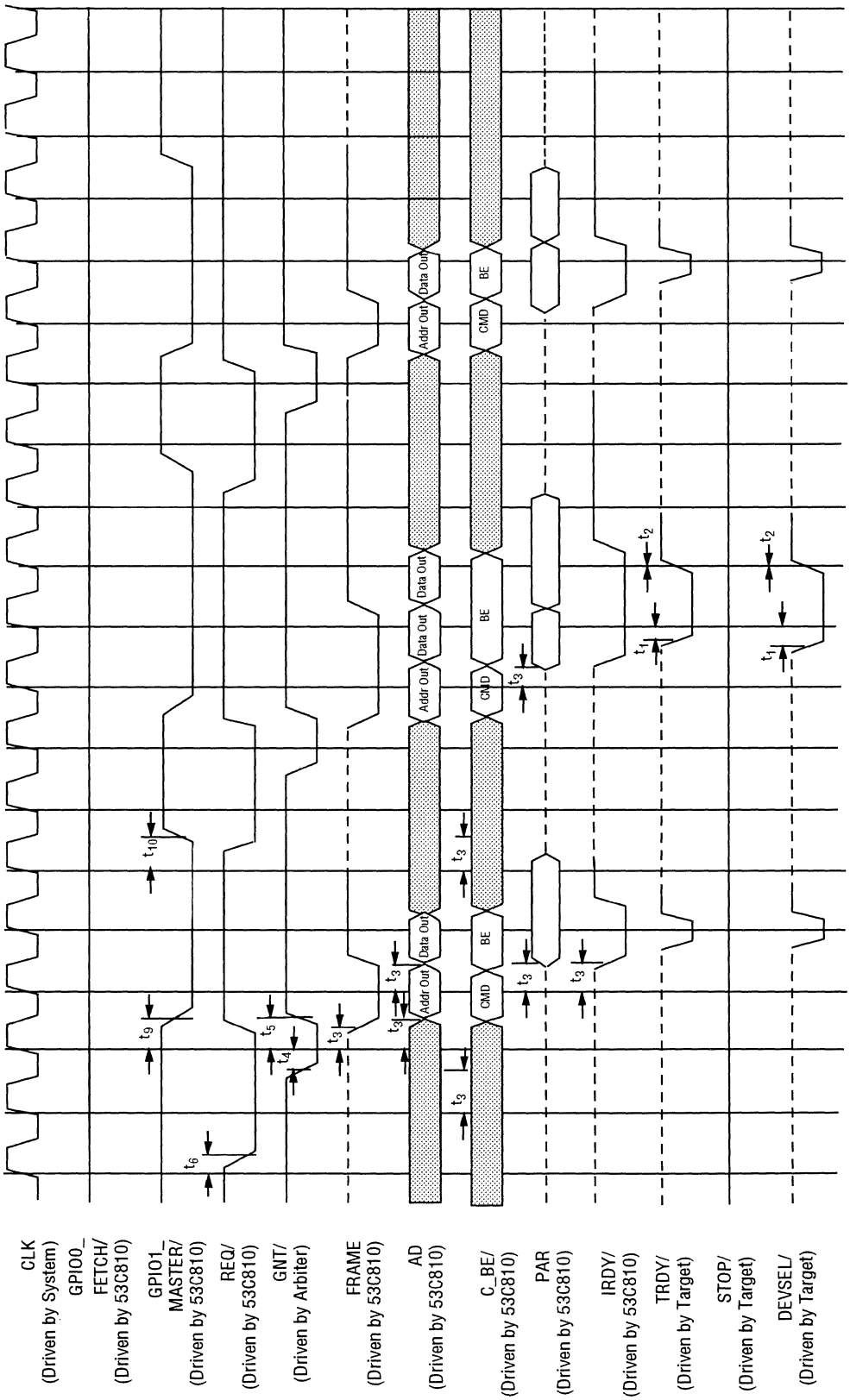


Figure 7-17. Burst Write



NCR 53C810 Timings

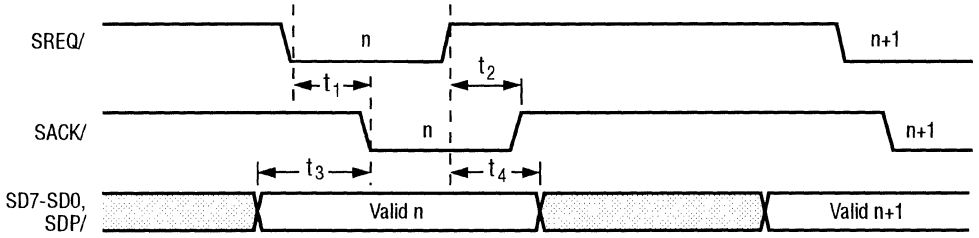
The previous pages illustrate the 53C810 timings. Please note that these are preliminary.

Symbol	Parameter	Min	Max	Units	Conditions
t_1	Shared signal input setup time	TBD	-	ns	-
t_2	Shared signal input hold time	TBD	-	ns	-
t_3	CLK to shared signal output valid	-	TBD	ns	-
t_4	Side signal input setup time	TBD	-	ns	-
t_5	Side signal input hold time	TBD	-	ns	-
t_6	CLK to side signal output valid	-	TBD	ns	-
t_7	CLK high to FETCH/ low		TBD	ns	-
t_8	CLK high to FETCH/ high	-	TBD	ns	-
t_9	CLK high to MASTER/ low	-	TBD	ns	-
t_{10}	CLK high to MASTER/ high	-	TBD	ns	-

Note: *PERR and SERR have the same timings as other PCI signals.*

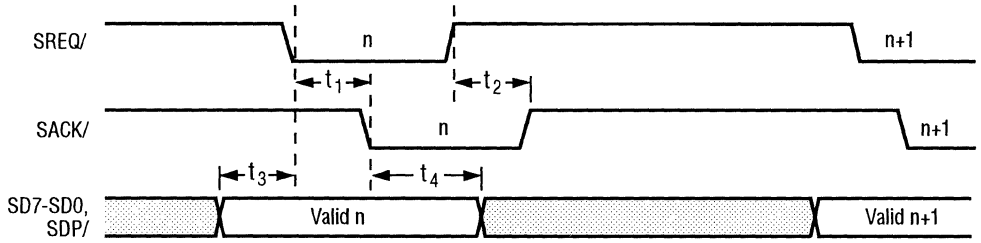
SCSI Timings

Figure 7-18. Initiator Asynchronous Send



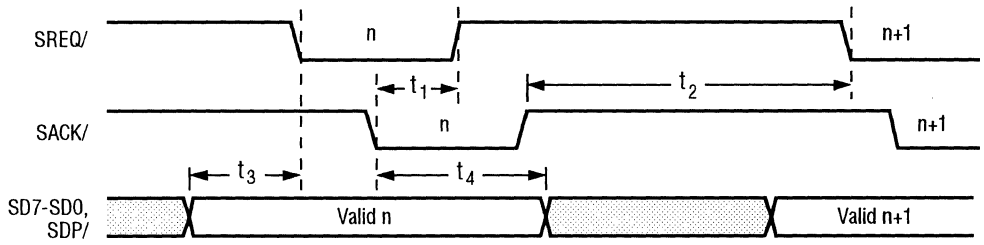
Parameter	Symbol	Min	Max	Units
SACK/ asserted from SREQ/ asserted	t_1	10	-	ns
SACK/ deasserted from SREQ/ deasserted	t_2	10	-	ns
Data setup to SACK/ asserted	t_3	55	-	ns
Data hold from SREQ/ deasserted	t_4	20	-	ns

Figure 7-19. Initiator Asynchronous Receive



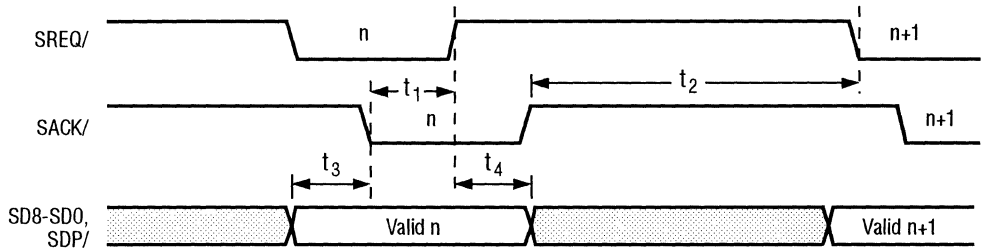
Parameter	Symbol	Min	Max	Units
SACK/ asserted from SREQ/ asserted	t_1	10	-	ns
SACK/ deasserted from SREQ/ deasserted	t_2	10	-	ns
Data setup to SREQ/ asserted	t_3	0	-	ns
Data hold from SACK/ deasserted	t_4	0	-	ns

Figure 7-20. Target Asynchronous Send



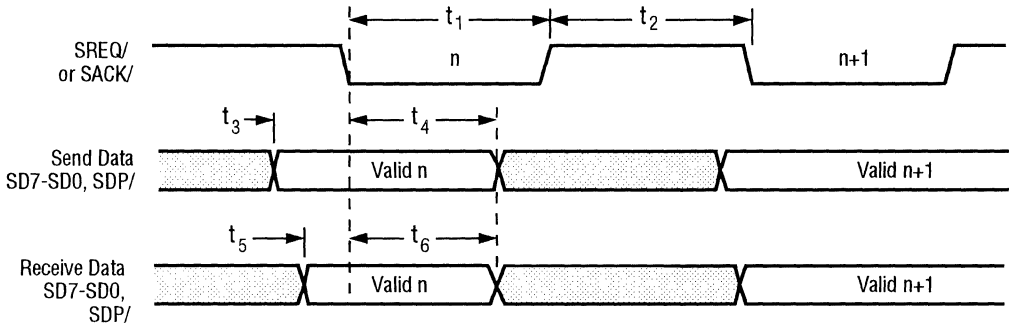
Parameter	Symbol	Min	Max	Units
SREQ/ deasserted from SACK/ asserted	t_1	10	-	ns
SREQ/ asserted from SACK/ deasserted	t_2	10	-	ns
Data setup to SREQ/ asserted	t_3	55	-	ns
Data hold from SACK/ asserted	t_4	20	-	ns

Figure 7-21. Target Asynchronous Receive



Parameter	Symbol	Min	Max	Units
SREQ/ deasserted from SACK/ asserted	t_1	10	-	ns
SREQ/ asserted from SACK/ deasserted	t_2	10	-	ns
Data setup to SACK/ asserted	t_3	0	-	ns
Data hold from SREQ/ deasserted	t_4	0	-	ns

Figure 7-22. Initiator and Target Synchronous Transfers



SCSI-1 Transfers (5.0 MB/sec)

Parameter	Symbol	Min	Max	Units
Send SREQ/ or SACK/ assertion pulse width	t_1	90	-	ns
Send SREQ/ or SACK/ deassertion pulse width	t_2	90	-	ns
Receive SREQ/ or SACK/ assertion pulse width	t_1	90	-	ns
Receive SREQ/ or SACK/ deassertion pulse width	t_2	90	-	ns
Send data setup to SREQ/ or SACK/ asserted	t_3	55	-	ns
Send data hold from SREQ/ or SACK/ asserted	t_4	100	-	ns
Receive data setup to SREQ/ or SACK/ asserted	t_5	0	-	ns
Receive data hold from SREQ/ or SACK/ asserted	t_6	45	-	ns

SCSI-2 Fast Transfers (10.0 MB/sec, 40 MHz Clock)

Parameter	Symbol	Min	Max	Units
Send REQ/ or SACK/ assertion pulse width	t_1	35	-	ns
Send SREQ/ or SACK/ deassertion pulse width	t_2	35	-	ns
Receive SREQ/ or SACK/ assertion pulse width	t_1	24	-	ns
Receive SREQ/ or SACK/ deassertion pulse width	t_2	24	-	ns
Send data setup to SREQ/ or SACK/ asserted	t_3	33	-	ns
Send data hold from SREQ/ or SACK/ asserted	t_4	45	-	ns
Receive data setup to SREQ/ or SACK/ asserted	t_5	0	-	ns
Receive data hold from SREQ/ or SACK/ asserted	t_6	10	-	ns

SCSI-2 Fast Transfers (10.0 MB/sec, 50 MHz clock)

Parameter	Symbol	Min	Max	Units
Send SREQ/ or SACK/ assertion pulse width	t_1	35	-	ns
Send SREQ/ or SACK/ deassertion pulse width	t_2	35	-	ns
Receive SREQ/ or SACK/ assertion pulse width	t_1	24	-	ns
Receive SREQ/ or SACK/ deassertion pulse width	t_2	24	-	ns
Send data setup to SREQ/ or SACK/ asserted	t_3	33	-	ns
Send data hold from SREQ/ or SACK/ asserted	t_4	40**	-	ns
Receive data setup to SREQ/ or SACK/ asserted	t_5	0	-	ns
Receive data hold from SREQ/ or SACK/ asserted	t_6	10	-	ns

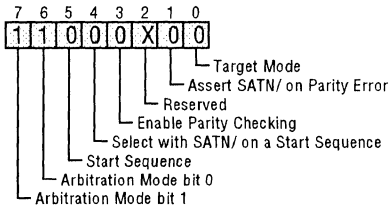
* *Transfer period bits (bits 6-4 in the SXFER register) are set to zero and the extra clock cycle of data setup bit (bit 7 in SCNTL1) is set.*

** *Analysis of system configuration is recommended due to reduced driver skew margin in differential systems.*

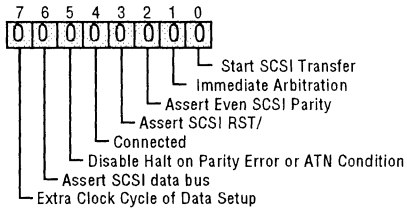
Note: *For fast SCSI, the TolerANT Enable bit (STEST3 bit 7) should be set.*

Appendix A
Register Summary

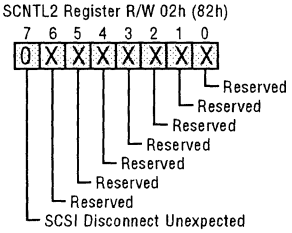
SCNTL0 Register R/W 00h (80h)



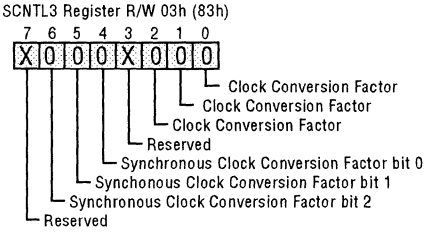
SCNTL1 Register R/W 01h (81h)



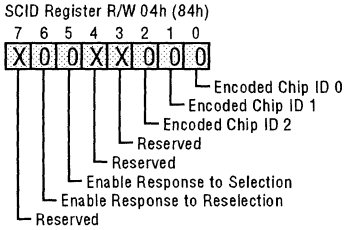
SCNTL2 Register R/W 02h (82h)



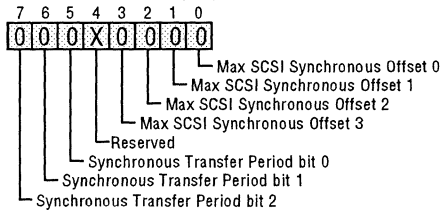
SCNTL3 Register R/W 03h (83h)



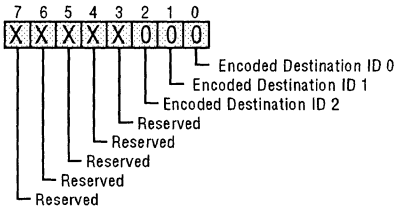
SCID Register R/W 04h (84h)



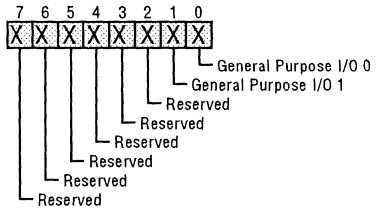
SXFER Register R/W 05h (85h)



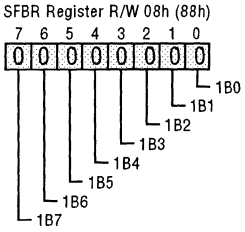
SDID Register R/W 06h (86h)



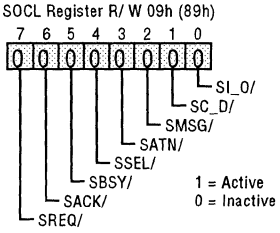
GPREG Register R/W 07h (87h)



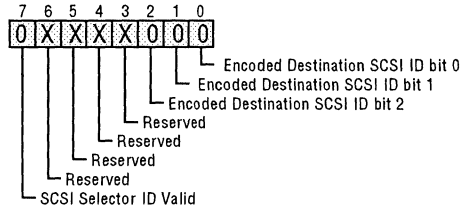
SFBR Register R/W 08h (88h)



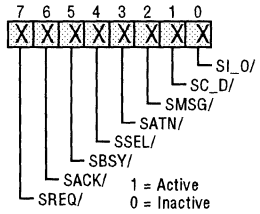
SOCL Register R/ W 09h (89h)



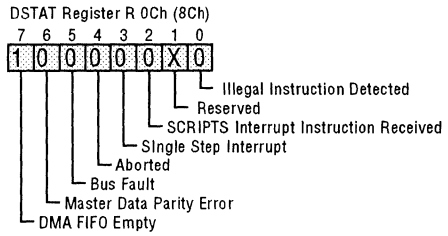
SSID Register R 0Ah (09h)



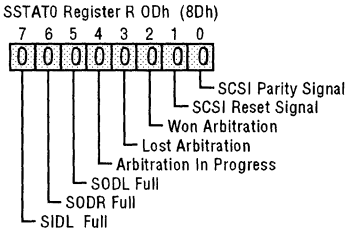
SBCL Register R 0Bh (8Bh)



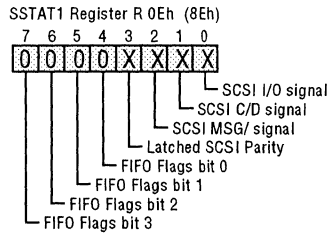
DSTAT Register R 0Ch (8Ch)



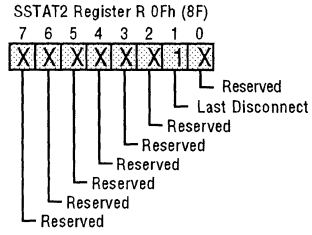
SSTAT0 Register R 0Dh (8Dh)



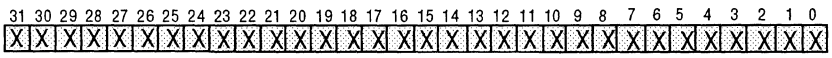
SSTAT1 Register R 0Eh (8Eh)



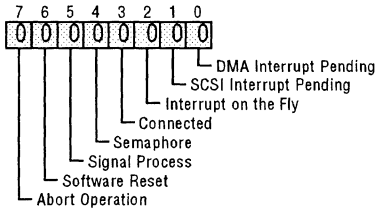
SSTAT2 Register R 0Fh (8F)



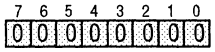
DSA Register R/W 10-13h (90-93h)



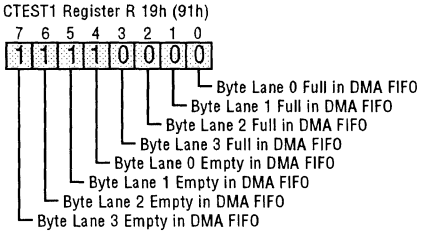
ISTAT Register R/W 14h (94h)



CTEST0 Register R/W 18h (98h)



CTEST1 Register R 19h (91h)



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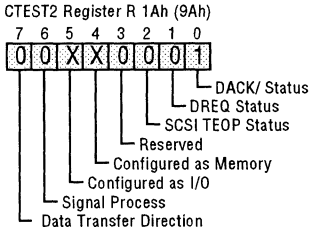

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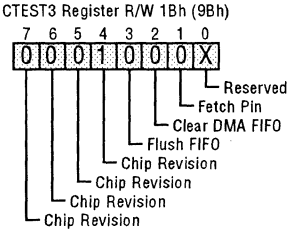

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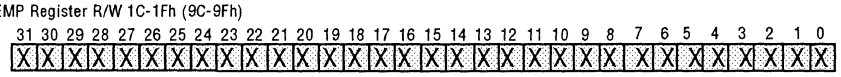

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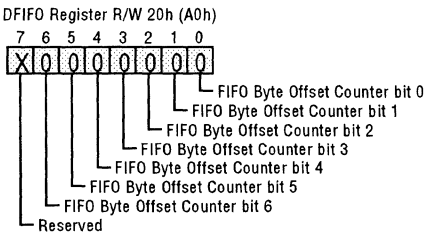

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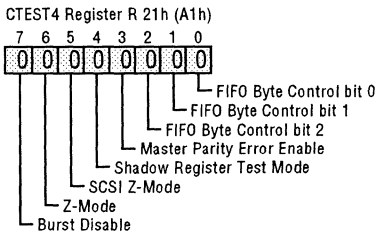

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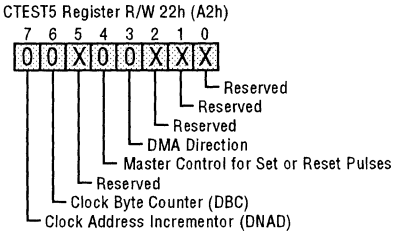

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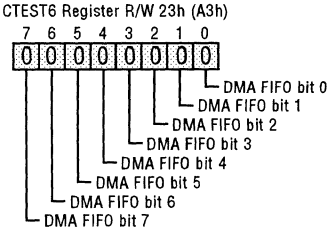

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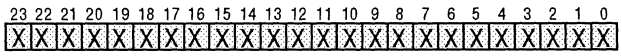

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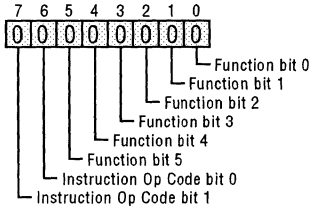

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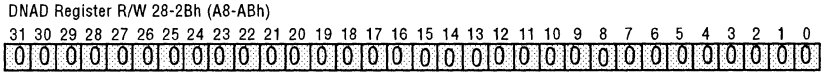

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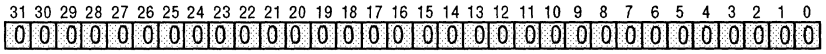

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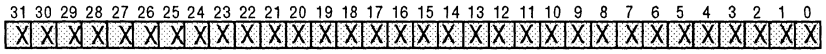

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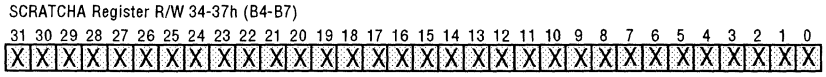

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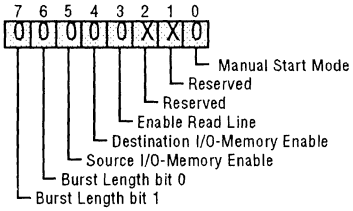

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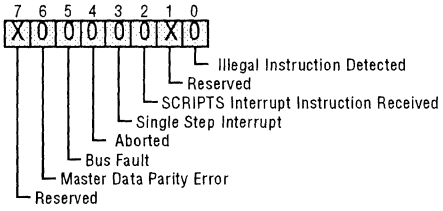

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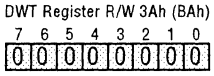

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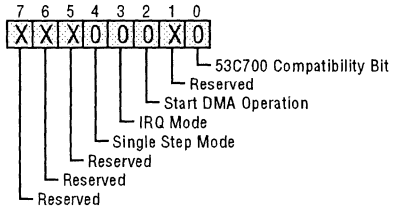

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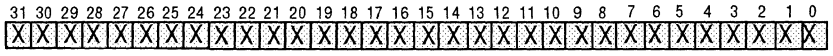

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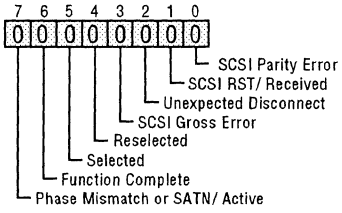

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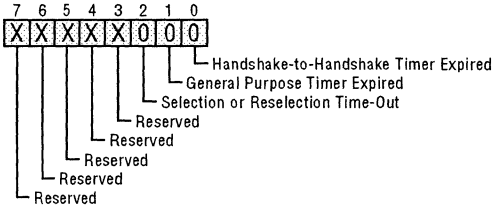

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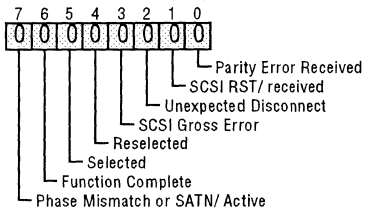

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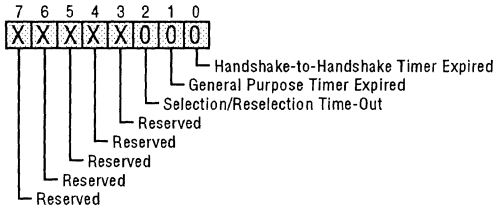

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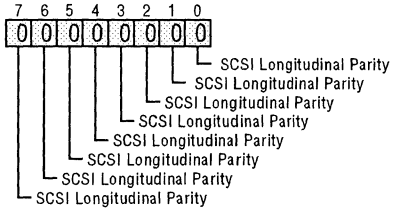

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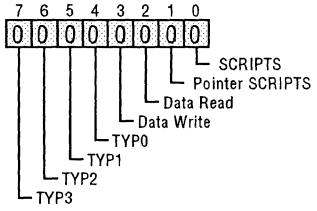

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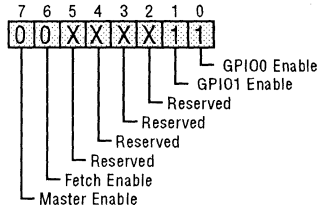

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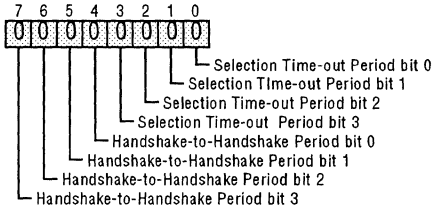

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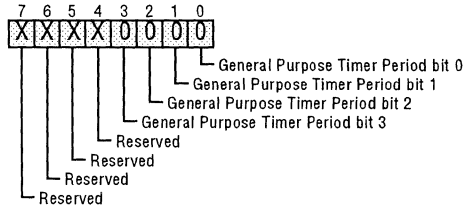

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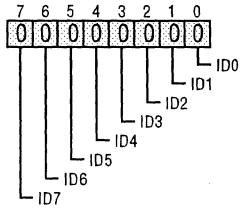

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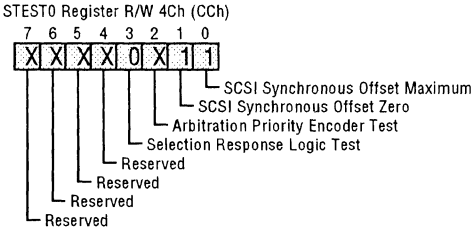

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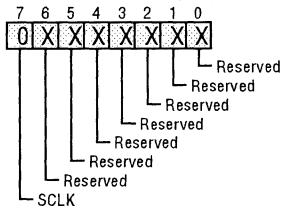

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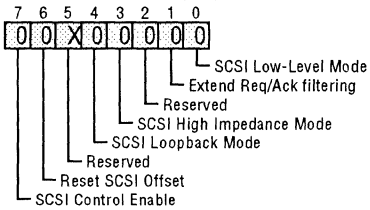

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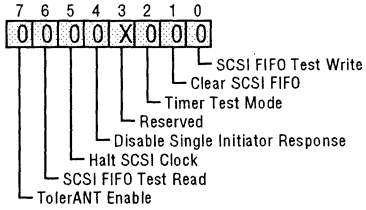

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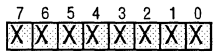

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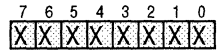

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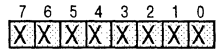
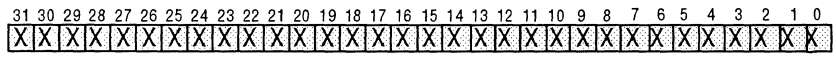
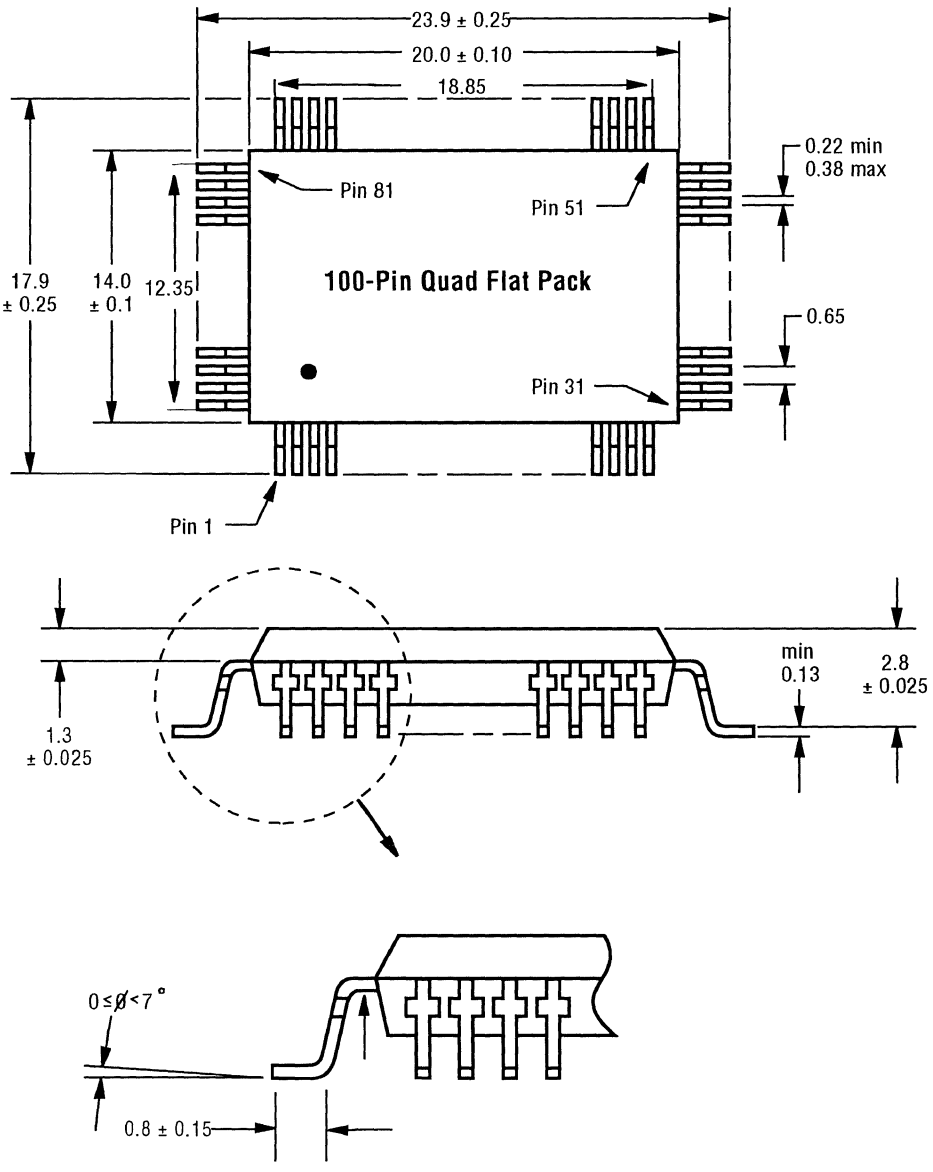


SCRATCHB Register R/W 5C-5Fh (DC-DFh)



Appendix B
Mechanical Drawing



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Index

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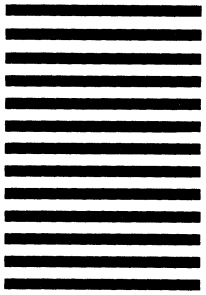

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