TECHNICAL MANUAL

LSI53C320 Ultra320 SCSI Bus Expander

Version 2.2

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LSI LOGIC®

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Preface

This manual provides a description of the LSI53C320 Ultra320 SCSI Bus Expander chip that supports all combinations of Single-Ended (SE) and Low Voltage Differential (LVD) SCSI bus conversions.

Audience

This manual assumes prior knowledge of the current and proposed SCSI standards. This manual also assumes that you are familiar with microprocessors and related support devices. The people who benefit from this book are

- engineers and/or managers who are evaluating the LSI53C320 for use in a system
- engineers who are designing the LSI53C320 into a system.

Related Publications

For background information, please contact:

LSI Logic World Wide Web Home Page
www.lsilogic.com

ANSI
www.ansi.org

Global Engineering Documents
www.global.ihs.com
Ask for document number X3.131-1994 (SCSI-2) or X3.253 *(SCSI-3 Parallel Interface)*

ENDL Publications
www.rahul.net/endl/
(408) 867-6630
Document names: *SCSI Bench Reference, SCSI Encyclopedia, SCSI Tutor*

Organization

This document has the following chapters and appendixes:

- Chapter 1, **Introduction**, contains the general information about the LSI53C320 product.
- Chapter 2, **Functional Descriptions**, describes the block diagram and operation of the LSI53C320.
- Chapter 3, **Signal Description**, provides signal descriptions for the LSI53C320.
- Chapter 4, **Specifications**, contains the electrical characteristics, timing diagrams, 272-PBGA diagram, and mechanical drawings for the LSI53C320.
- Appendix A, **Wiring Diagrams**, contains wiring diagrams for a typical LSI53C320 usage.
- Appendix B, **Glossary**, defines commonly used terms.

Revision Record

Date	Version	Remarks
2/2001	1.0	Advance/Confidential - includes 272 PBGA mechanical drawing
9/2002	1.1	Rearranged Chapters 2-3 into Chapters 2-4. Updated the Specifications chapter for G12 processes. Rewrote in active voice.
5/2003	2.0	Final Version for GCA. Added the serial EEPROM interface information. Added the maximum cable length information. Noted that QAS is not supported in the Ultra160 SCSI mode.
5/2003	2.1	Added disclaimer on the EPBGA mechanical drawing.
9/2003	2.2	Added ground to address lines in Figure 2.5 and Figure A.1.

Contents

Figures

Tables

Chapter 1
Introduction

This chapter describes the LSI53C320 Ultra320 SCSI Bus Expander and includes these sections:

1.1 General Description

The LSI53C320 Ultra320 SCSI Bus Expander is a single-chip solution allowing the extension of SCSI device connectivity and/or cable length limits. A SCSI bus expander couples bus segments without impact to the software, firmware, or SCSI protocol implementation. The LSI53C320 Ultra320 SCSI Bus Expander connects Single-Ended (SE) Ultra SCSI and Low Voltage Differential (LVD) Ultra320 SCSI peripherals together in any combination. The LSI53C320 *does not* support High Voltage Differential (HVD) mode.

The LSI53C320 supports any combination of the SE or LVD bus modes on either the A Side or B Side port. This provides the system designer with maximum flexibility in designing SCSI backplanes to accommodate any SCSI bus mode. Each bus side on the LSI53C320 has an independent RBIAS pin to allow for margining of each bus.

Figure 1.1 shows the two SCSI bus modes available on the A or B Side. LVDlink transceivers provide the multimode LVD or SE capability. The LSI53C320 operates as both an expander and a converter. In both SCSI Bus Expander and Converter modes, the LSI53C320 isolates the cable segments on the A Side and the B Side. This feature maintains the signal integrity of each cable segment.

Figure 1.1 LSI53C320 SCSI Bus Modes

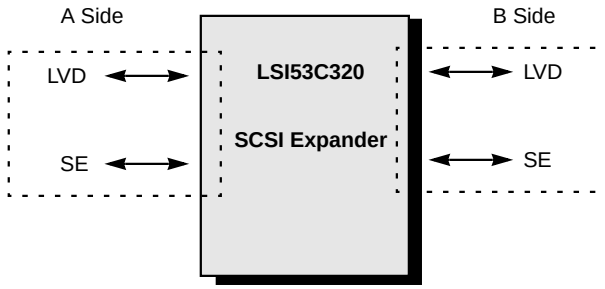


Table 1.1 shows the types of operational modes for the LSI53C320.

Table 1.1 Types of Operation

Signal Type	Speed
LVD to LVD	Up to Ultra320 SCSI
SE to SE	Up to Ultra SCSI
LVD to SE	Up to Ultra SCSI
SE to LVD	Up to Ultra SCSI

The LSI53C320 provides additional control capability through the pin-level isolation mode (Warm Swap Enable). This feature permits logical disconnection of the A Side bus or the B Side bus without disrupting SCSI transfers currently in progress. For example, users can logically disconnect the B Side bus while the A Side bus remains active.

The LSI53C320 is based on proven LSI Logic bus expander technology, which includes signal filtering along with retiming to maintain skew budgets. The LSI53C320 is independent of software. However, Domain Validation technology does require software control.

Note: The LSI53C320 does not support Quick Arbitration and Selection (QAS) while operating at Ultra160 SCSI rates.

1.2 Applications

The LSI53C320 supports

- server clustering environments
- expanders creating distinct SCSI cable segments that are isolated from each other

Configurations that use the LSI53C320 SCSI Bus Expander in the LVD to LVD mode allow the system designer to take advantage of the inherent cable distance, device connectivity, data reliability, and increased transfer rate benefits of LVD signaling with Ultra320 SCSI peripherals. Section 2.2.3, "Maximum Cable Lengths," discusses additional limits on the total SCSI cable length for systems operating at Ultra320 SCSI transfer rates.

Figure 1.2 shows how SCSI bus expanders couple bus segments with no impact on the SCSI protocol or software. Two LSI53C320 expanders configure three bus segments. Segment A is a point-to-point segment. Segments B and C are load segments and have at least 8 inches between every node. Table 1.2 shows the various distance requirements for each SCSI bus segment.

Figure 1.2 LSI53C320 Server Clustering

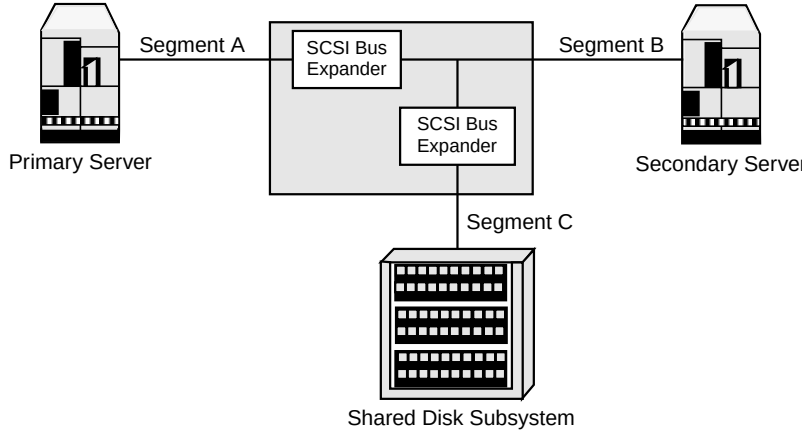


Table 1.2 SCSI Bus Length Limits in a Clustering Configuration

Segment	Mode	Length Limit
A	LVD (Ultra320 SCSI)	Up to 12 meters
	SE (Ultra SCSI)	Up to 3 meters[1]
B	LVD (Ultra320 SCSI)	Up to 12 meters
	SE (Ultra SCSI)	Up to 1.5 meters
C	LVD (Ultra320 SCSI)	Up to 12 meters
	SE (Ultra SCSI)	Up to 1.5 meters
A + B + C + D	Ultra320 SCSI (only)	Less than 29 meters[2]

1. The cable length can be more than 1.5 meters, since this is a point-to-point connection.
2. Refer to Section 2.2.3, "Maximum Cable Lengths," for more information on cable length limits in an Ultra320 SCSI environment.

Figure 1.3 shows cascading of the LSI53C320 to achieve four distinct SCSI segments. Segments A and D are point-to-point segments. Segments B and C are load segments and have at least 8-inch spacing between every node. Table 1.3 shows the distance requirements for each SCSI bus segment.

Figure 1.3 LSI53C320 SCSI Bus Device

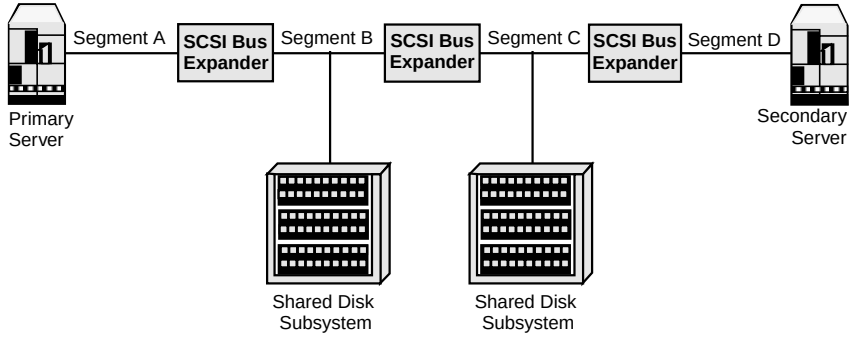


Table 1.3 SCSI Bus Length Limits

Segment	Mode	Length Limit
A, D	LVD (Ultra320 SCSI)	Up to 12 meters
	SE (Ultra SCSI)	Up to 1.5 meters
B, C	LVD (Ultra320 SCSI)	Up to 12 meters
	SE (Ultra SCSI)	Up to 1.5 meters
A + B + C + D	Ultra320 SCSI (only)	Less than 25 meters[1]

1. Refer to Section 2.2.3, "Maximum Cable Lengths," for more information on cable length limits in an Ultra320 SCSI environment.

1.3 Benefits of Ultra320 SCSI

The LSI53C320 SCSI Bus Expander supports Ultra320 SCSI. This interface expands the bandwidth of the SCSI bus to allow faster synchronous data transfers of up to 320 Mbytes/s. Ultra320 SCSI provides double the data transfer rate of the Ultra160 SCSI interface.

The LSI53C320 performs 16-bit, Ultra320 SCSI synchronous data transfers as fast as 320 Mbytes/s on the side of the device. This advantage is most noticeable in heavily loaded systems or large block size applications, such as video on-demand and image processing.

Ultra320 SCSI doubles both the data and clock frequencies from Ultra160 SCSI. Due to the increased data and clock speeds, Ultra320 SCSI introduces skew compensation and intersymbol interference (ISI) compensation. These new features simplify system design by resolving timing issues at the chip level. Skew compensation adjusts for timing differences between data and clock signals caused by cabling, board traces, and so on. ISI compensation enhances the first pulse after a change in state to ensure data integrity. The LSI53C320 performs skew compensation on the receiver side of the device and ISI compensation on the driver side of the device.

Ultra320 SCSI supports Cyclic Redundancy Check (CRC), which provides error checking code to detect the validity of data. CRC increases the reliability of data transfers by transferring four bytes of code along with data. CRC detects all single bit errors, two bits in error, or other error types within a single 32-bit range.

1.4 Benefits of SureLINK™ (Ultra320 SCSI Domain Validation)

SureLINK Domain Validation is a procedure that allows a host computer and target SCSI peripheral to negotiate and find the optimal transfer speed. This procedure improves overall reliability of the system by ensuring data integrity.

Domain Validation software ensures robust SCSI interconnect management and low risk Ultra320 SCSI implementations by extending the domain validation guidelines documented in the SPI-4 specifications. Domain validation verifies that the system is capable of transferring data at Ultra320 SCSI speeds, allowing the LSI53C320 to renegotiate to a lower data transfer speed and bus width if necessary. SureLINK Domain Validation is the software control for the domain validation manageability enhancements in the LSI53C320. SureLINK Domain Validation software provides domain validation management at boot time as well as during system operation.

SureLINK Domain Validation ensures robust system operation by providing three levels of integrity checking on a per-device basis: Basic (Level 1) with inquiry command; Enhanced (Level 2) with read/write buffer; and Margined (Level 3) with margining of drive strength and slew rates.

1.5 Benefits of LVDlink™ Technology

The LSI53C320 supports LVDlink technology for SCSI, a signaling technology that increases the reliability of SCSI data transfers over longer distances than those supported by SE SCSI technology. The low current output of LVD allows the I/O transceivers to be integrated directly onto the chip. For backward compatibility to existing SE devices, the LSI53C320 features multimode LVDlink transceivers that can switch between LVD and SE modes.

Some features of integrated LVDlink transceivers are listed below:

- supports SE or LVD modes
- allows greater device connectivity and longer cable length
- saves the cost of external differential transceivers
- provides a long-term performance migration path

1.6 Benefits of TolerANT® Technology

The LSI53C1320 features TolerANT technology, which provides active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation causes the SCSI Request, Acknowledge, Data, and Parity signals to be actively driven HIGH rather than passively pulled up by terminators.

TolerANT receiver technology improves data integrity in unreliable cabling environments where other devices would be subject to data corruption. TolerANT receivers filter the SCSI bus signals to eliminate unwanted transitions, without the long signal delay associated with RC-type input filters. This improved driver and receiver technology helps ensure correct clocking of data.

TolerANT technology increases noise immunity, balances duty cycles, and improves SCSI transfer rates. In addition, TolerANT SCSI devices do not cause glitches on the SCSI bus at power-up or power-down, which protects other devices on the bus from data corruption. When used with the LVDlink transceivers, TolerANT technology provides excellent signal quality and data reliability in real world cabling environments.

1.7 Features

The LSI53C320

- complies with the *SCSI Parallel Interface 4 (SPI-4)* Specifications
  - complies with SCSI Enhanced Parallel Interface (EPI) Specifications
  - supports Double Transition (DT) clocking
  - supports CRC in DT data phases
  - supports Domain Validation technology
  - supports Ultra320 SCSI Packetized Transfers
  - provides SCSI signal and timing calibration
  - is backward-compatible with previous revisions of the SCSI specification

- provides a flexible SCSI bus expander
- supports any combination of LVD or SE transceivers
- creates distinct SCSI bus segments that are isolated from each other
- uses integrated LVDlink transceivers for direct attachment to either LVD or SE bus segments
- operates as a SCSI Bus Expander or a SCSI Bus Converter
  - LVD to LVD (Ultra320 SCSI or Ultra160 SCSI)
  - SE to SE (up to Ultra SCSI)
  - LVD to SE (up to Ultra SCSI)
  - SE to LVD (up to Ultra SCSI)
- handles targets and initiators on either the A Side bus or B Side bus
- accepts any asynchronous or synchronous transfer speeds up to Ultra320 SCSI (for LVD to LVD mode only)
- supports dynamic addition/removal of SCSI bus segments using the isolation mode
- does not consume a SCSI ID
- propagates the RESET/ signal from one side to the other regardless of the SCSI bus state
- notifies initiator(s) of changes in transmission mode (SE/LVD) on A or B Side segments by using the SCSI bus RESET/
- provides a SCSI Busy LED driver for an activity indicator
- supports cascading of up to four LSI53C320s
- does not require software
- requires a 40 MHz Input Clock
- has a 272-pin Plastic Ball Grid Array package (PBGA).

Chapter 2
Functional Descriptions

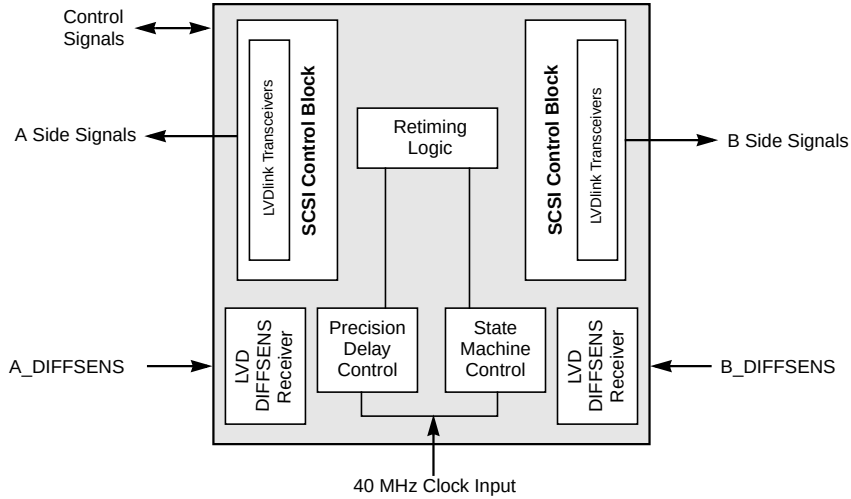
This chapter describes all signals, their groupings, and their functions. It includes these topics:

2.1 LSI53C320 Block Diagram Description

The LSI53C320 has no user programmable registers and does not require software. SCSI control signals control all LSI53C320 functions. Figure 2.1 shows a block diagram of the LSI53C320 device, which consists of these specific areas:

- A Side SCSI Control Block
  - LVD and SE Drivers and Receivers
- B Side SCSI Control Block
  - LVD and SE Drivers and Receivers
- Retiming Logic
- Precision Delay Control
- State Machine Control

Figure 2.1 LSI53C320 Block Diagram



The LSI53C320 passes data and parity from a source bus to a load bus. The source bus receives the SCSI signals from the initiator. The load bus transmits the SCSI signals to the target. The LSI53C320 retimes signals to maintain the signal skew budget from the source bus to the load bus.

2.1.1 SCSI Control Blocks

The SCSI A Side pins internally connect to the corresponding SCSI B Side pins. In the LVD/LVD mode, the A Side and B Side control blocks connect to SCSI devices and accept any asynchronous or synchronous Ultra320 SCSI data transfer rates. The SCSI control block supports TolerANT and LVDlink technologies to enable the SCSI bus transfers. For more information on these technologies, refer to Section 2.2.2.1, "SCSI Bus Modes."

2.1.2 Retiming Logic Block

As SCSI signals propagate through the LSI53C320, the chip retimes the signals to improve the SCSI timing. The Retiming Logic block contains numerous delay elements, which the Precision Delay Control block periodically calibrates to guarantee the output pulse widths, setup times, and hold times.

A synchronous negotiation between devices forms a nexus, for which the on-chip RAM stores information. This information remains in place until a chip reset, power down, or renegotiation. The nexus information enables the LSI53C320 to make accurate retiming adjustments.

2.1.3 Precision Delay Control Block

The Precision Delay Control block provides calibration information to the precision delay elements in the Retiming Logic block. Since the LSI53C320 voltage and temperature vary with time, the Precision Delay Control block periodically updates the delay settings in the Retiming Logic block to maintain constant and precise control over the bus timing.

2.1.4 State Machine Control Block

The State Machine Control block monitors the SCSI bus phases, the initiator and target device IDs, and various timing functions. This block controls the SCSI bus signal retiming and SCSI protocol implementation.

2.1.5 DIFFSENS Receiver Block

The LSI53C320 can operate with SE or LVD SCSI buses. The DIFFSENS Receiver block determine the operating mode of the SCSI bus by monitoring the voltage level on the DIFFSENS signal. For more information, refer to Section 2.2.2.1, “SCSI Bus Modes.”

2.2 Ultra320 SCSI Functional Description

The LSI53C320 supports Ultra320 SCSI. This interface expands the bandwidth of the SCSI bus to allow faster synchronous data transfers of up to 320 Mbytes/s. Ultra320 SCSI doubles the data transfer rate as compared to the Ultra160 SCSI interface. This section describes how the LSI53C320 implements the features in the SPI-4 draft specification.

2.2.1 Ultra320 SCSI Features

This section describes the Ultra320 SCSI features in the LSI53C320.

2.2.1.1 Double Transition (DT) Clocking

Ultra160 SCSI and Ultra320 SCSI implement DT clocking to provide speeds up to 80 megatransfers per second (megatransfers/s) for Ultra160 SCSI, and up to 160 megatransfers/s for Ultra320 SCSI. When implementing DT clocking, a SCSI device samples data on both the asserting and deasserting edge of REQ/ACK. DT clocking is only valid using an LVD SCSI bus.

2.2.1.2 Intersymbol Interference (ISI) Compensation

ISI Compensation uses paced transfers and precompensation to enable high data transfer rates. Ultra320 SCSI data transfers require the use of ISI Compensation.

Paced Transfers – The initiator and target must establish a paced transfer agreement that specifies the REQ/ACK offset and the transfer period before using this feature. Devices can only perform paced transfers during Ultra320 SCSI DT data phases. In paced transfers, the device sourcing the data drives the REQ/ACK signal as a free running clock. The transition of the REQ/ACK signal, either the assertion or the negation, clocks data across the bus. For successful completion of a paced transfer, the number of ACK transitions must equal the number of REQ transitions, and both the REQ and ACK lines must be negated.

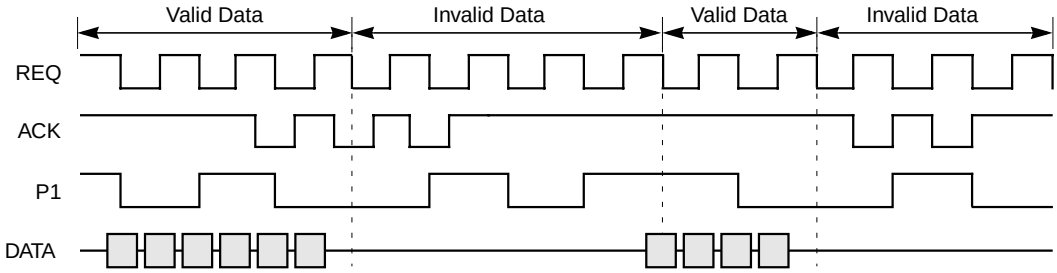
The P1 line indicates valid data in 4-byte quantities by using its phase. The transmitting device indicates the start of valid data state by holding the state of the P1 line for the first two data transfer periods. Beginning on the third data transfer period, the transmitting device continues the valid data state by toggling the state of the P1 line every two data transfer periods for as long as the data is valid. The transmitting device must toggle the P1 line coincident with the REQ/ACK assertion. This method provides a minimum valid data period of two transfer periods.

To pause the data transfer, the transmitting device reverses the phase of P1 by withholding the next transition of P1 at the start of the first two invalid data transfer periods. Beginning with the third invalid data transfer period, the transmitting device toggles the P1 line every two invalid data transfer periods until it sends valid data. The transmitting device returns to the valid data state by reversing the phase of the P1 line. The invalid data state must experience at least one P1 transition before returning to

the valid data state. This method provides a minimum invalid data period of four transfer periods.

Figure 2.2 provides a waveform diagram of paced data transfers and illustrates the use of the P1 line.

Figure 2.2 Paced Transfer Example

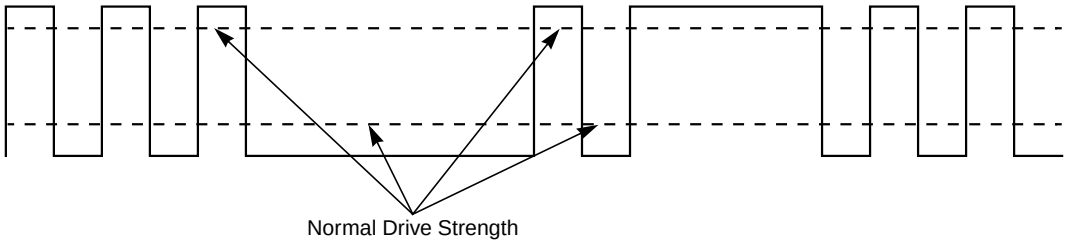


The LSI53C320 uses the PPR negotiation that the SPI-4 draft standard describes to establish a paced transfer agreement with the initiator on the source bus and the target on the load bus.

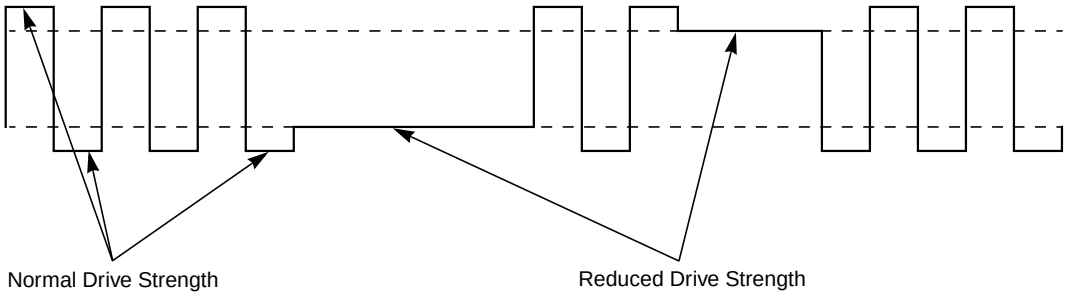
Precompensation – When transmitting in the Ultra320 SCSI mode, the LSI53C320 can use precompensation to adjust the strength of the REQ, ACK, parity, and data signals. When a signal transitions to HIGH or LOW, the LSI53C320 drives the signal at the signal drive strength for the first data transfer period, and then lowers the signal drive strength on the second data transfer period if the signal remains in the same state. The LSI53C320 maintains the lower signal drive strength until the signal again transitions HIGH or LOW. Figure 2.3 illustrates the drivers performance with precompensation enabled and disabled.

Figure 2.3 Example of Precompensation

a. Drivers with Precompensation Disabled



b. Drivers with Precompensation Enabled



2.2.1.3 Packetized Transfers

Packetized transfers are also referred to as information unit transfers. They reduce overhead on the SCSI bus by merging several of the SCSI bus phases.

2.2.1.4 Skew Compensation

The LSI53C320 provides a method to account for and control system skew between the clock and data signals. Skew compensation is only available when the device operates in the Ultra320 SCSI mode. The initiator-target pair uses the training sequences in the SPI-4 draft standard to determine the skew compensation. The LSI53C320 passes the training patterns between the initiator and target. The LSI53C320 stores the adjustment parameters and recalls them on subsequent connections with the given device pair (nexus).

2.2.1.5 Cyclic Redundancy Check (CRC)

Ultra320 SCSI and Ultra160 SCSI devices employ CRC as an error detection code during the DT Data phases. The LSI53C320 handles CRC as another data phase with the appropriate specific timing values.

2.2.1.6 LSI53C320 Requirements for Synchronous SCSI Negotiation

The LSI53C320 builds a table of information regarding devices on the bus in on-chip RAM. The LSI53C320 reads the PPR, Synchronous Data Transfer Request (SDTR), and Wide Data Transfer Request (WDTR) information for each device from the MSG bytes during negotiation.

For devices to communicate accurately through the LSI53C320 at Ultra320 SCSI rates, it is necessary for a complete asynchronous negotiation to occur between the initiator and target(s) prior to any synchronous data transfer. The LSI53C320 defaults to Ultra SCSI rates when a valid negotiation between the initiator and target does not occur.

2.2.2 SCSI Bus Interface

This section describes the SCSI bus interfaces on the LSI53C320.

2.2.2.1 SCSI Bus Modes

To support greater device connectivity and longer SCSI cables, the LSI53C320 features LVDlink technology, the LSI Logic implementation of multimode LVD SCSI. The LVDlink transceivers can operate in the LVD or SE modes.

The voltage levels on the A_DIFFSENS and B_DIFFSENS signals determine the SCSI bus mode. The LSI53C320 DIFFSENS receivers detect the voltage level on the A Side or B Side DIFFSENS lines independently. The LSI53C320 does not change the present signal mode until it continuously senses a new DIFFSENS voltage level for 100 ms. Table 2.1 shows the voltages on the DIFFSENS lines.

Table 2.1 DIFFSENS Voltage Levels

Mode	Voltage
SE	–0.35 to +0.5
LVD	+0.7 to +1.9

When the DIFFSENS voltage selects SE mode, the LSI53C230 internally ties the plus signals to ground and the minus SCSI signals become the SE input/outputs. When the DIFFSENS voltage selects LVD mode, the plus and minus signals are the differential signal pairs.

Any dynamic mode change (SE-to-LVD or LVD-to-SE) on a bus segment is a significant event, and the initiator must determine if the new bus mode meets the requirements for the bus segment. The LSI53C320 supports dynamic transmission mode changes by notifying the initiator(s) of changes in the transmission mode with a SCSI bus RESET/. The DIFFSENS line detects a valid mode switch on a bus segment. After the DIFFSENS state is continuously present for 100 ms, the LSI53C320 generates a SCSI reset on the bus opposite the bus on which the transmission mode change occurred. This reset informs initiators residing on the opposite bus segment of the change in the transmission mode. The initiator(s) then renegotiates synchronous transfer rates with each device on that segment.

If the LSI53C320 detects the HVD mode on a SCSI bus segment, the LSI53C320 3-states its outputs.

2.2.2.2 SCSI Termination

The terminator networks pull signals to an inactive voltage level and match the impedance seen at the end of the cable with the characteristic impedance of the cable. Install terminators at the ends of each SCSI segment, and only at the ends; *all SCSI buses must have exactly two terminators.*

2.2.3 Maximum Cable Lengths

The electrical length of a bus is the time required for round-trip signal propagation between bus ends. This section discusses the maximum electrical and physical cable lengths when cascading LSI53C320

expanders. For Ultra320 SCSI environments, the information in this section takes precedence over the information in Section 1.2, “Applications.”

2.2.3.1 Maximum Electrical Cable Length

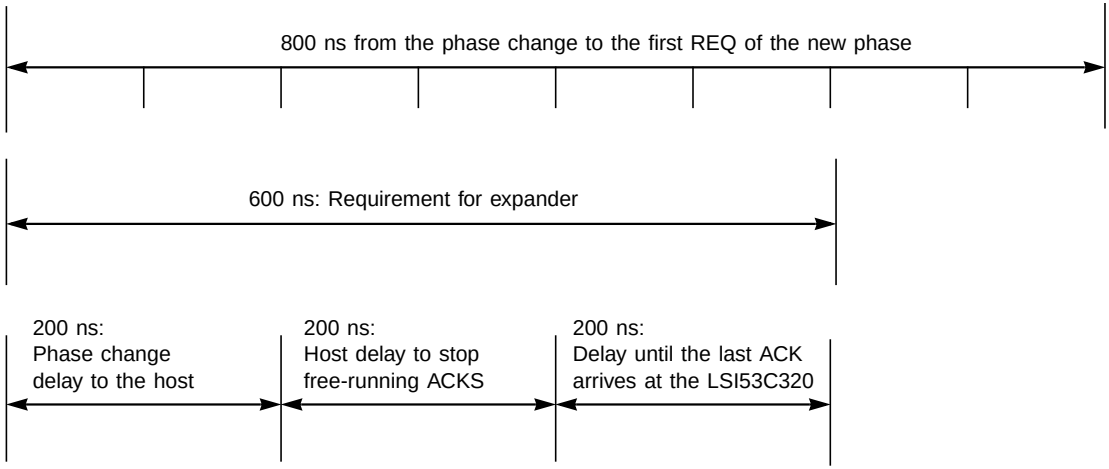
The *SCSI Parallel Interface-4* (SPI-4) standard states that the electrical length between the hosts arbitrating on different ends of a SCSI bus must not exceed 800 nanoseconds (ns), when operating at Ultra320 SCSI data transfer rates. Due to this constraint, LSI Logic specifies that a maximum of four expanders can be cascaded on a SCSI bus.

There are additional electrical length constraints imposed by the SPI-4 standard. When ending a paced transfer from DT_{OUT} to any other phase, the target must wait 800 ns before issuing a REQ. The SPI-4 standards allows 200 ns for the host to recognize the phase change and stop the free running ACK. This requirement reduces the electrical length of the bus to 600 ns.

Because the expander resides in the middle of the bus and retimes data to the active free running clock, the expander must switch its internal logic from ACK to REQ. The expander performs this switch 600 ns after detecting the phase change. Activity on the ACK or REQ line during this period adversely affects the expander. This reduces the electrical length of the bus to 400 ns.

Figure 2.4 illustrates the bus timing. Assuming a 400 ns electrical length and that the host uses the full 200 ns time allotment, the last free running ACK from the host returns to the expander at the 600 ns mark.

Figure 2.4 Electrical Cable Lengths at Ultra320 SCSI Speeds



2.2.3.2 Maximum Physical Cable Length

Table 2.2 provides information concerning the maximum physical cable length when operating the LSI53C320 at Ultra320 SCSI transfer rates.

Table 2.2 Total Cable Length for Ultra320 SCSI Using the LSI53C320

Number of Cascaded Expanders	Maximum Physical Cable Length in Meters (m)	Comments
1	37	LSI Logic recommends limiting the 25 m point-to-point bus cable length to 20 m and the fully-loaded bus cable length to 12 m.
2	29	
3	25	
4	21	

The SPI-4 standard allows a maximum point-to-point physical cable length of 25 m and a maximum fully loaded physical cable length 12 m. This limits the total physical cable length to 37 m. To allow for board capacitance and signal propagation through the expander, LSI Logic recommends limiting the point-to-point physical cable length to 20 m. This limits the total physical cable length to 32 m.

Table 2.2 provides the total maximum cable length depending on the number of expanders that are cascaded on the bus. As long as the total cable length between expanders, hosts, and drives does not exceed these limits, the 400 ns electrical cable length requirement will be met.

In designs that use a back plane, designers must additionally consider the signal propagation velocity through the back plane to ensure that the 400 ns electrical cable length requirement is met.

2.3 SCSI Signal Processing

Figure 3.1 shows the LSI53C320 signal grouping. The following sections describes the signal processing for the LSI53C320 SCSI signals. Refer to Section Chapter 3, “Signal Description,” and Section Chapter 4, “Specifications,” for more information on individual signals.

2.3.1 Data and Data Parity Signals

The LSI53C320 passes the data and parity signals from the source bus to the load bus and provides the necessary edge shifting to guarantee the skew budget for the load bus. Either side of the LSI53C320 can act as the source bus or the load bus. The side that the LSI53C320 receives signals on is the source bus. The side that the LSI53C320 drives signals on is the load bus. These steps describe the LSI53C320 data processing:

1. The receiver logic accepts the data. Once the clock signal (REQ/ACK) is received, the LSI53C320 gates the data from the receiver latch.
2. The LSI53C320 holds the asserting edge for a specified time to prevent signal bounce. The input signal controls the duration of the hold time.
3. The LSI53C320 samples the bus using a latch, which provides a stable data window for the load bus.
4. In the last stage, the LSI53C320 3-states the outputs.
5. To assure that the LSI53C320 does not sample its own signals, the LSI53C320 delays sampling until a specified time after the last signal deassertion.

2.3.2 Select Signal

A_SSEL and B_SSEL perform bus arbitration and selection. When a bus asserts the SSEL signal, the LSI53C320 propagates the signal assertion

to the other bus. When both buses assert SSEL simultaneously, A_SSEL takes precedence over B_SSEL. The SSEL output has a pull-down control for an open collector driver. The following steps describe the select control signal process:

1. If the LSI53C320 is driving the SSEL signal, the LSI53C320 blocks the SSEL input signal on the other bus.
2. The LSI53C320 filters the leading edge of the SSEL signal to ensure that the output does not switch for a specified time after the leading edge. The duration of the input signal determines the duration of the output signal.
3. To assure that the LSI53C320 does not sample its own signals, the LSI53C320 delays sampling until a specified time after the last signal deassertion.

2.3.3 Busy Signal

The controller propagates the A_SBSY and B_SBSY signals from the source bus to the load bus. The following steps describe the busy control signal process:

1. The LSI53C320 filters the leading edge of the SBSY signal. The LSI53C320 holds the assertion edge for a specified time to prevent signal bounce. The duration of the input signal determines the duration of the output signal.
2. To assure that the LSI53C320 does not sample its own signals, the LSI53C320 delays sampling until a specified time after the last signal deassertion.

2.3.4 Reset Signal

The controller passes the A_SRST and B_SRST signals from the source to the load bus. This output has pull-down control for an open collector driver. The following steps describe the processing of the reset signals:

1. If the LSI53C320 is driving the SRST signal, the LSI53C320 blocks the SRST input signal on the other bus.
2. The LSI53C320 filters the leading edge of the signal to ensure that the output does not switch during a specified time after the leading

edge. The duration of the input signal determines the duration of the output signal.

3. To assure that the LSI53C320 does not sample its own signals, the LSI53C320 delays sampling until a specified time after the last signal deassertion.

2.3.5 Request and Acknowledge Signals

The SREQ and SACK signal paths contain controls that guarantee minimum pulse widths, filter edges, and perform signal retiming.

When performing DT clocking, the LSI53C320 filters both the leading and trailing signal edges. When performing ST clocking, the LSI53C320 filters only the leading signal edge. The SREQ and SACK paths are from the A Side to the B Side and from the B Side to the A Side. The following steps describe the SREQ and SACK signal processing:

1. The LSI53C320 senses the asserted input signal and forwards it to the next stage if the direction control permits. The LSI53C320 state machine develops the direction controls from the sequence of the bus control signals.
2. The LSI53C320 filters the leading edge of the input and output signal to ensure that the signal does not switch during the specified hold time after the leading edge. The duration of the input signal determines the duration of the output signal **after the hold time**. The LSI53C320 guarantees a minimum pulse width.
3. The LSI53C320 passes the signal to the load bus if the signal is not a data clock. If SREQ or SACK is a data clock, it delays the leading edge to improve data output setup times. The duration of the input signal determines the duration of the output signal.
4. The LSI53C320 filters the trailing edge of the signal to prevent signal bounce after the signal deasserts. The LSI53C320 deasserts the output signal at the first deasserted edge of the input signal.
5. In the last stage, the LSI53C320 3-states the outputs.
6. To assure that the LSI53C320 does not sample its own signals, the LSI53C320 delays sampling until a specified time after the last signal deassertion.

2.3.6 Control/Data, Input/Output, Message, and Attention Signals

The following steps describe the processing of these signals:

1. If the LSI53C320 is driving the signal, the LSI53C320 blocks the input signal on the other bus.
2. The LSI53C320 filters the leading edge of the signal to ensure that the output does not switch for a specified time after the leading edge. The duration of the input signal determines the duration of the output signal.
3. In the last stage, the LSI53C320 3-states the outputs.
4. To assure that the LSI53C320 does not sample its own signals, the LSI53C320 delays sampling until a specified time after the last signal deassertion.

2.4 Internal Control Descriptions

This section provides information about self-calibration, delay line structures, and busy filters.

2.4.1 Self-Calibration

The LSI53C320 triggers self-calibration to adjust for variations in temperature, process, and voltage every second during bus free states.

2.4.2 Delay Line Structures

The signal and control interfaces for bus to bus transfers require fixed delay functions. The LSI53C320 uses programmable delay lines to implement the delay functions. Multiplexers select the incremental points in the delay chain. The LSI53C320 self-calibration manages the effects of temperature and voltage changes.

2.4.2.1 Data Path

The data path through the LSI53C320 includes two levels of latches. The first latch in the data path is located in the receiver and the REQ/ACK input clock and generates a hold. This latch holds the received data to capture incoming data that might have minimal setup and hold times. A

second latch is located on the transmitter side of the LSI53C320 and holds the data to enable optimal signal transmission on the isolated bus. This latch provides a regenerated clock signal and the maximum setup and hold times.

The data path also provides a timer for each data bit. This timer protects against reception from a target bus for a nominal 30 ns after the driver deasserts.

2.4.2.2 REQ/ACK Retiming

The LSI53C320 edge filters the REQ/ACK input clock signals. The chip also stretches these signals to their minimum timing values to avoid glitches. In double transition clocking, the chip filters both the leading and trailing edges. In single transition clocking, the chip filters only the leading edge. The filters remove noise within the initial signal transition. The current transmission speed determines the filter time values.

2.4.3 Busy Filters

The busy control signal passes from source to load bus. The current state of the SCSI bus determines the filtering. This filter provides a synchronized leading edge signal that is not true until the input signal stabilizes. The trailing edge occurs within several nanoseconds of the input deasserting. When the BSY signal asserts before and after the SEL signal, the filter is on.

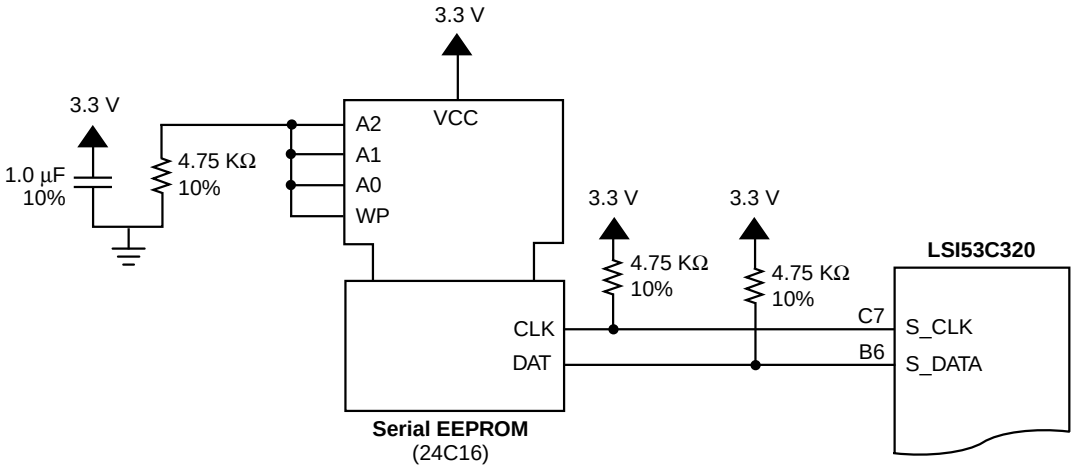
2.5 Serial EEPROM Connection

The serial EEPROM connects to the LSI53C320 through a 2-wire serial interface. SP_CLK (Ball C7) on the LSI53C320 connects to the serial EEPROM clock line and SP_DAT (Ball B6) on the LSI53C320 connects to the serial EEPROM data line. These two lines are pulled HIGH through resistors.

The LSI53C320 produces the 50 kHz SP_CLK for downloading data from the serial EEPROM. The LSI53C320 3-states the SP_CLK and SP_DAT lines during chip reset and after a successful download. The LSI53C320 continues to drive SP_CLK LOW if the download is unsuccessful, which enables detection of download failure by monitoring this signal.

LSI Logic recommends using a 3.3 V, 2 Kbyte (256 x 8 bit) serial EEPROM that can accept a 50 KHz clock. Figure 2.5 provides a sample layout.

Figure 2.5 Serial EEPROM Connection



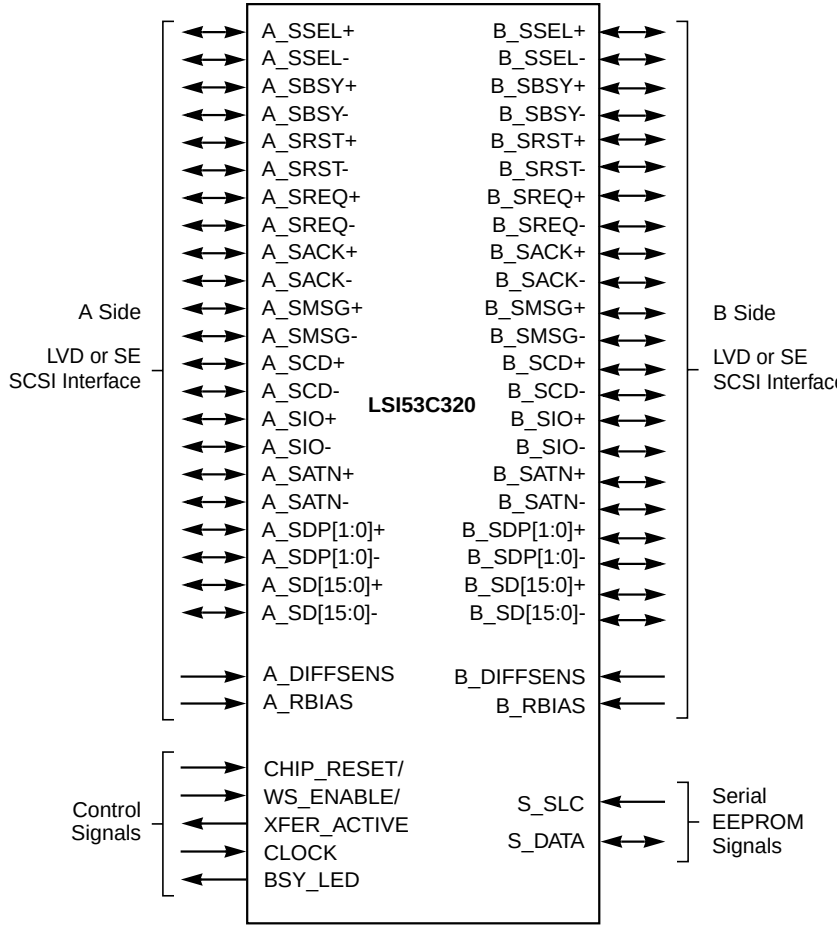
Chapter 3
Signal Description

This chapter provides the signal descriptions and electrical characteristics for the LSI53C320. It includes these topics:

3.1 Signal Grouping

Figure 3.1 illustrates the LSI53C320 signal grouping.

Figure 3.1 LSI53C320 Functional Signal Grouping



3.2 SCSI Interface Signals

Table 3.1 describes the SCSI interface signals for the A Side of the LSI53C320.

Table 3.1 SCSI A Side Interface Signals

Signal Name	BGA Pin	Type	Description
A_SSEL+ A_SSEL-	G1 H3	I/O	A Side Select signal.
A_SBSY+ A_SBSY-	K3 K1	I/O	A Side Busy signal.
A_SRST+ A_SRST-	J3 J2	I/O	A Side Reset signal.
A_SREQ+ A_SREQ-	F2 F1	I/O	A Side Request signal.
A_SACK+ A_SACK-	J1 K2	I/O	A Side Acknowledge signal.
A_SMSG+ A_SMSG-	H2 H1	I/O	A Side Message signal.
A_SCD+ A_SCD-	G3 G2	I/O	A Side Control and Data signal.
A_SIO+ A_SIO-	E1 F3	I/O	A Side Input and Output signal.
A_SATN+ A_SATN-	L2 L3	I/O	A Side Attention signal.
A_SDP[1:0]+ A_SDP[1:0]-	V2, M1 W1, M2	I/O	A Side Data Parity signals.
A_SD[15:0]+ A_SD[15:0]-	W3, W4, Y3, V5, B1, D2, C1, E3, N1, N3, P2, P3, T1, T2, T3, V1, Y2, V4, Y4, W5, C2, D3, D1, E2, N2, P1, R1, R2, R3, U1, U2, U3	I/O	A Side Data signals.
A_DIFFSENS	B3	I	A Side Differential Sense signal.
A_RBIAS	M3	RBIAS	A Side current control. Attach a 10 kΩ pull-up resistor on RBIAS to provide the correct bias level.

Table 3.2 describes the SCSI interface signals for the B Side of the LSI53C320.

Table 3.2 SCSI B Side Interface Signals

Signal Name	Pin	Type	Description
B_SSEL+ B_SSEL-	H19 H18	I/O	B Side Select signal.
B_SBSY+ B_SBSY-	F18 E19	I/O	B Side Busy signal.
B_SRST+ B_SRST-	F20 G18	I/O	B Side Reset signal.
B_SREQ+ B_SREQ-	J20 J19	I/O	B Side Request signal.
B_SACK+ B_SACK-	F19 E20	I/O	B Side Acknowledge signal.
B_SMSG+ B_SMSG-	G20 G19	I/O	B Side Message signal.
B_SCD+ B_SCD-	J18 H20	I/O	B Side Control and Data signal.
B_SIO+ B_SIO-	K19 K18	I/O	B Side Input and Output signal.
B_SATN+ B_SATN-	D20 E18	I/O	B Side Attention signal.
B_SDP[1:0]+ B_SDP[1:0]–	A14, D19 C13, C20	I/O	B Side Data Parity signals.
B_SD[15:0]+, B_SD[15:0]–	B13, C12, A12, C11, N19, M18, M20, L18, C19, A19, B17, A18, C16, A16, B15, C14 A13, B12, B11, A11, N20, M19, L19, L20, B20, B18, C17, A17, B16, C15, A15, B14	I/O	B Side Data signals.
B_DIFFSENS	B2	I	B Side Differential Sense signal.
B_RBIAS	D18	RBIAS	LVD current control. Attach a 10 kΩ pull-up resistor on RBIAS to provide the correct bias level.

3.3 Interface Control Signals

Table 3.3 describes the interface control signals for the LSI53C320. The LSI53C320 requires an external POR, which is implemented using the CHIP_RESET/ signal. Figure A.1 provides an example external POR circuit.

Table 3.3 Chip Interface Control Signals

Signal Name	Pin	Type	Description
CHIP_RESET/	C10	I	The active LOW **Master Reset** signal provides a general purpose chip reset that forces the internal elements of the LSI53C320 to a known state. Asserting this signal places the LSI53C320 state machine in an idle state and places all controls in a passive state. The minimum CHIP_RESET/ asserted pulse width is 100 ns.
WS_ENABLE/	A7	I	The Active LOW **Warm Swap Enable** signal enables and disables SCSI transfers through the LSI53C320. The WS_ENABLE/ input removes the chip from an active bus without disturbing the current SCSI transaction. When Warm Swap Enable asserts, the LSI53C320 3-states the SCSI signals after it detects the next bus free state. The LSI53C320 no longer passes on signals until the WS_ENABLE/ pin deasserts and both SCSI buses enter the Bus Free state.
XFER_ACTIVE	A8	O	The **Transfer Active** signal enables and disables SCSI transfers through the LSI53C320. The LSI53C320 asserts this signal when the chip is active to indicate that the chip completed its internal testing, the SCSI bus has entered a bus free state, or that SCSI traffic can now pass from one side of the chip to the other side of the chip. The LSI53C320 deasserts this signal to detect a Bus Free state due to the WS_ENABLE/ signal being LOW. Deasserting this signal disables transfers through the device.
CLOCK	A9	I	**CLOCK** provides the 40 MHz oscillator input to the LSI53C320. It is the clock source for the protocol control state machines and timing generation logic. The bus signal transfer paths do not use this clock.
BSY_LED	B9	O	The **Busy LED** signal provides an 8 mA SCSI activity LED output. The LSI53C320 asserts this signal to indicate SCSI bus activity.

3.4 Serial EEPROM Signals

Table 3.4 describes the serial EEPROM signals for the LSI53C320.

Table 3.4 Serial EEPROM Signals

Signal Name	Pin	Type	Description
S_CLK	C7	O	The LSI53C320 uses the **serial EEPROM clock** signal to provide the 50 kHz clock for downloading the serial EEPROM data.
S_DATA	B6	I/O	The LSI53C320 uses the **serial EEPROM data** signal to download data from the serial EEPROM.

3.5 Power and Ground Signals

Table 3.5 describes the power and ground signals for the LSI53C320.

Table 3.5 Power and Ground Pins

Signal Name	Pin	Type	Description
VDD_{SCSI}[1]	D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15	I	Power supplies to the SCSI bus I/O pins.
VDD_{CORE}[2]	A2, B19, D10, K17, L4, U11, W2, W19	I	Power supplies to the CORE logic.
VDD_{IO}[3, 4]	C8	I	Power supplies to the I/O logic.
VSS_{SCSI}	A1, D4, D8, D13, D17, H4, H17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, U4, U8, U13, U17	I	Ground ring.
VSS_{CORE} [4]	A20, B10, C3, K20, L1, Y1, Y11, Y20	I	Ground ring.
VSS_{IO}	B7	I	Ground ring.

Table 3.5 Power and Ground Pins (Cont.)

Signal Name	Pin	Type	Description
NC	A3, A5, A6, A10, B8, C4, C6, C9, C18, D5, D7, D9, D12, D14, D16, E4, E17, G4, G17, J4, J17, M4, M17, N18, P4, P17, P18, P19, P20, R18, R19, R20, T4, T17, T18, T19, T20, U5, U7, U9, U12, U14, U16, U18, U19, U20, V3, V6, V7, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, V19, V20, W6, W7, W8, W9, W10, W11, W12, W13, W14, W15, W16, W17, W18, W20, Y5, Y6, Y7, Y8, Y9, Y10, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19	N/A	No Connections.

1. VDD_{SCSI} must be supplied with 3.3 V.
2. VDD_{CORE} pins must be supplied 1.8 V.
3. VDD_{IO} must be supplied with 3.3 V.
4. The VDD_{IO} pin must always power down before the VDD_{CORE} pin.

3.6 Test Signals

Table 3.6 lists the LSI53C320 test signals and their associated ball number. These test signals are for use by LSI Logic only.

Note: Connect the tests signals to either test point or a header for debugging purposes.

Table 3.6 Test Signals for LSI Logic Only

Signal	Ball
TEST_3	A4
TEST_4	C5
TEST_5	B5
TEST_6	B4

3.7 Signal Layout Considerations

The pinout of the LSI53C320 package ensures that each signal requires the shortest possible trace length. Use active termination for the bus connections to the LSI53C320. When choosing an active terminator, set the load capacitance of the terminator as low as possible.

LSI Logic recommends the use of strip line. Strip line allows tighter connector placement, which reduces the noise effects from both internal and external sources. On long trace runs, such as those in a backplane environment, snaking of traces to equalize their length is appropriate. Place the decoupling capacitors as close as possible to the via attached to each corresponding voltage plane.

Chapter 4
Specifications

This chapter provides the electrical and environmental specifications for the LSI53C320 and consists of these topics:

4.1 Electrical Characteristics

This section provides the electrical characteristics of the LSI53C320.

4.1.1 DC Characteristics

Table 4.1 through 4.10 give the current and voltage specifications. Figure 4.1 and Figure 4.2 illustrate the driver and receiver schematics.

Table 4.1 Absolute Maximum Stress Ratings[1]

Symbol	Parameter	Min	Max	Unit	Test Conditions
T_{STG}	Storage Temperature	–40	125	˚C	–
$V_{DD\text{-}Core}$	Supply Voltage	–0.3	2.2	V	–
$V_{DD\text{-}IO}$	IO Supply Voltage	–0.3	3.9	V	–
V_{IN}	Input Voltage	–0.5	V_{DD} + 0.5	V	–
I_{LP}	Latch-up current	±150	–	mA	–2 V < VPIN < 8 V
ESD	Electrostatic Discharge	–	2000	V	MIL-STD 883C, Method 3015.7

1. Stresses beyond those listed can damage the device. These are stress ratings; functional operation at or beyond these values is not implied.

Table 4.2 Operating Conditions[1]

Symbol	Parameter	Min	Nominal	Max	Unit	Test Conditions
$V_{DD\text{-}Core}$	Supply voltage	1.71	1.80	1.89	V	–
$V_{DD\text{-}IO}$	I/O Supply voltage	3.13	3.30	3.47		
$I_{DD\text{-}Core}$	Core and Analog Supply Current (Dynamic)	–	275	360	mA	–
$I_{DD\text{-}IO}$	I/O Supply Current (Dynamic)	–	450	590	mA	RBIAS = 10 kΩ 1% V_{DD} = 3.3 V
I_{LP}[2]	Latch-up Current	150	–	–	mA	–
T_j	Junction Temperature	–	60	115	˚C	–
T_A	Operating free air	0	–	70	˚C	–
θ_{JA}	Thermal resistance (junction to ambient air)	–	–	16.4	˚C/W	–

1. Conditions that exceed the operating limits can cause the device to function incorrectly.
2. SCSI pins only.

Table 4.3 LVD Driver SCSI Signals—SD[15:0]±, SDP[1:0]±, SCD±, SIO±, SMSG±, SREQ±, SACK±, SBSY±, SATN±, SSEL±, SRST±[1]

Symbol	Parameter	Min	Max	Units	Test Conditions
I_O+	Source (+) current	9.6	14.4	mA	Asserted state
I_O–	Sink (–) current	–9.6	–14.4	mA	Asserted state
I_O+	Source (+) current	–6.4	–9.6	mA	Negated state
I_O–	Sink (–) current	6.4	9.6	mA	Negated state
I_{OZ}	3-state leakage	–20	20	µA	–

1. V_{CM} = 0.7 – 1.8 V, R_{bias} = 10 kΩ.

Figure 4.1 LVD Driver

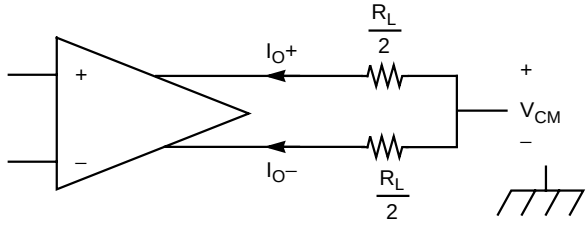


Table 4.4 LVD Receiver SCSI Signals—SD[15:0]±, SDP[1:0]±, SCD±, SIO±, SMSG±, SREQ±, SACK±, SBSY±, SATN±, SSEL±, SRST±[1]

Symbol	Parameter	Min	Max	Units	Test Conditions
V_I	LVD receiver voltage asserting	60	–	mV	–
V_I	LVD receiver voltage negating	–	–60	mV	–

1. V_{CM} = 0.7 – 1.8 V.

Figure 4.2 LVD Receiver

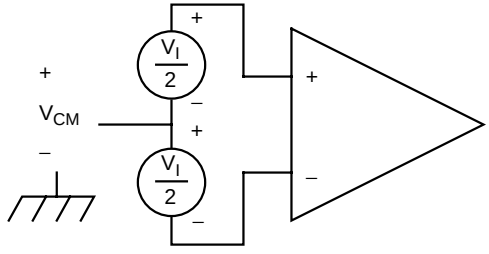


Table 4.5 Bidirectional SCSI Signals—SD[15:0]/, SDP[1:0]/, SREQ/, SACK/, SD[15:0]±, SDP[1:0]±, SREQ±, SACK±

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	1.9	V_{DD}	V	–
V_{IL}	Input low voltage	V_{SS}	1.0	V	–
V_{OH}[1]	Output high voltage	2.0	V_{DD}	V	I_{OH} = 7.0 mA
V_{OL}	Output low voltage	V_{SS}	0.5	V	48 mA
I_{OZ}	3-state leakage	–10	10	µA	–

1. TolerANT active negation enabled.

Table 4.6 Bidirectional SCSI Control Signals—SCD/, SIO/, SMSG/, SBSY/, SATN/, SSEL/, SRST/, SCD±, SIO±, SMSG±, SBSY±, SATN±, SSEL±, SRST±

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	1.9	V_{DD}	V	–
V_{IL}	Input low voltage	V_{SS}	1.0	V	–
V_{OL}	Output low voltage	V_{SS}	0.5	V	48 mA
I_{OZ}	3-state leakage	–10	10	µA	–

Table 4.7 DIFFSENS SCSI Signal

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_S	LVD sense voltage	0.7	1.9	V	–
V_{IL}	Single-ended sense voltage	V_{SS} – 0.3	0.5	V	–
I_{OZ}	3-state leakage	–10	10	µA	–

Table 4.8 Input Capacitance

Symbol	Parameter	Min	Max	Unit	Test Conditions
C_I	Input capacitance of input pads	–	7	pF	–
C_{IO}	Input capacitance of I/O pads	–	10	pF	–

Table 4.9 Input Control Signals—CLOCK, CHIP_RESET/, WS_ENABLE/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD}	V	–
V_{IL}	Input low voltage	V_{SS}	0.8	V	–
I_{OZ}	3-state leakage	–10	10	µA	–

Table 4.10 Output Control Signals—BSY_LED, XFER_ACTIVE

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	8 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	8 mA
I_{OZ}	3-state leakage	–10	10	µA	–

4.1.2 TolerANT Technology Electrical Characteristics

Table 4.11 provides the minimum and maximum values in units for the TolerANT Technology electrical characteristics.

Table 4.11 TolerANT Technology Electrical Characteristics

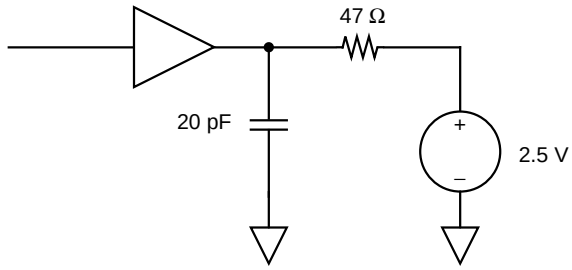
Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}[1]	Output high voltage	2.0	V_{DD} + 0.3	V	I_{OH} = 7 mA
V_{OL}	Output low voltage	V_{SS}	0.5	V	I_{OL} = 48 mA
V_{IH}	Input high voltage	2.0	V_{DD} + 0.3	V	–
V_{IL}	Input low voltage	V_{SS} – 0.3	0.8	V	Referenced to V_{SS}
V_{IK}	Input clamp voltage	–0.66	–0.77	V	V_{DD} = 4.75; I_I = –20 mA
V_{TH}	Threshold, HIGH to LOW	1.0	1.2	V	–
V_{TL}	Threshold, LOW to HIGH	1.4	1.6	V	–
V_{TH}-V_{TL}	Hysteresis	300	500	mV	–
I_{OH}[2]	Output high current	2.5	24	mA	V_{OH} = 2.5 V
I_{OL}	Output low current	100	200	mA	V_{OL} = 0.5 V
I_{OSH}[2]	Short-circuit output high current	–	625	mA	Output driving low, pin shorted to V_{DD} supply[2]
I_{OSL}	Short-circuit output low current	–	95	mA	Output driving high, pin shorted to V_{SS} supply
I_{LH}	Input high leakage	–	20	µA	–0.5<V_{DD}<5.25 V_{PIN} = 2.7 V[3]
I_{LL}	Input low leakage	–	–20	µA	–0.5<V_{DD}<5.25 V_{PIN} = 0.5 V
R_I	Input resistance	20	–	MΩ	Receivers Disabled[3]
C_P	Capacitance per pin	–	15	pF	PQFP
t_R[2]	Rise time, 10% to 90%	4.0	18.5	ns	Refer to Figure 4.3
t_F	Fall time, 90% to 10%	4.0	18.5	ns	Refer to Figure 4.3
dV_H/dt	Slew rate, LOW to HIGH	0.15	0.50	V/ns	Refer to Figure 4.3

Table 4.11 TolerANT Technology Electrical Characteristics (Cont.)

Symbol	Parameter	Min	Max	Units	Test Conditions
dV_L/dt	Slew rate, HIGH to LOW	0.15	0.50	V/ns	Refer to Figure 4.3
ESD	Electrostatic discharge	2	–	kV	MIL-STD-883C; 3015-7
	Latch-up	100	–	mA	–
	Filter delay	20	30	ns	–
	Ultra filter delay	10	15	ns	–
	Extended filter delay	40	60	ns	–

1. Active negation outputs only: Data, Parity, SREQ/, and SACK/. SCSI SE mode only (minus signals).
2. Single pin only; irreversible damage may occur if sustained for one second.
3. SCSI RESET pin has a 10 kΩ pull-up resistor.

Figure 4.3 Rise and Fall Time Test Conditions



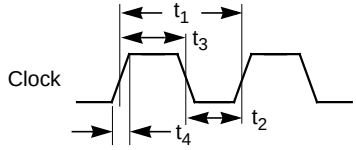
4.1.3 AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions. Chip timing is based on simulation at worst case voltage, temperature, and processing. The LSI53C320 requires a 40 MHz clock input. Table 4.12 and Figure 4.4 provide clock timing data.

Table 4.12 Clock Timing

Symbol	Parameter	Min	Max	Units
t_1	Clock period	24.75	25.25	ns
t_2	Clock low time	10	15	ns
t_3	Clock high time	10	15	ns
t_4	Clock rise time	1	–	V/ns

Figure 4.4 Clock Timing



4.2 Chip Drawings

This section provides the BGA and mechanical drawings for the LSI53C320.

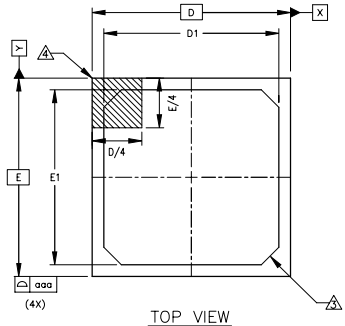
4.2.1 Mechanical Drawing

Figure 4.5 illustrates the LSI53C320 mechanical drawing. The LSI53C320 uses a 272-ball, PBGA package with a VG package code.

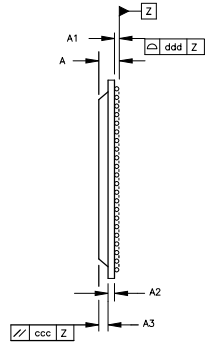
Figure 4.5 272-Ball-Count PBGA (VG) Mechanical Drawing (Sheet 1 of 2)

REVISIONS

APPROVAL	DATE	DESCRIPTION	REV
WK LIEW	11–30–01	INITIAL RELEASE	0
WK LIEW	03–13–02	REVISE DIMENSION (ddd)	1
WK LIEW	07–19–02	ADD PACKAGE CODE (F1)	2



TOP VIEW



SIDE VIEW

TABLE 1: COMMON DIMENSIONS			
SYM	MIN	NOM	MAX
A	–	–	2.60
A1	0.50	–	–
A2	0.25	–	0.70
A3	–	–	1.25
b	0.60	–	0.90
D	27.00 BSC		
D1	23.00	–	25.00
E	27.00 BSC		
E1	23.00	–	25.00
e	1.27 BSC		

TABLE 2: TOLERANCES OF FORM AND POSITION	
DIMENSION	[e] = 1.27
aaa	0.20
ccc	0.35
ddd	0.15
eee	0.30
fff	0.15

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. ALL DIMENSIONS IN MM.
3. CORNER DETAIL IS LSI LOGIC CORPORATION OPTION.
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, AND MAY CONSIST OF INK, LASER MARK OR METALLIZED MARKING, BUT MUST BE LOCATED WITHIN E ZONE INDICATED
5. JEDEC CODE MS–034.
6. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

LSI LOGIC CORPORATION
1551 McCARTHY BLVD. MILPITAS, CA. 95035

TITLE: 27x27mm PBGA/PBGA+/EPBGA–M
1.27 BALL PITCH

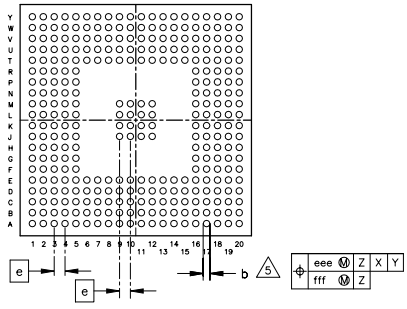
PKG CODE: BG F1 F7 F9 G9 GT GU IF IG KS V5 VF VG VS

DWG NO: JZ02–000003–00 REV: 2

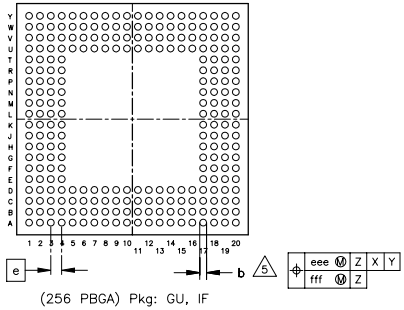
SCALE: NONE SHEET: 1 of 2

Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code VG.**

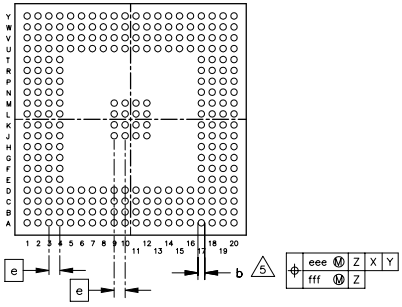
Figure 4.5 272-Ball-Count PBGA (VG) Mechanical Drawing (Sheet 2 of 2)



(316 PBGA) Pkg: BG, F9, G9
(316 PBGA+) Pkg: VS



(256 PBGA) Pkg: GU, IF
(256 PBGA+) Pkg: VF



(272 PBGA) Pkg: F7, GT, IG
(272 PBGA+) Pkg: VG, V5
(272 EPBGA–M) Pkg: KS, F1

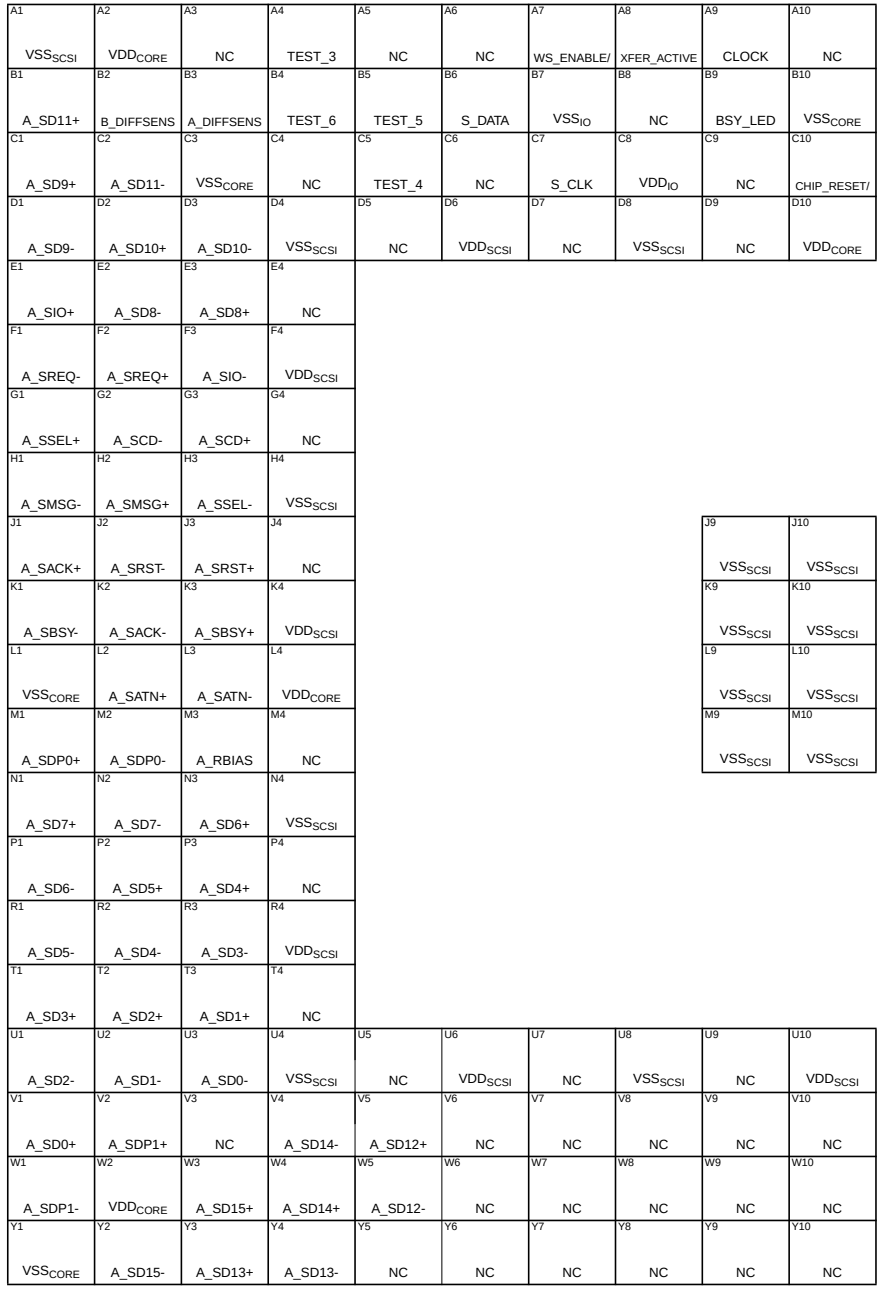
LSI LOGIC CORPORATION 1551 McCARTHY BLVD. MILPITAS, CA. 95035	
TITLE: 27x27mm PBGA/PBGA+/EPBGA–M 1.27 BALL PITCH	
PKG CODE: BG F1 F7 F9 G9 GT GU IF IG KS V5 VF VG VS	
DWG NO: JZ02–000003–00	REV: 2
SCALE: NONE	SHEET: 2 of 2

Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code VG.**

4.2.2 BGA Drawing

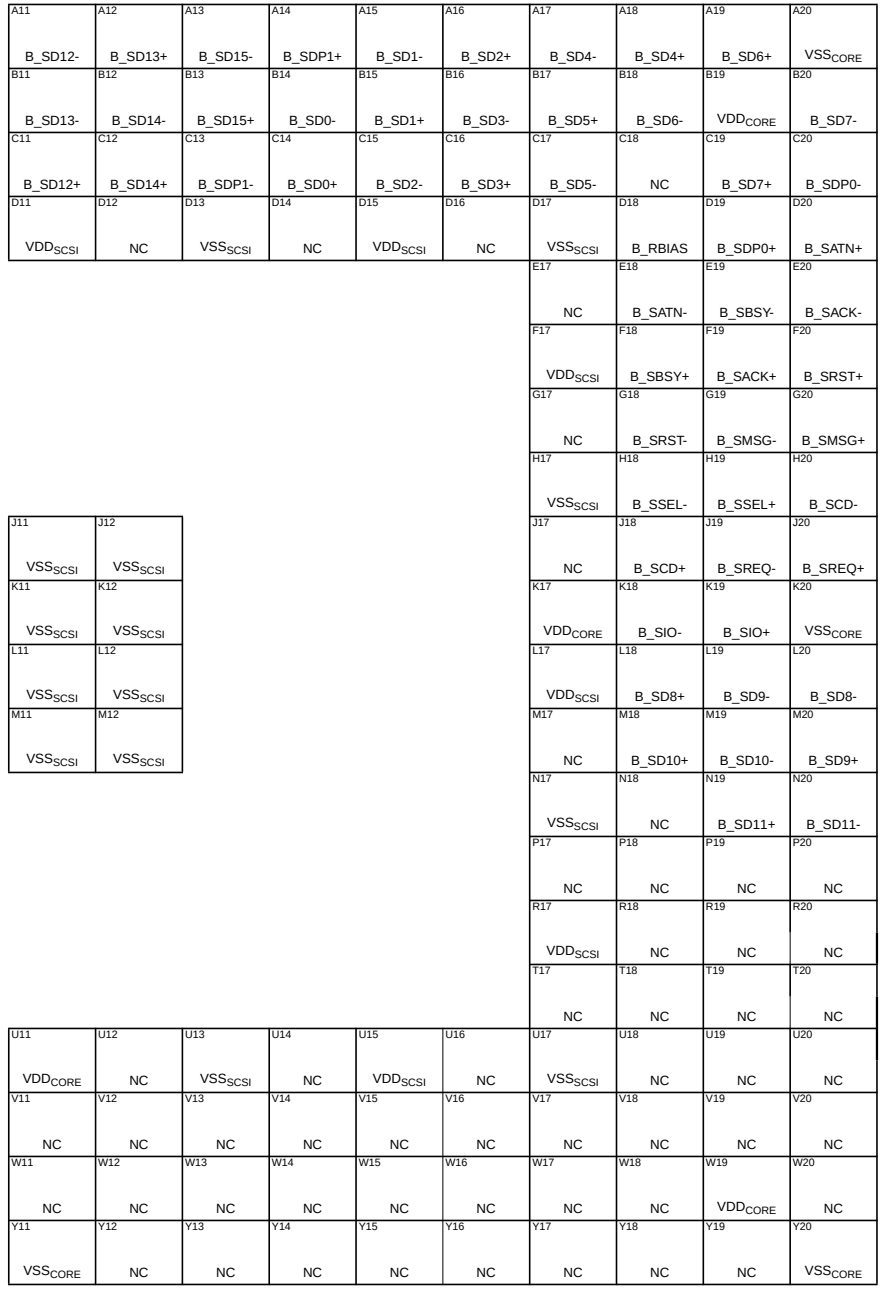
Figure 4.6 provides the BGA drawing for the LSI53C320. This drawing provides the pinout view when looking down on the chip from the top. Table 4.13 and Table 4.14 provide the pin lists for the LSI53C320.

Figure 4.6 LSI53C320 272-Ball BGA Top View[1]



1. The top view drawings provides the chip pinout from the top side of the chip.

Figure 4.6 LSI53C320 272-Ball BGA Top View (Cont.)



A11 B_SD12-	A12 B_SD13+	A13 B_SD15-	A14 B_SDP1+	A15 B_SD1-	A16 B_SD2+	A17 B_SD4-	A18 B_SD4+	A19 B_SD6+	A20 VSS_{CORE}
B11 B_SD13-	B12 B_SD14-	B13 B_SD15+	B14 B_SD0-	B15 B_SD1+	B16 B_SD3-	B17 B_SD5+	B18 B_SD6-	B19 VDD_{CORE}	B20 B_SD7-
C11 B_SD12+	C12 B_SD14+	C13 B_SDP1-	C14 B_SD0+	C15 B_SD2-	C16 B_SD3+	C17 B_SD5-	C18 NC	C19 B_SD7+	C20 B_SDP0-
D11 VDD_{SCSI}	D12 NC	D13 VSS_{SCSI}	D14 NC	D15 VDD_{SCSI}	D16 NC	D17 VSS_{SCSI}	D18 B_RBIAS	D19 B_SDP0+	D20 B_SATN+
						E17 NC	E18 B_SATN-	E19 B_SBSY-	E20 B_SACK-
						F17 VDD_{SCSI}	F18 B_SBSY+	F19 B_SACK+	F20 B_SRST+
						G17 NC	G18 B_SRST-	G19 B_SMSG-	G20 B_SMSG+
						H17 VSS_{SCSI}	H18 B_SSEL-	H19 B_SSEL+	H20 B_SCD-
J11 VSS_{SCSI}	J12 VSS_{SCSI}					J17 NC	J18 B_SCD+	J19 B_SREQ-	J20 B_SREQ+
K11 VSS_{SCSI}	K12 VSS_{SCSI}					K17 VDD_{CORE}	K18 B_SIO-	K19 B_SIO+	K20 VSS_{CORE}
L11 VSS_{SCSI}	L12 VSS_{SCSI}					L17 VDD_{SCSI}	L18 B_SD8+	L19 B_SD9-	L20 B_SD8-
M11 VSS_{SCSI}	M12 VSS_{SCSI}					M17 NC	M18 B_SD10+	M19 B_SD10-	M20 B_SD9+
						N17 VSS_{SCSI}	N18 NC	N19 B_SD11+	N20 B_SD11-
						P17 NC	P18 NC	P19 NC	P20 NC
						R17 VDD_{SCSI}	R18 NC	R19 NC	R20 NC
						T17 NC	T18 NC	T19 NC	T20 NC
U11 VDD_{CORE}	U12 NC	U13 VSS_{SCSI}	U14 NC	U15 VDD_{SCSI}	U16 NC	U17 VSS_{SCSI}	U18 NC	U19 NC	U20 NC
V11 NC	V12 NC	V13 NC	V14 NC	V15 NC	V16 NC	V17 NC	V18 NC	V19 NC	V20 NC
W11 NC	W12 NC	W13 NC	W14 NC	W15 NC	W16 NC	W17 NC	W18 NC	W19 VDD_{CORE}	W20 NC
Y11 VSS_{CORE}	Y12 NC	Y13 NC	Y14 NC	Y15 NC	Y16 NC	Y17 NC	Y18 NC	Y19 NC	Y20 VSS_{CORE}

Table 4.13 Pin List by Signal Name

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A_DIFFSENS	B3	A_SSEL-	H3	B_SSEL+	H19	NC	V9	VDD_{SCSI}	D6
A_RBIAS	M3	B_DIFFSENS	B2	B_SSEL-	H18	NC	V10	VDD_{SCSI}	D11
A_SACK+	J1	B_RBIAS	D18	BSY_LED	B9	NC	V11	VDD_{SCSI}	D15
A_SACK-	K2	B_SACK+	F19	CHIP_RESET/	C10	NC	V12	VDD_{SCSI}	F4
A_SATN+	L2	B_SACK-	E20	CLOCK	A9	NC	V13	VDD_{SCSI}	F17
A_SATN-	L3	B_SATN+	D20	NC	A3	NC	V14	VDD_{SCSI}	K4
A_SBSY+	K3	B_SATN-	E18	NC	A5	NC	V15	VDD_{SCSI}	L17
A_SBSY-	K1	B_SBSY+	F18	NC	A6	NC	V16	VDD_{SCSI}	R4
A_SCD+	G3	B_SBSY-	E19	NC	A10	NC	V17	VDD_{SCSI}	R17
A_SCD-	G2	B_SCD+	J18	NC	B8	NC	V18	VDD_{SCSI}	U6
A_SD0+	V1	B_SCD-	H20	NC	C4	NC	V19	VDD_{SCSI}	U10
A_SD0-	U3	B_SD0+	C14	NC	C6	NC	V20	VDD_{SCSI}	U15
A_SD1+	T3	B_SD0-	B14	NC	C9	NC	W6	VSS_{CORE}	A20
A_SD1-	U2	B_SD1+	B15	NC	C18	NC	W7	VSS_{CORE}	B10
A_SD10+	D2	B_SD1-	A15	NC	D5	NC	W8	VSS_{CORE}	C3
A_SD10-	D3	B_SD10+	M18	NC	D7	NC	W9	VSS_{CORE}	K20
A_SD11+	B1	B_SD10-	M19	NC	D9	NC	W10	VSS_{CORE}	L1
A_SD11-	C2	B_SD11+	N19	NC	D12	NC	W11	VSS_{CORE}	Y1
A_SD12+	V5	B_SD11-	N20	NC	D14	NC	W12	VSS_{CORE}	Y11
A_SD12-	W5	B_SD12+	C11	NC	D16	NC	W13	VSS_{CORE}	Y20
A_SD13+	Y3	B_SD12-	A11	NC	E4	NC	W14	VSS_{IO}	B7
A_SD13-	Y4	B_SD13+	A12	NC	E17	NC	W15	VSS_{SCSI}	A1
A_SD14+	W4	B_SD13-	B11	NC	G4	NC	W16	VSS_{SCSI}	D4
A_SD14-	V4	B_SD14+	C12	NC	G17	NC	W17	VSS_{SCSI}	D8
A_SD15+	W3	B_SD14-	B12	NC	J4	NC	W18	VSS_{SCSI}	D13
A_SD15-	Y2	B_SD15+	B13	NC	J17	NC	W20	VSS_{SCSI}	D17
A_SD2+	T2	B_SD15-	A13	NC	M4	NC	Y5	VSS_{SCSI}	H4
A_SD2-	U1	B_SD2+	A16	NC	M17	NC	Y6	VSS_{SCSI}	H17
A_SD3+	T1	B_SD2-	C15	NC	N18	NC	Y7	VSS_{SCSI}	J9
A_SD3-	R3	B_SD3+	C16	NC	P4	NC	Y8	VSS_{SCSI}	J10
A_SD4+	P3	B_SD3-	B16	NC	P17	NC	Y9	VSS_{SCSI}	J11
A_SD4-	R2	B_SD4+	A18	NC	P18	NC	Y10	VSS_{SCSI}	J12
A_SD5+	P2	B_SD4-	A17	NC	P19	NC	Y12	VSS_{SCSI}	K9
A_SD5-	R1	B_SD5+	B17	NC	P20	NC	Y13	VSS_{SCSI}	K10
A_SD6+	N3	B_SD5-	C17	NC	R18	NC	Y14	VSS_{SCSI}	K11
A_SD6-	P1	B_SD6+	A19	NC	R19	NC	Y15	VSS_{SCSI}	K12
A_SD7+	N1	B_SD6-	B18	NC	R20	NC	Y16	VSS_{SCSI}	L9
A_SD7-	N2	B_SD7+	C19	NC	T4	NC	Y17	VSS_{SCSI}	L10
A_SD8+	E3	B_SD7-	B20	NC	T17	NC	Y18	VSS_{SCSI}	L11
A_SD8-	E2	B_SD8+	L18	NC	T18	NC	Y19	VSS_{SCSI}	L12
A_SD9+	C1	B_SD8-	L20	NC	T19	S_CLK	C7	VSS_{SCSI}	M9
A_SD9-	D1	B_SD9+	M20	NC	T20	S_DATA	B6	VSS_{SCSI}	M10
A_SDP0+	M1	B_SD9-	L19	NC	U5	TEST_3	A4	VSS_{SCSI}	M11
A_SDP0-	M2	B_SDP0+	D19	NC	U7	TEST_4	C5	VSS_{SCSI}	M12
A_SDP1+	V2	B_SDP0-	C20	NC	U9	TEST_5	B5	VSS_{SCSI}	N4
A_SDP1-	W1	B_SDP1+	A14	NC	U12	TEST_6	B4	VSS_{SCSI}	N17
A_SIO+	E1	B_SDP1-	C13	NC	U14	VDD_{CORE}	A2	VSS_{SCSI}	U4
A_SIO-	F3	B_SIO+	K19	NC	U16	VDD_{CORE}	B19	VSS_{SCSI}	U8
A_SMSG+	H2	B_SIO-	K18	NC	U18	VDD_{CORE}	D10	VSS_{SCSI}	U13
A_SMSG-	H1	B_SMSG+	G20	NC	U19	VDD_{CORE}	K17	VSS_{SCSI}	U17
A_SREQ+	F2	B_SMSG-	G19	NC	U20	VDD_{CORE}	L4	WS_ENABLE/	A7
A_SREQ-	F1	B_SREQ+	J20	NC	V3	VDD_{CORE}	U11	XFER_ACTIVE	A8
A_SRST+	J3	B_SREQ-	J19	NC	V6	VDD_{CORE}	W2		
A_SRST-	J2	B_SRST+	F20	NC	V7	VDD_{CORE}	W19		
A_SSEL+	G1	B_SRST-	G18	NC	V8	VDD_{IO}	C8		

Table 4.14 Pin List by BGA Position

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	VSS_{SCSI}	C16	B_SD3+	H19	B_SSEL+	N18	NC	V9	NC
A2	VDD_{CORE}	C17	B_SD5-	H20	B_SCD-	N19	B_SD11+	V10	NC
A3	NC	C18	NC	J1	A_SACK+	N20	B_SD11-	V11	NC
A4	TEST_3	C19	B_SD7+	J2	A_SRST-	P1	A_SD6-	V12	NC
A5	NC	C20	B_SDP0-	J3	A_SRST+	P2	A_SD5+	V13	NC
A6	NC	D1	A_SD9-	J4	NC	P3	A_SD4+	V14	NC
A7	WS_ENABLE/	D2	A_SD10+	J9	VSS_{SCSI}	P4	NC	V15	NC
A8	XFER_ACTIVE	D3	A_SD10-	J10	VSS_{SCSI}	P17	NC	V16	NC
A9	CLOCK	D4	VSS_{SCSI}	J11	VSS_{SCSI}	P18	NC	V17	NC
A10	NC	D5	NC	J12	VSS_{SCSI}	P19	NC	V18	NC
A11	B_SD12-	D6	VDD_{SCSI}	J17	NC	P20	NC	V19	NC
A12	B_SD13+	D7	NC	J18	B_SCD+	R1	A_SD5-	V20	NC
A13	B_SD15-	D8	VSS_{SCSI}	J19	B_SREQ-	R2	A_SD4-	W1	A_SDP1-
A14	B_SDP1+	D9	NC	J20	B_SREQ+	R3	A_SD3-	W2	VDD_{CORE}
A15	B_SD1-	D10	VDD_{CORE}	K1	A_SBSY-	R4	VDD_{SCSI}	W3	A_SD15+
A16	B_SD2+	D11	VDD_{SCSI}	K2	A_SACK-	R17	VDD_{SCSI}	W4	A_SD14+
A17	B_SD4-	D12	NC	K3	A_SBSY+	R18	NC	W5	A_SD12-
A18	B_SD4+	D13	VSS_{SCSI}	K4	VDD_{SCSI}	R19	NC	W6	NC
A19	B_SD6+	D14	NC	K9	VSS_{SCSI}	R20	NC	W7	NC
A20	VSS_{CORE}	D15	VDD_{SCSI}	K10	VSS_{SCSI}	T1	A_SD3+	W8	NC
B1	A_SD11+	D16	NC	K11	VSS_{SCSI}	T2	A_SD2+	W9	NC
B2	B_DIFFSENS	D17	VSS_{SCSI}	K12	VSS_{SCSI}	T3	A_SD1+	W10	NC
B3	A_DIFFSENS	D18	B_RBIAS	K17	VDD_{CORE}	T4	NC	W11	NC
B4	TEST_6	D19	B_SDP0+	K18	B_SIO-	T17	NC	W12	NC
B5	TEST_5	D20	B_SATN+	K19	B_SIO+	T18	NC	W13	NC
B6	S_DATA	E1	A_SIO+	K20	VSS_{CORE}	T19	NC	W14	NC
B7	VSS_{IO}	E2	A_SD8-	L1	VSS_{CORE}	T20	NC	W15	NC
B8	NC	E3	A_SD8+	L2	A_SATN+	U1	A_SD2-	W16	NC
B9	BSY_LED	E4	NC	L3	A_SATN-	U2	A_SD1-	W17	NC
B10	VSS_{CORE}	E17	NC	L4	VDD_{CORE}	U3	A_SD0-	W18	NC
B11	B_SD13-	E18	B_SATN-	L9	VSS_{SCSI}	U4	VSS_{SCSI}	W19	VDD_{CORE}
B12	B_SD14-	E19	B_SBSY-	L10	VSS_{SCSI}	U5	NC	W20	NC
B13	B_SD15+	E20	B_SACK-	L11	VSS_{SCSI}	U6	VDD_{SCSI}	Y1	VSS_{CORE}
B14	B_SD0-	F1	A_SREQ-	L12	VSS_{SCSI}	U7	NC	Y2	A_SD15-
B15	B_SD1+	F2	A_SREQ+	L17	VDD_{SCSI}	U8	VSS_{SCSI}	Y3	A_SD13+
B16	B_SD3-	F3	A_SIO-	L18	B_SD8+	U9	NC	Y4	A_SD13-
B17	B_SD5+	F4	VDD_{SCSI}	L19	B_SD9-	U10	VDD_{SCSI}	Y5	NC
B18	B_SD6-	F17	VDD_{SCSI}	L20	B_SD8-	U11	VDD_{CORE}	Y6	NC
B19	VDD_{CORE}	F18	B_SBSY+	M1	A_SDP0+	U12	NC	Y7	NC
B20	B_SD7-	F19	B_SACK+	M2	A_SDP0-	U13	VSS_{SCSI}	Y8	NC
C1	A_SD9+	F20	B_SRST+	M3	A_RBIAS	U14	NC	Y9	NC
C2	A_SD11-	G1	A_SSEL+	M4	NC	U15	VDD_{SCSI}	Y10	NC
C3	VSS_{CORE}	G2	A_SCD-	M9	VSS_{SCSI}	U16	NC	Y11	VSS_{CORE}
C4	NC	G3	A_SCD+	M10	VSS_{SCSI}	U17	VSS_{SCSI}	Y12	NC
C5	TEST_4	G4	NC	M11	VSS_{SCSI}	U18	NC	Y13	NC
C6	NC	G17	NC	M12	VSS_{SCSI}	U19	NC	Y14	NC
C7	S_CLK	G18	B_SRST-	M17	NC	U20	NC	Y15	NC
C8	VDD_{IO}	G19	B_SMSG-	M18	B_SD10+	V1	A_SD0+	Y16	NC
C9	NC	G20	B_SMSG+	M19	B_SD10-	V2	A_SDP1+	Y17	NC
C10	CHIP_RESET/	H1	A_SMSG-	M20	B_SD9+	V3	NC	Y18	NC
C11	B_SD12+	H2	A_SMSG+	N1	A_SD7+	V4	A_SD14-	Y19	NC
C12	B_SD14+	H3	A_SSEL-	N2	A_SD7-	V5	A_SD12+	Y20	VSS_{CORE}
C13	B_SDP1-	H4	VSS_{SCSI}	N3	A_SD6+	V6	NC		
C14	B_SD0+	H17	VSS_{SCSI}	N4	VSS_{SCSI}	V7	NC		
C15	B_SD2-	H18	B_SSEL-	N17	VSS_{SCSI}	V8	NC		

Appendix A
Wiring Diagrams

A.1 LSI53C320 Wiring Diagrams

Figures A.1 through A.4 provide wiring diagrams for a typical LSI53C320 configuration in a evaluation test board application.

Figure A.1 LSI53C320 Wiring Diagram 1 of 4

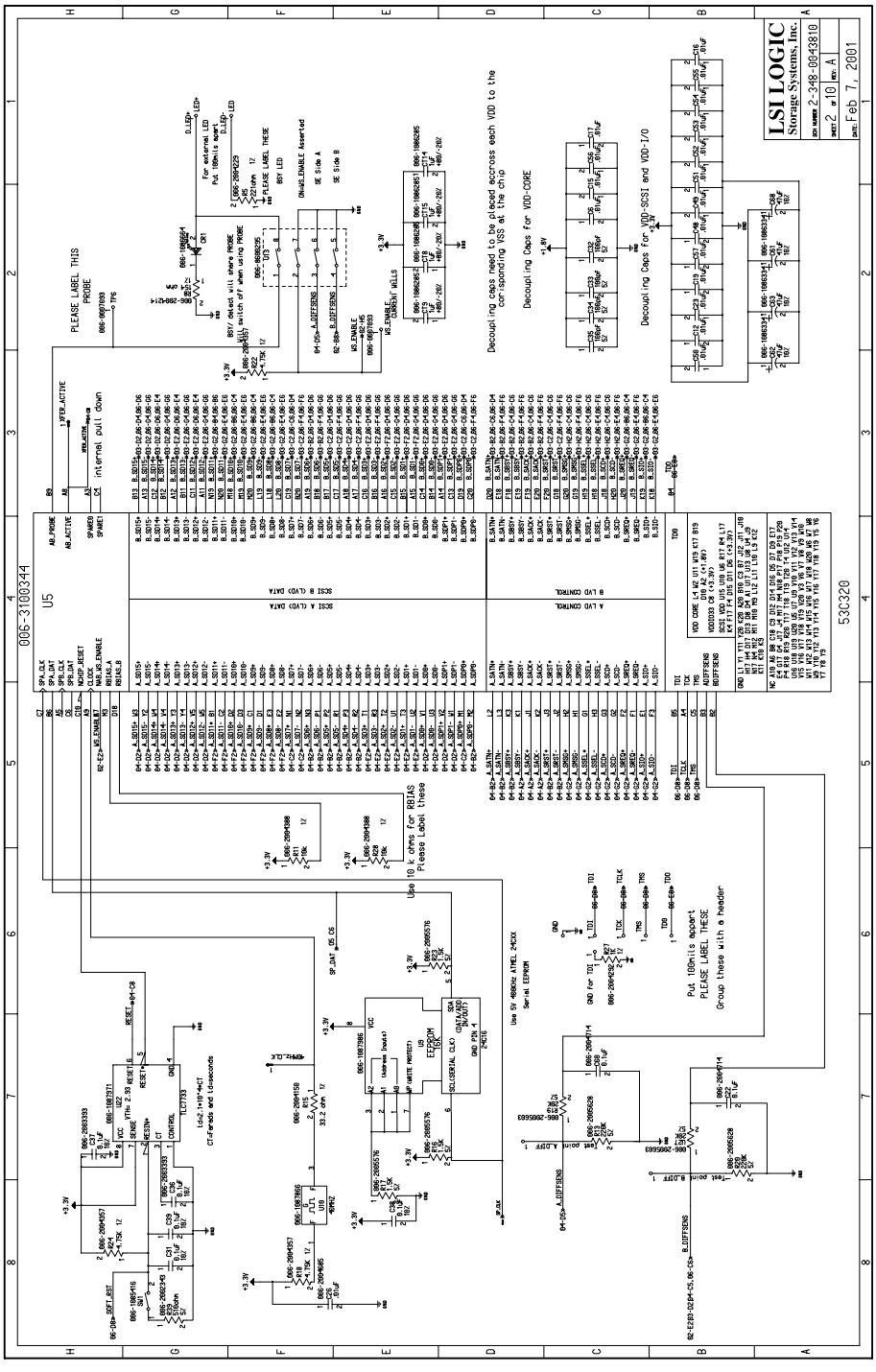


Figure A.2 LSI53C320 Wiring Diagram 2 of 4

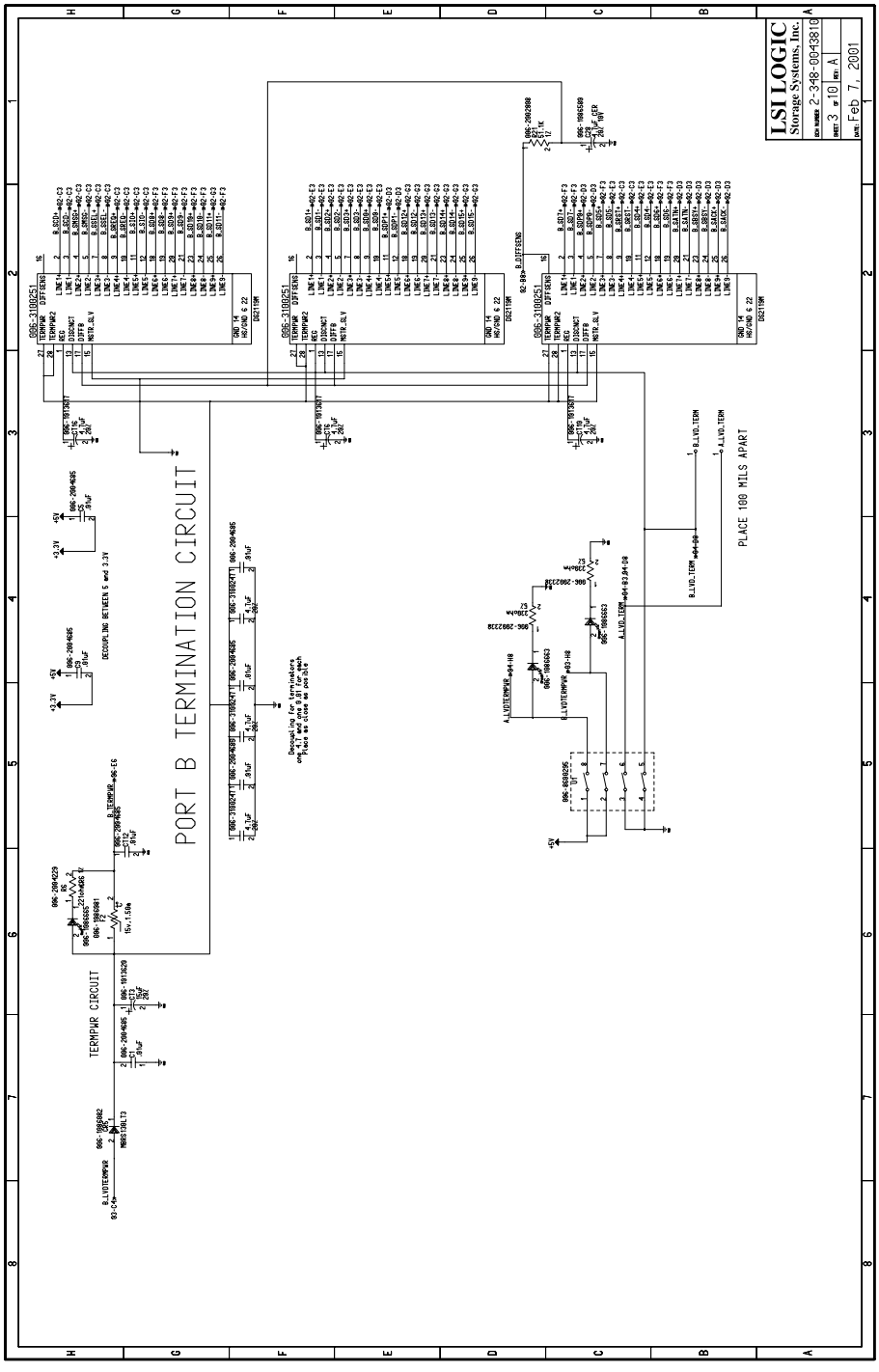


Figure A.3 LSI53C320 Wiring Diagram 3 of 4

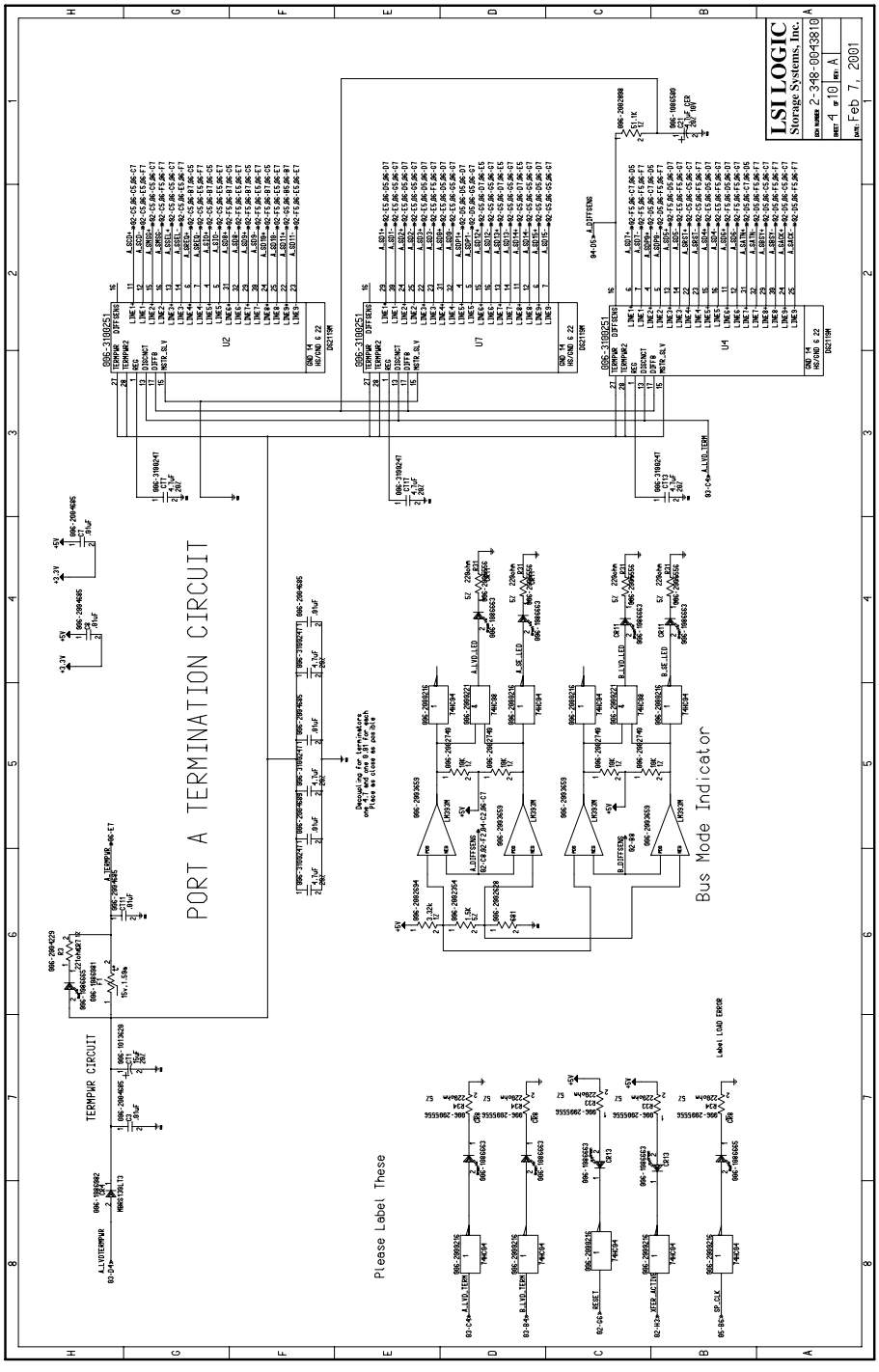
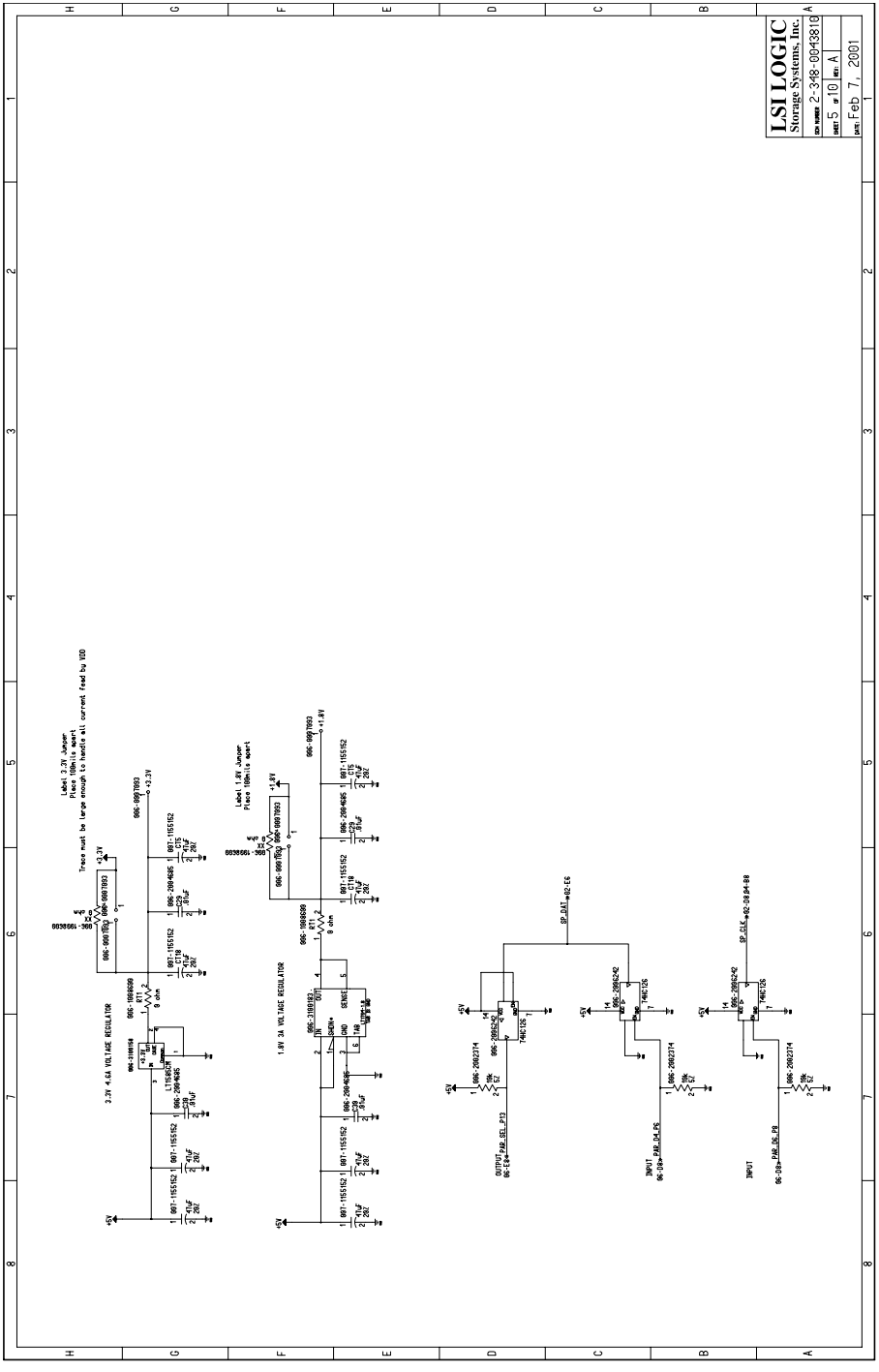


Figure A.4 LSI53C320 Wiring Diagram 4 of 4



Appendix B
Glossary

Block	A block is the basic 512 byte size of storage that the storage media is divided into. The Logical Block Address protocol uses sequential block addresses to access the media.
Bus Expander	Bus expander technology permits the extension of a bus by providing some signal filtering and retiming to maintain signal skew budgets.
Device	A single unit on the SCSI bus, identifiable by a SCSI address. It can be a processor unit, a storage unit (such as a disk or tape controller or drive), an output unit (such as a controller or printer), or a communications unit.
Differential	A signaling alternative that employs differential drivers and receivers to improve signal-to-noise ratios and increase maximum cable lengths.
Double Transition Clocking	In Double Transition (DT) Clocking data is sampled on both the asserting and deasserting edge of the REQ/ACK signal. DT clocking may only be implemented on an LVD SCSI bus.
Host	A processor, usually consisting of the central processing unit and main memory. Typically, a host communicates with other devices, such as peripherals and other hosts. On the SCSI bus, a host has a SCSI address.
Initiator	A SCSI device that requests another SCSI device (a target) to perform an operation. Usually, a host acts as an initiator and a peripheral device acts as a target.
Logical Unit	The logical representation of a physical or virtual device, addressable through a target. A physical device can have more than one logical unit.
LVD	Low Voltage Differential. LVD is a robust design methodology that improves power consumption, data integrity, cable lengths and support for multiple devices, while providing a migration path for increased I/O performance.

Negation	The act of driving a signal to the false state or allowing the cable terminators to bias the signal to the false state.
Parity	A method of checking the accuracy of binary numbers. An extra bit, called a parity bit, is added to a number. If even parity is used, the sum of all 1s in the number and its corresponding parity is always even. If odd parity is used, the sum of the 1s and the parity bit is always odd.
Port	A connection into a bus.
Priority	The ranking of the devices on the bus during arbitration.
Receiver	The circuitry that receives electrical signals on a line.
Reconnect	The function that occurs when a target reselects an initiator to continue an operation after a disconnect.
Reselect	A target can disconnect from an initiator in order to perform a time-consuming function, such as a disk seek. After performing the operation, the target can “reselect” the initiator.
Target	A SCSI device that performs an operation requested by an initiator.
Termination	The electrical connection at each end of the SCSI bus, composed of a set of resistors.
TolerANT	A technology developed and used by LSI Logic to improve data integrity, data transfer rates, and noise immunity through the use of active negation and input signal filtering.
Ultra320 SCSI	A standard for SCSI data transfers. It allows a transfer rate of up to 320 Mbytes/s over a 16-bit SCSI bus. STA (SCSI Trade Association) supports using the terms “Ultra320 SCSI” over the term “Fast-160.”

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