PRODUCT DEVELOPMENT PACKAGE

SPC8108F$_{0B}$
LCD VGA CONTROLLER

Release 0.0
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SPC8108F$_{0B}$ LCD VGA Controller

Power Save Modes

Drawing Office No.

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POWER SAVE MODES

1.0 POWER SAVE MODES

To accommodate the important need for power reduction in sub-notebook and palmtop computers, one hardware-controlled and five-software controlled Power Save Modes have been incorporated into the SPC8108. Additional options for these Power Save Modes can be enabled by setting bits in various Auxiliary registers, allowing flexibility in tailoring the power reduction scheme to any particular system implementation.

1.1 Software Power Save Modes

The Power Save Mode bits in the Power Save Register, Aux[03] select one of the five software Power Save Modes as shown below. Note that if hardware Suspend mode is activated, the software power save mode setting in this register is ignored (i.e. hardware Suspend mode overrides the software power save modes). If these bits are set to a values 110 or 111, then the chip will remain in normal active mode. The following descriptions outline the major functions of each power save mode. Some differences in power save mode operation exist between LCD and CRT display modes - see the following tables and notes for more information.

Power Save Mode Select			Mode Activated
bit 2	bit 1	bit 0	
0	0	0	Normal Operation
0	0	1	Power Save Mode 1 enable
0	1	0	Power Save Mode 2 enable (toggle between states 1 & 2, see below)
0	1	1	Power Save Mode 3 enable
1	0	0	Power Save Mode 4 enable
1	0	1	Power Save Mode 5 enable (n/a for CRT mode)

Software Power Save Mode 1

- No video display accesses to display memory.
- Sequencer is dedicated to CPU accesses to/from display memory.
- Display memory refresh is maintained and is generated from active CLKI input (28MHz for LCD, 25MHz or 28MHz for CRT). Refresh rate can be selected: 64 kHz or 8 kHz, (for 256 cycle/4 msec, or 256 cycle/32 msec DRAM, respectively).
- I/O read/write of all registers is allowed.
- /LCDPWR and IREFCNT signals forced high.
- LCD interface output signals tri-stated or forced low, depending on the state of the LCD Signal PS Mode bit in LCD Support Register 1, Aux[02] bit 1.
- if CRT display enabled, CRT and RAMDAC interface signals forced low (except /DACRD and /DACWR which remain active).

Software Power Save Mode 2

Power Save Mode 2 has two states. Initially when Power Save Mode 2 is set, the chip enters State 1. If no display memory read or write is detected for about two horizontal lines (approx. 63.5 us), the chip enters State 2. If a display memory read or write is requested while in State 2, the chip returns to State 1 to service the display memory access within 3 - 7 clock periods of the active CLKI input clock.

State 1

- No video display accesses to display memory.
- Sequencer is dedicated to CPU accesses to/from display memory.
- Display memory refresh is maintained and is generated from the active CLKI input (28MHz for LCD, 25MHz or 28MHz for CRT). Refresh rate can be selected: 64 kHz or 8 kHz, (for 256 cycle/4 msec, or 256 cycle/32 msec DRAM, respectively).
- I/O read/write of all registers is allowed.
- /LCDPWR and IREFCNT signals forced high.
- LCD interface output signals tri-stated or forced low, depending on the state of the LCD Signal PS Mode bit in LCD Support Register 1, Aux[02] bit 1.
- if CRT display enabled, CRT and RAMDAC interface signals forced low (except /DACRD and /DACWR which remain active).

State 2

- No video display accesses to display memory.
- No CPU accesses to/from display memory.
- Sequencer is halted.
- Display memory refresh is maintained and is generated from the active CLKI input (28MHz for LCD, 25MHz or 28MHz for CRT). Refresh rate can be selected: 64 kHz or 8 kHz, (for 256 cycle/4 msec, or 256 cycle/32 msec DRAM, respectively).
- I/O read/write of all registers is allowed.
- /LCDPWR and IREFCNT signals forced high.
- LCD interface output signals tri-stated or forced low, depending on the state of the LCD Signal PS Mode bit in LCD Support Register 1, Aux[02] bit 1.
- if CRT display enabled, CRT and RAMDAC interface signals forced low (except /DACRD and /DACWR which remain active).

Software Power Save Mode 3

- No video display accesses to display memory.
- No CPU accesses to/from display memory.
- Sequencer is halted.
- No display memory refresh.
- I/O read/write of all registers is allowed (except LUT and RAMDAC registers).
- /LCDPWR and IREFCNT signals forced high.

- LCD interface output signals tri-stated or forced low, depending on the state of the LCD Signal PS Mode bit in LCD Support Register 1, Aux[02] bit 1.
- if CRT display enabled, CRT and RAMDAC interface signals forced low (except /DACRD and /DACWR which are forced high).

Options

- I/O read/write to all registers except Auxiliary Registers can be disabled.
- the active internal clock oscillator cell can be disabled if a 2-terminal crystal is used. Note that the non-selected internal clock oscillator is automatically disabled in all active and power-save modes.

Software Power Save Mode 4

- No video display accesses to display memory.
- No CPU accesses to/from display memory.
- Sequencer is halted.
- Display memory refresh is maintained and is generated from one of 3 selectable sources: 1) from the active CLKI input (28MHz for LCD, 25MHz or 28MHz for CRT), 2) from the PDCLK pin (32kHz 50% duty cycle, or 64kHz with short low pulse duration), 3) or from a clock source connected to pin MEMEN.
- Refresh rate generated from CLKI can be selected: 64 kHz or 8 kHz, (for 256 cycle/4 msec, or 256 cycle/32 msec DRAM, respectively).
- Refresh rate generated from MEMEN or PDCLK can also be selected: 64 kHz or 8 kHz, (for 256 cycle/4 msec, or 256 cycle/32 msec DRAM, respectively).
- I/O read/write of all registers is allowed (except LUT and RAMDAC registers).
- /LCDPWR and IREFCNT signals forced high.
- LCD interface output signals tri-stated or forced low, depending on the state of the LCD Signal PS Mode bit in LCD Support Register 1, Aux[02] bit 1.
- if CRT display enabled, CRT and RAMDAC interface signals forced low (except /DACRD and /DACWR which are forced high).

Options

- I/O read/write to all registers except Auxiliary Registers can be disabled.
- Select MEMEN input pin, PDCLK input pin, or internally divided down CLKI as the clock source for display memory refresh generation.
- select self-refresh mode, for DRAMs that support self-refresh.
- the active internal clock oscillator cell can be disabled if a 2-terminal crystal is used. Note that the non-selected internal clock oscillator is automatically disabled in all active and power-save modes.

Software Power Save Mode 5 (LCD mode only)

- video display accesses to display memory allowed.
- CPU accesses to/from display memory allowed.
- Display memory refresh as in normal active mode.
- I/O read/write of all registers is allowed.
- /LCDPWR signal remains low (i.e. panel power enabled) and video display remains visible on LCD.
- internal LUT disabled.

- this power save mode not available when CRT display active.

Options

- internal clock can be slowed to 4/5 of normal rate.

Hardware Power Save Mode (Suspend Mode)

- No video display accesses to display memory.
- No CPU accesses to/from display memory.
- Sequencer is halted.
- Display memory refresh is maintained and is generated from one of 3 selectable sources: 1) from the active CLKI input (28MHz for LCD, 25MHz or 28MHz for CRT), 2) from the PDCLK pin (32kHz 50% duty cycle, or 64kHz with short low pulse duration), 3) or from a clock source connected to pin MEMEN.
- Refresh rate generated from CLKI can be selected: 64 kHz or 8 kHz, (for 256 cycle/4 msec, or 256 cycle/32 msec DRAM, respectively).
- Refresh rate generated from MEMEN or PDCLK can also be selected: 64 kHz or 8 kHz, (for 256 cycle/4 msec, or 256 cycle/32 msec DRAM, respectively).
- No I/O register or memory accesses allowed (including LUT and RAMDAC).
- /LCDPWR and IREFCNT signal forced high.
- LCD interface output signals tri-stated or forced low, depending on the state of the LCD Signal PS Mode bit in LCD Support Register 1, Aux[02] bit 1.
- if CRT display enabled, CRT and RAMDAC interface signals forced low (except /DACRD and /DACWR)
- All CPU interface input signals are internally masked off (i.e. ignored). All CPU interface output signals are inactive (except MEMEN).
- active internal clock oscillator will be automatically disabled unless CLKI is selected as the clock source for display memory refresh generation.

Options

- Select MEMEN input pin, PDCLK input pin, or internally divided down CLKI as the clock source for display memory refresh generation.
- select self-refresh mode, for DRAMs that support self-refresh.

1.2 Power Save Mode Function Summary

LCD Only (no CRT attached, RAMDAC powered off by system)

Power Save Mode (PSM) / Function	Normal (Active)	SPSM1	SPSM2 s1	SPSM2 s2	SPSM3	SPSM4	SPSM5	H-PSM Suspend
LCD Display Active?	On	Off	Off	Off	Off	Off	On	Off
CRT Display Active?	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
I/O access possible?	Yes	Yes	Yes	Yes	Yes, except LUT	Yes, except LUT	Yes	No
Memory access possible?	Yes	Yes	Yes	No	No	No	Yes	No
Memory refresh maintained?	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes
Internal LUT active?	Yes	Yes	Yes	Yes	No	No	Yes	No
External RAMDAC active?	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Sequencer running?	Yes	Yes	Yes	No	No	No	Yes	No
Refresh generated from CLKI (Sequencer running)	Yes	Yes	Yes	n/a	n/a	n/a	Yes	n/a
Refresh generated from CLKI (Sequencer stopped)	n/a	n/a	n/a	Yes	n/a	option	n/a	option
Refresh generated from MEMEN	No	No	No	No	n/a	option note 1	No	option note 1
Refresh generated from PDCLK	No	No	No	No	n/a	option note 2	No	option note 2
Self-refresh	No	No	No	No	n/a	option note 3	No	option note 3
256cycle/4ms, /32ms refresh selectable	Yes	Yes	Yes	Yes	n/a	Yes note 1, 2	Yes	Yes note 1, 2

LCD Signals

UD[3:0], LD[3:0]	Active	L/HiZ note 13	L/HiZ note 13	L/HiZ note 13	L/HiZ note 13	L/HiZ note 13	Active	L/HiZ note 13
YD, LP, XSCL, WF	Active	L/HiZ note 13	L/HiZ note 13	L/HiZ note 13	L/HiZ note 13	L/HiZ note 13	Active	L/HiZ note 13
/LCDPWR	L	H	H	H	H	H	L	H

RAMDAC Signals

IREFCNT	H	H	H	H	H	H	H	H
PD[7:0], PCLK	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ
/DACRD, /DACWR	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ
RS2, OL0, OL1, OL23	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ
D477	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ
/BLANK	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ

CRT Signals

/HSYNC, /VSYNC	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ
MS[2:0]	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c

CPU Signals

LA[23:20], A[19:0], D[15:0], /IOR, /IOW, /IOEN, /BHE, ALE, RESET	active	active	active	active	active	active	active	masked
/MEMR, /MEMW, MEMEN	active	active	active	active	masked	masked note 15	active	masked note 15

Clocks

25MHz	disabled	disabled	disabled	disabled	disabled	disabled	disabled	disabled
28MHz	Active	Active	Active	Active	can be disabled note 4	can be disabled note 4	Active	can be disabled note 5, 6, 7, 8

See “Implementation Notes” following for further details.

CRT Only (LCD off)

Power Save Mode (PSM) / Function	Normal (Active)	SPSM1	SPSM2 s1	SPSM2 s2	SPSM3	SPSM4	SPSM5 n/a CRT	H-PSM Suspend
LCD Display Active?	Off	Off	Off	Off	Off	Off	n/a	Off
CRT Display Active?	Active	Off	Off	Off	Off	Off	n/a	Off
I/O access possible?	Yes	Yes	Yes	Yes	Yes, except LUT	Yes, except LUT	n/a	No
Memory access possible?	Yes	Yes	Yes	No	No	No	n/a	No
Memory refresh maintained?	Yes	Yes	Yes	Yes	No	Yes	n/a	Yes
Internal LUT active?	WR only note 16	WR only note 16	WR only note 16	WR only note 16	disabled	disabled	n/a	disabled
External RAMDAC active?	Active	Active	Active	Active	disabled	disabled	n/a	disabled
Sequencer running?	Yes	Yes	Yes	No	No	No	n/a	No
Refresh generated from CLKI (Sequencer running)	Yes	Yes	Yes	n/a	n/a	n/a	n/a	n/a
Refresh generated from CLKI (Sequencer stopped)	n/a	n/a	n/a	Yes	n/a	option	n/a	option
Refresh generated from MEMEN	No	No	No	No	n/a	option note 1	n/a	option note 1
Refresh generated from PDCLK	No	No	No	No	n/a	option note 2	n/a	option note 2
Self-refresh	No	No	No	No	n/a	option note 3	n/a	option note 3
256cycle/4ms, /32ms refresh selectable	Yes	Yes	Yes	Yes	n/a	Yes note 1, 2	n/a	Yes note 1, 2

LCD Signals

UD[3:0], LD[3:0]	L/HiZ note 13	L/HiZ note 13	L/HiZ note 13	L/HiZ note 13	L/HiZ note 13	L/HiZ note 13	n/a	L/HiZ note 13
YD, LP, XSCL, WF	L/HiZ note 13	L/HiZ note 13	L/HiZ note 13	L/HiZ note 13	L/HiZ note 13	L/HiZ note 13	n/a	L/HiZ note 13
/LCDPWR	H	H	H	H	H	H	n/a	H

RAMDAC Signals

IREFCNT	L	H	H	H	H	H	n/a	H
PD[7:0], PCLK	Active	Active	Active	Active	L	L	n/a	L
/DACRD, /DACWR	Active	Active	Active	Active	H	H	n/a	H
RS2, OL0, OL1, OL23	Active	L	L	L	L	L	n/a	L
D477	L	H note 18	H note 18	H note 18	H note 18	H note 18	n/a	H note 18
/BLANK	Active	L	L	L	L	L	n/a	L

CRT Signals

/HSYNC, /VSYNC	Active	L	L	L	L	L	n/a	L
MS[2:0]	connected	connected	connected	connected	connected	connected	n/a	connected

CPU Signals

LA[23:20], A[19:0], D[15:0], /IOR, /IOW, /IOEN, /BHE, ALE, RESET	active	active	active	active	active	active	n/a	masked
/MEMR, /MEMW	active	active	active	active	masked	masked note 15	n/a	masked note 15

Clocks

25MHz	Active /disabled if not selected	Active /disabled if not selected	Active /disabled if not selected	Active /disabled if not selected	can be disabled note 4	can be disabled note 4	n/a	can be disabled note 5, 6, 7, 8
28MHz	Active /disabled if not selected	Active /disabled if not selected	Active /disabled if not selected	Active /disabled if not selected	can be disabled note 4	can be disabled note 4	n/a	can be disabled note 5, 6, 7, 8

See “Implementation Notes” following for further details.

1.3 Implementation Notes

1. For Software Power Save Mode 4 and the Hardware Power Save Mode (Suspend mode), the clock source from MEMEN should be running at a frequency of 64 kHz. MEMEN's active low pulse width should be as short as possible (but greater than the min. DRAM RAS pulse width requirement). The use of a 64 kHz clock source is required for meeting the 256 cycles/4 msec DRAM refresh specification. Optionally, an 8 kHz clock source may be connected to MEMEN for DRAMs supporting 256 cycles/32 msec, or the 64 kHz input can be internally divided down to 8 kHz by setting the 32/4msecRefresh Select bit (Aux[02] bit 0 = 1).
2. For Software Power Save Mode 4 and the Hardware Power Save Mode (Suspend mode), the clock source connected to the PDCLK input can be either a 32 kHz 50% duty cycle clock, or a 64 kHz clock with duty cycle similar to the requirement for MEMEN described above. In the case of a 32 kHz input clock, an external RC circuit is required and must be attached to pins 38, 39 with MD[13] = 1 at RESET (see pinout descriptions) in order to create an ~100ns delayed clock. This is used internally to generate a 64 kHz clock from the 32 kHz source with the appropriate duty cycle, as required by the 64 kHz refresh rate for 256cycles/4ms DRAM. If PDCLK is a 64 kHz clock with the appropriate duty cycle, then pins 38, 39 are not required and MD[13] can be set to 0 at RESET to permit usage of these pins for the sprite function on CRT display. For either type of PDCLK source input, the resulting internal 64 kHz refresh rate can be internally divided down to 8 kHz to support 256cycle/32msec DRAM by setting the 32/4msec Refresh Select bit (Aux[02] bit 0 = 1).
3. The self-refresh mode option available in Power Save Mode 4 and the Hardware Power Save Mode (Suspend mode) must only be enabled if the DRAM installed supports self-refresh operation.
4. In Software Power Save Modes 3 and 4, software may set an Auxiliary Register bit to disable the active internal clock oscillator. This can be used to further reduce system power consumption. The active clock is defined as either the 28 MHz clock (CLK2I) for LCD mode, or for CRT modes the clock selected by the Clock Select bits in Misc. Output Register 3C2H bits 3,2. In all modes, the unselected clock oscillator is automatically disabled.
5. In Hardware Power Save Mode (Suspend mode), the active internal clock oscillator is automatically turned off by hardware if the self-refresh option is enabled.
6. In Hardware Power Save Mode (Suspend), if MEMEN is selected as the refresh clock source, then the active internal clock oscillator is automatically turned off by hardware.
7. In Hardware Power Save Mode (Suspend), if PDCLK is selected as the refresh clock source, then the active internal clock oscillator is automatically turned off by hardware.
8. In Hardware Power Save Mode (Suspend), if the internal active clock is used as the refresh clock source, then the active internal clock oscillator cannot be turned off by hardware.
9. The output pin /LCDPWR should be used to control the LCD panel's power supply via external circuitry. When /LCDPWR is high, the external panel power supply should be turned off. When /LCDPWR is low, the power supply should be enabled.
10. After RESET is asserted, /LCDPWR is held high until the CRTC is programmed and running (i.e. LCD interface signals are active).
11. Circuitry in the chip will ensure that upon entering a power save mode, /LCDPWR will be driven high (panel power shut off) *before* the interface signals are tri-stated or forced low. Upon exiting a power save mode, /LCDPWR will be driven low (panel power turned on) *after* the interface

signals are returned to their active driving states. This sequencing of the /LCDPWR and interface signals is done to protect the panel from being damaged from DC signals applied to the interface while it is powered up.

12. Similarly, if the Sequencer is stopped, (Sequencer Reset Register bit 1 or bit 0 = 0), then /LCDPWR will be driven high (panel power shut off) *before* the Sequencer is shut down and the LCD interface signals are halted. Upon restarting the Sequencer (by setting Sequencer Reset Register bit 1 and bit 0 to 1), /LCDPWR will be driven low (panel power turned on) *after* the Sequencer is has started running and the LCD interface signals are returned to their active driving states. This sequencing of the /LCDPWR and interface signals is done to protect the panel from being damaged from DC signals applied to the interface while the Sequencer is stopped and all chip output signals are inactive.
13. A control bit in Auxiliary Register 1 allows selecting the power save mode state of the LCD interface signals. In power save modes, the LCD interface signals can all be driven low, or can be put into a high-impedance state, as selected by this option.
14. The output pin IREFCNT should be used to control the current reference source for the external RAMDAC. When IREFCNT is high, the current reference should be shut off - this will ensure that the DAC analog circuitry is not active. When IREFCNT is low, the current reference should be enabled. If a voltage reference is used for the RAMDAC, then IREFCNT is not required and may be left unconnected.
15. When the MEMEN pin is selected as the refresh clock source, this input will not be masked during Power Save Mode 4 or Suspend mode.
16. If Aux[0B] bit 2 = 1, then reads to the I/O address range 3C6H - 3C9H will be decoded as external RAMDAC reads. If Aux[0B] bit 2 = 0, then reads to this I/O address range will access the internal LUT registers. For CRT modes, this bit should be set to 1. If CRT mode is enabled, and the chip is in Active mode, Power Save Mode 1 or Power Save Mode 2, then writes to this I/O address range will result in data being written to both the internal LUT registers and the external RAMDAC registers.
17. In Active mode if the CRT is enabled, the logic value on the D477 pin is determined by Aux[0B] bit 4.
18. In order to properly make use of SLEEP mode of the RAMDAC, software is required to program the sleep bit in the external RAMDAC control register on system initialization. When the SPC8108 forces the D477 pin high in power save modes, the RAMDAC will enter sleep mode if this bit has been programmed correctly.

2.0 TARGET POWER CONSUMPTION IN POWER SAVE MODES

Conditions: f_{clkin} = 28MHz, LCD mode, no load.

Power Save Mode (PSM)	Normal (Active)	S-PSM1	S-PSM2 s1/s2	S-PSM3	S-PSM4	S-PSM5	H-PSM (Suspend)
I_{op} (mA) no load	tbd	tbd	tbd	tbd	tbd	tbd	tbd

SPC8108F$_{0B}$ LCD VGA Controller

A.C. Characteristics

Drawing Office No.

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A.C. CHARACTERISTICS

Conditions: V_{cc} = 5.0V ± 10% T_a = 0°C to 70°C

T_r, T_f for all inputs must be ≤ 5 nsec (10% ~ 90%)

C_L = 100 pF (CPU, RAMDAC Interface, LCD Panel Interface)
C_L = 20 pF (Video Memory Interface)

CLK Signal Dependant Input Timing:

$$T_S = \left[\frac{1}{f_{CLK}}\right], \quad T_{S\ Min} = \left[\frac{1}{f_{CLK\ Max}}\right] = \left[\frac{1}{28\ MHz}\right] = 36\ ns$$

Propagation Delay Time:
The following are tables of timing parameters and min/max values. These tables are followed by waveforms defining these parameters.

1. CPU BUS CYCLE TIMING - 16 BIT MEMORY

Symbol	Parameter	Min	Typ	Max	Units
t1	ALE pulse width	30			ns
t2	LA[23:17] valid setup to ALE asserted	20			ns
t3	LA[23:17] valid hold from ALE asserted	40			ns
t4	A[16:0], /BHE setup to ALE negated	10			ns
t5	LA[23:17] valid setup to memory command asserted	10			ns
t6	A[16:0], /BHE valid setup to memory command asserted	10			ns
t7	A[16:0], /BHE hold from memory command negated	10			ns
t8	valid write data delay from /MEMW asserted			3Ts-10	ns
t9	valid write data hold from /MEMW negated	10			ns
t10	/MEMCS16 asserted from valid LA[23:17]			30	ns
t11	/MEMCS16 hold from LA[23:17] invalid	0			ns
t12	READY negated from memory command asserted			50	ns
t13	READY negated pulse width	8Ts		102Ts	ns
t14	valid read data from READY released			40	ns
t15	read data hold from memory command negated	0			ns
t16	read command negated to D[15:0] high-impedance			30	ns

This table refers to standard ISA CPU bus timing . When configuration input MD[5] = 1 on the falling edge of RESET, refer to section 7.3 for modified address timing.

Parameter t13 max only occurs when a refresh cycle is pending during dual panel, fast dot, text modes. Max for single panel is 70Ts. Typical values are much shorter.

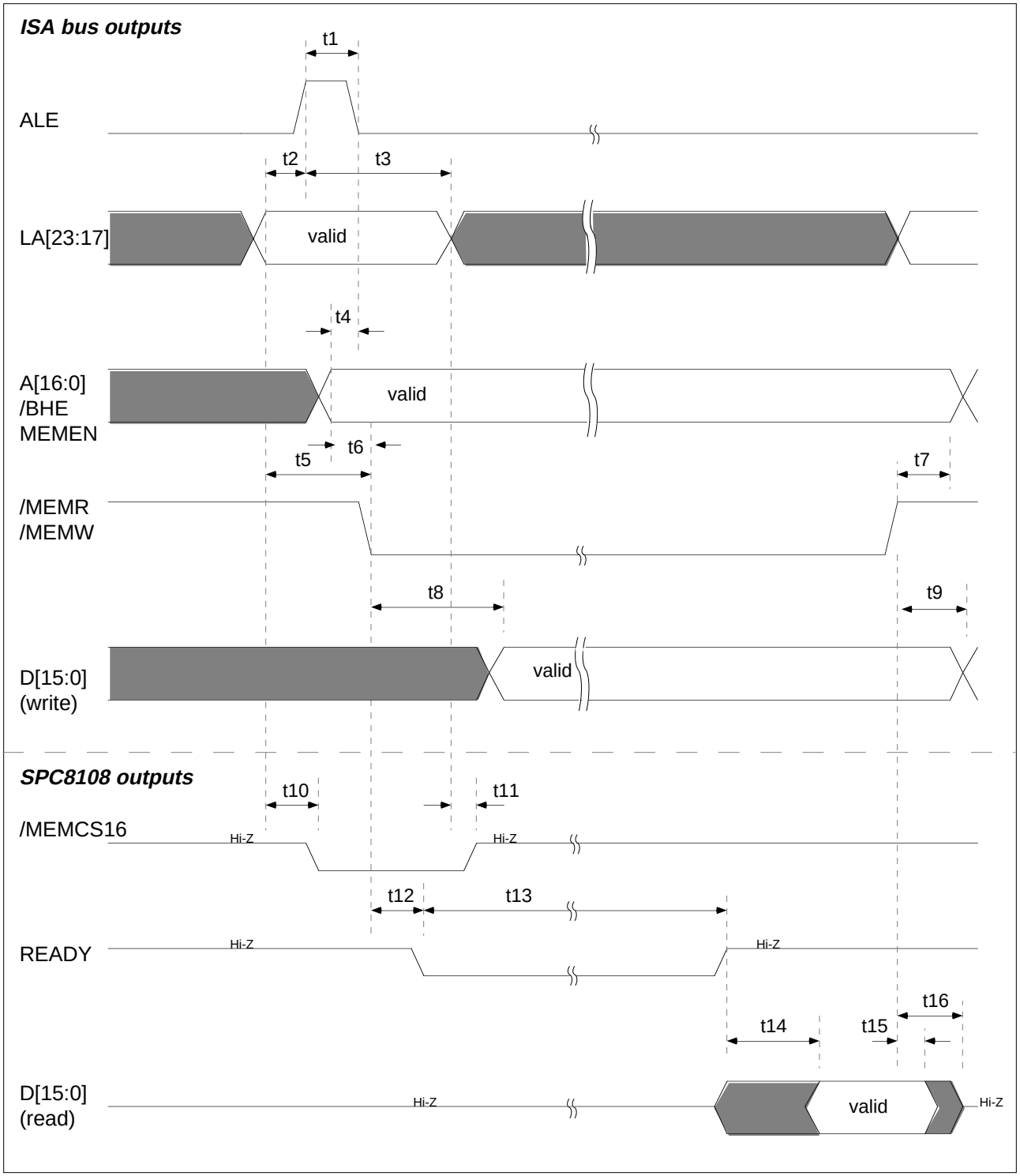

Figure 3. CPU Bus Cycle Timing - 16 Bit Memory

2. CPU BUS CYCLE TIMING - 16 BIT I/O

Symbol	Parameter	Min	Typ	Max	Units
t1	ALE pulse width	30			ns
t2	A[15:0], /BHE valid setup to I/O command negated	25			ns
t3	A[15:0], /BHE valid hold from ALE negated	10			ns
t4	/IOEN setup to I/O command asserted	10			ns
t5	/IOW command pulse width	120			ns
t5	/IOR command pulse width	180			ns
t6	valid write data setup to I/O command asserted	10			ns
t7	valid write data hold from I/O command negated	10			ns
t8	/IOCS16 asserted from A[15:0], /BHE valid			30	ns
t9	/IOCS16 hold from A[15:0], /BHE invalid	0			ns
t10	/0WS asserted from I/O command asserted (MD[5]=0 @ RESET only)			30	ns
t11	read data driven delay from read command asserted	10			ns
t12	valid read data from I/O read command asserted			150	ns
t13	read data hold from I/O command negated	5			ns
t14	read command negated to D[15:0] high-impedance			30	ns

This table refers to standard ISA CPU bus timing. When configuration input MD[5] = 1 on the falling edge of RESET, refer to section 4 for modified address timing.

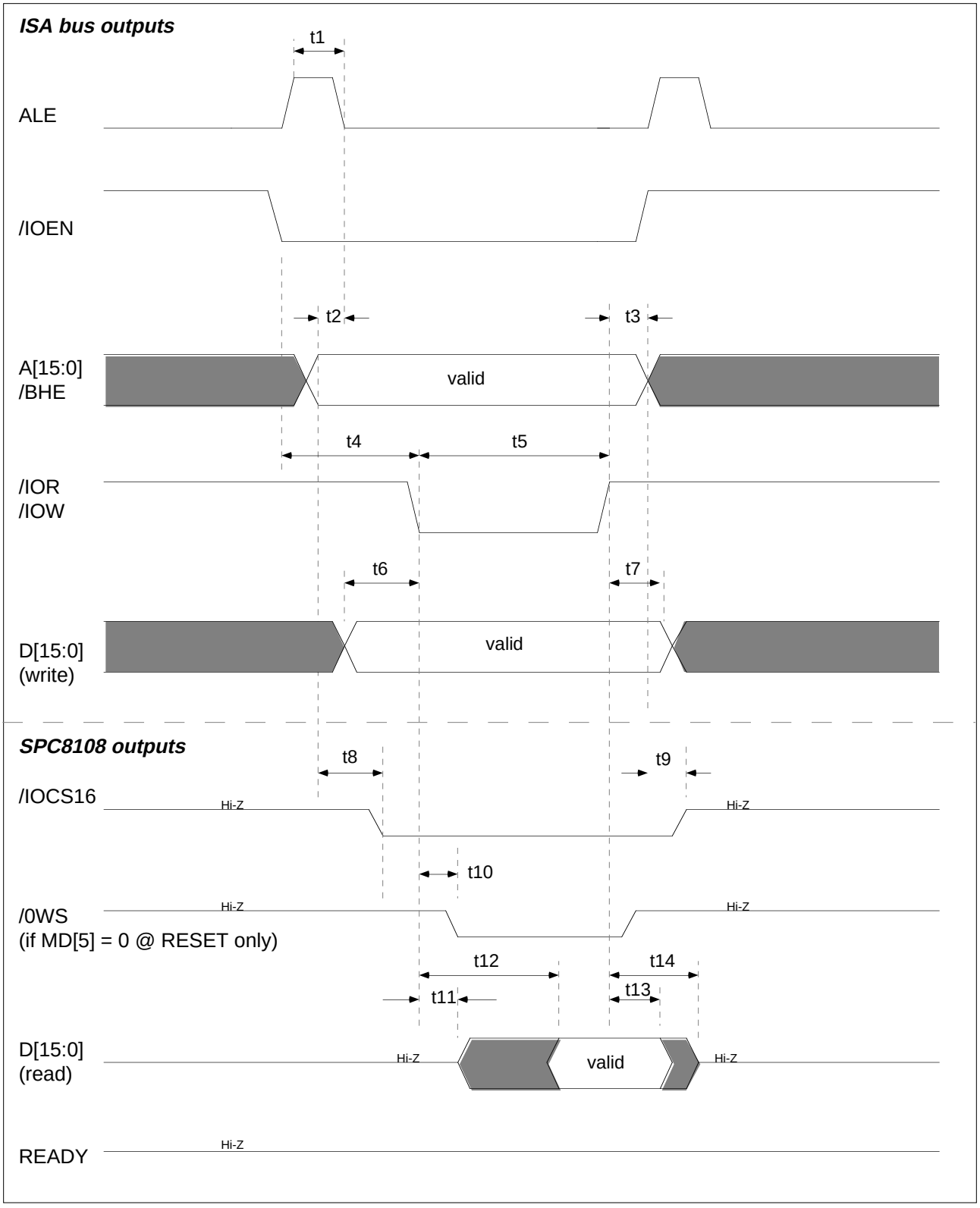

Figure 4. CPU Bus Cycle Timing - 16 Bit I/O

3. CPU BUS CYCLE TIMING—16 BIT MEMORY, MODIFIED ADDRESS TIMING

Symbol	Parameter	Min	Typ	Max	Units
t1	ALE pulse width	30			ns
t2	LA[23:17], A[16:2] valid setup to ALE asserted	0			ns
t3	LA[23:17], A[16:2] valid hold from ALE asserted	40			ns
t4	A[1:0], /BHE valid setup to ALE negated	10			ns
t5	LA[23:17], A[16:2] valid setup to memory command asserted	10			ns
t6	A[1:0], /BHE valid setup to memory command asserted	10			ns

This table refers to CPU bus timing when configuration input MD[5] = 1 on the falling edge of RESET. In this case, processor address lines PA[23:2] may be connected to address inputs LA[23:17] and A[16:2]. These inputs will be latched by the SPC8108 on the falling edge of ALE. Address inputs A[1:0] should be connected to the ISA bus address outputs A[1:0].

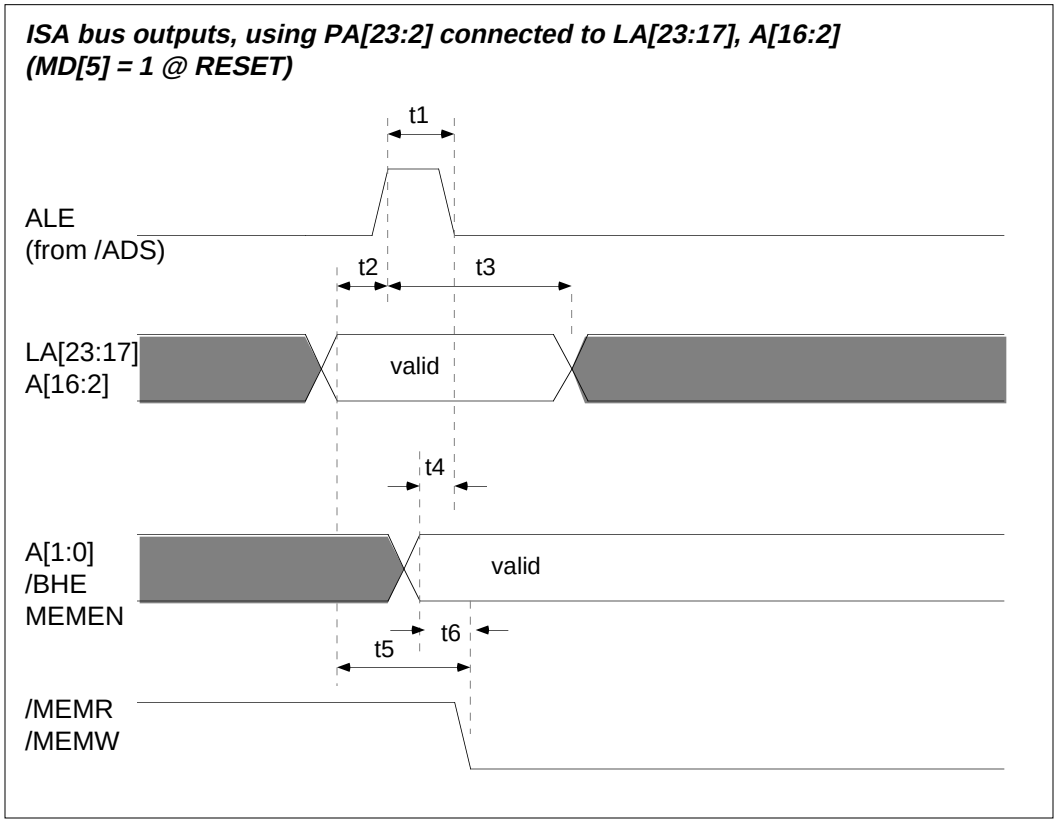

Figure 5. CPU Bus Cycle Timing - 16 Bit Memory, Modified Address Timing

4. CPU BUS CYCLE TIMING - 16 BIT I/O, MODIFIED ADDRESS TIMING

Symbol	Parameter	Min	Typ	Max	Units
t1	ALE pulse width	30			ns
t2	/IOEN active setup I/O command asserted	10			ns
t3	LA[23:17], A[16:2] valid setup to ALE asserted	0			ns
t4	LA[23:17], A[16:2] valid hold from ALE asserted	40			ns
t5	LA[23:17], A[16:2] valid setup to I/O command asserted	10			ns
t6	A[1:0], /BHE valid setup to I/O command asserted	10			ns

This table refers to CPU bus timing when configuration input MD[5] = 1 on the falling edge of RESET. In this case, processor address lines PA[23:2] may be connected to address inputs LA[23:17] and A[16:2]. These inputs will be latched by the SPC8108 on the falling edge of ALE. Address inputs A[1:0] should be connected to the ISA bus address outputs A[1:0].

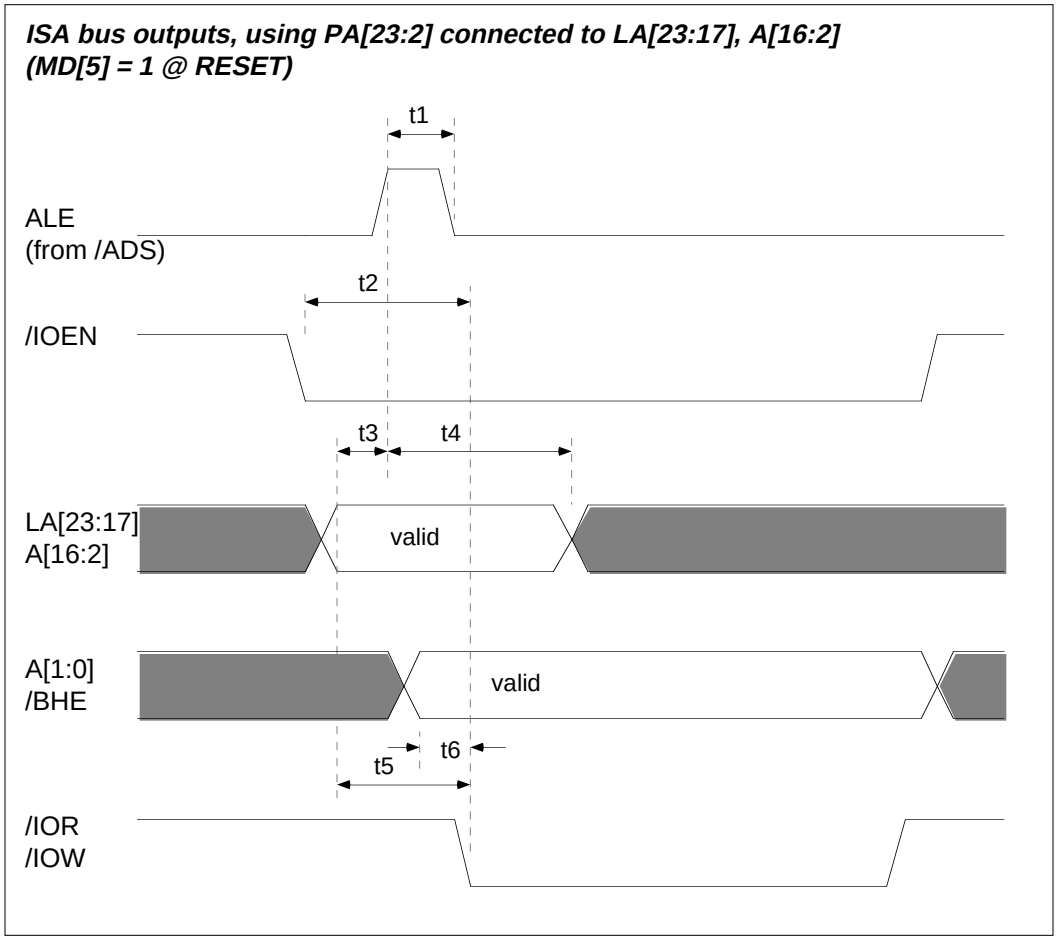

Figure 6. CPU Bus Cycle Timing - 16 Bit I/O - Modified Address Timing

5. DRAM READ CYCLE TIMING - NON-PAGE MODE

Symbol	Parameter	Min	Typ	Max	Units
t1	MA[9:0] row address setup to /RAS asserted				ns
t2	MA[9:0] row address hold from /RAS asserted				ns
t3	/RAS precharge				ns
t4	/RAS pulse width				ns
t5	/RAS asserted to /LCAS, /UCAS asserted				ns
t6	MA[9:0] column address setup to /LCAS, /UCAS asserted				ns
t7	MA[9:0] column address hold from /LCAS, /UCAS asserted				ns
t8	/LCAS, /UCAS asserted to /RAS negated				ns
t9	/LCAS, /UCAS pulse width				ns
t10	MD[15:0] read data setup to /LCAS, /UCAS negated				ns
t11	MD[15:0] read data hold from /LCAS, /UCAS negated				ns

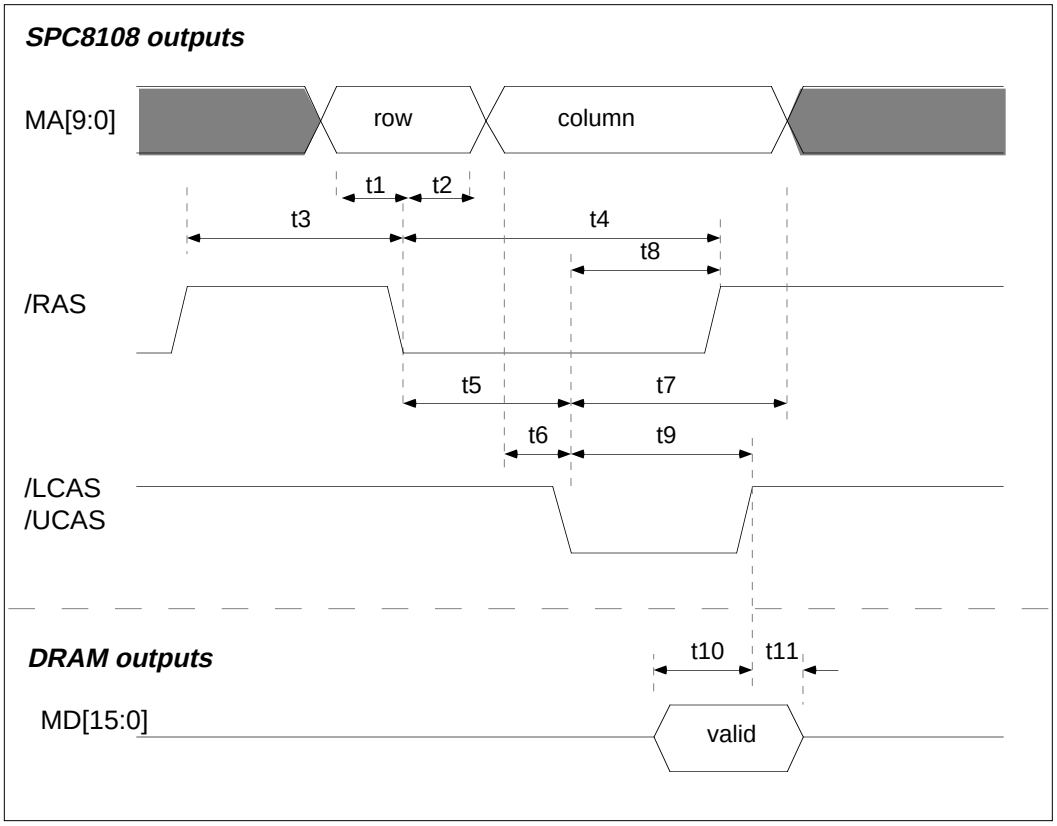

Figure 7. DRAM Read Cycle Timing - Non-Page Mode

6. DRAM READ CYCLE TIMING - PAGE MODE

Symbol	Parameter	Min	Typ	Max	Units
t1	MA[9:0] row address setup to /RAS asserted				ns
t2	MA[9:0] row address hold from /RAS asserted				ns
t3	/RAS precharge				ns
t4	/RAS pulse width				ns
t5	/RAS asserted to /LCAS, /UCAS asserted				ns
t6	MA[9:0] col addr setup to /LCAS, /UCAS asserted (1st)				ns
t7	MA[9:0] col addr hold from /LCAS, /UCAS asserted(1st)				ns
t8	/LCAS, /UCAS asserted to /RAS negated				ns
t9	/LCAS, /UCAS pulse width				ns
t10	MD[15:0] read data setup to /LCAS, /UCAS negated				ns
t11	MD[15:0] read data hold from /LCAS, /UCAS negated				ns
t12	MA[9:0] column address setup to /LCAS, /UCAS asserted (2^{nd} - n^{th} page access)				ns
t13	MA[9:0] column address hold from /LCAS, /UCAS asserted (2^{nd} - n^{th} page access)				ns
t14	/LCAS, /UCAS precharge				ns

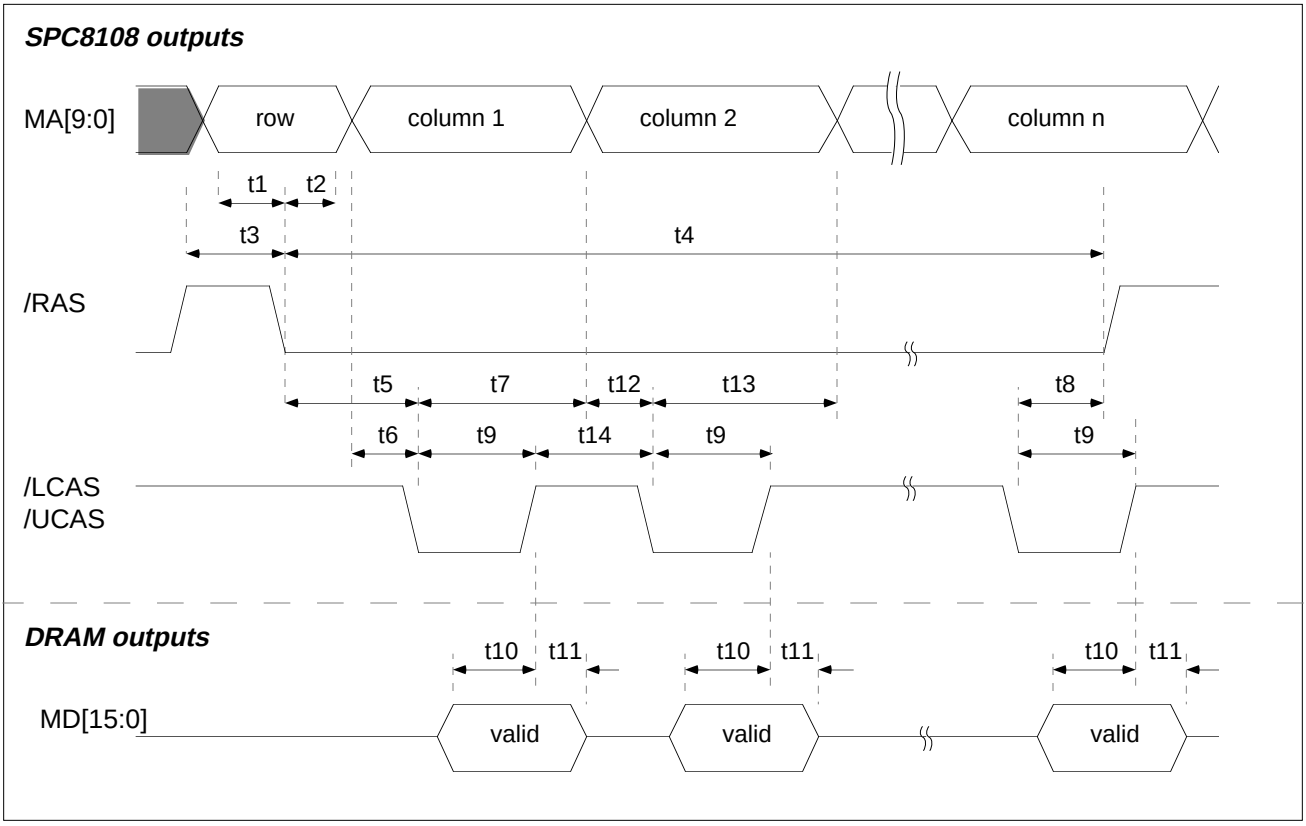

Figure 8. DRAM Read Cycle Timing - Page Mode

7. DRAM WRITE CYCLE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t1	MA[9:0] row address setup to /RAS asserted				ns
t2	MA[9:0] row address hold from /RAS asserted				ns
t3	/RAS precharge				ns
t4	/RAS pulse width				ns
t5	/RAS asserted to /LCAS, /UCAS asserted				ns
t6	MA[9:0] col addr setup to /LCAS, /UCAS asserted (1st)				ns
t7	MA[9:0] col addr hold from /LCAS, /UCAS asserted(1st)				ns
t8	/LCAS, /UCAS asserted to /RAS negated				ns
t9	/LCAS, /UCAS pulse width				ns
t10	MD[15:0] write data setup to /LCAS, /UCAS asserted				ns
t11	MD[15:0] write data hold from /LCAS, /UCAS asserted				ns
t12	MA[9:0] col addr setup to /LCAS, /UCAS asserted (2^{nd})				ns
t13	MA[9:0] col addr hld from /LCAS, /UCAS asserted (2^{nd})				ns
t14	/LCAS, /UCAS precharge				ns
t15	/WE setup to /LCAS, /UCAS asserted				ns
t16	/WE hold from /LCAS, /UCAS asserted				ns
t17	/WE pulse width				ns

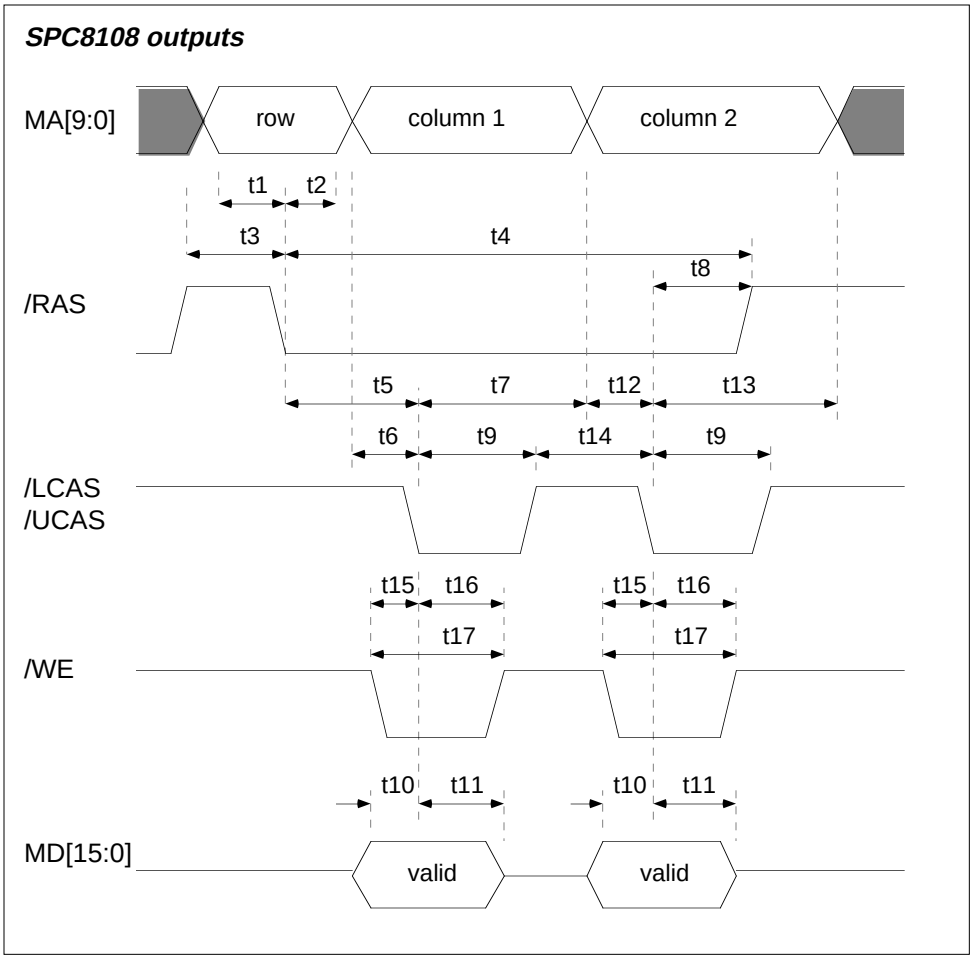

Figure 9. DRAM Write Cycle Timing

13. LCD INTERFACE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t1	YD setup to LP negated (single panel mode)	739Ts-24			ns
t1	YD setup to LP negated (dual panel mode)	1478Ts - 24			ns
t2	YD hold from LP negated (single panel mode)	13Ts-24			ns
t2	YD hold from LP negated (dual panel mode)	26Ts-24			ns
t3	LP period		752Ts-24		ns
t4	LP pulse width (Aux[0D] bit 6 =0)	5Ts-24			ns
t4	LP pulse width (Aux[0D] bit 6 =1)	6Ts-24			ns
t5	WF delay from LP negated	0		1	ns
t6	LP setup to XSCL falling edge (Aux[0D] bit 7 =0)	n/a	n/a	n/a	ns
t6	LP setup to XSCL falling edge (Aux[0D] bit 7 =1)	2Ts-24			ns
t7	LP hold from XSCL falling edge (Aux[0D] bit 7 =0)	n/a	n/a	n/a	ns
t7	LP hold from XSCL falling edge (Aux[0D] bit 7 =1)	4Ts-24			ns
t7*	XSCL falling edge to LP falling edge (Aux[0D] bit 7 = 0 only)	103Ts-24			ns
t8	LP negated to XSCL falling edge (Aux[0D] bits 7,6 = 00)	9Ts-24			ns
t8	LP negated to XSCL falling edge (Aux[0D] bits 7,6 =11)	4Ts-24			ns
t9	XSCL period	8Ts-24			ns
t10	XSCL low pulse width	4Ts-24			ns
t11	XSCL high pulse width	4Ts-24			ns
t12	UD[3:0], LD[3:0] setup to XSCL falling edge	4Ts-24			ns
t13	UD[3:0], LD[3:0] hold from XSCL falling edge	4Ts-24			ns
t14	LP negated to XSCL rising edge (Aux[0D] bits 7,6 = 00)	5Ts-24			ns
t14	LP negated to XSCL rising edge (Aux[0D] bits 7,6 = 11)	0			ns

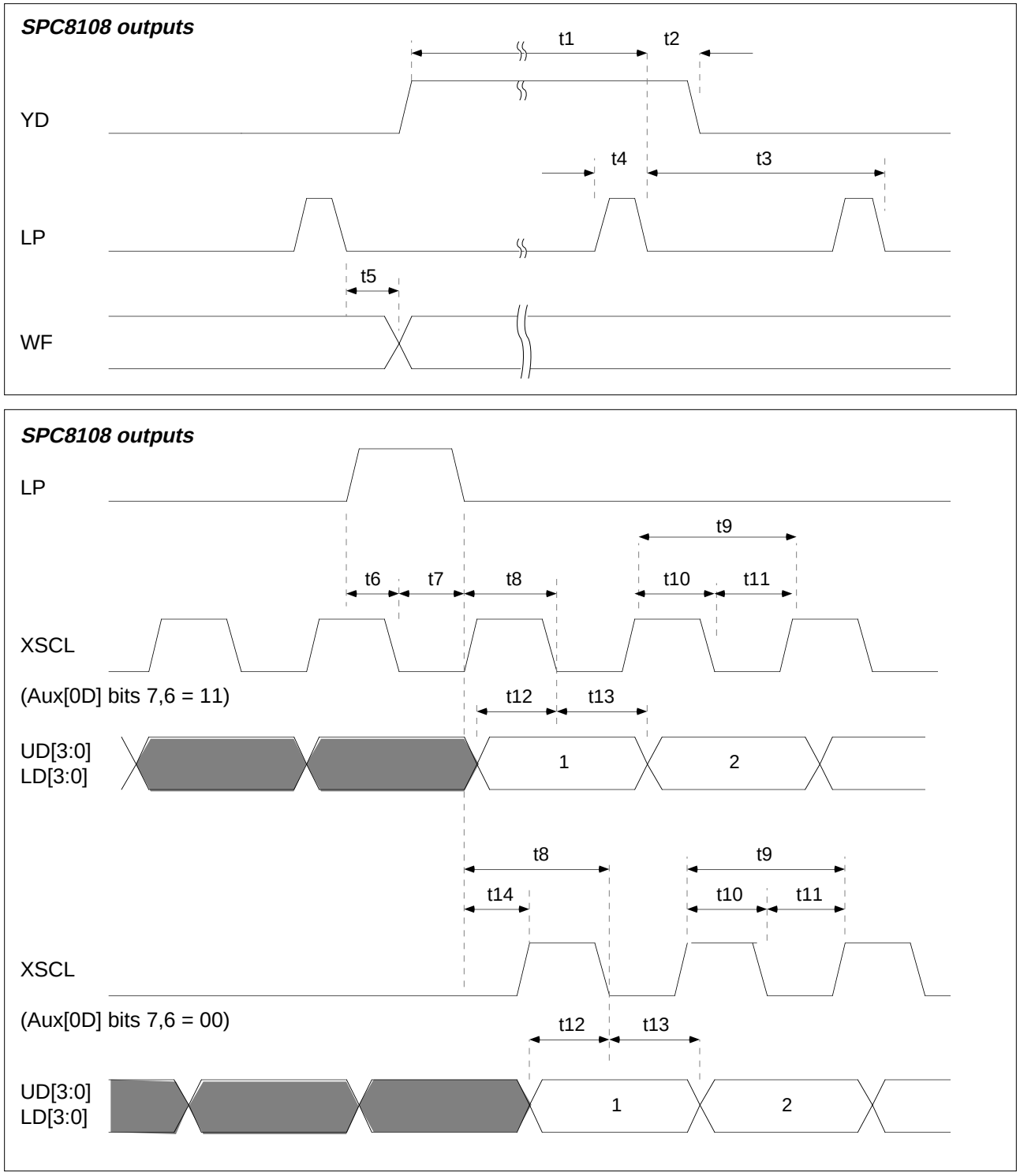

Figure 15. LCD Interface Timing

SPC8108F$_{0B}$ LCD VGA Controller

I/O Register Summary

Drawing Office No.

Revised: 4/8/93

3.0 I/O REGISTER SUMMARY

This section summarizes the I/O registers of SPC8108 - only those register bits supported by the chip are shown. Note that the functionality of a subset of the IBM VGA standard registers is supported, with an additional set of Auxiliary Registers containing SPC8108 specific functions. Only details of the register functions which are not part of the VGA standard definition are given below.

Note: • Unless otherwise noted, all read/write register bits are cleared to 0 after a RESET.
• All register bits marked as "n/a" are undefined. There is no effect if they are written to, and reading these bits will return an undefined value.

3.1 AUXILIARY REGISTERS

Auxiliary Index/Data Register 3DE RW 3DF RW							
n/a	n/a	n/a	n/a	Auxiliary Index Bit 3	Auxiliary Index Bit 2	Auxiliary Index Bit 1	Auxiliary Index Bit 0

00 Extended Function Register 0 RW							
			Test Mode Enable (must be 0)	n/a (reserved)	IRQ Output Enable	Multi-Font Enable	LCD B Reg Program Enable

Test Mode Enable

The Test Mode Enable bit must be set to 0 for normal operation. When set to 1, the chip is placed into device test mode and the test input and test output selector bits in Auxiliary Register 04H are enabled.

IRQ Output Enable

When the IRQ Output Enable bit is set to 0, the IRQ output is held in a high impedance state. When this bit is set to 1, the IRQ output pin is enabled and will be driven to indicate the Vertical Retrace interrupt status.

Multi-Font Enable

When the Multi-Font Enable bit is set to 0, normal text mode font selection is enabled. When this bit is 1, it allows bits 0 to 2 of the attribute byte (foreground color) to select one of eight simultaneously displayable fonts. In this case the attribute byte foreground color bits (normally bits 0 to 2) are forced to 1, the font selection bit (bit 3) is not used, and the blink/intensity bit (bit 7) functions normally.

LCD B Registers Program Enable

This bit is used to access the hidden LCD Panel Size and Vertical Panel Size registers (LCD B Registers), which reside in the same address space as their CRT mode conterparts. These hidden timing registers only have an effect when the LCD is the active display. When this bit is set to 0, accesses to CRTC Register

[01] affect the normal Horizontal Total Register, and accesses to CRTC Register [12] affect the normal Vertical Display Enable End Register. When this bit is set to 1, then the “B set” registers are enabled, and accesses to CRTC Register [01] affect the Horizontal Panel Size Register, and accesses to CRTC Register [12] affect the Vertical Panel Size Register. These “B Set” registers are used only for LCD only mode (Aux[0B] bits 1,0 = 01).

01 LCD Support Register 0 RW							
n/a (reserved)	Slow Blink Select	n/a (reserved)	Grn-only / NTSC GS Weighting	n/a (reserved)	Reverse/ Normal Display	Auto-Centering Enable	Single/ Dual Panel

Slow Blink Select

This bit is used to select the blink rate of the cursor and text in text modes and graphics pixels in graphics modes, if blink is enabled. If this bit is set to 0, the cursor, text or graphics pixels blink at their normal rates. If this bit is set to 1, then everything blinks at half their respective normal rates. This option may be used to make the blinking cursor more visible on some LCD panels. Note that in both normal and slow settings, the text mode cursor always blinks at twice the frequency of any blinking characters (i.e. cursor blink frequency = 2 x blink frequency of text).

Green-only / NTSC GS Weighting Select

This bit is used to select one of two possible gray scale weighting functions to be applied to RGB data as it is written to the internal 256x6 LCD gray scale lookup table. When this bit is set to 0, RGB data values are mapped to gray values using NTSC weighting. When this bit is set to 1, the green component of the RGB data is used as the gray value. See section on LCD gray scale lookup table for details.

Reverse/Normal Display

When the Reverse/Normal Display bit is 0, then normal display attributes are enabled. When this bit is 1, then inverse video is displayed on the LCD display. This bit also affects the overscan color as set in bit 5 of this register. This bit has no effect on the image displayed on the CRT display.

Auto-Centering Enable

This bit is used to control the auto-centering function which allows display modes with less than 480 lines to be vertically centered on the LCD panel, provided that vertical expansion is not enabled (see Auxiliary Register 07). If vertical expansion is not enabled and the Auto-Centering Enable bit is 0, then all modes will be displayed with the first line at the top of the panel. If this bit is set to 1 and vertical expansion is not enabled, then for all modes hardware will adjust the vertical position of the first line of the display so that the image is centered vertically on the panel. If vertical expansion is active (i.e. all conditions for a vertical expansion mode are met; see appropriate bit description in Auxiliary Register 7), then the setting of this bit is ignored and auto-centering is disabled. If CRT mode is enabled (Aux[0B] bit 1 = 1) then auto-centering is disabled and this bit has no effect.

Single/Dual Panel

The Single/Dual Panel bit is used to configure the chip timing for the correct LCD panel type. When this bit is 0, then dual panel mode is enabled. When this bit is 1, then single panel mode is enabled.

02 LCD Support Register 1 RW							
CRT Sprite Enable	n/a	n/a	4/8 Bit Panel Interface	PSM4/S Refresh Clk Select 1	PSM4/S Refresh Clk Select 0	LCD Signal PS Mode State	32/4 msec Refresh Select

CRT Sprite Enable

The CRT Sprite Enable bit is used to enable or disable the sprite display on the CRT monitor. When this bit is set to 0, the sprite will not be displayed on the CRT monitor. When this bit is set to 1, the sprite circuitry for the CRT display is enabled and it will be possible to display the sprite on the CRT monitor, provided that the value on MD[13] = 0 at RESET to allow use of the OL1 and OL0 output pins.

4/8 Bit Panel Interface

Tbe 4/8 Bit Panel Interface bit configures the LCD output data for either 4 bit or 8 bit single panels. When this bit is set to 0, then in LCD mode, an 8 bit single panel interface is provided with 8 bit pixel data output on UD[3:0] (msbits) and on LD[3:0] (lsbits). When this bit is set to 1, then in LCD mode a 4 bit single panel interface is provided, where 4 bit pixel data is output only on UD[3:0], and the LD[3:0] outputs are held low. Note that this bit must be set to 0 for all dual panel modes.

PSM4/S Refresh Clock Select 1-0

These bits are used to select the refresh clock source during Power Save Mode 4 or Suspend mode, according to the following table:

PSM4/S Refresh Clock Select 1	PSM4/S Refresh Clock Select 0	Refresh Clock Source in Power Save Mode 4 and Suspend
0	0	CLK1I, CLK2I
0	1	MEMEN
1	0	Self Refresh
1	1	PDCLK

CLK1I, CLK2I

When this option is selected, then the active pixel input clock (CLK1I or CLK2I) is used to generate all Power Save mode refresh timing. The active pixel clock is determined by the Clock Select bits in Misc Output Register (3C2), and by the LCD Enable and CRT Enable bits in Auxiliary Register [0B].

MEMEN

When this option is selected, then the MEMEN input pin is used as the clock source in Power Save Mode 4 and Suspend.

Self Refresh

This option may only be used when the DRAMs installed are capable of self-refresh. When this option is selected, during Power Save Mode 4 and Suspend mode, the DRAM control lines are driven in such a manner to cause the DRAM to enter self-refresh mode. When not in self refresh mode, then CAS-before-RAS refresh cycles are used during Power Save Mode 4 or Suspend mode. Note that regardless of the setting of these bits, CAS-before-RAS refresh cycles are used during active mode and Power Save Modes 1, 2 and 5.

PDCLK

When this option is selected, the PDCLK input pin is used as the clock source in Power Save Mode 4 and Suspend. For lowest possible DRAM power consumption, this input clock should have as short as possible low duration (but > min RAS pulse width). For normal refresh rate DRAM (256cycle/4ms), this input should be a 64kHz clock source. It is possible to use a 32 kHz 50% duty cycle clock for PDCLK - see pinout section for details.

LCD Signal PS Mode State

The LCD Signal PS Mode State bit controls the states of the LCD interface signals (UD[3:0], LD[3:0], XSCL, LP, YD, WF) when the chip goes into a power save mode. When this bit is 0, the LCD signals are put into a high-impedance state when a power save mode is entered. When this bit is set to 1, then when the chip is in a power save mode, the LCD interface signals will be forced low. On RESET, this bit is set to 1.

32/4 msec Refresh Select

The 32/4msc Refresh Select bit is used to select 256 cycle/4 msec or 256 cycle/32msec DRAM refresh timing in all modes of operation. When this bit is 0, then 4 msec refresh timing is generated. When this bit is 1, then 32msec refresh timing is generated. In active mode and Power Save Modes 1, 2 and 5, this 4 or 32 msec refresh timing is generated from the selected CLKI source (28MHz for LCD modes, 25MHz or 28MHz for CRT modes as selected by Clock Select bits in Misc Output Register 3C2H). For Power Save Mode 4 and Suspend, this 4 or 32 msec refresh timing is generated from the active CLKI, from MEMEN input, or the PDCLK input, as selected by Aux[02] bits 3,2.

03 Power Save Register RW							
n/a	n/a	Clock Slow Down	Oscillator Disable	Aux Reg Only Decode	Power Save Mode Select Bit 2	Power Save Mode Select Bit 1	Power Save Mode Select Bit 0

Clock Slow Down

The Clock Slow Down bit is used to provide additional power savings in some LCD modes. When this bit is set to 1, then the active internal clock rate is reduced by 20%. When this bit is set to 0, then the internal clock rate equals the input clock rate. This bit is intended for use in Power Save Mode 5. If CRT mode is enabled (Aux[0B] bit 1 = 1), then this bit is ignored and has no effect.

Oscillator Disable

The Oscillator Disable bit is used to control the operation of the internal clock oscillator connected to the active selected external 2-terminal crystal. When this bit is 0, then the active oscillator is enabled. When this bit is 1, then the active oscillator is disabled and the corresponding CLKI input is masked off. The active clock is defined as either the 28 MHz clock (CLK2I) for LCD mode, or for CRT modes the clock selected by the Clock Select bits in Misc. Output Register 3C2H bits 3,2. In all modes, the unselected clock oscillator is automatically disabled.

Aux Reg Only Decode

The Aux Reg Only Decode bit is intended for use by power save mode software. In power save modes, this bit may be set to 1 to disable all I/O access decoding except to the Auxiliary Registers. Note that setting this bit to 1 would normally be useful only when in Power Save Modes 3 or 4. At all other times this bit should be set to 0 to enable all I/O address decoding.

Power Save Mode Select Bits 2-0

These bits are used to select 1 of 5 software power save modes. When these bits are set to 000, 110, or 111 then the chip operates in normal active mode. Binary values of 001, 010, 011, 100, or 101 written to these bits cause the chip to enter power save modes 1, 2, 3, 4 or 5 respectively. If the /SUSPEND input pin is low, then the power save mode setting in this register is ignored.

04 General Storage and Test Register 0 RW							
Test Input Select Bit 3	Test Input Select Bit 2	Test Input Select Bit 1	Test Input Select Bit 0	Test Output Select Bit 3	Test Output Select Bit 2	Test Output Select Bit 1	Test Output Select Bit 0

General Storage and Test Bits

For normal operation, Auxiliary Register 00 bit 4 (Test Mode Enable) is set to 0, and then the General Storage and Test Register can be used to provide 8 bits of read/write temporary storage. In normal operation mode these bits have no effect on hardware.
When the Test Mode Enable bit is set to 1, then the chip is placed in a special test mode, and this register is used to select various internal test functions.

05 Extended Function Register 1 RW							
n/a (reserved)	n/a	Sprite/HW Cursor Enable	n/a (reserved)	Start Address Bit SA16	Extended Display Page Enable	Overlay / Ext Display Page Select	CPU Upper 256K Access Enable

Sprite / HW Cursor Enable

This bit is used to enable the sprite and hardware cursor functions. When this bit is set to 0, the sprite / hardware cursor function is disabled. When this bit is set to 1, the sprite / hardware cursor is enabled - see Section on sprite / hw cursor registers for more information.

Start Address Bit SA16

This bit is used to set the most significant diplay start address bit when utilizing the upper 256K bytes of display memory to provide the Extended Display Page function (see below). Along with the lower 16 bits of start address in CRTC registers 0C and 0D, this bit allows setting the start address of the image displayed to be anywhere in the 512K address space. For this bit to have an effect, the Extended Display Page Enable bit must be set to 1 and the Overlay/Extended Display Page Select bit must be set to 0.

Extended Display Page Enable

This bit is used to enable the Extended Display Page function. This function allows the display memory to wrap into the upper 256K bytes, and for 256K bytes of memory to be displayed starting anywhere in the entire 512K byte extended display memory space. If this bit is set to 1 and the Overlay / Ext Display Page Select bit is set to 0, then the extended display page function is enabled. If this bit is set to 0 or if the Overlay / Ext Display Page Select bit is set to 1, then the extended display page function is disabled, and the Overlay Modulation function may be enabled.

Overlay / Ext Display Page Select

This bit is used to select between the two options which utilize the upper 256K bytes of display memory available. When this bit is 0, if the Extended Display Page Enable bit is set to 1, then the Extended Display Page function is selected. If this bit is set to 1, then the Overlay function is enabled. Enabling the

Overlay function causes the image stored in the upper 256K bytes of display memory to be overlayed with the primary image in the lower 256K bytes of memory, as controlled by the bits in the Overlay Modulation Register.

CPU Upper 256K Access Enable

This bit is used to enable CPU accesses into the upper 256K bytes of display memory. When this bit is set to 1, the CPU can access the upper half of display memory through memory addresses B0000 - BFFFF. The lower 256K of video memory can still be accessed at addresses A0000 - AFFFF. When this bit is set to 0, only the lower 256K bytes of display memory can be accessed by the CPU. Note that the Upper Page Swap Enable bit can be used to swap the upper/lower page addresses. This function will only be useful in planar graphics modes.

06 Overlay Modulation Register RW							
Overlay Modulation Bit 7	Overlay Modulation Bit 6	Overlay Modulation Bit 5	Overlay Modulation Bit 4	Overlay Modulation Bit 3	Overlay Modulation Bit 2	Overlay Modulation Bit 1	Overlay Modulation Bit 0

Overlay Modulation Bits 7-0

The Overlay Modulation bits are used to control the Overlay function. This function allows the image stored in the upper 256K bytes of display memory to be overlayed with the primary image in the lower 256K bytes of memory. When the Overlay / Ext Display Page Select bit is set to 0, this register has no effect. When the Overlay / Ext Display Page Select bit is set to 1, the Overlay function is enabled and these bits will control the modulation of the two images from each half of the 512K bytes of display memory. An 8 vertical frame cycle used to modulate the overlay and primary image and the 8 bits in this register are each used to represent one frame in sequence of the 8 frame cycle. Each 1 in this register causes the overlay image to be displayed for the corresponding frame in the 8 frame cycle, and each 0 causes the primary image to be displayed for the corresponding frame. For example, the value 01010101 in this register will cause the the overlay and primary images to be alternately displayed every other frame. If all bits in this register are set to 0, then only the primary image will be displayed, and similarly if all bits in this register are set to 1, then only the overlay image will be displayed.

07 Extended Function Register 2 RW							
Mode 13H 32/64 Gray Select	Dithering Control	n/a	Graphics VExpand Start Bit 2	Graphics VExpand Start Bit 1	Graphics VExpand Start Bit 0	Graphics VExpand Enable	Text VExpand Enable

Mode 13H 32/64 Gray Select

This bit allows the selection of 32 or 64 gray shades on the LCD panel when in mode 13H (Graphics Controller Mode Register inded 05, bit 6 Mode13H Select = 1). When this bit is 0, 64 gray shades are displayed in mode 13H (16 gray levels by FRM + dithering). When this bit is 1, then 32 gray shades are displayed in mode 13H (16 gray levels by FRM + dithering). This bit has no effect on an image displayed on a CRT display.

Dithering Control

This bit is used to control the dithering logic for the LCD display. When this bit is 0, dithering is enabled for mode 13H (Graphics Controller register 05 bit 6 = 1) and disabled for other modes - this is the normal setting to provide 64 gray shades in mode 13H. When this bit is set to 1, then dithering is disabled for mode 13H. This bit has no effect on an image displayed on a CRT display.

Graphics VExpand Start Bits 2-0

These bits allow some flexibility in the graphics mode vertical expansion function. If graphics vertical expansion is enabled (see below), then these bits determine the position (0-5) of the first duplicated line on the LCD display. Values of 6 or 7 programmed into this register are invalid and vertical expansion will not occur in these cases. If CRT mode is enabled (Aux[0B] bit 1 = 1) then vertical expansion is disabled and this bit has no effect. Note that although vertical expansion will not occur when these bits are programmed to values 6 or 7, autocentering will still be disabled.

Graphics VExpand Enable

This bit is used to enable vertical expansion of 400 line graphics modes on the LCD display, using selective line duplication. If this bit is 0, then vertical expansion of graphics modes is disabled. If this bit is set to 1, then 400 line graphics modes are expanded vertically to fill the screen. All the following conditions must be true for graphics vertical expansion to occur:

1) Graphics VExpand Enable = 1
2) 400 line mode set, i.e. CRTC register 12H and associated overflow bits = 18FH
3) graphics mode set, i.e. Graphics Controller register 06H bit 0 = 1
4) Graphics VExpand Start Bits 2:0 must be programmed to a value from 0 to 5 inclusive

If a 400 line graphics mode is not set, then graphics expansion will not occur and this bit will have no effect. Note that if all conditions for graphics vertical expansion are met, then the Auto Centering Enable bit (Auxiliary Register 01 bit 1) is ignored and autocentering is disabled.

If CRT mode is enabled (Aux[0B] bit 1 = 1) then graphics vertical expansion is disabled and this bit has no effect.

Text VExpand Enable

This bit is used to enable vertical expansion of 400 line text modes on the LCD display, using selective line duplication. If this bit is 0, then vertical expansion of text modes is disabled. If this bit is set to 1, then 400 line text modes are expanded vertically to fill the screen, provided the following conditions are true:

1) 16 point font is set, i.e. the 5 least significant bits of CRTC register 09H = 0FH
2) 400 line mode is set, i.e. CRTC register 12H and associated overflow bits = 18FH
3) text mode is set, i.e. Graphics Controller register 06H bit 0 = 0.

If these conditions are not all met, then text expansion will not occur and this bit will have no effect. Note that if this bit is set to 1, then the Auto Centering Enable bit (Auxiliary Register 01 bit 1) is ignored and autocentering is disabled.

If CRT mode is enabled (Aux[0B] bit 1 = 1) then text vertical expansion is disabled and this bit has no effect.

08 Primary Revision Code Register RO							
Primary Revision Code Bit 2	Primary Revision Code Bit 1	Primary Revision Code Bit 0	n/a	n/a	Monitor ID Bit 2	Monitor ID Bit 1	Monitor ID Bit 0

Primary Revision Code Bits 2-0

The Primary Revision Code Bits 2 to 0 are read-only bits permanently set to 1. The current revision code of the chip is a combination of the primary and secondary revision code values. The secondary revision code bits are contained in register 0FH.

Monitor ID Bits 2-0

The Monitor ID Bits allow software to read the status on the monitor sense input pins MS[2:0]. These inputs are not latched and have internal pullups, so if nothing is connected to them these register bits will read 111.

09 Sprite Write Select Register RW							
n/a	n/a	n/a	n/a	Sprite Page Select	Sprite Logical Plane Sel	Upper Page Swap Enable	Sprite Write Mode Enable

Sprite Page Select

This bit is used to select the current sprite page (page 0 or 1) accessed at the A000H address segment when the sprite write mode is enabled. The mapping of the sprite pages to the Sprite Page Select bit and the Upper Page Swap Enable bit are given in the following table:

Upper Page Swap Enable	Sprite Page Select	Addressable Sprites
0	0	0 to 127
0	1	128 to 255
1	0	256 to 383
1	1	384 to 511

Note: Sprites 0 to 255 reside in standard VGA display memory space and should not be used.

Sprite Logical Plane Select

This bit is used in sprite write mode to select which sprite bit plane is currently being written. When this bit is set to 1, logical bit plane 1 is selected, and when this bit is set to 0, logical bit plane 0 is selected.

Upper Page Swap Enable

The Upper Page Swap Enable bit is used to swap access addresses for the upper and lower 256 sprites. When this bit is set to 1, the upper 256 sprites residing in the B000H address segment can be addressed at

A000H. When this bit is set to 0, the upper 256 sprites are addressed at B000H. The recommended setting for this bit is 1 when writing sprite data.

Sprite Write Mode Enable

This bit is used to enable sprite write mode. When this bit is set to 1, the Graphics Controller write mode logic is disabled and CPU data can be written directly to the selected sprite plane. When this bit is set to 0, the Graphics Controller write mode logic functions normally on all CPU write data.

0A General Storage Register 1 RW							
General Storage Bit 7	General Storage Bit 6	General Storage Bit 5	General Storage Bit 4	General Storage Bit 3	General Storage Bit 2	General Storage Bit 1	General Storage Bit 0

General Storage Bits

The General Storage Register 1 can be used to provide 8 bits of read/write temporary storage. These bits have no effect on hardware.

0B Extended Function Register 3 RW							
n/a	n/a	n/a	Ext. DAC Ctl Reg Wr Enable	Ext. DAC RS2 Bit	Ext. DAC Read Select	CRT Enable	LCD Enable

Ext. DAC Control Register Write Enable

This bit is used to control the logic level on output signal D477. If this bit is set to 0, then the D477 output is driven low. If this bit is set to 1, then the D477 output is driven high. Note that the logic level on this pin is also controlled by power save logic and CRT mode hardware and this bit setting may be ignored in some modes. This bit should be set to 1 before writing to the external RAMDAC control register, and should be reset to 0 after the control register is written.

Ext. DAC RS2 Bit

This bit is used to control the logic level on output signal RS2. If this bit is set to 0, then the RS2 output is driven low. If this bit is set to 1, then the RS2 output is driven high. This bit should be set to 1 before the CPU accesses the external RAMDAC overlay and control registers. This bit should be set back to 0 for normal operation so that the standard RAMDAC palette registers may be accessed. When this bit is set to 1, reads and writes to I/O addresses 3C6H - 3C9H will not access the internal LCD LUT registers.

Ext. DAC Read Select

The External DAC Read Select bit is used to enable reads of the external RAMDAC registers. When this bit is set to 0, reads to 3C6-3C9 return values from the internal LCD gray scale lookup table registers. When this bit is set to 1, then reads to these addresses are decoded as external RAMDAC reads. This bit should be set to 1 for CRT modes.

CRT Enable

When the CRT Enable bit is set to 1, CRT display hardware is enabled. When this bit is set to 0, CRT display hardware is disabled. This bit will be initialized to 0 on RESET.

LCD Enable

When the LCD Enable bit is set to 1, LCD display hardware is enabled. When this bit is set to 0, LCD display hardware is disabled. This bit will be initialized to 0 on RESET. Note that when LCD only is enabled (LCD Enable = 1, CRT Enable = 0), the active pixel clock is forced to the CLK2I input, i.e. 28.322MHz).

0C Configuration Readback Register RO							
MD12 Status on Reset RO	MD11 Status on Reset RO	MD10 Status on Reset RO	MD9 Status on Reset RO	MD3 Status on Reset RO	MD2 Status on Reset RO	MD1 Status on Reset RO	MD0 Status on Reset RO

MD[12:9] Status on Reset

These are read-only bits which may be used for inputting power-up reset information to be read by software. On the falling edge of the RESET input, the logic values on the MD[12:9] pins are latched into the chip and then may be read in this register. These bits have no effect in hardware. Internal pullups on these input pins ensure that if nothing is connected externally to these inputs, then these register bits will read 1111.

MD[3:0] Status on Reset

These are read-only bits which may be used for inputting power-up reset information to be read by software. On the falling edge of the RESET input, the logic values on the MD[3:0] pins are latched into the chip and then may be read in this register. These bits have no effect in hardware. Internal pullups on these input pins ensure that if nothing is connected externally to these inputs, then these register bits will read 1111.

0D LCD Support Registers 2 RW							
XSCL Enable	LP Timing Select	WF Count Bit 5	WF Count Bit 4	WF Count Bit 3	WF Count Bit 2	WF Count Bit 1	WF Count Bit 0

XSCL Enable

This bit is used to adjust the XSCL shift clock output timing. When this bit is set to 0, XSCL is masked off during the horizontal non-display period. When this bit is set to 1, XSCL is not masked off during the horizontal non-display period. Refer to the A.C. timing characteristics section and the LCD panel manufacturer's specification to determine the correct setting of this bit.

LP Timing Select

This bit is used to adjust the LP latch pulse output timing. When this bit is set to 0, then the LP latch pulse falling edge occurs 9 clock periods before the falling edge of the shift clock (XSCL). When this bit is set to 1, then the LP latch pulse falling edge occurs 4 clock periods before the falling edge of the shift clock. Refer to the A.C. timing characteristics section and the LCD panel manufacturer's specification to determine the correct setting of this bit.

WF Count Bits 5-0

These bits are used to adjust the WF output signal period. The binary value stored in these bits represents the number of LP pulses - 1 between toggles of the WF output. The power up reset value of these bits is 20H. A value of 0 programmed in these bits causes the WF output to toggle every frame. Values of 01H - 3FH programmed in these bits result in WF toggling every 1+n LP pulses.

0E Auxiliary Enable Register RW							
n/a	n/a	n/a	Auxiliary Enable Code Bit 4	Auxiliary Enable Code Bit 3	Auxiliary Enable Code Bit 2	Auxiliary Enable Code Bit 1	Auxiliary Enable Code Bit 0

Auxiliary Enable Code Bits 4-0

The Auxiliary Enable Register can be used to prevent application software from accidentally overwriting the Auxiliary Registers (3DF index 0-F). When disabled, the only Auxiliary Registers that can be accessed are the Auxiliary Index Register (3DEH) and the Auxiliary Enable Register (3DFH index 0EH). The Auxiliary Registers are disabled by writing any value to the Auxiliary Enable Register (index 0EH), including the enable code 1AH (the upper 3 bits of the enable byte are ignored). The Auxiliary Registers are enabled for access after the enable code 1AH is written to and then read back from the Auxiliary Enable Register.

After a RESET, the Auxiliary Registers are disabled.

0F Secondary Revision Code Register RO							
Secondary Revision Code Bit 7	Secondary Revision Code Bit 6	Secondary Revision Code Bit 5	Secondary Revision Code Bit 4	Secondary Revision Code Bit 3	Secondary Revision Code Bit 2	Secondary Revision Code Bit 1	Secondary Revision Code Bit 0

Secondary Revision Code Bits 7-0

The secondary revision code bits are read-only bits that are permanently fixed to the current revision code of the chip. Note that the primary revision code bits 2-0 in the Primary Revision Code Register (index 08) are always set to 1. For the TS revision of the chip, the Secondary Revision Code Register will contain the value 20 hex.

3.2 MISCELLANEOUS REGISTERS

Miscellaneous Output Register							
3C2 W 3CC R							
VRTC Polarity	HRTC Polarity	Odd/Even Page bit	n/a	Clock Select Bit 1	Clock Select Bit 0	Dummy En DRAM (see note)	3Dx/3Bx Select

Note: bit 1 of this register is a dummy read/write bit that has no effect in hardware. This read/write bit is provided for compatibility of some software which expects to read valid setting of this VGA standard bit.

Clock Select Bits 1-0

These bits are used to select which clock input (CLK1I or CLK2I) is used as the active pixel clock. For normal operation, the CLK1I input should be connected to a 25.175MHz crystal or oscillator, and the CLK2I input should be connected to a 28.322MHz crystal or oscillator.

Clock Select Bit 1	Clock Select Bit 0	Clock input selected
0	0	CLK1I (25.175 MHz)
0	1	CLK2I (28.322 MHz)
1	0	CLK1I (25.175 MHz)
1	1	CLK2I (28.322 MHz)

Note that for LCD only operation (Aux[0B] bits 1:0 = 01), the active pixel clock is forced to 28.322MHz (CLK2I) and the setting of the above bits is ignored. For any other setting of Aux[0B] bits 1:0, the Clock Select bits determine the active pixel clock. The internal oscillator for the inactive clock is automatically disabled in hardware.

Input Status Register 0							
3C2 R							
CRTC Vert Interrupt Status	n/a	n/a	n/a	n/a	n/a	n/a	n/a

Input Status Register 1							
3DA R							
n/a	n/a	n/a	n/a	Vertical Retrace Status	RO status Read 1	RO status Read 0	Display Enable Status

Video Subsystem Enable Register
3C3 RW

n/a	n/a	n/a	n/a	n/a	n/a	n/a	Video Subsystem Enable

3.3 SEQUENCER REGISTERS

Sequencer Index/Data Register 3C4 RW 3C5 RW							
n/a	n/a	n/a	n/a	n/a	Sequencer Index Bit 2	Sequencer Index Bit 1	Sequencer Index Bit 0
00 Reset Register RW							
n/a	n/a	n/a	n/a	n/a	n/a	Sequencer Reset	Sequencer Reset
01 Clocking Mode Register RW							
n/a	n/a	Screen Off	Dummy Shift by 4 (see note)	Dotclock Divide by 2	Dummy Shift Load (see note)	Dummy Bandwidth(see note)	8/9 Dot Select
02 Map Mask Register RW							
n/a	n/a	n/a	n/a	Plane 3 Write Enable	Plane 2 Write Enable	Plane 1 Write Enable	Plane 0 Write Enable
03 Character Map Select Register RW							
n/a	n/a	Map A Select Bit 2	Map B Select Bit 2	Map A Select Bit 1	Map A Select Bit 0	Map B Select Bit 1	Map B Select Bit 0
04 Memory Mode Register RW							
n/a	n/a	n/a	n/a	Chain 4	Odd/Even Map Select	RO Status Read 1	n/a

Notes: index 01 Clocking Mode Register bits 4, 2, 1 - are read/write bits that have no effect in hardware. These bits are provided for compatibility with some software that expects to read or write these bits.

index 00 bits 1, 0 Sequencer Reset bits - setting either or both of these bits to 1 will stop (i.e. reset) the Sequencer. Because stopping the Sequencer halts all interface signals to the LCD panel, logic exists to shut down the panel power (/LCDPWR goes high) before the Sequencer is actually shut down. During this delay between reset request (ie setting the reset bits) and actual Sequencer halting, any in-progress memory accesses will be completed. Also, during the actual period that the Sequencer is held in a reset state, if a memory access request is issued by the system, it will be held pending the restart of the Sequencer (while the memory cycle is held pending, the RDY output is held low).

index 01 bit 0 - 8/9 Dot Select Bit, this bit only has an effect for CRT modes. If LCD mode is selected (Aux[0B] bits 1:0 = 0,1), then this bit is a read/write only bit with no effect in hardware.

3.4 GRAPHICS CONTROLLER REGISTERS

Graphics Controller Index/Data Register 3CE RW 3CF RW							
n/a	n/a	n/a	n/a	Graphics Controller Index Bit 3	Graphics Controller Index Bit 2	Graphics Controller Index Bit 1	Graphics Controller Index Bit 0
00 Set/Reset Register RW							
n/a	n/a	n/a	n/a	Set/Reset Plane 3	Set/Reset Plane 2	Set/Reset Plane 1	Set/Reset Plane 0
01 Enable Set/Reset Register RW							
n/a	n/a	n/a	n/a	Enable Set/Reset Plane 3	Enable Set/Reset Plane 2	Enable Set/Reset Plane 1	Enable Set/Reset Plane 0
02 Color Compare Register RW							
n/a	n/a	n/a	n/a	Reference Color Bit 3	Reference Color Bit 2	Reference Color Bit 1	Reference Color Bit 0
03 Data Rotate Register RW							
n/a	n/a	n/a	Logic Function Select Bit 1	Logic Function Select Bit 0	Data Rotate Count Bit 2	Data Rotate Count Bit 1	Data Rotate Count Bit 0
04 Read Map Select Register RW							
n/a	n/a	n/a	n/a	n/a	n/a	Read Plane Select Bit 1	Read Plane Select Bit 0
05 Mode Register RW							
RO Status Read 0	Mode 13H Select	Shift Register Interleave	Odd/Even Plane Select	Read Mode Select	RO Status Read 0	Write Mode Select Bit 1	Write Mode Select Bit 0
06 Miscellaneous Register RW							
n/a	n/a	n/a	n/a	Display Memory Map Bit 1	Display Memory Map Bit 0	Odd Even Chain Select	Graphics Mode
07 Color Don't Care Register RW							
n/a	n/a	n/a	n/a	Compare Plane Select Bit 3	Compare Plane Select Bit 2	Compare Plane Select Bit 1	Compare Plane Select Bit 0
08 Bit Mask Register RW							
Graphics Data Write Mask Bit 7	Graphics Data Write Mask Bit 6	Graphics Data Write Mask Bit 5	Graphics Data Write Mask Bit 4	Graphics Data Write Mask Bit 3	Graphics Data Write Mask Bit 2	Graphics Data Write Mask Bit 1	Graphics Data Write Mask Bit 0

3.5 ATTRIBUTES CONTROLLER REGISTERS

Attributes Controller Index/Data Register 3C0 RW 3C0W 3C1R							
n/a	n/a	EGA Palette Enable	Attributes Controller Index Bit 4	Attributes Controller Index Bit 3	Attributes Controller Index Bit 2	Attributes Controller Index Bit 1	Attributes Controller Index Bit 0
00 - 0F EGA Palette Registers RW							
n/a	n/a	Secondary Red	Secondary Green	Secondary Blue	Primary Red	Primary Green	Primary Blue
10 Mode Control Register RW							
EGA Palette Bits 4, 5 Control	Dummy Pel Width (see note)	Pixel Pan Compat	n/a	Blink/ Intensity	Line Graphics 8>9 Dot	Mono Mode Select	Graphics Mode Select
11 Overscan Color Register RW							
Overscan Color Bit 7	Overscan Color Bit 6	Overscan Color Bit 5	Overscan Color Bit 4	Overscan Color Bit 3	Overscan Color Bit 2	Overscan Color Bit 1	Overscan Color Bit 0
12 Color Plane Enable Register RW							
n/a	n/a	RO status Read 0	RO status Read 0	Enable Plane 3	Enable Plane 2	Enable Plane 1	Enable Plane 0
13 Horizontal Panning Register RW							
n/a	n/a	n/a	n/a	Horizontal Pan Count Bit 3	Horizontal Pan Count Bit 2	Horizontal Pan Count Bit 1	Horizontal Pan Count Bit 0
14 Color Select Register RW							
n/a	n/a	n/a	n/a	Color Select Bit 3	Color Select Bit 2	Color Select Bit 1	Color Select Bit 0

Note: index 10 Mode Control Register bit 6 - the Dummy Pel Width bit is a read/write bit that has no effect in hardware. This bit is provided for compatibility with some software that expects to use the value stored in this VGA-defined register bit to determine if mode 13H is set.

index 10 Mode Control Register bit 2 - the Line Graphics 8->9 Dot bit only has an effect for CRT modes. If LCD mode is selected (Aux[0B] bits 1:0 = 0,1), then this bit is a read/write only bit with no effect in hardware.

index 13 Horizontal Panning Register bit 3 - the Horizontal Pan Count bit 3 only has an effect for CRT modes. If LCD mode is selected (Aux[0B] bits 1:0 = 0,1), then this bit is a read/write only bit with no effect in hardware.

3.6 CRT CONTROLLER REGISTERS

CRT Controller Index/Data Register 3B4/D4 RW 3B5/D5 RW							
n/a	n/a	CRT Controller Index Bit 5	CRT Controller Index Bit 4	CRT Controller Index Bit 3	CRT Controller Index Bit 2	CRT Controller Index Bit 1	CRT Controller Index Bit 0
00 Horizontal Total Register RW							
Horizontal Total Bit 7	Horizontal Total Bit 6	Horizontal Total Bit 5	Horizontal Total Bit 4	Horizontal Total Bit 3	Horizontal Total Bit 2	Horizontal Total Bit 1	Horizontal Total Bit 0
01 Horizontal Display Enable End Register RW (if Aux[00] bit 0 = 0)							
Horizonal DE End Bit 7	Horizonal DE End Bit 6	Horizonal DE End Bit 5	Horizonal DE End Bit 4	Horizonal DE End Bit 3	Horizonal DE End Bit 2	Horizonal DE End Bit 1	Horizonal DE End Bit 0
02 Horizontal Blanking Start Register RW							
Horizonal Blanking Start Bit 7	Horizonal Blanking Start Bit 6	Horizonal Blanking Start Bit 5	Horizonal Blanking Start Bit 4	Horizonal Blanking Start Bit 3	Horizonal Blanking Start Bit 2	Horizonal Blanking Start Bit 1	Horizonal Blanking Start Bit 0
03 Horizontal Blanking End Register RW (see note below)							
Dummy R/W Bit (see note)	Dummy R/W Bit (see note)	Dummy R/W Bit (see note)	Horizontal Blanking End Bit 4	Horizontal Blanking End Bit 3	Horizontal Blanking End Bit 2	Horizontal Blanking End Bit 1	Horizontal Blanking End Bit 0
04 Horizontal Retrace Start Register RW							
HRTC Start Bit 7	HRTC Start Bit 6	HRTC Start Bit 5	HRTC Start Bit 4	HRTC Start Bit 3	HRTC Start Bit 2	HRTC Start Bit 1	HRTC Start Bit 0
05 Horizontal Retrace End Register RW							
HRTC End Bit 7	HRTC End Bit 6	HRTC End Bit 5	HRTC End Bit 4	HRTC End Bit 3	HRTC End Bit 2	HRTC End Bit 1	HRTC End Bit 0
06 Vertical Total End Register RW							
VTotal End Bit 7	VTotal End Bit 6	VTotal End Bit 5	VTotal End Bit 4	VTotal End Bit 3	VTotal End Bit 2	VTotal End Bit 1	VTotal End Bit 0
07 CRTC Overflow Register RW							
VRTC Start Bit 9	VDisplay End Pos'n Bit9	VTotal End Bit 9	Line Compare Bit 8	VBlank Start Bit 8	VRTC Start Bit 8	VDisplay End Pos'n Bit 8	VTotal End Bit 8
08 Preset Row Scan Register RW							
n/a	Byte Pan Bit 1	Byte Pan Bit 0	Preset Row Scan Bit 4	Preset Row Scan Bit 3	Preset Row Scan Bit 2	Preset Row Scan Bit 1	Preset Row Scan Bit 0
09 Maximum Scan Line Register RW							

Line Doubling Enable	Line Compare Bit 9	VBlank Start Bit 9	Max Scan Line Bit 4	Max Scan Line Bit 3	Max Scan Line Bit 2	Max Scan Line Bit 1	Max Scan Line Bit 0

0A Cursor Start Register RW							
n/a	n/a	Cursor Disable	Cursor Start Row Bit 4	Cursor Start Row Bit 3	Cursor Start Row Bit 2	Cursor Start Row Bit 1	Cursor Start Row Bit 0
0B Cursor End Register RW							
n/a	Dummy R/W Bit (see note)	Dummy R/W Bit (see note)	Cursor End Row Bit 4	Cursor End Row Bit 3	Cursor End Row Bit 2	Cursor End Row Bit 1	Cursor End Row Bit 0
0C Start Address High Register RW							
Start Addr High Bit 15	Start Addr High Bit 14	Start Addr High Bit 13	Start Addr High Bit 12	Start Addr High Bit 11	Start Addr High Bit 10	Start Addr High Bit 9	Start Addr High Bit 8
0D Start Address Low Register RW							
Start Addr Low Bit 7	Start Addr Low Bit 6	Start Addr Low Bit 5	Start Addr Low Bit 4	Start Addr Low Bit 3	Start Addr Low Bit 2	Start Addr Low Bit 1	Start Addr Low Bit 0
0E Cursor Position High Register RW							
Cursor Position High Bit 15	Cursor Position High Bit 14	Cursor Position High Bit 13	Cursor Position High Bit 12	Cursor Position High Bit 11	Cursor Position High Bit 10	Cursor Position High Bit 9	Cursor Position High Bit 8
0F Cursor Position Low Register RW							
Cursor Position Low Bit 7	Cursor Position Low Bit 6	Cursor Position Low Bit 5	Cursor Position Low Bit 4	Cursor Position Low Bit 3	Cursor Position Low Bit 2	Cursor Position Low Bit 1	Cursor Position Low Bit 0
10 Vertical Retrace Start Register RW							
VRTC Start Bit 7	VRTC Start Bit 6	VRTC Start Bit 5	VRTC Start Bit 4	VRTC Start Bit 3	VRTC Start Bit 2	VRTC Start Bit 1	VRTC Start Bit 0
11 Vertical Retrace End Register RW							
Protect CRTC Registers 0-7	Dummy R/W Bit (see note)	Vertical Int Disable	Vertical Int Clear	VRTC End Bit 3	VRTC End Bit 2	VRTC End Bit 1	VRTC End Bit 0
12 Vertical Display Enable End Register RW (if Aux[00] bit 0 = 0)							
VDisplay End Pos'n Bit 7	VDisplay End Pos'n Bit 6	VDisplay End Pos'n Bit 5	VDisplay End Pos'n Bit 4	VDisplay End Pos'n Bit 3	VDisplay End Pos'n Bit 2	VDisplay End Pos'n Bit 1	VDisplay End Pos'n Bit 0
13 Offset Register RW							
Offset Bit 7	Offset Bit 6	Offset Bit 5	Offset Bit 4	Offset Bit 3	Offset Bit 2	Offset Bit 1	Offset Bit 0
14 Underline Location Register RW							

n/a	Double Word Select	Dummy R/W/ Bit (see note)	Underline Row Scan Bit 4	Underline Row Scan Bit 3	Underline Row Scan Bit 2	Underline Row Scan Bit 1	Underline Row Scan Bit 0

15 Vertical Blanking Start Register RW							
VBlank Start Bit 7	VBlank Start Bit 6	VBlank Start Bit 5	VBlank Start Bit 4	VBlank Start Bit 3	VBlank Start Bit 2	VBlank Start Bit 1	VBlank Start Bit 0
16 Vertical Blanking End Register RW							
VBlank End Bit 7	VBlank End Bit 6	VBlank End Bit 5	VBlank End Bit 4	VBlank End Bit 3	VBlank End Bit 2	VBlank End Bit 1	VBlank End Bit 0
17 Mode Control Register RW							
RO Status Read 1	Word/Byte Mode Select	MA0 Select MA13/15	n/a	n/a	n/a	MA14 Select MA14/rsc	Compat Mode Select
18 Line Compare Register RW							
Line Compare Bit 7	Line Compare Bit 6	Line Compare Bit 5	Line Compare Bit 4	Line Compare Bit 3	Line Compare Bit 2	Line Compare Bit 1	Line Compare Bit 0
24 Attribute Controller Addr/Data FF Register RO							
Attribute Ctl Index/Data	n/a	n/a	n/a	n/a	n/a	n/a	n/a

Note: registers and bits marked as “Dummy” or “Dummy R/W Bit” are read/write bits that have no effect in hardware. These registers and bits are provided for compatibility with some software that expects to use the values stored in these bits.

index 11 bit 7 Protect CRTC Registers 0-7 - when set to 1, this bit protects the following registers and bits from being written: index 00, 01, 02, 03, 04, 05, 06 - all bits, and index 07 bits 7,6,5,3,2,1,0.

in LCD only mode (Aux[0B] bits 1,0 = 0,1), the following CRTC registers are ignored and are treated as Dummy R/W bits:

index 00, 02, 03, 04, 05, 06, 10, 15, 16 - all bits
index 07 - bits 7, 6, 5, 3, 2, 0
index 09 - bits 6, 5
index 11 - bits 3, 2, 1, 0

3.7 LCD "B SET" PANEL SIZE REGISTERS

01 Horizontal Panel Size Register RW (if Aux[00] bit 0 = 1)							
Horizontal Panel Size Bit 7	Horizontal Panel Size Bit 6	Horizontal Panel Size Bit 5	Horizontal Panel Size Bit 4	Horizontal Panel Size Bit 3	Horizontal Panel Size Bit 2	Horizontal Panel Size Bit 1	Horizontal Panel Size Bit 0

Horizontal Panel Size Register

This value in this register specifies the horizontal size of the LCD panel in the number of 8-dot characters. For example, a 640 dot panel is programmed with the value 640÷8 = 50H. This register is ignored if Aux[02] bit 1 = 1, i.e. if CRT mode is enabled.

12 Vertical Panel Size Register RW (if Aux[00] bit 0 = 1)							
Vertical Panel Size Bit 8	Vertical Panel Size Bit 7	Vertical Panel Size Bit 6	Vertical Panel Size Bit 5	Vertical Panel Size Bit 4	Vertical Panel Size Bit 3	Vertical Panel Size Bit 2	Vertical Panel Size Bit 1

Vertical Panel Size Register

For dual-panel mode, this register contains the 8 most significant bits of the 9-bit number of lines in half the panel. For single-panel mode, this register contains the 8 most significant bits of the 9-bit number of lines in the panel. The least significant bit is always 0. For example, for a 480 line dual panel, this register is programmed with the 8 msb's of the 9-bit binary representation of 480÷2=240, i.e. 78H. For a 640 line single panel, this register is programmed with the 8 msb's of the 9-bit binary representation of 480 = F0H.

Note: These LCD B Registers are accessed in CRTC register space by setting Aux[00] bit 0 LCD B Registers Program Enable to 1. Also, if CRT mode is enabled, i.e. CRT Enable, Aux[0B] bit 1 = 1, then these registers are ignored.

3.8 SPRITE / HW CURSOR REGISTERS

CRT Controller Index/Data Register 3B4/D4 RW 3B5/D5 RW							
n/a	n/a	CRT Controller Index Bit 5	CRT Controller Index Bit 4	CRT Controller Index Bit 3	CRT Controller Index Bit 2	CRT Controller Index Bit 1	CRT Controller Index Bit 0

Note: the Sprite / Hardware Cursor registers are accessed via the CRTC index/data registers (3B4/3D4 and 3B5/3D5), at index 30H - 3FH.

30 Sprite/HW Cursor X Position High Register RW							
n/a	n/a	n/a	n/a	n/a	n/a	Sprite/HW Cursor X Pos'n Bit 9	Sprite/HW Cursor X Pos'n Bit 8

Sprite/HW Cursor X Position High

This register contains the most significant two bits of the current horizontal left-most displayed pixel position of the sprite or hardware cursor.

31 Sprite/HW Cursor X Position Low Register RW							
Sprite/HW Cursor X Pos'n Bit 7	Sprite/HW Cursor X Pos'n Bit 6	Sprite/HW Cursor X Pos'n Bit 5	Sprite/HW Cursor X Pos'n Bit 4	Sprite/HW Cursor X Pos'n Bit 3	Sprite/HW Cursor X Pos'n Bit 2	Sprite/HW Cursor X Pos'n Bit 1	Sprite/HW Cursor X Pos'n Bit 0

Sprite/HW Cursor X Position Low

This register contains the least significant eight bits of the current horizontal left-most displayed pixel position of the sprite or hardware cursor.

32 Sprite/HW Cursor Y Position High Register RW							
n/a	n/a	n/a	n/a	n/a	n/a	n/a	Sprite/HW Cursor Y Pos'n Bit 8

Sprite/HW Cursor Y Position High

This register contains the most significant bit of the current horizontal upper-most displayed pixel position of the sprite or hardware cursor.

33 Sprite/HW Cursor Y Position Low Register RW							
Sprite/HW Cursor Y Pos'n Bit 7	Sprite/HW Cursor Y Pos'n Bit 6	Sprite/HW Cursor Y Pos'n Bit 5	Sprite/HW Cursor Y Pos'n Bit 4	Sprite/HW Cursor Y Pos'n Bit 3	Sprite/HW Cursor Y Pos'n Bit 2	Sprite/HW Cursor Y Pos'n Bit 1	Sprite/HW Cursor Y Pos'n Bit 0

Sprite/HW Cursor Y Position Low

This register contains the least significant eight bits of the current horizontal upper-most displayed pixel position of the sprite or hardware cursor.

34 X Display Start Column Register RW							
n/a	n/a	X Disp Start Col Bit 5	X Disp Start Col Bit 4	X Disp Start Col Bit 3	X Disp Start Col Bit 2	X Disp Start Col Bit 1	X Disp Start Col Bit 0

X Display Start Column

This register specifies the first displayed column of the sprite or cursor. When this register is set to 0, there is no clipping of the left side of the sprite or cursor image.

35 Y Display Start Row Register RW							
n/a	n/a	Y Disp Start Row Bit 5	Y Disp Start Row Bit 4	Y Disp Start Row Bit 3	Y Disp Start Row Bit 2	Y Disp Start Row Bit 1	Y Disp Start Row Bit 0

Y Display Start Row

This register specifies the first displayed row of the sprite or cursor. When this register is set to 0, there is no clipping of the top of the sprite or cursor image.

36 Sprite/HW Cursor Address High Register RW							
n/a	n/a	n/a	n/a	n/a	n/a	n/a	Sprite/HW Cursor Addr Bit 8

Sprite/HW Cursor Address High

This is the most significant bit of the address location of the top left hand point of the sprite or hardware cursor pattern stored in memory. (see below)

37 Sprite/HW Cursor Address Low Register RW							
Sprite/HW Cursor Addr Bit 7	Sprite/HW Cursor Addr Bit 6	Sprite/HW Cursor Addr Bit 5	Sprite/HW Cursor Addr Bit 4	Sprite/HW Cursor Addr Bit 3	Sprite/HW Cursor Addr Bit 2	Sprite/HW Cursor Addr Bit 1	Sprite/HW Cursor Addr Bit 0

Sprite/HW Cursor Address Low

These are the least significant 8 bits of the address location of the top left hand point of the sprite or hardware cursor pattern stored in memory. The complete 18 bit memory address for the sprite/HW cursor is formed as follows:

MA[17:9]	Sprite/HW Cursor Address [8:0]
MA[8:3]	Row [5:0]
MA[2:0]	Column [2:0]

The row bits represent the current row of the sprite/HW cursor being fetched (0 - 63). The column bits represent the upper 3 bits of the horizontal position of the current pixels being fetched from memory, with each fetch retrieving 32 bits from memory: 8 pixels of the sprite, or 16 pixels of the HW cursor image.

38 Sprite/HW Cursor Function Register RW							
n/a	n/a	n/a	n/a	Vertical Doubling Enable	Horizontal Doubling Enable	HW Cursor /Sprite Select	Sprite Palette Scheme Sel

Vertical Doubling Enable

When this bit is set to 1, the displayed image of the sprite /HW cursor is doubled in the vertical dimension, providing the sprite/HW cursor function is enabled. When this bit is set to 0, the sprite/HW cursor is not doubled. If the sprite/HW cursor function is not enabled, then this bit has no effect. Note that the origin of the sprite/HW cursor is not affected by enabling vertical line doubling.

Horizontal Doubling Enable

When this bit is set to 1, the displayed image of the sprite /HW cursor is doubled in the horizontal dimension, providing the sprite/HW cursor function is enabled. When this bit is set to 0, the sprite/HW cursor is not doubled. If the sprite/HW cursor function is not enabled, then this bit has no effect. Note that the origin of the sprite/HW cursor is not affected by enabling horizontal line doubling.

HW Cursor / Sprite Select

Provided that the sprite/HW cursor function is enabled (Auxiliary Register 05 bit 5 = 1), when this bit is set to 0,the sprite function is selected, and when this bit is set to 1, the hardware cursor function is selected. If the sprite/HW cursor function is not enabled, then this bit has no effect.

Sprite Palette Scheme Select

This bit is used to select the palette scheme used for the sprite. The 2 bit sprite pixel color may represent either 1 of 4 colors, or 1 of 3 colors plus transparency. Provided that the sprite/HW cursor function is enabled (Auxiliary Register 05 bit 5 = 1), when this bit is set to 0,the sprite pixel bits select 1 of 4 sprite palette entries as the value of the currently displayed pixel. When this bit is set to 1, the sprite pixel values 1 to 3 select sprite palette entries 1 to 3 respectively, and sprite pixel value 0 selects transparency, setting the current pixel to the value of the displayed image behind the sprite pixel.

3C Sprite Palette Entry 0 / HW Cursor Background Register RW							
n/a	n/a	n/a	n/a	Sprite Color 0/BG Bit 3	Sprite Color 0/BG Bit 2	Sprite Color 0/BG Bit 1	Sprite Color 0/BG Bit 0

Sprite Palette Entry 0 / HW Cursor Background

These bits represent entry 0 of the 4x4 bit palette for the sprite, or the 4 bit background grey shade for the hardware cursor. Note that sprite and hardware cursor color values bypass the 256x6 Lookup Table and directly represent 1 of 16 gray shades.

3D Sprite Palette Entry 1 / HW Cursor Foreground Register RW							
n/a	n/a	n/a	n/a	Sprite Color 1/FG Bit 3	Sprite Color 1/FG Bit 2	Sprite Color 1/FG Bit 1	Sprite Color 1/FG Bit 0

Sprite Palette Entry 1 / HW Cursor Foreground

These bits represent entry 1 of the 4x4 bit palette for the sprite, or the 4 bit foreground grey shade for the hardware cursor. Note that sprite and hardware cursor color values bypass the 256x6 Lookup Table and directly represent 1 of 16 gray shades.

3E Sprite Palette Entry 2 Register RW							
n/a	n/a	n/a	n/a	Sprite Color 2 Bit 3	Sprite Color 2 Bit 2	Sprite Color 2 Bit 1	Sprite Color 2 Bit 0

Sprite Palette Entry 2

These bits represent entry 2 of the 4x4 bit palette for the sprite. Note that sprite color values bypass the 256x6 Lookup Table and directly represent 1 of 16 gray shades.

3F Sprite Palette Entry 3 Register RW							
n/a	n/a	n/a	n/a	Sprite Color 3 Bit 3	Sprite Color 3 Bit 2	Sprite Color 3 Bit 1	Sprite Color 3 Bit 0

Sprite Palette Entry 3

These bits represent entry 3 of the 4x4 bit palette for the sprite. Note that sprite color values bypass the 256x6 Lookup Table and directly represent 1 of 16 gray shades.

Sprite/HW Cursor Bit Definitions

The sprite and hardware cursor functions share common logic and cannot be displayed simultaneously. The following table defines the usage of the bits in off-screen memory representing the sprite or hardware cursor image:

Pixel bit 1	Pixel bit 0	CRTC[38] bits 1,0 = 00 Sprite Pixel Displayed	CRTC[38] bits 1,0 = 01 Sprite Pixel Displayed	CRTC[38] bits 1 = 1 Cursor Pixel Displayed
0	0	Sprite Palette Entry 0	Screen	Cursor Background
0	1	Sprite Palette Entry 1	Sprite Palette Entry 1	Cursor Foreground
1	0	Sprite Palette Entry 2	Sprite Palette Entry 2	Screen
1	1	Sprite Palette Entry 3	Sprite Palette Entry 3	NOT Screen

The pixel bits are packed in memory in the following configuration:

Plane/ Cursor Bit	Address X								Address X+1							
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
0/(Bit 0)	0	1	2	3	4	5	6	7	16	17	18	19	20	21	22	23
1/(Bit 1)	0	1	2	3	4	5	6	7	16	17	18	19	20	21	22	23
2/(Bit 0)	8	9	10	11	12	13	14	15	24	25	26	27	28	29	30	31
3/(Bit 1)	8	9	10	11	12	13	14	15	24	25	26	27	28	29	30	31

where:

X
X

= Displayed Pixel X

3.9 LCD GRAY SCALE LOOKUP TABLE REGISTERS

The LCD Gray Scale Lookup Table (LUT) Registers are provided for mapping pixels to gray scale values on the LCD display. For CRT modes, an external RAMDAC interface is provided. The LUT Registers share the same I/O address space as the external VGA RAMDAC, namely I/O addresses from 3C6H to 3C9H. If CRT mode is disabled (Aux[0B] bit 1 = 0), then reads and writes to I/O addresses 3C6H - 3C9H will access the internal LCD LUT Registers. If CRT mode is enabled (Aux[0B] bit 1 = 1), then writes to I/O addresses 3C6H - 3C9H will cause data to be written to both the internal LUT and the external RAMDAC. In this case, reads from this address range will result in accesses to either the internal LUT or the external RAMDAC depending on the setting of the External DAC Read Select bit in Aux[0B] bit 2. If this bit is set to 0, then reads will access the internal LUT registers. If this bit is 1, then reads will access the external RAMDAC registers. For CRT modes, this bit should be set to 1. Note however that the Ext. DAC RS2 Bit (Aux[0B] bit 3) must be set to 0 in order to allow accesses to the internal LUT registers, regardless of whether CRT or LCD mode is enabled. If Aux[0B] bit 3 is set to 1, then the internal LUT cannot be read or written.

Dummy LCD Lookup Table Pixel Mask Register 3C6 RW							
Dummy LUT Pixel Mask Bit 7	Dummy LUT Pixel Mask Bit 6	Dummy LUT Pixel Mask Bit 5	Dummy LUT Pixel Mask Bit 4	Dummy LUT Pixel Mask Bit 3	Dummy LUT Pixel Mask Bit 2	Dummy LUT Pixel Mask Bit 1	Dummy LUT Pixel Mask Bit 0

Dummy LCD Lookup Table Pixel Mask Register

This register contains 8 read/write bits that have no effect in hardware. These bits are provided for compatibility with some software that expects to use the value stored in this register while in LCD mode.

LCD Lookup Table Status Register 3C7 RO							
n/a	n/a	n/a	n/a	n/a	n/a	Read Write Mode Status Bit 1	Read Write Mode Status Bit 0

LCD Lookup Table Status Register

Directly after a write to the Lookup Table Read Address Register, the Read/Write Mode Status bits 1-0 are both set to 1. Directly after a write to the Lookup Table Write Address Register, both these bits are set to 0.

LCD Lookup Table Read Address Register 3C7 WO							
Lookup Table Read Addr Bit 7	Lookup Table Read Addr Bit 6	Lookup Table Read Addr Bit 5	Lookup Table Read Addr Bit 4	Lookup Table Read Addr Bit 3	Lookup Table Read Addr Bit 2	Lookup Table Read Addr Bit 1	Lookup Table Read Addr Bit 0

LCD Lookup Table Read Addr Bits 7-0

These 8 bits are used to select 1 of 256 gray scale lookup table registers to be read.

Once a valid read address is set in this register, the lookup table entry can be read by three successive reads (red, green, blue) of the Lookup Table Data Register 3C9H. After a successful read operation (i.e. three successive reads), the read address is automatically incremented.

Directly after writing an index value to this register, the Lookup Table Status Register Read/Write Mode Status bits 1-0 are both set to 1.

LCD Lookup Table Write Address Register 3C8 RW							
Lookup Table Wrt Addr Bit 7	Lookup Table Wrt Addr Bit 6	Lookup Table Wrt Addr Bit 5	Lookup Table Wrt Addr Bit 4	Lookup Table Wrt Addr Bit 3	Lookup Table Wrt Addr Bit 2	Lookup Table Wrt Addr Bit 1	Lookup Table Wrt Addr Bit 0

LCD Lookup Table Write Addr Bits 7-0

These 8 bits are used to select 1 of 256 gray scale lookup table registers to be written.

Once a valid write address is set in this register, the lookup table entry can be written by three successive writes (red, green, blue) to the Lookup Table Data Register 3C9H. After a successful write operation (i.e. three successive writes), the write address is automatically incremented.

Directly after writing an index value to this register, the Lookup Table Status Register Read/Write Mode Status bits 1-0 are both set to 0.

LCD Lookup Table Data Register 3C9 RW (see below)							
n/a	n/a	GS Lookup Table Data Bit 5	GS Lookup Table Data Bit 4	GS Lookup Table Data Bit 3	GS Lookup Table Data Bit 2	GS Lookup Table Data Bit 1	GS Lookup Table Data Bit 0

The use of the LCD Lookup Table Data Register varies depending on the setting of the Green-only/NTSC Weighting Select bit (Auxiliary Register index 01, bit 4). The chip allows 2 different gray scale weighting schemes, applied to data as it is written to the lookup table.

Aux [01] bit 4	**GS Weighting Function Selected**

0	GS Weighting Mode 0 (NTSC) GS = [19G + 9R + 4B] /32
1	GS Weighting Mode 1 (Green only) GS = $G_5G_4G_3G_2G_1G_0$

GS Weighting Modes 0 Writes

1st access (“Red”)							
n/a	n/a	Red Component Data Bit 5	Red Component Data Bit 4	Red Component Data Bit 3	Red Component Data Bit 2	Red Component Data Bit 1	Red Component Data Bit 0
2nd access (“Green”)							
n/a	n/a	Green Component Data Bit 5	Green Component Data Bit 4	Green Component Data Bit 3	Green Component Data Bit 2	Green Component Data Bit 1	Green Component Data Bit 0
3rd access (“Blue”)							
n/a	n/a	Blue Component Data Bit 5	Blue Component Data Bit 4	Blue Component Data Bit 3	Blue Component Data Bit 2	Blue Component Data Bit 1	Blue Component Data Bit 0

GS = [19G + 9R + 4B] /32

GS Weighting Mode 0 Reads

1st access (“Red”)							
n/a	n/a	Gray Scale Value Bit 5	Gray Scale Value Bit 4	Gray Scale Value Bit 3	Gray Scale Value Bit 2	Gray Scale Value Bit 1	Gray Scale Value Bit 0
2nd access (“Green”)							
n/a	n/a	Gray Scale Value Bit 5	Gray Scale Value Bit 4	Gray Scale Value Bit 3	Gray Scale Value Bit 2	Gray Scale Value Bit 1	Gray Scale Value Bit 0
3rd access (“Blue”)							
n/a	n/a	Gray Scale Value Bit 5	Gray Scale Value Bit 4	Gray Scale Value Bit 3	Gray Scale Value Bit 2	Gray Scale Value Bit 1	Gray Scale Value Bit 0

GS Weighting Mode 1 Writes

1st access (“Red”)							
n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
2nd access (“Green”)							
n/a	n/a	Green Component Data Bit 5	Green Component Data Bit 4	Green Component Data Bit 3	Green Component Data Bit 2	Green Component Data Bit 1	Green Component Data Bit 0
3rd access (“Blue”)							
n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a

GS Value = $G_5G_4G_3G_2G_1G_0$

GS Weighting Mode 1 Reads

1st access (“Red”)							
n/a	n/a	Green Component Data Bit 5	Green Component Data Bit 4	Green Component Data Bit 3	Green Component Data Bit 2	Green Component Data Bit 1	Green Component Data Bit 0
2nd access (“Green”)							
n/a	n/a	Green Component Data Bit 5	Green Component Data Bit 4	Green Component Data Bit 3	Green Component Data Bit 2	Green Component Data Bit 1	Green Component Data Bit 0
3rd access (“Blue”)							
n/a	n/a	Green Component Data Bit 5	Green Component Data Bit 4	Green Component Data Bit 3	Green Component Data Bit 2	Green Component Data Bit 1	Green Component Data Bit 0

SPC8108F$_{0B}$ LCD VGA Controller

Proprietary Register Implementation

Drawing Office No.

Revised: 4/8/93

2.0 PROPRIETARY REGISTER IMPLEMENTATION

This section describes deviations of the SPC8108 from the VGA standard. Section 9.2.1 (Background) gives a general description of the ways in which SPC8108 differs from the VGA standard. Section 9.2.2 (General Discussion) describes each difference in greater detail. Section 9.2.3 (Details) gives a detailed list of the changes to the VGA register set. For a list of all registers actually supported by SPC8108, see section 9.3 I/O Register Summary.

2.1 BACKGROUND

There are two ways in which the SPC8108 differs from the VGA standard.

Firstly, the CRTC timing registers differ since the SPC8108 is optimized to support 640x480 single/dual panel LCD's, with some flexibility to support other size panels. In LCD mode, the panel timing is determined by two special registers (horizontal and vertical panel size), so the CRTC registers of the VGA standard which would normally be used to vary the display monitor timings are ignored in LCD mode.

Secondly, there are some functions provided in the VGA register set that are never used in common VGA applications - the register bits for these functions have been removed from the register set supported in SPC8108 in order to optimize the design for VGA operation on a 16 gray-scale 640x480 dot LCD panel. In their place are read/writeable registers bits that have no effect.

2.2 GENERAL DISCUSSION

CRTC Timing Registers

In the SPC8108, the non-timing related CRTC registers are the same as in the VGA standard. However, in LCD modes the SPC8108 does not use any of the timing registers that provide full monitor timing programmability since much of the timing circuitry has been optimized in hardware to support 640x480 panels.

For LCD mode, the SPC8108 timing circuitry is programmed by a Horizontal Panel Size register and a Vertical Panel Size register - all other LCD timing parameters are fixed in hardware, so the functions of all the regular timing registers is ignored in LCD mode. The functions of registers 00H, 02H to 06H,10H, 15H, 16H , and certain bits in registers 07H, 09H and 11H are ignored in LCD mode - in their place dummy read/write registers are provided. Note that CRTC registers 01H and 12H (Horizontal/Vertical Display Enable End, respectively) have full functionality in both LCD and CRT modes.

For CRT mode, full CRTC register support is provided, with some minor exceptions (see next item).

Shift-Load, Shift-4, Count-by-2, Count-by-4 modes not supported

Shift-Load and Count-by-2 are normally used only in modes 0FH and 10H when run on 64kbyte VGA cards. Since the SPC8108 is exclusively a 256kbyte device, this option is not useful. The Shift-4 and Count-by-4 functions are not used in any standard VGA mode or by standard software. These bits have been removed from the register set.

Support for Maximum 640 Dot LCD Panel Only

The 720 dot text modes (0+,1+,2+,3+) must be reduced to 640 dot modes due to the fixed panel size. To simplify the design, the logic to select a 9-dot character clock has been removed for LCD display modes. The associated register bit in the Sequencer functions as normal in CRT modes, but for LCD modes this bit has no effect and only 8 dot modes are displayed on the LCD.

HRTC/2 mode has been omitted. In standard VGA, this mode was provided to support vertical resolutions greater than 1024.

6 bit Gray Scale Lookup Table for LCD Display

For LCD modes, the VGA palette has been replaced by an internal 256x6 bit Gray Scale Lookup Table. This lookup table operates in a similar manner as the VGA palette it replaces, with its registers at the same I/O addresses.

For mode 13H, the LCD controller will display a maximum of 64 shades of grey on a LCD rather than the 256 of 256k colors on a CRT monitor. These 64 shades of gray are achieved by using 16 gray-level frame-rate modulation plus dithering. For modes other than mode 13H, the controller will display up to 16 shades of gray using frame-rate modulation.

Because of the smaller number of grey shades displayable on the LCD, a method of mapping colors originally intended for display on a 16/256 color CRT monitor onto a 16/64 gray LCD panel is required. Hardware is provided to map the RGB (18 bit) values that are written to the lookup table by software expecting to program a regular VGA palette. These RGB values are mapped using 1 of 3 selectable schemes into 6 bit gray scale values that are stored in the lookup table.

For CRT display, the external RAMDAC supports the full 256 of 256k colors. If CRT mode is enabled, writes to the RAMDAC registers will also go to the internal LUT registers. An Auxiliary Register bit allows reading from either the external RAMDAC or internal LUT registers in this case.

2.3 DETAILS

This section gives a list of register bits in the SPC8108 that are different to the VGA standard. Only differences are listed here; any bits not mentioned are the same as VGA. For a complete list of the actual SPC8108 registers please see Section 9.3.

Misc. Output Reg. (3C2 W, 3CC R)

bit 1 Enable DRAM
Read / write only. No other effect in hardware.

Input Status Reg.0 (3C2 R)

bit 4 Switch Sense bit
Deleted.

Input Status Reg.1 (3DA R)

bits 1,2 Light Pen
Read Only as 0,1.
bits 4,5 Diagnostic
Deleted.

Feature Control Reg. (3DA W, 3CA R)

Register not supported.

Sequencer Registers (3C4,3C5)

Clocking Mode Reg. (Index 01h)

bit 0 8/9 Dot Select
For LCD-only modes (Aux[0B] bits 1,0 = 01) - Read / write only. No other effect in hardware.
For CRT modes, this bit selects 8 or 9 dot mode.
bit 1 CPU Bandwidth
Read / write only. No other effect in hardware.
bit 2 Shift-Load
Read / write only. No other effect in hardware.
bit 4 Shift-4
Read / write only. No other effect in hardware.

Memory Mode Mode Reg. (Index 04h)

bit 1 Ext. Mem.
Read only as 1. Always 256kbytes of memory.

CRTC Registers (3D4, 3D5)

Horizontal Total (Index 00h)

For LCD-only modes (Aux[0B] bits 1,0 = 01) - Read / write only. No other effect in hardware.
For CRT modes, normal VGA functionality.

Horizontal Display Enable (Index 01h)

For LCD-only modes (Aux[0B] bits 1,0 = 01), if Aux[00] bit 0 = 1, then index 01 accesses the LCD Horizontal Panel Size Register. Otherwise, normal VGA functionality.
For CRT modes, normal VGA functionality.

Horizontal Blanking Start (Index 02h)

For LCD-only modes (Aux[0B] bits 1,0 = 01) - Read / write only. No other effect in hardware.
For CRT modes, normal VGA functionality.

Horizontal Blank End (Index 03h)

bits 0-4 For LCD-only modes (Aux[0B] bits 1,0 = 01) - Read / write only. No other effect in hardware.
For CRT modes, normal VGA functionality.

bits 5, 6, 7
Read / write only. No other effect in hardware.

Horizontal Retrace Start (Index 04h)

For LCD-only modes (Aux[0B] bits 1,0 = 01) - Read / write only. No other effect in hardware.
For CRT modes, normal VGA functionality.

Horizontal Retrace End (Index 05h)

For LCD-only modes (Aux[0B] bits 1,0 = 01) - Read / write only. No other effect in hardware.
For CRT modes, normal VGA functionality.

Vertical Total End (Index 06h)

For LCD-only modes (Aux[0B] bits 1,0 = 01) - Read / write only. No other effect in hardware.
For CRT modes, normal VGA functionality.

CRTC Overflow (Index 07h)

bits 0,2,3,5,6,7
For LCD-only modes (Aux[0B] bits 1,0 = 01) - Read / write only. No other effect in hardware.
For CRT modes, normal VGA functionality.

Maximum Scan Line (Index 09h)

bits 6,7 For LCD-only modes (Aux[0B] bits 1,0 = 01) - Read / write only. No other effect in hardware.
For CRT modes, normal VGA functionality.

Cursor Start (Index 0Ah)

bit 7 IBM Test Bit
Deleted.

Cursor End (Index 0Bh)

bits 5,6 Cursor Skew
Read / write only. No other effect in hardware.

Vertical Retrace Start (Index 10h)

For LCD-only modes (Aux[0B] bits 1,0 = 01) - Read / write only. No other effect in hardware.
For CRT modes, normal VGA functionality.

VRTC End (Index 11h)

bit 6 3/5 Refresh
Read / write only. No other effect in hardware.

Vertical Display Enable End (Index 12h)

For LCD-only modes (Aux[0B] bits 1,0 = 01), if Aux[00] bit 0 = 1, then index 12 accesses the LCD Vertical Panel Size Register. Otherwise, normal VGA functionality.
For CRT modes, normal VGA functionality.

Underline Location(Index 14h)

bit 5 Count-by-4
Read / write only. No other effect in hardware.

Vertical Blanking Start (Index 15h)

For LCD-only modes (Aux[0B] bits 1,0 = 01) - Read / write only. No other effect in hardware.
For CRT modes, normal VGA functionality.

Vertical Blanking End (Index 16h)

For LCD-only modes (Aux[0B] bits 1,0 = 01) - Read / write only. No other effect in hardware.
For CRT modes, normal VGA functionality.

Mode Control (Index 17h)

bit 2 HRTC/2 Select
Read / write only. No other effect in hardware.
bit 3 Count-by-2
Read / write only. No other effect in hardware.
bit 7 Enable Retraces
Read only as 1. Retraces always enabled.

Attribute Controller Registers (3C0,3C1)

Mode Control Register (Index 10h)

bit 6 Pel Width
Read / write only. No other effect in hardware.
bit 2 Line Graphics 8>9 Dot
For LCD-only modes (Aux[0B] bits 1,0 = 01) - Read / write only. No other effect in hardware.
For CRT modes, this bit enables 8-9 dot copy for line graphics characters in text mode.

Color Plane Enable (Index 12h)

bits 4,5 Video Status MUX. Read only 0,0. IBM diagnostic use only.

Horizontal Panning Register (Index 13h)

bit 3 Horizontal Panning Bit 3
For LCD-only modes (Aux[0B] bits 1,0 = 01) - Read / write only. No other effect in hardware.
For CRT modes, this bit is bit 3 of the horizontal panning value for 9 dot modes.