SPC8107F$_{OE}$

LOW VOLTAGE VGA LCD CONTROLLER

■ DESCRIPTION

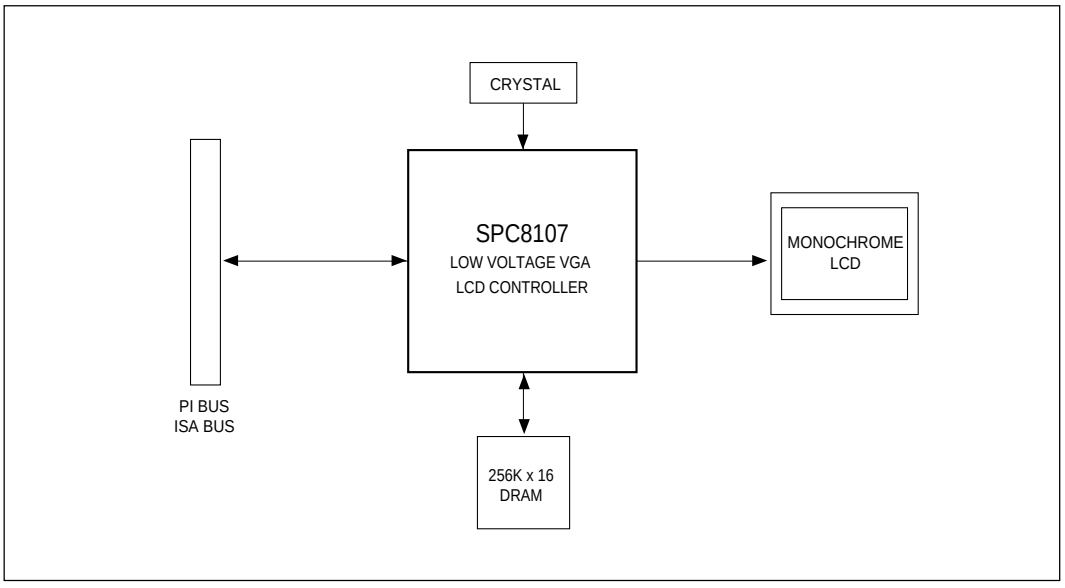
The SPC8107F$_{0E}$ is a single-chip, low-voltage LCD controller based on the VGA architecture and dedicated to driving a liquid crystal display. The fully VGA-compatible controller core, high-performance CPU interface and flexible 64 x 4-bit gray-scale lookup table are integrated into a very small footprint 100-pin QFP package.

The target markets for this device are low-cost and low-power sub-notebook and handheld products where low component count and a high performance 80 x 86 microprocessor interface are the major design considerations.

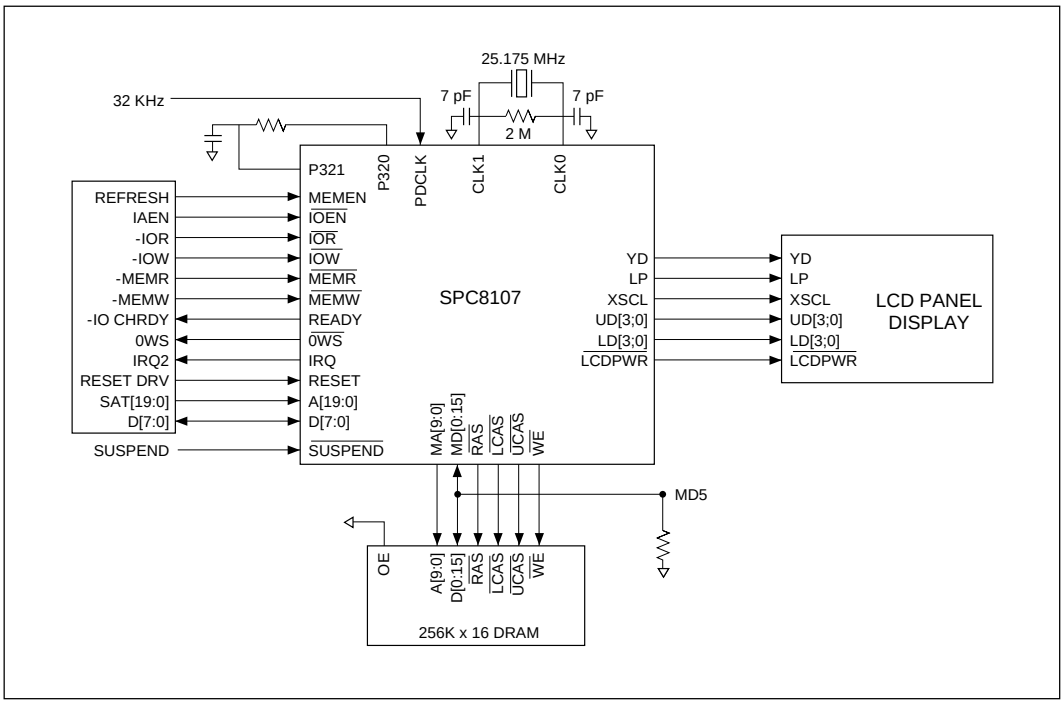
■ FEATURES

- Low-power CMOS technology
- Hardware VGA compatible
- High performance ISA & PI bus support
- One 256K x 16 self-refresh DRAM
- Four-stage display pipeline
- Video BIOS, software driver and utility support
- Single two-terminal crystal support
- Five power-down modes
- Package: QFP15-100 pin
- 3.3 volt core
- Monochrome LCD panel interface, for sizes 320 x 200 to 640 x 480
- On-chip 64 x 4 gray-scale look-up table
- 16 gray shades by frame rate modulation
- Three programmable gray-scale weightings (RGB), base (25, 50, 25), NTSC (30, 59, 11), and text (0, 100, 0)

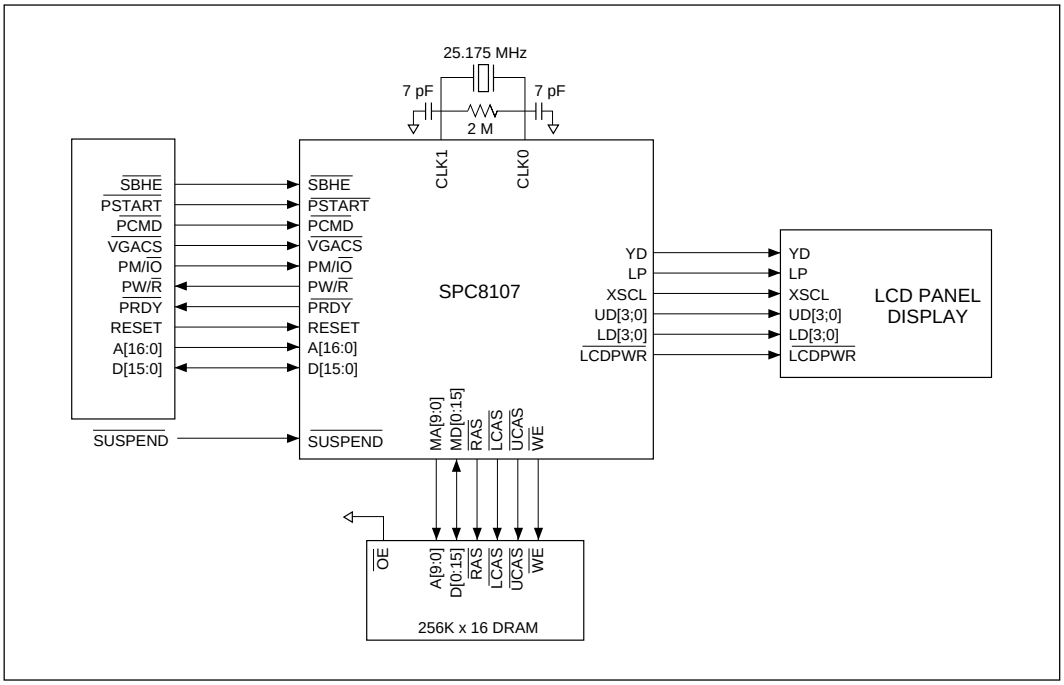
■ BLOCK DIAGRAM



■ ISA BUS SYSTEM BLOCK DIAGRAM



■ PI-BUS SYSTEM BLOCK DIAGRAM



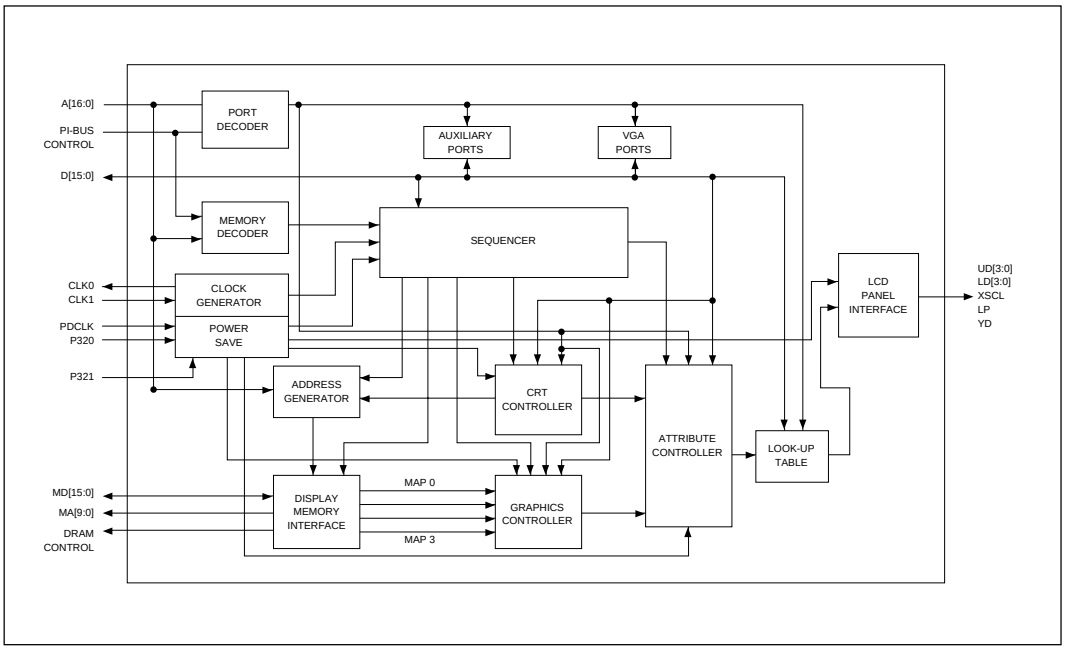
■ SPC8107 VIDEO MODES

Mode Number (Hex)	Horizontal Pixels Addressable	Vertical Pixels Addressable	Horizontal Pixels Displayed	Vertical Pixels Displayed	Monochrome LCD Display (Gray Shades)
0	320	200	320	200	16
0+	320	350	320	350	16
0++	360	400	320	400	16
1	320	200	320	200	16
1+	320	350	320	350	16
1++	360	400	320	400	16
2	640	200	640	200	16
2+	640	350	640	350	16
2++	720	400	640	400	16
3	640	200	640	200	16
3+	640	350	640	350	16
3++	720	400	640	400	16
4	320	200	320	200	4
5	320	200	320	200	4
6	640	200	640	200	2
7	720	350	640	350	2
7+	720	400	640	400	2
0D	320	200	320	200	16
0E	640	200	640	200	16
0F	640	350	640	350	2
10	640	350	640	350	16
11	640	480	640	480	2
12	640	480	640	480	16
13	320	200	640	400	16

■ SUPPORTED LCD PANELS

8-bit Interface				4-bit Interface	
Dual Panel		Single Panel		Single Panel	
Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical
640	400 480	640	400 480	320 480 640	200 240 320 400 480

■ FUNCTIONAL BLOCK DIAGRAM



■ FUNCTIONAL BLOCK DESCRIPTION

The Sequencer

The Sequencer generates internal signals to synchronize the operation of the chip as well as the signals to control the timing of the display DRAM. The Sequencer also arbitrates between CPU and video display accesses to the DRAM. It contains registers that allow selection of character font set, control the structure of the video memory and allow write masking of the individual planes of memory.

CRT Controller

The CRT Controller generates the horizontal and vertical synchronization signals for the single panel or dual panel LCD display and character and/or pixel addresses for display data from DRAM.

Address Generator

The Address Generator takes the display and refresh addresses from the CRT Controller and converts them into RAS and CAS addresses for the display DRAM and multiplexes these display accesses with CPU memory accesses.

Attributes Controller

The Attributes Controller takes in pixel and attribute information from the Graphics Controller and display DRAM and formats the data into pixel information which then passes through the lookup table. It also controls display character attributes such as blink, underline and horizontal pixel panning.

Graphics Controller

The Graphics Controller supplies display memory data to the Attributes Controller during display time and provides data translation between the CPU bus and the display memory during CPU read or write access cycles.

Memory Decoder

The Memory Decoder monitors the CPU-bus activity and decodes cycles for the display DRAM. It supplies memory access control signals to the Sequencer.

Port Decoder

The Port Decoder decodes CPU-bus I/O cycles to provide enable and write strobes for the on-chip I/O registers.

Auxiliary Ports

The Auxiliary Ports are I/O registers used to control functions of the chip beyond the basic VGA register set. Registers are included for controlling the LCD interface circuits as well as the power save modes.

VGA Ports

The VGA Ports contain the Miscellaneous Output Status register and the Video Subsystem Enable register used in VGA mode.

Clock Generation

The Clock Generation contains oscillator support for an external crystal.

Power Save

The Power Save block contains the logic to implement one hardware- and five software-controlled power save modes.

Lookup Table

The Lookup Table consists of a memory array of 64 locations of 4 bits each and hardware to convert VGA palette writes to gray-scale values.

LCD Interface

The LCD Interface block converts the display video data from the Lookup Table into LCD display data. It also generates control signals necessary to drive single or dual-panel LCD panels. The LCD interface block generates 16 levels of gray shades through frame rate modulation techniques.

■ DC SPECIFICATIONS

● Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DD}	Supply Voltage	V_{SS}–0.3 to +7.0	V
V_{IN}	Input Voltage	V_{SS}–0.3 to V_{DD}+0.3	V
V_{OUT}	Output Voltage	V_{SS} to V_{DD}	V
T_{OPR}	Operating Temperature	0 to +70	°C
T_{STG}	Storage Temperature	–65 to +150	°C
T_{SOL}	Soldering Temperature/Time	260 for 10 sec max at lead	°C

● Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Supply Voltage	V_{SS} = 0V	3.0	3.3	3.6	V
V_{IN}	Input Voltage		V_{SS}	—	V_{DD}	V
I_{OPR}	Average Power Consumption (estimated)		—	30	—	mA
$IP_{D1,2}$	Power Save Mode 1, 2		—	20, 5	—	mA
$IP_{D3, 4}$	Power Save Modes 3, 4 & SUSPEND		—	1	—	mA
IP_{D5}	Power Save Mode 5		—	25	—	mA

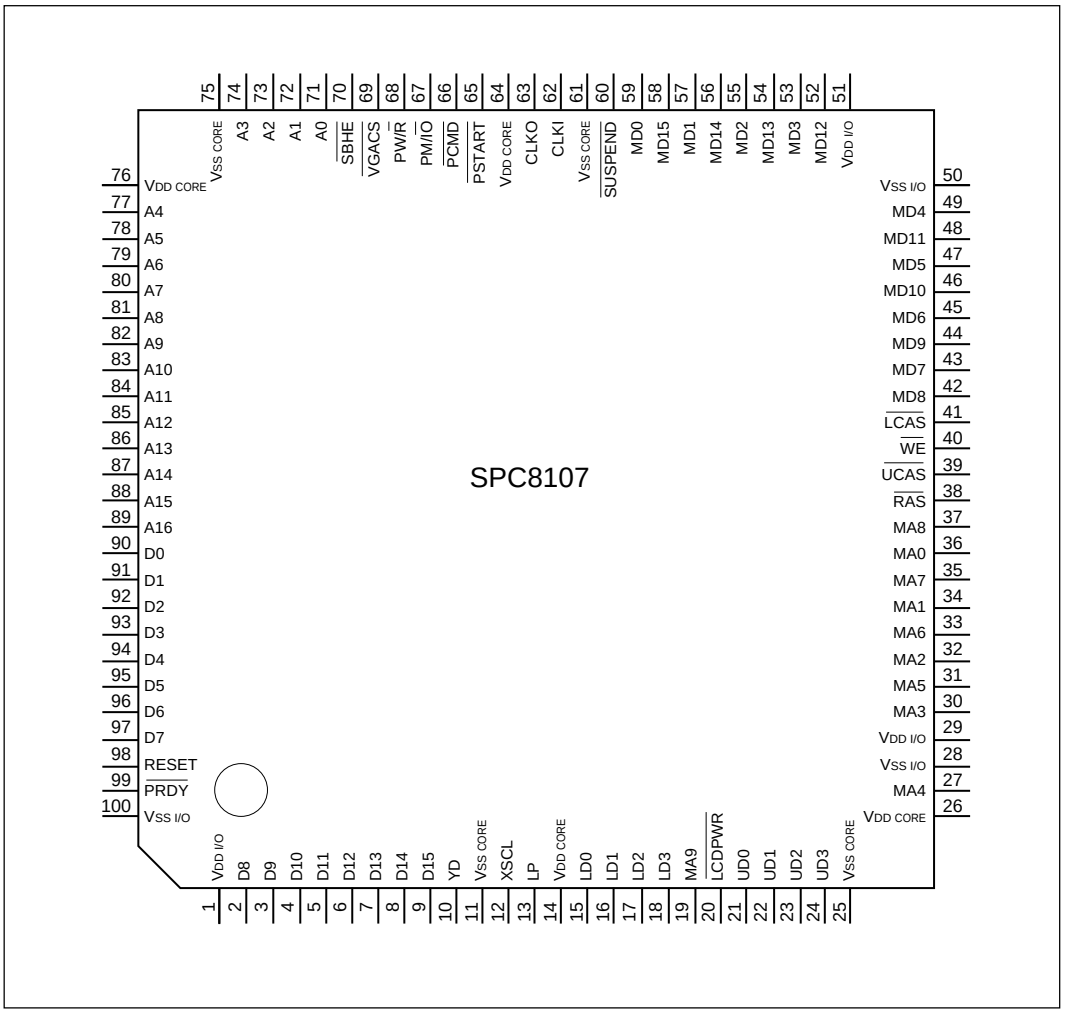
- **Input Specifications**

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Low-Level Input Voltage	V_{DD} = MIN	—	—	0.6	V
V_{IL}	Low-Level Input Voltage	V_{DD} = MIN	2.5	—	—	V
V_{T+}	Positive-going Threshold (CMOS Schmitt inputs)	V_{DD} =	—	—	—	V
V_{T-}	Negative-going Threshold (CMOS Schmitt inputs)	V_{DD} =	—	—	—	V
V_H	Hysteresis Voltage (CMOS Schmitt inputs)	V_{DD} =	—	—	—	V
I_{IZ}	Input Leakage Current	V_{DD} = MAX V_{IH} = V_{DD} V_{IL} = V_{SS}	–1	—	1	µA
C_{IN}	Input Pin Capacitance		—	8	—	pF
R_{PU}	Pull Up Resistance	V_{DD} = 3.3 V	90	—	360	kΩ

- **Output Specifications**

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{OL}	Low-Level Output Current	V_{DD} = 3.0V	3.0	—	—	mA
I_{OH}	High-Level Output Current	TS6, TSU6, CO2	–1.0	—	—	mA
I_{OL}	Low-Level Output Current	V_{DD} = 3.0V	6.0	—	—	mA
I_{OH}	High-Level Output Current	TS6, TSU6, CO3	–2.0	—	—	mA
I_{OL}	Low-Level Output Current	V_{DD} = 3.0V	12.0	—	—	mA
I_{OH}	High-Level Output Current	TS4	–4.0	—	—	mA
I_{OZ}	Output Leakage Current	V_{DD} = 3.6V V_{OH} = V_{DD} or V_{OL} = V_{SS}	–1	—	—	µA
C_{OUT}	Output Pin Capacitance		—	8	—	pF

■ SPC8107 PIN OUTS



Note: Pin names on this diagram correspond to the default configuration (PI Bus, 2 CAS, 1 WE DRAM).

■ PIN DESCRIPTION

Key

C = CMOS level input
CS = CMOS level input with hysteresis
COx = CMOS level output, x denotes cell type
TSx = Tri-state CMOS level driver, x denotes cell type
TSUx = Tri-state CMOS level driver with 100 kΩ pull up resistor, x denotes cell type

● CPU Interface - PI-Bus

Note: to configure chip for PI-Bus operation, MD[5] must be held at logic 1 during RESET (there is an internal pull up for the MD[5] pin, so no pullup resistor is required).

Pin Name	Type	Pin #	Drv	Description (when MD [5] = 1 during RESET)
A[0:16]	I	71..74, 77..89	C	CPU bus address inputs. In Suspend Mode, the Address inputs are internally masked off.
D[0:15]	I/O	90..97, 2..9	C /CO3	16 bit PI-Bus data bus. These lines are driven by the chip only during read cycles, and are in a hi-Z state at all other times. In Suspend Mode, these inputs are internally masked off.
/VGACS	I	69	C	PI-Bus VGA Chip Select. In Suspend Mode, the /VGACS input is disabled.
/PCMD	I	66	C	PI-Bus Command Strobe. In Suspend Mode the /PCMD input is disabled.
PM/IO	I	67	C	PI-Bus Memory or I/O Select. In Suspend Mode the PM/IO input is disabled.
PW/R	I	68	C	PI-Bus Write or Read Select. In Suspend Mode the PW/R input is disabled.
/SBHE	I	70	C	System Byte High Enable. In Suspend Mode the /SBHE input is disabled.
/PSTART	I	65	CS	PI-Bus Start Strobe. In Suspend Mode the /PSTART input is disabled.
/PRDY	O	99	TS3	PI-Bus Ready. This output is driven low to terminate a bus cycle.
RESET	I	98	CS	The active high Reset signal from the CPU clears all internal registers and forces all signals to their inactive state. During Suspend Mode the RESET input is ignored.

● Pin Mapping for ISA/PI Bus Interfaces

Pin No.	PI Bus Pin Name	ISA Bus Usage
71..74, 77..89	A[0:16]	A[0:16]
90..97	D[0:7]	D[0:7]
2..4	D[8:10]	A[17:19]
5	D[11]	IRQ
6	D[12]	/0WS
7..9	D[13:15]	PDCLK, P32O, P32I
65	/PSTART	/IOEN

Pin No.	PI Bus Pin Name	ISA Bus Usage
66	/PCMD	/IOR
67	PM/IO	/IOW
68	PW/R	/MEMR
69	/VGACS	MEMEN
70	/SBHE	/MEMW
99	/PRDY	READY

- **CPU Interface - ISA-Bus**

  Note: to configure chip for ISA Bus operation, MD[5] must be held at logic 0 during RESET with an external pull-down resistor.

Pin Name	Type	Pin #	Drv	Description (when MD [5] = 1 during RESET)
A[0:19]	I	71..74, 77..89, 2..4	C	CPU bus address inputs. In Suspend Mode, the Address inputs are internally masked off.
D[0:7]	I/O	90..97	C /CO3	8 bit ISA-Bus data bus. These lines are driven by the chip only during read cycles and are in a hi-Z state at all other times. In Suspend Mode, these inputs are internally masked off.
MEMEN	I	69	CS	ISA Bus Memory Enable. This signal should be connected to the /REFRESH signal on the ISA bus. When this signal is low (e.g. during a system memory refresh cycle), memory address decoding is disabled.
/IOR	I	66	C	ISA Bus I/O Read Strobe. In Suspend /IOR is disabled.
/IOW	I	67	C	ISA Bus I/O Write Strobe. In Suspend the /IOW is disabled.
/MEMR	I	68	C	ISA Bus Memory Read Strobe. In Suspend /MEMR is disabled.
/MEMW	I	70	C	ISA Bus Memory Write Strobe. In Suspend /MEMW is disabled.
/IOEN	I	65	CS	ISA Bus I/O Enable. This input should be connected to the ISA bus AEN signal. When this signal is high, I/O address decoding is disabled. In Suspend Mode, the /IOEN input is disabled.
READY	O	99	TS3	ISA Bus READY signal. This output is driven low to force the CPU to insert wait states during memory cycles. READY is released to high-Z after a transfer is complete.
RESET	I	98	CS	The active high Reset signal from the CPU clears all internal registers and forces all signals to their inactive state. During Suspend Mode the RESET input is ignored.
IRQ	O	5	TS3	ISA Bus Vertical Interrupt. When enabled, a Vertical Retrace Interrupt will cause this signal to be driven from a logic 0 state to a logic 1 (rising-edge triggered interrupt). Once set, this interrupt must be cleared by a bit in the CRTC registers. A control bit in the Auxiliary Registers allows this output to be optionally disabled (tri-stated).
/0WS	O	6	TS3	0 Wait State. This output is driven low when a valid I/O access is decoded. This will allow the CPU to complete the ISA bus I/O access with zero wait states. When inactive, this output will be tri-stated.

- **Video Memory Interface**

Pin Name	Type	Pin #	Drv	Description
MA[0:8]	O	36, 34, 32, 30, 27, 31, 33, 35, 37	CO3	Multiplexed row/column address bits for video display memory.
MA[9] (/RDACK, or WF)	O	19	CO3	Multiplexed row/column address bit 9 (MA[9]), or Read Acknowledge (/RDACK), or LCD Bias Signal WF, as determined by the logic value on MD[4] and MD[7] during RESET. When MD[7] is latched in as 0, this pin functions as the LCD Backplane Bias signal WF. When MD[7] is latched in as 1, then this pin's function is determined by MD[4] as follows: when MD[4] is latched in as 1, this pin is configured as address bit MA[9] which is only required for 256K x 16 DRAMs which are organized as 1024 x 256 x 16 (i.e. 10 row address bits, 8 column address bits). For other DRAMs, MA[9] is not required. When MD[4] is latched in as 0, this pin is configured as the /RDACK signal, which goes low during valid I/O or memory reads to the chip.
MD[0:15]	I/O	42-49, 52-59	C/ TSU3	Data bits for video display memory. The output drivers of these pins are placed into a high-impedance state when RESET is high, or when the Sequencer is in a reset state. On the falling edge of RESET, the values on MD[3:0] are latched into a read-only Auxiliary Register and are available to be read as configuration inputs. Other MD inputs are used to configure various hardware options. See Configuration Options below.
/RAS	O	38	CO6	DRAM Row Address Strobe.
/LCAS (/LWE)	O	41	CO6	DRAM Column Address Strobe for low byte (/LCAS) or Write Enable Strobe for low byte (/LWE), as determined by logic value on MD[6] during RESET (see pin mapping table).
/UCAS (/CAS)	O	39	CO6	DRAM Column Address Strobe for high byte (/UCAS) or single Column Address Strobe (/CAS) as determined by logic value on MD[6] during RESET.
/WE (/UWE)	O	40	CO6	DRAM Write Enable Strobe(/WE), or Write Enable Strobe for high byte (/UWE), as determined by logic value on MD[6] during RESET.

- **Miscellaneous**

Pin Name	Type	Pin #	Drv	Description
/SUSPEND	I	60	CS	A low level on this pin puts the chip into a hardware power save mode. The /SUSPEND signal overrides any software initiated power save modes, and disables the PI-Bus interface inputs. Address and Data inputs are also masked when this signal is low. When in Suspend Mode the UD(3:0), LD(3:0), XSCL, YD, LP and WF signals are driven into a high impedance state (optionally driven low) and the /LCDPWR signal is driven high.

- **Clock Inputs**

Pin Name	Type	Pin #	Drv	Description
CLKI	I	62	•	This pin, along with CLKO is the 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin is the clock input.
CLKO	O	63	•	This pin, along with CLKI is the 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin should be left unconnected.
PDCLK	I	7	C	Power Down Clock. This input may be used in ISA bus configuration (MD[5] = 0 at RESET) to provide a low frequency clock for generating refresh in Power Save Mode 4 and Suspend, as an optional alternative to using the pixel clock or MEMEN input as the refresh clock source.
P32O	O	8	CO2	P32 Clock Output. This pin is used to support a 50% duty cycle 32 KHz PDCLK input (pin 7). This P32O output is a buffered version of the PDCLK input used to drive an external RC circuit. For a 64 KHz PDCLK input, this output should be left unconnected.
P32I	I	9	C	P32I Clock Input. This pin is used to support a 50% duty cycle 32 KHz PDCLK input (pin 7). This P32I input should be connected to an external RC circuit which generates 100-200 ns delay from P32O. Internally this will be used to generate a 64 KHz refresh clock with the appropriate low period. For a 64 KHz PDCLK input, this pin must be tied high.

- **Power Supply**

Pin Name	Type	Pin #	Description
VDD CORE	P	14, 26, 64, 76	VDD supply for core logic.
VDD I/O	P	1, 51, 29	VDD supply for I/O pins.
VSS CORE	P	11, 25, 61, 75	VSS supply for core logic.
VSS I/O	P	50, 100, 28	VSS supply for I/O pins.

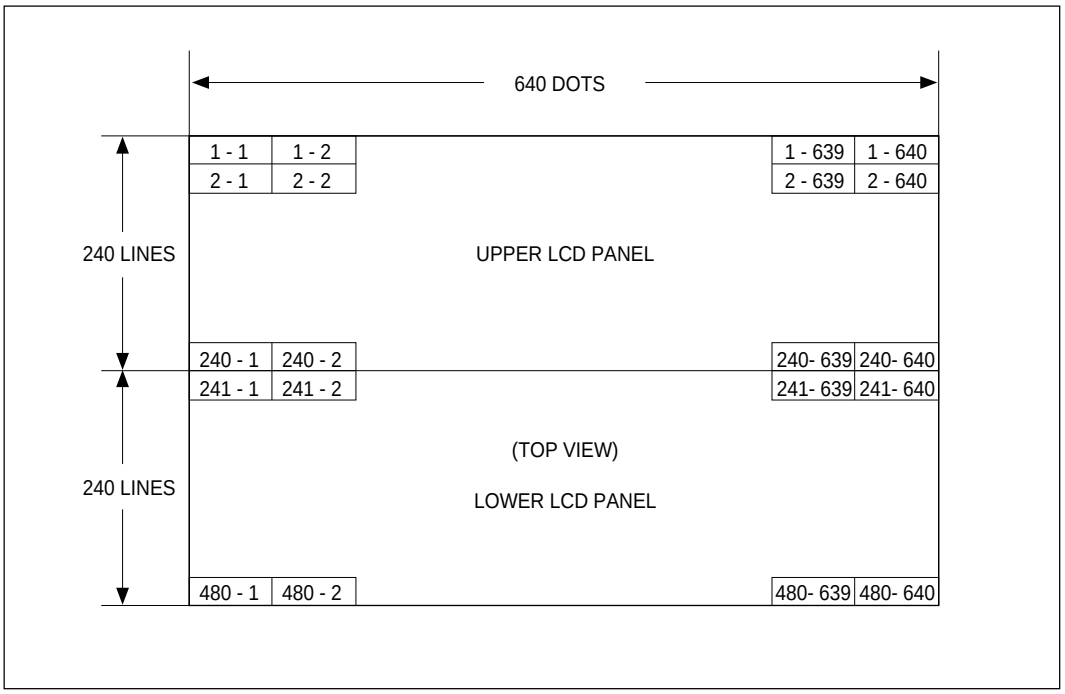
- **Configuration Options**

Pin Name	Values on this pin at falling edge of RESET is used to configure: (1/0)
MD[3:0]	Values stored in read-only Aux Reg [02] bits 7:4 for software use
MD[4]	Select the function of output pin 19 as MA[9] (1), or /RDACK (0) - see also MD[7]
MD[5]	PI-bus operation (1) /ISA bus operation (0)
MD[6]	2 CAS, 1 WE type DRAM (1) / 1 CAS, 2 WE type DRAM (0)
MD[7]	use MD[4] to configure pin 6 as MA9 or /RDACK (1) / pin 6 is WF output (0)
MD[8]	Reserved
MD[9]	Reserved

- **LCD Panel Interface**

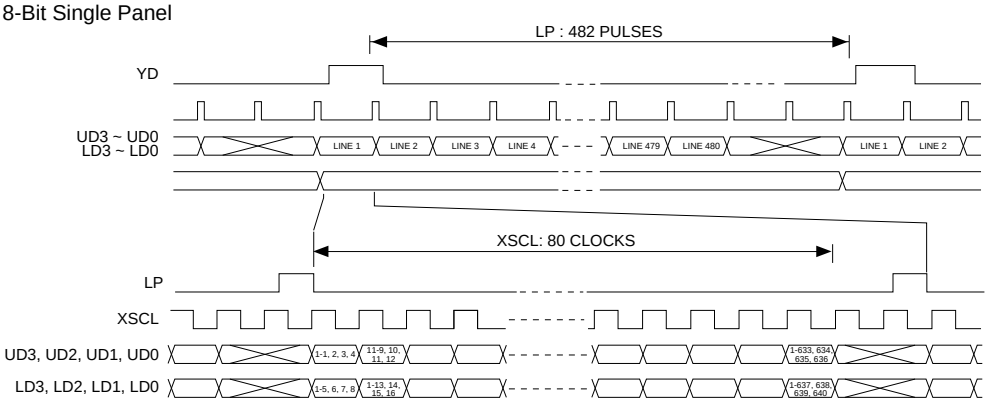
Pin Name	Type	Pin #	Drv	Description
YD	O	10	TS12	Vertical Scanning Start Pulse output. A logic 1 on this signal, sampled by the LCD module on the falling edge of LP, is used by the panel row drivers (Y drivers) to indicate the start of vertical frame.
LP	O	13	TS12	Latch Pulse output. The falling edge of this signal is used to latch a row of display data in the LCD module's column driver shift registers and to turn on the row driver (Y driver) for that line.
XSCL	O	12	TS12	Shift Clock for LCD data. Display data is clocked out of the chip on the rising edge of this signal to be shifted into the LCD panel module column drivers (X drivers) on each falling edge.
UD[0:3]	O	21..24	TS12	Upper panel display data for dual panel mode. For single panel mode these bits are the most significant 4 bits of the 8 bit output data to the panel (PD[4:7]). For 4-bit single panel mode, these bits are the 4 bits of output data to the panel.
LD[0:3]	O	15..18	TS12	Lower panel data for dual panel mode. For 8-bit single panel mode, these bits are the least significant 4 bits of the 8-bit output data to the panel (PD[0:3]). For 4-bit single panels, these bits are driven 0.
/LCDPWR	O	20	CO3	LCD power control. In normal operation this signal is driven low to enable an external LCD power supply. This signal is driven high when the chip is put into any power save mode, or if the Sequencer is in a reset state. It can be used externally to turn off the panel supply voltage and backlight. After a RESET, this signal is held high until the CRTC is programmed and running.
WF (MA[9] or /RDACK)	O	19	CO3	LCD Backplane Bias Signal. This pin is shared with the MA9 and /RDACK functions. To use this pin as WF, the value on MD[7] at RESET must be 0. The WF signal toggles once per vertical frame.

■ **LCD Panel Pixels**

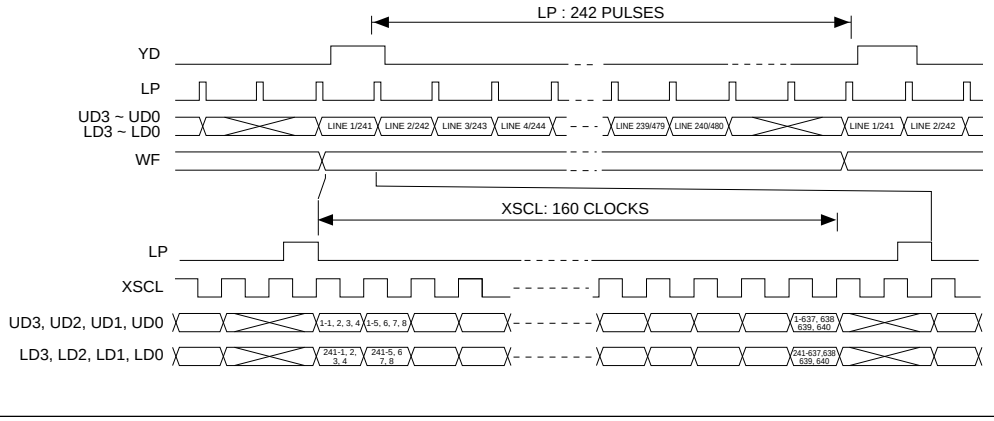


■ LCD Panel Interface

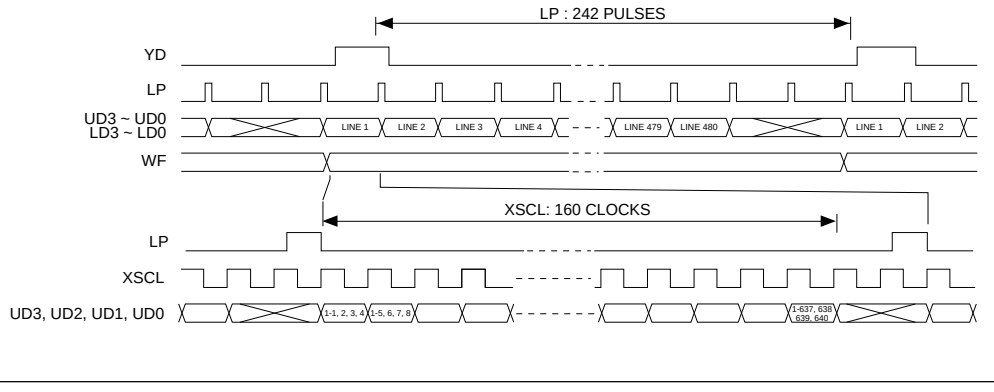
8-Bit Single Panel



8-Bit Dual Panel



4-Bit Single Panel



■ POWER SAVE MODES

One hardware-controlled and five software-controlled Power Save Modes are provided by the SPC8107.

Software Power Save Mode 1

- No video display accesses to display memory.
- Dedicated CPU accesses to display memory.
- Display memory refresh is maintained and is generated from CLKI input (nominally 25 MHz). Refresh rate can be selected: 64 kHz or 8 kHz, (for 256 cycle/4 msec, or 256 cycle/32 msec DRAM, respectively).
- I/O read/write of all registers is allowed.
- /LCDPWR signal forced high.

Options

- LCD output signals tri-stated or forced low.

Software Power Save Mode 2

Mode 2 has two states. Initially the chip enters State 1. If no display memory read or write is detected for about two horizontal lines (approx. 63.5 us), the chip enters State 2. If a display memory read or write is requested while in State 2, the chip returns to State 1 to service the display memory access within 3 - 7 Ts periods (CLKI input).

State 1

- Same as Power Save Mode 1

State 2

- No video display accesses to display memory.
- No CPU accesses to display memory.
- Sequencer is halted.
- Display memory refresh is maintained and is generated from CLKI input (nominally 25 MHz). Refresh rate can be selected: 64 kHz or 8 kHz, (for 256 cycle/4 msec, or 256 cycle/32 msec DRAM, respectively).
- I/O read/write of all registers is allowed.
- /LCDPWR signal forced high.

Options

- LCD output signals tri-stated or forced low.

Software Power Save Mode 3

- No video display accesses to display memory.
- No CPU accesses to display memory.
- Sequencer is halted.
- No display memory refresh.
- I/O read/write of all registers is allowed.
- /LCDPWR signal forced high.

Options

- I/O read/write to all registers except Auxiliary Registers can be disabled.
- Internal clock oscillator cell can be disabled if a 2-terminal crystal is used.
- LCD output signals tri-stated or forced low.

Software Power Save Mode 4

- No video display accesses to display memory.
- No CPU accesses to display memory.
- Sequencer is halted.
- Display memory refresh maintained.
- I/O read/write of all registers is allowed.
- /LCDPWR signal forced high.

Options

- Select MEMEN, PDCLK, or CLKI as refresh clock source (ISA only)
- I/O read/write to all registers except Auxiliary Registers can be disabled.
- Internal clock oscillator cell can be disabled, if a 2-terminal crystal is used.
- LCD output signals tri-stated or forced low.
- DRAM self-refresh mode can be used to maintain display memory contents.

Software Power Save Mode 5

- Video display remains active/visible.
- CPU accesses to display memory allowed.

Options

- Internal clock can be slowed by 20%.

Hardware Power Save Mode (Suspend Mode)

- No video display accesses to display memory.
- No CPU accesses to/from display memory.
- Sequencer is halted.
- Display memory refresh maintained.
- No I/O register or memory accesses allowed.
- /LCDPWR signal forced high.
- LCD output signals tri-stated or forced low.
- All CPU interface input signals are internally masked off. All CPU interface output signals are inactive.
- Internal clock oscillator cell will be disabled, if a 2-terminal crystal is used.

Options

- DRAM self-refresh mode can be used to maintain display memory contents.
- Select MEMEN, PDCLK, or CLKI as refresh clock source (ISA only).