S-MOS
SYSTEMS
A Seiko Epson Affiliate

SPC8106 LCD/CRT VGA CONTROLLER

Data Sheet

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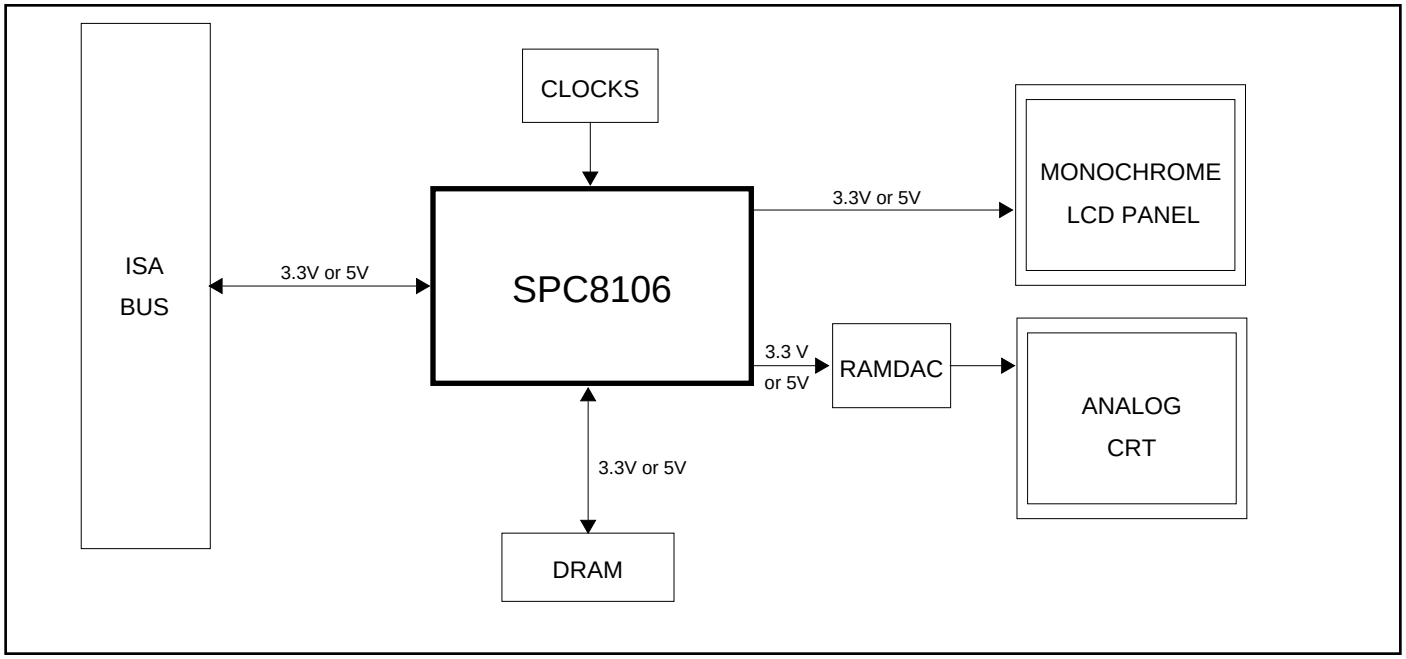
■ DESCRIPTION

The SPC8106 is a versatile mixed voltage VGA graphics controller capable of driving liquid crystal displays, TFT displays and analog CRT monitors. The controller integrates all LCD interface, sequencing and color modulation logic into one small form factor 144 pin package. With the addition of an industry standard ’477 compatible RAMDAC, the SPC8106 will also drive a VGA fixed frequency or multifrequency monitor.
The target products for this device are price and power sensitive 80x86 microprocessor based portable personal computer or other specialized LCD systems where 320 x 200 to 640 x 480 x 256 color LCD panel displays are the major design criteria.

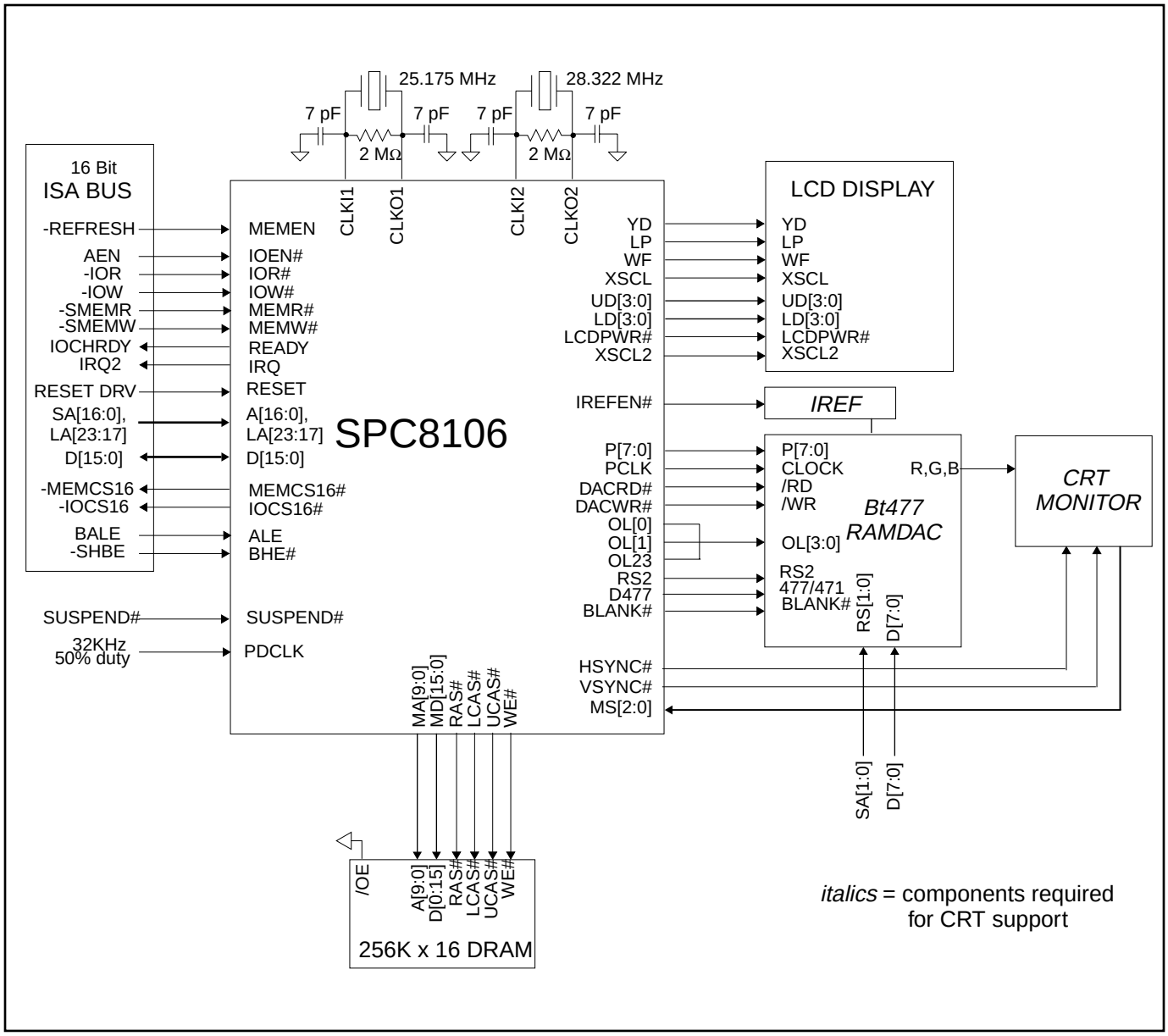
■ FEATURES

- Low-power CMOS technology
- Hardware VGA compatible
- 8- or 16-bit ISA support
- Supports one 256K x 16 80ns DRAM (self refresh optional)
- 64 x 64 x 2-bit pixel hardware cursor
- Two-terminal crystal or external oscillator support
- Hardware or software power-down
- Video BIOS, software driver and utility support
- 144-pin QFP package
- 9- or 12-bit color TFT panel interface for 640 x 480
- Single panel or dual panel interface for sizes 320 x 200 to 640 x 480
- On-chip 256 x 12-bit look-up table
- 16 gray shades or 4096 colors by FRM
- 64 gray shades by FRM and dithering
- Two programmable gray-scale weightings: NTSC and Green-Only
- Vertical centering and expansion for LCDs
- Full CRT support with ’477 compatible RAMDAC
- Pin Compatible with the SPC8108F0C
- Mixed voltage 3.3V/5V operation

■ SYSTEM BLOCK DIAGRAM



■ INTERFACE OPTIONS



Note: Example implementation, actual may vary.

■ SUPPORTED RESOLUTIONS

LCD Display Modes

Mode No.	Mode Type	Font	Characters	Resolution	Displayed Pixels	Gray Shades	Colors	Memory Segment
0	Text	8 x 8	40 x 25	320 x 200	640 x 400	16	16	B800
0+	Text	8 x 14	40 x 25	320 x 350	640 x 350	16	16	B800
0++	Text	8 x 16	40 x 25	320 x 400	640 x 400	16	16	B800
1	Text	8 x 8	40 x 25	320 x 200	640 x 400	16	16	B800
1+	Text	8 x 14	40 x 25	320 x 350	640 x 350	16	16	B800
1++	Text	8 x 16	40 x 25	320 x 400	640 x 400	16	16	B800
2	Text	8 x 8	80 x 25	640 x 200	640 x 400	16	16	B800
2+	Text	8 x 14	80 x 25	640 x 350	640 x 350	16	16	B800
2++	Text	8 x 16	80 x 25	640 x 400	640 x 400	16	16	B800
3	Text	8 x 8	80 x 25	640 x 200	640 x 400	16	16	B800
3+	Text	8 x 14	80 x 25	640 x 350	640 x 350	16	16	B800
3++	Text	8 x 16	80 x 25	640 x 400	640 x 400	16	16	B800
4	Graphics	N/A	N/A	320 x 200	640 x 400	4	4	B800
5	Graphics	N/A	N/A	320 x 200	640 x 400	4	4	B800
6	Graphics	N/A	N/A	640 x 200	640 x 400	2	2	B800
7	Text	8 x 14	80 x 25	640 x 350	640 x 350	2	2	B000
7+	Text	8 x 16	80 x 25	640 x 400	640 x 400	2	2	B000
0D	Graphics	N/A	N/A	320 x 200	640 x 400	16	16	A000
0E	Graphics	N/A	N/A	640 x 200	640 x 400	16	16	A000
0F	Graphics	N/A	N/A	640 x 350	640 x 350	2	2	A000
10	Graphics	N/A	N/A	640 x 350	640 x 350	16	16	A000
11	Graphics	N/A	N/A	640 x 480	640 x 480	2	2	A000
12	Graphics	N/A	N/A	640 x 480	640 x 480	16	16	A000
13	Graphics	N/A	N/A	320 x 200	640 x 400	64	256	A000
100	Graphics	N/A	N/A	640 x 400	640 x 400	64	256	A000
101	Graphics	N/A	N/A	640 x 480	640 x 480	64	256	A000
108	Text	8 x 8	80 x 60	640 x 480	640 x 480	16	16	B800

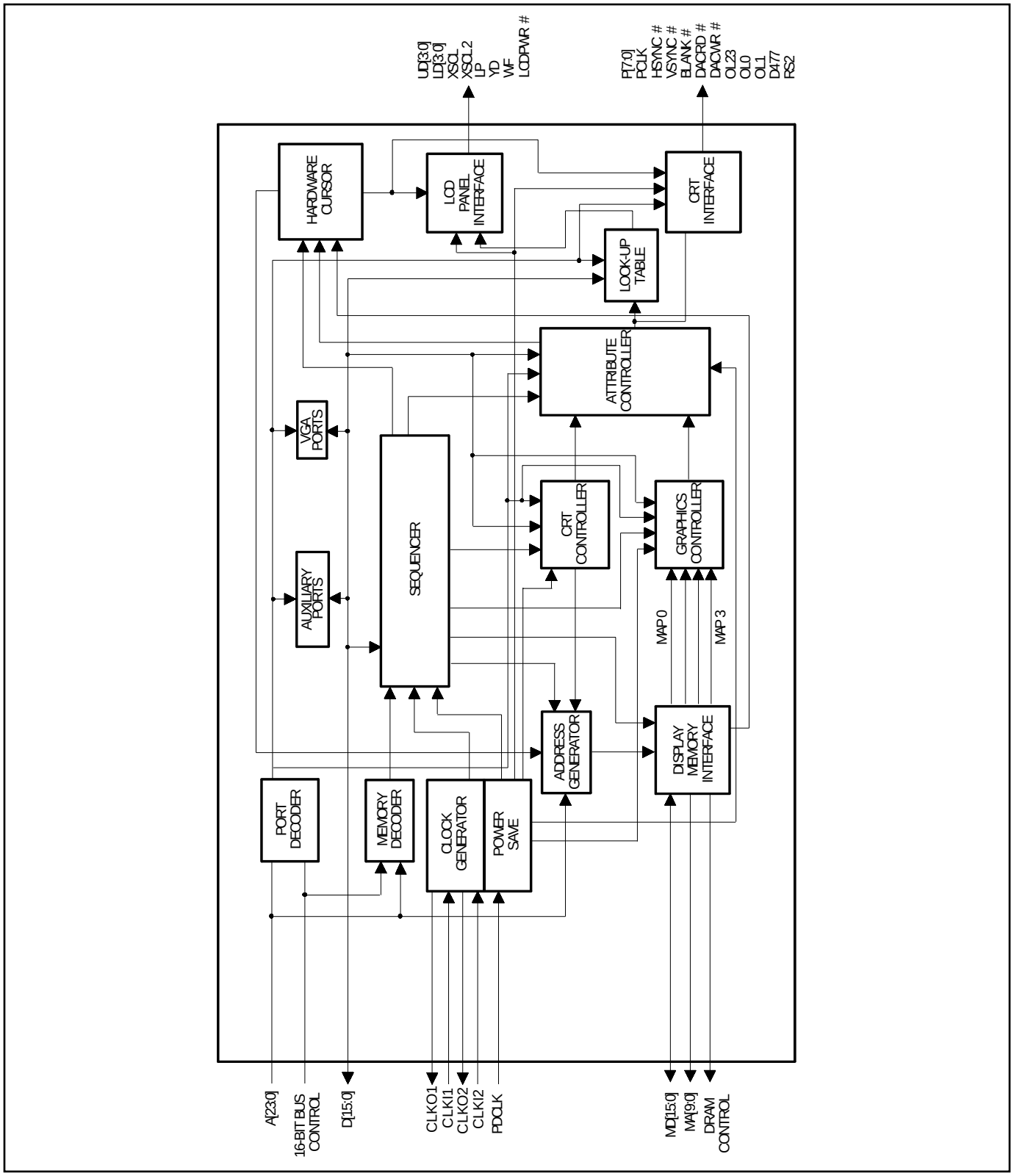
CRT Display Modes

Mode No.	Mode Type	Font	Characters	Resolution	Displayed Pixels	Colors	Memory Segment
0	Text	8 x 8	40 x 25	320 x 200	640x400	16	B800
0+	Text	8 x 14	40 x 25	320 x 350	640x350	16	B800
0++	Text	9 x 16	40 x 25	360 x 400	720x400	16	B800
1	Text	8 x 8	40 x 25	320 x 200	640x400	16	B800
1+	Text	8 x 14	40 x 25	320 x 350	640x350	16	B800
1++	Text	9 x 16	40 x 25	360 x 400	720x400	16	B800
2	Text	8 x 8	80 x 25	640 x 200	640x400	16	B800
2+	Text	8 x 14	80 x 25	640 x 350	640x350	16	B800
2++	Text	9 x 16	80 x 25	720 x 400	640x400	16	B800
3	Text	8 x 8	80 x 25	640 x 200	640x400	16	B800
3+	Text	8 x 14	80 x 25	640 x 350	640x350	16	B800
3++	Text	9 x 16	80 x 25	720 x 400	640x400	16	B800
4	Graphics	N/A	N/A	320 x 200	640x400	4	B800
5	Graphics	N/A	N/A	320 x 200	640x400	4	B800
6	Graphics	N/A	N/A	640 x 200	640x400	2	B800
7	Text	8 x 14	80 x 25	640 x 350	640x350	2	B000
7+	Text	9 x 16	80 x 25	720 x 400	720x400	2	B000
0D	Graphics	N/A	N/A	320 x 200	640x400	16	A000
0E	Graphics	N/A	N/A	640 x 200	640x400	16	A000
0F	Graphics	N/A	N/A	640 x 350	640x350	2	A000
10	Graphics	N/A	N/A	640 x 350	640x350	16	A000
11	Graphics	N/A	N/A	640 x 480	640x480	2	A000
12	Graphics	N/A	N/A	640 x 480	640x480	16	A000
13	Graphics	N/A	N/A	320 x 200	640x400	256	A000
100	Graphics	N/A	N/A	640 x 400	640x400	256	A000
101	Graphics	N/A	N/A	640 x 480	640 x 480	256	A000
108	Text	8 x 8	80 x 60	640 x 480	640 x 480	16	B800

■ SUPPORTED LCD INTERFACES

8-Bit Interface				4-Bit Interface	
Dual Panel		Single Panel		Single Panel	
Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical
640	400 480	640	1 to 480	320 480 640	200 240 320 400 480

■ BLOCK DIAGRAM



■ FUNCTIONAL BLOCK DESCRIPTION

The Sequencer

The Sequencer generates internal signals to synchronize the operation of the chip as well as the signals to control the timing of the display DRAM. The Sequencer also arbitrates between CPU and video display accesses to the DRAM. It contains registers that allows selection of character font set, control the structure of the video memory and allow write masking of the individual plane of memory.

CRT Controller

The CRT Controller generates the horizontal and vertical synchronization signals for the CRT, single panel or dual panel LCD display and character and/or pixel addresses for display data from DRAM.

CRT Interface

The CRT interface aligns CRT signals to the Pixel Clock and generates the I/O Control signals for CPU access to the RAMDAC.

Address Generator

The Address Generator takes the display and refresh addresses from the CRT Controller and converts them into RAS and CAS addresses for the display DRAM, and multiplexes these display accesses with CPU memory accesses.

Attributes Controller

The Attributes Controller takes in pixel and attribute information from the Graphics Controller and display DRAM and formats the data into pixel information which then passes through the lookup table. It also controls display character attributes such as blink, underline and horizontal pixel panning.

Graphics Controller

The Graphics Controller supplies display memory data to the Attributes Controller during display time and provides data translation between the CPU bus and the display memory during CPU read or write access cycles.

Display Memory Interface

The Display Memory Interface is a bridge by which the chip communicates with the DRAM. It contains buffers that are used to store recently fetched DRAM data.

Memory Decoder

The Memory Decoder monitors the CPU-bus activity and decodes cycles for the display DRAM. It supplies memory access control signals to the Sequencer.

Port Decoder

The Port Decoder decodes CPU-bus I/O cycles to provide enable and write strobes for the on-chip I/O registers.

Auxiliary Ports

The Auxiliary Ports are I/O registers used to control functions of the chip beyond the basic VGA register set. Registers are included for controlling the LCD interface circuits as well as the power save modes.

VGA Ports

The VGA Ports contain the Miscellaneous Output Status register and the Video Subsystem Enable register used in VGA mode.

Clock Generation

The Clock Generation contains oscillator support for external crystals.

Power Save

The Power Save block contains the logic to implement six software controlled and one hardware controlled power down modes.

Lookup Table

The Lookup Table consists of a memory array of 256 locations of 12 bits each and hardware to convert VGA palette writes to gray-scale values.

LCD Interface

The LCD Interface block converts the display video data from the Lookup Table into LCD display data. It also generates control signals necessary to drive single or dual-panel LCD panels. For monochrome LCD panels, the LCD interface block generates a maximum 64 gray shades through frame rate modulation and dithering techniques. For color LCD panels, the LCD interface block generates 256 simultaneous colors from a possible 4096 colors through frame rate modulation.

Hardware Cursor

The Hardware Cursor block generates a 4 gray shade or color cursor/sprite that can be overlaid on the LCD or CRT display. The cursor is 64 x 64 pixels or optionally expanded to 128 x 128 through pixel replication.

■ DC SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DD}	Supply Voltage	V_{SS}-0.3 to +7.0	V
V_{IN}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
V_{OUT}	Output Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
T_{OPR}	Operating Temperature	0 to +70	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{SOL}	Soldering Temperature/Time	260 for 10sec max at lead	°C

Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
HV_{DD}	Supply Voltage	V_{SS} = 0V	4.5	5.0	5.5	V
LV_{DD}	Supply Voltage	V_{SS} = 0V	3.0	3.3	3.6	V
V_{IN}	Input Voltage	V_{SS}	V_{SS}	--	V_{DD}	V
T_{OPR}	Operating Temperature		0	25	70	˚C
I_{OPR}	Average Current Consumption	Vcc Core = 3.3V V_{CC} I/O = 5.0V	typical I_{Core} = 52.31 typical I_{IO} = 13.85			mA

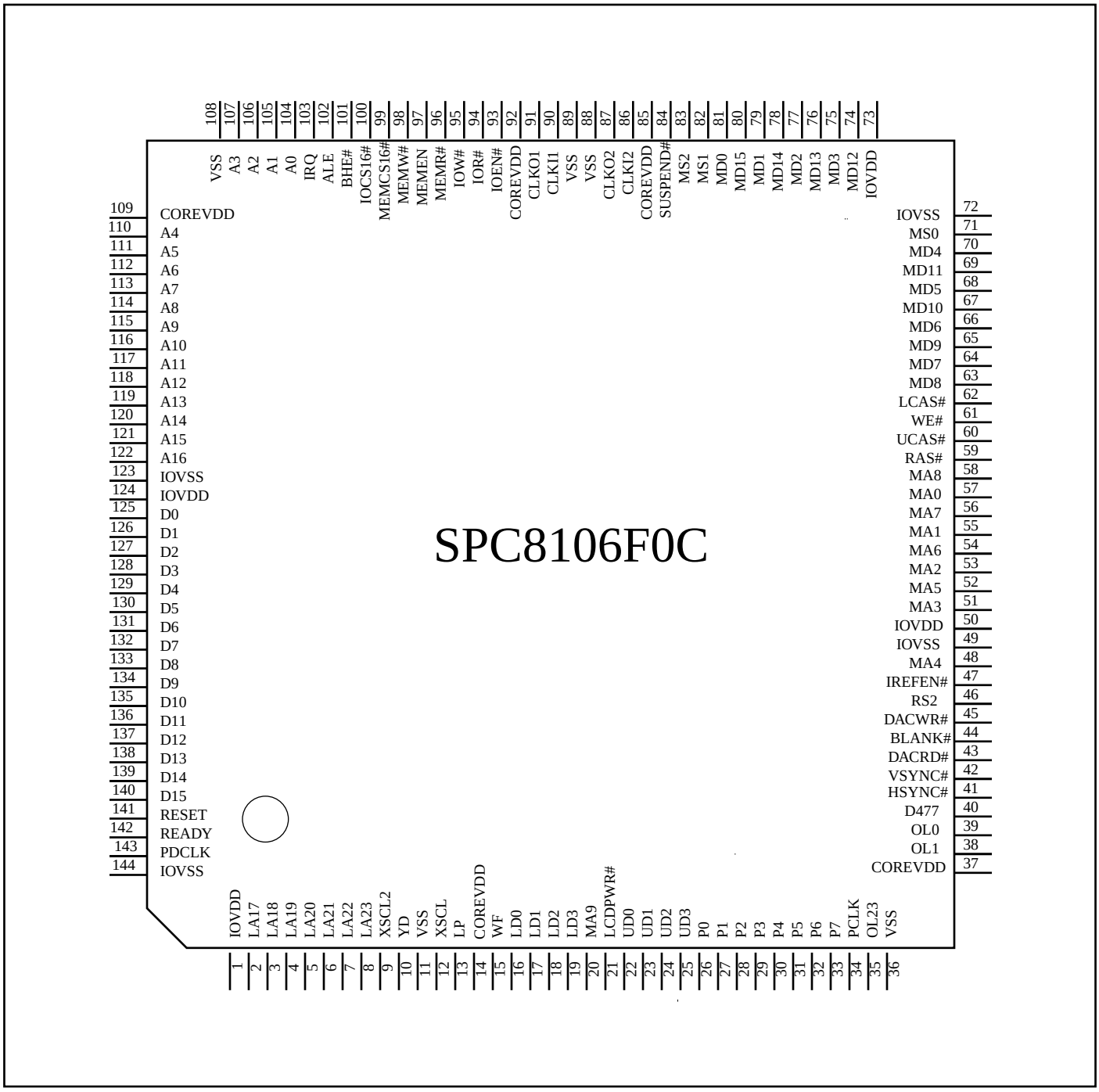
Input Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (CMOS inputs)	V_{DD} = MIN			1.0	V
V_{IH}	High Level Input Voltage (CMOS inputs)	V_{DD} = MAX	3.5			V
V_{IL}	Low Level Input Voltage (TTL inputs)	V_{DD} = MIN			0.8	V
V_{IH}	High Level Input Voltage (TTL inputs)	V_{DD} = MAX	2.0			V
V_{T+}	Positive-going Threshold (CMOS Schmitt inputs)	V_{DD} = 5.0			4.0	V
V_{T-}	Negative-going Threshold (CMOS Schmitt inputs)	V_{DD} = 5.0	0.8			V
V_H	Hysteresis Voltage (CMOS Schmitt inputs)	V_{DD} = 5.0	0.3			V
V_{T+}	Positive-going Threshold (TTL Schmitt inputs)	V_{DD} = 5.0			3.0	V
V_{T-}	Negative-going Threshold (TTL Schmitt inputs)	V_{DD} = 5.0	0.6			V
V_H	Hysteresis Voltage (TTL Schmitt inputs)	V_{DD} = 5.0	0.1			V
I_{IZ}	Input Leakage Current	V_{DD} = MAX V_{IH} = V_{DD} V_{IL} = V_{SS}	-1		1	µA
C_{IN}	Input Pin Capacitance			8		pF
R_{PU2}	Pull Up Resistance	V_{DD} = 5.0 V	50	100	200	kΩ
R_{PU3}	Pull Up Resistance	V_{DD} = 5.0 V	100	200	400	kΩ
R_{PD}	Pull Down Resistance	V_{DD} = 5.0 V	100	200	400	kΩ

Output Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{OL2}	Low Level Output Current	$V_{OL}=V_{SS}+0.4V$ TS2	6.0			mA
I_{OH2}	High Level Output Current	$V_{OH}=V_{DD}-0.4V$ TS2	-2.0			mA
I_{OL3}	Low Level Output Current	$V_{OL}=V_{SS}+0.4V$ TS3	12.0			mA
I_{OH3}	High Level Output Current	$V_{OH}=V_{DD}-0.4V$ TS3	-4.0			mA
I_{OL4}	Low Level Output Current	$V_{OL}=V_{SS}+0.4V$ TS4	24.0			mA
I_{OH4}	High Level Output Current	$V_{OH}=V_{DD}-0.4V$ TS4	-8.0			mA
I_{OZ}	Output Leakage Current	$V_{OH}=V_{DD}$ or $V_{OL}=V_{SS}$	-1		1	µA
C_{OUT}	Output Pin Capacitance			8		pF
C_{BID}	Bidirectional Pin Capacitance			10		pF

■ SPC8106F0C PIN OUTSOURCE: 8110_PINOUT_08.CAN



■ PIN DESCRIPTION

Key

A = Analog
I = Input
O = Output
I/O = Bidirectional
P = Power

CPU Interface

Pin Name	Type	Pin #	Description
A[0:16], LA[17:23]	I	104..107, 110..122, 2..4, 5..8	CPU bus address inputs. In Suspend Mode, the Address inputs are internally masked off. If the value on MD[5] at RESET = 1, then the ALE input pin is used to internally latch LA[19:17] and A[16:2], allowing these address bits to be driven by the processor address bus. If the value on MD[5] at RESET = 0, then standard ISA address timing is assumed, where pins A[0:16], LA[17:23] should be connected to the ISA bus signals SA[0:16], LA[17:23] respectively.
ALE	I	102	ISA Bus Address Latch Enable. In Suspend Mode the ALE input is disabled. If the value on MD[5] at RESET = 1, then the ALE input is used to internally latch LA[19:17] and A[16:2], allowing these address bits to be driven by the processor address bus. In this mode, the processor ADS# output should be connected to this pin. If the value on MD[5] at RESET = 0, then standard ISA address timing is assumed, and only the LA[19:17] inputs are internally latched.
D[0:15]	I/O	125..140	16 bit ISA-Bus data bus. These lines are driven by the chip only during read cycles, and are in a hi-Z state at all other times. In Suspend Mode, these inputs are internally masked off.
MEMEN	I	97	ISA Bus Memory Enable. This signal should be connected to the REFRESH# signal on the ISA bus. When this signal is low (e.g. during a system memory refresh cycle), memory address decoding is disabled.
IOR#	I	94	ISA Bus I/O Read Strobe. In Suspend Mode the IOR# input is disabled.
IOW#	I	95	ISA Bus I/O Write Strobe. In Suspend Mode the IOW# input is disabled.
MEMR#	I	96	ISA Bus System Memory Read Strobe. In Suspend Mode the MEMR# input is disabled.
MEMW#	I	98	ISA Bus System Memory Write Strobe. In Suspend Mode the MEMW# input is disabled.
IOEN#	I	93	ISA Bus I/O Enable. This input should be connected to the ISA bus AEN signal. When this signal is high, I/O address decoding is disabled. In Suspend Mode, the IOEN# input is disabled.
READY	O	142	ISA Bus READY signal. This output is driven low to force the CPU to insert wait states during memory cycles. READY is released to high-Z after a transfer is complete.
RESET	I	141	The active high Reset signal from the CPU clears all internal registers and forces all signals to their inactive state.
IRQ	O	103	ISA Bus Vertical Interrupt. When enabled, a Vertical Retrace Interrupt will cause this signal to be driven from a logic 0 state to a logic 1 (rising-edge triggered interrupt). Once set, this interrupt must be cleared by a bit in the CRTC registers. A control bit in the Auxiliary Registers allows this output to be optionally disabled (tri-stated). This pin also is used for the output of the NAND tree in pin test mode.
MEMCS16#	O	99	ISA Bus Memory Chip Select 16. Address inputs LA[23:17] are decoded to drive this output low when a valid memory address (AXXXXh, BXXXXH) appears on the bus.

Pin Name	Type	Pin #	Description
IOCS16#	O	100	ISA Bus I/O Chip Select 16. Address inputs A[15:0] and IOEN# are decoded to drive this output low when a valid SPC8106 I/O register address appears on the bus,. Note that I/O addresses 3C6h-3C9h do not result in IOCS16# being driven low (i.e. RAMDAC and internal LUT register reads and writes are 8 bit cycles).
BHE#	I	101	ISA Bus Byte High Enable. In Suspend Mode the BHE# input is disabled.

Video Memory Interface

Pin Name	Type	Pin #	Description
MA[0:9]	O	57, 55, 53, 51, 48, 52, 54, 56, 58, 20	Multiplexed row/column address bits for video display memory.
MD[0:15]	I/O	81, 79, 77, 75, 70, 68, 66, 64, 63, 65, 67, 69, 74, 76, 78, 80	Data bits for video display memory. The output drivers of these pins are placed into a high-impedance state when RESET is high, or when the Sequencer is in a reset state. On the falling edge of RESET, the values on MD[3:0] and MD[12:9] are latched into a read-only Auxiliary Register and are available to be read as configuration inputs. Also, the value on MD[8:4] and MD[15:13] are used to configure various hardware options. See “Summary of Configuration Options” on page 18 for details.
RAS#	O	59	DRAM Row Address Strobe for single 256Kx16 DRAM.
LCAS# (LWE#)	O	62	Multiple Function: DRAM Column Address Strobe for low byte (LCAS#). For alternate function see “Multiple Function Pin Descriptions” on page 19.
UCAS# (CAS#)	O	60	Multiple Function: DRAM Column Address Strobe for high byte (UCAS#). For alternate function see “Multiple Function Pin Descriptions” on page 19.
WE# (UWE#)	O	61	Multiple Function: DRAM Write Enable Strobe (WE#). For alternate function see “Multiple Function Pin Descriptions” on page 19.

Clock Inputs

Pin Name	Type	Pin #	Description
CLKI1	I	90	This pin, along with CLKO1 is the 25.175 MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin is the clock input.
CLKO1	O	91	This pin, along with CLKI1 is the 25.175 MHz2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin should be left unconnected.
CLKI2	I	86	This pin, along with CLKO2 is the 28.322 MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin is the clock input.
CLKO2	O	87	This pin, along with CLKI2 is the 28.322 MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin should be left unconnected.

LCD Panel Interface

Pin Name	Type	Pin #	Description
YD	O	10	Vertical Scanning Start Pulse output. A logic 1 on this signal, sampled by the LCD module on the falling edge of LP, is used by the panel row drivers (Y drivers) to indicate the start of the vertical frame.
LP	O	13	Latch Pulse output. The falling edge of this signal is used to latch a row of display data in the LCD module's column driver shift registers and to turn on the row driver (Y driver) for that line.
XSCL	O	12	Shift Clock for LCD data. Display data is clocked out of the chip on the rising edge of this signal, to be shifted into the LCD panel module column drivers (X drivers) on each falling edge.
XSCL2	O	9	This second shift clock is used together with XSCL in 8-bit single color panel mode to shift in alternate sets of display data. XSCL2 is also used alone as the shift clock in 8-bit dual color panel mode and 4-bit single color panel mode.
UD[0:3]	O	22..25	Upper panel display data for dual panel - dual drive mode. For 8-bit single panel-single drive mode, these bits are the most significant 4-bits of the 8-bit output data to the panel (data[7:4]). For 4-bit single panel mode, these bits are the 4 bits of data output to the panel. For 16-bit LCD modes, these outputs are the multiplexed upper panel data if MD[7]=1 at RESET, or the lower nibble of the upper panel data if MD[7]=0 at RESET.
UD[4:7]	O	26..29	When MD[7]=0 at RESET, these pins are the upper nibble of the 16-bit LCD mode upper panel data.
LD[0:3]	O	16..19	Lower panel display data for dual panel-dual drive mode. For 8-bit single panel-single drive mode, these bits are the least significant 4 bits of the 8-bit output data to the panel (data[3:0]). For 4-bit single panel mode, these outputs are driven low. For 16-bit LCD modes, these outputs are the multiplexed lower panel data if MD[7]=1 at RESET, or the lower nibble of the lower panel data if MD[7]=0 at RESET.
LD[4:7]	O	30..33	When MD[7]=0 at RESET, these pins are the upper nibble of the 16-bit LCD mode lower panel data.
LCDPWR#	O	21	LCD power control. In normal operation this signal is driven low to enable an external LCD power supply. This signal is driven high when the chip is put into any power save mode, when Auxiliary Register 06 bit 0 is set to 1, or when the Sequencer is in a reset state. It can be used externally to turn off the panel supply voltage and backlight. After a RESET, this signal is held high until the CRTC is programmed and running.
WF	O	15	LCD Backplane Bias signal. This output toggles once every n LP periods, as programmed in Auxiliary Register [0D].

External CRT/RAMDAC Interface

Pin Name	Type	Pin #	Description
P[0:7]	O	26..33	When MD[7]=1 at RESET, these pins are the Pixel Data outputs. These 8 bits are connected to the pixel select inputs of the external RAMDAC.
PCLK	O	34	Pixel Clock. Pixel data is clocked out of the chip on the falling edge of PCLK.
BLANK#	O	44	Blank output. This output is clocked out on the falling edge of PCLK and is driven low during display blanking periods.
HSYNC#	O	41	Horizontal Sync. This output is clocked out on the falling edge of PCLK and is driven to indicate the horizontal retrace period. The polarity of this signal is determined by a control bit in register 3C2h.
VSYNC#	O	42	Vertical Sync. This output is clocked out on the falling edge of PCLK and is driven to indicate the vertical retrace period. The polarity of this signal is determined by a control bit in register 3C2h.
DACRD#	O	43	RAMDAC Read Strobe. This signal goes low when a valid read access to the VGA RAMDAC is decoded by the chip.
DACWR#	O	45	RAMDAC Write Strobe. This signal goes low when a valid write access to the VGA RAMDAC is decoded by the chip.
RS2	O	46	Register Select 2 output. This output should be connected to the RS2 input of the RAMDAC (Bt477 or equivalent). The logic level on this output may be set by setting Auxiliary Register [0B] bit 3. This signal is required to allow CPU access the control and overlay registers of the external RAMDAC.
OL[0:1]	I/O	39, 38	Multiple Function: Overlay Select outputs 1:0 When MD[13]=0 at RESET, these pins are outputs used to provide sprite/HW cursor function on the CRT display. In this case, these outputs should be connected to the OL[0:1] inputs of the RAMDAC (Bt477 or equivalent). They are used by the sprite circuitry to access the overlay registers in the RAMDAC. For alternate function see “Multiple Function Pin Descriptions” on page 19.
OL23	O	35	Overlay Select output 2/3. This output should be connected to both the OL2 and OL3 inputs of the RAMDAC (Bt477 or equivalent). This signal is used by the sprite circuitry to access the overlay registers in the RAMDAC.For alternate function see “Multiple Function Pin Descriptions” on page 19.
D477	O	40	477 Control Signal. This output should be connected to the 477/471 input of the RAMDAC (Bt477 or equivalent). This signal is used to access the control register of the RAMDAC and to allow it to be powered down. The logic level on this output can be controlled by setting Auxiliary Register [0B] bit 4, and is also controlled by the power save logic.
IREFEN#	O	47	IREF Enable output. This signal is used to control the external current reference source required by the RAMDAC, allowing powering down the analog circuitry when not required. When this signal is driven low, the external current reference should be enabled. When this signal is high, the external current reference should be shut off.
MS[2:0]	I/O	83, 82, 71	Monitor Sense inputs. These signals should be connected to the monitor sense lines from the CRT monitor cable. The status of these bits is readable in Auxiliary Register [08] bits 2:0, and is used by BIOS software to determine the presence and type of monitor connected. Optionally, the SENSE output of the RAMDAC may be connected to one of these inputs to allow the BIOS to read the SENSE signal and detect the monitor. MS[2:1] can be forced low by the DCC2 monitor support bits in Auxiliary Register [10] bits 1:0.

Power Save Mode Control

Pin Name	Type	Pin #	Description
SUSPEND#	I	84	A low level on this pin puts the chip into a hardware power down mode. The SUSPEND# signal overrides any software initiated power down modes, and disables the ISA-Bus interface inputs except RESET. Address and Data inputs are also masked when this signal is low. When in Suspend Mode the UD(3:0), LD(3:0), XSCL, XSCL2, LP, YD and WF signals are driven into a high impedance or low state (configurable) and the LCDPWR# signal is driven high.
PDCLK	I	143	Power Down Clock. This input may be used to provide a low frequency clock for generating refresh in Power Save Modes 4 and Suspend, as an optional alternative to using the pixel clock or MEMEN input as the refresh clock source. This clock input should be driven by either by a 32 kHz 50% duty cycle clock source, or a 64 kHz clock source with a high period as short as possible (but > minimum RAS low pulse width) to minimize DRAM current consumption during refresh. The PDCLK input is used to directly generate the RAS and CAS pulses during Power Save Mode 4 and Suspend.

Power Supply

Pin Name	Type	Pin #	Description
COREVDD	P	14, 37, 85, 92, 109	V_{DD} supply for core logic.
IOVDD	P	1, 50, 73, 124	V_{DD} supply for interface pins.
VSS	P	11, 36, 88, 89, 108	V_{SS} supply for core logic.
IOVSS	P	49, 72, 123, 144	V_{SS} supply for interface pins.

Pin Mapping for Various Display Modes

SPC8106 Pin Name	Display Mode		RGBI	12-bit RGB	TFT		
	CRT	LCD			9-bit	12-bit AUX[00]b5=1 AUX[0B]b1=0	12-bit AUX[00]b5=1 AUX[0B]b1=1
VSYNC#	VSYNC#	None	None	None	None	None	VSYNC#
HSYNC#	HSYNC#	None	None	None	None	None	HSYNC#
YD	None	YD	VSYNC#	VSYNC#	VSYNC#	VSYNC#	None
LP	None	LP	HSYNC#	HSYNC#	HSYNC#	HSYNC#	None
WF	None	WF	None (forced 0)	None (forced 0)	DATAEN	DATAEN	DATAEN
XCSL	None	XCSL	PCLK	PCLK	PANCLK	PANCLK	PANCLK
XCSL2	None	XCSL2	None (forced 0)	R[3]	R[2]	R[3]	R[3]
UD[3]	None	UD[3]	None (forced 0)	B[3]	B[2]	B[3]	B[3]
UD[2]	None	UD[2]	None (forced 0)	B[2]	B[1]	B[2]	B[2]
UD[1]	None	UD[1]	None (forced 0)	B[1]	B[0]	B[1]	B[1]
UD[0]	None	UD[0]	None (forced 0)	R[2]	R[1]	R[2]	R[2]
LD[3]	None	LD[3]	D[3]	G[3]	G[2]	G[3]	G[3]
LD[2]	None	LD[2]	D[2]	G[2]	G[1]	G[2]	G[2]
LD[1]	None	LD[1]	D[1]	G[1]	G[0]	G[1]	G[1]
LD[0]	None	LD[0]	D[0]	R[1]	R[0]	R[1]	R[1]
OL0	OL0	None	None	B[0]	None	B[0]	B[0]
OL1	OL1	None	None	G[0]	None	G[0]	G[0]
OL23	OL23	None	None	R[0]	None	R[0]	R[0]

Mixed Voltage Configurations

Core VDD	I/O VDD	
	3.3 V	5.0 V
3.3 V	OK	OK
5.0 V	NO	OK

Summary of Configuration Options

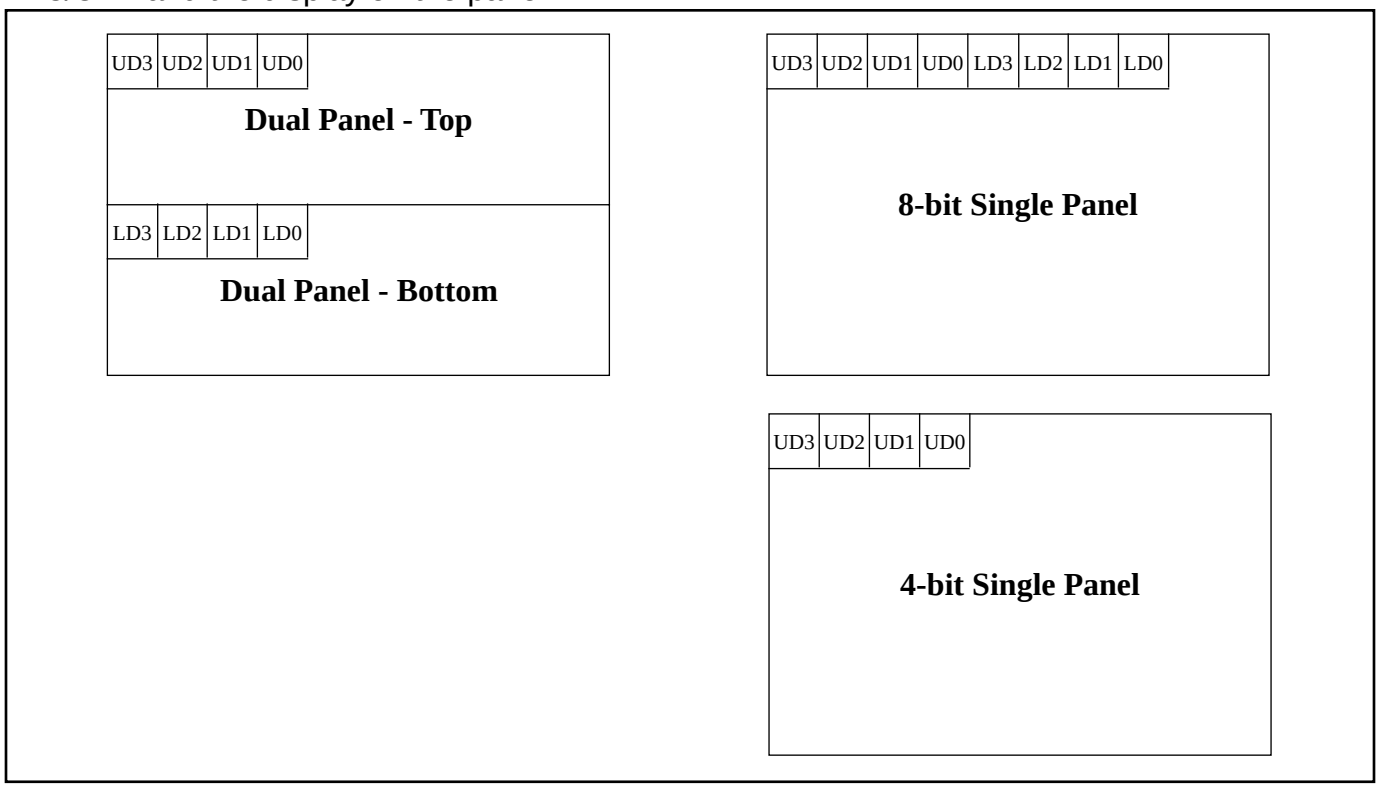
Pin Name	value on this pin at falling edge of RESET is used to configure: (1/0)
MD[3:0]	values latched into read-only Aux Reg[0C] bits 3:0 for software use
MD[4]	16-bit I/O interface (1) / 8-bit I/O interface (0)
MD[5]	A[19:2] latched internally by ALE (1) / standard ISA bus ALE - A[16:0] not latched (0)
MD[6]	2 CAS, 1 WE type DRAM (1) / 1 CAS, 2 WE type DRAM (0)
MD[7]	support 16-bit panel with external logic (1) / support 16-bit panel directly (0)
MD[8]	5 V core operating voltage (1) / 3.3 V core operating voltage (0)
MD[12:9]	values latched into read-only bits 7:4 of Aux Reg[0C] for software use
MD[13]	pins 38, 39 used for ext. RC for 32 kHz PDCLK (1) / pins 38, 39 used for OL[1:0] (0)
MD[14]	Internal PDCLK doubling disable (1) / enable (0)
MD[15]	3C3h used as video enable port (1) / 46E8h and 102h used as video enable port (0)

These inputs have internal pullup resistors. Based on the value of the internal pull-ups, the external pull-down resistors if necessary, should be approximately 15K ohm. This value will provide the correct voltage levels on power-up without loading the DRAM Data lines (V_{DD} = 5.0V).

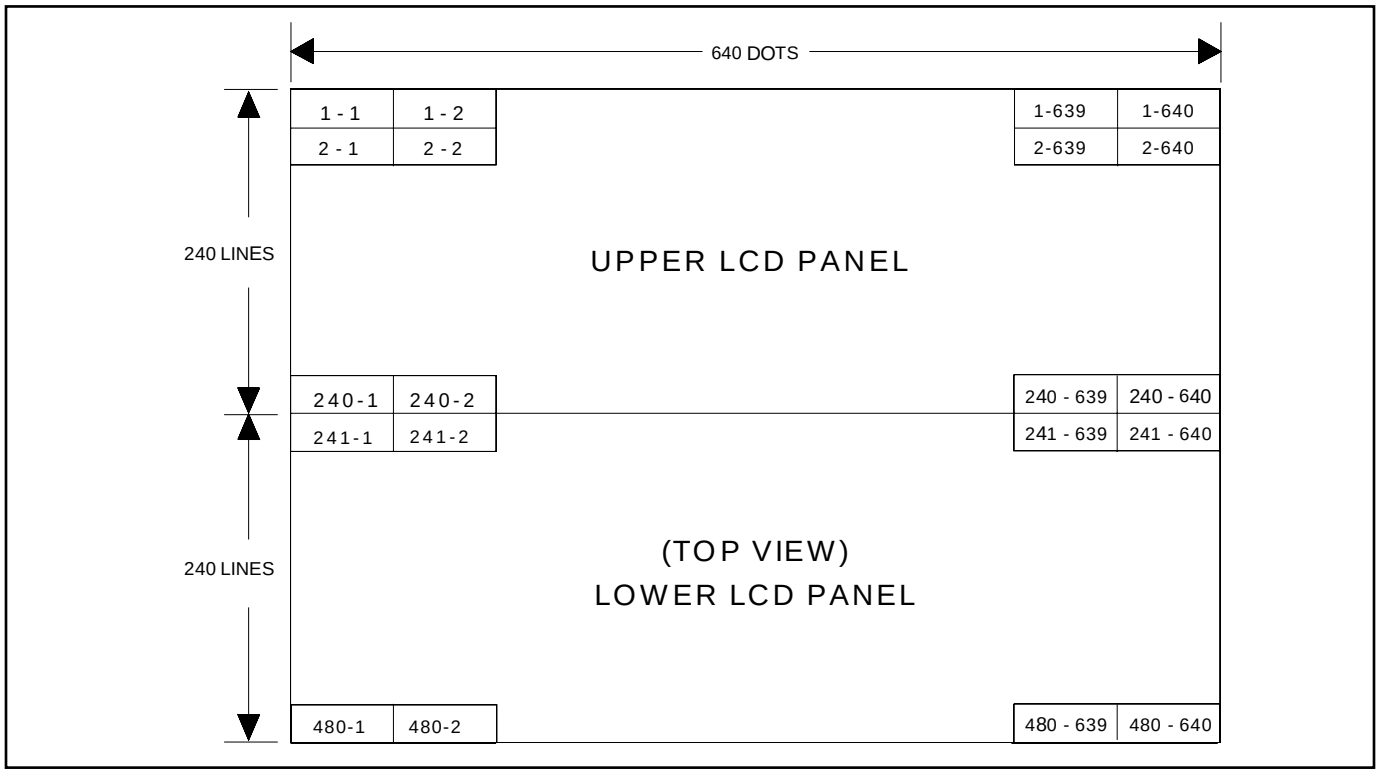
Multiple Function Pin Descriptions

Pin Name	Function	MD Line Status	Functional Description
LCAS#, LWE#	LCAS#	MD6 = 1	DRAM Column Address Strobe (Low Byte)
	LWE#	MD6 = 0	DRAM Write Strobe (Low Byte)
UCAS#, CAS#	UCAS#	MD6 = 1	DRAM Column Address Strobe (High Byte)
	CAS#	MD6 = 0	DRAM Column Address Strobe
WE#, UWE#	WE#	MD[6] = 1	DRAM Write Strobe
	UWE#	MD[6] = 0	DRAM Write Strobe (High Byte)
OL0, P320, B0	OL0	MD[13] = 0 AUX[00] b6=0	Overlay Bit 0. Used for CRT HW Cursor/Sprite support.
	P320	MD[13] = 1 MD[14] = 1	32 kHz Clock Output. Used with external RC when using external PDCLK support
	B0	MD[13] = 0 AUX[00] b6=1	Data bit B0 for 12-bit TFT support
OL1, P32I, G0	OL1	MD[13] = 0 AUX[00] b6=0	Overlay Bit 1. Used for CRT HW Cursor/Sprite support
	P32I	MD[13] = 1 MD[14] = 1	32 kHz Clock Input. Used with external RC when using external PDCLK support
	G0	MD[13] = 0 AUX[00] b6=1	Data bit G0 for 12-bit TFT support
OL23, R0	OL23	MD[13] = 0 AUX[00] b6=0	Overlay Bit 2. Used for CRT HW Cursor/Sprite support.
	R0	MD[13] = 0 AUX[00] b6=1	Data bit R0 for 12-bit TFT support
P[0:3]	P[0:3}	MD[7] = 1	Lower nibble of the CRT pixel data outputs
	UD[4:7}	MD[7] = 0	Upper nibble of the 16-bit LCD mode upper panel data
P[4:7]	P[4:7]	MD[7] = 1	Upper nibble of the CRT pixel data outputs
	LD[4:7]	MD[7] = 0	Upper nibble of the 16-bit LCD mode lower panel data

Illustrated below are the display data output which are output from the UD0 to UD3, LD0/UD4 to LD3/UD7 and the display on the panel:

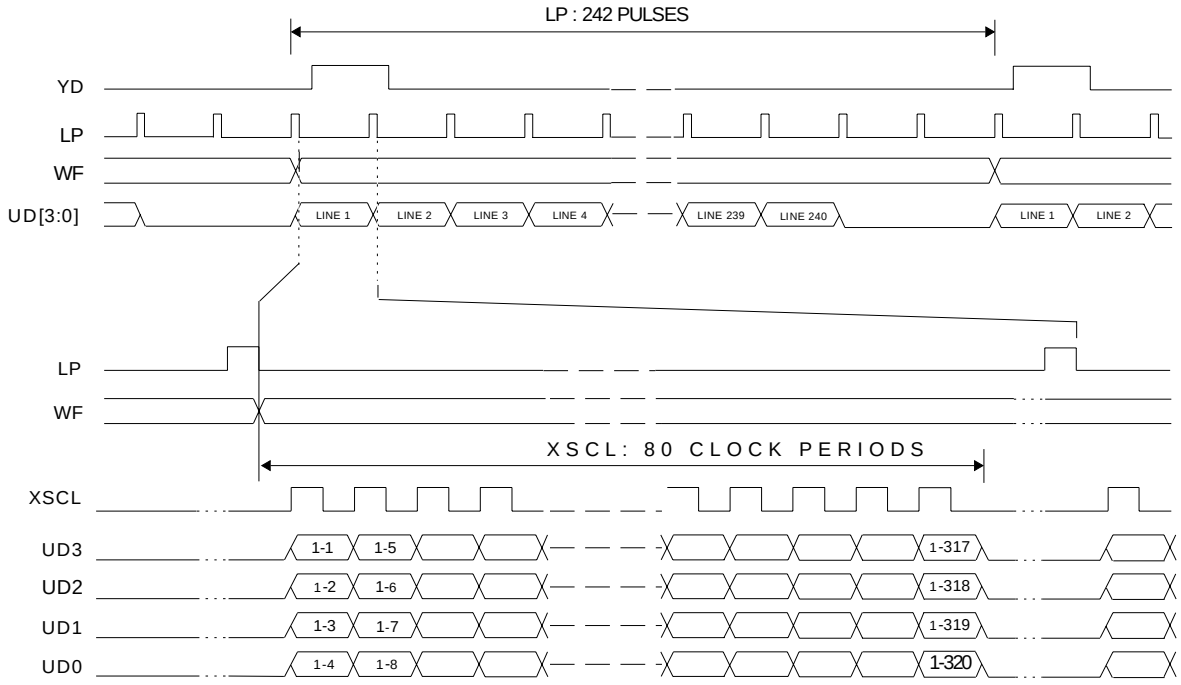


■ LCD PANEL PIXELS



■ MONOCHROME PASSIVE STN LCD PANEL INTERFACE

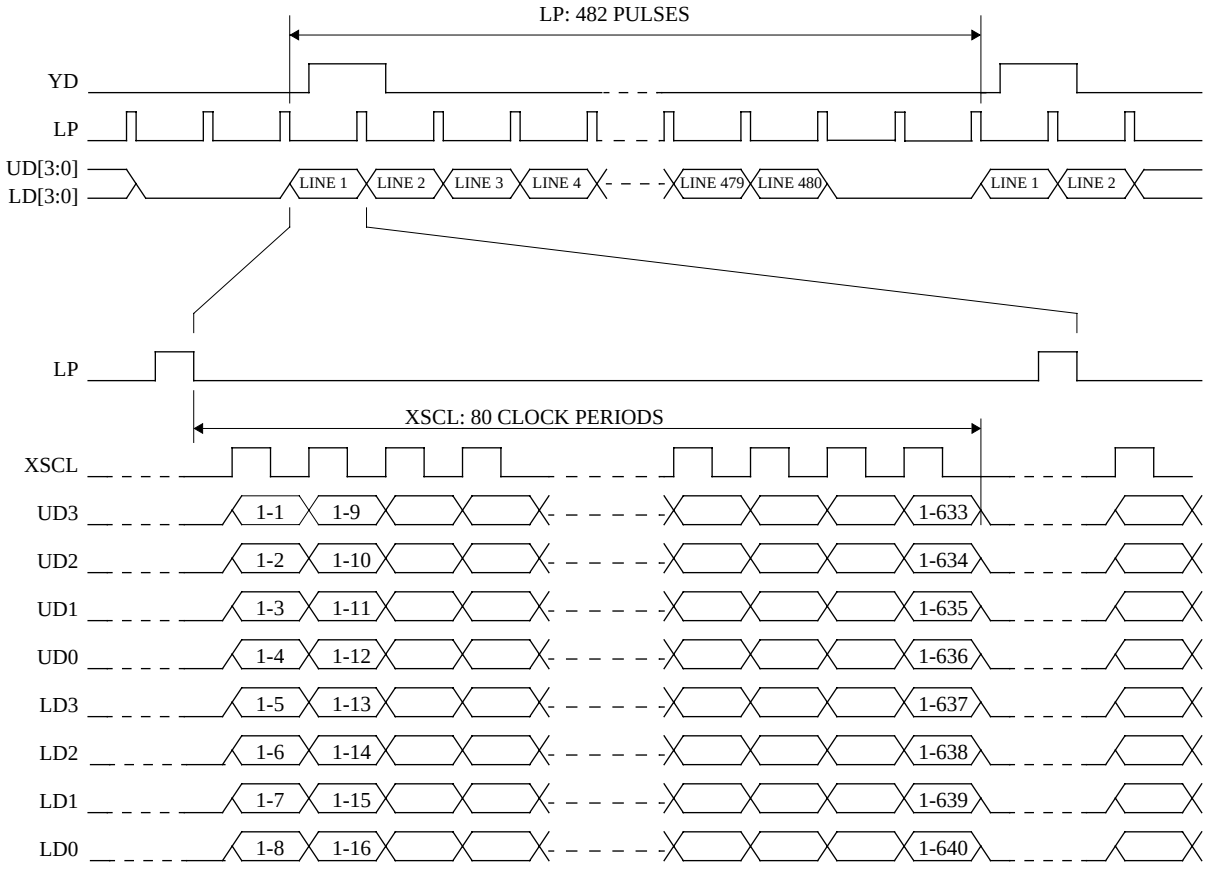
4-BIT SINGLE PANEL



Example timing for a 320 x 240 panel

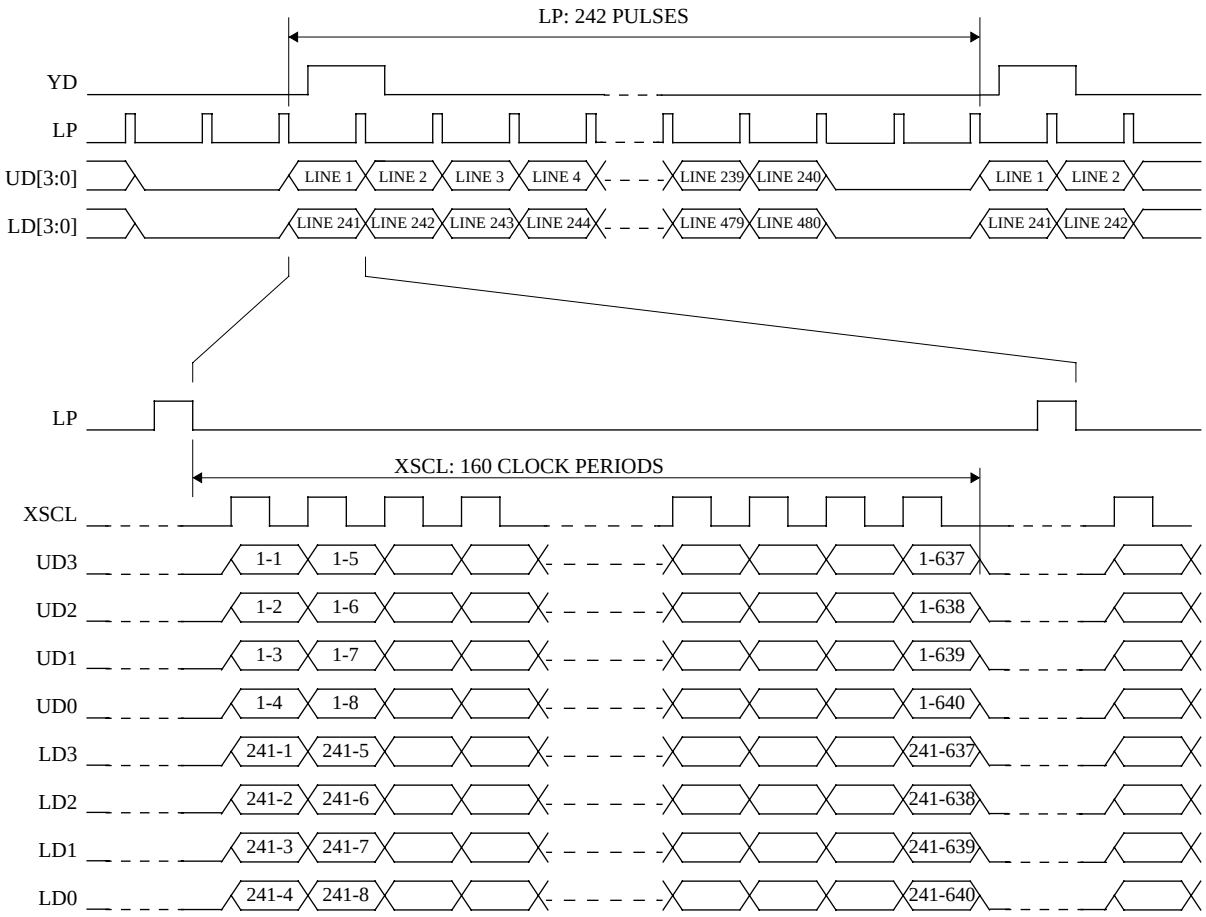
■ MONOCHROME PASSIVE STN LCD PANEL INTERFACE

8-BIT SINGLE PANEL



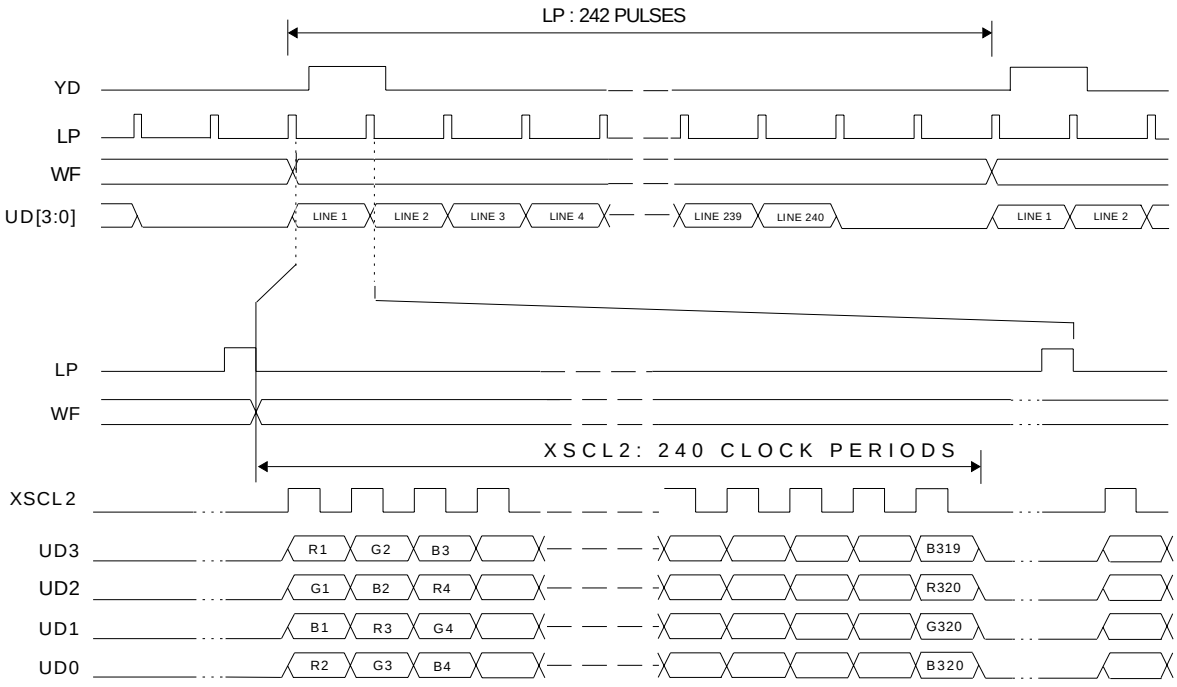
■ MONOCHROME PASSIVE STN LCD PANEL INTERFACE

8-BIT DUAL PANEL



■ COLOR STN LCD PANEL INTERFACE

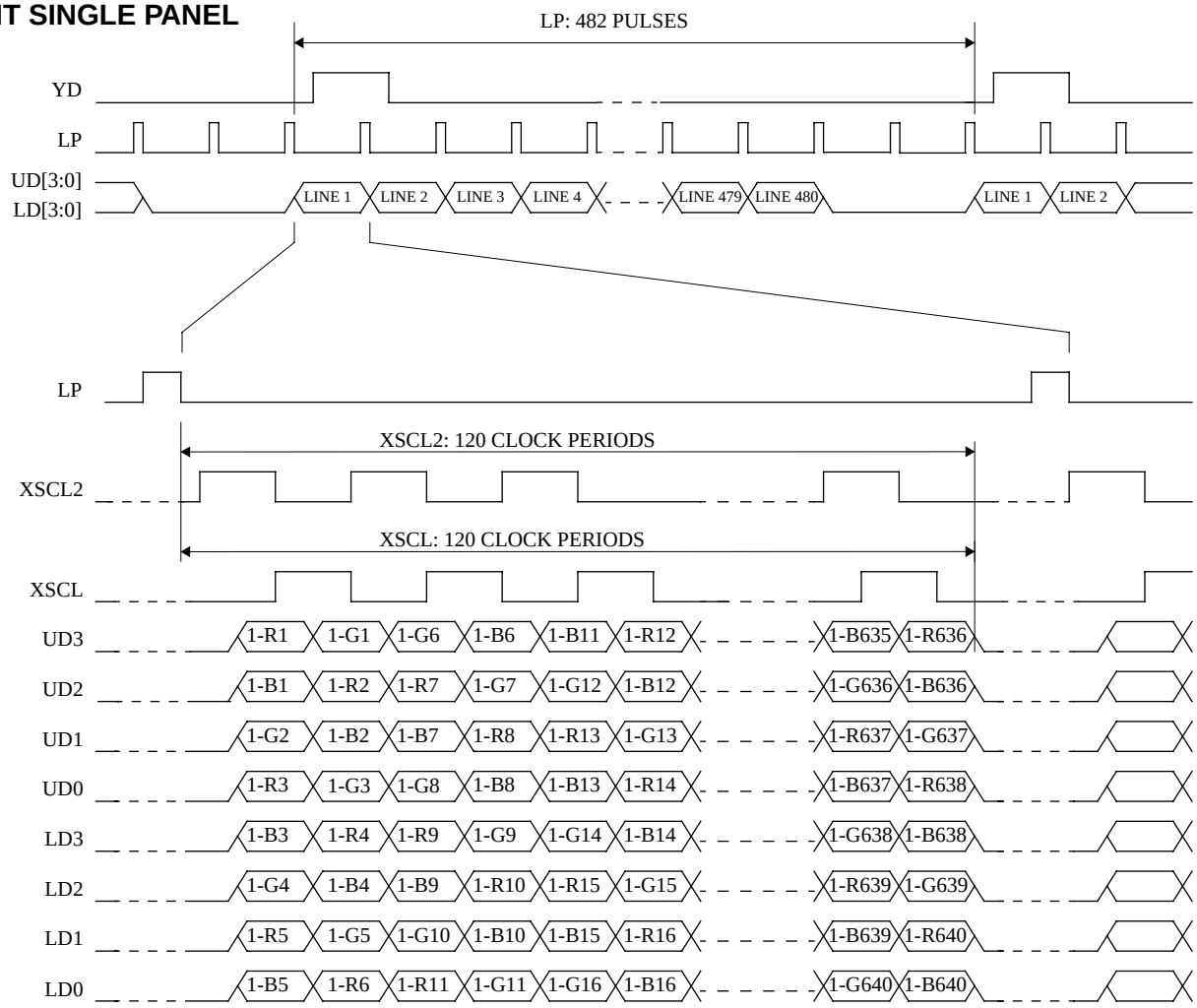
4-BIT SINGLE PANEL



Example timing for a 320 x 240 panel

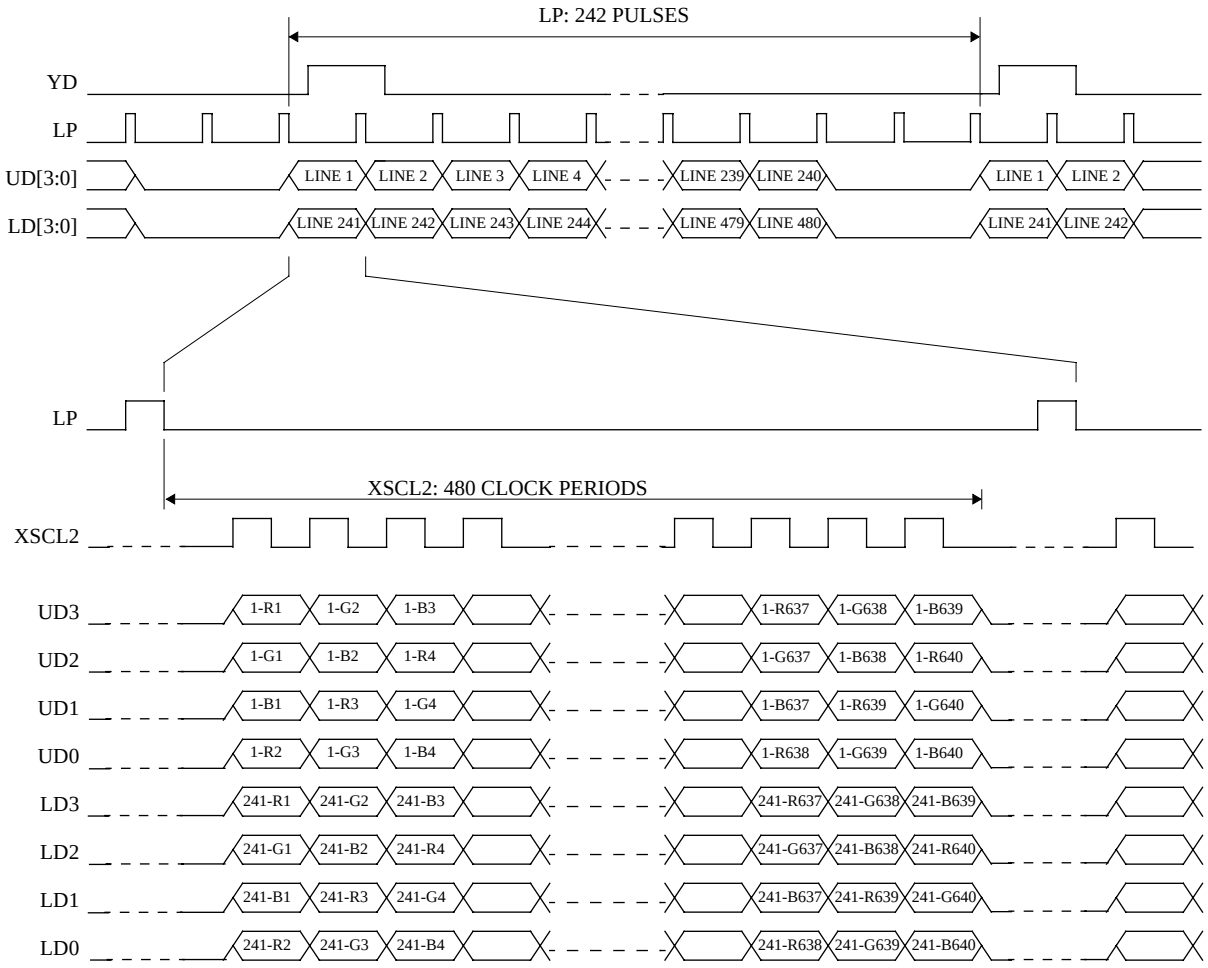
■ COLOR STN LCD PANEL INTERFACE

8-BIT SINGLE PANEL



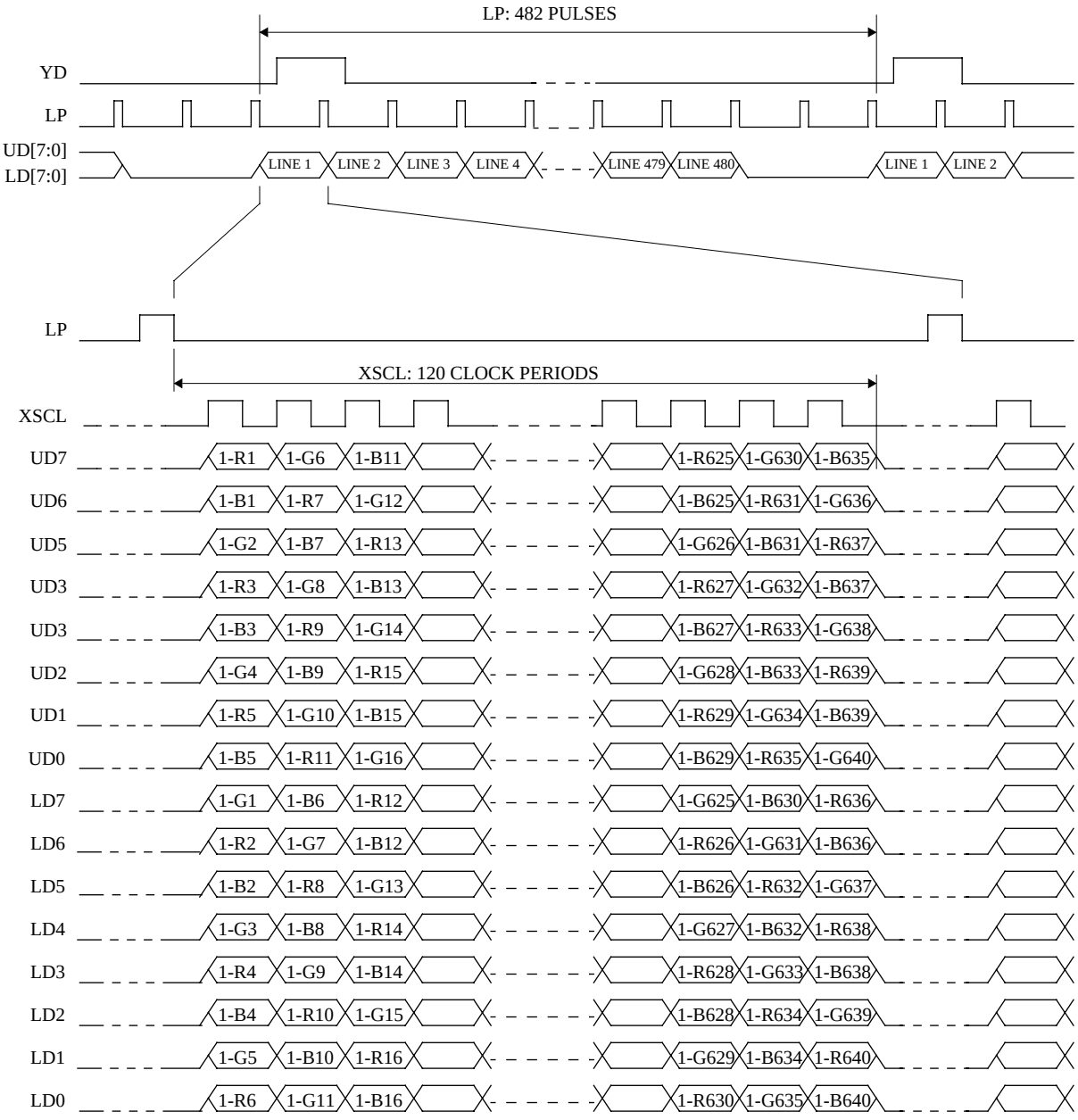
■ COLOR STN LCD PANEL INTERFACE

8-BIT DUAL PANEL



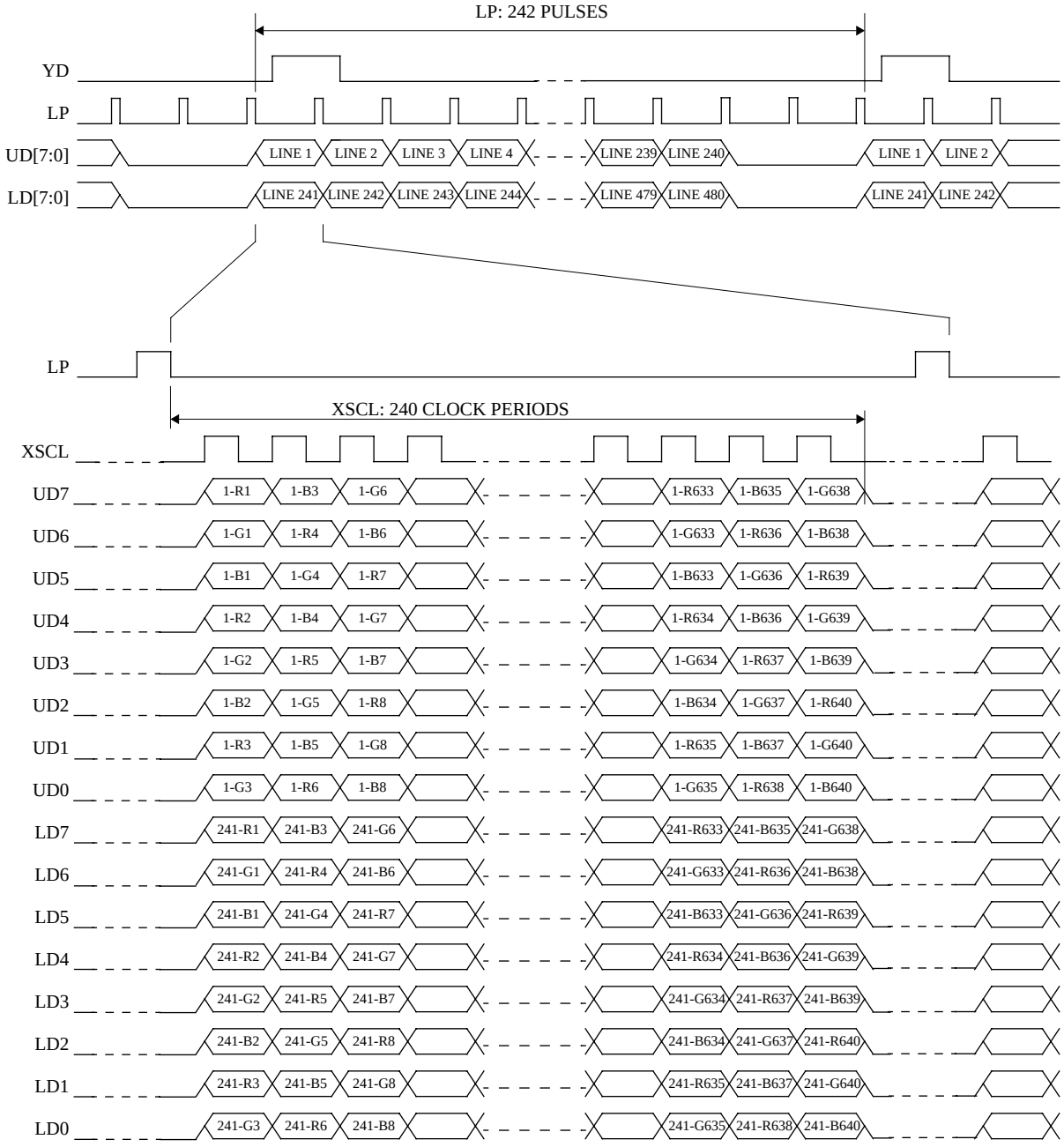
■ COLOR STN LCD PANEL INTERFACE

16-BIT SINGLE PANEL



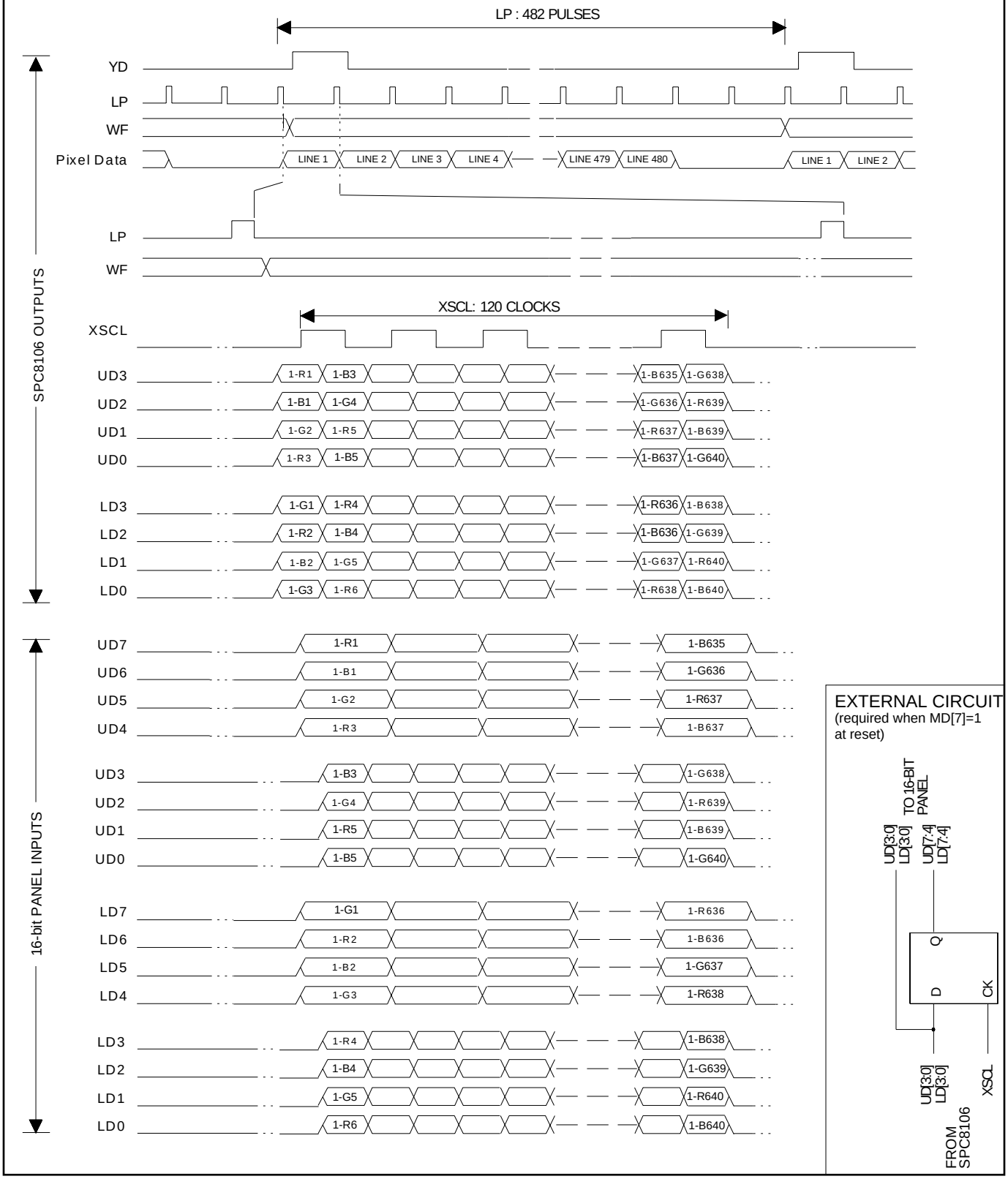
■ COLOR STN LCD PANEL INTERFACE

16-BIT DUAL PANEL



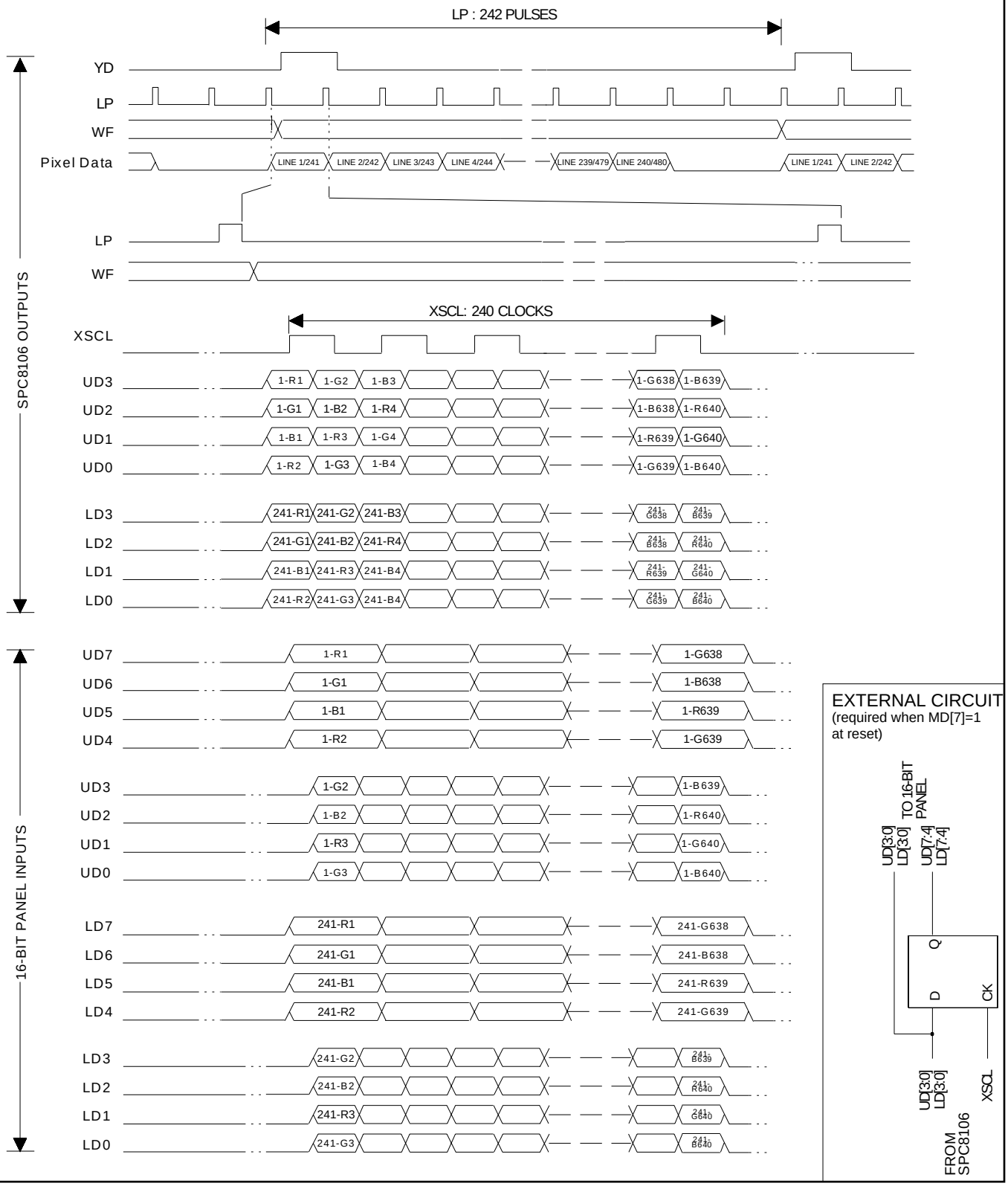
■ COLOR STN LCD PANEL INTERFACE

16-BIT SINGLE PANEL WITH EXTERNAL CIRCUIT



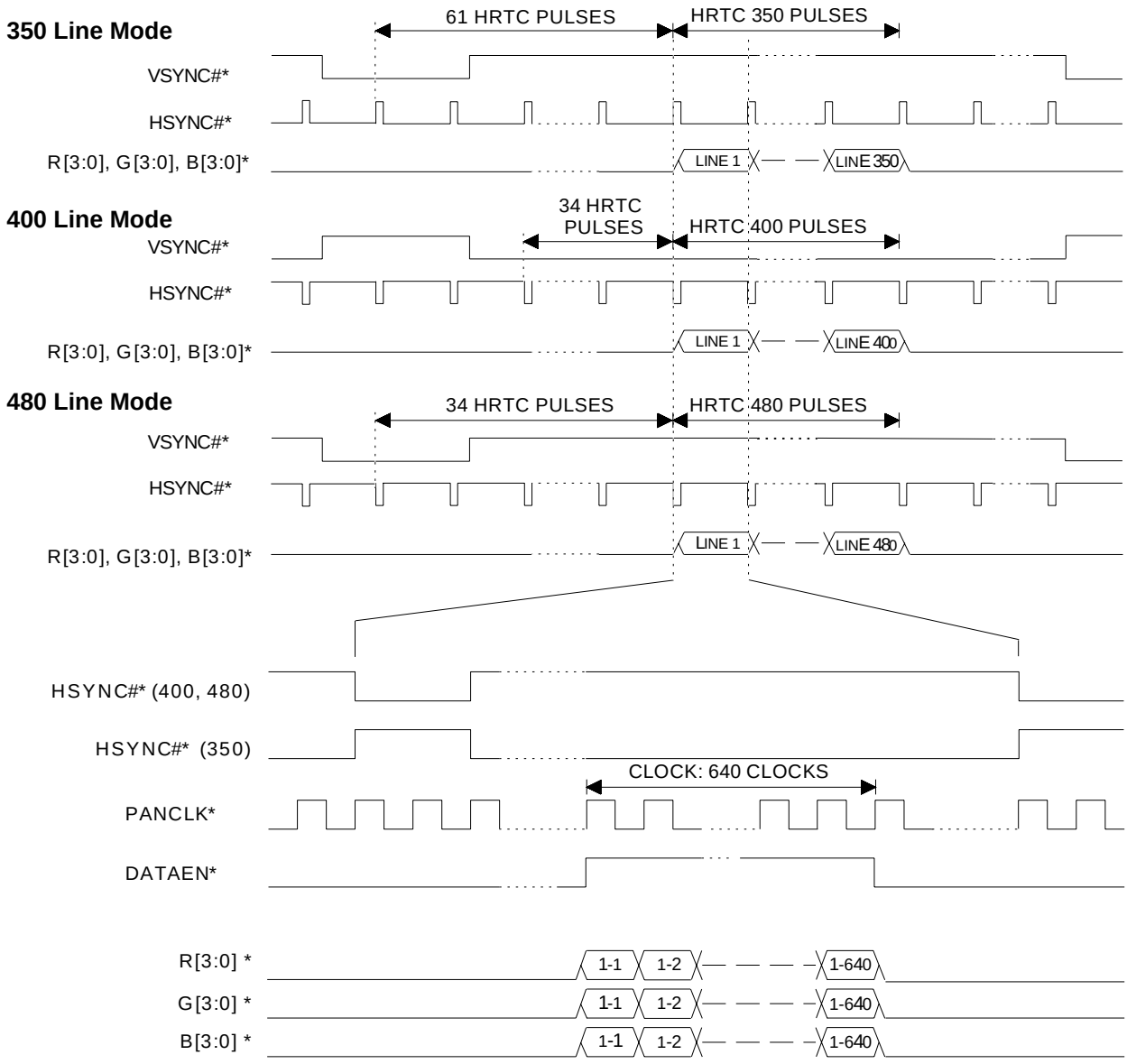
■ COLOR STN LCD PANEL INTERFACE

16-BIT DUAL PANEL WITH EXTERNAL CIRCUIT



■ COLOR TFT PANEL INTERFACE

Auxiliary Register [00] bit 5=1 and Auxiliary Register [0B] bit 1=1

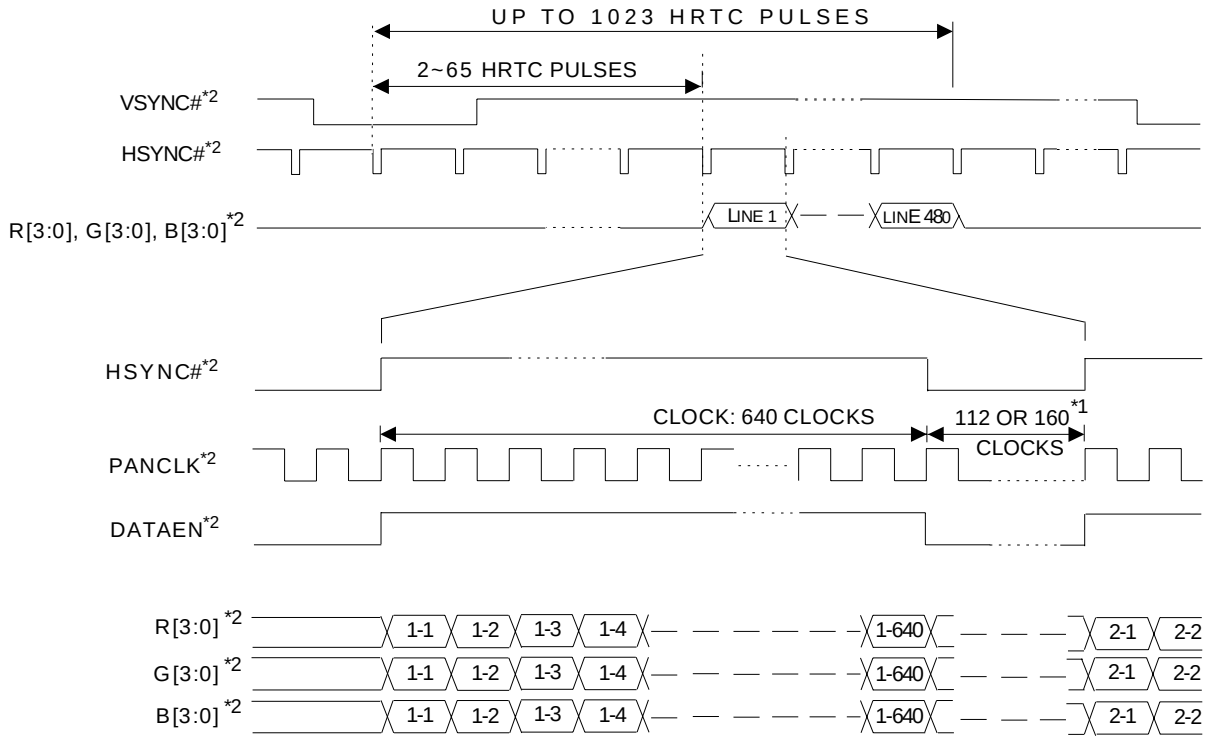


9-bit panels use data bits [2:0]

* Refer to “Pin Mapping for Various Display Modes” on page 15 for actual pin names

■ COLOR TFT PANEL INTERFACE

Auxiliary Register [00] bit 5=1 and Auxiliary Register [0B] bit 1=0



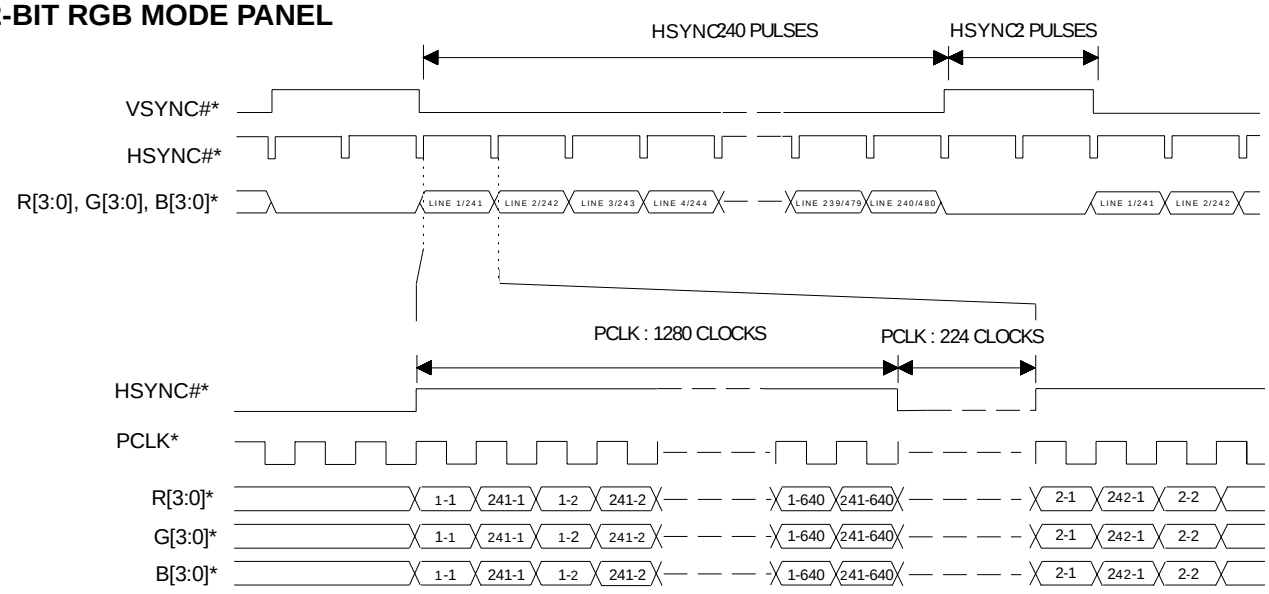
9-bit panels use data bits [2:0]

*1 - This number is controlled by Auxiliary Register [06] bit 2

*2 - Refer to “Pin Mapping for Various Display Modes” on page 15 for actual pin names

■ RGB MODE PANEL INTERFACE

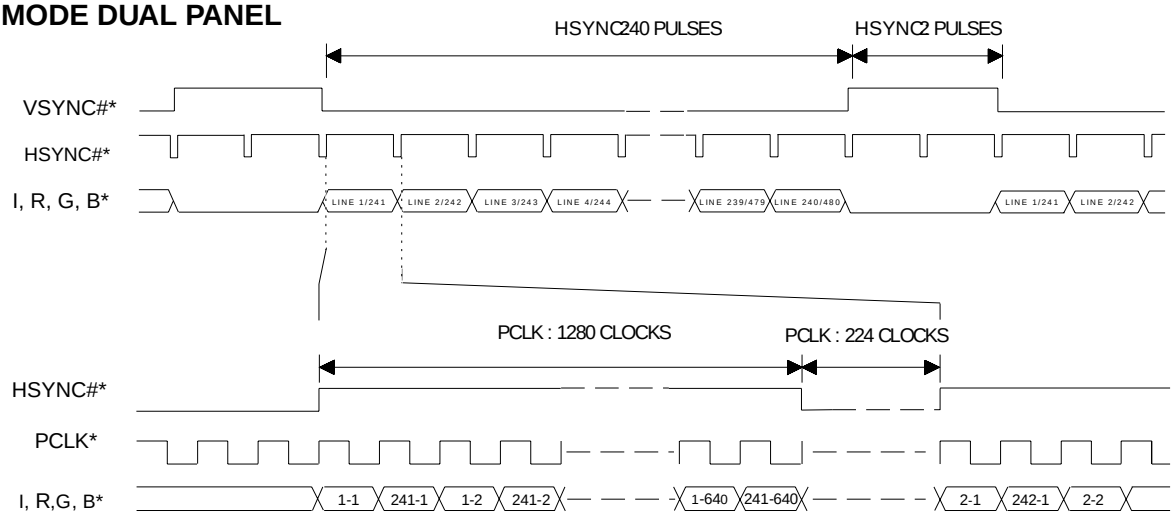
12-BIT RGB MODE PANEL



* Refer to “Pin Mapping for Various Display Modes” on page 15 for actual pin names

■ RGBI MODE DUAL PANEL INTERFACE

RGBI MODE DUAL PANEL



* Refer to “Pin Mapping for Various Display Modes” on page 15 for actual pin names

■ PACKAGE DIMENSIONS (SPC8106F0C)