CIRRUS LOGIC®

CL-GD5200

Preliminary Data Sheet

FEATURES

- 256 x 18-bit Color Lookup RAM
- Triple 8-bit D/A converters
- 80-MHz operation for analog outputs
- 80-MHz operation for pixel clock input (Multimedia Modes)
- Anti-sparkle circuitry
- Monitor-sense output with built-in comparators
- RS-343A/RS-170-compatible outputs
- External voltage or current reference
- Standard VGA-system-compatible interface
- Full compatibility with industry-standard Brooktree® Bt476 when used in compatible mode
- Full compatibility with Sierra® SC11487™
- 44-pin PLCC with Brooktree Bt476-compatible pinout
- 28-pin DIP with Sierra SC11487-compatible pinout
- 5V CMOS monolithic construction
- On-the-fly switching between Lookup Table and extended modes for video overlay
- Special keyed software switch allows access to extended modes
- Seven multimedia extended modes:
  - — 5-5-5 RGB Mode with 32K colors
  - — 5-6-5 RGB Mode with 64K colors
  - — 16-bit/pixel YUV Mode
  - — 8-bit/pixel Compressed Mode
  - — 15-color Border Encoded Mode for animation
  - — 8-8-8 RGB Mode with 16-million colors (Targa 24-bit/pixel True Color)
  - — 32K color plus 256-color LUT Mixed Mode

True Color Multimedia Palette DAC

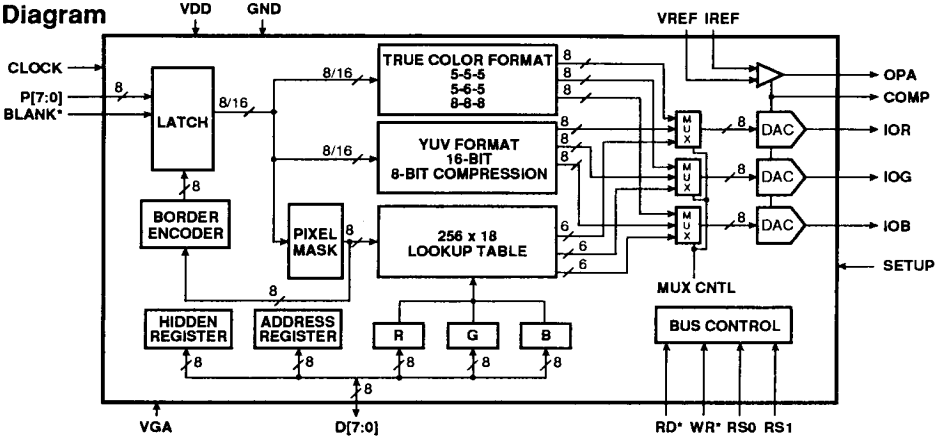
OVERVIEW

The CL-GD5200 is a high-performance multimedia palette DAC designed for high-resolution color graphics subsystems. The device is a Brooktree Bt476- and Sierra SC11487 pin- and software-compatible palette DAC designed specifically for VGA-compatible color graphics. The CL-GD5200 is available in a 44-pin PLCC or a 28-pin DIP package that is capable of replacing the existing SC11487 palette DAC in any graphics subsystem.

The CL-GD5200 has a 256 x 18-color Lookup Table with triple 8-bit video D/A converters. The CL-GD5200 also provides anti-sparkle circuitry to eliminate undesirable pixel flash during palette updates. The CL-GD5200 True Color Multimedia Palette DAC also supports several additional modes useful in multimedia applications: 16-bit/pixel YUV Mode, 5-5-5 RGB (TARGA) format, 5-6-5 RGB (XGA) format, 24-bit 8-8-8 RGB (TARGA) format; 8-bit/pixel Compressed YUV Mode, and 15-color Border Encoded Mode for animation.

The CL-GD5200 generates RS-343A-compatible video signals into a doubly-terminated 75Ω load, and RS-170-compatible video signals into a singly-terminated 75Ω load, without requiring external buffering.

Functional Block Diagram



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1. PIN INFORMATION

The CL-GD5200 is available in a 44-pin plastic lead chip carrier (PLCC) or 28-pin dual in-line package (DIP) device configuration.

1.1 Pin Diagram (44-Pin PLCC)

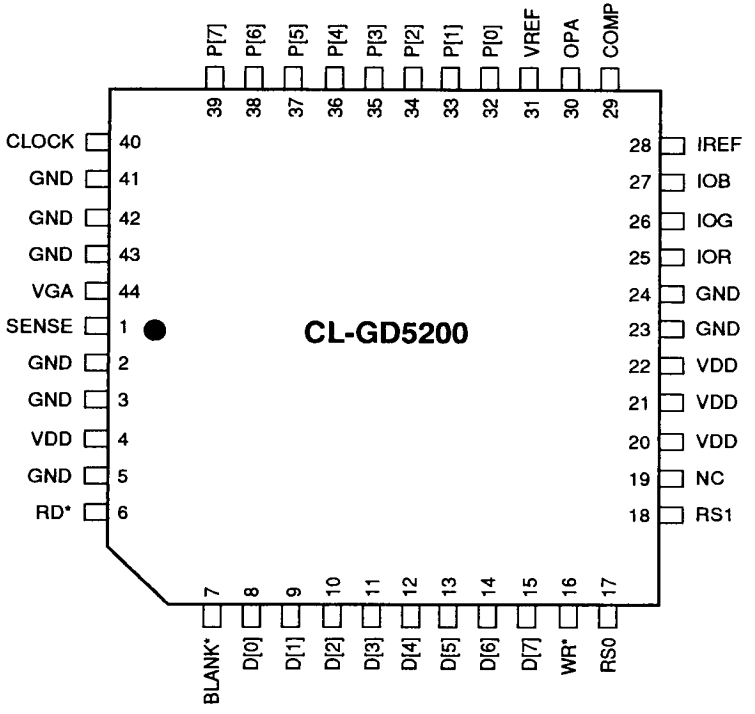


Figure 1–1. CL-GD5200 Pin Diagram (44-Pin)

1.2 Pin Diagram (28-Pin DIP)

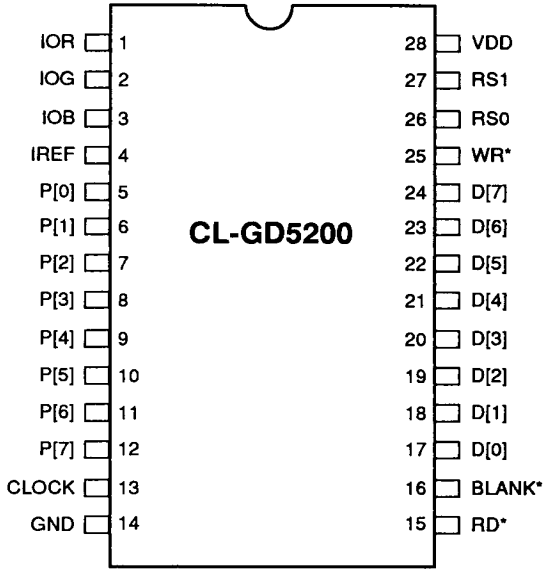


Figure 1–2. CL-GD5200 Pin Diagram (28-Pin)

1.3 Pin Assignment Table

The following conventions are used in the pin-assignment table: * = negative-true signal; I = input; O = output; AN = analog; PWR = power; TTL = the pad has standard TTL-input threshold and TTL-output levels.

Name	Pin (44-Pin)	Pin (28-Pin)	Type	Description
BLANK*	7	16	I	BLANK* Input
CLOCK	40	13	I	Video Clock Input
P[7:0]	39:32	12:5	I	Video Data Input
IOR	25	1	AN	Analog Red
IOG	26	2	AN	Analog Green
IOB	27	3	AN	Analog Blue
COMP	29	–	AN	Compensation
WR*	16	25	I	MPU Write Control
RD*	6	15	I	MPU Read Control
D[7:0]	15:8	24:17	I/O	MPU Data Bus
RS1	18	27	I	Register Select
RS0	17	26	I	Register Select
SENSE	1	–	O	Video Output Sense
VGA	44	–	I	VGA Standard LUT Select
IREF	28	4	AN	Current Reference
VREF	31	–	AN	Voltage Reference
OPA	30	–	AN	Reference Amplifier Output
VDD	4, 20, 21, 22	28	PWR	Analog Power (+5V)
GND	2, 3, 5, 23, 24, 41-43	14	PWR	Analog Ground
NC	19	–	–	No Connect

2. DETAILED PIN DESCRIPTIONS

Name	Type	Description
BLANK*	I	**COMPOSITE BLANK CONTROL INPUT:** A logic zero drives the analog outputs to the blanking level, as illustrated in Table 3–4. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the PEL inputs are ignored.
CLOCK	I	**CLOCK INPUT:** The rising edge of CLOCK latches the P[7:0] and BLANK* inputs. It is typically the pixel clock rate of the video system. For 15/16-bit/pixel Modes it is twice the video pixel rate, and for the 24-bit/Pixel Mode it is three-times the video pixel rate.
P[7:0]	I	**PIXEL SELECT INPUTS:** These inputs specify, on a pixel basis, which one of the 256 entries in the Color Palette RAM is to be used to provide color information. They are also inputs to the internal DACs. These inputs are latched on the rising edge of CLOCK. P[0] is the least-significant bit. Unused inputs should be connected to GND.
IOR	AN	**ANALOG RED:** This analog output supplies current corresponding to the red value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, either the 6-bit value from the Lookup Table or a 5-,6- or 8-bit true-color value is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the IOR, IOG, and IOB outputs is related to IREF as follows: $IF = (63/30) \times IREF$ To maintain IBM VGA-compatibility, each DAC output is typically terminated to monitor ground with a 150Ω two-percent resistor. This resistor in parallel with the 75Ω resistor in the monitor will yield a 50Ω impedance to ground. For a full-scale voltage of 700 mV, full-scale current output should be 14 mA.
IOG	AN	**ANALOG GREEN:** This analog output supplies current corresponding to the green value of the pixel being displayed. See the description of IOR for information regarding the termination of this pin.
IOB	AN	**ANALOG BLUE:** This analog output supplies current corresponding to the blue value of the pixel being displayed. See the description of IOR for information regarding the termination of this pin.
COMP	AN	**COMPENSATION:** (44-pin package only) If an external-voltage reference is used (see Figure 8–1), this pin should be connected to OPA. If an external current reference is used (see Figure 8–2), this pin should be connected to IREF. A 0.1-μF ceramic capacitor must always be used to bypass this pin to VDD. The COMP capacitor must be placed as close to the device as possible to keep lead lengths to an absolute minimum.
WR*	I	**CPU WRITE CONTROL:** D[7:0] data is latched on the rising edge of WR*, and RS1, RS0 are latched on the falling edge of WR* during CPU write operations.

2.0 DETAILED PIN DESCRIPTIONS *(cont.)*

Name	Type	Description
RD*	I	**CPU READ CONTROL:** To read data from the device, RD* must be a logical zero. RS1 and RS0 are latched on the falling edge of RD* during CPU read operations.
D[7:0]	I/O	**CPU DATA BUS:** Data is transferred into and out of the device over this 8-bit bidirectional data bus. D[0] is the least-significant bit.
RS1–RS0	I	**REGISTER SELECT:** RS1 and RS0 specify the type of read or write operation being performed, as illustrated in Tables 3–1 and 3–2.
SENSE	O	**VIDEO OUTPUT SENSE:** (44-pin package only) This output is a logical zero if one or more of the IOR, IOG, or IOB analog outputs have exceeded the internal-reference voltage of 335 mV. This may be used for monitor-type detection.
VGA	I	**VGA STANDARD LUT SELECT:** (44-pin package only) This input pin is normally kept at a logical zero (or GND) for CL-GD5200 operation, as controlled by the programming of the CL-GD5200 Hidden Register. If this pin is brought to a logic one, then the CL-GD5200 is forced into VGA-standard Lookup Table Mode; the data on D[7:0] will be input on the rising edge of CLOCK. This input is sampled on each rising edge of CLOCK.
IREF	AN	**CURRENT REFERENCE:** Full-Scale Adjust Control. When using an external voltage reference (see Figure 8–1) a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is: **RSET(Ω) = K*1,000*VREF(V)/Iout(mA)** 'K' is defined as 2.1 for doubly-terminated 75Ω loads. It is recommended that a 147Ω RSET resistor be used. When using an external-current reference, the relationship between IREF and the full-scale output current on each output is: **REF(mA) = Iout(mA)/K; K = 2.100**
VREF	AN	**VOLTAGE REFERENCE:** If an external-voltage reference is used (see Figure 8–1), it must supply this input with a 1.2V (typical) reference. If an external-current reference is used (see Figure 8–2 or 8–3), this pin should be left floating, except for the bypass capacitor. A 0.1-µF ceramic capacitor must always be used to decouple this input to VDD. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
OPA	AN	**REFERENCE AMPLIFIER OUTPUT:** (44-pin package only) If an external-voltage reference is used (see Figure 8–1), this pin must be connected to COMP. When using an external-current reference (see Figure 8–2), this pin should be left floating.
VDD	PWR	**ANALOG POWER (+5V):** All VDD Pins must be connected.
GND	PWR	**ANALOG GROUND:** All GND Pins must be connected.
NC	–	NO CONNECT

3. FUNCTIONAL DESCRIPTION

3.1 CPU Interface

The CL-GD5200 supports a standard CPU bus interface, allowing the CPU direct access to the Color Palette RAM.

The RS0 and RS1 select inputs specify whether the CPU is accessing the Address Register, Color Palette RAM, or Read Mask Register, as shown in Table 3–1. The 8-bit Address Register ADDR [7:0] is used to address the Color Palette RAM, eliminating the requirement for external address multiplexers. ADDR[0] corresponds to D0 of the CPU Data Bus [7:0] and is the least-significant bit.

3.2 Writing Color Palette RAM Data

To write color data, the CPU writes the Address Register (RAM Write Mode) with the address of the Color Palette RAM location to be modified. The CPU performs three successive write cycles (6 bits each of red, green, and blue), using RS0, RS1 to select the Color Palette RAM. After the Blue Write Cycle, the three bytes of color information are concatenated into an 18-bit word and written to the location specified by the Address Register. The Address Register then increments to the next location, which the CPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

3.3 Reading Color Palette RAM Data

To read Color Palette RAM data, the CPU loads the Address Register (RAM Read Mode) with the address of the Color Palette RAM location to be read. The contents of the Color Palette RAM at the specified address are copied into the RGB registers and the Address Register is incremented to the next RAM location. The CPU performs three successive read cycles (six bits each of red, green, and blue), using RS0, RS1 to select the Color Palette RAM. Following the Blue Read Cycle, the contents of the Color Palette RAM at the address specified by the Address Register are copied into the RGB Registers and the Address Register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Table 3–1. Control Input Truth Table

RS1	RS0	Addressed by CPU
0	0	Address Register (RAM Write Mode)
1	1	Address Register (RAM Read Mode)
0	1	Color Palette RAM
1	0	Pixel Mask Register

3.4 Additional Information

When accessing the Color Palette RAM, the Address Register resets to 00_H following a blue read or write cycle to RAM location FF_H.

The CPU interface operates asynchronously to the pixel clock. Data transfers between the Color Palette RAM and the Color Registers are synchronized by internal logic, and occur in the period between CPU accesses. Occasional accesses to the Color Palette RAM can be made without noticeable disturbance on the display screen. However, operations requiring frequent access to the Color Palette (i.e., block files of the Color Palette) should be done during the blanking interval. Anti-sparkle circuitry causes the most recently displayed color data to be maintained at the inputs of the three D/A converters to reduce noticeable sparkling.

To keep track of the red, green, and blue read/write cycles the Address Register has two additional bits (ADDRa, ADDRb) that count modulus three, as shown in Table 3–2. They are reset to a zero when the CPU writes to the Address Register, and are not reset to a zero when the CPU reads the Address Register. The CPU does not have access to these bits. The other eight bits of the Address Register increment following a blue read or write cycle. ADDR[7:0] are accessible to the CPU, and are used to address Color Palette RAM loca-

tions as shown in Table 3–2. The CPU may read the Address Register at any time without modifying its contents or the existing read/write mode.

Table 3–2. Address Register (ADDR) Operation

	Value	RS1	RS0	Addressed by CPU
ADDRa, ADDRb (counts 3)	00 01 10	0 0 0	1 1 1	red value green value blue value
ADDR[7:0] (counts binary)	$00_H - FF_H$	0	1	Color Palette RAM

3.5 Data Bus Interface

Color data is contained on the lower six bits of the data bus, with D0 being the LSB, and D5 the MSB of color data. When writing color data, D6 and D7 will be a logical zero.

3.6 Frame Buffer Interface

The P[7:0] inputs are used to address the Color Palette RAM as shown in Table 3–3. The contents of the Pixel Mask Register, which may be accessed by the CPU at any time, are bit-wise logically ANDed with the P[7:0] Inputs. Bit 0 of the pixel Read Mask Register corresponds to pixel input P0. The addressed location provides 18 bits of color information to the three D/A converters.

Table 3–3. Pixel Control Truth Table

P[7:0]	Addressed by frame buffer
00_H	Color Palette RAM location 00_H
01_H	Color Palette RAM location 01_H
:	:
FF_H	Color Palette RAM location FF_H

(Pixel Read Mask Register = FF_H)

The BLANK* Input, is latched on the rising edge of CLOCK to maintain synchronization with the color data. Table 3–4 details how the BLANK* Input modifies the output levels.

Table 3–4. Video Output Truth Table

Description	Iout (mA)	V_{OUT} (V)	BLANK	DAC (Input Data)
WHITE	17.62	0.660	1	FF_H
DATA	data	data	1	data
BLACK	0	0	1	00_H
BLANK	0	0	0	XX_H

NOTE:
75Ω doubly-terminated load, VREF = 1.235V, RSET = 147Ω.

The analog outputs of the CL-GD5200 are capable of directly driving a 37.5Ω load, such as a doubly-terminated 75Ω coaxial cable.

4. AVAILABLE MODES DESCRIPTION

4.1 Compatible Mode

When powered-up, or if the CL-GD5200 Hidden Register is cleared to all zeros, the palette chip is in Compatible Mode. In this mode all functionality is equivalent to the industry-standard Bt476.

4.2 Extended Modes

By writing a code to the CL-GD5200 Hidden Register, the chip can be placed in one of the six extended modes. The method of writing to the CL-GD5200 Hidden Register is as follows:

a) Read from the Pixel Mask Register at Address 10 (RS0 = 0, RS1 = 1) four times in succession. No other read/writes should be directed to that address.

b) The following single read or write from Address 10 will be directed to the CL-GD5200 Hidden Register. Subsequent reads or writes from the Register will need to be preceded by following step (a) again.

4.3 Extended Mode Hardware Override (On-the-Fly Mode Switching)

The CL-GD5200 Input Pin VGA (Pin 44; this feature is available only in the 44-pin PLCC package), when driven high, will force the CL-GD5200 into the compatible mode, overriding the Extended Mode programmed in the Hidden Register. This feature allows external hardware to control switching between standard VGA Mode and one of the 16-bit/pixel Extended Modes, to enable a video overlay function. For example, external hardware could control a data multiplexer that would select between video data from a VGA controller or from a video digitizer. The video digitizer data could be in 16-bit YUV or RGB format. The external hardware must be capable of supplying valid data one byte at a time at the required clock rate for the extended mode programmed. If 16-bit RGB Mode is used, multiples of two bytes must always be transferred. If the 16-bit YUV Mode is used, then multiples of four bytes must be sent for proper operation of the Extended Mode. The sampled high-to-low transition of VGA Pin will synchronize the video data input for 2-byte RGB or 4-byte YUV Mode.

5. HIDDEN REGISTER

Bit	Description	Reset State
7	Extended Modes Enable	0
6	Extended Mode Select	0
5	Data Clock Control	0
4	Interpolation and Mix-Mode Control	0
3	Reserved	0
2	Mode Bit 2	0
1	Mode Bit 1	0
0	Mode Bit 0	0

This register is used to enable extended color modes, including 15-bit/pixel, 16-bit/pixel, 24-bit/pixel, and YUV Modes. This register is cleared to all zeroes at RESET, placing the CL-GD5200 in VGA-compatibility Mode.

This register is accessed by reading the Pixel Mask Register at Address 10 (RS0 = 0, RS1 = 1) four times in succession. The next read or write at this address will access this Hidden Register. Subsequent accesses require the four accesses to the Pixel Mask Register.

Bit	Description
7	**Extended Modes Enable:** If this bit is programmed to a zero, the Extended Color Modes are disabled and the Palette DAC is VGA-compatible (Bt476 Mode). If this bit is programmed to a one, Extended Color Modes are enabled, as chosen by Bit 6 and Bits 2:0 of this register.
6	**Extended Mode Select:** If this bit is programmed to a zero and Bit 7 is programmed to a one, the Palette DAC will be in 5-5-5 RGB Color Mode (TARGA-compatible Mode), regardless of the value programmed into Bits 2:0. If this bit is programmed to a one and Bit 7 is programmed to a one, the Palette DAC Mode will be chosen by the value programmed into Bits 2:0 of this register.
5	**Data Clock Control:** If this bit is programmed to a zero, Clocking Mode 1 will be chosen. In Clocking Mode 1, 16-bit/pixel Modes will use both edges of CLOCK to latch data. The rising edge of CLOCK will latch the least-significant byte and the falling edge of CLOCK will latch the most-significant byte. If this bit is programmed to a one, Clocking Mode 2 will be chosen. In Clocking Mode 2, 16-bit/pixel Modes will use only the rising edge of CLOCK to latch data. The CLOCK must be supplied at twice the pixel rate. The least-significant byte is latched on the first rising edge and the most-significant byte is latched on the second rising edge. **NOTE:** All modes other than 16-bit/pixel Mode use only the rising edge of CLOCK regardless of the setting of this bit.

5. HIDDEN REGISTER *(cont.)*

Bit	Description
4	**Interpolation and Mix-Mode Control:** If this bit is programmed to a zero, interpolation for 16-bit YUV Mode, or normal 5-5-5 RGB Color Mode is enabled. If this bit is programmed to a one, interpolation of U and V for even pixels in 16-bit YUV Mode is disabled, or if set for 32K color (5-5-5 RGB) Mode, then Pixel Data Bit 15 is used to select between LUT operation (using Bits 7:0 with Bits 14:8 ignored) or 32K color (using Bits 14:0).
3	**Reserved:** This bit must always be programmed to a zero to guarantee upward compatibility.
2:0	**Mode Bits:** If Bits 7 and 6 are both programmed to ones, this three-bit field selects the Extended Color Mode as defined in the following table:

Bit 7	Bit 6	Bit 2	Bit 1	Bit 0	Function
0	X	X	X	X	VGA Compatibility
1	0	X	X	X	5-5-5 RGB Color Mode (Targa-compatible Mode)
1	1	0	0	X	5-6-5 RGB Color Mode (XGA-compatible Mode)
1	1	0	1	0	Border Encoded 8-bit Mode
1	1	0	1	1	YUV Mode, 16 bits/pixel
1	1	1	0	0	Compressed Mode, 8 bits/pixel
1	1	1	0	1	8-8-8 RGB Color Mode, 16M Colors
1	1	1	1	0	DAC Power-down
1	1	1	1	1	ID Register Access (reading Hidden Register will show $0B_H$ as current-revision CL-GD5200)

6. EXTENDED MODE DESCRIPTIONS

6.1 5-5-5 RGB Mode With 32K Colors

This mode supports the industry-standard 5-5-5 RGB Mode of 32K colors. Each pixel is represented by two bytes containing five bits each of red, green and blue color intensity information (format given below). The input sequence for each pixel is low-byte first, followed by high-byte. The first low-byte will be taken on the first rising edge of CLOCK occurring when BLANK* has gone inactive (high). All subsequent bytes are clocked in on the rising edge of CLOCK. The Color Lookup Table (LUT) is ignored in this mode. The data is presented to the DACs directly as the most-significant bits, with the low bit set to a zero.

Storage Scheme:

- 15 bits per PEL
- 32K colors per PEL
- 2 bytes per PEL
- Input sequence is low-byte first, high-byte second

PEL Data Format:

One PEL																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Field Bit Pos.
X	4	3	2	1	0	4	3	2	1	0	4	3	2	1	0	Color Bit Pos.
Red Level						Green Level					Blue Level					

MIX-MODE: If the Mix-mode Bit (Bit 4) in the Hidden Register is set, then Bit D15 of the pixel data is used to select between the 5-5-5 RGB Mode, and use of the standard Palette DAC Lookup Table (Palette) on a pixel-by-pixel basis. This will be useful in applications such as multimedia windows for displaying palettized image data in a 32K-color interface without the need to translate the image into 15-bit RGB data. The pixel data has the following format:

One PEL																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Field Bit Pos.
0	4	3	2	1	0	4	3	2	1	0	4	3	2	1	0	Color Bit Pos.
5-5-5	Red Level					Green Level					Blue Level					

One PEL																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Field Bit Pos.
1	X	X	X	X	X	X	X	7	6	5	4	3	2	1	0	Color Bit Pos.
LUT	Ignored							DAC Lookup Table Input								

6.2 5-6-5 RGB Mode with 64K Colors

This mode supports the 5-6-5 RGB Mode of 64K colors. Each pixel is represented by two bytes containing five bits of red and blue, and six bits of green color intensity information (format given below). The input sequence for each pixel is low-byte first, followed by high-byte. The first low-byte will be taken on the first rising edge of CLOCK occurring when BLANK* has gone inactive (high). All subsequent bytes are clocked in on the rising edge of CLOCK. The Color Lookup Table (LUT) is ignored in this mode. Data is presented to the DACs directly as the most-significant bits, with the lower bits set to a zero.

Storage Scheme:

- 16 bits per PEL
- 64K colors per PEL
- 2 bytes per PEL
- Input sequence is low-byte first, high-byte second

PEL Data Format:

One PEL																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Field Bit Pos.
4	3	2	1	0	5	4	3	2	1	0	4	3	2	1	0	Color Bit Pos.
Red Level					Green Level						Blue Level					

6.3 True Color 16-Bit YUV Mode

This mode displays 16 million colors using 16-bit YUV in a format compatible with 4:2:2 video. Each individual PEL has an associated 8-bit Y (or luminance) value that represents the intensity component for that PEL. The chrominance value for every two PELs — one 8-bit U and one 8-bit V — is accumulated, thus representing the color component for those two PELs. To smooth the color transitions, the odd PEL U and V values are computed as the average of the previous and current values. The tables below illustrate the input format and the interpolation scheme. Synchronization is achieved using the BLANK* Signal. Byte 1 is the first byte latched when BLANK* goes high. Interpolation is not applied to the first PEL of each scanline.

16-bit YUV PEL Data Format

Byte 1

7	6	5	4	3	2	1	0
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
PEL#1	PEL#1	PEL#1	PEL#1	PEL#1	PEL#1	PEL#1	PEL#1

Byte 2

7	6	5	4	3	2	1	0
U7	U6	U5	U4	U3	U2	U1	U0
PEL#1-2	PEL#1-2	PEL#1-2	PEL#1-2	PEL#1-2	PEL#1-2	PEL#1-2	PEL#1-2

Byte 3

7	6	5	4	3	2	1	0
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
PEL#2	PEL#2	PEL#2	PEL#2	PEL#2	PEL#2	PEL#2	PEL#2

Byte 4

7	6	5	4	3	2	1	0
V7	V6	V5	V4	V3	V2	V1	V0
PEL#1-2	PEL#1-2	PEL#1-2	PEL#1-2	PEL#1-2	PEL#1-2	PEL#1-2	PEL#1-2

Interpolation Format

PEL	1	2
Y-value:	Y0	Y1
U-value:	(Ua+Ub)/2	Ub
V-value:	(Va+Vb)/2	Vb

NOTE: Ua,Va are the previous U and V values; Ub,Vb are the current U and V values.

6.4 Compressed YUV Mode (8 Bits/PEL)

This mode displays up to 16-million colors (2^{24}) using a compressed delta-YUV data format.

This coding scheme used for natural images encodes the Y (luminance) information at high resolution and sub-samples the UV (chrominance) information at a fraction of the resolution of the Y Signal. This approach takes advantage of the lower sensitivity of the human eye to color as compared to luminance (brightness). Differential encoding further reduces the amount of memory used for an image by encoding the differences between successive Y, U, and V values, and uses companding to favor the resolution of small differential changes over large differential changes.

There are several pixel data compositions that can be used to encode the Y (luminance), U (blue-green axis) and V (red-green axis). In this scheme, each individual pixel element (PEL) has an associated 5-bit luminance (Y) component. Each luminance component is differentially encoded (i.e., an encoded value is used to represent the difference between that Y value and the previous Y value). By use of a companding table, each 5-bit encoded value represents a particular 8-bit difference value. Table 6–1 presents the companding table, which shows both the encoding that must be done on the original picture data and the decoding that is performed by the CL-GD5200. For the first PEL of each line, the 5-bit Y value represents the upper-five bits of an 8-bit initialization value for a running sum. The lower-three bits of the sum are initialized to zero. Each subsequent 5-bit encoded value for that line is then expanded to 8 bits, using a 5-to-8 expansion ROM, and added to the running sum to generate the next 8-bit Y value. The addition permits overflow so negative difference values are encoded by allowing the sum to wrap around.

Every four PELs, one 5-bit U and one 5-bit V chrominance component are accumulated, which represents the average color value for those PELs. These components are also encoded using the same differential companding method used for the Y component. An additional two bits used to form a 'Transition Code' are accumulated every four bytes. These bits indicate where the transition from the previous U and V values to the next U and V values should occur. This software-encoding process for the image handles the burden of determining where the significant color transitions of the image are, and encodes the color mixes and the codes appropriately. Table 6–1 illustrates how the colors transition for each of the available codes. Linear interpolation is used to average the delta between the previous and current U and V values. A value which is the average of the previous and current U or V value is sent for the PEL defined as the transition point. This averaging 'smooths-out' the color transitions between the four-PEL groups. Table 6–2 provides the encoded format for four bytes of PEL data representing a four-PEL group.

Table 6–1. Encoding and Decoding of Y, U, and V Companded Delta Values

Original Input Data Delta Value	Compressed Delta Data	CL-GD5200 Expanded Delta Output
0	0	0
1 OR -255	1	1
2 OR -254	2	2
3 OR -253	3	3
4 OR -252	4	4
5 OR -251	5	5
6 to 7 OR -250 to -249	6	6
8 to 10 OR -248 to -246	7	9
11 to 14 OR -245 to -242	8	12
15 to 19 OR -241 to -237	9	17
20 to 25 OR -236 to -231	10	22
26 to 33 OR -230 to -223	11	29
34 to 43 OR -222 to -213	12	38
44 to 56 OR -212 to -200	13	50
57 to 76 OR -199 to -180	14	66
77 to 106 OR -179 to -150	15	91
107 to 149 OR -149 to -107	16	128
150 to 179 OR -106 to -77	17	165
180 to 199 OR -76 to -57	18	190
200 to 212 OR -56 to -44	19	206
213 to 222 OR -43 to -34	20	218
223 to 230 OR -33 to -26	21	227
231 to 236 OR -25 to -20	22	234
237 to 241 OR -19 to -15	23	239
242 to 245 OR -14 to -11	24	244
246 to 248 OR -10 to -8	25	247
249 to 250 OR -7 to -6	26	250
251 OR -5	27	251
252 OR -4	28	252
253 OR -3	29	253
254 OR -2	30	254
255 OR -1	31	255

6.5 YUV-to-RGB Conversion Matrix for Both 16- and 8-Bit Compressed Modes

$$\begin{vmatrix} R \\ G \\ B \end{vmatrix} = \begin{vmatrix} 1 & 0 & 1.371 \\ 1 & -0.337 & -0.698 \\ 1 & 1.733 & 0 \end{vmatrix} \begin{vmatrix} Y \\ U \\ V \end{vmatrix}$$

Table 6–2. Transition Codes and Interpolation for a Four-PEL Block of Compressed YUV

Transition code: 00

PEL:	1	2	3	4
Y-value:	Y0	Y1	Y2	Y3
U-value:	(Ua+Ub)/2	Ub	Ub	Ub
V-value:	(Va+Vb)/2	Vb	Vb	Vb

Transition code: 01

PEL:	1	2	3	4
Y-value:	Y0	Y1	Y2	Y3
U-value:	Ua	(Ua+Ub)/2	Ub	Ub
V-value:	Va	(Va+Vb)/2	Vb	Vb

Transition code: 10

PEL:	1	2	3	4
Y-value:	Y0	Y1	Y2	Y3
U-value:	Ua	Ua	(Ua+Ub)/2	Ub
V-value:	Va	Va	(Va+Vb)/2	vb

Transition code: 11

PEL:	1	2	3	4
Y-value:	Y0	Y1	Y2	Y3
U-value:	Ua	Ua	Ua	(Ua+Ub)/2
V-value:	Va	Va	Va	(Va+Vb)/2

NOTE: PELs 1-4 indicate the position of the four PELs encoded in each 32 bits of data. Ub and Vb represent the value of U and V from the **current** data. Ua and Va represent the value of U and V from the **previous** data. The U-value and V-value are the displayed result for the indicated PEL. For the first four PELs of each scan-line Ua = Ub = U and Va = Vb = V.

Table 6–3. Compressed Delta-YUV PEL Data Format

Byte 1

7	6	5	4	3	2	1	0
TRANS CODE BIT 0	U1 PEL#1-4	U0 PEL#1-4	Y4 PEL#1	Y3 PEL#1	Y2 PEL#1	Y1 PEL#1	Y0 PEL#1

Byte 2

7	6	5	4	3	2	1	0
U4 PEL#1-4	U3 PEL#1-4	U2 PEL#1-4	Y4 PEL#2	Y3 PEL#2	Y2 PEL#2	Y1 PEL#2	Y0 PEL#2

Byte 3

7	6	5	4	3	2	1	0
TRANS CODE BIT 1	V1 PEL#1-4	V0 PEL#1-4	Y4 PEL#3	Y3 PEL#3	Y2 PEL#3	Y1 PEL#3	Y0 PEL#3

Byte 4

7	6	5	4	3	2	1	0
V4 PEL#1-4	V3 PEL#1-4	V2 PEL#1-4	Y4 PEL#4	Y3 PEL#4	Y2 PEL#4	Y1 PEL#4	Y0 PEL#4

After the interpolation process is completed, the processed UV color values are then dematrixed with the Y-intensity components to generate 8 bits each of R, G, and B output, which is presented directly to the 8-bit output DACs.

The synchronization of the byte-wide data starts from the first rising edge of CLOCK (PEL Data Clock) when the BLANK* Signal becomes inactive (high). All subsequent bytes are clocked in on each rising edge of CLOCK. In the CL-GD5200, there is a 7-CLOCK pipeline delay from when the first valid PEL data is clocked into the first valid RGB output.

6.6 15-Color Border Encoded Mode

This is a border encoded format designed for cartoon-type animation. In this format, each PEL is encoded with four bits. These four bits provide a LUT (Color Lookup Table) address to the palette, together with the upper-four Bank-select Bits from the VGA controller. These upper-four bits will be supplied from the Color-Select Registers. The lower-four bits of each non-zero PEL value are latched simultaneously while being presented to the LUT. If all four-lower bits of a PEL are a zero, then the previous non-zero latched 4-bit color value is sent to the LUT. The upper-four Bank-select Bits are not latched. As long as the latched lower 4-bit value equals a zero, the previous latched non-zero value is repeated until a new non-zero value is given.

Storage Scheme:

- 4 bits per PEL
- 15/256 colors per PEL
- 1 byte per PEL
- If color value P[3..0] equals a zero, the previous non-zero color value is repeated for LUT ADDR [3..0].

Byte Format

7	6	5	4	3	2	1	0
LUT ADDR 7	LUT ADDR 6	LUT ADDR 5	LUT ADDR 4	P3/LUT ADDR 3	P2/LUT ADDR 2	P1/LUT ADDR 1	P0/LUT ADDR 0

6.7 8-8-8 RGB Mode with 16M Colors

This mode supports the industry-standard 8-8-8 RGB Mode of 16-million colors. Each PEL is represented by three bytes containing 8 bits each of red, green, and blue color intensity information (format given below). The input sequence for each PEL is low-byte first, followed by middle-byte and then high-byte. The first low-byte will be taken on the first rising edge of CLOCK occurring when BLANK* has gone inactive (high). All subsequent bytes are clocked in on the rising edge of CLOCK. The Color Lookup Table (LUT) is ignored in this mode. The data is presented to the DACs directly, and the PEL output is at one-third of the CLOCK input rate.

Storage Scheme:

- 24 bits per PEL
- 16M colors per PEL
- Input sequence is Byte 1, Byte 2, Byte 3, Byte 1...

PEL Data Format:

Byte 1 (Blue Data)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Byte 2 (Green Data)

7	6	5	4	3	2	1	0
G7	G6	G5	G4	G3	G2	G1	G0

Byte 3 (Red Data)

7	6	5	4	3	2	1	0
R7	R6	R5	R4	R3	R2	R1	R0

7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Ambient operating temperature ..... -55° C to +125° C
Storage temperature ..... -65° C to +150° C
Junction temperature ..... +150° C
Soldering temperature ..... (5 seconds, 1/4" from pin) ..+260° C
Vapor phase soldering (1 minute) ..... +220° C
Voltage on any digital pin ..... GND -0.5V to V_{DD} + 0.5V
Analog output short circuit duration to any power supply or common ..... Indefinite
Power supply voltage (V_{DD} measured to GND) 7V

NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Units
V_{DD}	Power Supply Voltage	4.75	5.00	5.25	Volts
T_A	Ambient Operating Temperature	0		70	°C
R_L	Output Load		37.5		Ohms
I_{REF}	Current Reference (RS-343A)	-3	-8.39	-10	mA
I_{REF}	Current Reference (PS/2-compatible)	-3	-8.88	-10	mA

7.3 DC Specifications (Digital)

(V_{DD} = 5V ± 5%, T_A = 0 to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	TYP	MAX	Units	Test Conditions
V_{DD}	Power Supply Voltage	4.75	5.00	5.25	Volts	Normal Operation
V_{IL}	Input Low Voltage	0		0.8	Volts	
V_{IH}	Input High Voltage	2.0		V_{DD} + 0.5	Volts	
V_{OL}	Output Low Voltage			0.4	Volts	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			Volts	I_{OH} = 400 µA
I_{DD}	V_{DD} Supply Current		180	220	mA	At FMAX, I_{DD} (TYP) at V_{DD} = 5.0V, I_{DD} (MAX) at V_{DD} = 5.25V
I_{IH}	Input High Current			1	µA	V_{in} = 2.4V
I_{IL}	Input Low Current			-1	µA	V_{in} = 0.4V
I_{OZ}	Input Leakage			50	µA	
C_{IN}	Input Capacitance			7	pF	(f = 1 MHz, V_{in} = 2.4V)
C_{OUT}	Output Capacitance			7	pF	

7.4 DC Specifications (Palette DAC)

Symbol	Parameter	MIN	TYP	MAX	Units
	Resolution (each DAC)	8	8	8	Bits
Accuracy (each DAC)					
IL	Integral Linearity Error			± 1.5	LSB
DL	Differential Linearity Error			± 1.5	LSB
	Grayscale Error			± 7	% Grayscale
	Monotonicity		guaranteed		
	Coding			Binary	

7.5 DC Specifications (Analog Standard RS-343A Compatibility)

(V_{DD} = 5V ± 5%, T_A = 0 to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	TYP	MAX	Units
	Grayscale Current Range			20	mA
Output Current (Standard RS-343A)					
	White Level Relative to Black	16.34	17.62	18.85	mA
	Black Level Relative to Blank	0	0	0	µA
	Blank Level	0	5	50	µA
	LSB Size		279.68		µA
	DAC-to-DAC Matching		2	5	%
V_{OC}	Output Compliance	-1.0		+1.5	V
RA_{OUT}	Output Impedance		10		KΩ
CA_{OUT}	Output Capacitance (f = 1 MHz, I_{OUT} = 0 mA)			30	pF
I_{VREF}	Voltage Reference Input Current		10		µA
PSRR	Power Supply Rejection Ratio		0.5	%/% delta	V_{AA}

NOTE: Test conditions to generate RS-343A-standard video signals (unless otherwise specified). Recommended operating conditions using external-voltage reference with RSET = 147Ω, VREF = 1.235V. For 28-pin DIP version of the CL-GD5200, IREF = -8.39 mA. The above parameters are guaranteed over the full-temperature range, and temperature coefficients are not specified or required.

7.6 DC Specifications (Analog PS/2 Compatibility)

(V_{DD} = 5V ± 5%, T_A = 0 to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	TYP	MAX	Units
Analog Outputs					
	White Level Relative to Black	17.34	18.65	19.96	mA
	Black Level Relative to Blank	0	5	50	µA
	Blank Level	0	5	50	µA

NOTE: Test conditions to generate PS/2-compatible video signals (unless otherwise specified). Recommended operating conditions using external-voltage reference with R_{SET} = 140Ω, V_{REF} = 1.235V.

7.7 List of Waveforms

Table 7–1. CPU Read/Write Timing

Symbol	Parameter	MIN	MAX	Units
t_1	RS0, RS1 Setup Time	10		ns
t_2	RS0, RS1 Hold Time	10		ns
t_3	RD* Asserted to Data Bus Driven	5		ns
t_4	RD* Asserted to Data Valid		40	ns
t_5	RD* Negated to Data Bus 3-state		20	ns
t_6	Read Data Hold Time	5		ns
t_7	Write Data Setup Time	10		ns
t_8	Write Data Hold Time	10		ns
t_9	RD*, WR* Pulse Width Low	50		ns
t_{10}	RD*, WR* Pulse Width High	5		CLOCKS

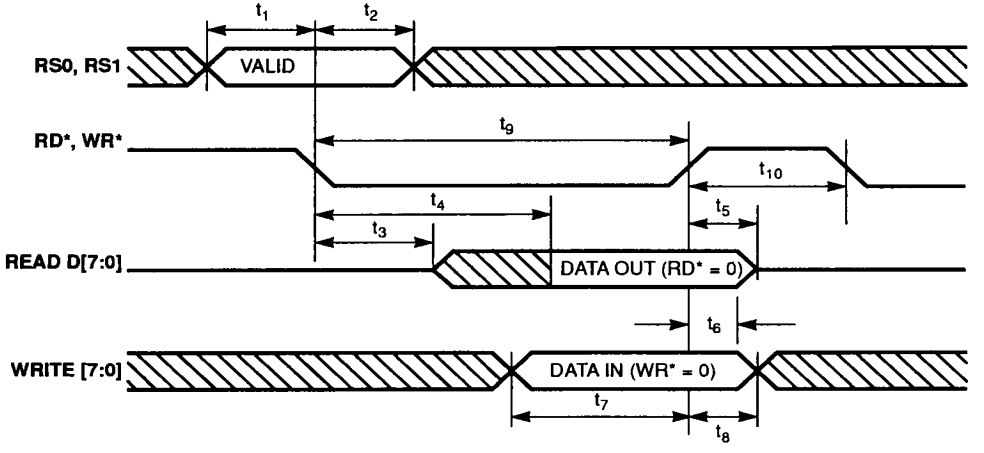


Figure 7–1. CPU Read/Write Timing

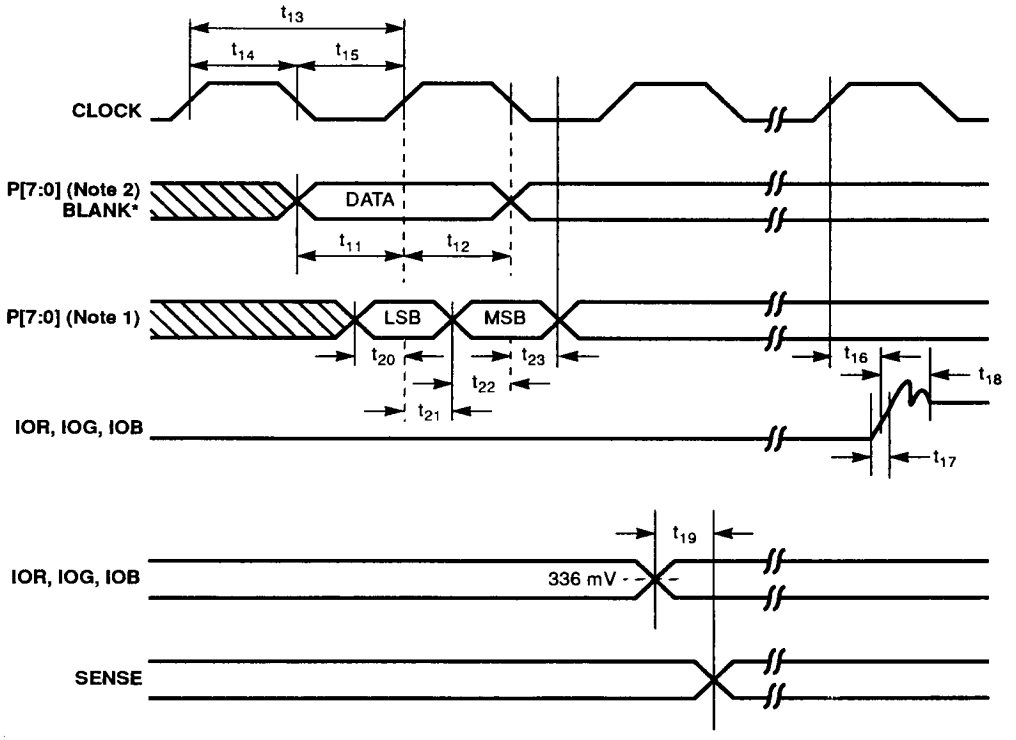
Table 7–2. Video Input/Output Timing

Symbol	Parameter	MIN	MAX	Units
t_{11}	Pixel and Control Setup Time Clock Mode 2	3		ns
t_{12}	Pixel and Control Hold Time Clock Mode 2	3		ns
t_{13}	Clock Cycle Time	12.5		ns
t_{13}	Clock Cycle Time Clocking Mode 1	25		ns
t_{14}	Clock Pulse Width High Time Clock Mode 2	4		ns
t_{14}	Clock Pulse Width High Time Clocking Mode 1	9		ns
t_{15}	Clock Pulse Width Low Time Clock Mode 2	4		ns
t_{15}	Clock Pulse Width Low Time Clocking Mode 1	9		ns
t_{16}	Analog Output Delay		30	ns
t_{17}	Analog Output Rise/Fall Time	6		ns
t_{18}	Analog Output Settling Time* Analog Output Skew	13	 2	ns ns
t_{19}	SENSE Output Delay	1		us
t_{20}	Pixel and Control Setup Time LSB Clocking Mode 1	0		ns
t_{21}	Pixel and Control Hold LSB Clocking Mode 1	3		ns
t_{22}	Pixel and Control Setup Time MSB Clocking Mode 1	0		ns
t_{23}	Pixel and Control Hold MSB Clocking Mode 1	3		ns

* Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1KΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch Impulse includes clock and data feedthrough; -3 dB test bandwidth = 2x clock rate.

TEST CONDITIONS

Recommended operating conditions using external-voltage reference with R_{SET} = 147Ω, V_{REF} = 1.235V. For the 28-pin DIP version, I_{REF} = -8.39 mA. TTL-input values are 0 to 3V, with input rise/fall times <= 2 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog-output load <= 10 pF, D[7:0] output load <= 50 F.



NOTES:
1) Clocking Mode 1
2) Clocking Mode 2

Figure 7–2. Video Input/Output Timing

Table 7–3. Pipeline Delay for PEL Data and Blanking Input to RGB Output — Clocking Mode 1

CL-GD5200 Mode	Pipeline Delay	Units
Compatible (Standard VGA)	NA	CLOCKS
Border Encoded	NA	CLOCKS
Compressed YUV	NA	CLOCKS
16-bit YUV	5	CLOCKS
5-5-5 and 5-6-5 RGB	3	CLOCKS
5-5-5 LUT Mixed Mode	3	CLOCKS
24-bit (8-8-8) RGB	NA	CLOCKS

NOTE: Clocking Mode 1 (data clocked on rising and falling edges of CLOCK) is used only for the 16-bit/PEL Modes.

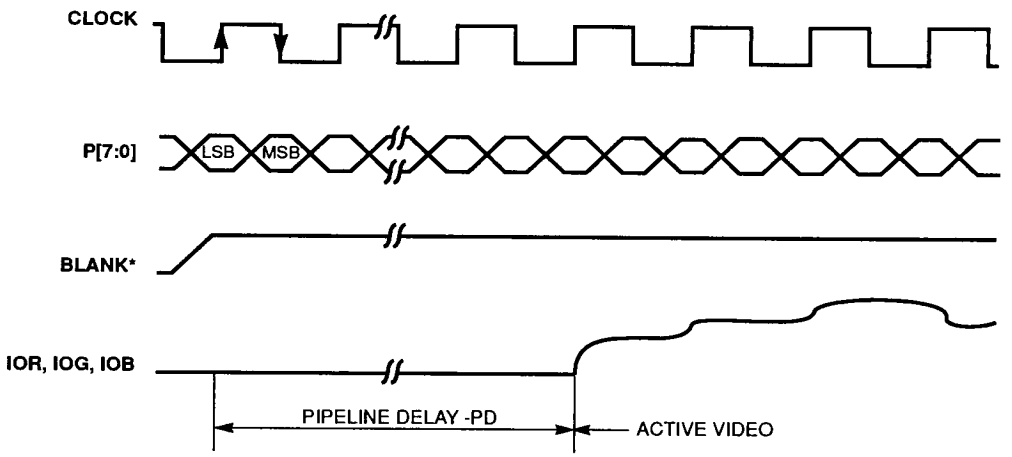


Figure 7–3. Clocking Mode 1 Timing

Table 7–4. Pipeline Delay for PEL Data and Blanking Input to RGB Output — Clocking Mode 2

CL-GD5200 Mode	Pipeline Delay	Units
Compatible (Standard VGA)	3	CLOCKS
Border Encoded	3	CLOCKS
Compressed YUV	7	CLOCKS
16-bit YUV	10	CLOCKS
5-5-5 and 5-6-5 RGB	6	CLOCKS
5-5-5 LUT Mixed Mode	6	CLOCKS
24-bit (8-8-8) RGB	9	CLOCKS

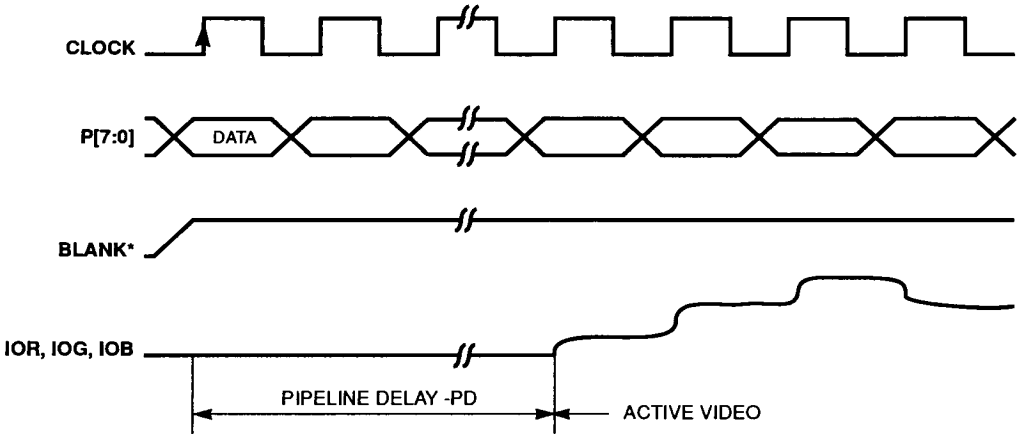


Figure 7–4. Clocking Mode 2 Timing

8. PC BOARD LAYOUT CONSIDERATIONS

8.1 PC Board Considerations

Layout should be optimized for low noise on the CL-GD5200 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{DD} and GND pins should be minimized to minimize inductive ringing.

8.2 Ground Planes

The Ground Plane should encompass all CL-GD5200 Ground Pins, current/voltage-reference circuitry, power supply bypass circuitry for the CL-GD5200, the analog-output traces, and all the digital-signal traces leading to the CL-GD5200.

8.3 Power Planes

The CL-GD5200 and any associated analog circuitry should have its own power plane, referred to as the Analog-power Plane. This power plane should be connected to the regular PCB Power Plane at a single point through a ferrite bead, as illustrated in Figures 8–1, 8–2, and 8–3. This bead should be located within three inches of the CL-GD5200.

The PCB Power Plane should provide power to all digital logic on the PC board, and the Analog-power Plane should provide power to all CL-GD5200 Power Pins and current/voltage-reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB Power and Ground Planes do not overlay portions of the Analog-power Plane, unless they can be arranged such that the plane-to-plane noise is common mode.

8.4 Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

Best performance is obtained with a 0.1-µF ceramic capacitor decoupling each of the two groups of V_{DD} Pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note while the CL-GD5200 contains circuitry to reject power-supply noise, this rejection decreases with frequency. If a high-frequency switching power supply is used, the designer should pay close attention to reducing power-supply noise, and consider using a three-terminal voltage regulator for supplying power to the Analog-power Plane.

8.5 Digital Signal Interconnect

Digital inputs to the CL-GD5200 should be isolated as much as possible from analog outputs and other analog circuitry. Also, these input signals should not overlay the Analog-power Plane.

Due to the high clock rates involved, long clock lines to the CL-GD5200 should be avoided to reduce noise pickup.

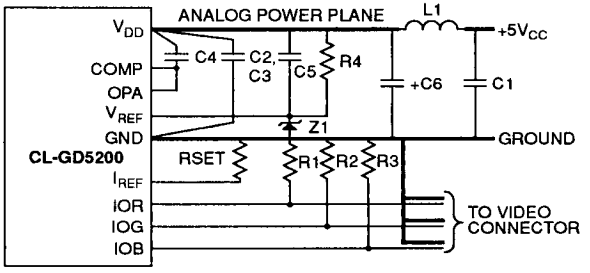
Any active termination resistors for digital inputs should be connected to the regular PCB power plane, and not the Analog-power Plane.

8.6 Analog Signal Interconnect

The CL-GD5200 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The Video Output Signals should overlay the Ground Plane, not the Analog-power Plane, to maximize the high-frequency power supply rejection.

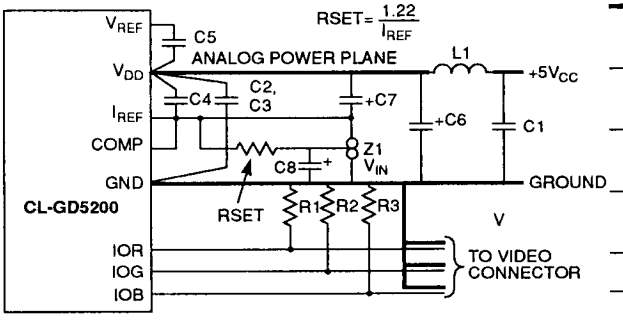
For maximum performance, analog outputs should each have a 75Ω load resistor connected to GND. The connection between the current output and GND should be as close as possible to the CL-GD5200 to minimize reflections.



Location	Description
C1–C5	0.1-µF Ceramic Capacitor (Erie® RPE112Z5U104M50V)
C6	10-µF Tantalum Capacitor (Mallory® CSR13G106KM)
L1	Ferrite Bead (Fair-Rite® 2743001111)
R1, R2, R3	75Ω 1% Metal Film Resistor (Dale® CMF-55C)
RSET	1% Metal Film Resistor (Dale CMF-55C)
Z1	1.2V Voltage Reference (National Semiconductor® LM385BZ-1.2)
R4	1KΩ 5% Resistor

NOTE:
Vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the CL-GD5200.

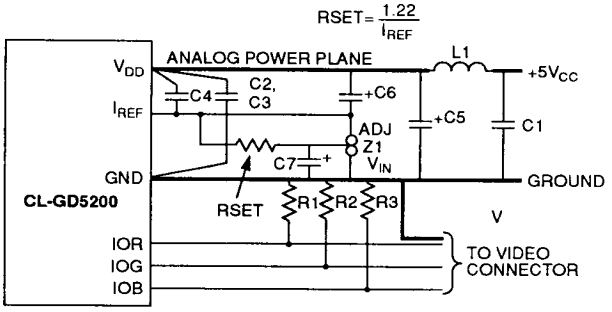
Figure 8–1. Typical CL-GD5200 Connection Diagram and Parts List (External Voltage Reference)



Location	Description
C1–C4	0.1-µF Ceramic Capacitor (Erie RPE112Z5U104M50V)
C5	10-µF Tantalum Capacitor (Mallory CSR13G106KM)
C6	47-µF Tantalum Capacitor (Mallory CSR13F476KM)
C7	1-µF Capacitor (Mallory CSR13G105KM)
L1	Ferrite Bead (Fair-Rite 2743001111)
Z1	Adjustable Regulator (National Semiconductor LM337LZ)
R1, R2, R3	75Ω 1% Metal Film Resistor (Dale CMF-55C)
RSET	1% Metal Film Resistor (Dale CMF-55C)

NOTE:
Vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the CL-GD5200.

Figure 8–2. Typical CL-GD5200 Connection Diagram and Parts List (External Current Reference for 44-Pin PLCC)

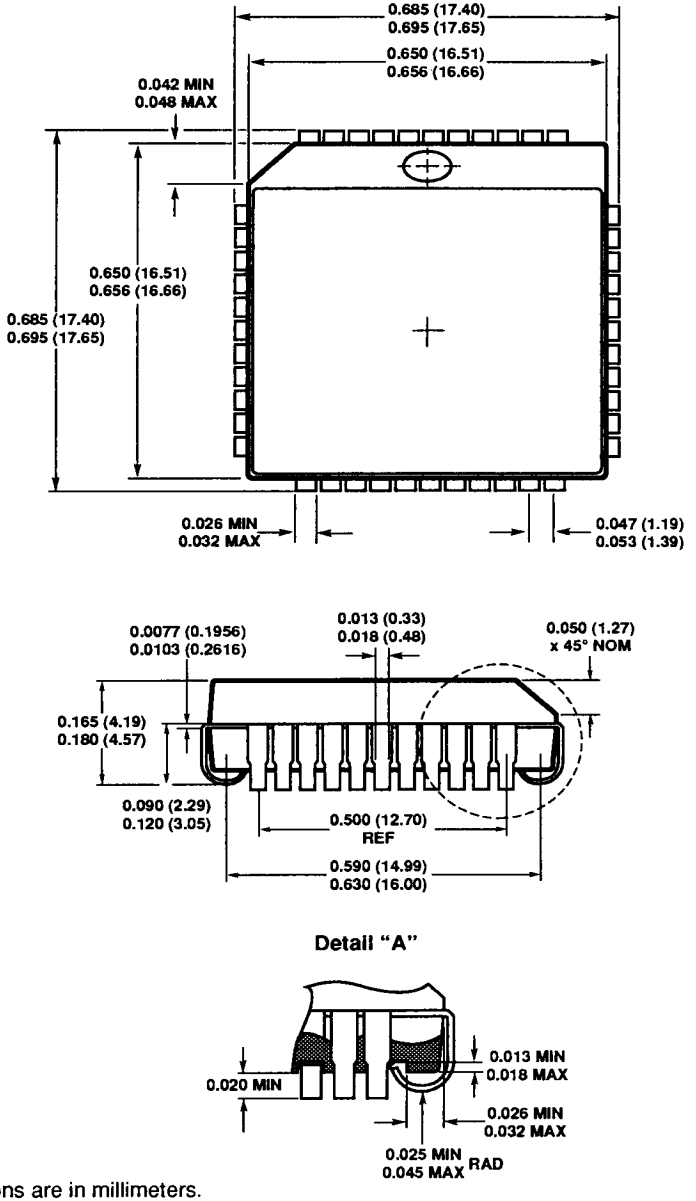


NOTE:
Vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the CL-GD5200.

Location	Description
C1–C4	0.1-µF Ceramic Capacitor (Erie RPE112Z5U104M50V)
C5	10-µF Tantalum Capacitor (Mallory CSR13G106KM)
C6	47-µF Tantalum Capacitor (Mallory CSR13F476KM)
C7	1-µF Capacitor (Mallory CSR13G105KM)
L1	Ferrite Bead (Fair-Rite 2743001111)
R1, R2, R3	75Ω 1% Metal Film Resistor (Dale CMF-55C)
RSET	1% Metal Film Resistor (Dale CMF-55C)
Z1	Adjustable Regulator (National Semiconductor LM337LZ)

Figure 8–3. Typical CL-GD5200 Connection Diagram and Parts List (External Current Reference for 28-Pin DIP)

9. SAMPLE PACKAGE DIMENSIONS

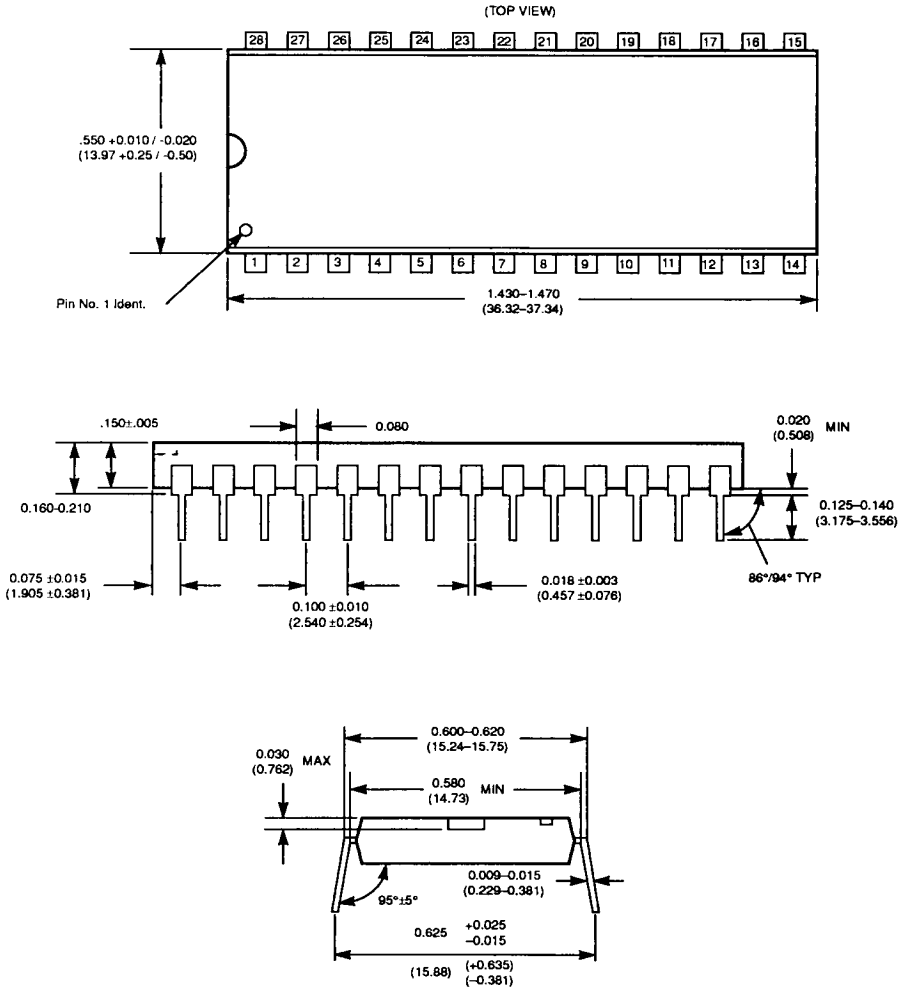


NOTE: The dimensions are in millimeters.

345200-1

Figure 9–1. CL-GD5200 44-Pin PLCC Dimensions

9. SAMPLE PACKAGE DIMENSIONS *(cont.)*

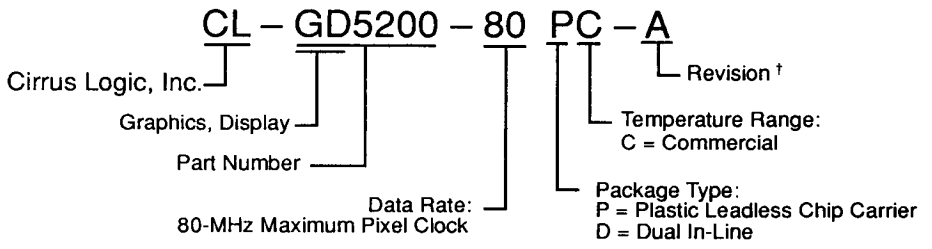


NOTE: The dimensions are in millimeters.

Figure 9–2. CL-GD5200 28-Pin DIP

10. ORDERING INFORMATION

10.1 Package Marking Numbering Guide



† Contact Cirrus Logic, Inc. for up-to-date information on revisions.

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