Pentium II Integrated 3D Graphics Chipset

SiS 620

Preliminary

Rev. 1.0

January 15, 1999

CONTENTS

FIGURES

TABLES

1. SiS620/SiS5595 OVERVIEW

The SiS620 integrates the high performance host bus interface, the DRAM controller, the IDE controller, the PCI interface, 2D/3D Graphics accelerator and video playback accelerator.

The DRAM controller supports 3-DIMM/6-Bank of 3.3V SDRAM. The maximum memory size supported per bank is 256MB, with a total of 1.5GB system memory. The memory clock frequency can be operated at up to 100MHz and can be in synchronous or asynchronous modes with respect to host bus frequency. The supported host/DRAM clock schemes include 100/100, 83/83, 75/75, 66/66, 100/75, 100/66, 83/66, 66/83 and 66/100. For power saving, the SDRAM can be put into suspend mode.

The IDE controller is ATA-3 compliant, supporting PIO mode 0/1/2/3/4, DMA multiword 0/1/2 and Ultra DMA 33/66 operations. The two IDE channels are fully independent with dedicated 16 double-word FIFO built-in.

The PCI interface is PCI2.2 compliant and supports up to 4 PCI masters. The built-in PCI arbiter uses rotating priority arbitration scheme with guaranteed minimum access time for PCI masters, providing fair access as well as low latency for each PCI masters.

The integrated 2D accelerator is a 64-bit BITBLT graphics engine. It supports all 256 raster operations and DirectDraw. The accelerated primitives include BLT, Transparent BLT, Color expansion, Clipping, Multiple scanline, Polylines, Patterns, Trapezoid Fills. Up to 8MB of frame buffer can be used with linear addressing.

The integrated 3D graphics accelerator is composed of the triangle setup engine and the rendering engine. The hardware acceleration features can be enabled by SiS driver under Direct 3D and OpenGL. The supported 3D-quality acceleration includes Gouroud Shading, Z buffer, Alpha buffer, Perspective Correction, MipMaping, Tri-linear Texture Filtering, Specular Lighting and Dithering.

The integrated graphics accelerator is compatible with AGP1.0 and PCI2.2 configuration. SiS620 provides two options –UMA and Non-UMA modes for display memory allocation. In UMA mode, the display memory is shared with system memory. In Non-UMA mode, the display memory can be up to 8MB SDRAM or SGRAM.

In UMA mode operation, the integrated graphics accelerator uses up to 8MB of system memory as display memory, thereby saving the on-board DRAM cost for building a PC system. To reduce the performance degradation inherent from the UMA architecture, SiS620 has included the super-AGP architecture, which consists of dual 64bits data path. One data path is between VGA and host bus, the other is between VGA and system memory. Both data paths are operating at 100MHz and provide 800MB/s bandwidth. The internal arbitration logic further allows concurrent transactions to take place in different data paths. As a result, the overall system performance can be maintained at a reasonable high level while maximum cost saving is achieved.

In non-UMA mode, on-board SDRAM or SGRAM (up to 8MB) will be used as display memory. This gives system designers an option to achieve maximum system performance. The super-AGP architecture provides 800MB/s bandwidth between VGA and host bus, which is 50% more than the AGP 2X mode(532MB/s). The display memory interface bus frequency can also be operated at up to 100MHz, with 64-bit or 32-bit data path(the 32-bit

data path configuration gives the designer a low-cost solution). In summary, SiS620 provides consistent 800MB/s bandwidth among internal module as well as external memory interfaces, and delivers high performance in 2D and 3D applications.

For flat panel display support, SiS620 provides external LVDS/TMDS controller interface. This interface shares the pins with display memory data bus[63:32], therefore, the flat panel function is available only in UMA mode or in 32-bit non-UMA mode.

The SiS5595 PCI system I/O integrates the PCI-to-ISA bridge, KBC, USB, RTC, SMBUS, ACPI/APM compatible PMU, system environment monitoring for thermal, fan, voltage as well as comprehensive PCI audio support including DDMA, TDMA and SB-Link.

1.1. SiS620/SiS5595 SYSTEM BLOCK DIAGRAM

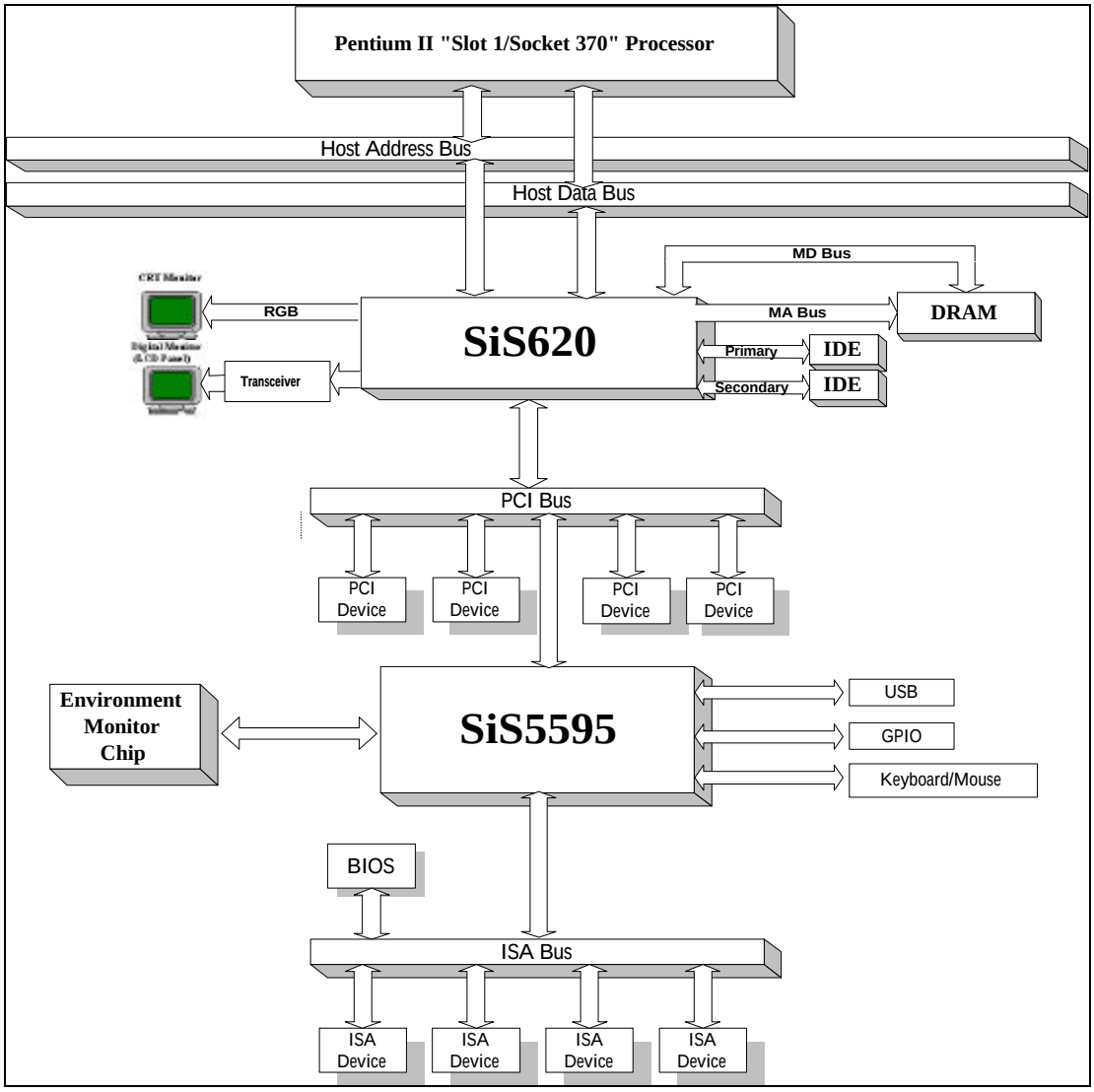


Figure 1.1-1 SiS620 System Block Diagram

1.2. SiS620 FUNCTIONAL BLOCK DIAGRAM FEATURE

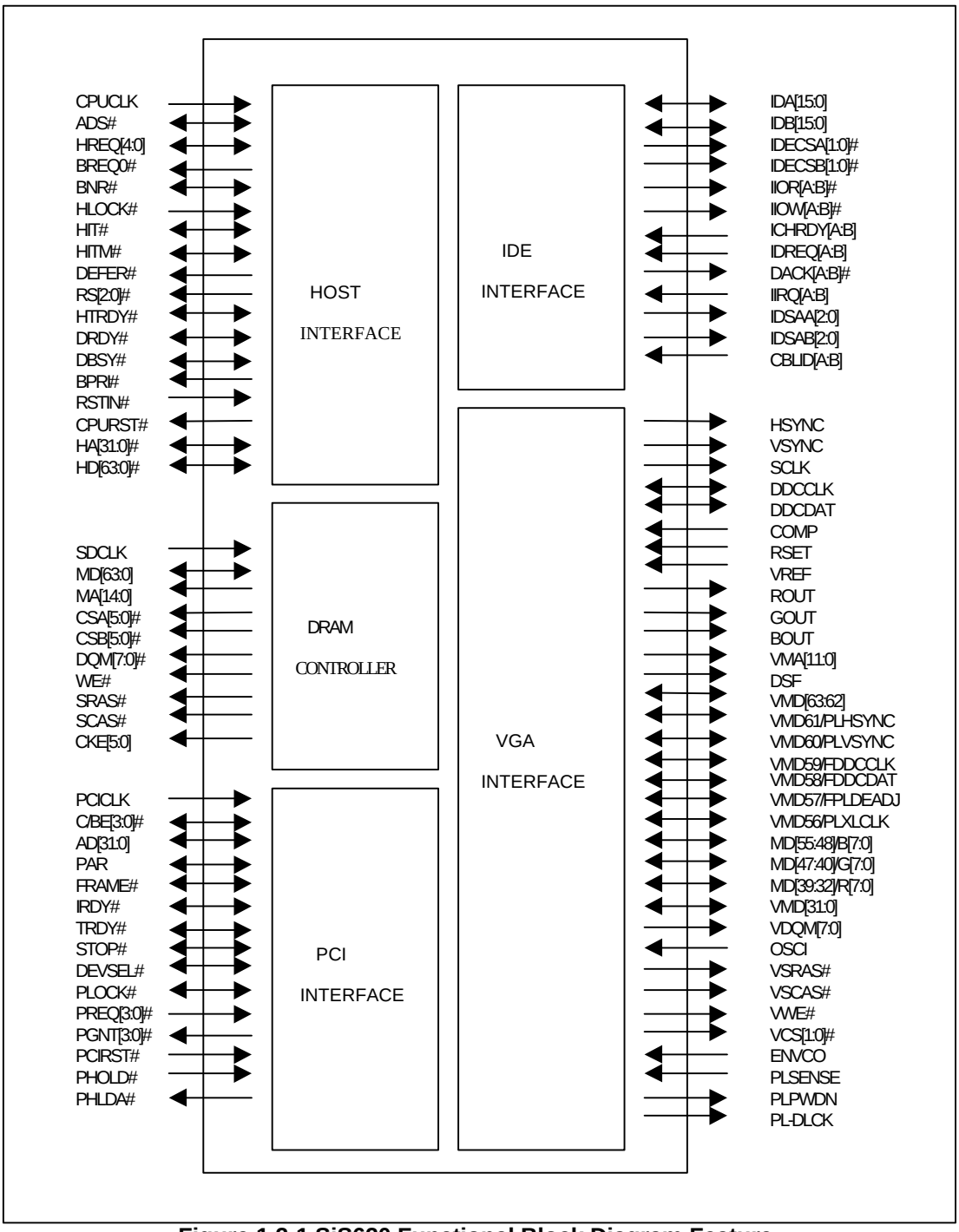


Figure 1.2-1 SiS620 Functional Block Diagram Feature

2. FEATURE

2.1. INTEGRATED HOST/DRAM/PCI/IDE CONTROLLER

Supports Intel Pentium II CPU at 66M/100MHz Front Side Bus Frequency

- Synchronous Host/DRAM Clock Scheme:100/100, 83/83, 75/75, 66/66 MHz
- Asynchronous Host/DRAM Clock Scheme: 100/75 ,100/66 , 83/66, 66/83, 66/100MHz

Integrated DRAM Controller

- 3-DIMM/6-Bank of 3.3VSDRAM
- System Memory Size up to 1.5GB
- Up to 256MB per Row
- Support 16Mb, 64Mb, 128Mb, 256Mb SDRAM technology
- Suspend-To-RAM (STR)
- Relocatable System Management Memory Region
- Programmable Buffer Strength for RAMWE#, SDRAS#, SDCAS#, CKE, MA[14:0]
- Shadow RAM size from 640KB To 1MB in 16KB increments
- 8-1-1-1(-1-1-1-1) Burst Read Cycles
- 2-2-2-2 Back-To-Back Single QW Read Cycles
- X-1-1-1/X-2-2-2 Burst Write Cycles
- Two Programmable PCI Hole Areas

A.G.P. Revision 2.0 Specification Compliant

- Built-in 8-Way/16-Entry set-associative GART Cache for AGP master

Meet PC99 Requirements

PCI 2.2 Specification Compliant

High Performance PCI Arbiter

- Support 4 PCI Masters
- Rotating Priority Arbitration Scheme
- Advanced Arbitration Scheme Minimizing Arbitration Overhead.
- Host-To-Memory and PCI-To-PCI Concurrent Transactions
- Guaranteed minimum access time for CPU and PCI masters

Integrated Host-To-PCI Bridge

- Zero Wait State Burst Cycles
- CPU-To-PCI Pipeline Access
- 256B to 4KB PCI Burst Length For PCI Masters

- PCI Master Initiated Graphical Texture Write Cycles Remapping
- Reassembles PCI Burst Data Size Into Optimized Block Size

Fast PCI IDE Master/Slave Controller

- Support PCI Bus Mastering
- Native Mode and Compatibility Mode
- PIO Mode 0, 1, 2 , 3, 4
- Multiword DMA Mode 0, 1, 2
- Ultra DMA 33/66
- Two Independent IDE Channels each with 16 DW FIFO

Integrated Post Write Data Buffers And Read Prefetch Data Buffers

- 8 QW Of Host-To-Memory Write Buffer
- 8 QW Of Host-To-Memory Read Buffer
- 16 QW Of Host-To-PCI Or Host-To-GUI PCI-to-Host Read Prefetch Multi-Purpose Write Buffer (MPWB)
- 4 DW Of Host-To-PCI Dedicated Write Data Buffer (Cascade With Multi-Purpose Write FIFO)
- 16 QW Of PCI-To-Host Post Write Buffer
- 4 DW PCI-To-Host Read Prefetch Data Buffer (Cascaded With MPWB)

Supports The Following Concurrent Transactions

- Host-To-Memory Read/Write and PCI-To-PCI Read/Write
- Host-To-Memory Read/Write and PCI-To-Memory Read/Write
- Host-To-Memory Read/Write and GUI-To-Memory Read/Write
- Host-To-Memory Read/Write and PCI-To-GUI Write
- Host-To-PCI Read/Write and GUI-To-Memory Read/Write
- Host-To-PCI Write and PCI-To-Memory Write
- Host-To-GUI and GUI-To-Memory Write
- PCI-To-GUI Write and GUI-To-Memory Write

Virtual PCI-to-PCI Bridge

Super-AGP Architecture

- 3D Engine Fetch Texture Data at Up to 800MB/s
- Dual 64-bit Data Bus Architecture

  64-Bit Data Path between GUI and System Memory at up to 100MHz

64-Bit Data Path between GUI and Host at up to 100MHz

2.2. 2D/3D GRAPHICS AND VIDEO ACCELERATOR

Host & System Memory Interface

- AGP/PCI Configuration Space Compliant
- Relocatable Memory Mapped IO Address
- Relocatable Linear Frame Buffer Address
- High Performance Host-To-GUI Command Transfer
- Non-UMA Mode Achieves Optimum 2D/3D Performance
- UMA Mode Requires No External Display Memory For Cost-Saving
- Integrated 64x8 Host-to-GUI Post Write Buffer And 64x8 GUI-to-Host Read Cache
- 2M/4M/8M Frame Buffer Located In System Memory (UMA Mode)

3D Graphics Accelerator

- 3D Engine For High Performance

  32-Bit Floating Point Format VLIW Triangle Setup Engine

  16K-Bit Texture Cache

- 3D Engine For High Quality

  Supports Solid, Flat, Gouraud Shading

  High Quality Dithering

  Z-Test, Alpha-Test and Scissors Clipping Test

  Line, Pattern and ROP

  Z-Buffer and Alpha Buffer

  Per-Pixel Texture Perspective Correction

  Nearest, Linear, Bi-Linear and Tri-Linear Texture Filtering

  MIP Structure Texture

  Rectangle Structure Texture

  1/2/4 Bpp Palletized Texture

  1/2/4/8 Bpp Luminance Texture

  8/16/24/32 Bpp RGB/ARGB Texture Format

  Video Texture in RGB555, RGB565 And YUV422 Formats

  Texture Transparency, Blending, Wrapping, Mirror and Clamping

  Fogging and Alpha Blending

  Specular Lighting

2D Graphics Accelerator

- 42 DW Hardware Command Queue
- Turbo Queue achieves extra-High Performance
- Direct Draw Accelerator
- 64 bits Programmable Stride Graphic Engine with:
  - 256 Raster Operation
  - Rectangle Fill
  - Color Expansion
  - Enhanced Color Expansion
  - Line-Drawing With Stylish Patterns
  - NT Fractional Format Line Drawing
  - Multiple Scan Line Drawing
  - Trapezoid Fill
  - 8x8 Pattern Registers
  - 8x8 Mask Registers
  - Rectangle Clipping
  - Transparent BITBLT
- Memory-Mapped, Zero Wait-State, Burst Engine Write
- Burst Frame Buffer Reads And Writes For SDRAM/SGRAM
- Supports 64x64x2 bit-mapped Hardware Cursor
- Supports up to 8MB Frame Buffer With Linear Addressing
- 6-Stage Engine Write Buffer And 9x64-Bit Read Buffer
- 64x64 CRT FIFO To Support High Resolution Graphic Modes

Video Accelerator

- Supports Single Frame Buffer Architecture
- Supports YUV-To-RGB Color Space Conversion
- Supports Bi-Linear Video Interpolation With Integer Increments Of 1/64
- Supports Graphic And Video Overlay Function
  - Independent Graphic And Video Format
  - 16 Color-Key And/Or Chroma-Key Operation
  - Rectangular Video Window Modes
- Current Scan-Line Of Refresh Read-Back

- Tearing Free Double Buffering
- RGB555, RGB565, YUV422, And YUV420 Video Format
- Two 96x64 Video Playback Line Buffers
- DDA-Based Bi-linear Video Scaling Algorithm
- Supports DCI Drivers
- Supports Direct Draw Drivers
- Supports S/W MPEG-I And MPEG-II Video Playback

Display Memory Interface (Non-UMA Mode)

- 2MB/4MB/8MB SGRAM
- 2MB/4MB/8MB SDRAM
- 256Kx32, 512Kx32, 1Mx32 SGRAM or 1Mx16 SDRAM
- SGRAM Block Write
- Automatic Memory Type And Size Detection
- SO-DIMM Interface Compliant
- Maximum 100MHz Memory Clock Frequency
- 32-/64-Bit Display Memory Path
- UMA Mode Allows 2M/4M/8M of System Memory Used as Frame Buffer

High Integration

- Programmable 24-Bit True-Color 230MHz RAMDAC
  - Reference Voltage Generator And Monitor Sense Circuit
  - Loadable RAMDAC For Gamma Correction In High/True Color Modes
- Dual-Clock Generator
  - Integrates PLL Loop Filter
- PCI Multimedia Interface

Resolution

- Supports Super High Resolution Graphic Modes

640x480	8/16/32 Bpp Colors @85Hz NI
800x600	8/16/32 Bpp Colors @85Hz NI
1024x768	8/16/32 Bpp Colors @85Hz NI
1280x1024	8/16/32* Bpp Colors @85Hz NI (*Not Support In UMA Mode)
1600x1200	8/16* Bpp Colors @85Hz NI (* Not Support In UMA Mode)

- Support Virtual Screen up To 2048x2048

– Support 80-Column and 132-Column Text Modes

Digital Flat Panel Port

– Provides TMDS/LVDS Controller interface

– Supports TFT-24bit, TFT-18bit, TFT-12bit LCD Monitor

– DDC2B (VESA DDC 3.0) Display Configuration and Detection

– VESA DMPS Power Management

– Compliant with VESA EDID 3.0 Standard

– Supports Screen Centering

– VESA Plug and Display (P&D) 1.0 Standard Hot Plugging

– Up to 1024x768@75Hz (VESA standard CRT timings)

– Supports 85MHz pixel clock for 1280x1024 flat panel display by using the reduced refresh

rate timing

Power Management

– Supports VESA DPMS Compliant VGA Monitor

– 30-Minute Standby/Suspend Timers Triggered By Keyboard, HW Cursor, Video Memory

Access Events

– Standby/Suspend/Off States Can Be Activated Immediately By I/O Command

– Power-Down Internal SRAM In Direct Color Mode

Multimedia Application

– Supports DDC1 And DDC2B Specifications

Miscellaneous

– Optionally Disable the Integrated VGA Controller by a Hardware Trap Pin

– Supports Signature Analysis For Automatic Testing

– Implemented By 3.3V CMOS Technology With 5.0V Tolerance I/O Buffers

Supports NAND Tree For Ball Connectivity Testing

576 Balls BGA Package

3.3V CMOS Technology

3. PIN ASSIGNMENT

3.1. SiS620 PIN ASSIGNMENT(TOP VIEW)

3.1.1. SiS620 PIN ASSIGNMENT(TOP VIEW-LEFT SIDE)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A			AVDD1	AVDD 2/3	ROUT	BOUT	AVSS4	AD4	AD8	AD13	PAR	FRAME#	AD19	C/BE3#	AD25
B		ENVCO	DDCCLK	AVSS 2/3	AVDD4	GOUT	RSET	AD3	C/BE0#	AD12	C/BE1#	IRDY#	AD18	AD23	AD27
C	VMD63	PLPWDN	DDCDATA	VSYNC	N.C.	N.C.	VREF	AD2	AD6	AD11	AD15	TRDY#	AD16	AD22	AD28
D	PL-DCLK	VMD60	VMD62	HSYNC	N.C.	N.C.	N.C.	AD0	AD7	AD9	STOP#	PLOCK#	C/BE2#	AD20	AD29
E	VCS1#	VMD56	VMD57	VMD59	OSCI	AVSS1	COMP	AD1	AD5	AD10	AD14	DEVSEL#	AD21	AD26	N.C.
F	VMD55	VDQM4	VDQM6	VDQM7	PLSENSE								AD17	AD24	N.C.
G	VMD50	VMD51	VMD52	VMD54	VMD61										
H	VMD44	VMD46	VMD47	VMD48	VMD58										
J	VMD40	VMD42	VMD43	VMD53	VDQM5										
K	VMD35	VMD36	VMD38	VMD39	VMD49						OVDD3	DVDD	OVDD3	DVDD	OVDD3
L	SCLK	VMD32	VMD34	VMD41	VMD45					OVDD3					
M	VMA8	VMA9	VMA10	DSF	VMD37					DVDD		VSS	VSS	VSS	VSS
N	VMA3	VMA4	VMA6	VMA7	VMA11	VMD33				OVDD3		VSS	VSS	VSS	VSS
P	VSRAS#	VCS0#	VMA0	VMA2	VMA1	VMA5				DVDD		VSS	VSS	VSS	VSS
R	VMD29	VMD30	VWE#	VSCAS#	N.C.	N.C.				OVDD3		VSS	VSS	VSS	VSS
T	VMD28	VMD27	VMD26	VMD25	VMD31	VDQM3				DVDD		VSS	VSS	VSS	VSS
U	VMD24	VDQM2	VDQM0	VMD23	VDQM1	VMD21				OVDD3		VSS	VSS	VSS	VSS
V	VMD22	VMD20	VMD19	VMD18	VMD17					DVDD		VSS	VSS	VSS	VSS
W	VMD16	VMD15	VMD14	VMD13	VMD9					OVDD3					
Y	VMD12	VMD11	VMD10	VMD8	VMD5					OVDD3	OVDD3	DVDD	OVDD3	DVDD	OVDD3
AA	VMD7	VMD6	VMD4	VMD1	IRQ15										
AB	VMD3	VMD2	VMD0	INTA#	IDA10	**ver 1.0**									
AC	IRQ14	IDA7	IDA8	IDA6	IDA12										
AD	IDA9	IDA5	IDA4	IDA11	IDA14								MD34	MD38	N.C.
AE	IDA3	IDA2	IDA13	IDA1	5VDD	IDSAA1	IDECSA0#	IDB6	IDB4	AVSS	IDACKB#	MD32	MD36	MD40	N.C.
AF	IDA0	IDA15	IDREQA	IIOWA	CBLIDA	IDB9	IDB3	IDB1	IDB0	IDREQB	IIRQB	IDECSB0#	MD1	MD4	MD39
AG	AVDD	PCICLK	AVSS	IIRQA	IDECSA1#	IDB5	IDB12	IDB14	IIOWB	IIORB	IDSAB0	IDECSB1#	MD2	MD37	MD7
AH		IIORA	ICHRDYA	IDSAA0	IDB7	IDB10	IDB2	IDB15	TEST#	ICHRDYB	IDSAB2	MD0	MD35	MD5	MD8
AJ			IDACKA#	IDSAA2	IDB8	IDB11	IDB13	SDCLK	AVDD	IDSAB1	CBLIDB	MD33	MD3	MD6	MD41
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

3.1.2. SiS620 PIN ASSIGNMENT(TOP VIEW-RIGHT SIDE)

16	17	18	19	20	21	22	23	24	25	26	27	28	29	
AVDD	CPUCLK	PREQ1#	PHLDA#	HD63#	HD53#	HD46#	HD41#	VTTB	HD40#	HD32#	HD31#			A
AD31	PGNT0#	PREQ3#	HD62#	HD55#	HD54#	HD48#	HD42#	VSSREFB	HD34#	HD35#	HD30#	HD26#		B
PGNT3#	PREQ2#	RSTIN	HD58#	HD56#	HD59#	HD49#	HD47#	GTLREFB	HD37#	HD28#	HD27#	HD25#	HD24#	C
PGNT2#	PCIRST#	BMREQ#	HD61#	HD50#	HD51#	HD52#	HD44#	HD36#	HD38#	HD23#	HD19#	HD21#	HD16#	D
AD30	AVSS	PHOLD#	HD60#	HD57#	HD45#	HD39#	HD43#	HD33#	HD29#	HD20#	HD13#	HD11#	HD15#	E
PGNT1#	PREQ0#								HD22#	HD10#	HD12#	HD14#	HD9#	F
									HD18#	HD6#	HD8#	HD4#	HD5#	G
									HD17#	HD2#	HD0#	HD1#	CPURST#	H
									HD7#	N.C.	HA29#	HA30#	HA26#	J
DVDD	OVDD3	DVDD	OVDD3	OVDD3					HD3#	HA31#	HA24#	HA27#	HA28#	K
				OVDD3					BREQ0#	N.C.	HA22#	HA23#	HA21#	L
VSS	VSS	VSS		DVDD					HA20#	HA25#	HA19#	HA18#	HA17#	M
VSS	VSS	VSS		OVDD3				N.C.	HA15#	HA16#	HA11#	HA13#	HA14#	N
VSS	VSS	VSS		DVDD				N.C.	HA12#	HA8#	HA10#	HA7#	VTTA	P
VSS	VSS	VSS		OVDD3				N.C.	N.C.	HA9#	HA5#	GTLREFA	VSSREFA	R
VSS	VSS	VSS		DVDD				N.C.	HA3#	BPRI#	BNR#	HA4#	HA6#	T
VSS	VSS	VSS		OVDD3				N.C.	HREQ0#	DEFER#	HREQ4#	HTRDY#	HREQ1#	U
VSS	VSS	VSS		DVDD					N.C.	HREQ3#	DRDY#	HREQ2#	HLOCK#	V
				OVDD3					RS1#	N.C.	HIT#	HITM#	RS0#	W
DVDD	OVDD3	DVDD	OVDD3	OVDD3					MD30	MD31	ADS#	RS2#	DBSY#	Y
									MD26	MD28	MD29	MD62	MD63	AA
									MD23	MD59	MD27	MD60	MD61	AB
									N.C.	MD24	MD57	MD25	MD58	AC
MD44	DQM4								N.C.	MD54	MD22	MD55	MD56	AD
MD42	MD46	SRAS#	MA3	MA7	CSB3#	DQM7	CKE5	CKE1	MD49	MD52	MD20	MD53	MD21	AE
MD11	MD14	WE#	CSA2#	CSA1#	MA11	MA6	MA12	CSB4#	DQM6	CKE4	MD18	MD51	MD19	AF
MD43	MD13	SCAS#	DQM1	CSA3#	MA1	MA5	MA10	CSB5#	CSB0#	DQM3	CKE2	MD17	MD50	AG
MD10	MD45	MD15	DQM5	CSA4#	MA0	MA4	MA9	MA14	CSB1#	DQM2	CKE3	CKE0		AH
MD9	MD12	MD47	DQM0	CSA5#	CSA0#	MA2	MA8	MA13	CSB2#	MD48	MD16			AJ
16	17	18	19	20	21	22	23	24	25	26	27	28	29	

3.2. ALPHABETICAL PIN LIST

SIGNAL NAME	SiS620 BALL NO
ENVCO	B2
PLSENSE	F5
PLPWDN	C2
VMD63	C1
VMD62	D3
VMD61	G5
VMD60	D2
OVDD	
PL-DCLK	D1
OVSS	
VMD59	E4
VMD58	H5
VMD57	E3
VMD56	E2
VCS1#	E1
VDQM7	F4
VDQM6	F3
VDQM5	J5
VDQM4	F2
OVDD	
VMD55	F1
OVSS	
VMD54	G4
VMD53	J4
VMD52	G3
VMD51	G2
VMD50	G1
VMD49	K5

SIGNAL NAME	SiS620 BALL NO
VMD48	H4
DVDD	
VMD47	H3
DVSS	
VMD46	H2
VMD45	L5
VMD44	H1
OVDD	
VMD43	J3
OVSS	
VMD42	J2
VMD41	L4
VMD40	J1
VMD39	K4
VMD38	K3
VMD37	M5
VMD36	K2
VMD35	K1
VMD34	L3
VMD33	N6
VMD32	L2
OVDD	
SCLK	L1
OVSS	
DSF	M4
VMA11	N5
VMA10	M3
VMA9	M2

SIGNAL NAME	SiS620 BALL NO
VMA8	M1
VMA7	N4
VMA6	N3
VMA5	P6
VMA4	N2
OVDD	
VMA3	N1
OVSS	
VMA2	P4
VMA1	P5
VMA0	P3
VCS0#	P2
VSRAS#	P1
VSCAS#	R4
VWE#	R3
VMD31	T5
VMD30	R2
OVDD	
VMD29	R1
OVSS	
VMD28	T1
DVSS	
VMD27	T2
DVDD	
VMD26	T3
DVDD	
VMD25	T4
DVSS	

SIGNAL NAME	SiS620 BALL NO
VMD24	U1
VDQM3	T6
VDQM2	U2
VDQM1	U5
VDQM0	U3
OVDD	
VMD23	U4
OVSS	
VMD22	V1
VMD21	U6
VMD20	V2
VMD19	V3
VMD18	V4
VMD17	V5
VMD16	W1
VMD15	W2
VMD14	W3
VMD13	W4
VMD12	Y1
OVDD	
VMD11	Y2
OVSS	
VMD10	Y3
VMD9	W5
VMD8	Y4
VMD7	AA1
VMD6	AA2
VMD5	Y5
VMD4	AA3

SIGNAL NAME	SiS620 BALL NO
OVDD	
VMD3	AB1
OVSS	
VMD2	AB2
VMD1	AA4
VMD0	AB3
INTA#	AB4
IRQ14	AC1
IRQ15	AA5
IDA7	AC2
IDA8	AC3
IDA6	AC4
OVDD	
IDA9	AD1
OVSS	
IDA5	AD2
IDA10	AB5
IDA4	AD3
DVSS	
IDA11	AD4
DVDD	
IDA3	AE1
IDA12	AC5
IDA2	AE2
IDA13	AE3
IDA1	AE4
IDA14	AD5
IDA0	AF1
IDA15	AF2

SIGNAL NAME	SiS620 BALL NO
IDREQA	AF3
OVDD	
IIOWA	AF4
OVSS	
PCICLK	AG2
AVDD	AG1
AVSS	AG3
5VDD	AE5
OVDD	
OVSS	
IIORA	AH2
ICHRDYA	AH3
IDACKA#	AJ3
IIRQA	AG4
IDSAA1	AE6
IDSAA0	AH4
IDSAA2	AJ4
CBLIDA	AF5
IDECSA0#	AE7
IDECSA1#	AG5
IDB7	AH5
IDB8	AJ5
IDB6	AE8
IDB9	AF6
IDB5	AG6
IDB10	AH6
IDB4	AE9
IDB11	AJ6

SIGNAL NAME	SiS620 BALL NO
IDB3	AF7
IDB12	AG7
IDB2	AH7
IDB13	AJ7
IDB1	AF8
IDB14	AG8
IDB0	AF9
IDB15	AH8
OVDD	
SDCLK	AJ8
OVSS	
IIOWB	AG9
TEST#	AH9
AVDD	AJ9
AVSS	AE10
IDREQB	AF10
DVDD	
IIORB	AG10
DVSS	
ICHRDYB	AH10
IDACKB#	AE11
IDSAB1	AJ10
IDSAB0	AG11
IDSAB2	AH11
IIRQB	AF11
CBLIDB	AJ11
OVDD	
IDECSB0#	AF12

SIGNAL NAME	SiS620 BALL NO
OVSS	
IDECSB1#	AG12
MD32	AE12
MD0	AH12
OVDD	
MD33	AJ12
OVSS	
MD1	AF13
MD34	AD13
MD2	AG13
OVDD	
MD35	AH13
OVSS	
MD3	AJ13
MD36	AE13
MD4	AF14
OVDD	
MD37	AG14
OVSS	
MD5	AH14
MD38	AD14
MD6	AJ14
OVDD	
MD39	AF15
OVSS	
MD7	AG15
MD40	AE14
MD8	AH15

SIGNAL NAME	SiS620 BALL NO
OVDD	
MD41	AJ15
OVSS	
MD9	AJ16
MD42	AE16
MD10	AH16
OVDD	
MD43	AG16
OVSS	
MD11	AF16
MD44	AD16
MD12	AJ17
OVDD	
MD45	AH17
OVSS	
MD13	AG17
MD46	AE17
MD14	AF17
OVDD	
MD47	AJ18
OVSS	
MD15	AH18
DVDD	
SCAS#	AG18
DVSS	
WE#	AF18
DQM4	AD17
DQM0	AJ19

SIGNAL NAME	SiS620 BALL NO
OVDD	
DQM5	AH19
OVSS	
DQM1	AG19
SRAS#	AE18
CSA5#	AJ20
CSA4#	AH20
CSA3#	AG20
CSA2#	AF19
CSA1#	AF20
OVDD	
CSA0#	AJ21
OVSS	
MA0	AH21
OVDD	
MA1	AG21
OVSS	
MA2	AJ22
MA3	AE19
MA4	AH22
OVDD	
MA5	AG22
OVSS	
MA6	AF22
MA7	AE20
MA8	AJ23
OVDD	
MA9	AH23

SIGNAL NAME	SiS620 BALL NO
OVSS	
MA10	AG23
MA11	AF21
MA12	AF23
OVDD	
MA13	AJ24
OVSS	
MA14	AH24
CSB5#	AG24
CSB4#	AF24
CSB3#	AE21
CSB2#	AJ25
DVDD	
CSB1#	AH25
DVSS	
CSB0#	AG25
OVDD	
DQM6	AF25
OVSS	
DQM2	AH26
DQM7	AE22
DQM3	AG26
CKE5	AE23
CKE4	AF26
OVDD	
CKE3	AH27
OVSS	
CKE2	AG27

SIGNAL NAME	SiS620 BALL NO
CKE1	AE24
CKE0	AH28
OVDD	
MD48	AJ26
OVSS	
MD16	AJ27
MD49	AE25
OVDD	
OVSS	
MD17	AG28
MD50	**AG29**
MD18	AF27
MD51	AF28
N.C.	AD25
MD19	AF29
MD52	AE26
OVDD	
MD20	AE27
OVSS	
N.C.	AC25
MD53	AE28
DVDD	
MD21	AE29
DVSS	
MD54	AD26
MD22	AD27
MD55	AD28
MD23	AB25

SIGNAL NAME	SiS620 BALL NO
MD56	AD29
OVDD	
MD24	AC26
OVSS	
MD57	AC27
MD25	AC28
MD58	AC29
MD26	AA25
MD59	AB26
OVDD	
MD27	AB27
OVSS	
MD60	AB28
MD28	AA26
MD61	AB29
OVDD	
MD29	AA27
OVSS	
MD62	AA28
MD30	Y25
MD63	AA29
MD31	Y26
ADS#	Y27
RS1#	W25
RS2#	Y28
OVSS	
DBSY#	Y29
HIT#	W27

SIGNAL NAME	SiS620 BALL NO
N.C.	W26
HITM#	W28
OVSS	
RS0#	W29
HREQ3#	V26
N.C.	V25
DRDY#	V27
OVSS	
HREQ2#	V28
HLOCK#	V29
DEFER#	U26
OVSS	
HREQ4#	U27
N.C.	U24
HTRDY#	U28
HREQ1#	U29
OVSS	
BPRI#	T26
HREQ0#	U25
BNR#	T27
OVSS	
HA4#	T28
HA6#	T29
N.C.	T24
HA9#	R26
HA3#	T25
HA5#	R27
OVSS	

SIGNAL NAME	SiS620 BALL NO
GTLREFA	R28
VSSREFA	R29
VTTA	P29
HA7#	P28
HA10#	P27
OVSS	
HA8#	P26
HA12#	P25
HA14#	N29
DVSS	
HA13#	N28
DVDD	
HA11#	N27
N.C.	P24
DVDD	
HA16#	N26
DVSS	
HA17#	M29
OVSS	
HA18#	M28
HA15#	N25
HA19#	M27
OVSS	
HA25#	M26
HA21#	L29
N.C.	N24
HA23#	L28
HA20#	M25

SIGNAL NAME	SiS620 BALL NO
HA22#	L27
OVSS	
HA28#	K29
HA27#	K28
N.C.	L26
HA24#	K27
OVSS	
HA31#	K26
HA26#	J29
HA30#	J28
OVSS	
HA29#	J27
BREQ0#	L25
CPURST#	H29
OVSS	
HD1#	H28
OVSS	
HD0#	H27
HD3#	K25
HD2#	H26
OVSS	
HD5#	G29
OVSS	
HD4#	G28
N.C.	J26
OVSS	
HD8#	G27
OVSS	

SIGNAL NAME	SiS620 BALL NO
HD6#	G26
OVSS	
HD9#	F29
HD7#	J25
HD14#	F28
OVSS	
HD12#	F27
HD10#	F26
HD15#	E29
OVSS	
HD11#	E28
HD17#	H25
HD13#	E27
OVSS	
HD20#	E26
OVSS	
HD16#	D29
HD18#	G25
HD21#	D28
OVSS	
HD19#	D27
OVSS	
HD23#	D26
HD22#	F25
HD24#	C29
OVSS	
HD25#	C28
OVSS	

SIGNAL NAME	SiS620 BALL NO
HD27#	C27
DVSS	
HD26#	B28
DVDD	
HD30#	B27
HD29#	E25
OVSS	
HD31#	A27
HD28#	**C26**
HD35#	B26
HD32#	A26
HD33#	E24
HD38#	D25
OVSS	
HD37#	C25
OVSS	
HD34#	B25
HD43#	E23
HD40#	A25
OVSS	
HD36#	D24
OVSS	
GTLREFB	C24
VSSREFB	B24
VTTB	A24
HD39#	E22
HD44#	D23
HD45#	E21

SIGNAL NAME	SiS620 BALL NO
HD47#	C23
OVSS	
HD42#	B23
OVSS	
HD41#	A23
HD51#	D21
HD52#	D22
OVSS	
HD49#	C22
DVSS	
HD48#	B22
DVDD	
HD46#	A22
OVSS	
HD59#	C21
HD57#	E20
HD54#	B21
OVSS	
HD53#	A21
OVSS	
HD50#	D20
HD60#	E19
HD56#	C20
OVSS	
HD55#	B20
OVSS	
HD63#	A20
HD61#	D19

SIGNAL NAME	SiS620 BALL NO
HD58#	C19
HD62#	B19
PHLDA#	A19
PHOLD#	E18
BMREQ#	D18
RSTIN	C18
PREQ3#	B18
PREQ0#	F17
PREQ1#	A18
OVDD	
CPUCLK	A17
OVSS	
AVDD	A16
AVSS	E17
PCIRST#	D17
PREQ2#	C17
PGNT0#	B17
PGNT1#	F16
PGNT2#	D16
DVSS	
PGNT3#	C16
DVDD	
AD31	B16
AD30	E16
AD29	D15
OVDD	
AD28	C15
OVSS	

SIGNAL NAME	SiS620 BALL NO
AD27	B15
AD26	E14
AD25	A15
AD24	F14
C/BE3#	A14
OVDD	
AD23	B14
OVSS	
AD22	C14
AD21	E13
AD20	D14
OVDD	
AD19	A13
OVSS	
AD18	B13
AD17	F13
AD16	C13
DVSS	
C/BE2#	D13
DVDD	
FRAME#	A12
OVDD	
IRDY#	B12
OVSS	
TRDY#	C12
DEVSEL#	E12
PLOCK#	D12
STOP#	D11

SIGNAL NAME	SiS620 BALL NO
PAR	A11
C/BE1#	B11
AD15	C11
AD14	E11
AD13	A10
OVDD	
AD12	B10
OVSS	
AD11	C10
AD10	E10
AD9	D10
OVDD	
AD8	A9
OVSS	
C/BE0#	B9
AD7	D9
AD6	C9
AD5	E9
AD4	A8
OVDD	
AD3	B8
OVSS	
AD2	C8
AD1	E8
AD0	D8
AVSS4	A7
RSET	B7
COMP	E7

SIGNAL NAME	SiS620 BALL NO
VREF	C7
BOUT	**A6**
GOUT	**B6**
ROUT	**A5**
AVDD4	**B5**
AVDD 2/3	A4
AVSS 2/3	B4
AVSS1	E6
AVDD1	A3
OSCI	E5
VSYNC	C4
OVSS	
HSYNC	D4
OVDD	
DDCCLK	B3
OVDD	
OVSS	
DDCDATA	C3
N.C.	
N.C.	
N.C.	
N.C.	
N.C.	
N.C.	
N.C.	
N.C.	
N.C.	

SIGNAL NAME	SiS620 BALL NO
N.C.	
N.C.	

4. PIN DESCRIPTION

4.1. HOST BUS INTERFACE

NAME	TYPE ATTR	DESCRIPTION
CPUCLK	I	**CPU Clock**
ADS#	I/O GTL+	**Address Strobe :** Address Strobe is driven by the CPU to indicate the start of a CPU bus cycle.
HREQ[4:0]#	I/O GTL+	**Request Command:** HREQ[4:0]# are used to define each transaction type during the clock when ADS# is asserted and the clock after ADS# is asserted.
BREQ0#	O GTL+	**Symmetric Agent Bus Request:** BREQ0# is driven by the symmetric agent to request for the bus.
BNR#	I/O GTL+	**Block Next Request:** This signal can be driven asserted by any bus agent to block further requests being pipelined.
HLOCK#	I GTL+	**Host Lock :** CPU asserts HLOCK# to indicate the current bus cycle is locked.
HIT#	I/O GTL+	**Keeping a Non-Modified Cache Line**
HITM#	I/O GTL+	**Hits a Modified Cache Line:** Hit Modified indicates the snoop cycle hits a modified line in the L1 cache of CPU.
DEFER#	O GTL+	**Defer Transaction Completion:** SiS620 will use this signal to indicate a retry response to the host bus.

RS[2:0]#	O GTL+	**Response Status:** RS[2:0]# are driven by the response agent to indicate the transaction response type. The following shows the response type. **RS[2:0] Response RS[2:0] Response** 000 Idle State 100 Reserved 001 Retry 101 No data 010 Reserved 110 Implicit Write-back 011 Reserved 111 Normal Data
HTRDY#	I/O GTL+	**Target Retry:** During write cycles, response agent will drive TRDY# to indicate the agent is ready to accept data.
DRDY#	I/O GTL+	**Data Ready:** DRDY# is driven by the bus owner whenever the data is valid on the bus.
DBSY#	I/O GTL+	**Data Bus Busy:** Whenever the data is not valid on the bus with DRDY# is deserted, DBSY# is asserted to hold the bus.
BPRI#	O GTL+	**Priority Agent Bus Request:** BPRI# is driven by the priority agent that wants to request the bus. BPRI# has higher priority than BREQ0# to access a bus.
RSTIN#	I	**Reset:** RSTIN# is generated from SiS5595 and is used to reset the SiS620 into initial state. The SiS620 drives out CPURST# to reset CPU based on this signal.
CPURST#	O GTL+	**Host Bus Reset:** CPURST# is used to keep all the bus agents in the same initial state before valid cycles issued.
HA[31:3]#	I/O GTL+	**Host Address Bus**
HD[63:0]#	I/O GTL+	**Host Data Bus**

4.2. DRAM CONTROLLER

NAME	TYPE ATTR	DESCRIPTION
SDCLK	I	**SDRAM Clock Input**
MD[63:0]	I/O	**System Memory Data Bus**
MA[14:0]	O	**System Memory Address Bus**
CSA[5:0]#	O	**SDRAM Chip Select**
CSB[5:0]#	O	**SDRAM Chip Select Signals (Duplicated Copy)**
DQM[7:0]#	O	**SDRAM Input/Output Data Mask**
WE#	O	**SDRAM Write Enable**
SRAS#	O	**SDRAM Row Address Strobe**
SCAS#	O	**SDRAM Column Address Strobe**
CKE[5:0]	O	**SDRAM Clock Enable [5:0]:** During Suspend-to-DRAM mode (ACPI S2 or S3 state), SDRAM can be put into self-refresh mode by asserting CKE[5:0].

4.3. PCI INTERFACE

NAME	TYPE ATTR	DESCRIPTION
PCICLK	I	**PCI Clock:** The PCICLK input provides the fundamental timing and the internal operating frequency for the SiS Chip. It runs at the same frequency and skew of the PCI local bus.
C/BE[3:0]#	I/O	**PCI Bus Command and Byte Enables:** PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. C/BE[3:0]# are outputs when the SiS Chip is a PCI bus master and inputs when it is a PCI slave.

AD[31:0]	I/O	**PCI Address /Data Bus:** In address phase: 1.When the SiS Chip is a PCI bus master, AD[31:0] are output signals. 2.When the SiS Chip is a PCI target, AD[31:0] are input signals. In data phase: 1.When the SiS Chip is a target of a memory read/write cycle, AD[31:0] are floating. 2.When the SiS Chip is a target of a configuration or an I/O cycle, AD[31:0] are output signals in a read cycle, and input signals in a write cycle.
PAR	I/O	**Parity :** SiS620 drives out Even Parity covering AD[31:0] and C/BE[3:0]#. It does not check the input parity signal.
FRAME#	I/O	**Frame#:** FRAME# is an output when the SiS Chip is a PCI bus master. The SiS Chip drives FRAME# to indicate the beginning and duration of an access. When the SiS Chip is a PCI slave device, FRAME# is an input signal.
IRDY#	I/O	**Initiator Ready:** IRDY# is an output when the SiS Chip is a PCI bus master. The assertion of IRDY# indicates the current PCI bus master's ability to complete the current data phase of the transaction. For a read cycle, IRDY# indicates that the PCI bus master is prepared to accept the read data on the following rising edge of the PCI clock. For a write cycle, IRDY# indicates that the bus master has driven valid data on the PCI bus. When the SiS Chip is a PCI slave, IRDY# is an input pin.
TRDY#	I/O	**Target Ready:** TRDY# is an output when the SiS Chip is a PCI slave. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, TRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, TRDY# indicates that the target is prepared to accept data from the PCI bus. When the SiS Chip is a PCI master, it is an input pin.

STOP#	I/O	**Stop#:** STOP# indicates that the bus master must start terminating its current PCI bus cycle at the next clock edge and release control of the PCI bus. STOP# is used for disconnect, retry, and target-abort sequences on the PCI bus.
DEVSEL#	I/O	**Device Select:** As a PCI target, SiS Chip asserts DEVSEL# by doing positive or subtractive decoding. SiS Chip positively asserts DEVSEL# when the DRAM address is being accessed by a PCI master, PCI configuration registers or embedded controllers' registers are being addressed, or the BIOS memory space is being accessed. The low 16K I/O space and low 16M memory space are responded subtractively. The DEVESEL# is an input pin when SiS Chip is acting as a PCI master. It is asserted by the addressed agent to claim the current transaction.
PLOCK#	I/O	**PCI Lock:** When PLOCK# is sampled asserted at the beginning of a PCI cycle, SiS620 considers itself being locked and remains in the locked state until PLOCK# is sampled and negated at the following PCI cycle.
PREQ[3:0]#	I	**PCI Bus Request:** PCI Bus Master Request Signals
PGNT[3:0]#	O	**PCI Bus Grant:** PCI Bus Master Grant Signals
PCIRST#	I	**PCI Bus Reset:** The PCIRST# is used to reset the device on PCI bus.
PHOLD#	I	**Bus Hold:** PHOLD# is driven by SiS5595 to indicate its intention to become PCI bus master.
PHLDA#	O	**Bus Hold Acknowledge:** The PCI arbiter inside the SiS620 asserts PHLDA# in response to the assertion of PHOLD#, indicating the SiS5595 can become PCI master.

4.4. PCI IDE INTERFACE

NAME	TYPE ATTR	DESCRIPTION
IDA[15:0]	I/O	**Primary Channel Data Bus**
IDB[15:0]	I/O	**Secondary Channel Data Bus**
IDECSA[1:0]#	O	**Primary Channel CS[1:0]**
IDECSB[1:0]#	O	**Secondary Channel CS[1:0]**
IIOR[A:B]#	O	**Primary/Secondary Channel IOR# Signals**
IIOW[A:B]#	O	**Primary/Secondary Channel IOW# Signals**
ICHRDY[A:B]	I	**Primary/Secondary Channel ICHRDY# Signals**
IDREQ[A:B]	I	**Primary/Secondary Channel DMA Request Signals**
IDACK[A:B]#	O	**Primary/Secondary Channel DMACK# Signals**
IIRQ[A:B]	I	**Primary/Secondary Channel Interrupt Signals**
IDSAA[2:0]	O	**Primary Channel Address [2:0]**
IDSAB[2:0]	O	**Secondary Channel Address [2:0]**
CBLID[A:B]	I	**Primary/Secondary Ultra-66 Cable ID**

4.5. VGA INTERFACE

NAME	TYPE ATTR	DESCRIPTION
HSYNC	O	**Horizontal Sync**
VSYNC	O	**Vertical Sync**
SCLK	O	**Clock Output to Display Memory**
DDCCLK	I/O	**Display Data Channel Clock Line**
DDCDATA	I/O	**Display Data Channel Data Line**
COMP	AI	**Compensation Pin** Connect this pin to AVDD via a 0.1uF capacitor
RSET	AI	**Reference Resistor** An external resistor is connected between the RSET pin and AGND to control the magnitude of the full-scale current.
VREF	AI	**Voltage Reference** If an external voltage supply is used, it must supply this input with a 1.235V reference voltage.

ROUT	AO	**Red Signal Output**
GOUT	AO	**Green Signal Output**
BOUT	AO	**Blue Signal Output**
VMA[11:0]	O	**Display Memory Address Bus**
DSF	O	**SGRAM Special Function Input Flag**
VMD[63:62]	I/O	**Display Memory Data Bus**
VMD61/ PLHSYNC	I/O	**Display Memory Data Bus/** **Flat Panel Horizontal SYNC**
VMD60/ PLVSYNC	I/O	**Display Memory Data Bus/** **Flat Panel Vertical SYNC**
VMD59/ FDDCCLK	I/O	**Display Memory Data Bus/** **Flat Panel DDCCLK**
VMD58/ FDDCDAT	I/O	**Display Memory Data Bus/** **Flat Panel DDCDATA**
VMD57/ FPLDEADJ	I/O	**Display Memory Data Bus/** **Flat Panel Device Enable**
VMD56/ PLXLCLK	I/O	**Display Memory Data Bus/** **LVDS Controller Clock**
MD[55:48]/B[7:0]	I/O	**Display Memory Data Bus/** **Flat Panel Blue Digital Out [7:0]**
MD[47:40]/G[7:0]	I/O	**Display Memory Data Bus/** **Flat Panel Green Digital Out [7:0]**
MD[39:32]/R[7:0]	I/O	**Display Memory Data Bus/** **Flat Panel Red Digital Out [7:0]**
VMD[31:0]	I/O	**Display Memory Data Bus**
VDQM[7:0]	O	**Display Memory SDRAM Input/Output Mask**
OSCI	I	**External 14.318MHz Clock Input**
VSRAS#	O	**Display Memory SDRAM Row Strobe**
VSCAS#	O	**Display Memory SDRAM Column Strobe**
VWE#	O	**Display Memory SDRAM Write Enable**
VCS[1:0]#	O	**Display Memory SDRAM Chip Select**

ENVCO	I/O	**1: Enable Internal VCO** **0: Disable Internal VCO**
PLSENSE	I	**Flat Panel Presence Detection**
PLPWDN	O	**Flat Panel Power Down**
PL-DCLK	O	**Flat Panel Clock**

4.6. POWER PINS

NAME	TYPE ATTR	DESCRIPTION
DVDD	PWR	**Digital Power**
DVSS	PWR	**Digital Ground**
5VCC	PWR	**5V DC Power Source.**
OVDD	PWR	**IO Power**
OVSS	PWR	**IO Ground**
AVDDA/AVSSA	PWR	**Power for IDE Ultra/66 Clock PLL**
AVDDB/AVSSB	PWR	**Power for System Memory Clock PLL**
AVDDC/AVSSC	PWR	**Power for CPU Clock PLL**
AVDD1/AVSS1	PWR	**Power for VGA Dot Clock PLL**
AVDD2/3/AVSS2/3	PWR	**Power for VGA Memory Interface Clock PLL**
AVDD4/AVSS4	PWR	**Power for VGA RAMDAC**
GTLREF[A:B]	PWR	**Reference Voltage for GTL+ interface.**
VSSREF[A:B]	PWR	**Ground signals for reference voltages.**
VTT[A:B]	PWR	**Termination to Termination Voltage.**

4.7. MISC. PINS

NAME	TYPE ATTR	DESCRIPTION
TEST#	I	**Test Mode Select for NAND Tree Function.** Ball connectivity test mode Pull-up : Disable Pull-down : Enable

BMREQ#	O	**Bus Master Request Status** This signal is used to carry two messages: 1. AGP activities to reload the system standby timer in SiS5595. 2. AGP/PCI/IDE bus master requests event to exit from ACPI/C3 state. Upon power up, the clock after the FRAME# is sampled and asserted, is defined as the slot containing the Bus master request event, the next clock containing the AGP activity event, ...etc.
INTA#	O	**PCI INTA# Signal**
IRQ14	O	**IDE Primary Channel Interrupt**
IRQ15	O	**IDE Secondary Channel Interrupt**

5. HARDWARE TRAP

There are some pins used for trapping purpose to identify the hardware configurations at the power-up stage. These pins will be recognized as "1" if pull-up resistors are employed; and will be recognized as "0" if pull-down resistors are employed.

SYMBOL	DESCRIPTION
MD62	**Integrated VGA Function Enable** Pull-up: Disable Pull-down: Enable (recommended)
MD61	**Integrated VGA Decoding Selection at Host Interface** Pull-up: Slow Decode Pull-down: Fast Decode (recommended)
MD59	**VGA & DFP INTA# Enable** Pull-up: Disable Pull-down: Enable (recommended)
MD48	**Integrated VGA : UMA/Non-UMA Selection** Pull-up: VGA in UMA mode Pull-down: VGA in Non-UMA mode
MD47	**PCI Clock PLL Circuit Enable** Pull-up: Disable Pull-down: Enable (recommended)
MD46	**SDRAM Clock PLL Circuit Enable** Pull-up: Disable Pull-down: Enable (recommended)
MD45	**CPU Clock PLL Circuit Enable** Pull-up: Disable Pull-down: Enable (recommended)
MD43	**Internal Clock Test Mode** Pull-up: Enable Pull-down: Disable (recommended)
MD[39:36]	**Internal Display Memory Clock(SCLK) Delay Control Bits[3:0]** Please refer to Note 2

ENVCO	**Test Mode Control for MCLK Clock Generator** Pull-up: Normal Mode (recommended) Pull-down: Test Mode
MD58	**Panel Link Enable** Pull-up: Enable Panel Link Pull-Down: Disable Panel Link(default)
MD49	**Video Subsystem Enable** Pull-up: Disabled Pull-Down: Enable (recommended)
MD52	**AGP Bus Enable** Pull-up: Disabled Pull-Down: Enable (recommended)
MD44	**Test Mode Control** Pull-up: Test Mode Pull-down: Normal Mode (recommended)
VMD63, VMD62, VMD61	**Please refer to Note 3.**

Note:

1. There are internal pull-down resistors on MD lines.
2. This field controls the phase of internal display memory clock with respect to external SDRAM clock (SDCLK).

MD[39:36]	Descriptions	MD[39:36]	Descriptions
1111	+8.0ns	0111	+4.0ns
1110	+7.5ns	0110	+3.5ns
1101	+7.0ns	0101	+3.0ns
1100	+6.5ns	0100	+2.5ns
1011	+6.0ns	0011	+2.0ns
1010	+5.5ns	0010	+1.5ns
1001	+5.0ns	0001	+1.0ns
1000	+4.5ns	0000	+0.5n

For determining the frequency of Local Frame Buffer:

VMD61	VMD62	VMD63	MCLK	FRAME BUFFER TYPE
0	0	0	83MHz	SDRAM
0	0	1	90MHz	SDRAM
0	1	0	100MHz	SDRAM
1	1	1	110MHz	SDRAM
1	0	0	83MHz	SGRAM
1	0	1	90MHz	SGRAM
1	1	0	100MHz	SGRAM
1	1	1	110MHz	SGRAM

6. FUNCTION DESCRIPTION

6.1. HOST INTERFACE

6.2. DRAM CONTROLLER

The SiS620 supports three-DIMM/six-bank up to 1.5GBytes of SDRAM. Each bank can be single or double sided with 64-bit data bus.

6.2.1. SDRAM CONFIGURATION

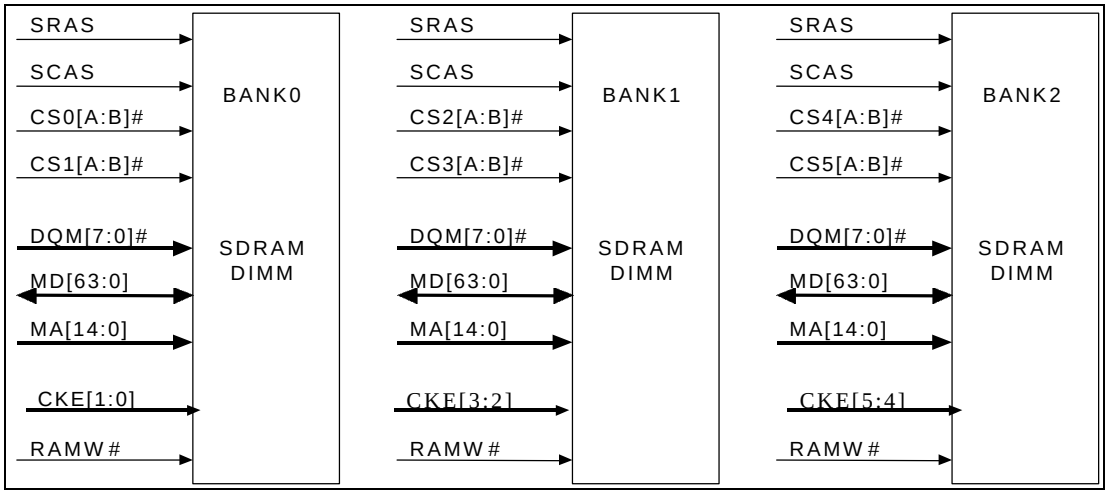


Figure 6.2- 1 SDRAM Configuration

6.2.2. DRAM SCRAMBLE TABLE

The DRAM scramble table contains information for memory address mapping. These tables provide the translation between CPU host address and memory Row and Column address.

6.2.2.1. 2 Banks Device SDRAM Type:

Type	1M (1x11x8)		2M (1x11x9)		4M (1x11x10)	
Address	Row	Column	Row	Column	Row	Column
MA0	15	3	15	3	15	3
MA1	16	4	16	4	16	4
MA2	17	5	17	5	17	5
MA3	18	6	18	6	18	6
MA4	19	7	19	7	19	7
MA5	20	8	20	8	20	8
MA6	21	9	21	9	21	9

MA7	22	10	22	10	22	10
MA8	12	NA	23	11	23	11
MA9	13	NA	13	NA	24	12
MA10	14	NA	14	NA	14	NA
MA11	11	11	12	12	13	13
MA12	NA	NA	NA	NA	NA	NA
MA13	NA	NA	NA	NA	NA	NA
MA14	NA	NA	NA	NA	NA	NA

Type	**4M (1x13x8)**		**8M (1x13x9)**		**16M (1x13x10)**	
Address	Row	Column	Row	Column	Row	Column
MA0	15	3	15	3	15	3
MA1	16	4	16	4	16	4
MA2	17	5	17	5	17	5
MA3	18	6	18	6	18	6
MA4	19	7	19	7	19	7
MA5	20	8	20	8	20	8
MA6	21	9	21	9	21	9
MA7	22	10	22	10	22	10
MA8	12	NA	23	11	23	11
MA9	13	NA	13	NA	24	12
MA10	14	NA	14	NA	14	NA
MA11	11	11	12	12	13	13
MA12	NA	NA	NA	NA	NA	NA
MA13	23	NA	24	NA	25	NA
MA14	24	NA	25	NA	26	NA

6.2.2.2. 4 banks Device SDRAM Type:

Type	**2M (2x11x8))**		**4M (2x12x8)**		**8M (2x12x9)**		**16M (2x12x10)**	
Address	Row	Column	Row	Column	Row	Column	Row	Column
MA0	15	3	15	3	15	3	15	3

MA1	16	4	16	4	16	4	16	4
MA2	17	5	17	5	17	5	17	5
MA3	18	6	18	6	18	6	18	6
MA4	19	7	19	7	19	7	19	7
MA5	20	8	20	8	20	8	20	8
MA6	21	9	21	9	21	9	21	9
MA7	22	10	22	10	22	10	22	10
MA8	23	NA	23	NA	23	11	23	11
MA9	13	NA	13	NA	24	NA	24	12
MA10	14	NA	14	NA	14	NA	25	NA
MA11	11	11	11	11	12	12	13	13
MA12	12	12	12	12	13	13	14	14
MA13	NA	NA	24	NA	25	NA	26	NA
MA14	NA	NA	NA	NA	NA	NA	NA	NA

Type	**8M (2x13x8)**		**16M (2x13x9)**		**32M (2x13x10)**	
Address	Row	Column	Row	Column	Row	Column
MA0	15	3	15	3	15	3
MA1	16	4	16	4	16	4
MA2	17	5	17	5	17	5
MA3	18	6	18	6	18	6
MA4	19	7	19	7	19	7
MA5	20	8	20	8	20	8
MA6	21	9	21	9	21	9
MA7	22	10	22	10	22	10
MA8	23	NA	23	11	23	11
MA9	13	NA	24	NA	24	12
MA10	14	NA	14	NA	25	NA
MA11	11	11	12	12	13	13
MA12	12	12	13	13	14	14
MA13	24	NA	25	NA	26	NA

MA14	25	NA	26	NA	27	NA

6.2.3. DRAM DETECTION SEQUENCE

The DRAM detection is a repeated sequence performed on a bank-by-bank basis by BIOS. The proper configuration settings for each bank will be written into corresponding DRAM configuration registers when the detection is accomplished. The following steps describe the SDRAM detection sequence.

Step 1. Issue a PRECHARGE command to SDRAM by toggling Reg57_b7h to "1" and then to "0".

Step 2. Issue a "Mode Register Set"(MRS) command to SDRAM by toggling Reg57_b6 to "1" and then to "0". The SDRAM device, if exist, should respond to this command by loading the necessary information (CAS Latency) into SDRAM.

Step 3. Instruct SDRAM to perform refresh cycles (at least two times) by toggling Reg57_b5 to "1".

Step 4. Write and then read a predefined test pattern into SDRAM. If the data being read back match the data being previously written into the same address location, then there exist SDRAM.

Step 5. The SDRAM size can then be determined by writing/reading the test pattern based on the MA mapping table.

Step 6. Repeat step 1 to step 8 for all banks.

6.2.4. SDRAM PERFORMANCE

Table 6.2-1 SDRAM Timing Table –Host bus and Memory Bus in synchronous mode

CYCLE TYPE	DRAM TYPE	100/66 MHz	NOTE
Read Page Hit	SDRAM	8-1-1-1	CL=2
Read Page Hit	SDRAM	9-1-1-1	CL=3
Read Row Start	SDRAM	11-1-1-1	CL=2
		12-1-1-1	CL=3
Read Page Miss	SDRAM	14-1-1-1	CL=2
		15-1-1-1	CL=3
Back-to-Back Burst Read Page Hit	SDRAM	8-1-1-1-1-1-1-1-...	CL=2
		9-1-1-1-1-1-1-1-...	CL=3
Posted Write	SDRAM	6-1-1-1	
Write Retire Rate	SDRAM	1-1-1/2-2-2	CL=2
(Write Retire Rate) (Buffer to DRAM)	SDRAM	1-1-1/2-2-2	CL=3
(Write Page Hit) (Buffer to DRAM)	SDRAM	3	CL=2
		3	CL=3

Write Row Start	SDRAM	6	CL=2
		6	CL=3
Write Page Miss	SDRAM	9	CL=2
		9	CL=3

6.2.5. DRAM ARBITER

The DRAM arbiter is the interface between the DRAM controller and the host interface which can access DRAMs. In addition to passing or translating the information from outside to DRAM controller, arbiter is also responsible for which master has higher priority to access DRAMs. The arbiter treats different DRAM access request as DRAM master, and that makes there be 8 masters which are trying to access DRAMs by sending their request to the arbiter. After one of them gets the grant from the arbiter, it owns DRAM bus and begins to do memory data transaction. The masters are: Refresh high request, CRT-High request, CPU read request, CPU write request, VGA AGP access request, CRT-Low request, Refresh low request. The order of these masters shown above also stands for their priority to access memory.

6.2.6. REFRESH CYCLE

The refresh cycle occurs every 15.6us. It is timed with a counter based on PCI clock.

6.3. IDE CONTROLLER

The integrated PCI IDE controller supports PIO, Mutiword DMA and Ultra DMA/33/66 operation.

There is a 64-byte FIFO associated with each channel. Data can be pushed into FIFO in word- or Dword- increments. When doing post write in PIO mode, the command/control port access is suspended until the FIFO is empty. When doing prefetch in PIO mode, the command/control port access is suspended until the FIFO is full. In DMA mode, the command/control access will go through a higher priority than the DMA data transfer cycles. Both primary and secondary channels may be programmed as Native mode or Compatibility mode via the Class Code Field in the controller's Configuration Space register.

In Compatibility mode, the interrupt requests for channel 0 and channel 1 are re-routed to IRQ 14 and IRQ 15 of the built-in Interrupt Controller. In Native mode, the interrupt requests of both channels share the same PCI interrupt pin. The interrupt pin may be re-routed to any one of eleven ISA compatible interrupts (IRQ[15:14], IRQ[12:9], and IRQ[7:3]) by programming Register 61h bits [3:0] in SiS5595 PCI to ISA bridge Configure space. Accesses to the I/O ports are via the addresses programmed in Base Address Registers 10h~13h, 14h~17h, 18h~1Bh and 1Ch~1Fh in PCI IDE configuration space.

While serving as a bus master device, the IDE controller may transfer data between IDE devices and main memory directly. By performing the DMA transfer, IDE offloads the CPU and improves system performance. Bus master DMA programming is according to the information specification "Programming Interface for Bus Master IDE Controller". Proper cycle timing is generated to meet PCI Bus speed and different modes of IDE drive. All cycle timing can be controlled by software programming from Register 40h to Register 49h in PCI IDE configuration space.

PIO mode operation

The IDE controller is capable of doing prefetch or postwrite in PIO mode. The count(in bytes) of prefetch length for each channel can be programmed in Prefetch Count Registers 4Ch~4Dh and 4Eh~4Fh in PCI IDE Configuration space. When prefetch is enabled, the controller will start doing prefetch when the first read data port command is received. It will keep prefetching until the FIFO is full or when prefetch count is reached. Whenever the FIFO becomes non-empty again, the prefetch will automatically resume until the prefetch count is reached.

When post write is enabled, the host can write data to FIFO in word- or Dword- increment. The IDE controller will automatically start IDE write cycles as long as FIFO is non-empty. When the fast post write function is enabled, the write IDE data port command on PCI bus will last for 3 PCI clocks only. When disabled, the PCI command will be 5 PCI clocks.

6.3.1. DMA MODE OPERATION

There is a DMA engine associated with each channel. The DMA engine can be invoked by writing the start-bit in Bus Master command register. The DMA engine will first request for PCI bus to read the descriptor from memory, load the address pointer and byte-count. For IDE read operation, the controller will start prefetching data into FIFO at this moment. For write operation, after descriptor is read, the DMA engine will again request for PCI bus to read data from memory to FIFO. At the same time, when the FIFO becomes non-empty, the controller will automatically start IDE write cycles to flush data in FIFO to IDE device. When data in FIFO is less than eight bytes, the DMA engine will again request for PCI bus to re-fill the FIFO.

6.3.2. ULTRA-DMA/33/66 OPERATION

Ultra DMA is a fast data transfer protocol used on IDE bus. By utilizing both the rising edge and the falling edge of the data strobe signal to latch data from DD[15:0], the data transfer rate is effectively doubled than that of the traditional multi-word DMA while the highest fundamental frequency on the cable is the same. For Ultra-DMA operations, the following signal lines shall change to their new definition when IDACK# is asserted. These signals will revert back to their old definitions right after IDACK# is de-asserted.

Table 6.3-1 Table for Different Command Definition

OLD DEFINITION	NEW DEFINITION
IIOW#	STOP#
IIOR#	HDMARDY# --- data in operation HSTROBE --- data out operation
ICHRDY#	DSTROBE --- data in operation DDMARDY# --- data out operation

There are three phases for an Ultra-DMA operation as defined in the protocol: Burst Initiation phase, Data Transfer phase and Burst Termination phase. The Burst Initiation phase is always initiated by the device when it asserts IDREQ. The SiS620 will respond IDACK# after the base address and byte-count in the PRD table entry are read from system memory.

During Data Transfer phase, either the sender or the receiver can pause a burst to allow for internal data processing and then resume the burst some time later. There are three situations that SiS620 will pause a burst:

1. As a sender during data-out operation and the internal FIFO is empty. The burst will resume after the DMA engine re-fill the FIFO with data from system memory.
2. As a receiver during data-in operation and the internal FIFO is full. The burst will resume after the DMA engine dumps the data in FIFO to system memory.
3. For a PRD table with multiple entries, the DMA engine will start the burst data transfer after base address and byte-count of one entry are read. When the data transfer for the current entry is completed and the next entry has not yet been read into the controller, the SiS620 shall also initiate a pause. After the base address and byte-count for next entry are read, the burst resumes.

The Burst Termination phase can be initiated by either the SiS620 or the device. In normal situations, when the data transfer has reached the byte-count as defined in the last entry of the PRD table, the SiS620 will initiate a burst termination by asserting STOP#. After the termination is acknowledged by the device and HSTROBE signal returns to the asserted state, the CRC will be sent on negation of IDACK#. There is one additional situation that the SiS620 will also initiate a burst termination:

During the burst data transfer, the host(CPU) is trying to access the command/control block registers. Since the command/control block access cycle is assigned to have higher priority than data transfer cycles, the SiS620 must first terminate the burst, de-assert the IDACK# signal, generate the corresponding DA[2:0] and CS[1:0] on IDE bus, and then complete the command/control block register access cycle. After that, the burst can be resumed by entering the Burst Initiation phase when the device re-asserts IDREQ.

6.4. PCI BRIDGE

The PCI bridge of SiS620 consists of three parts: PCI arbiter, PCI master bridge and PCI target bridge. The PCI arbiter controls the assignment of PCI bus ownership among all PCI masters. The PCI master bridge forwards the transactions from host bus. The PCI target bridge claims PCI cycles toward system memory or AGP bus as required by PCI master devices.

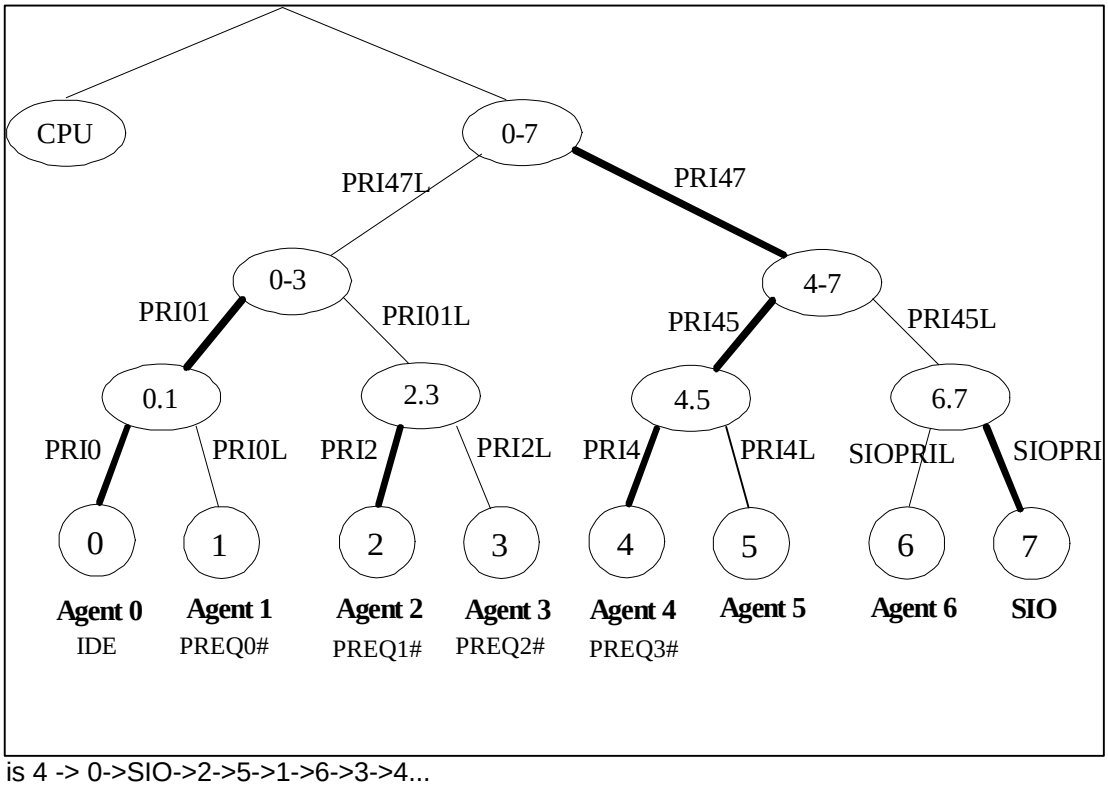
6.4.1. PCI ARBITER

The main function of PCI arbiter takes charge of the PCI bus ownership assignment. This PCI arbiter supports at most 4 external PCI masters using standard PCI REQ#/GNT# mechanism and 1 PCI master using PHOLD#/PHLDA# mechanism. The master that uses PHOLD#/PHLDA mechanism is not pre-emptive. That means the master can own the bus as long as it wishes after it gains the control of PCI bus. The master that use PHOLD#/PHLDA# mechanism to access PCI bus is typically SiS5595 chip.

Arbitration Algorithm

PCI Masters (Agent 0~6, SIO) Requests

Figure6.4-1 Arbitration Tree shows the arbitration tree in arbiter design. Whenever a PCI cycle occurs, priority status will be changed. The initial priority for master 0-7 to own PCI bus



is 4 -> 0->SIO->2->5->1->6->3->4...

Figure 6.4- 1 Arbitration Tree

NOTE: 1. "SIO" means the System I/O, i.e., SiS5595.

2. The arbiter will treat PHOLD# as Agent SIO.

6.4.1.1. CPU Request

To present CPU from using PCI bus for a long time while PCI masters continuously deliver requests to the arbiter, SiS620 implemented a timer-based algorithm to reserve PCI bandwidth for CPU. Three timers, PCI Grant Timer (PGT)/ Master Latency Timer (MLT)/ CPU Idle Timer (CIT), are included in the host bridge for this purpose.

Whenever any PCI device owns the PCI bus other than host bridge, PCI grant timer (PGT) starts to count. After the timer is expired, the arbiter gives PCI bus grant to host bridge.

Once the host bridge gets a chance to start a transaction on PCI bus, its master latency timer (MLT) begins to count. After MLT is expired, the arbiter grants the bus to a PCI master device.

If there is no request from any PCI devices, the arbiter parks the bus on the host bridge. The ratio MLT/PGT approximately guarantees the minimum PCI bandwidth allocated to host bridge when CPU and PCI masters are contending for system resources, but it does not constrain CPU's highest utilization of PCI bus because of our bus parking policy.

To prevent the host bridge from capturing PCI bus too long while CPU actually has nothing to do at all, the third timer, CPU Idle Timer (CIT) is included in our design. CIT starts to count when the host bridge get a chance to start a transaction on PCI bus, but is reloaded with its initial value whenever the host bus leaves idle state. CIT actually keeps track on how long the CPU is in idle state. After CIT is expired, the host bridge de-asserts its request signal just in the same manner as the case of MLT' s expiration.

PGT is a 16-bit timer. MLT and CIT are both 8-bit timers. All of the initial values of the three timers are programmable and can be tuned according to the nature of the application. Although CIT & MLT are both 8-bit timers, the initial value of CIT is typically programmed much smaller than MLT. SiS620 supports concurrency between Host-to-PCI write transactions and PCI-to-Memory write transactions. Host bridge and PCI Master Priority Timer is used to balance the PCI bandwidth between CPU and PCI masters during the period of concurrency

6.4.2. PCI BUS INTERFACE

The bridge performs medium address decoding and supports all memory cycles (including memory write, memory write and invalidate, memory read, memory read multiple and memory read line) and configuration cycles targeting the bridge.

While the PCI master creating a resource lock on the bridge, the bridge will translate this exclusive access by keeping the Pentium II bus ownership continuously.

6.4.3. TARGET INITIATED TERMINATION

The SiS620 as a PCI slave will terminate a transaction with RETRY when:

1. It cannot meet the initial latency requirement.

2. It is currently being locked by another master.

3. The posting buffers become unavailable during PCI write.

4. The posting buffers are not flushed during PCI read.

The SiS620 as a PCI slave will terminate a transaction with DISCONNECT WITHOUT DATA when:

1. The bridge cannot meet the subsequent latency requirement.

2. The posting buffers become unavailable during PCI write.

The SiS620 as a PCI slave will terminate a transaction with DISCONNECT WITH DATA when:

1. The burst length reaches the resource boundary.

2. The prefetch is not enabled during PCI master read cycles.

3. The posting buffers become unavailable during PCI master write cycles.

6.4.4. PCI MASTER CONTROLLER (PMR)

PMR locally has 4 level deep DW wide circular buffer.

Supports Asynchronous PCI clock.

Supports post write, burst read/write.

Zero wait state burst cycles up to 512 bytes.

Supports fast back-to-back transfer.

Supports PCI LOCK# transaction.

Fast reset emulation.

Fast A20M# emulation.

CPU involves PCI master arbitration.

Using configuration mechanism #1 for converting CPU I/O cycles to PCI configuration cycles.

When CPU issues a line read cycle, converts the toggle mode address to the linear mode address automatically, then forwards to the PCI side.

The PCI Master Controller forwards the CPU cycles not targeting the local memory to the PCI bus. In the case of a 64-bit CPU request or a misalign 32-bit CPU request the PMR assumes the read assembly and write disassembly control. A 4 level local posted write buffer is implemented to improve the CPU to PCI memory write performance. For PCI memory write cycles, the CPU data are pushed into the buffer as soon as FIFO is empty and then forwarded to PCI bus. If a line read cycle forwarded to the PCI, PCI master controller will convert the toggle mode address to the linear mode address automatically, then forward to the PCI side. If the consecutive written data is in DW incremental sequence, they will be transferred to the PCI bus in a burst manner.

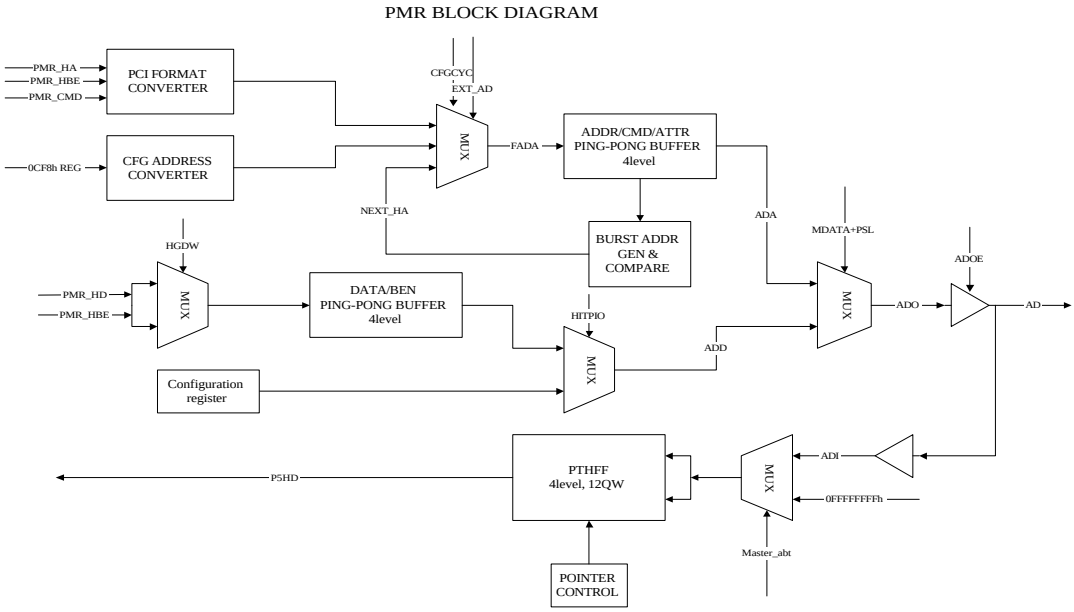


Figure 6.4-2 Block Diagram for PMR

6.4.5. PCI BURST AND POST MODE

If the BIOS turns on the burst feature, SiS620 will forward the cycle to PCI side and progress in burst mode. If this is a line read cycle, because CPU deliver a burst cycle in toggle mode, PMR will translate it to linear mode and start from "00" QW.

6.5. SUPER-AGP ARCHITECTURE

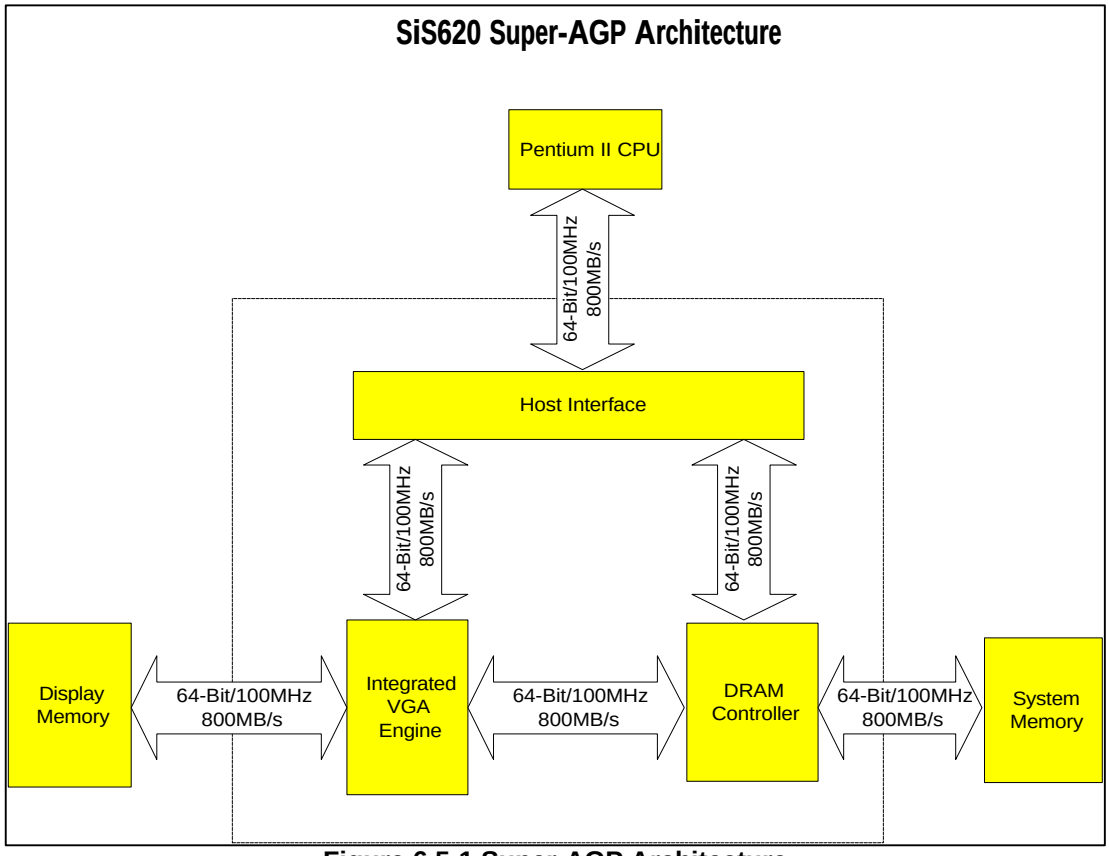


Figure 6.5-1 Super-AGP Architecture

6.5.1. VGA AND HOST/MEMORY INTERFACE

6.5.2. GRAPHIC WINDOW

The Graphic Window (GW) is a virtual, contiguous, programmable range and can be re-mapped by Graphic Address Re-mapping Table (GART) into non-contiguous pages of the system memory. Graphic Window is defined by Graphic Window Base Address (GWBA) configuration register. The size of Graphic Window is allowed the selection of 4M, 8M, 16M, 32M, 64M, 128M and 256M. It is defined by Graphic Window Size Register. When an access cycle falls within the Graphic Window, the memory controller will first read the re-mapping information from GART, translate into physical address, and then read the data from system memory.

Figure 6.5-2 shows the graphic address re-mapping function.

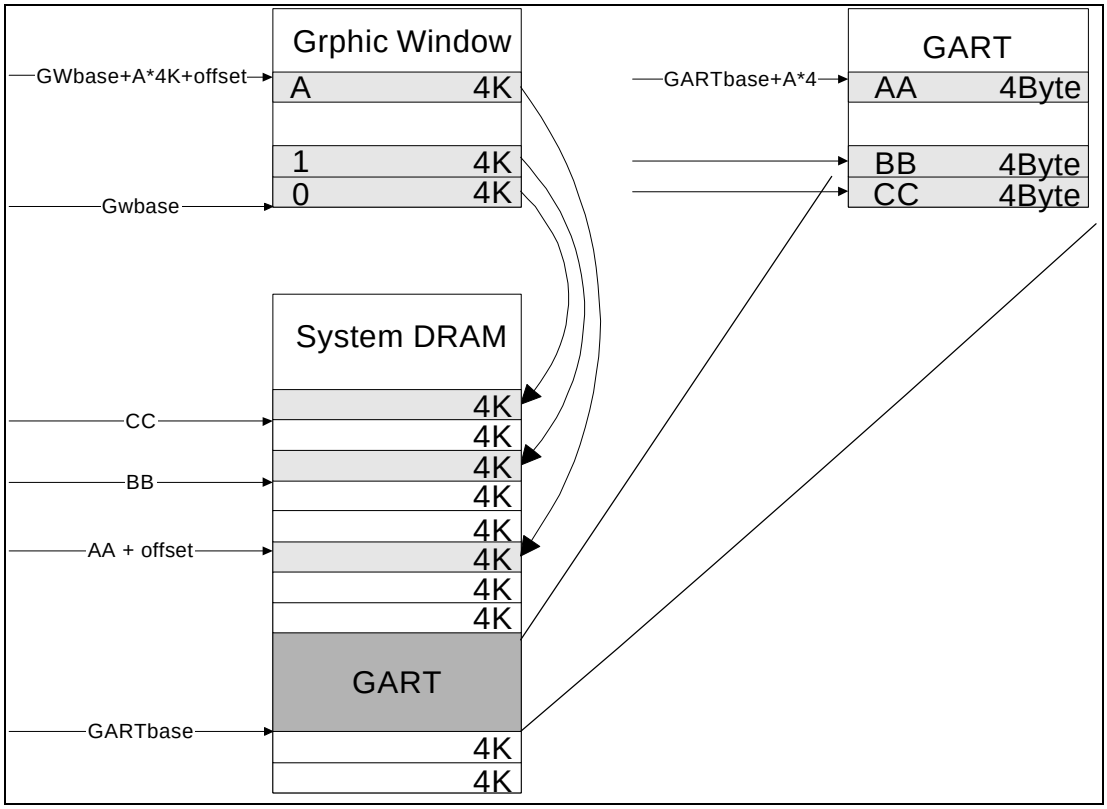


Figure 6.5-1 Graphic Address Re-mapping Function

In order to accelerate graphic window accesses, a page table cache is built in. The page table stores re-mapping relations of the most frequently used pages. It is set-associative with 8 ways and each way has 2 entries. If the page table stores the re-mapping relation of one specific page, then access within this page will directly be translated to the physical address without looking up the GART and be read by the memory controller.

6.6. INTEGRATED GRAPHICS ACCELERATOR

6.6.1. 2D GRAPHICS ACCELERATOR

The 2D graphics engine is an enhanced 1T 64-bit BitBlt Graphics Engine. For 256/32K/64K /16M color graphics modes, the engine supports the following functions:

- 256 raster operations
- Rectangle fill
- Color expansion
- Enhanced Color expansion
- Line-drawing with styled pattern

- NT Fractional Format Line Drawing
- Multiple Scan Line Drawing
- Trapezoid Fill
- Built-in 8x8 pattern registers
- Built-in 8x8 mask registers
- Rectangle Clipping
- Transparent BitBlt

Descriptions of the graphics engine functions are summarized as follows:

Bit Block Transfer (BitBlt)

BitBlt moves a block of data from one location (source) to another location (destination). It is a ternary operation. The operands could be the source data, the destination data, and the brush pattern. There are three different kinds of BitBlt: from the host memory to the display memory, from the display memory to the host memory, and from one location of the display memory to another location of the display memory. In the first two cases, the operation simply uses the "move string instruction" (REP MOVS) to move the source data to the destination to accomplish the BitBlt operation. It is called "CPU-driven BitBlt". In the case of moving from the display memory to the display memory, integrated Graphics Controller could gain the advantage of its advanced engine design to solve the problems of memory overlapping during the block transfers. The only effort is to program the adequate parameters.

BitBlt with Mask

When the BitBlt operation deals with the hatched brush pattern, the programmer just needs to set the monochrome mask into Mask Registers then the engine would handle the complicated process.

Color Expansion

The color expansion is used to expand a monochrome data (one bit per pixel) into a second color format which is n-bit per pixel during a moving operation.

The foreground color and background color is addressed respectively from I/O address 8224h to 8227h and from I/O address 8228h to 822Bh. The font patterns are stored in the pattern registers (I/O address 8300h to 847Fh) or in the off-screen memory called Enhanced Color/Font Expansion. These pattern registers store the monochrome bitmap. The BitBlt engine can expand 3072 pixels at a time. Thus the font-drawing and monochrome bitmap expansion can be easily accomplished.

Enhanced Color Expansion

If the size of a monochrome bitmap is larger than 3072 pixels, there is not enough space in pattern registers to store this bitmap. In this case, the bitmap should be stored in the off-screen display memory instead of the pattern registers. The operation is called Enhanced Color Expansion.

The format written into the off-screen memory of the Enhanced Color Expansion operation is m x n.

Line Drawing

The Bresenham's Line Algorithm is a well popular algorithm in graphics, which is used to draw a line. The drawing line could be either a solid line or a dashed line. To draw a solid line, we must use one solid foreground color. To draw a dashed line, we'll use two colors specified by the foreground and background color registers. There are several registers involved to control the starting location, pixel count and line style, etc.

Rectangle Fill

A rectangle area fill is a function to fill a specified rectangle area by using either a solid color (rectangle fill) or a pattern (pattern fill).

Rectangle Fill is simply to fill the destination rectangle with a solid color. The solid color is specified into the pattern foreground color register.

Pattern Fill repeats a source pattern into a destination rectangle. Therefore the pattern registers must be specified.

Raster Operations (Raster Ops or ROPs)

Raster Ops would perform some logical or arithmetic operations on the graphics data. There are 256 raster ops defined by Microsoft. Each raster op code is a Boolean operation with three operands: the source, the selected pattern, and the destination.

Direct Draw

The Windows 95 Game SDK enables the creation of world class computer games. Direct Draw is a component of that SDK that allows direct manipulation of video display memory. To enhance the performance of games, SiS620 provides some Direct Draw functions.

Since the former engine functions can just support part of Direct Draw capabilities, transparent BitBlt functions are added into the graphics accelerator to meet the other Direct Draw functions. They are color key range comparison, alpha blending, and Direct Draw raster operation. The register format for transparent BitBlt is different from those of the engine's functions listed above.

When transparent BitBlt is enabled, the source and destination data are sent to the color key range comparators to determine whether they are between the high and low color key values. If they are in the color key range, the Direct Draw raster operation (D_Rop) will determine whether the source data after alpha blending or the original destination will be written back to memory.

Turbo Queue in 2D Graphics Engine

The graphics engine performs the acceleration functions as stated in the previous section via the acceleration commands stored in the command queue. The command queue is a FIFO (First In First Out) and ring structure, i.e., if an acceleration command is filled in the last stage of the command queue, then the following acceleration command would be filled in the first stage of the command queue.

Once this command queue is congested, the CPU's request will be pending until the command queue has free space to accept more acceleration commands. This would downgrade the graphics system performance severely. Thus the length of command queue will dominate the performance of the graphics engine.

To lengthen the command queue as long as required, SiS620 provides two different kinds of command queue. The first one is built in SiS620 called Hardware Command Queue. The other one is built in the off-screen display memory, which is called Turbo Queue and patent owned by SiS. The architecture diagram of SiS620 command queue is as follows.

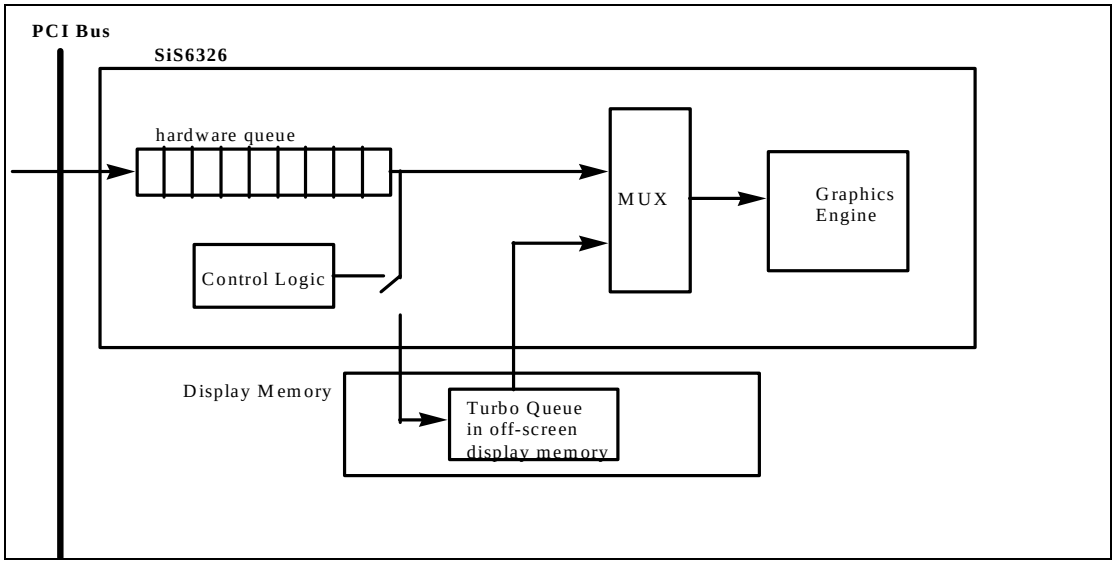


Figure 6.6- 1Block Diagram of Hardware Command Queue

Figure 6.6-1The Hardware Command Queue is a 42 double-words queue. There are 62K Bytes off-screen memory space reserved for the Turbo Queue. Since the average length of an engine command is 8 double-words (which is called 1 stage), therefore the SiS620 command queue could be regarded as infinity stages with Turbo Queue and could get rid of the CPU waiting issue to get extra high performance.

When the hardware command queue is going to be full, the head commands would be moved to the Turbo Queue and left hardware queue space for new commands. The command queue architecture makes the transmission of SiS620 commands most efficient.

The Turbo Queue is also a FIFO and ring structure as stated before. The Turbo Queue base address is generally set to the last 64K Bytes segment on off-screen. To program the extended register SR2C (Turbo Queue Base Address Register) could allocate the Turbo Queue into the off-screen region of the display memory automatically.

6.6.2. 3D GRAPHICS ACCELERATOR

The major technologies for the high performance and high quality 3D rendering in SiS620 are:

- Turbo Queue

- Setup Engine
- Texture Cache
- Pipeline Rendering Engine

Turbo Queue in 3D Accelerator

Using the Turbo Queue architecture (SiS patent) will speedup the rendering for 3D engine. The Turbo Queue length is virtually infinite, therefore 3D driver can issue commands without waiting. To save the high cost for building a long enough hardware command queue, SiS620 allocates a portion of the off-screen memory as the command queue buffer. Once SiS620 detects the status of the internal hardware command queue nearly full, some of the commands in the hardware queue will be temporally swapped to the off-screen area. When 2D or 3D engine finishes previous command, these off-screen commands will be read back first as the next command for execution.

In SiS620 architecture, 2D and 3D engines share the same hardware queue and off-screen command queue but only one engine is active at a time. In this way, we can guarantee a correct execution sequence.

Setup Engine

Setup Engine is one of the most critical parts in the new generation 3D design. It calculates and prepares all of the parameters for primitive drawing. All these computations need more than hundreds of addition, subtraction, multiplication, and division. If we do this setup calculation by host CPU, the sequential coding and processing forms a bottleneck for 3D rendering.

To off-load this computation time from host CPU and to do it in parallel, SiS620 integrates a VLIW-like 32-bit floating point Setup Engine. It can finish all of the setup computations for a triangle within 60 memory clocks. This should be 10 times faster than the computing power from Pentium-200 CPU. Moreover, Setup Engine also supports line and point setup calculations with much less memory clocks than triangle setup required. This Setup Engine, specially designed to fit all the data formats in Microsoft Direct3D API, can accept vertex values directly in floating point format.

Once Setup Engine finishes the setup computations for a triangle, it transfers all these parameters to Render Engine within one memory clock. While Rendering Engine is busying drawing a triangle, Setup Engine can calculate the parameters needed for the next one.

Rendering Engine

Rendering Engine is a pipeline structure engine in SiS620. This engine consists of Shading Engine, Texture Engine and Post Engine.

The output of Shading Engine is a series of pixel color representing the shade of a primitive. Texture Engine is responsible for attaching the texture color on a pixel. Post Engine will do some operations such as fogging, alpha blending, dithering and ROP for this pixel.

To support high quality texture mapping, SiS620 supports point-sampled, linear, Bi-linear and tri-linear texture filtering. With an integrated high-capacity texture cache, SiS620 can render texture pixels in the same fill rate no matter point-sampled, linear, or Bi-linear texture

filtering method is employed. For tri-linear texture mapping, half fill rate is achieved. But better video quality is expected rendering in tri-linear texture mapping mode.

Texture Cache

Texture Cache is one of the critical parts of high performance 3D design. Most of the 3D chips have not built-in texture cache and need to fetch each texture pixel again and again during the rendering process. If the texture is employed for several times, there is no reason to fetch texture from memory again and again. Built-in texture cache could significantly improve texture-mapping performance.

With built-in texture cache, each time when a texture miss happens, a segment of texture will be read from texture buffer and stored in a internal texture cache line. Replacement policy is based on LRU (Least Recently Used) algorithm to optimize the texture cache hit rate. Under Direct3D benchmark, more than 90%-hit rate has been measured. The texture buffer can locate in off-screen area or system memory. If you need very large texture buffer size, the location in system memory is suggested.

6.6.3. VIDEO ACCELERATOR

Video Password/Identification Register

A video registers protection is implemented in the index 80h of CRT index register 3D4. To disable the protection, the software must first match the protection key value of 86h. If not match, read/write to any of the video associated registers are denied.

Multi-format Video Frame Buffer

The video frame buffer of SiS620 is shared with graphics frame buffer and is a multi-format frame buffer. It could accept 16-bpp YUV422, RGB555, and RGB565 color format and 12-bpp YUV420 (plane mode). The decompression CODEC, hardware or software, could fill the valid decompressed video frame data into the off-screen video frame buffer through the PCI local bus. The other PCI motion video card or CPU can transfer the video data through PCI local bus directly into video frame buffer. Then SiS620 would overlay the video on the screen.

YUV420 Plane Mode

SiS620 supports YUV420 plane mode. The data rate of YUV420 is 12-bpp which is smaller than 16-bpp of YUV422. So that the data bandwidth can be reduced and improve the video playback performance. The YUV420 mode needs three start addresses for Y, U and V plane, and two offsets for Y, U and V plane.

Video Playback Line Buffers

When CRT refreshes the screen, the video data must be overlaid with graphics data. Therefore the video data would first be read out from off-screen video frame buffer into the video playback line buffers for further handling. The video playback line buffers serve as buffers between display memory and the playback mechanisms, are provided to fit the limitation of the display memory during video playback operation.

Color Space Conversion & Color Format Conversion

If the data read from the video frame buffer is in YUV422, the real time YUV-to-RGB converter will be turned on. The video data would be converted to RGB888 format for successive processing. The YUV422 are converted to follow the CCIR601-2 standard. If the data read from the video frame buffer is in RGB format, the YUV-to-RGB converter would be bypassed. All the RGB565 and RGB555 format are supported and then would be converted to RGB888 format.

Horizontal Interpolation DDA

The DDA (Digital Differential Accumulator) using the following mathematical calculation with 2-tap, N-phase and scaling up factor UFACT (from J points scaling up to J * UFACT points):

Destination[i] = (1 - Weight") * Source[j] + Weight" * Source[j+1]
j = TRUNC(i / UFACT)
Weight" = TRUNC(i / UFACT) – j

However since the *Weight" is not an integer, the multiplication is hard to implement and therefore the following Weight is used for calculation.

Weight = TRUNC(Weight" * N) / N

The SiS620 builds in an X-interpolation DDA mechanism to get better video stretching quality. The interpolation accuracy of DDA mechanism is 2-tap and 8-phase.

Vertical Interpolation DDA

SiS620 built-in a Y-interpolation DDA mechanism and two line buffers mechanism to get better video stretching quality. The interpolation accuracy of DDA mechanism is 2-tap and 8-phase.

Video Playback Horizontal Zooming

The playback video data can be horizontal zoom-in in 64/n factor (n = 1 ~ 64) and zoom-out in about m/16 factor (m = 1 ~ 16). The zooming factor (HPFACT) is controlled by 4-bit integer part and 6-bit fraction part. The horizontal video size will be zoomed to 1/HPFACT. If HPFACT<1, it will perform horizontal up scaling. If HPFACT>1, it will perform horizontal down scaling.

Video Playback Vertical Zooming

The playback video data can be vertical zoom-in in 64/n factor (n = 1 ~ 64) and zoom-out in arbitrary factor. The zooming factor (VPFACT) is controlled by 6-bit fraction part. The video size will be zoomed to 1/VPFACT. Since the VPFACT is always less than 1, therefore you can only perform vertical up scaling by this factor. The vertical down scaling can be done by multiplying the Video Frame Buffer Offset with an integer I. Then the vertical video size will be zoomed to 1/(I*VPFACT).

Color Keying

A control signal is generated by comparing the 24 bits graphics data to the 24 bits color key low value and 24 bits color key high value. The bit number is dependent on color depth used. If the graphics data value is between the two color key values (all of the three RGB parts), the color key is detected. This comparison mechanism can be disabled by setting the video window size to zero, i.e. X-start=0, X-end=0, Y-start=0, and Y-end=0.

Chroma Keying

A control signal is generated by comparing the 24 bits video data to the 24 bits chroma key low value and 24-bit chroma key high value. The chroma key can be YUV or RGB format. If the video data value is between two chroma key values (all of the three RGB or YUV parts), the chroma key is detected.

Graphics & Video Overlay

The overlay of the graphics data and the video data is performed by color keying and chroma keying method. The overlay operation is set by Key Overlay Operation Mode Register. The operation is defined below:

Table 6.6- 1 Table of Graphics and Video Overlay Operation Mode

OPERATION MODE	OPERATION
0000	Always select graphics data
0001	Select blended data when color key and chroma key, Otherwise select graphics data
0010	Select blended data when color key and not chroma key, Otherwise select graphics data
0011	Select blended data when color key, Otherwise select graphics data
0100	select blended data when not color key and chroma key, otherwise select graphics data
0101	select blended data when chroma key, otherwise select graphics data
0110	select blended data when color key *xor chroma key, otherwise select graphics data
0111	select blended data when color key or chroma key, otherwise select graphics data
1000	select blended data when not color key and not chroma key, otherwise select graphics data

1001	select blended data when color key *xnor chroma key, otherwise select graphics data
1010	select blended data when not chroma key, otherwise select graphics data
1011	select blended data when color key or not chroma key, otherwise select graphics data
1100	select blended data when not chroma key, otherwise select graphics data
1101	select blended data when not color key or chroma key, otherwise select graphics data
1110	select blended data when not color key or not chroma key, otherwise select graphics data
1111	always select blended data

Video Window Control Registers

The video window area is defined by six registers that specify a rectangular region by X-start, X-end, Y-start, and Y-end (X: Horizontal, Y: Vertical). Please refer to " 7.9.2 to 7.9.7". The location of the video window is referred to the VGA sync signals. The size of the video window is defined in VGA pixels and lines.

Video Panning

The displayed video image could be panned around the captured video image by setting the video display starting address, i.e., you may selectively display any part of the captured video image. The vieo display starting address is equal to the video frame buffer starting address adding the panning offset. Please refer to " 7.9.11, 7.9.12 and 7.9.14".

Overlay Memory Data

The display memory is configured to two areas: one is the graphics area (which is the actual screen display area) storing graphics pixel data, and the other is the video area (which is also called off-screen area) storing the video pixel data. In the graphics area, the corresponding video window area is reserved with the color key value. During the CRT scan period, a comparison of graphics data with color key data is performed. Once a match meets, the CRT output path would be switched from graphics path to video path to display the video data.

Video Playback Contrast Enhancement and Brightness Control

To achieve higher video quality, the SiS620 builds in the Contrast Enhancement and Brightness Control mechanism. For Contrast Enhancement, first, the mean value is calculated by some pixels and some frames. The number of sampled pixels and frames is

programmable by registers. Contrast Enhancement mechanism then increases the difference between the video data and mean value. The increasing rate is programmed by gain. The value of gain is frame 1.0 to 1.4375. The Brightness of video data can be controlled. The Brightness is a 2's complement value from -128 to 127. This value is then added with the video data to increase or decrease the brightness of video.

6.6.4. DISPLAY MEMORY INTERFACE

SiS620 supports 2MB/4MB/8MB SDRAM and SGRAM and also supports auto memory size detection.

The DRAM types supported are:

1Mx16 SDRAM

256Kx32 SGRAM

512Kx32 SGRAM

1Mx32 SGRAM

Memory Configuration Pins (For SGRAM & SDRAM)

In 1-bank configuration:

- SCLK would be active.
- CS0# would be active.
- Only DQM[0:3] would be active.
- WE# would be active.
- SRAS* and SCAS* would be active.
- Only MD[0:31] would be active.
- MA[0:11] would be connected to all bank.

In 2-bank configuration:

- SCLK would be active.
- CS0* would be active.
- DQM[0:7] would be active.
- WE* would be active.
- SRAS* and SCAS* would be active.
- MD[0:63] would be active.
- MA[0:11] would be connected to all bank.

In 4-bank configuration:

- SCLK would be active.
- CS0*, CS1* would be active.

- DQM[0:7] would be active.
- WE* would be active.
- SRAS* and SCAS* would be active.
- MD[0:63] would be active.
- MA[0:11] would be connected to all bank.

6.6.5. RESOLUTIONS SUPPORTED

Table 6.6- 2 Table of Resolutions Supported

RESOLUTION	1M BYTE DRAM	2M BYTE DRAM	4M BYTE DRAM
640x480x8	√	√	√
640x480x16	√	√	√
640x480x24	√	√	√
800x600x4	√	√	√
800x600x8	√	√	√
800x600x16	√	√	√
800x600x24	X	√	√
1024x768x4	√	√	√
1024x768x8	√	√	√
1024x768x16	X	√	√
1024x768x24	X	X	√
1280x1024x4	√	√	√
1280x1024x8	X	√	√
1280x1024x16	X	X	√
1600x1200x4	√	√	√
1600x1200x8	X	√	√

Except these real resolution modes, SiS620 also builds in virtual screen mode which could support up to 2048x2048 resolution.

6.6.6. SIGNATURE ANALYSIS

The signature analysis is provided to automatically test the graphics data input to the DAC. This technique is based on the concept of cyclic redundancy checking (CRC) and is implemented in hardware using linear feedback shift registers (LFSRs). It is composed of a 16-bit signature generator register called multiple-input signature register (MISR, shown in the following figure) and is used to ensure a unique signature of different patterns.

For a given test image, the signature analysis could get a right unique signature number. If

an error occurs in the controller or the data manipulation, it would result in a different wrong signature number as compared to the pre-calculated signature value. Thus a test technician could sort the good or bad chips more quickly and accurately and requires no visual inspection of the screen for errors in the mass product environment. This could save significant testing time. If the display screen includes blinking attributes or a blinking cursor, then the signature will be different when blink-off and blink-on for those frames. Assume all error patterns are equally likely, then the probability of failing to detect an error by the MISR is approximately 0.000015.

To match the inputs of MISR, the 24-bit graphics data (i.e. the input of the DAC of the RAMDAC) would be first converted into 16-bit data. The corresponding transfer function of the MISR of the following figure is

$$p(x) = 1 + c_1 \cdot x + c_2 \cdot x^2 + c_3 \cdot x^3 + ... + c_{16} \cdot x^{16}$$

where $c_1, c_2, c_3, ..., c_{16}$ can be either 0 or 1. SiS620 sets the parameters of the signature register as

$$p(x) = 1 + x + x^7 + x^{10} + x^{16}$$

Once the software enables the signature analysis function, SiS620 could test itself intelligently and automatically. This function could also be disabled by the extended control register for power saving purposes.

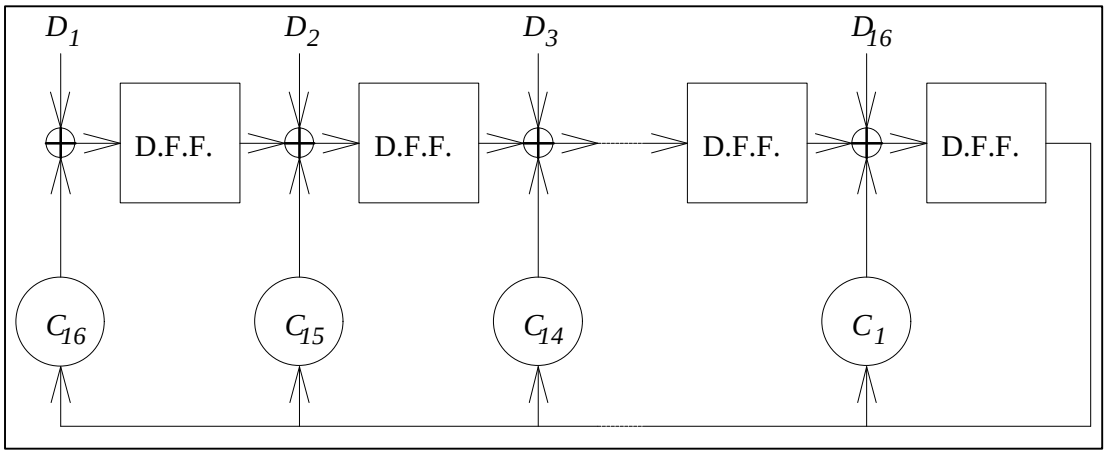


Figure 6.6- 2 Multi-Input Signature Register (MISR)

6.6.7. COMPATIBILITY

The SiS620 is fully compatible with standard IBM VGA modes, EGA, CGA, MDA, and Hercules modes.

6.6.8. SOFTWARE SUPPORT

To fully utilize and support the built-in graphics hardware features, SiS has developed a high-performance VESA extension compliant BIOS.

Extended graphics and text modes are supported by software application drivers developed by SiS. The following applications are currently supported:

- 3D Studio Version 3.0
- AutoCAD/386 Release 11, 12, 13
- Auto Shade/386 Version 2.0
- Microsoft Windows 3.1 & 3.11
- Microsoft Windows 95/98
- Microsoft Windows NT Version 4.0 and 5.0
- OS/2 Presentation Manager 3.0, and 4.0

Video operation is supported by software application drivers developed by SiS. The following applications are currently supported:

- DCI driver
- Direct Draw driver

3D operation are supported by software application drivers developed by SiS. The following applications are currently supported:

- Microsoft Direct3D
- OpenGL in Windows NT 4.0/5.0
- OpenGL in Windows 98
- Renderware for Windows 95/98

6.7. POWER MANAGEMENT

To support power management, SiS620 reports activities related to PCI master and CPU via the BMREQ# pin to SiS5595, where the power management state machine is located. The information contained by BMREQ# can be classified into two categories. The first category is CPU operation and the second category is master operation. Each category occupies different time slot. If BMREQ# is reporting CPU operation in this clock, then BMREQ# will report master operation in the next clock and vice versa. Configuration Register 6Bh of host bridge is used to define what kinds of operations should be reported.

SiS620 may also trap ACPI I/O port accesses to support ACPI S3 and S2 states and to disable system arbiter. Configuration register 68~69h is used to define the ACPI I/O space base address and SiS620 uses this register to trap the ACPI I/O port accesses.

6.7.1. DISPLAY POWER MANAGEMENT

To support the power saving of Green PC, SiS620 supports DPMS (Display Power Management Signaling) proposed by VESA Monitor Committee.

SiS620 has built-in two timers for stand-by and suspend modes respectively. The timers can be programmed with an expiration time from 2 minutes to 30 minutes (in 2 min. increment) via the extended registers. The video subsystem can also be forced to enter stand-by,

suspend, or off modes immediately by blocking HSYNC and/or VSYNC signals to the VGA monitor. The activating events can be the monitoring of keyboard, hardware cursor, and/or video memory read/write cycles. The following table shows the signal activities in different power management states.

Table 6.7- 1 POWER MANAGEMENT

POWER MANAGEMENT STATE	HORIZONTAL SYNC	VERTICAL SYNC	VIDEO DISPLAY
ON	Pulses	Pulses	Yes
Stand-By	No Pulses	Pulses	No
Suspend	Pulses	No Pulses	No
OFF	No Pulses	No Pulses	No

6.8. BALL CONNECTIVITY TESTING

SiS620 provides a NAND chain Test Mode when TEST# is pulled low. To ensure the connections of balls to traces of main board, SiS620 provides a simple way to do connective measurements. An additional 2-input-NAND gate is added into the I/O buffer cells. And, one of inputs of NAND gate is connected to input pin of I/O buffer as test input port in test mode. To monitor the test result at test output port, the output of the NAND gate is connected to the other input of the next NAND gate. Such that, the test result could be propagated and it forms a NAND tree. To adapt to the scheme, all output buffers of SiS620 are changed to bi-direction buffers to accept test signals.

6.8.1. NAND TREE TEST SCHEME

7. REGISTER SUMMARY

7.1. DEVICE 0, FUNCTION 0 (HOST-TO-PCI BRIDGE)

Configuration Space Header

Register Address	Register Name	Default Value	Access type
00~01h	Vendor ID	1039h	RO
02~03h	Device ID	0620h	RO
04~05h	PCI Command Register	0005h	RO R/W
06~07h	PCI Status Register	0210h	RO R/W WC (*)
08h	Revision ID	02h	RO
09h	Programming Interface	00h	RO
0Ah	Sub-Class Code	00h	RO
0Bh	Base Class Code	06h	RO
0Ch	Cache Line Size	00h	RO
0Dh	Master Latency timer	FFh	R/W
0Eh	Header Type	80h	RO
0Fh	BIST	00h	RO
10~13h	Graphic Window Base Address	00000000h	RO R/W
14~33h	Reserved	00h	RO
34h	Capability Pointer	C0h	RO

Note: “WC” stands for Write Clear. If the register‘s access type is WC, that means every write cycles issued to the register can only reset(Write Clear from 1 to 0) each specific bit in this register, but can not set it(write 1 into the corresponding bit). Each bit will be reset whenever the register is written, and the corresponding bit contains “1”. For instance, to write value 0100_0000_0000_0000b to the register will clear bit 14 and the other bits keep the same value.

Registers for Host & DRAM

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
50h	Host Interface Control 1	00h	R/W

51h	Host Interface Control 2	00h	R/W
52h	DRAM MISC control 1	00h	R/W
53h	DRAM Timing control	00h	R/W
54h	DRAM RAS# Timing Control	00h	R/W
55h	DRAM MISC Control 2	00h	R/W
56h	DRAM MISC Control 3	00h	R/W
57h	SDRAM Control	00h	R/W
58h	Reserved	00h	R/O
59h	PCI Buffer Strength and Current Rating	00h	R/W
5Ah~5Fh	DRAM Buffer Strength and Current Rating	00h	R/W
5Bh~5Fh	Reserved	00h	RO
60h~62h	DRAM Type Registers of Bank 0/1	00h	R/W
63h	DRAM Status Register(Bit-x = Bank-x)	FFh	R/W
64h~67h	Reserved	00h	R/O
69h~68h	ACPI I/O Space Base Address Register	0000h	R/W
6Ah	SMRAM Access Control	00h	R/W
6Bh	System Event Monitor control for Power Management	00h	R/W

Shadow RAM & PCI-Hole Area

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
70h~73h	Shadow RAM attribute & Read/Write Control	00000000h	R/W
74h~76h	Reserved	00h	RO
77h	Characteristics of PCI-Hole area	00h	R/W
78h~79h	Allocation of PCI-Hole area #1	0000h	R/W
7Ah~7Bh	Allocation of PCI-Hole area #2	0000h	R/W

Host Bridge & PCI Arbiter Characteristics

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
80h	Target Bridge to DRAM Characteristics	00h	R/W

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
81h	Reserved	00h	RO
82h	PCI Target Bridge Bus Characteristics	00h	R/W
83h	CPU to PCI Characteristics	00h	R/W
84h~85h	PCI Grant Timer	FFFFh	R/W
86h	CPU Idle Timer for PCI	FFh	R/W
87h	Host Bridge & PCI Master Priority Timer	FFh	R/W
88h~89h	PCI Discard Timer	0000h	R/W

Clock Control

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
8Ch	SDRCLK/SDWCLK Control	2Ah	R/W
8Dh	MCLK Control	09h	R/W
8Eh	CPU clock & SDRAM Clock Relationship	00h	R/W

GART and Page Table Registers

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
90h~93h	GART Base Address	00000000h	R/W
94h	Graphic Window Control	00h	R/W
95h~96h	Reserved	00h	RO
97h	Page Table Cache Control	00h	R/W
98h	Page Table Cache Invalidation Control	00h	R/W

Integrated VGA Control

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
9Ch	Integrated VGA Control	00h	R/W

A.G.P.

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
C0h~C3h	A.G.P. Capability Identify Register	00200002h	RO
C4h~C7h	A.G.P. Status Register	1F000203h	RO

C8h~CBh	A.G.P. Command Register	00000000h	R/W

7.2. DEVICE 2, FUNCTION 0 (VIRTUAL PCI-TO-PCI BRIDGE)

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
00-01h	Vendor ID	1039h	RO
02-03h	Device ID	0001h	RO
04-05h	PCI Command Register	0000h	RO R/W
06-07h	PCI Status Register	0000h	RO
08h	Revision ID	00h	RO
09h	Programming Interface	00h	RO
0Ah	Sub-Class Code	04h	RO
0Bh	Base Class Code	06h	RO
0Ch	Cache Line Size	00h	RO
0Dh	Master Latency timer	00h	RO
0Eh	Header Type	01h	RO
0Fh	BIST	00h	RO
19h	Secondary Bus Number	00h	R/W
1Ah	Subordinate Bus Number	00h	R/W
1Bh	Secondary Master Latency Timer	00h	R/W
1Ch	I/O Base	F0h	R/W RO
1Dh	I/O Limit	00h	R/W RO
1Eh	Secondary PCI-PCI Status	0000h	R/W RO
20~21h	Non-prefetchable Memory Base Address	FFF0h	R/W RO
22~23h	Non-prefetchable Memory Limit Address	0000h	R/W RO
24~25h	Prefetchable Memory Base Address	FFF0h	R/W RO

26~27h	Prefetchable Memory Limit Address	0000h	R/W RO
28~3Dh	Reserved		
3Eh	PCI to PCI Bridge Control	0000h	RW RO

7.3. PCI IDE DEVICE

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
00-01h	Vendor ID	1039h	RO
02-03h	Device ID	5513h	RO
04-05h	PCI Command Register	0000h	RO R/W
06-07h	PCI Status Register	0000h	RO
08h	Revision ID	D0h	RO
09h	Programming Interface	00h	RO
0Ah	Sub-Class Code	01h	RO
0Bh	Base Class Code	01h	RO
0Ch	Cache Line Size	00h	RO
0Dh	Master Latency timer	00h	RO
0Eh	Header Type	80h	RO
0Fh	BIST	00h	RO
10h~13h	Primary Channel Command Block Base Address Register	00000000h	R/W
14h~17h	Primary Channel Control Block Base Address Register	00000000h	R/W
18h~1Bh	Secondary Channel Command Block Base Address Register	00000000h	R/W
1Ch~1Fh	Secondary Channel Control Block Base Address Register	00000000h	R/W
20h~23h	Bus Master IDE Control Register Base Address	00000000h	R/W
24h~2Bh	Reserved		
2Ch~2Dh	Subsystem Vendor ID	0000h	R/W

2Eh~2Fh	Subsystem ID	0000h	R/W
30h~33h	Expansion ROM Base Address	00000000h	R/W
40h	IDE Primary Channel/Master Drive Data Recovery Time	00h	R/W
41h	IDE Primary Channel/Master Drive Data Active Time	00h	R/W
42h	IDE Primary Channel/Slave Drive Data Recovery Time	00h	R/W
43h	IDE Primary Channel/Slave Drive Data Active Time	00h	R/W
44h	IDE Secondary Channel/Master Drive Data Recovery Time	00h	R/W
45h	IDE Secondary Channel/Master Drive Data Active Time	00h	R/W
46h	IDE Secondary Channel/Slave Drive Data Recovery Time	00h	R/W
47h	IDE Secondary Channel/Slave Drive Data Active Time	00h	R/W
48h	IDE Status Register	00h	R/W
49h	Reserved		
4Ah	IDE General Control Register 0	00h	R/W
4Bh	IDE General Control Register 1	00h	R/W
4Ch~4Dh	Prefetch Count of Primary Channel	FFFFh	R/W
4Eh~4Fh	Prefetch Count of Secondary Channel	FFFFh	R/W
50h~51h	IDE minimum accessed time register	0000h	R/W
52h	IDE Miscellaneous Control Register	00h	R/W

8. REGISTER DESCRIPTION –CORE LOGIC

The SiS620 has three programmer visible registers located in the I/O space. These registers are listed in the following.

I/O SPACE ADDRESS	CONFIGURATION REGISTER FUNCTION
0CF8h	CONFIG_ADDRESS register (only valid for DWord access)
0CFCh	CONFIG_DATA register (only valid if enable bit is set in the CONFIG_ADDRESS register)

8.1. HOST BRIDGE REGISTERS (FUNCTION 0)

8.1.1. CONFIGURATION SPACE HEADER

Register 00h Vendor ID

Default Value: 1039h

Access: Read Only

The register identifies the manufacturer of the device. SiS is allocated as 1039h by PCI SIG.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Vendor Identification Number**

Register 02h Device ID

Default Value: 0620h

Access: Read Only

The device identifier is allocated as 0620h by Silicon Integrated Systems Corp.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Device Identification Number**

Register 04h Command

Default Value: 0005h

Access: Read/Write, Read Only

The Command register provides coarse control over a device's ability to generate and respond to PCI cycles.

BIT	ACCESS	DESCRIPTION
15:3	RO	**Reserved**
2	RO	**Bus Master** Default value is 1. That means you cannot disable bus master function of the host bridge.

1	R/W	**Memory Space** The bit controls the response to memory space accesses. When the bit is disabled, the host bridge ignores all access from PCI masters. 0: Disable 1: Enable
0	RO	**I/O Space** Default value is 1. The host bridge only respond to the addresses 0CF8h and 0CFCh in the I/O space and the I/O transaction must be generated by the host bridge itself.

Register 06h Status

Default Value: 0210h

Access: Read/Write, Read Only, Write Clear

The Status register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that each bit in this register can only be reset(Write Clear from 1 to 0), but not set. Each bit will be reset whenever the register is written, and the corresponding bit contains "1". For instance, to write value 0100_0000_0000_0000b to the register will clear bit 14 and not affect any other bits.

BIT	ACCESS	DESCRIPTION
15:14	RO	**Reserved** This bit is always 0, SiS620 does not support parity checking on the PCI bus.
13	WC	**Received Master Abort** This bit is set by SiS620 whenever its transaction is terminated with master abort. This bit is cleared by writing a 1 to it.
12	WC	**Received Target Abort.** This bit is set by SiS620 whenever it terminates a transaction with target abort. This bit is cleared by writing a 1 to it.
11	RO	**Reserved**
10:9	RO	**DEVSEL# Timing DEVT.** These two bits define the timing to assert DEVSEL#. SiS620 always asserts DEVSEL# within two clocks after the assertion of FRAME#.
8:5	RO	**Reserved**
4	RO	**CAP_LIST** The value of "1" for this bit specifies SiS620's configuration space implements a list of capabilities.
3:0	RO	**Reserved**

Register 08h Revision ID

Default Value: 02h

Access: Read Only

The Revision ID is 02h for A2 Revision.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Revision Identification Number**

Register 09h Programming Interface

Default Value: 00h

Access: Read Only

The default value is 00h since no specific register-level programming interface is provided.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Programming Interface**

Register 0Ah Sub Class Code

Default Value: 00h

Access: Read Only

The Sub Class Code is 00h for host bridge.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Sub Class Code**

Register 0Bh Base Class Code

Default Value: 06h

Access: Read Only

The value of 06h in this field identifies a bridge device.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Base Class Code**

Register 0Ch Cache Line Size

Default Value: 00h

Access: Read Only

The value of this register is always 00h since the host bridge won't generate the Memory Write and Invalidate command.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Cache Line Size**

Register 0Dh Master Latency Timer (MLT)

Default Value: FFh

Access: Read/Write

The MLT is used in conjunction with PGT(Register84h) and CIT(Register 86h) to provide a fair and efficient system arbitration mechanism. The value of MLT guarantees the minimum system bandwidth for CPU when CPU and PCI masters are all craving for system resources(system memory or PCI bus).

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Initial Value for Master Latency Timer** Power-on default value is FFh but we recommend you to set its value to 20h. Unit: PCI clock

Register 0Eh Header Type

Default Value: 80h

Access: Read Only

The value of 80h implies that SiS620 is a multiple function device.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Header Type**

Register 0Fh BIST

Default Value: 00h

Access: Read Only

The value is 00h since we don't support Build-in Self Test.

BIT	ACCESS	DESCRIPTION
7:0	RO	**BIST**

Register 10h Graphic Window Base Address (GWBA)

Default Value: 00000000h

Access: Read/Write, Read Only

The register defines the starting address of the graphic window for A.G.P. Accessibility and effectiveness of this register is controlled by the Graphic Window Control Register(Register 94h).

BIT	ACCESS	DESCRIPTION
31:22	R/W RO	**Define A[31:22] of Graphic window base address** The accessibility of bits[31:22] are controlled by graphic window size(Bits[6:4], Register 94h).

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Size
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	4M
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	8M
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	16M
R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	32M
R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	0	64M
R/W	R/W	R/W	R/W	R/W	0	0	0	0	0	128M
R/W	R/W	R/W	R/W	0	0	0	0	0	0	256M

21:0	RO	**Reserved and read as 000000h**

Register 34h Capability Pointer (CAPPTR)

Default Value: C0h

Access: Read Only

The value of C0h indicates that the A.G.P. standard register block is started from Register C0h.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Capability Pointer** Pointer to the Start of A.G.P. standard register block.

8.1.2. HOST CONTROL REGISTERS

Register 50h Host Bus Interface Control I

Default Value: 00h

Access: Read/Write

This register defines the functions supported by the Host interface.

BIT	ACCESS	DESCRIPTION
7:4	R/W	**Reserved**

3	R/W	**CPU & PCI Masters Concurrently Access Memory Function** When this bit is enabled, CPU access memory cycles and PCI masters access memory cycles can be concurrently issued onto host bus and PCI bus, respectively, and then the memory access cycles will be rearranged by SiS620 to memory sequentially. In this case, the utilization of the buses will be optimized. When this bit is disabled, either CPU or PCI masters starts memory access cycle will block the other one' s cycle until the current cycle is finished. 0: Disable 1: Enable
2	R/W	**CPU & PCI Masters Concurrently Access PCI Bus Function** When this bit is enabled, CPU access PCI bus cycle and PCI masters access memory cycles can be concurrently issued onto host bus and PCI bus, respectively. By doing this, these cycles will be forwarded to PCI bus and memory bus at the same time. This bit is valid only bit 3 is set. When this bit is disabled, either one of these two kinds of cycles will block the other until the current cycle is finished. 0: Disable 1: Enable
1	R/W	**CPU Pipeline Function** When this bit is 0, only one pending cycle is allowed at one time. When this bit is 1, there might be more than two pending cycles at one time depends on the CPU behavior. 0: no pipeline 1: pipeline enable
0	R/W	**Reserved**

Register 51h Host Bus Interface Control II

Default Value: 00h

Access: Read/Write

This register defines the functions supported by the Host interface.

BIT	ACCESS	DESCRIPTION
7:2	R/W	**Reserved**

1	R/W	**Host-to-PCI Cycle Timing Control** When set to 1, the Host-to-PCI bridge will start the transaction of Host-to-PCI cycle once the cycle appears on the host bus. When set to 0, the start of the Host-to-PCI translation will be delayed by one CPU clock. 0: Delay 1 CPU clock 1: Without Delay
0	R/W	**Host-to-Memory Cycle Lead-off Time Control** When set to 1, the host controller will start the translation of Host-to-Memory access cycle once the cycle appears on the host bus. The resulting Lead-off time for memory access cycle will be 8T. When set to 0, the start of translation will be delayed one CPU clock and the resulting Lead-off time is 9T. 0: Lead-off time = 9T 1: Lead-off time = 8T

8.1.3. DRAM CONTROL REGISTERS

Register 52h DRAM MISC Control 1

Default Value: 00h

Access: Read/Write

The register defines timing for Refresh cycles.

BIT	ACCESS	DESCRIPTION
7:6	R/W	**Refresh Queue Depth** Bits[2:1] control the depth of refresh queue. To minimize the performance penalty caused by refresh cycles, the concept of refresh queue is introduced. Refresh request is arbitrated with other DRAM request, if a refresh request does not get served, it enters the refresh queue. The priority of refresh request is promoted to highest when the refresh queue is full. **Bits[2:1] Depth** 00 0 01 4 10 8 11 12

5:4	R/W	**DRAM Refresh Period Control** This bit is used to test internal refresh circuit. For normal operation, it must be programmed with 0. 0 0: 15.6us 0 1: 7.8us 1 0: 3.9us 1 1: Reserved
2	R/W	**Refresh Mode Control**
1	R/W	**DRAM Refresh Test Mode** This bit is used to test internal refresh circuit. For normal operation, it must be programmed with 0. 0: Normal Mode 1: Test Mode
0	R/W	**Refresh Enable**

Register 53h DRAM Timing Control

Default Value: 00h

Access: Read/Write

This register controls the paging prediction options for various cycles.

BIT	ACCESS	DESCRIPTION
7:6	R/W	**Starting Point of Paging Function** These bits control when to perform RAS# precharge cycle after each DRAM transaction is finished and there is no any DRAM cycle pipelined. **Bits[7:6]** **Delay** 00 1T 01 2T 10 4T 11 8T
5	R/W	**Always Paging after Write DRAM Cycles** Bit[5:3] define what kind of DRAM access cycles will implement Paging function, and the timing to issue paging cycle is defined in bits[7:6]. 0: Disable 1: Enable

4	R/W	**Always Paging after Data Read DRAM Cycles** 0: Disable 1: Enable
3	R/W	**Always Paging after Code Read DRAM Cycles** 0: Disable 1: Enable
2:1	R/W	**Reserved.**
0	R/W	**Page Hit Control** 0: Normal Operation 1: Always Page Miss

Register 54h DRAM RAS# Timing Control

Default Value: 00h

Access: Read/Write

This register controls the RAS# timing for SDRAM.

BIT	ACCESS	DESCRIPTION
7:6	R/W	**RAS Active Time** Bits[7:6] defines the RAS# pulse width for refresh cycles **Bits[7:6] Pulse Width** 00 4T 01 5T 10 6T 11 7T
5:4	R/W	**RAS# Precharge Time** **Bits[5:4] Description** 00 2T 01 3T 10 4T 11 5T

3:2	R/W	**RAS to CAS Delay** **Bits[5:4] Description** 00 2T 01 3T 10 4T 11 5T
1:0	R/W	**Reserved**

Register 55h DRAM MISC Control 2

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	R/W	**Reserved**
5	R/W	**Turn Around Time Control between SDRAM Read and Write Cycles** This bit is used to control memory data bus (MD) turn around time between two consecutive SDRAM read and write cycles. The turn around time in normal condition should be 1T. For certain SDRAMs that will not halt the driving of MD in time, the turnaround time will be 2T to avoid contention. 0: Normal 1: Faster
4	R/W	**SDRAM RAS# Precharge Time Control** When this bit is enabled, SiS620 will optimize the RAS# precharge time by comparing the memory address of every consecutive DRAM cycles to check whether the addresses are located at the same row or not. If the cycles are destined to the same row, the minimum RAS# precharge time for SDRAM should be met before issuing a row active command. However, if they are destined to the different rows, the RAS# precharge time is met automatically, and row active command can be issued immediately. 0: Disable 1: Enable
3:2	R/W	**Reserved**
1	R/W	**Lead-off Time Control for DRAM Read Cycles** 0:Normal 1:Slow

0	R/W	**Reserved**

Register 56h DRAM MISC Control 3

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	R/W	**Reserved**
3	R/W	**SDRAM Initialization Mode Selection** This bit controls whether the command specified in register 57h bits[7:5] should be issued to one row only or to all rows. If this bit is 0, the DRAM Status Register (Register 63h) decides which row the command should be issued to. 0: One Row 1: All Rows
2:0	R/W	**Reserved**

Register 57h SDRAM Control

Default Value 00h

Access Read/Write

This register controls SDRAM initialization process and timing.

BIT	ACCESS	DESCRIPTION
7	R/W	**Precharge Command** When this bit is set, SiS620 will issue precharge command to SDRAM. This bit is automatically cleared after the precharge command is completed. 0: Disable 1: Enable
6	R/W	**Mode Register Set Command** When this bit is set, SiS620 will issue mode register setting command to SDRAM. This bit is automatically cleared after the mode register setting command is completed. 0: Disable 1: Enable

5	R/W	**Refresh Command** When this bit is set, SiS620 will issue refresh command to SDRAM. This bit is automatically cleared after the refresh command is completed. 0: Disable 1: Enable
4	R/W	**CAS# Latency (CL) Setting** This bit contains the information for SDRAM initialization procedure. 0: 2T 1: 3T
3	R/W	**SDRAM Write Retire Rate** This bit controls the timing that SiS620 writes data into SDRAM during burst cycles. 0: X-2-2-2 1: X-1-1-1
2	R/W	**Reserved**
1	R/W	**SDRAM Multi-bank Function control** When this bit is enabled, SiS620 supports the SDRAM internal multi-bank function up to 4 internal banks. 0: Disable 1: Enable
0	R/W	**NOP Command** When this bit is set, SiS620 will issue NOP command to SDRAM. This bit is automatically cleared after the NOP command is completed. 0: Disable 1: Enable

Register 59h PCI Buffer Strength and Current Rating

Default Value: 00h

Access: Read/Write

This register controls the buffer strength of PCI bus related signals.

BIT	ACCESS	DESCRIPTION
7:2	R/W	**Reserved**

1	R/W	**AD[31:0] Current Rating** This bit controls the buffer strength of AD[31:0] on PCI bus. 0: 4mA 1: 8mA
0	R/W	**PCI Control Signals Current Rating** This bit controls the buffer strength of FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, C/BE[3:0]# and GNT[2:0]#. 0: 4mA 1: 8mA

Register 5Ah Memory Buffer Strength and Current Rating

Default Value: 00h

Access: Read/Write

This register controls the buffer strength of DRAM related signals.

BIT	ACCESS	DESCRIPTION
7	R/W	**CSA[5:0]# Driving Rate** 0: Weak 1: Strong
6	R/W	**CSB[5:0]# Driving Rate** 0: Weak 1: Strong
5	R/W	**DQM[7:0]# Driving Rate** 0: Weak 1: Strong
4	R/W	**CKE Driving Rate** 0: Weak 1: Strong
3	R/W	**MA[14:0] Driving Rate** 0: Weak 1: Strong
2	R/W	**SRAS#/SCAS# Driving Rating** 0: Weak 1: Strong

1	R/W	**WE# Driving Rating** 0: Weak 1: Strong
0	R/W	**MD[63:0] Driving Rating** 0: Weak 1: Strong

Register 60h/61h/62h for bank x=0..2 DRAM Type Registers

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	R/W	**Reserved**
5	R/W	**DRAM Configuration Selection** 0: Single side 1: Double side
4	R/W	**Reserved**
		RAM Type Selection 0000: 1x11x8(1M) 0001: 1x13x8(4M) 0010: 2x12x8(4M) 0011: 2x13x8(8M) 0100: 1x11x9(2M) 0101: 1x13x9(8M) 0110: 2x12x9(8M) 0111: 2x13x9(16M) 1000: 1x11x10(4M) 1001: 1x13x10(16M) 1010: 2x12x10(16M) 1011: 2x13x10(32M) 1100: 2x11x8(2M) Others: Reserved

Register 63h DRAM Status Register (bit-x =bank-x)

Default Value: FFh

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Reserved**
6	R/W	**Shared Memory Control** 0: Disable 1: Enable

5:4	R/W	**Shared Memory Size** **Bits[5:4]** **Size** 00 1M 01 2M 10 4M 11 8M
3	R/W	**Reserved**
2	R/W	**DRAM Bank2 Status** 0: Absent 1: Installed
1	R/W	**DRAM Bank1 Status** 0: Absent 1: Installed
0	R/W	**DRAM Bank0 Status** 0: Absent 1: Installed

8.1.4. POWER MANAGEMENT

Register 68h ACPI I/O Space Base Address Register

Default Value: 0000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:5	R/W	**A[15:5] for ACPI I/O Space base Address** This register provides A[15:5] for the start address of the ACPI I/O space.
4:3	R/W	**Reserved**
2	R/W	**A.G.P. Request Enable** This bit controls the A.G.P. request during ACPI cycles. When this bit is disabled, SiS620 does not accept any AGP request during ACPI cycles. 0: Disable 1: Enable
1	R/W	**Reserved**

0	R/W	**Validity Bit** If this bit is set to 1, the base address contained in Bit[15:5]is in valid. Otherwise the base address defined in Bit[15:5] is ignored. 0: Invalid 1: Valid

Register 6Ah SMRAM Access Control Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	R/W	**SMRAM Area Re-mapping Control** This field controls how the address in the host bus is mapped to the system memory address when the SMARM access control bit is enabled or CPU is in the system management mode. **Bits[7:6] Host Address System Memory Address** 00 E0000h~E7FFFh E0000h~E7FFFh (32K) 01 E0000h~E7FFFh A0000h~A7FFFh (32K) 10 E0000h~E7FFFh B0000h~B7FFFh (32K) 11 A0000h~AFFFFh A0000h~AFFFFh (64K)
5	R/W	**Reserved**
4	R/W	**SMRAM Access Control** When this bit is enabled, SMRAM area can be used even when SMIACT# is not asserted, this function is mainly used for SMRAM initialization by BIOS. When this bit is disabled, SMRAM area can only be accessed during the SMI handler. 0: Disable 1: Enable
3:0	R/W	**Reserved**

Register 6Bh System Event Monitor Control for Power Management

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Monitoring A.G.P. I/O Access** When this bit is enabled, any I/O access from CPU to A.G.P. will be reported to the south bridge via BM_REQ# if the address of the cycle is defined within the range of base address register. 0: Disable 1: Enable
6	R/W	**Monitoring A.G.P. Non-prefetchable Memory Access** When this bit is enabled, any memory access from CPU to A.G.P. non-prefetchable memory area will be reported to the south bridge via BM_REQ#. When this bit is disabled, the memory accesses from CPU to A.G.P. non-prefetchable memory area won't be reported. 0: Disable 1: Enable
5	R/W	**Monitoring A.G.P. Prefetchable Memory Access** When this bit is enabled, any memory access from CPU to A.G.P. prefetchable memory area will be reported to the south bridge via BM_REQ#. When this bit is disabled, the memory accesses from CPU to A.G.P. prefetchable memory area won't be reported. 0: Disable 1: Enable
4	R/W	**Monitoring VGA Compatible IO Access toward A.G.P.** When this bit is enabled, any VGA compatible I/O access(3B0h ~ 3BBh, 3C0 ~ 3DFh) toward A.G.P. will be reported to the south bridge via BM_REQ#. When this bit is disabled, VGA compatible I/O accesses from CPU to A.G.P. won't be reported. 0: Disable 1: Enable
3	R/W	**Monitoring VGA Compatible Memory Access toward A.G.P.** When this bit is enabled, any VGA compatible memory access(A0000h~BFFFFh) toward A.G.P. will be reported to the south bridge via BM_REQ#. When this bit is disabled, VGA compatible I/O accesses from CPU to A.G.P. won't be reported. 0: Disable 1: Enable

2	R/W	**Monitoring A.G.P. Bus Master Activity** When this bit is enabled, any A.G.P. bus master activity will be reported to the south bridge via BM_REQ#. When this bit is disabled, No bus master activity will be reported. 0: Disable 1: Enable
1:0	R/W	**Reserved**

Register 6Ch DRAM Self-Refresh Control for Power Management

Default Value: 00h

Access: Read/Write

This register controls ACPI sleep states supported by SiS620 and CKE behavior.

BIT	ACCESS	DESCRIPTION
7	R/W	**ACPI S3 State Support** 0: Disable 1: Enable
6	R/W	**ACPI S2 State Support** 0: Disable 1: Enable
5	R/W	**CKE Output Enable Control** When enabled, SiS620 drivers CKE. When disabled, SiS620 floats its CKE output. 0: Disable 1: Enable
4	R/W	**CKE Selection** This bit is controlled by BIOS during power management mode, and is only valid when the CKE Output Enable Control bit is enabled. When set to 1, SiS620 always drives CKE to low. When set to 0, SiS620 drivers CKE to low only when it enters self-refresh mode (S2 or S3 state and stop grant cycle issued) 0: Normal Mode 1: Force Low

3:0		**CKE Timing Control** These bits control the timing of CKE. When the value of this field is 0000, CKE is driven out from flip-flop, otherwise, it is driven out from combinational logic. Various delay options are provided to ensure that CKE can meet SDRAM setup time and hold time specification when CKE is driven out from combinational logic. **Bits** **Description** 0000 Flip-flop Output 0001 Delay 2ns 0010 Delay 3ns 0011 Delay 4ns 0100 Delay 5ns 0101 Delay 6ns 0110 Delay 7ns 0111 Delay 8ns 1000 Delay 9ns 1001 Delay 10ns 1010 Delay 11ns 1011 Delay 12ns 1100 Delay 13ns 1101 Delay 14ns 1110 Delay 1ns 1111 No Delay

8.1.5. SHADOW RAM AREA

Register 70h Shadow RAM Read Attribute Control
This register defines the read accessiblity of each shadow RAM region

BIT	ACCESS	DESCRIPTION
15	R/W	**Shadow RAM Enable for PCI Master Access** When this bit is enable, accesses from PCI masters toward shadow RAM area is allowed. 0: Disable 1: Enable
14:13	R/W	**Reserved**

12	R/W	**Read accessibility of Shadow Region F0000h~FFFFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
11	R/W	**Read accessibility of Shadow Region EC000h~EFFFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
10	R/W	**Read accessibility of Shadow Region E8000h~EBFFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
9	R/W	**Read accessibility of Shadow Region E4000h~E7FFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
8	R/W	**Read accessibility of Shadow Region E0000h~E3FFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
7	R/W	**Read accessibility of Shadow Region DC000h~DFFFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
6	R/W	**Read accessibility of Shadow Region D8000h~DBFFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
5	R/W	**Read accessibility of Shadow Region D4000h~D7FFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
4	R/W	**Read accessibility of Shadow Region D0000h~D3FFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.

3	R/W	**Read accessibility of Shadow Region CC000h~CFFFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
2	R/W	**Read accessibility of Shadow Region C8000h~CBFFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
1	R/W	**Read accessibility of Shadow Region C4000h~C7FFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
0	R/W	**Read accessibility of Shadow Region C0000h~C3FFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.

Register 72h Shadow RAM Write Attribute Control

BIT	ACCESS	DESCRIPTION
15:13	R/W	**Reserved**
12	R/W	**Write Accessibility of Shadow Region F0000h~FFFFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
11	R/W	**Write Accessibility of Shadow Region EC000h~EFFFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
10	R/W	**Write Accessibility of Shadow Region E8000h~EBFFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
9	R/W	**Write Accessibility of Shadow Region E4000h~E7FFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.

8	R/W	**Write Accessibility of Shadow Region E0000h~E3FFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
7	R/W	**Write Accessibility of Shadow Region DC000h~DFFFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
6	R/W	**Write Accessibility of Shadow Region D8000h~DBFFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
5	R/W	**Write Accessibility of Shadow Region D4000h~D7FFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
4	R/W	**Write Accessibility of Shadow Region D0000h~D3FFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
3	R/W	**Write Accessibility of Shadow Region CC000h~CFFFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
2	R/W	**Write Accessibility of Shadow Region C8000h~CBFFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
1	R/W	**Write Accessibility of Shadow Region C4000h~C7FFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
0	R/W	**Write Accessibility of Shadow Region C0000h~C3FFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.

8.1.6. PCI HOLE AREA

Register 77h Characteristics of PCI-Hole Area

Default Value: 00h

Access: Read/Write

This register controls the PCI Hole area support. When ACPI hole area is enabled, a cycle with the address located within the PCI hole area will be forwarded to PCI bus.

BIT	ACCESS	DESCRIPTION
7:3	R/W	**Reserved**
2	R/W	**PCI-Hole Area I Enable** 0: Disable 1: Enable
1	R/W	**Reserved**
0	R/W	**PCI-Hole Area II Enable** 0: Disable 1: Enable

Register 78h Allocation of PCI-Hole Area #1

Default Value: 0000h

Access: Read/Write

Register 78h and 79h define the size and the base address of the first PCI-Hole area.

BIT	ACCESS	DESCRIPTION
15:13	R/W	**Size of PCI-Hole Area I (within 512 Mbytes)** **Bits[7:5]** **Size** 000 64KB 001 128KB 010 256KB 011 512KB 100 1MB 101 2MB 110 4MB 111 8MB
12:0	R/W	**Base Address of PCI-Hole Area I** This field specifies A[28:16] for the base address of the PCI-Hole area.

Register 7Ah Allocation of PCI-Hole Area #2

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:13	R/W	**Size of PCI-Hole Area II (within 512 Mbytes)** **Bits[7:5]** **Size** 000 64KB 001 128KB 010 256KB 011 512KB 100 1MB 101 2MB 110 4MB 111 8MB
12:0	R/W	**Base Address of PCI-Hole Area II** This field specifies A[28:16] for the base address of the PCI-Hole area.

8.1.7. TARGET BRIDGE CHARACTERISTICS

Register 80h Target Bridge to DRAM Characteristics

Default Value: 00h

Access: Read/Write

This register controls the characteristics for PCI target bridge to access DRAM.

BIT	ACCESS	DESCRIPTION
7:5	R/W	**Address Boundary Alignment for PCI Bursting** This field controls the alignment of address boundaries. For SiS620, a master-generated PCI burst cycle can never across any address boundary defined by this field. If a cycle is trying to across an address boundary for a memory burst transaction, SiS620 will terminate this transaction with disconnect immediately. **Bits[7:5] Boundary Alignment** 000 256 Bytes 001 512 Bytes 010 1K Bytes 011 2K Bytes 100 4K Bytes Others reserved
4:0	R/W	**Reserved**

Register 82h Target Bridge Characteristics

Default Value: 00h

Access: Read/Write

This register controls the characteristics for PCI target bridge.

BIT	ACCESS	DESCRIPTION
7	R/W	**Reserved**
6	R/W	**PCI Master Write Cycle Following Read Cycle Pipeline Control** When this bit is disabled, any PCI master write cycle won't be issued to the addressed target only after PCI read FIFO is empty. In this case, there are wait states asserted between the target executes two consecutive PCI read cycle and PCI write cycle. When this bit is enabled, PCI write cycles will be generated to the addressed target right after the previous PCI read cycle, independent of the PCI read FIFO status. 0: Disable 1: Enable

5	R/W	**PCI Memory Read Line or Memory Read Multiple Command Prefetch Enable** This bit controls whether or not SiS620 prefetch data for Memory Read Line or Memory Read Multiple command. 0: Disable 1: Enable
4	R/W	**PCI Memory Read Command Prefetch Enable** This bit controls whether or not SiS620 prefetch data for Memory Read command. 0: Disable 1: Enable
3:2	R/W	**Initial Latency Control** This field controls the target initial latency of the target bridge. If SiS620 is unable to assert TRDY# for a transaction within the target initial latency defined by this field, SiS620 asserts STOP# to retry this cycle. 00: Disable 01: 16 PCI Clocks 10: 24 PCI Clocks 11: 32 PCI Clocks
1	R/W	**Subsequent Latency Control** When this bit is enabled, SiS620 terminates a transaction with STOP# if it fails to assert TRDY# for the subsequent block within 8 clocks. 0: Disable 1: Enable
0	R/W	**PCI Memory Read Multiple Lines Control** This bit is only valid whenever PCI master memory read prefetch function is enabled, which function is controlled by Register 82h bits[5:4]. When this bit is 0, one more pending memory read prefetch cycle will be issued by SiS620 for PCI masters; When this bit is 1, two more pending memory read prefetch cycles can be generated. 0: 1 more pending cycle 1: 2 more pending cycles

Register 83h CPU to PCI Characteristics and Arbitration Option

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	R/W	**Reserved**
5	R/W	**PGT & PDT Test Mode** 0: Disable 1: Enable
4	R/W	**Lock Control** When this bit is enabled, SiS620 converts a 64-bit memory cycle on host bus to 2 locked 32-bit memroy read cycles on PCI bus.SiS620 also issues locked cycles on PCI bus on behalf of CPU. When this bit is disabled, SiS620 never asserts Lock# on PCI bus. 0: Disable 1: Enable
3	R/W	**CPU Involved Arbitration on PCI** PGT(Register 84h), CIT(Register 86h) and MLT(Register 0Dh) can only take effect when this bit is enabled. When this bit is enabled, SiS620 doesn't block CPU from operation longer than the period defined by PGT to serve PCI masters, and minimum access time for CPU is guaranteed by MLT. 0: Disable 1: Enable
2	R/W	**Non-Post Cycle Retry Behavior Control** When this bit is 1, if retry occurs from any kind of CPU to PCI non-post cycles, SiS620 won't back off CPU immediately, but tries to issue one more retry cycle to try to complete the cycle successfully on PCI bus. When this bit is 0, retry from any non-post CPU to PCI cycle results in CPU back off. 1: Try one more time 0: Backoff CPU
1	R/W	**Memory Burst Control** This bit controls whether or not the host bridge generates memory burst cycles. 0: Disable 1: Enable

0	R/W	**Memory Post Write Control** When this bit is enabled, all CPU to PCI memory write cycles are posted. 0: Disable 1: Enable

Register 84 PCI Grant Timer

Default Value: FFFFh

Access: Read/Write

The timer is used to prevent PCI masters from seizing the PCI bus too long. When the timer expires, PCI arbiter forces the master that is currently occupying PCI bus to relinquish PCI bus by removing its grant.

BIT	ACCESS	DESCRIPTION
15:0	R/W	**Initial Value of PCI Grant Timer** The setting of this register should consider the overall system configuration and the value of MLT(Register 1Dh). For a system that has many PCI master devices, the value should be higher. For a system with fewer master devices, the value should be smaller. Typical value of this timer is 60h if MLT is set to 20h. Unit: PCI clock

Register 86h CPU Idle Timer

Default Value: FFh

Access: Read/Write

Bit	Access	Description
7:0	R/W	**Initial Value of CPU Idle Timer** Recommended value for this timer is 03h. Unit: PCI clock

Register 87h Host Bridge & PCI Master Priority Timer

Default Value: FFh

Access: Read/Write

SiS620 supports the concurrency between CPU to PCI accesses and PCI to system memory accesses. During the period of concurrency, this timer is used to balance the PCI bandwidth between CPU and PCI masters.

Bit	Access	Description
7:0	R/W	**Host Bridge & PCI Master Priority Timer** Recommended value for this timer is 40h. Unit: PCI clock

Register 88h PCI Discard Timer

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:0	R/W	**PCI Discard Timer** This timer is used to keep PCI hold when PCI read is retried due to the CPU-to-PCI post write FIFO is not empty. The recommended value for this timer is 0800h. Unit: CPU clock

8.1.8. CPU/PCI CLOCKS DLL CONTROL REGISTERS

Register 8Ch SDRCLK/SDWCLK Control Register

Default Value: 2Ah

Access: Read/Write

To improve the setup time of MD for read/write DRAM, SiS5599 introduces two clocks, SDRCLK and SDWCLK, that have some phase differences from SDCLK,which is the clock that applies to SDRAM. Adjusting these two clocks lets the target to have more setup time budget. However, it decreases the hold time.

Bit	Access	Description
7:4	R/W	**SDRCLK Control** This field controls the phase of SDRCLK that lags behind SDCLK. **Bit[7:4] Descriptions Bit[7:4] Descriptions** 1111 +6.5ns 0111 +2.5ns 1110 +6.0ns 0110 +2.0ns 1101 +5.5ns 0101 +1.5ns 1100 +5.0ns 0100 +1.0ns 1011 +4.5ns 0011 +0.5ns 1010 +4.0ns 0010 +0.0ns (default) 1001 +3.5ns 0001 -0.5ns 1000 +3.0ns 0000 -1.0ns
3:0	R/W	**SDWCLK Control** This field controls the phase of SDWCLK that lags behind SDCLK. **Bit[7:4] Descriptions Bit[7:4] Descriptions** 1111 +2.5ns 0111 -1.5ns 1110 +2.0ns 0110 -2.0ns 1101 +1.5ns 0101 -2.5ns 1100 +1.0ns 0100 -3.0ns 1011 +0.5ns 0011 -3.5ns 1010 0.0ns(default) 0010 -4.0ns 1001 -0.5ns 0001 -4.5ns 1000 -1.0ns 0000 -5.0ns

Register 8Eh CPU Clock & SDRAM Clock Relationship

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:2	R/W	**Reserved**
1	R/W	**Frequency Relationship of CPU Clock and SDRAM clock** 0: CPU clock frequency is higher than SDRAM clock frequency 1: CPU clock frequency is lower than SDRAM clock frequency

0	R/W	**SDRAM Synchronous Mode** 0: Enable 1: Disable

8.1.9. A.G.P. GART AND PAGE TABLE CONTROL REGISTERS

Register 90h GART Base Address for Re-mapping

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:12	R/W	**A[31:12] for GART Base Address** This register provides the start address of the Graphics Address Re-mapping Table Base Locates in main memory. (Please note that the address provides via GART Base is 4KB aligned)
11:0	R/W	**Reserved**

Register 94h Graphic Window Control

Default Value: 00h

Access: Read/Write

This register specifies the size of the graphic window and indicates that whether the Graphic Window Base Address Register and Re-mapping GART Base Address Register contain valid information or not.

Bit	Access	Description
7	R/W	**Reserved**
6:4	R/W	**Graphic Window Size** This field defines the size of the graphic window. The accessibility of GWBA register (Register 10h) is also controlled by this field. **Bits[6:4]** **Size** 000 4M 001 8M 010 16M 011 32M 100 64M 101 128M 110 256M 111 Reserved

3:2	R/W	**Reserved**
1	R/W	**Graphic Window Base Address (Register 10h) Validation** The value of "1" for this bit indicates that the Graphic Window Base Address specified in GWBA Register (Register 10h) is valid. Otherwise, the address specified in GWBA Register is invalid. 0: Invalid 1: Valid
0	R/W	**GART Base Address for Re-mapping (Register 90h) Validation** The value of "1" for this bit indicates that the Re-mapping GART Base Address specified in Register 90h is valid. Otherwise, the address specified in Register 90h is invalid. 0: Invalid 1: Valid

Register 97h Page Table Cache Control

Default Value: 00h

Access: Read/Write

Page Table Cache is used to speedup the address translation process from graphic address to system memory address. It stores recently used GART entries in the core logic to prevent traffics toward system memory during address translation process. This register controls the characteristic of the page table cache and the address translation mechanism.

Bit	Access	Description
7:3	R/W	**Reserved**
2	R/W	**Page Table Cache Invalidation Control** In either way, this bit controls SiS620 to avoid using stalled page table cache. When this bit is 0, SiS620 automatically detects write accesses toward all GART entries and it invalidates the entire page table cache immediately once it observes such an event. When this bit is 1, aids from software must be provided to prevent SiS620 from using stalled page table cache entries. Mini-port driver must write Page Table Cache Invalidation Control Register (Register 98h) when new re-mapping information is updated to GART. 0: Detect writing GART entry 1: Write Configuration Register 98h
1	R/W	**Reserved**

0	R/W	**Page Table Cache Enable** When this bit is enabled, page table cache will be used for accelerating the address translation process. When this bit is disabled, no GART entries are cached in the page table cache and any address translation is done through memory accesses. 0: Disable 1: Enable

Register 98h Page Table Cache Invalidation Control

Default Value: 00h

Access: Read/Write

This register controls the invalidation of page table cache. The invalidation process can apply to the whole page table cache.

Bit	Access	Description
7:2	R/W	**Reserved**
1	R/W	**Invalidate Page Table Cache** Invalidate all page table cache entries when write 1 to this bit. This bit is cleared after the invalidation process completed.
0	R/W	**Reserved**

Register 9Ch Integrated VGA Control

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:2	R/W	**Reserved**
1	R/W	**CPU to Integrated VGA Memory Posted Write Control** 0: Disable 1: Enable
0	R/W	**Monochrome Device Adapter(MDA) Existence Control** 0: Not exist 1: Exist

8.1.10. DRAM PRIORITY TIMER CONTROL REGISTER

Register A0h CPU/PCI-GUI Privilege Timer

Default Value: 0000h

Access: Read/Write

SiS620 maintains the privilege of DRAM usage between CPU/PCI and GUI. When both

CPU/PCI and GUI are craving for the resource of system memory, this set of timers provides the adjustment of DRAM bandwidth between these two agents. The operation of the set of timers is explained below.

If GUI data transfer has higher privilege over CPU/PCI, GUI high privilege timer decreases every clock when GUI accesses toward system memory is undergoing. If CPU/PCI privilege is higher than GUI, CPU/PCI high privilege timer decreases every clock when CPU/PCI accesses system memory. The privilege relationship between CPU/PCI and GUI is exchanged after the timer expired. CPU/PCI accesses do not affect any one of these two timers if CPU/PCI does not have higher privilege than GUI. In the same way, GUI low priority accesses do not affect timers if GUI device does not have higher privilege than CPU/PCI.

Bit	Access	Description
15:8	R/W	**Initial Value for GUI High Privilege Timer** The timer controls how long GUI data transfer has higher privilege over CPU/PCI for DRAM accesses. Unit: DRAM clock * 4
7:0	R/W	**Initial Value for CPU/PCI high Privilege Timer** The timer controls how long the CPU/PCI has higher privilege over GUI data transfer for DRAM accesses.

Register A2h CPU/PCI-GUI Privilege Timer Control

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:6	R/W	**CPU/PCI-GUI Privilege Timer Control** **Bits[7:6]** — **Privilege** 00 — CPU/PCI High Privilege 01 — GUI High Privilege 1x — Enable CPU/PCI-GUI Privilege Timer
5:0	R/W	**Reserved**

Register A3h VGA Grant Timer

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:1	R/W	**Initial Value of VGA Grant Timer** The timer controls how long VGA grant hold once it get the DRAM bus. Unit: DRAM clock * 8

0	R/W	**Reserved**

8.1.11. A.G.P. CONTROL REGISTERS

Register C0h A.G.P. Capability Identify Register(ACAPID)

Default Value: 00200002h

Access: Read Only

Bit	Access	Description
31:24	RO	**Reserved**
23:20	RO	**A.G.P. revision Major** Default value is "0010b" to indicate that SiS620 conforms to the major revision 2 of A.G.P. interface specification.
19:16	RO	**A.G.P. revision Minor** Default value is "0000b" to indicate that SiS620 conforms to the minor revision 0 of A.G.P. interface specification..
15:8	RO	**Next Capability** Default value is "00h" to indicate the final item.
7:0	RO	**A.G.P. Capability ID** Default value is "02h". to indicate the list item as pertaining to A.G.P. registers.

Register C4h A.G.P. Status Register

Default Value: 1F000203h

Access: Read Only

Bit	Access	Description
31:24	RO	**RQ Field** The RQ field contains the maximum number of AGP command requests SiS620 can manage. Default value is "1Fh" to indicate that the maximum number of A.G.P. command requests SiS620 can manage is 32.
23:10	RO	**Reserved**
9	RO	**SBA** Default value is 1 to indicate that SiS620 supports side band addressing.
8:2	RO	**Reserved**

1:0	RO	**Data Rate** The RATE field indicates the data transfer rates supported by this devices. Default value is "11b" to indicate SiS620 support both 1X and 2X mode.

Register C8h A.G.P. Command Register

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:10	R/W	**Reserved**
9	R/W	**SBA_ENABLE.** When set, the side band address mechanism is enabled.
8	R/W	**AGP_ENABLE.** Setting the bit allows the target to accept A.G.P. operations. When cleared, the target ignores incoming A.G.P. operations. Please note that the target must be enabled before the master.
7:2	R/W	**Reserved**
1:0	R/W	**Data Rate** One(and only one) bit in the DATA_RATE field must be set to indicate the desired data transfer rate. <Bit 0: 1X, Bit 1: 2X>. The same bit must be set on both master and target. The DATA_RATE field applies to AD and SBA buses. **Bits[1:0]** — **Data Rate** 00 — Reserved 01 — 1X mode 10 — 2X mode 11 — Reserved

8.2. VIRTUAL PCI-TO-PCI BRIDGE REGISTERS (DEVICE 2)

Register 00h Vendor ID

Default Value: 1039h

Access: Read Only

The register identifies the manufacturer of the device. SiS is allocated as 1039h by PCI SIG.

Bit	Access	Description
15:0	RO	**Vendor Identification Number**

Register 02h Device ID

Default Value: 0001h

Access: Read Only

The device identifier is allocated as 0001h by Silicon Integrated Systems Corp.

Bit	Access	Description
15:0	RO	**Device Identification Number**

Register 04h Command

Default Value: 00h

Access: Read/Write, Read Only

The Command register provides coarse control over a device's ability to generate and respond to PCI cycles.

Bit	Access	Description
15:9	RO	**Reserved**
8:6	RO	**Reserved** Default value is 000b
5	R/W	**VGA Palette Snoop Enable :** Controls the behavior in the case of CPU access destined to VGA compatible address. The bit affects the destinations of I/O writes issued by the CPU with address 3C6, 3C8, 3C9. 0: Disable 1: Enable
4:2	RO	**Reserved**
1	R/W	**Memory Space Enable** Controls the forwarding of memory accesses from CPU to A.G.P. When the bit is disabled, the bridge won't forward any memory accesses to A.G.P. When the bit is enabled, the bridge forwards CPU memory cycles toward A.G.P. according to standard PCI-to-PCI bridge forwarding rule. 0: Disable 1: Enable

0	R/W	**I/O Space Enable** Controls the forwarding of I/O accesses from CPU to A.G.P. When the bit is disabled, the bridge won't forward any I/O accesses to A.G.P. When the bit is enabled, the bridge forwards CPU I/O cycles toward A.G.P. according to standard PCI-to-PCI bridge forwarding rule. 0: Disable 1: Enable

Register 06h Status

Default Value: 00h

Access: Read Only

This register is reserved since the status information of the primary bus is stored in the status register of Device 0.

Bit	Access	Description
15:0	RO	**Reserved**

Register 08h Revision ID

Default Value: 00h

Access: Read Only

The Revision ID is 00h for our first Revision.

Bit	Access	Description
7:0	RO	**Revision Identification Number**

Register 09h Programming Interface

Default Value: 00h

Access: Read Only

The default value is 00h since no specific register-level programming interface is provided.

Bit	Access	Description
7:0	RO	**Programming Interface**

Register 0Ah Sub Class Code

Default Value: 04h

Access: Read Only

The Sub Class Code is 04h for PCI-to-PCI bridge.

Bit	Access	Description
7:0	RO	**Sub Class Code**

Register 0Bh Base Class Code

Default Value: 06h

Access: Read Only

The value of 06h in this field identifies a bridge device.

Bit	Access	Description
7:0	RO	**Base Class Code**

Register 0Ch Cache Line Size

Default Value: 00h

Access: Read Only

The value of this register is always 00h since the host bridge won't generate the Memory Write and Invalidate command.

Bit	Access	Description
7:0	RO	**Cache Line Size**

Register 0Dh Master Latency Timer (MLT)

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	**Initial Value for Master Latency Timer** Unit: A.G.P. clock

Register 0Eh Header Type

Default Value: 01h

Access: Read Only

The value of 06h identifies PCI-to-PCI bridge header is being used.

Bit	Access	Description
7:0	RO	**Header Type**

Register 0Fh BIST

Default Value: 00h

Access: Read Only

The value is 00h since we don't support Build-in Self Test.

Bit	Access	Description
7:0	RO	**BIST**

Register 19h Secondary Bus Number (SBUSN)

Default Value: 00h

Access: Read/Write

This register identifies the bus number assigned to the second bus side of the "virtual" PCI-to-PCI Bridge. This field is programmed by the PCI configuration software to allow mapping of configuration cycles to AGP.

Bit	Access	Description
7:0	R/W	**Secondary Bus Number**

Register 1Ah Subordinate Bus Number (SUBUSN)

Default Value: 00h

Access: Read/Write

This register is used to record the number of the highest numbered PCI bus that is behind A.G.P.

Bit	Access	Description
7:0	R/W	**Subordinate Bus Number** Default value is 00h.

Register 1Bh Secondary Master Latency Timer (SMLT)

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	**Reserved**

Register 1Ch I/O Base

Default Value: F0h

Access: Read/Write, Read Only

The I/O Base register defines the bottom address of an address range that is used by SiS620 to determine the timing to forward I/O transactions from CPU to A.G.P.

Bit	Access	Description
7:4	R/W	**I/O Address Base A[15:12]** Bits[7:4] controls the CPU to A.G.P. I/O access. SiS620 forward I/O cycle initiated by CPU to A.G.P. if the address of the cycle meets the following requirement. IO_BASE ≤ address ≤ IO_LIMIT
3:0	RO	**Reserved**

Register 1Dh I/O Limit

Default Value: 00h

Access: Read/Write, Read Only

The I/O Limit register defines the top address of an address range that is used SiS620 to determine the timing to forward I/O transactions from CPU to A.G.P.

Bit	Access	Description
7:4	R/W	**I/O Address Limit A[15:12]** Bits[7:4] control the CPU to A.G.P. I/O access. SiS620 forwards I/O cycle initiated by CPU to A.G.P. if the address of the cycle meets the following requirement. IO_BASE ≤ address ≤ IO_LIMIT
3:0	RO	**Reserved**

Register 1Eh Secondary PCI-PCI Status (SSTS)

Default Value: 0000h

Access: Read/Write, Read Only

The Secondary Status register is similar in function and bit definition to the Status register of device 0 function 0 of SiS620.

Bit	Access	Description
15:14	RO	**Reserved**
13	WC	**Receiver Master Abort** When 620 terminates a cycle on A.G.P. with master abort. This bit is set to 1. This bit can be cleared by writing a 1 to it.
12:0	RO	**Reserved**

Register 20h Non-prefetchable Memory Base Address (MBASE)

Default Value: FFF0h

Access: Read/Write, Read Only

The register defines the base address of a non-prefetchable memory address range that is used by SiS620 to determine the timing to forward memory transactions from CPU to A.G.P.

Bit	Access	Description
15:4	R/W	**Memory Address Base A[31:20].** Bits[15:4] control the CPU to A.G.P. memory access. SiS620 forwards I/O cycle initiated by CPU to A.G.P. if the address of the cycle meets the following requirement. MBASE ≤ address ≤ MLIMIT
3:0	RO	**Reserved**

Register 22h Non-prefetchable Memory Limit Address (MLIMIT)

Default Value: 0000h

Access: Read/Write, Read Only

The register defines the top address of a non-prefetchable memory address range that is used by SiS620 to determine the timing to forward memory transactions from CPU to A.G.P.

Bit	Access	Description
15:4	R/W	**Memory Address Limit A[31:20].** Bits[15:4] control the CPU to A.G.P. memory access. SiS620 forwards I/O cycle initiated by CPU to A.G.P. if the address of the cycle meets the following requirement. MBASE ≤ address ≤ MLIMIT
3:0	RO	**Reserved**

Register 24h Prefetchable Memory Base Address (PMBASE)

Default Value: FFF0h

Access: Read/Write, Read Only

The register defines the base address of a prefetchable memory address range that is used by SiS620 to determine the timing to forward memory transactions from CPU to A.G.P.

Bit	Access	Description
15:4	R/W	**Memory Address Base A[31:20].** Bits[15:4] control the CPU to A.G.P. memory access. SiS620 forwards I/O cycle initiated by CPU to A.G.P. if the address of the cycle meets the following requirement. PMBASE ≤ address ≤ PMLIMIT
3:0	RO	**Reserved**

Register 26h Prefetchable Memory Limit Address (PMLIMIT)

Default Value: 0000h

Access: Read/Write, Read Only

The register defines the top address of a prefetchable memory address range that is used by SiS620 to determine the timing to forward memory transactions from CPU to A.G.P.

Bit	Access	Description
15:4	R/W	**Memory Address Limit A[31:20].** Bits[15:4] control the CPU to A.G.P. memory access. SiS620 forwards I/O cycle initiated by CPU to A.G.P. if the address of the cycle meets the following requirement. PMBASE ≤ address ≤ PMLIMIT
3:0	RO	**Reserved**

Register 3Eh PCI to PCI Bridge Control (BCTRL)

Default Value: 0000h

Access: Read/Write, Read Only

The Bridge Control register provides control extensions to the Command register.

Bit	Access	Description
15:4	RO	**Reserved.**
3	R/W	**VGA Enable** The bit controls the forwarding of transactions initiated by CPU. When the bit is enabled, SiS620 forwards CPU-initiated cycles with the following address to A.G.P. Memory Address: 0A0000h ~ 0BFFFFh I/O Address: 3B0h ~ 3BBh, 3C0 ~ 3DFh 0 : Disable 1 : Enable
2	R/W	**ISA Enable** When Enabled, if I/O addressing the last 768 bytes in each 1KB Block (that is A9 or A8 = 1) . This cycle forwards to Primary PCI even if the address is within the range defined by the IOBASE and IOLIMIT. 0 : Disable 1 : Enable
1:0	RO	**Reserved**

8.3. PCI IDE CONFIGURATION SPACE REGISTER

DEVICE	IDSEL	FUNCTION NUMBER
IDE	AD11	0001b

Register 00h Vendor ID

Default Value: 1039h

Access: Read Only

The register identifies the manufacturer of the device. SiS is allocated as 1039h by PCI SIG.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Vendor Identification Number**

Register 02h Device ID

Default Value: 5513h

Access: Read Only

The device identifier is allocated as 5513h by Silicon Integrated Systems Corp.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Device Identification Number**

Register 04h Command

Default Value: 0000h

Access: Read/Write, Read Only

The Command register provides coarse control over a device ability to generate and respond to PCI cycles.

BIT	ACCESS	DESCRIPTION
15:3	RO	**Reserved**
2	R/W	**Bus Master** When set, the Bus master function is enabled. It is disabled by default.
1	R/W	**Memory Space** The bit controls the response to memory space accesses. This bit should be programmed as "0".
0	R/W	**I/O Space** When enabled, the built-in IDE will respond to any access of the IDE legacy ports in the compatibility mode, or to any access of the IDE relocatable ports in the native mode. Also, any access to the PCI bus master IDE registers are allowed. This bit is zero (disabled) on reset.

Register 06h Status

Default Value: 0000h

Access: Read/Write, Read Only, Write Clear

The Status register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a 1. For instance, to clear bit 14 and not affect any other bits, write the value 0100_0000_0000_0000b to the register.

BIT	ACCESS	DESCRIPTION
15:14	RO	**Reserved** These bits are hardware to zero.
13	WC	**Master Abort Asserted** This bit is set when a PCI bus master IDE transaction is terminated by master abort. While this bit is set, IDE will issue an interrupt request. This bit can be cleared by writing a 1 to it.

12	WC	**Received Target Abort** The bit is set whenever PCI bus master IDE transaction is terminated with target abort.
11	RO	**Signaled Target Abort** The bit will be asserted when IDE terminates a transaction with target abort.
10:9	RO	**DEVSEL# Timing DEVT** These two bits define the timing of asserting DEVSEL#. The built-in IDE always asserts DEVSEL# in fast timing, and thus the two bits are hardwired to 0 per PCI Spec.
8	R/W	**Reserved, Read as "0".**
7:0	RO	**Reserved** Default value is 00h

Register 08h Revision ID

Default Value: D0h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Revision Identification Number**

Register 09h Programming Interface

Default Value: 00h

Access: Read Only

The default value is 00h since no specific register-level programming interface is provided.

BIT	ACCESS	DESCRIPTION
7	RO	**Master IDE Device** This bit is hardwired to one to indicate that the built-in IDE is capable of supporting bus master function.
6:4	RO	**Reserved**
3	RO	**Secondary IDE Programmable Indicator** When the bit is programmed as "1", it means that the primary channel can be programmed to operate in compatible or native mode. When the bit is programmed as "0", the mode is fixed and is determined by the value of bit 2. This bit should be programmed as “1” during the BIOS boot up procedures.

2	RO	**Secondary IDE Operating Mode** This bit defines the mode that the secondary IDE channel is operating in. Zero corresponds to 'compatibility' while one means native mode. By default, this bit is 0 and is programmable.
1	RO	**Primary IDE Programmable Indicator** When the bit is programmed as "1", it means that the primary channel can be programmed to operate in compatible or native mode. When the bit is programmed as "0", the mode is fixed and is determined by the value of bit 0. This bit should be programmed as "1" during the BIOS boot up procedures.
0	RO	**Primary IDE Operating Mode** This bit defines the mode that the primary IDE channel is operating in. Zero corresponds to 'compatibility' while one means native mode. By default, this bit is 0 and is programmable.

Register 0Ah Sub Class Code

Default Value: 01h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Sub Class Code**

Register 0Bh Base Class Code

Default Value: 01h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Base Class Code**

Register 0Ch Cache Line Size

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Cache Line Size**

Register 0Dh Latency Timer

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Initial Value for Latency Timer** The default value is 0. Unit: PCI clock

Register 0Eh Header Type

Default Value: 80h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Header Type**

Register 0Fh BIST

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**BIST**

Register 10h~13h Primary Channel Command Block Base Address Register

Register 14h~17h Primary Channel Control Block Base Address Register

Register 18h~1Bh Secondary Channel Command Block Base Address Register

Register 1Ch~1Fh Secondary Channel Control Block Base Address Register

In the native mode, above four registers define the IDE base address for each of the two IDE devices in both the primary and secondary channels respectively. In the compatible mode, the four registers can still be programmed and read out, but it does not affect the IDE address decoding.

Register 20h~23h Bus Master IDE Control Register Base Address

OFFSET REGISTER	REGISTER ACCESS
00h	**Bus Master IDE Command Register (Primary)**
01h	**Reserved**
02h	**Bus Master IDE Status Register(Primary)**
03h	**Reserved**
04-07h	**Bus Master IDE PRD (*) Table Pointer (Primary)**
08h	**Bus Master IDE Command Register (Secondary)**
09h	**Reserved**

0Ah	**Bus Master IDE Status Register (Secondary)**
0Bh	**Reserved**
0C-0Fh	**Bus Master IDE PRD (*) Table Pointer (Secondary)**

*PRD: Physical Region Descriptor

Register 24h~2Bh Reserved

Default Value: 00h

Access: Read Only

Register 2C~2Dh Subsystem Vendor ID

Default Value: 0000h

Access: Read/Write

This register can be written once and is used to identify vendor of the subsystem.

Register 2Eh~2Fh Subsystem ID

Default Value: 0000h

Access: Read/Write

This register can be written once and is used to identify subsystem ID.

Register 30h~33h Expansion ROM Base Address

Default Value: 00000000h

Access: Read/Write

Register 34h~3Fh Reserved

Register 40h IDE Primary Channel/Master Drive Data Recovery Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Test mode for internal use only** 0: Normal mode 1: Test mode This test mode for recovery and active timer counter.
6	R/W	**Test mode for internal use only** 0: Normal mode 1: Test mode This test mode for prefetch byte counter.
5:4	R/W	**Reserved**

3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 41h IDE Primary Channel/Master Drive Data Active Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Ultra DMA Mode Control** 0: Disable 1: Enable
6:4	R/W	**Ultra DMA 33/66 cycle time Select** 000: Reserved 001: Cycle time of 2 CLK clocks for data out 010: Cycle time of 3 CLK clocks for data out 011: Cycle time of 4 CLK clocks for data out 100: Cycle time of 5 CLK clocks for data out 101: Cycle time of 6 CLK clocks for data out 110: Cycle time of 7 CLK clocks for data out 111: Cycle time of 8 CLK clocks for data out Note : 2 CLK = 1 PCICLK
3	RO	**Reserved**
2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 42h IDE Primary Channel/Slave Drive Data Recovery Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	RO	**Reserved**
3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 43h IDE Primary Channel/Slave Drive Data Active Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Ultra DMA Mode Control** 0: Disable 1: Enable
6:4	R/W	**Ultra DMA 33/66 cycle time Select** 000: Reserved 001: Cycle time of 2 CLK clocks for data out 010: Cycle time of 3 CLK clocks for data out 011: Cycle time of 4 CLK clocks for data out 100: Cycle time of 5 CLK clocks for data out 101: Cycle time of 6 CLK clocks for data out 110: Cycle time of 7 CLK clocks for data out 111: Cycle time of 8 CLK clocks for data out Note : 2 CLK = 1 PCICLK
3	RO	**Reserved**
2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 44h IDE Secondary Channel/Master Drive Data Recovery Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	RO	**Reserved**
3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 45h IDE Secondary Channel/Master Drive Data Active Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Ultra DMA Mode Control** 0: Disable 1: Enable
6:4	R/W	**Ultra DMA 33/66 cycle time Select** 000: Reserved 001: Cycle time of 2 CLK clocks for data out 010: Cycle time of 3 CLK clocks for data out 011: Cycle time of 4 CLK clocks for data out 100: Cycle time of 5 CLK clocks for data out 101: Cycle time of 6 CLK clocks for data out 110: Cycle time of 7 CLK clocks for data out 111: Cycle time of 8 CLK clocks for data out Note : 2 CLK = 1 PCICLK
3	RO	**Reserved**

2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 46h IDE Secondary Channel/Slave Drive Data Recovery Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	RO	**Reserved**
3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 47h IDE Secondary Channel/Slave Drive Data Active Time Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Ultra DMA Mode Control** 0: Disable 1: Enable

6:4	R/W	**Ultra DMA 33/66 cycle time Select** 000: Reserved 001: Cycle time of 2 CLK clocks for data out 010: Cycle time of 3 CLK clocks for data out 011: Cycle time of 4 CLK clocks for data out 100: Cycle time of 5 CLK clocks for data out 101: Cycle time of 6 CLK clocks for data out 110: Cycle time of 7 CLK clocks for data out 111: Cycle time of 8 CLK clocks for data out Note : 2 CLK = 1 PCICLK
3	RO	**Reserved**
2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 48h IDE Status Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	RO	**Reserved**
5	RO	**Channel 1 Cable Type Status (via CBLIDB signal)** 0: 80 pins cable type 1: 40 pins cable type
4	RO	**Channel 0 Cable Type Status (via CBLIDA signal)** 0: 80 pins cable type 1: 40 pins cable type
3:2	R/W	**PCI Read Request Threshold Setting** 00: PCI Request asserted when FIFO is 62.5% full during prefetch cycles. 01: PCI Request asserted when FIFO is 50.0% full during prefetch cycles. 10: PCI Request asserted when FIFO is 25.0% full during prefetch cycles. 11: PCI Request asserted when FIFO is 12.5% full during prefetch cycles.

1:0	R/W	**PCI Write Request Threshold Setting** 00: PCI Request asserted when FIFO is 12.5% full during prefetch cycles. 01: PCI Request asserted when FIFO is 25.0% full during prefetch cycles. 10: PCI Request asserted when FIFO is 50.0% full during prefetch cycles. 11: PCI Request asserted when FIFO is 62.5% full during prefetch cycles.

Register 49h Reserved

Register 4Ah IDE General Control Register 0

Default Value: 00h

Access: Read/Write

BIT	ACESS	DESCRIPTION
7	R/W	**Bus Master generates PCI burst cycles Control** 0: Disable 1: Enable
6	R/W	**Test Mode for internal use only** 0: Test Mode 1: Normal Mode
5	R/W	**Fast post-write control** 0: Disabled 1: Enabled (Recommended)
4	R/W	**Test Mode for internal use only** 0: Normal Mode 1: Test Mode When this bit is set 1, the IRQ of HD drive would pass direct to 8259. On the others hand, IDE would gate IRQ until IDE FIFO is empty under abnormal operation.
3	R/W	**Reserved**
2	R/W	**IDE Channel 1 Enable Bit** 0: Disabled 1: Enabled
1	R/W	**IDE Channel 0 Enable Bit** 0: Disabled 1: Enabled

0	R/W	**Reserved**

Register 4Bh IDE General Control register 1

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Enable Postwrite of the Slave Drive in Channel 1** 0: Disabled 1: Enabled
6	R/W	**Enable Postwrite of the Master Drive in Channel 1** 0: Disabled 1: Enabled
5	R/W	**Enable Postwrite of the Slave Drive in Channel 0** 0: Disabled 1: Enabled
4	R/W	**Enable Postwrite of the Master Drive in Channel 0** 0: Disabled 1: Enabled
3	R/W	**Enable Prefetch of the Slave Drive in Channel 1** 0: Disabled 1: Enabled
2	R/W	**Enable Prefetch of the Master Drive in Channel 1** 0: Disabled 1: Enabled
1	R/W	**Enable Prefetch of the Slave Drive in Channel 0** 0: Disabled 1: Enabled
0	R/W	**Enable Prefetch of the Master Drive in Channel 0** 0: Disabled 1: Enabled

(Following two 16-bit wide registers define the prefetching length of each IDE channel respectively.)

Register 4Ch~4Dh Prefetch Count of Primary Channel

Default Value: FFFFh

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:0	R/W	**Prefetch Count of Primary Channel** The Count (in bytes) of IDE prefetch. The maximum value can be programmed is 512. (Default value is 512)

Register 4Eh~4Fh Prefetch Count of Secondary Channel

Default Value: FFFFh

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:0	R/W	**Prefetch Count of Secondary Channel** The Count (in bytes) of IDE prefetch. The maximum value can be programmed is 512. (Default value is 512)

Register 50h~51h Reserved

Default Value: 0000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:0	R/W	**Reserved**

Register 52h IDE Miscellaneous Control Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:5	RO	**Reserved**
4	R/W	**IDE I/O Buffer Driving Strength Control** 0: 4mA 1: 8mA
3	R/W	**Reserved**
2	R/W	**Control of IDE Programmable Indicator (Reg. 09 bit 1 and 3)** 0: IDE register 09 bit 1 and 3 would be read as "1¡ ¨ 1: IDE register 09 bit 1 and 3 would be programmable
1	R/W	**Test Mode for internal use only** 0 : Normal Mode 1 : Test Mode If this bit is set 1, IDE would reset IDE FIFO pointer when 8 bit command is forward to HDs driver. This bit would work on the condition that the transferring byte count of OS is not equal to the byte count received by HDs driver.
0	R/W	**Reserved**

8.3.1. OFFSET REGISTERS FOR PCI BUS MASTER IDE CONTROL REGISTERS

The PCI Bus master IDE Registers use 16 bytes of I/O Space. These registers can be accessed through I/O R/W to the address defined in the Bus Master IDE control register Base Address in the PCI IDE Configuration space. The base address is also defined in

Register 20h~23h of PCI IDE configuration space.

Register 00h Bus Master Primary IDE Command Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	RO	**Reserved. Return 0 on reads.**
6:5	R/W	**Read or Write Control** This bit defines the R/W control of the bus master transfer. When set to zero, PCI bus master reads are conducted. When set to one, PCI bus master writes are conducted.
2:1	RO	**Reserved**
0	R/W	**Start/Stop Bus Master** The SiS Chip built-in IDE Controller enables its bus master operation whenever it detects this bit changing from a zero to a one. The operation can be halted by writing a zero to this bit.

Register 01h Reserved

Register 02h Bus Master Primary IDE Status Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	RO	**Simplex Only** This bit is hardwired to zero to indicate that both bus master channels can be operated at a time.
6	R/W	**Drive 1 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 1 for this channel is capable of DMA transfers.
5	R/W	**Drive 0 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 0 for this channel is capable of DMA transfers.
4:3	RO	**Reserved. Return 0 on reads**
2	R/W	**Interrupt** The bit is set by the rising edge of the IDE interrupt line to indicate that all data transferred from the drive is visible in the system memory. Writing a '1' to this bit can reset it.
1	RO	**Error** This bit is set when the IDE controller encounters an error during data transferring to/from memory.

0	R/W	**Bus Master IDE Device Active** This bit is set when the start bit in the command register is set. It can be cleared when the last transfer of a region is performed, or the start bit is reset.

Register 03h Reserved

Register 04h~07h Bus Master Primary IDE PRD Table Pointer Register

This 32-bit register contains address pointing to the starting address of the PRD table.

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:2	R/W	**Base Address of the PRD Table**
1:0	R/W	**Reserved**

*PRD: Physical Region Descriptor

Register 08h Bus Master Secondary IDE Command Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	RO	**Reserved. Return 0 on reads.**
3	R/W	**Read or Write Control.** This bit defines the R/W control of the bus master transfer. When set to "0", PCI bus master reads are conducted. When set to "1", PCI bus master writes are conducted.
2:1	RO	**Reserved**
0	R/W	**Start/Stop Bus Master** The SiS chip built-in IDE Controller enables its bus master operation whenever it detects this bit changing from a zero to a one. The operation can be halted by writing a zero to this bit.

Register 09h Reserved

Register 0Ah Bus Master Secondary IDE Status Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	RO	**Simplex Only** This bit is hardwired to zero to indicate that both bus master channels can be operated at a time.

6	R/W	**Drive 1 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 1 for this channel is capable of DMA transfers.
5	R/W	**Drive 0 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 0 for this channel is capable of DMA transfers**.**
4:3	RO	**Reserved. Return 0 on reads**
2	R/W	**Interrupt** The bit is set by the rising edge of the IDE interrupt line to indicate that all data transferred from the drive is visible in the system memory. Writing a '1' to this bit can reset it.
1	RO	**Error** This bit is set when the IDE controller encounters an error during data transferring to/from memory.
0	R/W	**Bus Master IDE Device Active** This bit is set when the start bit in the command register is set. It can be cleared when the last transfer of a region is performed, or the start bit is reset.

Register 0Bh Reserved

Register 0Ch~0Fh Bus Master Secondary IDE PRD Table Pointer Register

This 32-bit register contains address pointing to the starting address of the PRD table.

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:2	R/W	**Base Address of the PRD Table**
1:0	R/W	**Reserved**

*PRD: Physical Region Descriptor

9. REGISTER DESCRIPTION – GRAPHICS

9.1. GENERAL REGISTERS

Miscellaneous Output Register

Register Type: Read/Write

Read Port: 3CC

Write Port: 3C2

Default: 00h

D7 Vertical Sync Polarity

0: Select 'positive vertical sync'

1: Select 'negative vertical sync'

D6 Horizontal Sync Polarity

0: Select 'positive horizontal sync'

1: Select 'negative horizontal sync'

Table 9.1-1 Sync Polarity vs. Vertical Screen Resolution

D7	D6	EGA	VGA
0	0	200 Lines	Invalid
0	1	350 Lines	400 Lines
1	0	Invalid	350 Lines
1	1	Invalid	480 Lines

D5 Odd/Even Page

0: Select low page of memory

1: Select high page of memory

D4 Reserved

D[3:2] Clock Select

Table 9.1-2 Table for Video Clock Selection

D3	D2	DCLK
0	0	25.175 MHz
0	1	28.322 MHz
1	0	Don't Care
1	1	For internal clock generator.

D1 Display RAM Enable

0: Disable processor access to video RAM

1: Enable processor access to video RAM

D0 I/O Address Select

0: Sets addresses for monochrome emulation

1: Sets addresses for color graphics emulation

Feature Control Register

Register Type: Read/Write

Read Port: 3CA

Write Port: 3BA/3DA

Default: 00h

D[7:4] Reserved (0)

D3 Vertical Sync Select

0: Normal Vertical Sync output to monitor

1: [Vertical Sync OR Vertical Display Enable] output to monitor

D[2:0] Reserved (0)

Input Status Register 0

Register Type: Read only

Read Port: 3C2

Default: 00h

D7 Vertical Retrace Interrupt Pending

0: Cleared

1: Pending

D[6:5] Reserved

D4 Switch Sense

D[3:0] Reserved

Input Status Register 1

Register Type: Read only

Read Port: 3BA/3DA

Default: 00h

D[7:6] Reserved

D[5:4] Diagnostic

Table 9.1-3 Table for Video Read-back Through Diagnostic Bit (I)

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
D5	**D4**	**D5**	**D4**
0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Unused	Unused

Table 9.1-4 Table for Video Read-back Through Diagnostic Bit (II)

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
D5	**D4**	**D5**	**D4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

D3 Vertical Trace

0: Inactive

1: Active

D[2:1] Reserved

D0 Display Enable Not

0: Display period

1: Retrace period

VGA Enable Register

Register Type: Read/Write

Read/Write Port: 3C3 or 46E8

Default: 00h

D0 VGA Enable (for 3C3 only)

0: Disable

1: Enable

D3 VGA Enable (for 46E8 only)

0: Disable

1: Enable

Segment Selection Register 0

Register Type: Read/Write

Read/Write Port: 3CD

Default: 00h

If D3 of SRB (Dual Segment Mode Enable bit) sets to 1, then

D7 Reserved

D[6:0] Segment Selection Write Bit[6:0]

If D3 of SRB (Dual Segment Mode Enable bit) sets to 0, then

D[7:4] Segment Selection Write Bit[3:0]

D[3:0] Segment Selection Read Bit[3:0]

Segment Selection Register 1

Register Type: Read/Write

Read/Write Port: 3CB

Default: 00h

If D3 of SRB (Dual Segment Mode Enable bit) sets to 1, then

D7 Reserved

D[6:0] Segment Selection Read Bit[6:0]

If D3 of SRB (Dual Segment Mode Enable bit) sets to 0, then

D[7:0] Reserved

9.2. CRT CONTROLLER REGISTERS

CRT Controller Index Register

Register Type: Read/Write

Read/Write Port: 3B4/3D4

Default: 00h

D[7:0] CRT Controller Index

- 00h ~ 18h for standard VGA
- 19h ~ 26h for SiS extended CRT registers
- 80h ~ BFh for SiS extended video registers

Table 9.2- 1 Table of CRT Controller Registers

INDEX (3B4/3D4)	CRT CONTROLLER REGISTERS (3B5/3D5)
00h	Horizontal Total
01h	Horizontal Display Enable End
02h	Horizontal Blank Start
03h	Horizontal Blank End
04h	Horizontal Retrace Start
05h	Horizontal Retrace End
06h	Vertical Total
07h	Overflow Register
08h	Preset Row Scan
09h	Max Scan Line/Text Character Height
0Ah	Text Cursor Start
0Bh	Text Cursor End
0Ch	Screen Start Address High
0Dh	Screen Start Address Low
0Eh	Text Cursor Location High
0Fh	Text Cursor Location Low
10h	Vertical Retrace Start
11h	Vertical Retrace End
12h	Vertical Display Enable End
13h	Screen Offset
14h	Underline Location
15h	Vertical Blank Start
16h	Vertical Blank End
17h	Mode Control
18h	Line Compare
19h	Extended Signature Read-Back Register 0
1Ah	Extended Signature Read-Back Register 1
1Bh	CRT horizontal counter read-back

1Ch	CRT vertical counter read back
1Dh	CRT overflow counter read back
1Eh	Extended Signature Read-Back Register 2
22h	Graphics Data Latch Read-back Register
24h	Attribute Controller Toggle Read-back Register
26h	Attribute Controller Index Read-back Register

CR0: Horizontal Total

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 00h

Default: 00h

D[7:0] Horizontal Total Bit[7:0]

CR1: Horizontal Display Enable End

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 01h

Default: 00h

D[7:0] Horizontal Display Enable End Bit[7:0]

CR2: Horizontal Blank Start

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 02h

Default: 00h

D[7:0] Horizontal Blank Start Bit[7:0]

CR3: Horizontal Blank End

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 03h

Default: 00h

D7 Reserved

D[6:5] Display Skew Control Bit[1:0]

00: No skew

01: Skew 1 character

10: Skew 2 characters

11: Skew 3 characters

D[4:0] Horizontal Blank End Bit[4:0]

CR4: Horizontal Retrace Start

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 04h

Default: 00h

D[7:0] Horizontal Retrace Start Bit[7:0]

CR5: Horizontal Retrace End

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 05h

Default: 00h

D7 Horizontal Blank End Bit[5]

D[6:5] Horizontal Retrace Delay Bit[1:0]

00: Skew 0 character clock

01: Skew 1 character clock

10: Skew 2 character clocks

11: Skew 3 character clocks

D[4:0] Horizontal Retrace End Bit[4:0]

CR6: Vertical Total

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 06h

Default: 00h

D[7:0] Vertical Total Bit[7:0]

CR7: Overflow Register

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 07h

Default: 00h

D7 Vertical Retrace Start Bit[9]

D6 Vertical Display Enable End Bit[9]

D5 Vertical Total Bit[9]

D4 Line Compare Bit[8]

D3 Vertical Blank Start Bit[8]

D2 Vertical Retrace Start Bit[8]

D1 Vertical Display Enable End Bit[8]

D0 Vertical Total Bit[8]

CR8: Preset Row Scan

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 08h

Default: 00h

D7 Reserved

D[6:5] Byte Panning Control Bit[1:0]

D[4:0] Preset Row Scan Bit[4:0]

CR9: Maximum Scan Line/Text Character Height

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 09h

Default: 00h

D7 Double Scan

0: Disable

1: Enable 400 lines display

D6 Line Compare Bit[9]

D5 Vertical Blank Start Bit[9]

D[4:0] Character Cell Height Bit[4:0]

CRA: Text Cursor Start

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 0Ah

Default: 00h

D[7:6] Reserved

D5 Text Cursor Off

0: Text Cursor On

1: Text Cursor Off

D[4:0] Text Cursor Start Bit[4:0]

CRB: Text Cursor End

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 0Bh

Default: 00h

D7 Reserved

D[6:5] Text Cursor Skew

00: No skew

01: Skew one character clock

10: Skew two character clocks

11: Skew three character clocks

D[4:0] Text Cursor End Bit[4:0]

CRC: Screen Start Address High

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 0Ch

Default: 00h

D[7:0] Screen Start Address Bit[15:8]

CRD: Screen Start Address Low

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 0Dh

Default: 00h

D[7:0] Screen Start Address Bit[7:0]

CRE: Text Cursor Location High

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 0Eh

Default: 00h

D[7:0] Text Cursor Location Bit[15:8]

CRF: Text Cursor Location Low

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 0Fh

Default: 00h

D[7:0] Text Cursor Location Bit[7:0]

CR10: Vertical Retrace Start

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 10h

Default: 00h

D[7:0] Vertical Retrace Start Bit[7:0]

CR11: Vertical Retrace End

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 11h

Default: 00h

D7 Write Protect for CR0 to CR7

0: Disable Write Protect

1: Enable Write Protect

D6 Alternate Refresh Rate

0: Selects three refresh cycles per scanline

1: Selects five refresh cycles per scanline

D5 Vertical Interrupt Enable

0: Enable

1: Disable

D4 Vertical Interrupt Clear

0: Clear

1: Not Clear

D[3:0] Vertical Retrace End Bit[3:0]

CR12: Vertical Display Enable End

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 12h

Default: 00h

D[7:0] Vertical Display Enable End Bit[7:0]

CR13: Screen Offset

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 13h

Default: 00h

D[7:0] Screen Offset Bit[7:0]

CR14: Underline Location Register

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 14h

Default: 00h

D7 Reserved

D6 Double-word Mode Enable

0: Disable

1: Enable

D5 Count by 4

0: Disable

1: Enable

D[4:0] Underline Location Bit[4:0]

CR15: Vertical Blank Start

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 15h

Default: 00h

D[7:0] Vertical Blank Start Bit[7:0]

CR16: Vertical Blank End

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 16h

Default: 00h

D[7:0] Vertical Blank End Bit[7:0]

CR17: Mode Control Register

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 17h

Default: 00h

D7 Hardware Reset

0: Disable horizontal and vertical retrace outputs

1: Enable horizontal and vertical retrace outputs

D6 Word/Byte Address Mode

0: Set the memory address mode to word

1: Set the memory address mode to byte

D5 Address Wrap

0: Disable the full 256K of memory

1: Enable the full 256K of memory

D4 Reserved

D3 Count by Two

0: Byte refresh

1: Word refresh

D2 Horizontal Retrace Select

0: Normal

1: Double Scan

D1 RA1 replace MA14

0: Enable

1: Disable

D0 RA0 replace MA13

0: Enable

1: Disable

CR18: Line Compare Register

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 18h

Default: 00h

D[7:0] Line Compare Bit[7:0]

CR19: Extended Signature Read-back Register 0

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 19h

Default: xxh

D[7:0] Signature read-back bit[7:0]

CR1A: Extended Signature Read-back Register 1

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 1Ah

Default: xxh

D[7:0] Signature read-back bit[15:8]

CR1B: CRT Horizontal Counter Read Back

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 1Bh

Default: xxh

D[7:0] CRT horizontal counter bit[7:0]

CR1C: CRT Vertical Counter Read Back

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 1Ch

Default: xxh

D[7:0] CRT vertical counter bit[7:0]

CR1D: CRT Overflow Counter Read Back

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 1Dh

Default: xxh

D7 Reserved

D6 MCLK Synthesizer Locking

D5 MCLK Synthesizer Locking

D4 CRT horizontal counter bit 8

D3 Reserved

D[2:0] CRT vertical counter bit[10:8]

Note: THE HORIZONTAL AND VERTICAL COUNTER VALUE WILL BE LATCHED WHEN READ REGISTER CR20. SO THE THREE REGISTERS VALUE SHOULD BE READ AFTER READ CR20.

CR1E: Extended Signature Read-Back Register 2

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 1Eh

Default: xxh

D[7:0] Signature read-back bit[23:16]

CR20: CRT Counter Trigger Port

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 20h

Default: xxh

D[7:0] Reserved

CR22: Graphics Data Latch Read-back Register

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 22h

Default: xxh

D[7:0] Graphics Data Latch bit[7:0]

CR24: Attribute Controller Toggle Read-back Register

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 24h

Default: xxh

D7 Attribute Controller Toggle

D[6:0] Reserved

CR26: Attribute Controller Index Read-back Register

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 26h

Default: xxh

D[7:6] Reserved

D5 Video Enable

D[4:0] Attribute Controller Index bit[4:0]

9.3. SEQUENCER REGISTERS

Sequencer Index Register

Register Type: Read/Write

Read/Write Port: 3C4

Default: 00h

D[7:6] Reserved

D[5:0] Sequencer Index Bit[5:0]

Table 9.3-1 Table of Sequencer Registers

INDEX (3C4)	SEQUENCER REGISTER (3C5)
00	Reset Register
01	Clock Mode
02	Color Plane Write Enable
03	Character Generator Select
04	Memory Mode

SR0: Reset Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 00h

Default: 00h

D[7:2] Reserved

D1 Synchronous reset

0: Reset

1: Normal

D0 Asynchronous reset

0: Reset

1: Normal

SR1: Clock Mode Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 01h

Default: 00h

D[7:6] Reserved

D5 Screen Off

0: Display On

1: Display Off

D4 Shifter Load 32 enable

0: Disable

1: Data shifter loaded every 4th Character Clock

D3 Dot Clock Divide by 2 enable

0: Disable

1: Video Clock is divided by 2 to generate Dot Clock

D2 Shifter Load 16 (while D4=0)

0: Disable

1: Data shifter loaded every 2nd Character Clock

D1 Reserved

D0 8/9 Dot Clock

0: Dot Clock is divided by 9 to generate Character Clock

1: Dot Clock is divided by 8 to generate Character Clock

SR2: Color Plane Write Enable Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 02h

Default: 00h

D[7:4] Reserved

D3 Plane 3 write enable

0: Disable

1: Enable

D2 Plane 2 write enable

0: Disable

1: Enable

D1 Plane 1 write enable

0: Disable

1: Enable

D0 Plane 0 write enable

0: Disable

1: Enable

SR3: Character Generator Select Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 03h

Default: 00h

D[7:6] Reserved

D5 Character generator table B select Bit[2]

D4 Character generator table A select Bit[2]

D[3:2] Character generator table B select Bit[1:0]

D[1:0] Character generator table A select Bit[1:0]

Table 9.3-2 Table of Selecting Active Character Generator

D5	D3	D2	USED WHEN TEXT ATTRIBUTE BIT 3 IS 1
D4	D1	D0	USED WHEN TEXT ATTRIBUTE BIT 3 IS 0
0	0	0	Character Table 1
0	0	1	Character Table 2
0	1	0	Character Table 3
0	1	1	Character Table 4
1	0	0	Character Table 5 (VGA only)
1	0	1	Character Table 6 (VGA only)
1	1	0	Character Table 7 (VGA only)
1	1	1	Character Table 8 (VGA only)

SR4: Memory Mode Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 04h

Default: 00h

D[7:4] Reserved

D3 Chain-4 Mode enable

0: Disable

1: Enable

D2 Odd/Even Mode enable

0: Enable

1: Disable

D1 Extended Memory

0: Select 64K

1: Select 256K

D0 Reserved

9.4. GRAPHICS CONTROLLER REGISTERS

Graphics Controller Index Register

Register Type: Read/Write

Read/Write Port: 3CE

Default: 00h

D[7:4] Reserved

D[3:0] Graphics Controller Index Bit[3:0]

Table 9.4- 1 Table of Graphics Controller Registers

INDEX (3CE)	GRAPHICS CONTROLLER REGISTER (3CF)
00	Set/Reset Register
01	Set/Reset Enable Register
02	Color Compare Register
03	Data Rotate & Function Select
04	Read Plane Select Register
05	Mode Register
06	Miscellaneous Register
07	Color Don't Care Register
08	Bit Mask Register

GR0: Set/Reset Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 00h

Default: 00h

D[7:4] Reserved

D3 Set/Reset Map for plane 3

D2 Set/Reset Map for plane 2

D1 Set/Reset Map for plane 1

D0 Set/Reset Map for plane 0

GR1: Set/Reset Enable Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 01h

Default: 00h

D[7:4] Reserved

D3 Enable Set/Reset for plane 3

0: Disable

1: Enable

D2 Enable Set/Reset for plane 2

0: Disable

1: Enable

D1 Enable Set/Reset for plane 1

0: Disable

1: Enable

D0 Enable Set/Reset for plane 0

0: Disable

1: Enable

GR2: Color Compare Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 02h

Default: 00h

D[7:4] Reserved

D3 Color Compare Map for plane 3

D2 Color Compare Map for plane 2

D1 Color Compare Map for plane 1

D0 Color Compare Map for plane 0

GR3: Data Rotate/Function Select Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 03h

Default: 00h

D[7:5] Reserved

D[4:3] Function Select

Table 9.4- 2 Table of Function Select

D4	D3	FUNCTION
0	0	write data unmodified
0	1	write data AND processor latches
1	0	write data OR processor latches
1	1	write data XOR processor latches

D[2:0] Rotate Count

Table 9.4- 3 Table of Rotate Count

D2	D1	D0	RIGHT ROTATION
0	0	0	none
0	0	1	1 bits
0	1	0	2 bits
0	1	1	3 bits
1	0	0	4 bits
1	0	1	5 bits
1	1	0	6 bits
1	1	1	7 bits

GR4: Read Plane Select Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 04h

Default: 00h

D[7:2] Reserved

D[1:0] Read Plane Select bit 1, 0

00: Plane 0

01: Plane 1

10: Plane 2

11: Plane 3

GR5: Mode Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 05h

Default: 00h

D7 Reserved

D6 256-color Mode

0: Disable

1: Enable

D5 Shift Register Mode

0: Configure shift register to be EGA compatible

1: Configure shift register to be CGA compatible

D4 Odd/Even Addressing Mode enable

0: Disable

1: Enable

D3 Read Mode

0: Map Select Read

1: Color Compare Read

D2 Reserved

D[1:0] Write mode

Table 9.4- 4 Table for Write Mode

D1	D0	MODE SELECTED
0	0	Write Mode 0: Direct processor write (Data Rotate, Set/Reset may apply).
0	1	Write Mode 1: Use content of latches as write data.
1	0	Write Mode 2: Color Plane n(0-3) is filled with the value of bit m in the processor write data.
1	1	Write Mode 3: Color Plane n(0-3) is filled with 8 bits of the color value contained in the Set/Reset Register for that plane. The Enable Set/Reset Register is not effective. Processor data will be AND with Bit Mask Register content to form new bit mask pattern. (data rotate may apply).

GR6: Miscellaneous Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 06h

Default: 00h

D[7:4] Reserved

D[3:2] Memory Address Select

Table 9.4- 5 Table of Memory Address Select

D3	D2	ADDRESS RANGE
0	0	A0000 to BFFFF
0	1	A0000 to AFFFF
1	0	B0000 to B7FFF
1	1	B8000 to BFFFF

D1 Chain Odd And Even Maps

0: Disable

1: Enable

D0 Graphics Mode Enable

0: Select alphanumeric mode

1: Select graphics mode

GR7: Color Don't Care Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 07h

Default: 00h

D[7:4] Reserved

D3 Plane 3 Don't Care

0: Disable color comparison

1: Enable color comparison

D2 Plane 2 Don't Care

0: Disable color comparison

1: Enable color comparison

D1 Plane 1 Don't Care

0: Disable color comparison

1: Enable color comparison

D0 Plane 0 Don't Care

0: Disable color comparison

1: Enable color comparison

GR8: Bit Mask Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 08h

Default: 00h

D[7:0] Bit Mask Enable Bit[7:0]

9.5. ATTRIBUTE CONTROLLER AND VIDEO DAC REGISTERS

Attribute Controller Index Register

Register Type: Read/Write

Read Port: 3C0

Write Port: 3C0

Default: 00h

D[7:6] Reserved

D5 Palette Address Source

0: From CPU

1: From CRT

D[4:0] Attribute Controller Index Bit[4:0] (00h-14h)

Table 9.5-1 Table of Attribute Controller Registers

INDEX (3C0)	ATTRIBUTE CONTROLLER REGISTER (3C0)
00h	Color Palette Register 0
01h	Color Palette Register 1
02h	Color Palette Register 2
03h	Color Palette Register 3
04h	Color Palette Register 4
05h	Color Palette Register 5
06h	Color Palette Register 6
07h	Color Palette Register 7
08h	Color Palette Register 8
09h	Color Palette Register 9
0Ah	Color Palette Register 10
0Bh	Color Palette Register 11
0Ch	Color Palette Register 12
0Dh	Color Palette Register 13
0Eh	Color Palette Register 14
0Fh	Color Palette Register 15

10h	Mode Control Register
11h	Screen Border Color
12h	Color Plane Enable Register
13h	Pixel Panning Register
14h	Color Select Register (VGA)

AR0~ARF: Palette Registers

Register Type: Read/Write

Read Port: 3C1, Index 00h ~ 0Fh

Write Port: 3C0, Index 00h ~ 0Fh

Default: 00h

D[7:6] Reserved

D[5:0] Palette Entries

AR10: Mode Control Register

Register Type: Read/Write

Read Port: 3C1, Index 10h

Write Port: 3C0, Index 10h

Default: 00h

D7 P4, P5 Source Select

0: AR0-F Bit[5:4] are used as the source for the Lookup Table Address Bit[5:4]

1: AR14 Bit[1:0] are used as the source for the Lookup Table Address Bit[5:4]

D6 Pixel Double Clock Select

0: The pixels are clocked at every clock cycle

1: The pixels are clocked at every other clock cycle

D5 PEL Panning Compatibility with Line Compare

0: Disable

1: Enable

D4 Reserved

D3 Background Intensity or Blink enable (while the Character Attribute D7=1)

0: Background Intensity attribute enable

1: Background Blink attribute enable

D2 Line Graphics enable

0: The ninth bit of nine-bit-wide character cell will be the same as the background.

1: The ninth bit of nine-bit-wide character cell will be made be the same as the eighth bit for character codes in the range C0h through DFh.

D1 Display Type

0: The contents of the Attribute byte are treated as color attribute.

1: The contents of the Attribute byte are treated as MDA-compatible attribute.

D0 Graphics/Text Mode

0: The Attribute Controller will function in text mode.

1: The Attribute Controller will function in graphics mode.

AR11: Screen Border Color

Register Type: Read/Write

Read Port: 3C1, Index 11h

Write Port: 3C0, Index 11h

Default: 00h

D[7:6] Reserved

D[5:0] Palette Entry

AR12: Color Plane Enable Register

Register Type: Read/Write

Read Port: 3C1, Index 12h

Write Port: 3C0, Index 12h

Default: 00h

D[7:6] Reserved

D[5:4] Display Status MUX Bit[1:0]

These bits select two of the eight bits color outputs to be available in the status register. The output color combinations available on the status bits are as follows:

Table 9.5-2 Table for Video Read-back Through Diagnostic Bit (I)

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1 (REFER TO 7.1.4)	
D5	**D4**	**D5**	**D4**
0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Unused	Unused

Table 9.5-3 Table for Video Read-back Through Diagnostic Bit (II)

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1 (REFER TO 7.1.4)	
D5	D4	D5	D4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

D[3:0] Enable Color Plane Bit[3:0]

AR13: Pixel Panning Register

Register Type: Read/Write

Read Port: 3C1, Index 13h

Write Port: 3C0, Index 13h

Default: 00h

D[7:4] Reserved

D[3:0] Pixel Pan Bit[3:0]

This field specifies the number of pixels the display data will be shifted to the left. This field is interpreted as indicated in the following table:

Table 9.5-4 Table of Pixel Panning

D3	D2	D1	D0	MONOCHROME TEXT	VGA MODE 13	ALL OTHERS
0	0	0	0	8	0	0
0	0	0	1	0	Invalid	1
0	0	1	0	1	1	2
0	0	1	1	2	Invalid	3
0	1	0	0	3	2	4
0	1	0	1	4	Invalid	5
0	1	1	0	5	3	6
0	1	1	1	6	Invalid	7
1	0	0	0	7	Invalid	Invalid
1	0	0	1	Invalid	Invalid	Invalid
1	0	1	0	Invalid	Invalid	Invalid
1	0	1	1	Invalid	Invalid	Invalid
1	1	0	0	Invalid	Invalid	Invalid
1	1	0	1	Invalid	Invalid	Invalid
1	1	1	0	Invalid	Invalid	Invalid
1	1	1	1	Invalid	Invalid	Invalid

AR14: Color Select Register

Register Type: Read/Write

Read Port: 3C1, Index 14h

Write Port: 3C0, Index 14h

Default: 00h

D[7:4] Reserved

D[3:2] Color Bit[7:6]

These two bits are concatenated with the six bits from the Palette Register to form the address into the LUT and to drive P[7:6].

D[1:0] Color Bit[5:4]

If AR10 D7 is programmed to a '1', these two bits replace the corresponding two bits from the Palette Register to form the address into the LUT and to drive P[5:4]. If AR10 D7 is programmed to a '0', these two bits are ignored.

9.6. COLOR REGISTERS

DAC Status Register

Register Type: Read Only

Read Port: 3C7

Default: 00h

D[7:2] Reserved

D[1:0] DAC State Bit[1:0]

00: Write Operation in progress

11: Read Operation in progress

DAC Index Register (Read Mode)

Register Type: Write Only

Write Port: 3C7

Default: 00h

D[7:0] DAC Index Bit[7:0]

DAC Index Register (Write Mode)

Register Type: Read/Write

Read/Write Port: 3C8

Default: 00h

D[7:0] DAC Index Bit[7:0]

DAC Data Register

Register Type: Read/Write

Read/Write Port: 3C9

Default: 00h

When SR7 D2 = 1,

D[7:6] Reserved

D[5:0] DAC Data [5:0]

Before writing to this register, 3C8h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue values for the DAC entry are written. After the third value is written, the values are transferred to the LUT and the DAC index is incremented in case new values for the next DAC index are to be written.

Before reading from this register, 3C7h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue value for the DAC entry may be read from this DAC index. After the third value is read, the DAC index is incremented in case the value for the next DAC index to be read.

When SR7 D2 = 0,

D[7:0] DAC Data [7:0]

When SR7 D2 = 0, the 24-bit LUT is enabled. This LUT can translate the R, G, B values into new R, G, B values independently. This LUT can be used for performing GAMMA correction function. The programming procedure is same as standard LUT when SR7 D2 = 1.

PEL Mask Register

Register Type: Read/Write

Read/Write Port: 3C6

Default: 00h

D[7:0] Pixel Mask Bit[7:0]

This field is the Pixel Mask for the palette DAC. If a bit in this field is programmed to a '0', the corresponding bit in the pixel data will be ignored in looking up an entry in the LUT.

9.7. EXTENDED REGISTERS

Extended Index Register

Register Type: Read/Write

Read/Write Port: 3C4

Default: 00h

D[7:6] Reserved

D[5:0] Extended Register Index Bit[5:0] (05h ~ 37h)

Table 9.7-1 Table of Extended Registers

INDEX (3C4)	EXTENDED ENHANCED REGISTER (3C5)
05h	Extended Password/Identification Register
06h	Extended Graphics Mode Control Register
07h	Extended Misc. Control Register 0
08h	Extended CRT/CPU Threshold Control Register 0
09h	Extended CRT/CPU Threshold Control Register 1
0Ah	Extended CRT Overflow Register
0Bh	Extended Misc. Control Register 1
0Ch	Extended Misc. Control Register 2
0Dh	Extended Configuration Status 0
0Eh	Extended Configuration Status 1
0Fh	Extended Scratch Register 0
10h	Extended Scratch Register 1
11h	Extended DDC and Power Control Register
12h	Extended Horizontal Overflow Register
13h	Extended Clock Generator Register
13h	Extended 25Mhz Video Clock Register 2
13h	Extended 28Mhz Video Clock Register 2
14h	Extended Hardware Cursor Color 0 Red Register
15h	Extended Hardware Cursor Color 0 Green Register
16h	Extended Hardware Cursor Color 0 Blue Register
17h	Extended Hardware Cursor Color 1 Red Register
18h	Extended Hardware Cursor Color 1 Green Register
19h	Extended Hardware Cursor Color 1 Blue Register
1Ah	Extended Hardware Cursor Horizontal Start Register 0
1Bh	Extended Hardware Cursor Horizontal Start Register 1

1Ch	Extended Hardware Cursor Horizontal Preset Register
1Dh	Extended Hardware Cursor Vertical Start Register 0
1Eh	Extended Hardware Cursor Vertical Start Register 1
1Fh	Extended Hardware Cursor Vertical Preset Register
20h	Extended Linear Addressing Base Address Register 0
21h	Extended Linear Addressing Base Address Register 1
22h	Extended Standby/Suspend Timer Register
23h	Extended Misc. Control Register 3
24h	Extended Reserved Register
25h	Extended Scratch Register 2
26h	Extended Graphics Engine Register 0
27h	Extended Graphics Engine Register 1
28h	Extended Internal Memory Clock Register 0
29h	Extended Internal Memory Clock Register 1
2Ah	Extended Internal Video Clock Register 0
2Ah	Extended 25Mhz Video Clock Register 0
2Ah	Extended 28Mhz Video Clock Register 0
2Bh	Extended Internal Video Clock Register 1
2Bh	Extended 25Mhz Video Clock Register 1
2Bh	Extended 28Mhz Video Clock Register 1
2Ch	Extended Turbo Queue Base Address
2Dh	Extended Memory Start Control Register
2Eh	Extended Reserved Register
2Fh	Extended DRAM Frame Buffer Size Register
30h	Extended Fast Page Flip Starting Address Low Register
31h	Extended Fast Page Flip Starting Address Middle Register
32h	Extended Fast Page Flip Starting Address High Register
33h	Extended Misc. Control Register 4
34h	Extended Misc. Control Register 5
35h	Extended Misc. Control Register 6

36h	Extended Scratch Register 3
37h	Extended Scratch Register 4
38h	Extended Misc. Control Register 7
39h	Extended Misc. Control Register 8
3Ah	Extended MPEG Turbo Queue Base Address
3Bh	Extended Clock Generator Control Register
3Ch	Extended Misc. Control Register 9
3Dh	Extended Misc. Control Register 10
3Eh	Extended Misc. Control Register 11
3Fh	Extended Misc. Control Register 12

SR5: Extended Password/Identification Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 05h

Default: 00h

D[7:0] Password/Identification Bit[7:0]

If 86h is written into this register, then A1h will be read from this register, and unlock all the extension registers.

If the value other than 86h is written into this register, then 21h will be read from this register, and lock all the extension registers.

SR6: Extended Graphics Mode Control Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 06h

Default: 00h

D7 Graphics mode linear addressing enable

0: Disable

1: Enable

D6 Graphics mode hardware cursor display enable

0: Disable

1: Enable

D5 Graphics mode interlaced enable

0: Disable

1: Enable

D4 True-Color graphics mode enable

0: Disable

1: Enable

D3 64K-Color graphics mode enable

0: Disable

1: Enable

D2 32K-Color graphics mode enable

0: Disable

1: Enable

D1 Enhanced graphics mode enable

0: Disable

1: Enable

D0 Enhanced text mode enable

0: Disable

1: Enable

SR7: Extended Misc. Control Register 0

Register Type: Read/Write

Read/Write Port: 3C5, Index 07h

Default: 00h

D7 Merge video line buffer into CRT FIFO

0: Disable

1: Enable

The size of CRT FIFO can be set to 256x64 bit when merged with video line buffer only when video playback is disabled.

D6 Reserved

D5 Internal RAMDAC power saving mode

0: Power saving mode

1: High power mode

D4 Extended video clock frequency divided by 2

0: Disable

1: Enable

D3 Enable multi-line pre-fetch function

0: Enable

1: Disable

D2 24-bit color palette enable for direct color mode

0: Enable

1: Disable

D1 High Speed DAC operation Bit[0]

D0 External DAC reference voltage input

0: Internal DAC reference voltage

1: External DAC reference voltage

To achieve more accurate reference voltage. The reference voltage of DAC can be input from external.

SR8: Extended CRT/CPU Threshold Control Register 0

Register Type: Read/Write

Read/Write Port: 3C5, Index 08h

Default: 00h

D[7:4] CRT/CPU Arbitration Threshold Low Bit[3:0]

D[3:0] CRT/Engine Threshold High Bit[3:0]

SR9: Extended CRT/CPU Threshold Control Register 1

Register Type: Read/Write

Read/Write Port: 3C5, Index 09h

Default: 00h

D7 32-bpp True-Color graphics mode enable

0: Disable

1: Enable

D[6:4] ASCII/Attribute Threshold Bit[2:0]

D[3:0] CRT/CPU Threshold High Bit[3:0]

SRA: Extended CRT Overflow Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 0Ah

Default: 00h

D[7:4] Extended Screen Offset Bit[11:8]

D3 Extended Vertical Retrace Start Bit[10]

D2 Extended Vertical Blank Start Bit[10]

D1 Extended Vertical Display Enable End Bit[10]

D0 Extended Vertical Total Bit[10]

SRB: Extended Misc. Control Register 1

Register Type: Read/Write

Read/Write Port: 3C5, Index 0Bh

Default: 00h

D7 True-Color Graphics mode RGB Sequence Selection

0: Red, Green, and Blue in byte order

1: Blue, Green, and Red in byte order

D[6:5] Memory-mapped I/O Space Selection Bit[1:0]

00: Disable

01: Select Axxxxh as Memory-mapped I/O Space

10: Select Bxxxxh as Memory-mapped I/O Space

11: Select PCI config register 14H as Memory-mapped I/O space

D4 True-Color frame rate modulation enable

0: Disable

1: Enable

D3 Dual segment register mode enable

0: Disable

1: Enable

D2 I/O gating enable while write-buffer is not empty

0: Disable

1: Enable

D1 16-color packed pixel enable

0: Disable

1: Enable

D0 CPU-driven BITBLT operation enable

0: Disable

1: Enable

SRC: Extended Misc. Control Register 2

Register Type: Read/Write

Read/Write Port: 3C5, Index 0Ch

Default: 00h

D7 Graphics mode 32-bit memory access enable

0: Disable

1: Enable

D6 Text mode 16-bit memory access enable

0: Disable

1: Enable

D5 Read-ahead cache operation enable

0: Disable

1: Enable

D3 Test mode enable

0: Disable

1: Enable

D[4, 2:1] Memory Configuration Bit[2:0]

000: 1MByte/1 bank

001: 2MByte/2 banks

010: 4MByte/2 banks or 4 banks

011: Reserved

100: Reserved

101: 2MByte/1 banks

110: 4MByte/1 banks

111: 8MByte/2 banks

D0 Synchronous reset timing generator enable

0: Disable

1: Enable

SRD: Extended Configuration Status 0

Register Type: Read Only

Read Port: 3C5, Index 0Dh

Default: 00h

D7 Leading MCLK bit[0] Status

This bit will present the status of trapping of MD36.

Please refer to H/W trapping section for more details.

D6 Internal Clock Generator Status

0: Select external clock generator

1: Select internal clock generator

This bit will present the status of trapping of ENVCO.

D5 Reserved for VGA BIOS

This bit will present the status of trapping of VMD62.

D4 Internal AGP bus Status

0: Disable internal AGP Bus

1: Enable internal AGP bus

This bit will present the status of trapping of MD52.

D3 Reserved for VGA BIOS

This bit will present the status of trapping of VMD63.

D2 Leading MCLK bit[3] Status

This bit will present the status of trapping of MD39.

Please refer to H/W trapping section for more details.

D1 Video Subsystem Control Status

This bit will present the status of trapping of MD49.

When this bit is present 0 that means this function is controlled by BIOS.

D0 Shared Frame buffer/Local Frame buffer Status

0: Local Frame Buffer Mode

1: Shared Frame Buffer Mode

This bit will present the status of trapping of MD48.

SRE: Extended Configuration Status 1

Register Type: Read Only

Read Port: 3C5, Index 0Eh

Default: 00h

D7 Reserved for VGA BIOS

This bit will present the status of trapping of VMD61.

D6 Integrated VGA Controller Status

0: Disable

1: Enable

This bit will present the status of trapping of MD62.

D5 Host bus Decoding Mode Status

0: Slow

1: Fast

This bit will present the status of trapping of MD61.

D4 Reserved

D3 Support INT#A for Digital Flat Panel Interface Status

0: Disable

1: Enable

This bit will present the status of trapping of MD59.

D2 Reserved for MD58 status

D1 Leading MCLK bit[2] Status

This bit will present the status of trapping of MD38.

Please refer to H/W trapping section for more details.

D0 Leading MCLK bit[1] Status

This bit will present the status of trapping of MD37.

Please refer to H/W trapping section for more details.

SRF: Extended Scratch Register 0

Register Type: Read/Write

Read/Write Port: 3C5, Index 0Fh

Default: 00h

D[7:0] Reserved for video BIOS

SR10: Extended Scratch Register 1

Register Type: Read/Write

Read/Write Port: 3C5, Index 10h

Default: 00h

D[7:0] Reserved for video BIOS

SR11: Extended DDC and Power Control Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 11h

Default: 00h

D7 Force VGA into suspend mode

0: Disable

1: Enable

D6 Force VGA into standby mode

0: Disable

: Enable

D5 Enable video memory access as activation source

0: Disable

1: Enable

D4 Enable keyboard and hardware cursor as system activation source

0: Disable

1: Enable

D3 Enable ACPI Power Management

0: Disable

1: Enable

D2 Reserved

D1 DDC DATA Programming

While writing this bit,

0: Output '0' logic into DDC Data Signal.

1: Output '1' logic into DDC Data Signal.

While reading this bit,

0: Get '0' logic from DDC Data Signal .

1: Get '1' logic from DDC Data Signal .

D0 DDC CLK Programming

While writing this bit,

0: Output '0' logic into DDC Clock Signal.

1: Output '1' logic into DDC Clock Signal.

While reading this bit,

0: Get '0' logic from DDC Clock Signal .

1: Get '1' logic from DDC Clock Signal .

SR12: Extended Horizontal Overflow Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 12h

Default: 00h

D[7:5] Horizontal Retrace Skew

000 : no delay

001 : delay 1 DCLK

010 : delay 2 DCLK

011 : delay 3 DCLK

100 : delay 4 DCLK

101 : delay 5 DCLK

110 : delay 6 DCLK

111 : delay 7 DCLK

D4 Extended Horizontal Blank End Bit[6]

D3 Extended Horizontal Retrace Start Bit[8]

D2 Extended Horizontal Blank Start Bit[8]

D1 Extended Horizontal Display Enable End Bit[8]

D0 Extended Horizontal Total Bit[8]

SR13: Extended Clock Generator Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 13h

Default: 00h

D7 MCLK Post-scale Bit[2]

D6 Internal VCLK Post-Scale Bit[2]

D[5:0] Reserved

SR13-1: Extended 25Mhz Video Clock Register 2

Register Type: Read/Write

Read/Write Port: 3C5, Index 13h

Default: 00h

D7 Reserved

D6 25Mhz VCLK Post-Scale Bit[2]

D[5:0] Reserved

SR13-2: Extended 28Mhz Video Clock Register 2

Register Type: Read/Write

Read/Write Port: 3C5, Index 13h

Default: 00h

D7 Reserved

D6 28Mhz VCLK Post-Scale Bit[2]

D[5:0] Reserved

SR14: Extended Hardware Cursor Color 0 Red Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 14h

Default: 00h

D[7:6] Reserved

D[5:0] Hardware Cursor Color 0 Red Bit[5:0]

SR15: Extended Hardware Cursor Color 0 Green Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 15h

Default: 00h

D[7:6] Reserved

D[5:0] Hardware Cursor Color 0 Green Bit[5:0]

SR16: Extended Hardware Cursor Color 0 Blue Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 16h

Default: 00h

D[7:6] Reserved

D[5:0] Hardware Cursor Color 0 Blue Bit[5:0]

SR17: Extended Hardware Cursor Color 1 Red Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 17h

Default: 00h

D[7:6] Reserved

D[5:0] Hardware Cursor Color 1 Red Bit[5:0]

SR18: Extended Hardware Cursor Color 1 Green Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 18h

Default: 00h

D[7:6] Reserved

D[5:0] Hardware Cursor Color 1 Green Bit[5:0]

SR19: Extended Hardware Cursor Color 1 Blue Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 19h

Default: 00h

D[7:6] Reserved

D[5:0] Hardware Cursor Color 1 Blue Bit[5:0]

SR1A: Extended Hardware Cursor Horizontal Start Register 0

Register Type: Read/Write

Read/Write Port: 3C5, Index 1Ah

Default: 00h

D[7:0] Hardware Cursor Horizontal Start Bit[7:0]

SR1B: Extended Hardware Cursor Horizontal Start Register 1

Register Type: Read/Write

Read/Write Port: 3C5, Index 1Bh

Default: 00h

D7 Enable hardware cursor using memory-mapped I/O

0: Disable

1: Enable

D[6:4] Reserved

D[3:0] Hardware Cursor Horizontal Start Bit[11:8]

SR1C: Extended Hardware Cursor Horizontal Preset Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 1Ch

Default: 00h

D[7:6] Reserved

D[5:0] Hardware Cursor Horizontal Preset Bit[5:0]

SR1D: Extended Hardware Cursor Vertical Start Register 0

Register Type: Read/Write

Read/Write Port: 3C5, Index 1Dh

Default: 00h

D[7:0] Hardware Cursor Vertical Start Bit[7:0]

SR1E: Extended Hardware Cursor Vertical Start Register 1

Register Type: Read/Write

Read/Write Port: 3C5, Index 1Eh

Default: 00h

D[7:4] Hardware Cursor Pattern Select Bit[3:0]

D3 Hardware Cursor Side Pattern Enable

0: Disable

1: Enable

D[2:0] Hardware Cursor Vertical Start Bit[10:8]

SR1F: Extended Hardware Cursor Vertical Preset Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 1Fh

Default: 00h

D[7:6] Reserved

D[5:0] Hardware Cursor Vertical Preset Bit[5:0]

SR20: Extended Linear Addressing Base Address Register 0

Register Type: Read/Write

Read/Write Port: 3C5, Index 20h

Default: 00h

D[7:0] Linear Addressing Base Address Bit[26:19]

SR21: Extended Linear Addressing Base Address Register 1

Register Type: Read/Write

Read/Write Port: 3C5, Index 21h

Default: 00h

D[7:5] Linear Addressing Space Aperture Bit[2:0]

000: 512 Kbyte

001: 1 Mbyte

010: 2 Mbyte

011: 4 Mbyte

100: 8 MByte

Others: Reserved

D[4:0] Linear Addressing Base Address Bit[31:27]

SR22: Extended Standby/Suspend Timer Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 22h

Default: 00h

D[7:4] Suspend Timer Bit[3:0]

The resolution for Suspend Timer is 2 minutes.

D[3:0] Standby Timer Bit[3:0]

The resolution for Standby Timer is 2 minutes.

SR23: Extended Misc. Control Register 3

Register Type: Read/Write

Read/Write Port: 3C5, Index 23h

Default: 00h

D7 Reserved

D6 CRC Generator Enable

0: Disable

1: Enable

D5 Reserved

D4 Bypass SRAM

0: Disable

1: Enable

D3 Video Compatible Hardware Cursor Visibility Enable

0: Disable

1: Enable

D[2:0] DRAM Control Signal Delay Compensation Bit[1:0]

000: Delay 4 ns

001: Delay 5 ns

010: Delay 6 ns

011: Delay 7 ns

100: Delay 8 ns

101: Delay 9 ns

110: Delay 10 ns

111: Delay 11 ns

SR24: Extended Reserved Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 24h

Default: 00h

D[7:0] Graphics frame buffer location address Bit[7:0]

SR25: Extended Scratch Register 2

Register Type: Read/Write

Read/Write Port: 3C5, Index 25h

Default: 00h

D[7:0] Reserved for VGA BIOS

SR26: Extended Graphics Engine Register 0

Register Type: Read/Write

Read/Write Port: 3C5, Index 26h

Default: 00h

D7 Reserved

D6 Power-down Internal RAMDAC

0: Disable

1: Enable

D[5:1] Reserved

D0 Extended screen starting address Bit[20]

SR27: Extended Graphics Engine Register 1

Register Type: Read/Write

Read/Write Port: 3C5, Index 27h

Default: 00h

D7 Turbo Queue Engine enable

0: Disable

1: Enable

D6 Graphics Engine Register Programming enable

0: Disable

1: Enable

D[5:4] Logical Screen Width and Byte-Per-Pixel Select Bit[1:0]

00 1024, 256 colors or 512, 32k/64k colors

01 2048, 256 colors or 1024, 32k/64k colors

10 4096, 256 colors or 2048, 32k/64k colors

11 invalid

D[3:0] Extended Screen Start Address Bit[19:16]

SR28: Extended Internal Memory Clock Register 0

Register Type: Read/Write

Read/Write Port: 3C5, Index 28h

Default: 00h

D[7] MCLK Divider

0: Do not divide

1: Divide by 2

D[6:0] MCLK Numerator Bit[6:0]

[0000000:1111111] = [1:128]

NOTE: For the operation of internal memory clock generation, please refer to " the section of Internal Dual-Clock Synthesizer".

SR29: Extended Internal Memory Clock Register 1

Register Type: Read/Write

Read/Write Port: 3C5, Index 29h

Default: 00h

D7 MCLK VCO Gain

0: Gain for low frequency operation

1: Gain for high frequency operation

D[6:5] MCLK Post-Scale Bit[1:0]

When SR13 D7=0

00: Do not scale

01: Scaled by 2

10: Scaled by 3

11: Scaled by 4

When SR13 D7=1

00: Reserved

01: Reserved

10: Scaled by 6

11: Scaled by 8

D[4:0] MCLK DeNumerator Bit[4:0]

[00000:11111] = [1:32]

NOTE: For the operation of internal memory clock generation, please refer to "the section of Internal Dual-Clock Synthesizer".

SR2A: Extended Internal Video Clock Register 0

Register Type: Read/Write

Read/Write Port: 3C5h,Index 2Ah

Default: 00h

D[7] Internal VCLK Divider

0: Do not divide

1: Divide by 2

D[6:0] Internal VCLK Numerator Bit[6:0]

[0000000:1111111] = [1:128]

NOTE: For the operation of internal video clock generation, please refer to "the section of Internal Dual-Clock Synthesizer ".

SR2A-1: Extended 25MHz Video Clock Register 0

Register Type: Read/Write

Read/Write Port: 3C5h,Index 2Ah

Default: 00h

D[7] 25Mhz VCLK Divider

0: Do not divide

1: Divide by 2

D[6:0] 25Mhz VCLK Numerator Bit[6:0]

[0000000:1111111] = [1:128]

SR2A-2: Extended 28MHz Video Clock Register 0

Register Type: Read/Write

Read/Write Port: 3C5h,Index 2Ah

Default: 00h

D[7] 28Mhz VCLK Divider

0: Do not divide

1: Divide by 2

D[6:0] 28Mhz VCLK Numerator Bit[6:0]

[0000000:1111111] = [1:128]

SR2B: Extended Internal Video Clock Register 1

Register Type: Read/Write

Read/Write Port: 3C5h, Index 2Bh

Default: 00h

D7 Internal VCLK VCO Gain

0: Gain for low frequency operation

1: Gain for high frequency operation

D[6:5] Internal VCLK Post-Scale Bit[1:0]

When SR13 D6 = 0

00: Do not scale

01: Scaled by 2

10: Scaled by 3

11: Scaled by 4

When SR13 D6 = 1

00: Reserved

01: Reserved

10: Scaled by 6

11: Scaled by 8

D[4:0] Internal VCLK DeNumerator Bit[4:0]

[00000:11111] = [1:32]

NOTE: For the operation of internal video clock generation, please refer to "the section of Internal Dual-Clock Synthesizer".

SR2B-1: Extended 25MHz Video Clock Register 1

Register Type: Read/Write

Read/Write Port: 3C5h, Index 2Bh

Default: 00h

D7 25MHz VCLK VCO Gain

0: Gain for low frequency operation

1: Gain for high frequency operation

D[6:5] 25MHz VCLK Post-Scale Bit[1:0]

When SR13-1 D6 = 0

00: Do not scale

01: Scaled by 2

10: Scaled by 3

11: Scaled by 4

When SR13-1 D6 = 1

00: Reserved

01: Reserved

10: Scaled by 6

11: Scaled by 8

D[4:0] 25MHz VCLK DeNumerator Bit[4:0]

[00000:11111] = [1:32]

SR2B-2: Extended 28MHz Video Clock Register 1

Register Type: Read/Write

Read/Write Port: 3C5h, Index 2Bh

Default: 00h

D7 28MHz VCLK VCO Gain

0: Gain for low frequency operation

1: Gain for high frequency operation

D[6:5] 28MHz VCLK Post-Scale Bit[1:0]

When SR13-2 D6= 0,

00: Do not scale

01: Scaled by 2

10: Scaled by 3

11: Scaled by 4

When SR13B D6= 1

00: Reserved

01: Reserved

10: Scaled by 6

11: Scaled by 8

D[4:0] 28MHz VCLK DeNumerator Bit[4:0]

[00000:11111] = [1:32]

SR2C: Extended Turbo Queue Base Address

Register Type: Read/Write

Read/Write Port: 3C5h, Index 2Ch

Default: 00h

D[7:0] Turbo Queue Base Address Bit[7:0]

SR2D: Extended Memory Start Control Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 2Dh

Default: 00h

D[7:4] Reserved

D[3:0] Page Size Select

0000: 2 KB at 32-bit mode, 4 KB at 64-bit mode

0001: 4 KB at 32-bit mode, 8 KB at 64-bit mode

0010: 8 KB at 32-bit mode, 16 KB at 64-bit mode

0011: 16 KB at 32-bit mode, 32 KB at 64-bit mode

0100: 1 KB at 32-bit mode, 2 KB at 64-bit mode

Others: Reserved

SR2E: Extended Reserved Register

Register Type: Read/Write

Read/Write Port: 3C5h, Index 2Eh

Default: 00h

D[7:4] Memory Address Scrambling Table Selection Bit[3:0]

D[3:0] Reserved

SR2F: Extended DRAM Frame Buffer Size Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 2Fh

Default: 00h

D[7:6] Reserved

D5 Enable Fast Change Mode Timing

0: Disable

1: Enable

D4 Enable Fast Page Flip

0: Disable

1: Enable

D[3:2] Reserved

D[1:0] Shared Frame Buffer Size

00 : Reserved

01 : 2 MB

10 : 4 MB

11 : 8MB

SR30: Extended Fast Page Flip Starting Address Low Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 30h

Default: 00h

D[7:0] Fast page flip starting address bit[7:0]

SR31: Extend Fast Page Flip Starting Address Middle Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 31h

Default: 00h

D[7:0] Fast page flip start address bit[15:8]

SR32: Extended Fast Page Flip Starting Address High Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 32h

Default: 00h

D[7:5] Reserved

D[4:0] Fast page flip start address bit[20:16]

Note: The fast page flip starting address is latched when SR32 is written. So the registers, SR30 and SR31, should be programmed before SR32. These registers are enabled by setting SR2F D4.

SR33: Extended Misc. Control Register 4

Register Type: Read/Write

Read/Write Port: 3C5, Index 33h

Default: 00h

D7 Reserved

D6 Select external 14MHz(OSCI) as MCLK (Shared Frame Buffer Mode Only)

0: Disable

1: Enable

D5 Relocated VGA I/O port addresses decoding disable

0: Disable

1: Enable

The standard VGA register I/O port address can be relocated to address defined by PCI Config Register 18H. This bit disables the relocated address decoding.

D4 Standard VGA I/O port addresses decoding enable

0: Enable

1: Disable

The standard VGA register I/O port address decoding can be disabled by this bit.

D3 Reserved

D2 Select SGRAM Latency

0: Latency = 3

1: Latency = 2

D1 Enable SGRAM Mode Write timing

0: Disable

1: Enable

This bit must be set before accessing SGRAM. It must clear to 0 before setting to 1 to generate a new Mode Write cycle.

D0 Enable SGRAM timing

0: Disable

1: Enable

SR34: Extended Misc. control Register 5

Register Type: Read/Write

Read/Write Port: 3C5, Index 34h

Default: 00h

D7 DRAM controller one cycle write enable

0: Disable

1: Enable

D6 DRAM controller one cycle read enable

0: Enable

1: Disable

D[5:3] Reserved

D2 Enable MD output PAD low power consumption

0: Disable

1: Enable

D1 Enable CRT low request cycle on UMA mode

0: Disable

1: Enable

D0 Enable Hardware Command Queue threshold low

0: Disable

1: Enable

SR35: Extended Misc. Control Register 6

Register Type: Read/Write

Read/Write Port: 3C5, Index 35h

Default: 00h

D7 Reserved

D6 Enable MA output PAD low power consumption

0: Disable

1: Enable

D5 SGRAM burst timing enable

0: Enable

1: Disable

D4 Enable Host Bus burst write zero-wait

0: Disable

1: Enable

D[3:2] DRAM DQM LOW period width compensation bit[1:0]

00: Add 0ns

01: Add 2ns

10: Add 4ns

11: Add 6ns

D1 Level selection of hardware command queue

0: Select high level

1: Select low level

D0 Level selection of host bus post write buffer

0: Select low level

1: Select high level

SR36: Extended Scratch Register 3

Register Type: Read/Write

Read/Write Port: 3C5, Index 36h

Default: 00h

D[7:0] Reserved for VGA BIOS

SR37: Extended Scratch Register 4

Register Type: Read/Write

Read/Write Port: 3C5, Index 37h

Default: 00h

D[7:0] Reserved for VGA BIOS

SR38: Extended Misc. Control Register 7

Register Type: Read/Write

Read/Write Port: 3C5, Index 38h

Default: 00h

D[7:4] Hardware Cursor Location

Hardware Cursor Starting Address Bit[21:18]

D3 PCI read cache time-out function enable

0: Enable

1: Disable

D2 Disable Line compare

0: Enable

1: Disable

D[1:0] Video Clock Register Selection Bit[1:0]

00 : Select Internal Video Clock Registers

SR13, SR2A, SR2B

01 : Select 25MHz Video Clock Registers

SR13, SR2A-1, SR2B-1

10 : Select 28MHz Video Clock Registers

SR13, SR2A-2, SR2B-2

11 : Reserved

There are three video clock registers Internal Video Clock Registers, 25Mhz Video Clock Registers, 28Mhz Video Clock Registers. All three registers use the same index of 3C5, index 13, 2A and 2B. The selection is programmed by Video Clock Register Selection Bit[1:0]. The VCLK frequency is generated from Internal Video Clock Registers when Miscellaneous Output Register (write port 3C2) Bit[3:2]=11. The VCLK frequency is generated from 25Mhz Video Clock Registers when Miscellaneous Output Register (write port 3C2) bit[3:2]=00. The VCLK frequency is generated from 28Mhz Video Clock Registers when Miscellaneous Output Register (write port 3C2) bit[3:2]=01.

SR39: Extended Misc. Control Register 8

Register Type: Read/Write

Read/Write Port: 3C5, Index 39h

Default: 00h

D[7:3] Reserved

D2 3D Accelerator Control

0: Disable

1: Enable

D[1:0] Reserved

SR3A: Reserved

SR3B: Extended Clock Generator Control Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 3Bh

Default: 00h

D[7:4] Video clock generator control bit[3:0]

D[3:0] Memory clock generator control bit[3:0]

SR3C: Extended Misc. Control Register 9

Register Type: Read/Write

Read/Write Port: 3C5, Index 3Ch

Default: 00h

D7 Enable DRAM control signal output PAD low power consumption

0: Disable

1: Enable

D6 Enable SCLK output PAD low power consumption

0: Enable

1: Disable

D[5:0] Reserved

SR3D: Extended Misc. Control Register 10

Register Type: Read/Write

Read/Write Port: 3C5, Index 3Dh

Default: 00h

D7 Enable 2D/3D software queue 62K bytes

0: software queue 30K bytes

1: software queue 62K bytes

D6 DRAM Handshaking signal delay bit 2 (Shared Frame Buffer Mode only)

D5 Reserved

D[4:3] DRAM Handshaking signal delay bit [1:0] (Shared Frame Buffer Mode only)

D2 Disable standard display memory (A0000~BFFFF) access

0: Enable

1: Disable

D1 Enable CRT end of line detection

0: Disable

1: Enable

D0 Enable 3D pre-setup engine

0: Disable

1: Enable

SR3E: Extended Misc. Control Register11

Register Type: Read/Write

Read/Write Port: 3C5, Index 3Eh

Default: 00h

D7 Enable DCLK off

0: Disable

1: Enable

D[6:5] AGP Control signal delay compensation Bit [1:0]

00: delay 0 ns

01: delay 1 ns

00: delay 2ns

01: delay 3 ns

D4 Select type of 16Mb (512k*32) when using SGRAM

0: Select SGRAM of 8Mb (256k*32)

1: Select SGRAM of 16Mb (512k*32)

D3 Enable DRAM controller stick to texture-read request

0: Disable

1: Enable

D2 Hardware cursor starting address Bit[22]

D1 Enable block write function when using SGRAM

0: Disable

1: Enable

D0 Enable high speed DCLK

0: Disable

1: Enable

SR3F: Extended Misc. Control Register12

Register Type: Read/Write

Read/Write Port: 3C5, Index 3Fh

Default: 00h

D7 High Speed DAC operation Bit[1]

D6 Reserved

D5 Enable CRT 64-stage threshold full

0: using CRT 32-stage threshold full

1: using CRT 64-stage threshold full

D4 CRT/CPU Threshold High Bit[4]

D3 CRT/Engine Threshold High Bit[4]

D2 CRT/CPU Arbitration Threshold Low Bit[4]

D1 Enable Flat Panel Data/Control Out PAD high driving

0: Disable

1: Enable

D0 Select PCLK-out or debug mode of the pin ENVCO

0: Select PCLK-out

1: Select debug mode on UMA mode

9.8. 2D GRAPHICS ENGINE REGISTERS

9.8.1. REGISTER FORMAT FOR GENERAL ENGINE FUNCTIONS

Sinbad integrated graphics controller supports a powerful graphics engine to enhance the performance. The functions of the graphics engine in Sinbad include BitBlt, Color Expansion,

Enhanced Color Expansion, Line Drawing, Transparent BitBlt, Multiple Scan-line and Trapezoid Fill.

Since the register formats for the line drawing, transparent BitBlt, multiple scan-line and trapezoid fill are different from those of the other general engine functions, we would like to describe these five register formats separately in the following paragraphs:

Register Format for General Engine Functions

The following table shows the register format for the general Graphics Engine functions. The general Graphics Engine functions are BitBlt, Color Expansion and Enhanced Color Expansion.

Table 9.8-1 Table of General Engine Register

D[31:24]	D[23:16]	D[15:08]	D[07:00]	I/O ADDRESS
Source Base Address				8200h
Reserved		Source Pitch		8204h
Source X		Source Y		8208h
Destination X		Destination Y		820Ch
Destination Base Address				8210h
Destination Height		Destination Pitch		8214h
Rectangular Height		Rectangular Width		8218h
Pattern FG (Foreground) Color				821Ch
Pattern BG (Background) Color				8220h
Source FG (Foreground) Color				8224h
Source BG (Background) Color				8228h
Mask3	Mask2	Mask1	Mask0	822Ch
Mask7	Mask6	Mask5	Mask4	8230h
Top Clipping		Left Clipping		8234h
Bottom Clipping		Right Clipping		8238h
Command				823Ch
Command Queue Status				8240h
Pattern 3	Pattern 2	Pattern 1	Pattern 0	8300h
Pattern 7	Pattern 6	Pattern 5	Pattern 4	8304h
Pattern 11	Pattern 10	Pattern 9	Pattern 8	8308h
Pattern 15	Pattern 14	Pattern 13	Pattern 12	830Ch

Pattern 19	Pattern 18	Pattern 17	Pattern 16	8310h
Pattern 23	Pattern 22	Pattern 21	Pattern 20	8314h
Pattern 27	Pattern 26	Pattern 25	Pattern 24	8318h
Pattern 31	Pattern 30	Pattern 29	Pattern 28	831Ch
Pattern 35	Pattern 34	Pattern 33	Pattern 32	8320h
Pattern 39	Pattern 38	Pattern 37	Pattern 36	8324h
Pattern 43	Pattern 42	Pattern 41	Pattern 40	8328h
Pattern 47	Pattern 46	Pattern 45	Pattern 44	832Ch
Pattern 51	Pattern 50	Pattern 49	Pattern 48	8330h
Pattern 55	Pattern 54	Pattern 53	Pattern 52	8334h
Pattern 59	Pattern 58	Pattern 57	Pattern 56	8338h
Pattern 63	Pattern 62	Pattern 61	Pattern 60	833Ch
Pattern 67	Pattern 66	Pattern 65	Pattern 64	8340h
Pattern 71	Pattern 70	Pattern 69	Pattern 68	8344h
Pattern 75	Pattern 74	Pattern 73	Pattern 72	8348h
Pattern 79	Pattern 78	Pattern 77	Pattern 76	834Ch
Pattern 83	Pattern 82	Pattern 81	Pattern 80	8350h
Pattern 87	Pattern 86	Pattern 85	Pattern 84	8354h
Pattern 91	Pattern 90	Pattern 89	Pattern 88	8358h
Pattern 95	Pattern 94	Pattern 93	Pattern 92	835Ch
Pattern 99	Pattern 98	Pattern 97	Pattern 96	8360h
Pattern 103	Pattern 102	Pattern 101	Pattern 100	8364h
Pattern 107	Pattern 106	Pattern 105	Pattern 104	8368h
Pattern 111	Pattern 110	Pattern 109	Pattern 108	836Ch
Pattern 115	Pattern 114	Pattern 113	Pattern 112	8370h
Pattern 119	Pattern 118	Pattern 117	Pattern 116	8374h
Pattern 123	Pattern 122	Pattern 121	Pattern 120	8378h
Pattern 127	Pattern 126	Pattern 125	Pattern 124	837Ch
Pattern 131	Pattern 130	Pattern 129	Pattern 128	8380h
Pattern 135	Pattern 134	Pattern 133	Pattern 132	8384h
Pattern 139	Pattern 138	Pattern 137	Pattern 136	8388h

Pattern 143	Pattern 142	Pattern 141	Pattern 140	838Ch
Pattern 147	Pattern 146	Pattern 145	Pattern 144	8390h
Pattern 151	Pattern 150	Pattern 149	Pattern 148	8394h
Pattern 155	Pattern 154	Pattern 153	Pattern 152	8398h
Pattern 159	Pattern 158	Pattern 157	Pattern 156	839Ch
Pattern 163	Pattern 162	Pattern 161	Pattern 160	83A0h
Pattern 167	Pattern 166	Pattern 165	Pattern 164	83A4h
Pattern 171	Pattern 170	Pattern 169	Pattern 168	83A8h
Pattern 175	Pattern 174	Pattern 173	Pattern 172	83ACh
Pattern 179	Pattern 178	Pattern 177	Pattern 176	83B0h
Pattern 183	Pattern 182	Pattern 181	Pattern 180	83B4h
Pattern 187	Pattern 186	Pattern 185	Pattern 184	83B8h
Pattern 191	Pattern 190	Pattern 189	Pattern 188	83BCh
Pattern 195	Pattern 194	Pattern 193	Pattern 192	83C0h
Pattern 199	Pattern 198	Pattern 197	Pattern 196	83C4h
Pattern 203	Pattern 202	Pattern 201	Pattern 200	83C8h
Pattern 207	Pattern 206	Pattern 205	Pattern 204	83CCh
Pattern 211	Pattern 210	Pattern 209	Pattern 208	83D0h
Pattern 215	Pattern 214	Pattern 213	Pattern 212	83D4h
Pattern 219	Pattern 218	Pattern 217	Pattern 216	83D8h
Pattern 223	Pattern 222	Pattern 221	Pattern 220	83DCh
Pattern 227	Pattern 226	Pattern 225	Pattern 224	83E0h
Pattern 231	Pattern 230	Pattern 229	Pattern 228	83E4h
Pattern 235	Pattern 234	Pattern 233	Pattern 232	83E8h
Pattern 239	Pattern 238	Pattern 237	Pattern 236	83ECh
Pattern 243	Pattern 242	Pattern 241	Pattern 240	83F0h
Pattern 247	Pattern 246	Pattern 245	Pattern 244	83F4h
Pattern 251	Pattern 250	Pattern 249	Pattern 248	83F8h
Pattern 255	Pattern 254	Pattern 253	Pattern 252	83FCh

Source Base Address

Register Type: Read/Write

Read/Write Port: 8200h~8203h

D[31:23] Reserved

D[22:0] Base Linear Address of Source Bitmap in Byte

Limit: Source Bitmap Addressing Range is from 0 to 8M,

Quad-Word Boundary in BitBlt,

Byte Boundary in Enhanced Color Expansion.

Source Pitch

Register Type: Read/Write

Read/Write Port: 8204h~8205h

D[15:13] Reserved

D[12:0] Row Pitch of Source Bitmap in Byte.

Limit: Double Word Boundary in BitBlt,

Byte Boundary in Color Expansion and Enhanced Color Expansion.

Rectangle Source Y

Register Type: Read/Write

Read/Write Port: 8208h~8209h

D[15:12] Reserved

D[11:0] Started Y Coordinate of Source Bitmap in Pixel

Rectangle Source X

Register Type: Read/Write

Read/Write Port: 820Ah~820Bh

D[15:12] Reserved

D[11:0] Started X Coordinate of Source Bitmap in Pixel

Rectangle Destination Y

Register Type: Read/Write

Read/Write Port: 820Ch~820Dh

D[15:12] Reserved

D[11:0] Started Y Coordinate of Destination Bitmap in Pixel

Rectangle Destination X

Register Type: Read/Write

Read/Write Port: 820Eh~820Fh

D[15:12] Reserved

D[11:0] Started X Coordinate of Destination Bitmap in Pixel

Destination Base Address

Register Type: Read/Write

Read/Write Port: 8210h~8213h

D[31:23] Reserved

D[22:0] Base Linear Address of Destination Bitmap in Byte

Limit: Destination Bitmap Addressing Range is from 0 to 8M,

Quad-Word Boundary.

Destination Pitch

Register Type: Read/Write

Read/Write Port: 8214h~8215h

D[15:13] Reserved

D[12:0] Row Pitch of Destination Bitmap in Byte

Limit: Double Word Boundary.

Destination Height

Register Type: Read/Write

Read/Write Port: 8216h~8217h

D[15:13] Reserved

D[12:0] Device Height of Destination Bitmap in Pixel

Rectangular Width

Register Type: Read/Write

Read/Write Port: 8218h~8219h

D[15:13] Reserved

D[12:0] Destination Rectangular Drawing Width of Bitmap in Pixel

Rectangular Height

Register Type: Read/Write

Read/Write Port: 821Ah~821Bh

D[15:13] Reserved

D[12:0] Destination Rectangular Drawing Height of Bitmap in Pixel

Pattern Foreground Color

Register Type: Read/Write

Read/Write Port: 821Ch~821Fh

D[31:0] Foreground Color Register of Pattern

Pattern Background Color

Register Type: Read/Write

Read/Write Port: 8220h~8223h

D[31:0] Background Color Register of Pattern

Source Foreground Color

Register Type: Read/Write

Read/Write Port: 8224h~8227h

D[31:0] Foreground Color Register of Source

Source Background Color

Register Type: Read/Write

Read/Write Port: 8228h~822Bh

D[31:0] Background Color Register of Source

Mono Mask Register

Register Type: Read/Write

Read/Write Port: 822Ch~8233h

D[63:0] Monochrome Mask Register of Pattern

Left Clipping

Register Type: Read/Write

Read/Write Port: 8234h~8235h

D[15:0] Left Bound of Rectangular Clipping in Pixel

Limit:In the 2's complement format.

Top Clipping

Register Type: Read/Write

Read/Write Port: 8236h~8237h

D[15:0] Top Bound of Rectangular Clipping in Pixel

Limit:In the 2's complement format.

Right Clipping

Register Type: Read/Write

Read/Write Port: 8238h~8239h

D[15:0] Right Bound of Rectangular Clipping in Pixel

Limit:In the 2's complement format.

Bottom Clipping

Register Type: Read/Write

Read/Write Port: 823Ah~823Bh

D[15:0] Bottom Bound of Rectangular Clipping in Pixel

Limit:In the 2's complement format.

Command Register

Register Type: Read/Write

Read/Write Port: 823Ch~823Fh

D[31:27] Reserved

D26 Rectangular Clipping Merge Control

0:Merge clipping bound with screen bound

1:Do not merge clipping bound with screen bound

D[25:24] Reserved

D[23:21] Enhanced Color Expansion Pixel Preset

Limit: Preset must "000" in color expansion command

D20 Transparent Control

0: Opaque

1: Transparent

D19 Reserved

D18 Rectangular Clipping Control

0: Disable rectangular clipping logic

1: Enable rectangular clipping logic

D17 Y direction control

0: Y counter decrease

1: Y counter increase

D16 X direction control

0: X counter decrease

1: X counter increase

D[15:8] 256 Raster Operations

D[7:6] Pattern select bit 1-0

00: Pattern is from pattern foreground color register

01: Pattern is from pattern register

10: Pattern is from monochrome mask register

11: Reserved

D[5:4] Source select

00: Source is from video memory

01: Source is from CPU-driven BitBlt buffer

10: Reserved

11: Reserved

D[3:0] Command type select Bit[3:0]

0000: BitBlt

0001: Color Expansion

0010: Enhanced Color Expansion

0011: Multiple Scanline

0100: Line Draw

0101: Trapezoid Fill

0110: Transparent BitBlt

Others: Reserved

Command Queue Status

Register Type: Read

Read/Write Port: 8240h~8243h

D31 2D graphics engine is idle

0: 2D graphics engine is busy

1: 2D graphics engine is idle

D30 3D engine is idle

0: 3D engine is busy

1: 3D engine is idle

D29 Command queue is empty

0: Command queue is not empty

1: Command queue is empty

D[28:24]Current CPU-driven BitBlt buffer stages Bit[4:0]

D23 Status of enhanced color expansion command

0: Command is not in queue

1: Command is in queue

D[22:13]reserved

D[12:0] Available queue length Bit[12:0]

Pattern Register n

Register Type: Read/Write

Read/Write Port: 8300h~833Fh for 256-color

8300h~837Fh for high-color

8300h~83FFh for true-color

D[7: 0] For BitBlt and Enhanced Color Expansion function, these registers store the 8x8 color pattern bitmap.

For Color Expansion function, the registers from 8300h to 847Fh store the monochrome bitmap, thus it can expand 3072 pixels at one command.

9.8.2. REGISTER FORMAT FOR LINE DRAWING

The register format for Line-Drawing is shown in the following table.

Table 9.8-2 Table of Line-Drawing Registers

D[31:24]	D[23:16]	D[15:08]	D[07:00]	I/O ADDRESS
Y0		X0		8208h
Y1		X1		820Ch
Destination Base Address				8210h
Destination Height		Destination Pitch		8214h
Style Period		Line Count		8218h
FG (Foreground) Color				821Ch
BG (Background) Color				8220h
Line Style 0				822Ch
Line Style 1				8230h

Top Clipping	Left Clipping	8234h
Bottom Clipping	Right Clipping	8238h
Command		823Ch
Command Queue Status		8240h
Y2	X2	8300h
...	...	...
Y97	X97	847Ch

X0

Register Type: Read/Write

Read/Write Port: 8208h~8209h

D[15:0] The X-start Coordinate of the First Line

Limit: For normal resolution mode it is in the 12.0 format,for high resolution mode it is in the 12.4 format.

Y0

Register Type: Read/Write

Read/Write Port: 820Ah~820Bh

D[15:0] The Y-start Coordinate of the First Line

Limit: For normal resolution mode it is in the 12.0 format,for high resolution mode it is in the 12.4 format.

X1

Register Type: Read/Write

Read/Write Port: 820Ch~820Dh

D[15:0] The X-end Coordinate of the First Line and X-start Coordinate of the Second Line

Limit: For normal resolution mode it is in the 12.0 format,for high resolution mode it is in the 12.4 format.

Y1

Register Type: Read/Write

Read/Write Port: 820Eh~820Fh

D[15:0] The Y-end Coordinate of the First Line and Y-start Coordinate of the Second Line

Limit: For normal resolution mode it is in the 12.0 format,For high resolution mode it is in the 12.4 format.

Destination Base Address

Register Type: Read/Write

Read/Write Port: 8210h~8213h

D[31:23]Reserved

D[22:0] Base Linear Address of Destination Bitmap in Byte

Limit: Destination Bitmap Addressing Range is from 0 to 8M,Quad-Word Boundary.

Destination Pitch

Register Type: Read/Write

Read/Write Port: 8214h~8215h

D[15:13] Reserved

D[12:0] Row Pitch of Destination Bitmap in Byte

Limit: Double Word Boundary

Destination Height

Register Type: Read/Write

Read/Write Port: 8216h~8217h

D[15:13] Reserved

D[12:0] Device Height of Destination Bitmap in Pixel

Line Count

Register Type: Read/Write

Read/Write Port: 8218h~8219h

D[15:7] Reserved

D[6:0] Total Line Count

Limit: The range is from 1 to 97.

Style Period

Register Type: Read/Write

Read/Write Port: 821Ah~821Bh

D[15:6] Reserved

D[5:0] Period of the Line Style in Pixel

Limit: A value of 0 equals 1 pixel.

Foreground Color

Register Type: Read/Write

Read/Write Port: 821Ch~821Fh

D[31:0] Foreground Color of the Line Style

Background Color

Register Type: Read/Write

Read/Write Port: 8220h~8223h

D[31:0] Background Color of the Line Style

Line Style

Register Type: Read/Write

Read/Write Port: 822Ch~8233h

D[63:0] Pattern of the Line Style

Left Clipping

Register Type: Read/Write

Read/Write Port: 8234h~8235h

D[15:0] Left Bound of Rectangular Clipping in Pixel

Limit: In the 2's complement format.

Top Clipping

Register Type: Read/Write

Read/Write Port: 8236h~8237h

D[15:0] Top Bound of Rectangular Clipping in Pixel

Limit: In the 2's complement format.

Right Clipping

Register Type: Read/Write

Read/Write Port: 8238h~8239h

D[15:0] Right Bound of Rectangular Clipping in Pixel

Limit: In the 2's complement format.

Bottom Clipping

Register Type: Read/Write

Read/Write Port: 823Ah~823Bh

D[15:0] Bottom Bound of Rectangular Clipping in Pixel

Limit: In the 2's complement format.

Command Register

Register Type: Read/Write

Read/Write Port: 823Ch~823Fh

D[31:27]Reserved

D26 Rectangular Clipping Merge Control

0:Merge clipping bound with screen bound

1:Do not merge clipping bound with screen bound

D[25:24]Reserved

D23 Line Style Control

0:Disable line style

1:Enable line style

D22 Style counter reset control

0:Style counter will be reset

1:Style counter will not be reset

D21 Line drawing last pixel control

0:Last pixel will be drawn

1:Last pixel will not be drawn

D20 Transparent Control

0:Opaque

1:Transparent

D19 Line Resolution Control

0:Disable high resolution line drawing

1:Enable high resolution line drawing

D18 Rectangular Clipping Control

0:Disable rectangular clipping logic

1:Enable rectangular clipping logic

D[17:16] Reserved

D[15:8] 256 Raster Operations

D[7:4] Reserved

D[3:0] Command type select Bit[3:0]

0000: BitBlt

0001: Color Expansion

0010: Enhanced Color Expansion

0011: Multiple Scanline

0100: Line Draw

0101: Trapezoid Fill

0110: Transparent BitBlt

Others: Reserved

Command Queue Status

Register Type: Read

Read/Write Port: 8240h~8243h

D31 2D graphics engine is idle

0: 2D graphics engine is busy

1:2D graphics engine is idle

D30 3D engine is idle

0:3D engine is busy

1:3D engine is idle

D29 Command queue is empty

0:Command queue is not empty

1:Command queue is empty

D[28:24]Current CPU-driven BitBlt buffer stages Bit[4:0]

D23 Status of enhanced color expansion command

0:Command is not in queue

1:Command is in queue

D[22:13]Reserved

D[12:0] Available queue length Bit[12:0]

Points

Register Type: Read/Write

Read/Write Port: 8300h~847Fh

D[31:16]The Y coordinate of the N-th point

D[15:0] The X coordinate of the N-th point

9.8.3. REGISTER FORMAT FOR TRANSPARENT BITBLT

The register format for Transparent BitBlt is shown in the following table.

Table 9.8-3 Table of Transparent Bitblt Registers

D[31:24]	D[23:16]	D[15:08]	D[07:00]	I/O ADDRESS
Source Base Address				8200h
Reserved		Source Pitch		8204h
Source X		Source Y		8208h
Destination X		Destination Y		820Ch
Destination Base Address				8210h
Destination Height		Destination Pitch		8214h
Rectangular Height		Rectangular Width		8218h
High Value of Destination Color Key				821Ch
Low Value of Destination Color Key				8220h
High Value of Source Color Key				8224h
Low Value of Source Color Key				8228h
Top Clipping		Left Clipping		8234h
Bottom Clipping		Right Clipping		8238h
Command				823Ch
Command Queue Status				8240h

Source Base Address

Register Type: Read/Write

Read/Write Port: 8200h~8203h

D[31:23]Reserved

D[22:0] Base Linear Address of Source Bitmap in Byte

Limit: Source Bitmap Addressing Range is from 0 to 8M,Quad-Word Boundary.

Source Pitch

Register Type: Read/Write

Read/Write Port: 8204h~8205h

D[15:13]Reserved

D[12:0] Row Pitch of Source Bitmap in Byte

Limit: Double Word Boundary.

Rectangle Source Y

Register Type: Read/Write

Read/Write Port: 8208h~8209h

D[15:12]Reserved

D[11:0] Started Y Coordinate of Source Bitmap in Pixel

Rectangle Source X

Register Type: Read/Write

Read/Write Port: 820Ah~820Bh

D[15:12]Reserved

D[11:0] Started X Coordinate of Source Bitmap in Pixel

Rectangle Destination Y

Register Type: Read/Write

Read/Write Port: 820Ch~820Dh

D[15:12]Reserved

D[11:0] Started Y Coordinate of Destination Bitmap in Pixel

Rectangle Destination X

Register Type: Read/Write

Read/Write Port: 820Eh~820Fh

D[15:12]Reserved

D[11:0] Started X Coordinate of Destination Bitmap in Pixel

Destination Base Address

Register Type: Read/Write

Read/Write Port: 8210h~8213h

D[31:0] Base Linear Address of Destination Bitmap in Byte

Limit: Destination Bitmap Addressing Range is from 0 to 8M, Quad-Word Boundary.

Destination Pitch

Register Type: Read/Write

Read/Write Port: 8214h~8215h

D[15:13]Reserved

D[12:0] Row Pitch of Destination Bitmap in Byte

Limit:Double Word Boundary.

Destination Height

Register Type: Read/Write

Read/Write Port: 8216h~8217h

D[15:13]Reserved

D[12:0] Device Height of Destination Bitmap in Pixel

Rectangular Width

Register Type: Read/Write

Read/Write Port: 8218h~8219h

D[15:13]Reserved

D[12:0] Destination Rectangular Drawing Width of Bitmap in Pixel

Rectangular Height

Register Type: Read/Write

Read/Write Port: 821Ah~821Bh

D[15:13]Reserved

D[12:0] Destination Rectangular Drawing Height of Bitmap in Pixel

High Value of Destination Color Key

Register Type: Read/Write

Read/Write Port: 821Ch~821Fh

D[31:0] High Value of Destination Color Key

Low Value of Destination Color Key

Register Type: Read/Write

Read/Write Port: 8220h~8223h

D[31:0] Low Value of Destination Color Key

High Value of Source Color Key

Register Type: Read/Write

Read/Write Port: 8224h~8227h

D[31:0] High Value of Source Color Key

Low Value of Source Color Key

Register Type: Read/Write

Read/Write Port: 8228h~822Bh

D[31:0] Low Value of Source Color Key

Left Clipping

Register Type: Read/Write

Read/Write Port: 8234h~8235h

D[15:0] Left Bound of Rectangular Clipping in Pixel

Limit: In the 2's complement format.

Top Clipping

Register Type: Read/Write

Read/Write Port: 8236h~8237h

D[15:0] Top Bound of Rectangular Clipping in Pixel

Limit: In the 2's complement format.

Right Clipping

Register Type: Read/Write

Read/Write Port: 8238h~8239h

D[15:0] Right Bound of Rectangular Clipping in Pixel

Limit: In the 2's complement format.

Bottom Clipping

Register Type: Read/Write

Read/Write Port: 823Ah~823Bh

D[15:0] Bottom Bound of Rectangular Clipping in Pixel

Limit: In the 2's complement format.

Command Register

Register Type: Read/Write

Read/Write Port: 823Ch~823Fh

D[31:27]Reserved

D26 Rectangular Clipping Merge Control

0:Merge clipping bound with screen bound

1:Do not merge clipping bound with screen bound

D[25:19]Reserved

D18 Rectangular Clipping Control

0:Disable rectangular clipping logic

1:Enable rectangular clipping logic

D17 Y direction control

0:Y counter decrease

1:Y counter increase

D16 X direction control

0:X counter decrease

1:X counter increase

D[15:12]Reserved

D[11:8] Raster Operation Bit[3:0]

D[7:6] Reserved

D[5:4] Source select

00:Source is from video memory

01:Source is from CPU-driven BitBlt buffer

10:Reserved

11:Reserved

D[3:0] Command type select Bit[3:0]

0000:BitBlt

0001:Color Expansion

0010:Enhanced Color Expansion

0011:Multiple Scanline

0100:Line Draw

0101:Trapezoid Fill

0110:Transparent BitBlt

Others: Reserved

Command Queue Status

Register Type: Read

Read/Write Port: 8240h~8243h

D31 2D graphics engine is idle

0:2D graphics engine is busy

1:2D graphics engine is idle

D30 3D engine is idle

0:3D engine is busy

1:3D engine is idle

D29 Command queue is empty

0:Command queue is not empty

1:Command queue is empty

D[28:24]Current CPU-driven BitBlt buffer stages Bit[4:0]

D23 Status of enhanced color expansion command

0:Command is not in queue

1:Command is in queue

D[22:13]reserved

D[12:0] Available queue length Bit[12:0]

9.8.4. REGISTER FORMAT FOR MULTIPLE SCAN-LINE

The register format for Multiple Scan-line is shown in the following table.

Table 9.8-4 Table of Multiple Scan-line Registers

D[31:24]	D[23:16]	D[15:08]	D[07:00]	I/O ADDRESS
Y Start		Scan-Line Count		8208h
X0 End		X0 Start		820Ch
Destination Base Address				8210h
Destination Height		Destination Pitch		8214h
Pattern FG (Foreground) Color				821Ch
Pattern BG (Background) Color				8220h
Mask3	Mask2	Mask1	Mask0	822Ch
Mask7	Mask6	Mask5	Mask4	8230h
Top Clipping		Left Clipping		8234h
Bottom Clipping		Right Clipping		8238h
Command				823Ch
Command Queue Status				8240h
X1 End		X1 Start		8244h
Pattern 3	Pattern 2	Pattern 1	Pattern 0	8300h
....	....	....	....	....
Pattern 63	Pattern 62	Pattern 61	Pattern 60	833Ch
X2 End		X2 Start		8340h

....	....	....
X81 End	X81 Start	847Ch

Scan-Line Count

Register Type: Read/Write

Read/Write Port: 8208h~8209h

D[15:7] Reserved

D[6:0] Total Scan-Line Count

Limit:The range is from 1 to 82 for 256-color,

1 to 66 for high-color,

1 to 34 for true-color.

Y Start

Register Type: Read/Write

Read/Write Port: 820Ah~820Bh

D[15:12]Reserved

D[11:0] The Y-start Coordinate of the First Scan-Line

X0 Start

Register Type: Read/Write

Read/Write Port: 820Ch~820Dh

D[15:12]Reserved

D[11:0] The X-start Coordinate of the First Scan-Line

X0 End

Register Type: Read/Write

Read/Write Port: 820Eh~820Fh

D[15:12]Reserved

D[11:0] The X-end Coordinate of the First Scan-Line

Destination Base Address

Register Type: Read/Write

Read/Write Port: 8210h~8213h

D[31:0] Base Linear Address of Destination Bitmap in Byte

Limit:Destination Bitmap Addressing Range is from 0 to 8M,Quad-Word Boundary

Destination Pitch

Register Type: Read/Write

Read/Write Port: 8214h~8215h

D[15:13]Reserved

D[12:0] Row Pitch of Destination Bitmap in Byte

Limit:Double Word Boundary

Destination Height

Register Type: Read/Write

Read/Write Port: 8216h~8217h

D[15:13]Reserved

D[12:0] Device Height of Destination Bitmap in Pixel

Pattern Foreground Color

Register Type: Read/Write

Read/Write Port: 821Ch~821Fh

D[31:0] Foreground Color Register of Pattern

Pattern Background Color

Register Type: Read/Write

Read/Write Port: 8220h~8223h

D[31:0] Background Color Register of Pattern

Mono Mask Register

Register Type: Read/Write

Read/Write Port: 822Ch~8233h

D[63:0] Monochrome Mask Register of Pattern

Left Clipping

Register Type: Read/Write

Read/Write Port: 8234h~8235h

D[15:0] Left Bound of Rectangular Clipping in Pixel

Limit:In the 2's complement format.

Top Clipping

Register Type: Read/Write

Read/Write Port: 8236h~8237h

D[15:0] Top Bound of Rectangular Clipping in Pixel

Limit:In the 2's complement format.

Right Clipping

Register Type: Read/Write

Read/Write Port: 8238h~8239h

D[15:0] Right Bound of Rectangular Clipping in Pixel

Limit:In the 2's complement format.

Bottom Clipping

Register Type: Read/Write

Read/Write Port: 823Ah~823Bh

D[15:0] Bottom Bound of Rectangular Clipping in Pixel

Limit:In the 2's complement format.

Command Register

Register Type: Read/Write

Read/Write Port: 823Ch~823Fh

D[31:27]Reserved

D26 Rectangular Clipping Merge Control

0:Merge clipping bound with screen bound

1:Do not merge clipping bound with screen bound

D[25:22] Reserved

D21 Scan-line last pixel control

0:Last pixel will be drawn

1:Last pixel will not be drawn

D20 Transparent Control

0:Opaque

1:Transparent

D19 Reserved

D18 Rectangular Clipping Control

0:Disable rectangular clipping logic

1:Enable rectangular clipping logic

D[17:16] Scan-line direction select bit 1-0

00:Draw scanlines upward

01:Draw scanlines at a specified vertical position

10:Draw scanlines downward

11:Reserved

D[15:8] 256 Raster Operations

D[7:6] Pattern select bit 1-0

00:Pattern is from pattern foreground color register

01:Pattern is from pattern register

10:Pattern is from monochrome mask register

11:Reserved

D[5:4] Reserved

D[3:0] Command type select Bit[3:0]

0000: BitBlt

0001: Color Expansion

0010: Enhanced Color Expansion

0011: Multiple Scanline

0100: Line Draw

0101: Trapezoid Fill

0110: Transparent BitBlt

Others: Reserved

Command Queue Status

Register Type: Read

Read/Write Port: 8240h~8243h

D31 2D graphics engine is idle

0:2D graphics engine is busy

1:2D graphics engine is idle

D30 3D engine is idle

0:3D engine is busy

1:3D engine is idle

D29 Command queue is empty

0:Command queue is not empty

1:Command queue is empty

D[28:24]Current CPU-driven BitBlt buffer stages Bit[4:0]

D23 Status of enhanced color expansion command

0:Command is not in queue

1:Command is in queue

D[22:13]Reserved

D[12:0] Available queue length Bit[12:0]

X1 Start

Register Type: Read/Write

Read/Write Port: 8244h~8245h

D[15:12]Reserved

D[11:0] The X-start Coordinate of the Second Scan-Line

X1 End

Register Type: Read/Write

Read/Write Port: 8246h~8247h

D[15:12]Reserved

D[11:0] The X-end Coordinate of the Second Scan-Line

Pattern Register n

Register Type: Read/Write

Read/Write Port: 8300h~833Fh for 256-color

8300h~837Fh for high-color

8300h~83FFh for true-color

D[7:0] For 256-color, high-color and true-color mode, these registers store the 8x8 color pattern bitmap.

Points

Register Type: Read/Write

Read/Write Port: 8340h~847Fh for 256-color

8380h~847Fh for high-color

8400h~847Fh for true-color

D[31:28] Reserved

D[27:16] The X-end coordinate of the N-th Scan-line

D[15:12] Reserved

D[11:0] The X-start coordinate of the N-th Scan-line

9.8.5. REGISTER FORMAT FOR TRAPEZOID FILL

The register format for Trapezoid Fill is shown in the following table.

Table 9.8-5 Table of Trapezoid Fill Registers

D[31:24]	D[23:16]	D[15:08]	D[07:00]	I/O ADDRESS
Y Start		Trapezoid Height		8208h
Right Edge X Start		Left Edge X Start		820Ch
Destination Base Address				8210h
Destination Height		Destination Pitch		8214h
Pattern FG (Foreground) Color				821Ch
Pattern BG (Background) Color				8220h
Mask3	Mask2	Mask1	Mask0	822Ch
Mask7	Mask6	Mask5	Mask4	8230h
Top Clipping		Left Clipping		8234h
Bottom Clipping		Right Clipping		8238h
Command				823Ch
Command Queue Status				8240h
Left Edge Delta Y		Left Edge Delta X		8244h
Right Edge Delta Y		Right Edge Delta X		8248h
Left Edge Error Term				824Ch
Right Edge Error Term				8250h

Trapezoid Height

Register Type: Read/Write

Read/Write Port: 8208h~8209h

D[15:12]Reserved

D[11:0] Height of the trapezoid in pixel

Y Start

Register Type: Read/Write

Read/Write Port: 820Ah~820Bh

D[15:12]Reserved

D[11:0] The Y-start Coordinate

Left Edge X Start

Register Type: Read/Write

Read/Write Port: 820Ch~820Dh

D[15:12]Reserved

D[11:0] The X-start Coordinate of Left Edge

Right Edge X Start

Register Type: Read/Write

Read/Write Port: 820Eh~820Fh

D[15:12]Reserved

D[11:0] The X-start Coordinate of Right Edge

Destination Base Address

Register Type: Read/Write

Read/Write Port: 8210h~8213h

D[31:0] Base Linear Address of Destination Bitmap in Byte

Limit: Destination Bitmap Addressing Range is from 0 to 8M, Quad-Word Boundary

Destination Pitch

Register Type: Read/Write

Read/Write Port: 8214h~8215h

D[15:13]Reserved

D[12:0] Row Pitch of Destination Bitmap in Byte

Limit: Double Word Boundary

Destination Height

Register Type: Read/Write

Read/Write Port: 8216h~8217h

D[15:13]Reserved

D[12:0] Device Height of Destination Bitmap in Pixel

Pattern Foreground Color

Register Type: Read/Write

Read/Write Port: 821Ch~821Fh

D[31:0] Foreground Color Register of Pattern

Pattern Background Color

Register Type: Read/Write

Read/Write Port: 8220h~8223h

D[31:0] Background Color Register of Pattern

Mono Mask Register

Register Type: Read/Write

Read/Write Port: 822Ch~8233h

D[63:0] Monochrome Mask Register of Pattern

Left Clipping

Register Type: Read/Write

Read/Write Port: 8234h~8235h

D[15:0] Left Bound of Rectangular Clipping in Pixel

Limit: In the 2's complement format.

Top Clipping

Register Type: Read/Write

Read/Write Port: 8236h~8237h

D[15:0] Top Bound of Rectangular Clipping in Pixel

Limit: In the 2's complement format.

Right Clipping

Register Type: Read/Write

Read/Write Port: 8238h~8239h

D[15:0] Right Bound of Rectangular Clipping in Pixel

Limit: In the 2's complement format.

Bottom Clipping

Register Type: Read/Write

Read/Write Port: 823Ah~823Bh

D[15:0] Bottom Bound of Rectangular Clipping in Pixel

Limit: In the 2's complement format.

Command Register

Register Type: Read/Write

Read/Write Port: 823Ch~823Fh

D[31:27]Reserved

D26 Rectangular Clipping Merge Control

0:Merge clipping bound with screen bound

1:Do not merge clipping bound with screen bound

D25 Reserved

D24 Right edge major axial selection

0:Y-axial is major

1:X-axial is major

D23 Left edge major axial selection

0:Y-axial is major

1:X-axial is major

D22 Right edge Y direction control

0:Y counter decrease

1:Y counter increase

D21 Right edge X direction control

0:X counter decrease

1:X counter increase

D20 Transparent Control

0:Opaque

1:Transparent

D19 Line Resolution Control

0:Disable high resolution mode

1:Enable high resolution mode

D18 Rectangular Clipping Control

0:Disable rectangular clipping logic

1:Enable rectangular clipping logic

D17 Left edge Y direction control

0:Y counter decrease

1:Y counter increase

D16 Left edge X direction control

0:X counter decrease

1:X counter increase

D[15:8] 256 Raster Operations

D[7:6] Pattern select bit 1-0

00:Pattern is from pattern foreground color register

01:Pattern is from pattern register

10:Pattern is from monochrome mask register

11:Reserved

D[5:4] Reserved

D[3:0] Command type select Bit[3:0]

0000:BitBlt

0001:Color Expansion

0010:Enhanced Color Expansion

0011:Multiple Scanline

0100:Line Draw

0101:Trapezoid Fill

0110:Transparent BitBlt

Others: Reserved

Command Queue Status

Register Type: Read

Read/Write Port: 8240h~8243h

D31 2D graphics engine is idle

0: 2D graphics engine is busy

1:2D graphics engine is idle

D30 3D engine is idle

0:3D engine is busy

1:3D engine is idle

D29 Command queue is empty

0:Command queue is not empty

1:Command queue is empty

D[28:24]Current CPU-driven BitBlt buffer stages Bit[4:0]

D23 Status of enhanced color expansion command

0:Command is not in queue

1:Command is in queue

D[22:13]Reserved

D[12:0] Available queue length Bit[12:0]

Left Edge Delta X

Register Type: Read/Write

Read/Write Port: 8244h~8245h

D[15:0] Delta X of Left edge

Limit: For normal resolution mode it is in the 12.0 format,For high resolution mode it is in the 12.4 format.

Left Edge Delta Y

Register Type: Read/Write

Read/Write Port: 8246h~8247h

D[15:0] Delta Y of Left edge

Limit: For normal resolution mode it is in the 12.0 format,For high resolution mode it is in the 12.4 format.

Right Edge Delta X

Register Type: Read/Write

Read/Write Port: 8248h~8249h

D[15:0] Delta X of Right edge

Limit: For normal resolution mode it is in the 12.0 format,For high resolution mode it is in the 12.4 format.

Right Edge Delta Y

Register Type: Read/Write

Read/Write Port: 824Ah~824Bh

D[15:0] Delta Y of Right edge

Limit: For normal resolution mode it is in the 12.0 format,For high resolution mode it is in the 12.4 format.

Left Edge Error Term

Register Type: Read/Write

Read/Write Port: 824Ch~824Fh

D[31:22]Reserved

D[21:0] Initial Error Term of Left edge

Limit: In the 2's complement format.

Right Edge Error Term

Register Type: Read/Write

Read/Write Port: 8250h~8253h

D[31:22]Reserved

D[21:0] Initial Error Term of Right edge

Limit: In the 2's complement format.

Pattern Register n

Register Type: Read/Write

Read/Write Port: 8300h~833Fh for 256-color

8300h~837Fh for high-color

8300h~83FFh for true-color

D[7:0] For 256-color, high-color and true-color mode, these registers store the 8x8 color pattern bitmap.

9.9. VIDEO ACCELERATOR REGISTERS

Table 9.9-1 Table of Video Accelerator Registers

INDEX(3D4)	VIDEO ACCELERATOR REGISTER (3D5)
80h	Password/Identification Register
81h	Video Window Horizontal Display Start Low Register
82h	Video Window Horizontal Display End Low Register
83h	Video Window Horizontal Display Overflow Register
84h	Video Window Vertical Display Start Low Register
85h	Video Window Vertical Display End Low Register
86h	Video Window Vertical Display Overflow Register
87h	Reserved
88h	Reserved

89h	Video Frame Buffer Overflow Register
8Ah	Video Display Frame Buffer Starting Address Low Register
8Bh	Video Display Frame Buffer Starting Address Middle Register
8Ch	Video Frame Buffer Offset Low Register
8Dh	Reserved
8Eh	Video Frame Buffer Offset Address High Register
8Fh	Reserved
90h	Reserved
91h	Reserved
92h	Horizontal Up Scaling Factor and Horizontal Interpolation Accuracy Factor Register
93h	Vertical Up Scaling Factor Register
94h	Horizontal Scaling Factor Integer Register
95h	Video Overlay Color Key Blue Low Value Register
96h	Video Overlay Color Key Green Low Value Register
97h	Video Overlay Color Key Red Low Value Register
98h	Video Control Misc. Register 0
99h	Reserved
9Ah	Video Chroma Key B/Y Low Value Register
9Bh	Video Chroma Key G/U Low Value Register
9Ch	Video Chroma Key R/V Low Value Register
9Dh	Video Control Misc. Register 3
9Eh	Video Playback Threshold Low Value Register
9Fh	Video Playback Threshold High Value Register
A0h	Line Buffer Size Register
A1h	Video Overlay Color Key Blue High Value Register
A2h	Video Overlay Color Key Green High Value Register
A3h	Video Overlay Color Key Red High Value Register
A4h	Video Chroma Key B/Y High Value Register
A5h	Video Chroma Key G/U High Value Register
A6h	Video Chroma Key R/V High Value Register

A7h	Reserved
A8h	Reserved
A9h	Key Overlay Operation Mode Register
AAh~B2h	Reserved
B3h	Contrast Enhancement Mean Value Sampling Rate Factor Register
B4h	Brightness Register
B5h	Contrast Enhancement Control Register
B6h	Video Misc. Control Register 3
B7h	Video U Plane Starting Address Low Register
B8h	Video U Plane Starting Address Middle Register
B9h	Video UV Plane Starting Address High Register
BAh	Video V Plane Starting Address Low Register
BBh	Video V Plane Starting Address Middle Register
BCh	Video UV Plane Offset Register
BDh	Video UV Plane Offset High Register
BEh	Video Misc. Control Register 4

Password/Identification Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 80h

Default: 00h

D[7:0] Password/identification Bit[7:0]

Description:

If 86h is written to this register, A1h will be read from this register and all the video extension registers would be unlocked to allow desired change.

If any value other than 86h is written to this register, 21h will be read from this register and all the video extension registers would be locked to prevent unauthorized change.

Video Window Horizontal Display Start Low Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 81h

Default: 00h

D[7:0] Video window horizontal display start Bit[7:0]

Description:

The Video Window Horizontal Display Start Bit[10:0] form the left boundary of the video window. The Bit[10:8] is located in the Video Window Horizontal Display Overflow Register (Index 83h). The boundary is in unit of pixel.

Video Window Horizontal Display End Low Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 82h

Default: 00h

D[7:0] Video window horizontal display end Bit[7:0]

Description:

The Video Window Horizontal Display End Bit[10:0] form the right boundary of the video window. The Bits[10:8] is located in the Video Window Horizontal Display Overflow Register (Index 83h). The boundary is in unit of pixel.

Video Window Horizontal Display Overflow Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 83h

Default: 00h

D[2:0] Video window horizontal display start Bit[10:8]

D3 Reserved

D[6:4] Video window horizontal display end Bit[10:8]

D7 Reserved

Video Window Vertical Display Start Low Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 84h

Default: 00h

D[7:0] Video window vertical display start Bit[7:0]

Description:

The Video Window Vertical Display Start Bit[10:0] form the top boundary of the video window. The Bit[10:8] is located in the Video Window Vertical Display Overflow Register (Index 86h). The boundary is in unit of line.

Video Window Vertical Display End Low Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 85h

Default: 00h

D[7:0] Video window vertical display end Bit[7:0]

Description:

The Video Window Vertical Display End Bit[10:0] form the bottom boundary of the video window. The Bit[10:8] is located in the Video Window Vertical Display Overflow Register (Index 86h). The boundary is in unit of line.

Video Window Vertical Display Overflow Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 86h

Default: 00h

D7 Reserved

D[6:4] Video window horizontal display end Bit[10:8]

D3 Reserved

D[2:0] Video window horizontal display start Bit[10:8]

Video Frame Buffer Overflow Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 89h

Default: 00h

D[7:3] Video display frame buffer starting address Bit[20:16]

D[2:0] Reserved

Video Display Frame Buffer Starting Address Low Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 8Ah

Default: 00h

D[7:0] Video display frame buffer starting address Bit[7:0]

Description:

The Video Display Frame Buffer Starting Address Bit[19:0] form the video display starting address in unit of double-word. The Bit[15:8] are located in the Video Display Frame Buffer Starting Address Middle Register (Index 8Bh). The Bits[19:16] are located in the Video Frame Buffer Overflow Register (Index 89h).

This address could be different from the video capture frame buffer starting address to perform the video display panning function.

Video Display Frame Buffer Starting Address Middle Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 8Bh

Default: 00h

D[7:0] Video display frame buffer starting address Bit[15:8]

Video Frame Buffer Offset Low Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 8Ch

Default: 00h

D[7:0] Video frame buffer offset Bit[7:0]

Description:

The Video Frame Buffer Offset Bit[11:0] form the offset of the video frame buffer. The Bit[11:8] are located in the Video Frame Buffer Offset High Register (Index 8Eh).

The offset defines the size of the scan line of the video data captured in the video frame buffer in unit of double word. It should slightly larger than the actual size of captured video image to avoid the data over stored to next scan line buffer.

Video Frame Buffer Offset Address High Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 8Eh

Default: 00h

D[3:0] Video frame buffer offset Bit[11:8]

D[7:4] Reserved

Horizontal Up Scaling Factor and Horizontal Interpolation Accuracy Factor Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 92h

Default: 00h

D[5:0] Horizontal up scaling factor Bit[5:0]

D[7:6] Horizontal up-scaling interpolation accuracy factor

00: replication

01: 2-phase

10: 4-phase

11: 8-phase

Description:

This field contains the video playback horizontal up scaling factor fraction (HSFF). It is combined with the horizontal scaling factor integer (HSFI) register (Index 94h) to form horizontal scaling. The horizontal size will be scaled to 1/(HSFI+(HSFF/64)). The HSFI should be zero for up-scaling. The HSFI should not be zero for down-scaling.

The Up-scaling interpolation accuracy factor can modify the up-scaling interpolation DDA accuracy phases.

Vertical Up Scaling Factor Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 93h

Default: 00h

D[5:0] Vertical up scaling factor Bit[5:0]

D[7:6] Video frame buffer data format selection Bit[1:0]

For YUV format,

00: UYVY 4:2:2

01: VYUY 4:2:2

10: YUYV 4:2:2

11: YVYU 4:2:2

For RGB format,

00: RGB 5:5:5

01: RGB 5:6:5

Description:

This field contains the video playback vertical up scaling factor (VUSF). The vertical size will be scaled to 64/VUSF. If VUSF=0, the vertical size will not be scaled.

Horizontal Scaling Factor Integer Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 94h

Default: 00h

D[7:4] Reserved

D[3:0] Horizontal Scaling Factor Integer Bit[3:0]

Video Overlay Color Key Blue Low Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 95h

Default: 00h

D[7:0] Blue Key Bit[7:0]

Description:

This register contains the blue video overlay color key low value.

In 8-bit color mode, it is used as the color key low value.

In 16-bit color mode, it is used as the low byte of color key low value.

In 24-bit color mode, it is used as the blue byte of the color key low value.

If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

Video Overlay Color Green Low Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 96h

Default: 00h

D[7:0] Green Key Bit[7:0]

Description:

This register contains the green video overlay color key low value.

In 8-bit color mode, it is invalid.

In 16-bit color mode, it is used as the high byte of color key low value.

In 24-bit color mode, it is used as the green byte of the color key low value.

If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

Video Overlay Color Red Low Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 97h

Default: 00h

D[7:0] Red Key Bit[7:0]

Description:

This register contains the red video overlay color key low value.

In 8-bit color mode, it is invalid.

In 16-bit color mode, it is invalid.

In 24-bit color mode, it is used as the red byte of the color key low value.

If the value of the graphics data is greater than or equal to the color key low value, and lower

than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

Video Control Misc. Register 0

Register Type: Read/Write

Read/Write Port: 3D5, Index 98h

Default: 00h

D7 Reserved

D6 Video format selection

0: Select RGB format

1: Select YUV format

This bit is used with the video frame buffer data format selection field of register CR92 to select the correct video data format.

D5 Reserved

D4 Video only display mode

0: Disable video only display mode

1: Enable video only display mode

The graphics display can be disabled by setting this bit. This can reduce the DRAM bandwidth especially on the full screen video playback mode.

D[3:2] Reserved

D1 Enable video playback

0: Disable video playback

1: Enable video playback

This bit could enable the video playback. When the data of the video frame buffer is fetched by the system, the bandwidth of DRAM may be not enough. The video playback can be disabled to gain the bandwidth but the video will not be played back.

D0 Reserved

Video Control Misc. Register 1

Register Type: Read/Write

Read/Write Port: 3D5, Index 99h

Default: 00h

D[7:0] Reserved

Video Chroma Key B/Y Low Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 9Ah

Default: 00h

D[7:0] Video Chroma B/Y Key Low Bit[7:0]

Description:

This register contains the blue or Y video overlay chroma key low value.

In RGB chroma key mode, it is used as the blue byte of the chroma key low value.

In YUV chroma key mode, it is used as the Y of the chroma key low value.

If the value of the video data is greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced graphics data in the way defined by key operation mode.

Video Chroma Key G/U Low Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 9Bh

Default: 00h

D[7:0] Video Chroma G/U Key Low Bit[7:0]

Description:

This register contains the green or U video overlay chroma key low value.

In RGB chroma key mode, it is used as the green byte of the chroma key low value.

In YUV chroma key mode, it is used as the U of the chroma key low value.

If the value of the video data is greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced graphics data in the way defined by key operation mode.

Video Chroma Key R/V Low Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 9Ch

Default: 00h

D[7:0] Video Chroma R/V Key Low Value Bit[7:0]

Description:

This register contains the red or V video overlay chroma key low value.

In RGB chroma key mode, it is used as the red byte of the chroma key low value.

In YUV chroma key mode, it is used as the V of the chroma key low value.

If the value of the video data is greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced graphics data in the way defined by key operation mode.

Video Control Misc. Register 2

Register Type: Read/Write

Read/Write Port: 3D5, Index 9Dh

Default: 00h

D[7:3] Reserved

D2 Chroma Key Format selection

0: RGB format

1: YUV format

D1 UV format select for video playback

0: CCIR 601 format

1: 2's complement format

D0 Reserved

Video Playback Threshold Low Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 9Eh

Default: 00h

D7 Reserved

D[6:0] Video playback threshold low Bit[6:0]

Description:

This register contains the video line buffer threshold low.

The threshold low defines the video line buffer lower boundary which indicates the line buffer is not enough and the video data should be read from the DRAM.

Video Playback Threshold High Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index 9Fh

Default: 00h

D7 Reserved

D[6:0] Video playback threshold high Bit[6:0]

Description:

This register contains the video line buffer threshold high.

The threshold high defines the video line buffer upper boundary which indicates the data in the video line buffer is enough.

These two thresholds (video playback threshold low and threshold high) should be modified to obtain the maximum performance by compromising with the CRT threshold, video capture threshold, and DRAM refresh rate, etc.

Line Buffer Size Register

Register Type: Read/Write

Read/Write Port: 3D5, Index A0h

Default: 00h

D[7:0] Line Buffer Size Bit[7:0]

Description:

This register should be set to the line buffer size used by playback. The size is in unit of quad-word.

Video Overlay Color Key Blue High Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index A1h

Default: 00h

D[7:0] Blue Key High Value Bit[7:0]

Description:

This register contains the blue video overlay color key high value.

In 8-bit color mode, it is used as the color key high value.

In 16-bit color mode, it is used as the low byte of color key high value.

In 24-bit color mode, it is used as the blue byte of the color key high value.

If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

Video Overlay Color Key Green High Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index A2h

Default: 00h

D[7:0] Green Key High Value Bit[7:0]

Description:

This register contains the green video overlay color key high value.

In 8-bit color mode, it is invalid.

In 16-bit color mode, it is used as the high byte of color key high value.

In 24-bit color mode, it is used as the green byte of the color key high value.

If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

Video Overlay Color Key Red High Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index A3h

Default: 00h

D[7:0] Red Key High Value Bit[7:0]

Description:

This register contains the red video overlay color key high value.

In 8-bit color mode, it is invalid.

In 16-bit color mode, it is invalid.

In 24-bit color mode, it is used as the red byte of the color key high value.

If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

Video Chroma Key B/Y High Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index A4h

Default: 00h

D[7:0] Video Chroma B/Y Key High Value Bit[7:0]

Description:

This register contains the blue or Y video overlay chroma key high value.

In RGB chroma key mode, it is used as the blue byte of the chroma key high value.

In YUV chroma key mode, it is used as the Y of the chroma key high value.

If the value of the video data is the greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced by graphics data in the way defined by key operation mode.

Video Chroma Key G/U High Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index A5h

Default: 00h

D[7:0] Video Chroma G/U Key High Value Bit[7:0]

Description:

This register contains the green or U video overlay chroma key high value.

In RGB chroma key mode, it is used as the green byte of the chroma key high value.

In YUV chroma key mode, it is used as the U of the chroma key high value.

If the value of the video data is the greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced by graphics data in the way defined by key operation mode.

Video Chroma Key R/V High Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index A6h

Default: 00h

D[7:0] Video Chroma R/V Key High Value Bit[7:0]

Description:

This register contains the red or V video overlay chroma key high value.

In RGB chroma key mode, it is used as the red byte of the chroma key high value.

In YUV chroma key mode, it is used as the V of the chroma key high value.

If the value of the video data is the greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced graphics data in the way defined by key operation mode.

Key Overlay Operation Mode Register

Register Type: Read/Write

Read/Write Port: 3D5, Index A9h

Default: 00h

D[7:4] Reserved

D[3:0] Key Overlay Operation Mode Bit[3:0]

Description:

There are two keys for graphics data and video data overlay, which are color key and chroma key. The key overlay operation mode indicates the way the overlay would be performed.

Table 9.9-1 Table of Key Overlay Operation Mode

OPERATION MODE	OPERATION
0000	always select graphics data
0001	select blended data when color key and chroma key,

	otherwise select graphics data
0010	select blended data when color key and not chroma key, otherwise select graphics data
0011	select blended data when color key, otherwise select graphics data
0100	select blended data when not color key and chroma key, otherwise select graphics data
0101	select blended data when chroma key, otherwise select graphics data
0110	select blended data when color key xor chroma key, otherwise select graphics data
0111	select blended data when color key or chroma key, otherwise select graphics data
1000	select blended data when not color key and not chroma key, otherwise select graphics data
1001	select blended data when color key xnor chroma key, otherwise select graphics data
1010	select blended data when not chroma key, otherwise select graphics data
1011	select blended data when color key or not chroma key, otherwise select graphics data
1100	select blended data when not chroma key, otherwise select graphics data
1101	select blended data when not color key or chroma key, otherwise select graphics data
1110	select blended data when not color key or not chroma key, otherwise select graphics data
1111	always select blended data

Contrast Enhancement Mean Value Sampling Rate Factor Register

Register Type: Read/Write

Read/Write Port: 3D5, Index B3h

Default: 00h

D[7:0] Contrast Enhancement Mean Value Sampling Rate Factor Bits[7:0]

Description:

The contrast enhancement needs mean value for each frame. This mean value is calculated by sampling some pixels from one video frame. The sampling rate = Contrast Enhancement Mean Value Sampling Rate Factor / 1024.

Brightness

Register Type: Read/Write

Read/Write Port: 3D5, Index B4h

Default: 00h

D[7:0] Brightness Bit[7:0]

Description:

The Brightness is an 8-bit 2's complement number from -128 to +127. This value is added with the video data to control the brightness.

Contrast Enhancement Control Register

Register Type: Read/Write

Read/Write Port: 3D5, Index B5h

Default: 00h

D[2:0] Contrast Gain Bit[2:0]

000: 1.0

001: 1.0625

010: 1.125

011: 1.1875

100: 1.25

101: 1.3125

110: 1.375

111: 1.4375

D[5:3] Contrast Mean Frame Samples Bit[2:0]

000: 2 frames

001: 4 frames

010: Reserved

011: 8 frames

100: Reserved

101: Reserved

110: Reserved

111: 16 frames

D[7:6] Contrast Mean Pixel Samples Bit[1:0]

00: 2048 pixels

01: 4096 pixels

10: 8192 pixels

11: 16384 pixels

Video Control Misc. Register 3

Register Type: Read/Write

Read/Write Port: 3D5, Index B6h

Default: 00h

D[7:3] Reserved

D2 Enable YUV 420 mode

0: Disable

1: Enable

D[1:0] Reserved

Video U Plane Starting Address Low Register

Register Type: Read/Write

Read/Write Port: 3D5, Index B7h

Default: 00h

D[7:0] Video U Plane Starting Address Low Bit[7:0]

Video U Plane Starting Address Middle Register

Register Type: Read/Write

Read/Write Port: 3D5, Index B8h

Default: 00h

D[7:0] Video U Plane Starting Address Middle Bit[15:8]

Video UV Plane Starting Address High Register

Register Type: Read/Write

Read/Write Port: 3D5, Index B9h

Default: 00h

D[7:4] Video V Plane Starting Address High Bit[19:16]

D[3:0] Video U Plane Starting Address High Bit[19:16]

Video V Plane Starting Address Low Register

Register Type: Read/Write

Read/Write Port: 3D5, Index BAh

Default: 00h

D[7:0] Video V Plane Starting Address Low Bit[7:0]

Video V Plane Starting Address Low Register

Register Type: Read/Write

Read/Write Port: 3D5, Index BBh

Default: 00h

D[7:0] Video V Plane Starting Address Middle Bit[15:8]

Video UV Plane Offset Register

Register Type: Read/Write

Read/Write Port: 3D5, Index BCh

Default: 00h

D[7:0] Video UV Plane Offset Bit[7:0]

9.9.1. VIDEO UV PLANE OFFSET HIGH REGISTER

Register Type: Read/Write

Read/Write Port: 3D5, Index BDh

Default: 00h

D[7:4] Reserved

D[3:0] Video UV Plane Offset Bit[11:8]

9.9.2. VIDEO CONTROL MISC. REGISTER 4

Register Type: Read/Write

Read/Write Port: 3D5, Index BEh

Default: 00h

D[7:5] Reserved

D4 Line Buffer Merge Control

0: Disable

0: Enable

D3 Reserved

D2 Video V Plane Starting Address High Bit20

D1 Video U Plane Starting Address High Bit20

D0 Reserved

9.10. PCI CONFIGURATION REGISTERS

Configuration Register 00h

Register Type: Read

Read Port: 0000h

Default: 63061039h

D[31:16] Device ID

The Device ID of integrated 3D VGA is 6306h

D[15:0] Vendor ID

Integrated Vendor ID is 1039h

Configuration Register 04h

Register Type: Read/Write

Read Port: 0004h

Default: 02200004h

D[26:25] DEVSEL* timing (= 01, Read Only)

00: fast

01: medium (fixed at this value)

10: slow

D21 66 MHz Capable

0: Support 33MHz

1: Support 66 MHz (fixed at this value)

D12 Capabilities List

0: does not implement a list of capabilities

1: implements a list of capabilities

D5 VGA Palette Snoop

0: Disable

1: Enable

D3 Bus Master

0: Device is not a bus master

1: Device is a bus master (fixed at this value)

D1 Memory Space

0: Disable

1: Enable

D0 I/O Space

0: Disable

1: Enable

Configuration Register 08h

Register Type: Read

Read Port: 0008h

Default: 030000AXh

D[31:8] Class Code (= 030000h)

D[7:0] Revision ID (= Axh, for Rev. Ax)

Configuration Register 10h

Register Type: Read/Write

Read Port: 0010h

Default: 00000008h

D[31:0] 32-bit memory base register for 4MB linear frame buffer

Configuration Register 14h

Register Type: Read/Write

Read Port: 0014h

Default: 00000000h

D[31:0] 32-bit memory base register for 64KB memory mapped I/O

Configuration Register 18h

Register Type: Read/Write

Read Port: 0018h

Default: 00000001h

D[31:0] 32-bit I/O base register for 16 I/O space which is reserved for VMI interface

Configuration Register 2Ch

Register Type: Read/Write Once Only

Read Port: 002Ch

Default: 00000000h

D[31:16] Subsystem ID

D[15:0] Subsystem Vendor ID

Configuration Register 30h

Register Type: Read/Write

Read Port: 0030h

Default: 000C0000h

D[31:11] Expansion ROM Base Address

D0 ROM Enable Bit

0: Disable

1: Enable

Configuration Register 3Ch

Register Type: Read/Write

Read Port: 003Ch

Default: 00000100h

If D3 of SRE is 1, then

D[15:8] Interrupt Pin (= 01h, Read Only)

D[7:0] Interrupt Line (= 00h)

If D3 of SRE is 0, then

D[15:8] Interrupt Pin (= 00h, Read Only)

D[7:0] Interrupt Line (= 00h)

9.11. AGP CONFIGURATION REGISTERS

Note: All the registers described in this section can be accessed only when AGP is enable.

Configuration Register 34h

Register Type: Read Only

Read Port: 0034h

Default: 00000050h

D[7:0] Capabilities list offset pointer (Read Only)

Configuration Register 50h

Register Type: Read Only

Read Port: 0050h

Default: 00105C02h

D[23:20] Major revision number

D[19:16] Minor revision number

D[15:8] Pointer to next item

D[7:0] Cap_ID: value 02h identifies the list item as pertaining to AGP register

Configuration Register 54h

Register Type: Read Only

Read Port: 0054h

Default: 01000003h

D[31:24] Maximum number of AGP command requests

D9 Side band addressing support

0: Not support

1: Support

D1 2X mode support

0: Not support

1: Support

D0 1X mode support

0: Not support

1: Support

Configuration Register 58h

Register Type: Read/Write

Read Port: 0058h

Default: 00000000h

D[31:24] Maximum number of AGP requests can be enqueued

D9 1: sideband address mode enable

0: sideband address mode disable

D8 1: AGP enable

0: AGP disable

D1 1: 2X mode enable

0: 2X mode disable

D0 1: 1X mode enable

0: 1X mode disable

Configuration Register 5Ch

Register Type: Read

Read Port: 005Ch

Default: 00000000h

D[15:8] NULL: 00h indicates final item in the capability list

9.12. DIGITAL FLAT PANEL INTERFACE REGISTERS

Panel link horizontal retrace start

Register Type: Read/Write

Read/Write Port:3D5, index C0

D[7:0] PLHRS[7:0]

Panel link horizontal retrace start

Panel link horizontal retrace end/skew

Register Type: Read/Write

Read/Write Port:3D5, index C1

D[7:5] PLHSKEW[2:0]

Panel Link horizontal retrace skew: 0~7 dclk

D[4:0] PLHRE[4:0]

Panel Link horizontal retrace end

Panel link horizontal display start

Register Type: Read/Write

Read/Write Port:3D5, index C2

D[7:0] PLHDES[7:0]

Panel Link horizontal display enable start

Panel link horizontal display end

Register Type: Read/Write

Read/Write Port:3D5, index C3

D[7:0] PLHDEE[7:0]

Panel Link horizontal display enable end

Panel link vertical retrace start

Register Type: Read/Write

Read/Write Port:3D5, index C4

D[7:0] PLVRS[7:0]

Panel Link vertical retrace start

Panel link vertical retrace end/misc.

Register Type: Read/Write

Read/Write Port:3D5, index C5

D7 PLVSPLTY

0: Vertical Sync high active

1: Vertical Sync low active

D6 PLHSPLTY

0: Horizontal Sync high active

1: Horizontal Sync low active

D[5:4] PLMODE[1:0]

00: 12-bit RGB to LVDS/TMDS transmitter

10: 18-bit RGB to LVDS/TMDS transmitter

11: 24-bit RGB to LVDS/TMDS transmitter

D[3:0] PLVRE[3:0]

Panel Link vertical retrace end

Panel link vertical retrace start

Register Type: Read/Write

Read/Write Port:3D5, index C6

D7 ENPLINK

0: Disable Panel Link

1: Enable Panel Link

D6 ENTESTP32K

0: Normal operation

1: Test mode: Enable counter test

D[5:3] PLVRS[10:8]

High bits of vertical retrace start

D[2:0] PLDESKEW[2:0]

Display enable skew: 1~7 dclk

Panel link vertical display enable start: low bits

Register Type: Read/Write

Read/Write Port:3D5, index C7

D[7:0] PLVDES[7:0]

Panel Link vertical display enable start

Panel link vertical display enable end: low bits

Register Type: Read/Write

Read/Write Port:3D5, index C8

D[7:0] PLVDEE[7:0]

Panel Link verticaly display enable end

Panel link interrupt control signal and high bits of vertical display control registers

Register Type: Read/Write

Read/Write Port:3D5, index C9

D7 PLINTCLR

0: Normal

1: Clear Panel Link interrupt request

D6 ENPLINT

0: Disable Panel Link interrupt

1: Enable Panel Link interrupt

D[5:3] PLVDEE[10:8]

High bits of Panel Link display enable end

D[2:0] PLVDES[10:8]

High bits of Panel Link display enable start

Panel link interrupt read back bits

Register Type: Read

Read Port:3D5, index CA

D7 DE only mode

0: Sync and DE mode

1: DE only mode

D6 EnPLCKHDRV

0: Panel Link clock output low driving

1: Panel Link clock output high driving

D[5:4] PLCLKDLY[1:0]

00: no delay Panel Link clock output

01: delay Panel Link clock output 1 ns

10: delay Panel Link clock output 2 ns

11: delay Panel Link clock output 3ns

D3 DIVPLCLK

0: Panel Link clock output frequency is equivalent to DCLK

1: Panel Link clock output frequency is Dclk divided by 2

D2 INVPLCLK

0: Panel Link clock output phase is the same as DCLK

1: Panel Link clock output phase is inverse of DCLK

D1 PLSWITCH

0: Disable Panel Link output pad

1: Enable Panel Link output pad

D0 EnHWINT

0: Disable hardware interrupt: INTAN

1: Enable hardware interrupt: INTAN

Panel link interrupt read back and DDC data/clock

Register Type: Read/write

Read/write Port:3D5, index CB

D7 LSBALIGN, used at 18,12 color mode

0: MSB align

1: LSB align

D6 ENDITHER, enable dither function

0: disable R/G/B data dithering

1: enable R/G/B data dithering at non-24-bit color mode

D5 write Flat Panel DDC clock output : FDDCCLKN

0: pull high DDC clock output

1: pull low DDC clock output

D4 write Flat Panel DDC data output : FDDCDATN

0: pull high DDC data output

1: pull low DDC data output

D3 read Flat Panel DDC clock input: FDDCCLKI

0: Flat Panel DDC clock input low

1: Flat Panel DDC clock input high

D2 read Flat Panel DDC data input: FDDCDI

0: Flat Panel DDC data input low

1: Flat Panel DDC data input high

D1 PLINTRTP: Flat Panel interrupt read-back bit

0: No interrupt

1: Panel Link Interrupt

D0 PLATTCH: Flat Panel Plugging Status read back bit

0: No Flat Panel plugged

1: Flat Panel Plugge

Panel link display horizontal scaling factor

Register Type: Read/write

Read/write Port:3D5, index CC

D7 ENPLCLKDDA, enable panel link clock DDA operation

0: disable panel link clock DDA operation

1: enable panel link clock DDA operation

D6 HFSECTST, test for half-second counting

0: normal mode

1: test mode

D[5:0] PLHCFACT, panel link horizontal scaling factor

Panel link vertical scaling factor

Register Type: Read/write

Read/write Port:3D5, index CD

D[7:6] TRUEDLY[1:0], delay compensation of TRUEDCLK for CRT1 dot clock(DCLK) gating

D[5:0] PLVCFACT, panel link vertical scaling factor

Panel link vertical scaling factor

Register Type: Read/write

Read/write Port:3D5, index CE

D[7:4] Reserved

D[3:2] DLYCOMP[3:2], reserved

D[1:0] DLYCOMP[1:0], delay compensation for DCLK

9.13. LEGEND OF 3D REGISTERS

Table 9.13-1 Legend of 3D Registers

NOTATION	DEFINITION
(number)	The number of bits
(f)	Floating point representation
(i)	Integer representation
(s12)	Sign Magnitude Representation with 12 integer bits
A	Alpha component
A8	Alpha component, 8 bits integer representation
$Addr_{number}$	Address buss
Apix	Alpha component of a pixel
Atex	Alpha component of a texel
B	Blue color component
Cout	Output color
Cpix	Pixel color
Cr	Color stored in the color register CR
F	Fog factor
G	Green color component
Ltex	Luminance of a texel
M	Mix mode factor

R	Red color component
SB	Specular blue color component
SG	Specular green color component
SR	Specular red color component
TSARGBa	The register which stores the color component ARGB of vertex a
TSARGBb	The register which stores the color component ARGB of vertex b
TSARGBc	The register which stores the color component ARGB of vertex c
TSFSa	The register which stores the fog factor and specular color components of vertex a
TSFSb	The register which stores the fog factor and specular color components of vertex b
TSFSc	The register which stores the fog factor and specular color components of vertex c
TSUa	The register which stores the U coordinate of vertex a
TSUb	The register which stores the U coordinate of vertex b
TSUc	The register which stores the U coordinate of vertex c
TSVa	The register which stores the V coordinate of vertex a
TSVb	The register which stores the V coordinate of vertex b
TSVc	The register which stores the V coordinate of vertex c
TSWa	The register which stores the W perspective correction factor of vertex a
TSWb	The register which stores the W perspective correction factor of vertex b
TSWc	The register which stores the W perspective correction factor of vertex c
TSXa	The register which stores the X coordinate of vertex a
TSXb	The register which stores the X coordinate of vertex b
TSXc	The register which stores the X coordinate of vertex c
TSYa	The register which stores the Y coordinate of vertex a
TSYb	The register which stores the Y coordinate of vertex b
TSYc	The register which stores the Y coordinate of vertex c

TSZa	The register which stores the Z coordinate of vertex a
TSZb	The register which stores the Z coordinate of vertex b
TSZc	The register which stores the Z coordinate of vertex c
U	The X coordinate in a Texture
V	The Y coordinate in a Texture
W	Perspective correction factor
X	X coordinate
Y	Y coordinate
Z	Z coordinate
Z16	Z value, 16 bits representation

9.13.1. 3D REGISTERS SUMMARY

Table 9.13-1 Vertex Parameter Registers

	NAME	I/O ADDRESS	TRIANGLE DRAWING	LINE DRAWING	POINT DRAWING
1	TSFSa	8803h-8800h	√	√	√
2	TSZa	8807h-8804h	√	√	√
3	TSXa	880Bh-8808h	√	√	√
4	TSYa	880Fh-880Ch	√	√	√
5	TSARGBa	8813h-8810h	√	√	√
6	TSUa	8817h-8814h	√	√	√
7	TSVa	881Bh-8818h	√	√	√
8	TSWa	881Fh-881Ch	√	√	
9	TSFSb	8823h-8820h	√	√	
10	TSZb	8827h-8824h	√	√	
11	TSXb	882Bh-8828h	√	√	
12	TSYb	882Fh-882Ch	√	√	
13	TSARGBb	8833h-8830h	√	√	
14	TSUb	8837h-8834h	√	√	
15	TSVb	883Bh-8838h	√	√	
16	TSWb	883Fh-883Ch	√	√	
17	TSFSc	8843h-8840h	√		
18	TSZc	8847h-8844h	√		
19	TSXc	884Bh-8848h	√		

20	TSYc	884Fh-884Ch	√		
21	TSARGBc	8853h-8850h	√		
22	TSUc	8857h-8854h	√		
23	TSVc	885Bh-8858h	√		
24	TSWc	885Fh-885Ch	√		
25	Reserved	89F7h-8860h	√		

Table 9.13-2 Primitive Setting Register

89FBh ~	D[31:24]	Reserved	
89F8h	D[23:21]	Reserved	
	D[20:18]	TSHMD	Shading Mode
	D[17:16]	TTFROM	Point, Start, or Top Vertex Come From
	D[15:14]	TMFROM	Middle Vertex Come From
	D[13:12]	TBFROM	End or Bottom Vertex Come From
	D[11:8]	TSETFIRE	Set 3D Engine Fire Position
	D[7]	TDRAWDIR	Drawing Direction
	D[6:3]	Reserved	
	D[2:0]	TDRAW	Drawing Primitive Command

Table 9.13-3 Engine Fire & Status Register

89FFh ~	D[31:0]	TFIRE	Write for 3D Engine Fire
89FCh	D[31:0]	TSTATUS	Read for 3D Engine Status

Table 9.13-4 Enable Setting Register

8A03h ~	D[31:24]	Reserved	
8A00h	D[23:22]	Reserved	
	D[21]	TenZW	Z Write Enable
	D[20]	TenZT	Z Test Enable
	D[19]	Reserved	
	D[18]	TenAW	Alpha Write Enable
	D[17]	TenAT	Alpha Test Enable
	D[16]	TenABUF	Alpha Buffer Enable
	D[15]	TenMips	
	D[14]	Reserved	
	D[13]	Reserved	
	D[12]	TenLPT	Line Pattern Enable

	D[11]	Reserved	
	D[10]	TenTXMP	Texture Mapping Enable
	D[9]	TenTXPP	Texture Perspective Enable
	D[8]	TenTXTR	Texture Transparency Enable
	D[7]	TenCACHE	Enable Texture Cache
	D[6]	Reserved	
	D[5]	Reserved	
	D[4]	TenSPEC	Specular Enable
	D[3]	TenFOG	Fog Enable
	D[2]	TenBLEND	Blending Enable
	D[1]	TenTRSP	Transparency Enable
	D[0]	TenDITH	Dither Enable

Table 9.13-5 Z Setting Registers

8A07h ~	D[31:24]	Reserved	
8A04h	D[23:22]	Reserved	
	D[21:20]	TZBUFFM	Z-Buffer Data Format
	D[19]	Reserved	
	D[18:16]	TZTMD	Z-Test Mode
	D[15:14]	Reserved	
	D[13:0]	TZPIT	Z-Buffer Pitch
8A0Bh ~ 8A08h	D[31:0]	TZBAS	Z-Buffer Base Address

Table 9.13-6 Alpha Setting Registers

8A0Fh ~	D[31:30]	Reserved	
8A0Ch	D[29:28]	TABUFFM	Alpha Buffer Data Format
	D[27]	Reserved	
	D[26:24]	TATMD	Alpha Test Mode
	D[23:16]	TAREF	Alpha Reference Value
	D[15:12]	Reserved	
	D[11:0]	TAPIT	Alpha Buffer Pitch
8A13h ~ 8A10h	D[31:0]	TABAS	Alpha Buffer Base Address

Table 9.13-7 Destination Setting Registers

8A17h ~	D[31:28]	Reserved	
8A14h	D[27:24]	TROP	Raster Operation
	D[23]	Reserved	
	D[22:16]	TDSTCFM	Destination Color Format
	D[15:14]	Reserved	
	D[13:0]	TDSTPIT	Destination Color Surface Pitch
8A1Bh ~ 8A18h	D[31:0]	TDSTBAS	Destination Color Surface Base Address

Table 9.13-8 Line Setting Register

8A1Fh ~ 8A1Ch	D[31:0]	TLPT	Line Pattern and Repeat Factor

Table 9.13-9 Fog Setting Register

8A23h ~	D[31:25]	Reserved	
8A20h	D[24]	TFOGMD	Fog Mode
	D[23:0]	TFOGC	Fog Color Register

Table 9.13-10 Miscellaneous Setting Registers

8A27h ~	D[31:24]	Reserved	
8A24h	D[23:0]	TTRSL	Transparency Color Range Low Value
8A2Bh ~	D[31:28]	TBLDST	Destination Blending Mode
8A28h	D[27:24]	TBLSRC	Source Blending Mode
	D[23:0]	TTRSH	Transparency Color Range High Value
8A2Fh ~ 8A2C	D[31:0]	Reserved	
8A33h ~	D[31:26]	Reserved	
8A30h	D[25:0]	TCLTB	Clipping Value for Top & Bottom
8A37h ~	D[31:26]	Reserved	
8A34h	D[25:0]	TCLLR	Clipping Value for Left & Right

Table 9.13-11 Texture Setting Registers

8A3Bh ~	D[31:24]	TTXFM	Texel Format
8A38h	D[23:16]	TTXMPMD	Texture Mapping Mode

	D[15]	UVPOLAR	Set Sign or Un-sign Format of U,V
	D[14:12]	TTXBLMKB	Texture Blending Mask Bit Setting
	D[11:8]	TTXLV	Texture Level
	D[7:6]	Reserved	
	D[5]	TTXINSY	Texture Memory Located in System Memory
	D[4]	TTXCHCL	Clear Texture Cache
	D[3]	TTXFLMAX	Texture Magnified Filter Mode
	D[2:0]	TTXFLMIN	Texture Restrictional Filter Mode
8A3Fh ~	D[31:26]	TTXBLCMD	Texture Blending Color Mode Setting
8A3Ch	D[25:24]	TTXBLAMD	Texture Blending Alpha Mode Setting
	D[23:0]	TTXTRSL	Texture Transparency Color Range Low Value
8A43h ~	D[31:24]	Reserved	
8A40h	D[23:0]	TTXTRSH	Texture Transparency Color Range High Value
8A47h ~ 8A44h	D[31:0]	TTX0BAS	Texture Level 0 Base Address
8A4Bh ~ 8A48h	D[31:0]	TTX1BAS	Texture Level 1 Base Address
8A4Fh ~ 8A4Ch	D[31:0]	TTX2BAS	Texture Level 2 Base Address
8A53h ~ 8A50h	D[31:0]	TTX3BAS	Texture Level 3 Base Address
8A57h ~ 8A54h	D[31:0]	TTX4BAS	Texture Level 4 Base Address
8A5Bh ~ 8A58h	D[31:0]	TTX5BAS	Texture Level 5 Base Address
8A5Fh ~ 8A5Ch	D[31:0]	TTX6BAS	Texture Level 6 Base Address
8A63h ~ 8A60h	D[31:0]	TTX7BAS	Texture Level 7 Base Address
8A67h ~ 8A64h	D[31:0]	TTX8BAS	Texture Level 8 Base Address
8A6Bh ~ 8A68h	D[31:0]	TTX9BAS	Texture Level 9 Base Address
8A6Fh ~	D[31:27]	Reserved	

8A6Ch	D[26:16]	TTX0PCTL	Texture Level 0 Pitch
	D[15:11]	Reserved	
	D[10:0]	TTX1PCTL	Texture Level 1 Pitch
8A73h ~	D[31:27]	Reserved	
8A70h	D[26:16]	TTX2PCTL	Texture Level 2 Pitch
	D[15:11]	Reserved	
	D[10:0]	TTX3PCTL	Texture Level 3 Pitch
8A77h ~	D[31:27]	Reserved	
8A74h	D[26:16]	TTX4PCTL	Texture Level 4 Pitch
	D[15:11]	Reserved	
	D[10:0]	TTX5PCTL	Texture Level 5 Pitch
8A7Bh ~	D[31:27]	Reserved	
8A78h	D[26:16]	TTX6PCTL	Texture Level 6 Pitch
	D[15:11]	Reserved	
	D[10:0]	TTX7PCTL	Texture Level 7 Pitch
8A7Fh ~	D[31:27]	Reserved	
8A7Ch	D[26:16]	TTX8PCTL	Texture Level 8 Pitch
	D[15:11]	Reserved	
	D[10:0]	TTX9PCTL	Texture Level 9 Pitch
8A83h ~	D[31:28]	TTXW	Width of Texture Level 0
8A80h	D[27:24]	TTXH	Height of Texture Level 0
	D[23:19]	Reserved	
	D[18:10]	TTXMIPBS	Texture MIPMAP Bias
	D[9:0]	TTXLVINSY	Texture Level # in System Memory
8A87h ~	D[31:0]	Reserved	
8A84h			
8A8Bh ~	D[31:0]	Reserved	
8A88h			
8A8Fh ~	D[31:0]	Reserved	
8A8Ch	D[23:0]	TTXCR	Texture Color Register for Luminance
8A93h ~ 8A90h	D[31:0]	TTXCTB	Texture Border Color Register
8AD3h ~ 8A94h	D[31:0] x 16	TTXIDX15 ~ TTXIDX0	Texture Index Palette Register 0 ~ Texture Index Palette Register 15

Index Format

Index4: Use TTXIDX15 - TTXIDX0

Index2: Use TTXIDX3 - TTXIDX0

Index1: Use TTXIDX1 - TTXIDX0

Table 9.13-12 Reserved Registers

8AFEh ~ 8AD4h		Reserved	

Table 9.13-13 End of Primitive Setting Register

8AFFh	D[7:0]	TEND	End of Primitive List

9.13.2. VERTEX PARAMETER REGISTERS

Fog & Specular Color Components of Vertex a

Register Type: Read/Write

Read/Write Port: 8803h ~ 8800h

Default: xx xx xx xxh

D[31:24] TSFSa (i) ➡➡ fog factor of vertex a

D[23:16] TSSRa (i) ➡➡ specular red color of vertex a

D[15:8] TSSGa (i) ➡➡ specular green color of vertex a

D[7:0] TSSBa (i) ➡➡ specular blue color of vertex a

Z Coordinate of Vertex a

Register Type: Read/Write

Read/Write Port: 8807h ~ 8804h

Default: xx xx xx xxh

D[31:0] TSZa (f) ➡➡ Z of vertex a

X Coordinate of Vertex a

Register Type: Read/Write

Read/Write Port: 880Bh ~ 8808h

Default: xx xx xx xxh

D[31:0] TSXa (f) ➡➡ X of vertex a

Y Coordinate of Vertex a

Register Type: Read/Write

Read/Write Port: 880Fh ~ 880Ch

Default: xx xx xx xxh

D[31:0] TSYa (f) ➡➡ Y of vertex a

Color Component ARGB of Vertex a

Register Type: Read/Write

Read/Write Port: 8813h ~ 8810h

Default: xx xx xx xxh

D[31:24] TSAa (i) ➡➡ A of vertex a

D[23:16] TSRa (i) ➡➡ R of vertex a

D[15:8] TSGa (i) ➡➡ G of vertex a

D[7:0] TSBa (i) ➡➡ B of vertex a

X Coordinate in a Texture of Vertex a

Register Type: Read/Write

Read/Write Port: 8817h ~ 8814h

Default: xx xx xx xxh

D[31:0] TSUa (f) ➡➡ U of vertex a

Y Coordinate in a Texture of Vertex a

Register Type: Read/Write

Read/Write Port: 881Bh ~ 8818h

Default: xx xx xx xxh

D[31:0] TSVa (f) ➡➡ V of vertex a

Perspective Correction Factor in a Texture of Vertex a

Register Type: Read/Write

Read/Write Port: 881Fh ~ 881Ch

Default: xx xx xx xxh

D[31:0] TSWa (f) ➡➡ W of vertex a

Fog & Specular Color Components of Vertex b

Register Type: Read/Write

Read/Write Port: 8823h ~ 8820h

Default: xx xx xx xxh

D[31:24] TSFSb (i) ➡➡ fog factor of vertex b

D[23:16] TSSRb (i) ➡➡ specular red color of vertex b

D[15:8] TSSGb (i) ➡➡ specular green color of vertex b

D[7:0] TSSBb (i) ➡➡ specular blue color of vertex b

Z Coordinate of Vertex b

Register Type: Read/Write

Read/Write Port: 8827h ~ 8824h

Default: xx xx xx xxh

D[31:0] TSZb (f) ➡➡ Z of vertex b

X Coordinate of Vertex b

Register Type: Read/Write

Read/Write Port: 882Bh ~ 8828h

Default: xx xx xx xxh

D[31:0] TSXb (f) ➡➡ X of vertex b

Y Coordinate of Vertex b

Register Type: Read/Write

Read/Write Port: 882Fh ~ 882Ch

Default: xx xx xx xxh

D[31:0] TSYb (f) ➡➡ Y of vertex b

Color Component ARGB of Vertex b

Register Type: Read/Write

Read/Write Port: 8833h ~ 8830h

Default: xx xx xx xxh

D[31:24] TSAb (i) ➡➡ A of vertex b

D[23:16] TSRb (i) ➡➡ R of vertex b

D[15:8] TSGb (i) ➡➡ G of vertex b

D[7:0] TSBb (i) ➡➡ B of vertex b

X Coordinate in a Texture of Vertex b

Register Type: Read/Write

Read/Write Port: 8837h ~ 8834h

Default: xx xx xx xxh

D[31:0] TSUb (f) ➡➡ U of vertex b

Y Coordinate in a Texture of Vertex c

Register Type: Read/Write

Read/Write Port: 883Bh ~ 8838h

Default: xx xx xx xxh

D[31:0] TSVb (f) ➡➡ V of vertex b

Perspective Correction Factor in a Texture of Vertex b

Register Type: Read/Write

Read/Write Port: 883Fh ~ 883Ch

Default: xx xx xx xxh

D[31:0] TSWb (f) ➡➡ W of vertex b

Fog & Specular Color Components of Vertex c

Register Type: Read/Write

Read/Write Port: 8843h ~ 8840h

Default: xx xx xx xxh

D[31:24] TSFSc (i) ➡➡ fog factor of vertex c

D[23:16] TSSRc (i) ➡➡ specular red color of vertex c

D[15:8] TSSGc (i) ➡➡ specular green color of vertex c

D[7:0] TSSBc (i) ➡➡ specular blue color of vertex c

Z Coordinate of Vertex c

Register Type: Read/Write

Read/Write Port: 8847h ~ 8844h

Default: xx xx xx xxh

D[31:0] TSZc (f) ➡➡ Z of vertex c

X Coordinate of Vertex c

Register Type: Read/Write

Read/Write Port: 884Bh ~ 8848h

Default: xx xx xx xxh

D[31:0] TSXc (f) ➡➡ X of vertex c

Y Coordinate of Vertex c

Register Type: Read/Write

Read/Write Port: 884Fh ~ 884Ch

Default: xx xx xx xxh

D[31:0] TSYc (f) ➡➡ Y of vertex c

Color Component ARGB of Vertex c

Register Type: Read/Write

Read/Write Port: 8853h ~ 8850h

Default: xx xx xx xxh

D[31:24] TSAc (i) ➡➡ A of vertex c

D[23:16] TSRc (i) ➡➡ R of vertex c

D[15:8] TSGc (i) ➡➡ G of vertex c

D[7:0] TSBc (i) ➡➡ B of vertex c

X Coordinate in a Texture of Vertex c

Register Type: Read/Write

Read/Write Port: 8857h ~ 8854h

Default: xx xx xx xxh

D[31:0] TSUc (f) ➡➡ U of vertex c

Y Coordinate in a Texture of Vertex c

Register Type: Read/Write

Read/Write Port: 885Bh ~ 8858h

Default: xx xx xx xxh

D[31:0] TSVc (f) ➡➡ V of vertex c

Perspective Correction Factor in a Texture of Vertex c

Register Type: Read/Write

Read/Write Port: 885Fh ~ 885Ch

Default: xx xx xx xxh

D[31:0] TSWc (f) ➡➡ W of vertex c

Reserved Registers

Register Type: Read/Write

Read/Write Port: 89F7h ~ 8860h

Default: xx xx xx xxh

D[31:0] Reserved

9.13.3. PRIMITIVE SETTING REGISTERS

Register Type: Read/Write

Read/Write Port: 89FBh ~ 89F8h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:21] Reserved

D[20:18] TSHMD ➡➡ Shading Mode

For triangle shading,

000: Reserved

001: FLAT_SHADING via top vertex

010: FLAT_SHADING via middle vertex

011: FLAT_SHADING via bottom vertex

100: SMOOTH_SHADING via GOURAUD_SHADING

111 ~ 101: Reserved

For line shading,

000: Reserved

001: FLAT_SHADING via start vertex

010: Reserved

011: FLAT_SHADING via end vertex

100: SMOOTH_SHADING via GOURAUD_SHADING

111 ~ 101: Reserved

D[17:16] TTFROM ➡➡ top vertex come from

For triangle,

00: top vertex come from vertex a

01: top vertex come from vertex b

10: top vertex come from vertex c

11: reserved

For line,

00: start vertex come from vertex a

01: start vertex come from vertex b

10: start vertex come from vertex c

11: reserved

For point,

00: vertex come from vertex a

01: vertex come from vertex b

10: vertex come from vertex c

11: reserved

D[15:14]TMFROM ➡➡ middle vertex come from

For triangle,

00: middle vertex come from vertex a

01: middle vertex come from vertex b

10: middle vertex come from vertex c

11: reserved

D[13:12]TBFROM ➡➡ bottom vertex come from

For triangle,

00: bottom vertex come from vertex a

01: bottom vertex come from vertex b

10: bottom vertex come from vertex c

11: reserved

For line,

00: end vertex come from vertex a

01: end vertex come from vertex b

10: end vertex come from vertex c

11: reserved

D[11:8] TSETFIRE ➡➡ Set 3D Engine Fire Position

0000: 3D Engine fired right after the write of TFIRE

0001: 3D Engine fired right after the write of TSARGBa

0010: 3D Engine fired right after the write of TSWa

0011: 3D Engine fired right after the write of TSARGBb

0100: 3D Engine fired right after the write of TSWb

0101: 3D Engine fired right after the write of TSARGBc

0110: 3D Engine fired right after the writE of TSWc

0111: 3D Engine fired right after the write of TSVc

1000-1111: Reserved

D7 TDRAWDIR ➡➡ Drawing Direction

For triangle drawing,

0: left to right

1: right to left

For line drawing,

0: horizontal

1: vertical

D[6:3] Reserved

D[2:0] TDRAW ➡➡ Drawing Primitive Command

000: Draw a Point

001: Draw a Line

010: Draw a Triangle

9.13.4. 011-111: RESERVED

9.13.5. ENGINE FIRE & STATUS REGISTER

Register Type: Read/Write

Read/Write Port: 89FFh ~ 89FCh

Default: xx xx xx xxh

For write operation,

D[31:0] TFIRE ➡➡ Write to Fire 3D Engine

For read operation,

D[31:0] TSTATUS ➡➡ Read for 3D Engine Status as follow:

D[27:16] Available 3D Queue Length

3D Queue Length = D[27:16] * 8 Bytes

D[15:2] Reserved

D1 T3IDLEQE ➡➡ 3D Engine Idle & 3D Queue Empty

0: 3D Engine Busy or 3D Queue not Empty

1: 3D Engine Idle and 3D Queue Empty

D0 T3IDLE ➡➡ 3D Engine Idle

0: 3D Engine Busy

1: 3D Engine Idle

9.13.6. ENABLE SETTING REGISTER

Register Type: Read/Write

Read/Write Port: 8A03h ~ 8A00h

Default: all 00h

D[31:22] Reserved

D21 TenZW ➡➡ Z Write Enable

0: Z Write Disable

1: Z Write Enable

D20 TenZT ➡➡ Z Test Enable

0: Z Test Disable

1: Z Test Enable

D19 Reserved

D18 TenAW ➡➡ Alpha Write Enable

0: Alpha Write Disable

1: Alpha Write Enable

D17 TenAT ➡➡ Alpha Test Enable

0: Alpha Test Disable

1: Alpha Test Enable

D16 TenABUF ➡➡ Alpha Buffer Enable

0: Alpha Buffer Disable

1: Alpha Buffer Enable

D15 Reserved

D[14:13] TenSTIP, TenSTIPA ➡➡ Stipple Enable, Stipple Alpha Enable

0x: Stipple Disable

10: Stipple Enable, Stipple Alpha Disable

11: Stipple Enable, Stipple Alpha Enable

D12 TenLPT ➡➡ Line Pattern Enable

0: Line Pattern Disable

1: Line Pattern Enable

D11 TenPRSET ➡➡ Primitive Setup Enable

0: Primitive Setup Disable

1: Primitive Setup Enable

D10 TenTXMP ➡➡ Texture Mapping Enable

0: Texture Mapping Disable

1: Texture Mapping Enable

D9 TenTXPP ➡➡ Texture Perspective Correction Enable

0: Texture Perspective Correction Disable

1: Texture Perspective Correction Enable

D8 TenTXTR ➡➡ Texture Transparency Enable

0: Texture Transparency Disable

1: Texture Transparency Enable

D7 TenCACHE ➡➡ Enable Texture Cache

0: Texture Cache Disable

1: Texture Cache Enable

D6 Reserved

D5 TenLCH ➡➡ Enable Large Cache Size

0: Small Cache Size

1: Large Cache Size

D4 TenSPEC ➡➡ Specular Enable

0: Specular Disable

1: Specular Enable

D3 TenFOG ➡➡ Fog Enable

0: Fog Disable

1: Fog Enable

D2 TenBLEND ➡➡ Blending Enable

0: Blending Disable

1: Blending Enable

D1 TenTRSP ➡➡ Transparency Enable

0: Transparency Disable

1: Transparency Enable

D0 TenDITH ➡➡ Dither Enable

0: Dither Disable

1: Dither Enable

9.13.7. Z SETTING REGISTERS

Z Setting Register 1

Register Type: Read/Write

Read/Write Port: 8A07h ~ 8A04h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:22] Reserved

D[21:20] TZBUFFM ➡➡ Z Buffer Format

00: Z8

01: Z16

1x: Reserved

D19 Reserved

D[18:16] TZTMD ➡➡ Z Test Mode

000: Z test never pass

001: Pass if Znew < Zdst

010: Pass if Znew = Zdst

011: Pass if Znew ≤ Zdst

100: Pass if Znew > Zdst

101: Pass if Znew ≠ Zdst

110: Pass if Znew ≥ Zdst

111: Z test always pass

D[15:14] Reserved

D[13:0] TZPIT ➡➡ Z Buffer Pitch

Addr13 ~ Addr0

Z Setting Register 2

Register Type: Read/Write

Read/Write Port: 8A0Bh ~ 8A08h

Default: xx xx xx xxh

D[31:0] TZBAS ➡➡ Z Buffer Base Address

If Z Buffer is located in system memory,

D[31:0] Addr31 ~ Addr0

If Z Buffer is located in local frame buffer,

D[31:23] Reserved

D[22:0] Addr22 ~ Addr0

9.13.8. ALPHA SETTING REGISTERS

Alpha Setting Register 1

Register Type: Read/Write

Read/Write Port: 8A0Fh ~ 8A0Ch

Default: xx xx xx xxh

D[31:30] Reserved

D[29:28] TABUFFM ➡➡ Alpha Buffer Color Format

00 ~ 10: Reserved

11: A8 (alpha component, 8-bit integer representation)

D27 Reserved

D[26:24] TATMD ➡➡ Alpha Test Mode

000: Alpha test never pass

001: Pass if Anew < Aref

010: Pass if Anew = Aref

011: Pass if Anew ≤ Aref

100: Pass if Anew > Aref

101: Pass if Anew ≠ Aref

110: Pass if Anew ≥ Aref

111: Alpha test always pass

D[23:16] TAREF ➡➡ Alpha Reference Value

A8 format (alpha component, 8-bit integer representation)

D[15:12] Reserved

D[11:0] TAPIT ➡➡ Alpha Buffer Pitch

Addr11 ~ Addr0

Alpha Setting Register 2

Register Type: Read/Write

Read/Write Port: 8A13h ~ 8A10h

Default: xx xx xx xxh

D[31:0] TABAS ➡➡ Alpha Buffer Base Address

If Alpha Buffer is located in system memory,

D[31:0] Addr31 ~ Addr0

If Alpha Buffer is located in local frame buffer,

D[31:23] Reserved

D[22:0] Addr22 ~ Addr0

9.13.9. DESTINATION SETTING REGISTERS

Destination Setting Register 1

Register Type: Read/Write

Read/Write Port: 8A17h ~ 8A14h

Default: xx xx xx xxh

D[31:28] Reserved

D[27:24] TROP ➡➡ Raster Operation

Table 9.13-1 Raster Operation

0000: BLACK	0
0001: NOT_MERGE_PEN	DPon
0010: MASK_NOT_PEN	DPna
0011: NOT_COPY_PEN	Pn
0100: MASK_PEN_NOT	PDna
0101: NOT	Dn
0110: XOR_PEN	DPx
0111: NOT_MASK_PEN	DPan
1000: MASK_PEN	DPa
1001: NOT_XOR_PEN	DPxn
1010: NOP	D
1011: MERGE_NOT_PEN	DPno
1100: COPY_PEN	P
1101: MERGE_PEN_NOT	PDno
1110: MERGE_PEN	DPo
1111: WHITE	1

D23 Reserved

D[22:16] TDSTCFM ➡➡ Destination Color Format

D22 0: RGB ordering in RGB format

1: BGR ordering in RGB format

D[21:20] 00: Index format or RGB_8bpp format

01: RGB_16bpp format

10: RGB_24bpp format

11: RGB_32bpp format

For D[22] = 0,

D[19:16] For D[21:20] = 01 (RGB_16bpp format),

Table 9.13-2 RGB_16bpp Format

0000: RGB555,	xRRR RRGG GGGB BBBB
0001: RGB565,	RRRR RGGG GGGB BBBB
0010: ARGB1555,	ARRR RRGG GGGB BBBB
0011: ARGB4444,	AAAA RRRR GGGG BBBB

For D[21:20] = 11 (RGB_32bpp format),

Table 9.13-3 RGB_32bpp Format

0000: ARGB1888	Axxx xxxx RRRR RRRR GGGG GGGG BBBB BBBB
0001: ARGB2888	AAxx xxxx RRRR RRRR GGGG GGGG BBBB BBBB
0010: ARGB4888	AAAA xxxx RRRR RRRR GGGG GGGG BBBB BBBB
0011: ARGB8888	AAAA AAAA RRRR RRRR GGGG GGGG BBBB BBBB
0100: RGB0888	xxxx xxxx RRRR RRRR GGGG GGGG BBBB BBBB
Others: Reserved	

For D[22] = 1,

D[19:16] For D[21:20] = 01 (RGB_16bpp format)

GB_16bpp format)

Table 9.13-4 RGB_16bpp Format

0000: BGR555	xBBB BBGG GGGR RRRR

0001: BGR565	BBBB BGGG GGGR RRRR
0010: ABGR1555	ABBB BBGG GGGR RRRR
0011: ABGR4444	AAAA BBBB GGGG RRRR

For D[21:20] = 11 (RGB_32bpp format),

Table 9.13-5 RGB_32bpp Format

0000: ABGR1888	Axxx xxxx BBBB BBBB GGGG GGGG RRRR RRRR
0001: ABGR2888	AAxx xxxx BBBB BBBB GGGG GGGG RRRR RRRR
0010: ABGR4888	AAAA xxxx BBBB BBBB GGGG GGGG RRRR RRRR
0011: ABGR8888	AAAA AAAA BBBB BBBB GGGG GGGG RRRR RRRR
0100: BGR0888	xxxx xxxx BBBB BBBB GGGG GGGG RRRR RRRR
Others: Reserved	

D[15:14] Reserved

D[13:0] TDSTPIT ➡➡ Destination Pitch

Addr13 ~ Addr0

Destination Setting Register 2

Register Type: Read/Write

Read/Write Port: 8A1Bh ~ 8A18h

Default: xx xx xx xxh

D[31:0] TDSTBAS ➡➡ Destination Base Address

If Destination Surface is located in system memory,

D[31:0] Addr31 ~ Addr0

If Destination Surface is located in local frame buffer,

D[31:23] Reserved

D[22:0] Addr22 ~ Addr0

9.13.10.Line Setting Register

Register Type: Read/Write

Read/Write Port: 8A1Fh ~ 8A1Ch

Default: xx xx xx xxh

D[31:16] TLPT ➡➡ Line pattern

D[15:0] TLPTNRP (i) ➡➡ Repeat factor of Line Pattern

9.13.11.Fog Setting Register

Register Type: Read/Write

Read/Write Port: 8A23h ~ 8A20h

Default: xx xx xx xxh

D[31:25] Reserved

D24 TFOGMD ➡➡ Fog Mode

0: Constant Fog Mode

1: Normal Fog Mode

D[23:0] TFOGC ➡➡ Color Register of Fog

D[23:16] = TGFR (i) ➡➡ Fog Color R

D[15:8] = TGFG (i) ➡➡ Fog Color G

D[7:0] = TGFB (i) ➡➡ Fog Color B

9.13.12.MISCELLANEOUS SETTING REGISTERS

Miscellaneous Setting Register 1

Register Type: Read/Write

Read/Write Port: 8A27h ~ 8A24h

Default: xx xx xx xxh

D[31:27] Reserved

D[23:16] TTRSLR (i) ➡➡ R of Transparency Color Low Range

D[15:8] TTRSLG (i) ➡➡ G of Transparency Color Low Range

D[7:0] TTRSLB (i) ➡➡ B of Transparency Color Low Range

Miscellaneous Setting Register 2

Register Type: Read/Write

Read/Write Port: 8A2Bh ~ 8A28h

Default: xx xx xx xxh

D[31:28] TBLDST ➡➡ Destination Blending Mode

0000: BLEND_ZERO

Blend factor is (0, 0, 0, 0) for (A,R,G,B)

0001: BLEND_ONE

Blend factor is (1, 1, 1, 1) for (A,R,G,B)

0010: BLEND_SRC_COLOR

Blend factor is [R(s),G(s),B(s),A(s)]

0011: BLEND_INV_SRC_COLOR

Blend factor is [1-R(s),1-G(s),1-B(s),1-A(s)]

0100: BLEND_SRC_ALPHA

Blend factor is [A(s),A(s),A(s),A(s)]

0101: BLEND_INV_SRC_ALPHA

Blend factor is [1-A(s),1-A(s),1-A(s), 1-A(s)]

0110: BLEND_DST_ALPHA

Blend factor is [A(d),A(d),A(d),A(d)]

0111: BLEND_INV_DST_ALPHA

Blend factor is [1-A(d),1-A(d),1-A(d)]

1111 ~ 1000: Reserved

D[27:24] TBLSRC ➡➡ Source Blending Mode

0000: BLEND_ZERO

Blend factor is (0, 0, 0, 0)

0001: BLEND_ONE

Blend factor is (1, 1, 1, 1)

0010-0011: Reserved

0100: BLEND_SRC_ALPHA

Blend factor is [A(s), A(s), A(s), A(s)]

0101: BLEND_INV_SRC_ALPHA

Blend factor is [1-A(s), 1-A(s), 1-A(s), 1-A(s)]

0110: BLEND_DST_ALPHA

Blend factor is [A(d), A(d), A(d), A(d)]

0111: BLEND_INV_DST_ALPHA

Blend factor is [1-A(d), 1-A(d), 1-A(d)]

1000: BLEND_DST_COLOR

Blend factor is [R(d), G(d), B(d), A(d)]

1001: BLEND_INV_DST_COLOR

Blend factor is [1-R(d), 1-G(d), 1-B(d), 1-A(d)]

1010: BLEND_SRC_ALPHA_SAT

Blend factor is (f, f, f, 1); f = min[A(s), 1-A(d)]

1011: BLEND_BOTH_SRC_ALPHA

Source blend factor is [A(s), A(s), A(s), A(s)]

Destination blend factor is [1-A(s), 1-A(s), 1-A(s), 1-A(s)]

1100: BLEND_BOTH_INV_SRC_ALPHA

Source blend factor is [1-A(s), 1-A(s), 1-A(s), 1-A(s)]

Destination blend factor is [A(s), A(s), A(s), A(s)]

1111-1101: Reserved

D[23:16] TTRSHR (i) ➡➡ R of Transparency Color High Range

D[15:8] TTRSHG (i) ➡➡ G of Transparency Color High Range

D[7:0] TTRSHB (i) ➡➡ B of Transparency Color High Range

Miscellaneous Setting Register 3

Register Type: Read/Write

Read/Write Port: 8A2Fh ~ 8A2Ch

Default: xx xx xx xxh

D[31:0] Reserved

Miscellaneous Setting Register 4

Register Type: Read/Write

Read/Write Port: 8A33h ~ 8A30h

Default: xx xx xx xxh

D[31:26] Reserved

D[25:13] TCLTOP (s12) ➡➡ Top Clipping Value

D[12:0] TCLBOT (s12) ➡➡ Bottom Clipping Value

Miscellaneous Setting Register 5

Register Type: Read/Write

Read/Write Port: 8A37h ~ 8A34h

Default: xx xx xx xxh

D[31:26] Reserved

D[25:13] TCLLEFT (s12) ➡➡ Left Clipping Value

D[12:0] TCLRGT (s12) ➡➡ Right Clipping Value

9.13.13.TEXTURE SETTING REGISTERS

Texture Setting Register 1

Register Type: Read/Write

Read/Write Port: 8A3Bh ~ 8A38h

Default: xxh, xxh, x0000000b, 00h

D[31:24] TTXFM ➡➡ Texel Format

D31 RGB ordering

0: RGB ordering in RGB format

1: BGR ordering in RGB format

D[30:28] Format

000: Palette Index format

001: Mix format

010: YUV format

011: Luminance format

100: RGB_8bpp or BGR_8bpp format

101: RGB_16bpp or BGR_8bpp format

110: RGB_24bpp or BGR_24bpp format

111: RGB_32bpp or BGR_32bpp format

(Color ordering is shown from MSB to LSB)

For D[31:28] = 0000 (RGB ordering & palette index format),

D[27:24] 0000: Index1

Use TTXIDX0, 1

0001: Index2

Use TTXIDX0, 1, 2, 3

0010: Index4

Use TTXIDX0-15

For D[31:28] = 0001 (RGB ordering & mix format),

D[27:24] 0000: M4

MMMM

0110: AM44

AAAA MMMM

For D[31:28] = 0010 (RGB ordering & YUV format),

D[27:24]

0000: YUV422

$Y_1Y_1Y_1Y_1\ Y_1Y_1Y_1Y_1$ CuCuCuCu CuCuCuCu $Y_0Y_0Y_0Y_0\ Y_0Y_0Y_0Y_0$

CvCvCvCv CvCvCvCv

0001: YVU422

$Y_1Y_1Y_1Y_1\ Y_1Y_1Y_1Y_1$ CvCvCvCv CvCvCvCv $Y_0Y_0Y_0Y_0\ Y_0Y_0Y_0Y_0$

CuCuCuCu CuCuCuCu

0010: UVY422

CuCuCuCu CuCuCuCu $Y_1Y_1Y_1Y_1\ Y_1Y_1Y_1Y_1$

CvCvCvCvCvCvCvCv $Y_0Y_0Y_0Y_0Y_0\ Y_0Y_0Y_0$

0011: VUY422

CvCvCvCv CvCvCvCv $Y_1Y_1Y_1Y_1$ $Y_1Y_1Y_1Y_1$

CuCuCuCuCuCuCuCu $Y_0Y_0Y_0Y_0Y_0Y_0Y_0Y_0$

For D[31:28] = 0011 (RGB ordering & luminance format),

D[27:24]

0000: L1

L

0001: L2

LL

0010: L4

LLLL

0011: L8

LLLL LLLL

0101: AL22

AALL

1000: AL44

AAAA LLLL

1100: AL88

AA AAAA LLLL LLLL

For D[31:28] = 0100 (ARGB 8bpp format),

D[27:24] 0000: RGB332

RRRG GGBB

0001: RGB233

RRGG GBBB

0010: RGB232

xRRG GGBB

0011: ARGB1232

ARRG GGBB

For D[31:28] = 0101 (ARGB 16bpp format),

D[27:24] 0000: RGB555

xRRR RRGG GGGB BBBB

0001: RGB565

RRRR RGGG GGGB BBBB

0010: ARGB1555

ARRR RRGG GGGB BBBB

0011: ARGB4444

AAAA RRRR GGGG BBBB

0111: ARGB8332

AAAA AAAA RRRG GGBB

1011: ARGB8233

AAAA AAAA RRGG GBBB

1111: ARGB8232

AAAA AAAA xRRG GGBB

For D[31:28] = 0110 (ARGB 24bpp format),

D[27:24] 0011: ARGB8565

AAAA AAAA RRRR RGGG GGGB BBBB

0111: ARGB8555

AAAA AAAA xRRR RRGG GGGB BBBB

1000: RGB888

RRRR RRRR GGGG GGGG BBBB BBBB

For D[31:28] = 0111 (ARGB 32bpp format),

D[27:24] 0011: ARGB8888

AAAA AAAA RRRR RRRR GGGG GGGG BBBB BBBB

0100: ARGB0888

xxxx xxxx RRRR RRRR GGGG GGGG BBBB BBBB

For D[31:28] = 1100 (ABGR 8bpp format),

D[27:24] 0000: BGR332

BBBG GGRR

0001: BGR233

BBGG GRRR

0010: BGR232

xBBG GGRR

0011: ABGR1232

ABBG GGRR

For D[31:28] = 1101 (ABGR 16bpp format),

D[27:24] 0000: BGR555

xBBB BBGG GGGR RRRR

0001: BGR565

BBBB BGGG GGGR RRRR

0010: ABGR1555

ABBB BBGG GGGR RRRR

0011: ABGR4444

AAAA BBBB GGGG RRRR

0111: ABGR8332

AAAA AAAA BBBG GGRR

1011: ABGR8233

AAAA AAAA BBGG GRRR

1111: ABGR8232

AAAA AAAA xBBG GGRR

For D[31:28] = 1110 (ABGR 24bpp format),

D[27:24] 0011: ABGR8565

AAAA AAAA BBBB BGGG GGGR RRRR

0111: ABGR8555

AAAA AAAA xRRR RRGG GGGB RRRR

1000: BGR888

BBBB BBBB GGGG GGGG RRRR RRRR

For D[31:28] = 1111 (ABGR 32bpp format),

D[27:24] 0011: ABGR8888

AAAA AAAA BBBB BBBB GGGG GGGG RRRR RRRR

0100: ABGR0888

xxxx xxxx BBBB BBBB GGGG GGGG RRRR RRRR

Others: Reserved

D[23:16] TTXMPMD ➡➡ Texture Mapping Mode

(Priority: wrap > mirror > clamp)

xx xxxx00: Wrap Disable

xx xx00xx: Mirror Disable

xx 00xxxx: Clamp Disable

xx xxxxx1: Wrap along U axis

xx xxxx1x: Wrap along V axis

xx xxx1x0: Mirror along U axis

xx xx1x0x: Mirror along V axis

xx x1x0x0: Clamp along U axis

xx 1x0x0x: Clamp along V axis

x0 xxxxxx: Do not use Border Color (CTB) for smoothing

x1 xxxxxx: Use CTB for smoothing

0x xxxxxx: Do not use CTB if out of texture area

1x xxxxxx: Use CTB if out of texture area

D15 UVPOLAR ➡➡ Set Sign or Un-sign Format of Cu, Cv

0: Cu and Cv are un-sign representation

1: Cu and Cv are Sign magnitude representation

D[14:2] TTXBLMKB ➡➡ Texture Blending Mask Bit Setting

000: Bit n = Bit 0 of Atex

001: Bit n = Bit 1 of Atex

010: Bit n = Bit 2 of Atex

011: Bit n = Bit 3 of Atex

100: Bit n = Bit 4 of Atex

101: Bit n = Bit 5 of Atex

110: Bit n = Bit 6 of Atex

111: Bit n = Bit 7 of Atex

D[11:8] TTXLV ➡➡ Texture Level

0000: Single Texture Structure

1001 ~ 0001: MIP structure

This number must small than or equal to

max {TTXW, TTXH}.

1111 ~ 1010: Reserved

D[7:6] Reserved

D5 TTXINSY ➡➡ Texture Memory Located in System Memory

0: Texture Memory is located in local frame buffer

1: Texture Memory is located in system memory

D4 TTXCHCL ➡➡ Clear Texture Cache

0: Let Texture Cache Work Normally

1: Clear Data in Texture Cache

D3 TTXFLMAX ➡➡ Texture filter mode when a texture is magnified

0: Nearest

1: Linear

D[2:0] TTXFLMIN ➡➡ Texture filter mode when a texture is restricted

000: NEAREST

001: LINEAR

010: NEAREST_MIP_NEAREST

011: NEAREST_MIP_LINEAR

100: LINEAR_MIP_NEAREST

101: LINEAR_MIP_LINEAR

11x: Reserved

Texture Setting Register 2

Register Type: Read/Write

Read/Write Port: 8A3Fh ~ 8A3Ch

Default: xx xx xx xxh

D[31:26] TTXBLCMD ➡➡ Texture Blending Color Mode Setting

For ARGB format,

00 0000: Cout = Ctex

00 0001: Cout = Cpix

00 0010: Cout = Cpix Ctex

00 0011: Cout = Cpix Ctex

00 0100: Cout = (1 - Atex) Cpix + Atex Ctex

00 0101: Reserved

00 0110: Cout = (1 - Apix) Ctex + Apix Cpix

00 0111: Cout = (1 - Apix) Ctex + Apix Cpix

00 1000: Cout = Ctex, if Bit n of Atex = 1,

Cout = Cpix, if Bit n of Atex = 0

00 1001: Cout = Ctex , if Bit n of Atex = 1,

Cout = Cpix, if Bit n of Atex = 0

00 101x: Reserved

00 1100: Cout = Cpix Ctex, if Bit n of Atex = 1,

Cout = Cpix , if Bit n of Atex = 0

00 1101: Cout = Cpix Ctex, if Bit n of Atex = 1,

Cout = Cpix, if Bit n of Atex = 0

00 1110: Cout = Cpix Ctex, if Bit n of Atex = 1,

Cout = Cpix, if Bit n of Atex = 0

0 1111: Reserved

01 xxxx: Reserved

1x xxxx: Reserved

For RGB format,

00 0000: Cout = Ctex

00 0001: Cout = Cpix

00 0010: Cout = Cpix Ctex

00 0011: Cout = Cpix Ctex

00 0100: Cout = Ctex

00 0101: Reserved

00 0110: Cout = Cpix

00 0111: Cout = Cpix

00 1000: Cout = Ctex

00 1001: Cout = Cpix

00 101x: Reserved

00 1100: Cout = Cpix Ctex

00 1101: Cout = Cpix

00 1110: Cout = Cpix Ctex

00 1111: Reserved

01 xxxx: Reserved

1x xxxx: Reserved

For AL format,

00 0000: Cout = Ltex Cr

00 0001: Cout = Cpix

00 0010: Cout = Ltex Cpix

00 0011: Cout = Ltex Cr Cpix

00 0100: Cout = (1 - Ltex) Cpix + Ltex Cr

00 0101: Reserved

00 0110: Cout = (1- Apix) Cr + Apix Cpix

00 0111: Cout = (1- Apix) Ltex Cr + Apix Cpix

00 1000: Cout = Ltex Cr, if Bit n of Atex = 1

Cout = Cpix, if Bit n of Atex = 0

00 1001: Cout = Ltex Cr, if Bit n of Atex = 1

Cout = Cpix, if Bit n of Atex = 0

00 101x: Reserved

00 1100: Cout = Ltex Cpix, if Bit n of Atex = 1

Cout = Cpix, if Bit n of Atex = 0

00 1101: Cout = Ltex Cpix, if Bit n of Atex = 1

Cout = Cpix, if Bit n of Atex = 0

00 1110: Cout = Ltex Cr Cpix, if Bit n of Atex = 1

Cout = Cpix, if Bit n of Atex = 0

00 1111: Reserved

01 xxxx: Reserved

1x xxxx: Reserved

For L format,

00 0000: Cout = Ltex Cr

00 0001: Cout = Cpix

00 0010: Cout = Ltex Cpix

00 0011: Cout = Ltex Cr Cpix

00 0100: Cout = Ltex Cr

00 0101: Reserved

00 0110: Cout = Cpix

00 0111: Cout = Cpix

00 1000: Cout = Ltex Cr

00 1001: Cout = Cpix

00 101x: Reserved

00 1100: Cout = Ltex Cpix

00 1101: Cout = Cpix

00 1110: Cout = Ltex Cr Cpix

00 1111: Reserved

01 xxxx: Reserved

1x xxxx: Reserved

D[25:24] TTXBLAMD ➡➡ Texture Blending Alpha Mode Setting

00: Aout = Atex, for ARGB, AL texture format

Aout = Apix, for RGB, L texture format

01: Aout = Apix

10: Aout = Apix Atex, for ARGB, AL texture format

Aout = Apix, for RGB, L texture format

11: Reserved

D[23:16] TTXTRSLR (i) ➡➡ R of Texture Transparency Color Low Range

D[15:8] TTXTRSLG (i) ➡➡ G of Texture Transparency Color Low Range

D[7:0] TTXTRSLB (i) ➡➡ B of Texture Transparency Color Low Range

Texture Setting Register 3

Register Type: Read/Write

Read/Write Port: 8A43h ~ 8A40h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXTRSHR (i) ➡➡ R of Texture Transparency Color High Range

D[15:8] TTXTRSHG (i) ➡➡ G of Texture Transparency Color High Range

D[7:0] TTXTRSHB (i) ➡➡ B of Texture Transparency Color High Range

Texture Level 0 Base Address

Register Type: Read/Write

Read/Write Port: 8A47h ~ 8A44h

Default: xx xx xx xxh

D[31:0] TTX0BAS ➡➡ Texture Level 0 Base Address

If Texture Memory is located in system memory,

D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,

D[31:23] Reserved

D[22:0] Addr22 ~ Addr0

Texture Level 1 Base Address

Register Type: Read/Write

Read/Write Port: 8A4Bh ~ 8A48h

Default: xx xx xx xxh

D[31:0] TTX1BAS ➡➡ Texture Level 1 Base Address

If Texture Memory is located in system memory,

D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,

D[31:23] Reserved

D[22:0] Addr22 ~ Addr0

Texture Level 2 Base Address

Register Type: Read/Write

Read/Write Port: 8A4Fh ~ 8A4Ch

Default: xx xx xx xxh

D[31:0] TTX2BAS ➡➡ Texture Level 2 Base Address

If Texture Memory is located in system memory,

D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,

D[31:23] Reserved

D[22:0] Addr22 ~ Addr0

Texture Level 3 Base Address

Register Type: Read/Write

Read/Write Port: 8A53h ~ 8A50h

Default: xx xx xx xxh

D[31:0] TTX3BAS ➡➡ Texture Level 3 Base Address

If Texture Memory is located in system memory,

D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,

D[31:23] Reserved

D[22:0] Addr22 ~ Addr0

Texture Level 4 Base Address

Register Type: Read/Write

Read/Write Port: 8A57h ~ 8A54h

Default: xx xx xx xxh

D[31:0] TTX4BAS ➡➡ Texture Level 4 Base Address

If Texture Memory is located in system memory,

D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,

D[31:23] Reserved

D[22:0] Addr22 ~ Addr0

Texture Level 5 Base Address

Register Type: Read/Write

Read/Write Port: 8A5Bh ~ 8A58h

Default: xx xx xx xxh

D[31:0] TTX5BAS ➡➡ Texture Level 5 Base Address

If Texture Memory is located in system memory,

D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,

D[31:23] Reserved

D[22:0] Addr22 ~ Addr0

Texture Level 6 Base Address

Register Type: Read/Write

Read/Write Port: 8A5Fh ~ 8A5Ch

Default: xx xx xx xxh

D[31:0] TTX6BAS ➡➡ Texture Level 6 Base Address

If Texture Memory is located in system memory,

D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,

D[31:23] Reserved

D[22:0] Addr22 ~ Addr0

Texture Level 7 Base Address

Register Type: Read/Write

Read/Write Port: 8A63h ~ 8A60h

Default: xx xx xx xxh

D[31:0] TTX7BAS ➡➡ Texture Level 7 Base Address

If Texture Memory is located in system memory,

D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,

D[31:23] Reserved

D[22:0] Addr22 ~ Addr0

Texture Level 8 Base Address

Register Type: Read/Write

Read/Write Port: 8A67h ~ 8A64h

Default: xx xx xx xxh

D[31:0] TTX8BAS ➡➡ Texture Level 8 Base Address

If Texture Memory is located in system memory,

D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,

D[31:23] Reserved

D[22:0] Addr22 ~ Addr0

Texture Level 9 Base Address

Register Type: Read/Write

Read/Write Port: 8A6Bh ~ 8A68h

Default: xx xx xx xxh

D[31:0] TTX9BAS ➡➡ Texture Level 9 Base Address

If Texture Memory is located in system memory,

D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,

D[31:23] Reserved

D[22:0] Addr22 ~ Addr0

Texture Level 0 & 1 Pitch Control

Register Type: Read/Write

Read/Write Port: 8A6Fh ~ 8A6Ch

Default: xx xx xx xxh

D[31:27] Reserved

D[26:16] TTX0PCTL ➡➡ Texture Level 0 Pitch Control

Addr10 ~ Addr0

D[15:11] Reserved

D[10:0] TTX1PCTL ➡➡ Texture Level 1 Pitch Control

Addr10 ~ Addr0

Texture Level 2 & 3 Pitch Control

Register Type: Read/Write

Read/Write Port: 8A73h ~ 8A70h

Default: xx xx xx xxh

D[31:27] Reserved

D[26:16] TTX2PCTL ➡➡ Texture Level 2 Pitch Control

Addr10 ~ Addr0

D[15:11] Reserved

D[10:0] TTX3PCTL ➡➡ Texture Level 3 Pitch Control

Addr10 ~ Addr0

Texture Level 4 & 5 Pitch Control

Register Type: Read/Write

Read/Write Port: 8A77h ~ 8A74h

Default: xx xx xx xxh

D[31:27] Reserved

D[26:16] TTX4PCTL ➡➡ Texture Level 4 Pitch Control

Addr10 ~ Addr0

D[15:11] Reserved

D[10:0] TTX5PCTL ➡➡ Texture Level 5 Pitch Control

Addr10 ~ Addr0

Texture Level 2 & 3 Pitch Control

Register Type: Read/Write

Read/Write Port: 8A7Bh ~ 8A78h

Default: xx xx xx xxh

D[31:27] Reserved

D[26:16] TTX6PCTL ➡➡ Texture Level 6 Pitch Control

Addr10 ~ Addr0

D[15:11] Reserved

D[10:0] TTX7PCTL ➡➡ Texture Level 7 Pitch Control

Addr10 ~ Addr0

Texture Level 8 & 9 Pitch Control

Register Type: Read/Write

Read/Write Port: 8A7Fh ~ 8A7Ch

Default: xx xx xx xxh

D[31:27] Reserved

D[26:16] TTX8PCTL ➡➡ Texture Level 8 Pitch Control

Addr10 ~ Addr0

D[15:11] Reserved

D[10:0] TTX9PCTL ➡➡ Texture Level 9 Pitch Control

Addr10 ~ Addr0

Texture Setting Register 4

Register Type: Read/Write

Read/Write Port: 8A83h ~ 8A80h

Default: xx xx xx xxh

D[31:28] TTXW ➡➡ Texture Width

0000: Texture Width = 2^0 = 1

0001: Texture Width = 2^1 = 2

0010: Texture Width = 2^2 = 4

0011: Texture Width = 2^3 = 8

0100: Texture Width = 2^4 = 16

0101: Texture Width = 2^5 = 32

0110: Texture Width = 2^6 = 64

0111: Texture Width = 2^7 = 128

1000: Texture Width = 2^8 = 256

1001: Texture Width = 2^9 = 512

1010 ~ 1111: Reserved

D[27:24] TTXH ➡➡ Texture Height

0000: Texture Height = 2^0 = 1

0001: Texture Height = 2^1 = 2

0010: Texture Height = 2^2 = 4

0011: Texture Height = 2^3 = 8

0100: Texture Height = 2^4 = 16

0101: Texture Height = 2^5 = 32

0110: Texture Height = 2^6 = 64

0111: Texture Height = 2^7 = 128

1000: Texture Height = 2^8 = 256

1001: Texture Height = 2^9 = 512

1010-1111: Reserved

D[23:16] TXCBR (i) ➡➡ R of Texture Color Base Register for Mix Mode

D[15:8] TXCBG (i) ➡➡ G of Texture Color Base Register for Mix Mode

D[7:0] TXCBB (i) ➡➡ B of Texture Color Base Register for Mix Mode

Texture Color Register 0 for Mix Mode

Register Type: Read/Write

Read/Write Port: 8A87h ~ 8A84h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXC0R (i) ➡➡ R of Texture Color Register 0

D[15:8] TTXC0G (i) ➡➡ G of Texture Color Register 0

D[7:0] TTXC0B (i) ➡➡ B of Texture Color Register 0

Texture Color Register 1 for Mix Mode

Register Type: Read/Write

Read/Write Port: 8A8Bh ~ 8A88h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXC1R (i) ➡➡ R of Texture Color Register 1

D[15:8] TTXC1G (i) ➡➡ G of Texture Color Register 1

D[7:0] TTXC1B (i) ➡➡ B of Texture Color Register 1

Texture Color Register for Luminance

Register Type: Read/Write

Read/Write Port: 8A8Fh ~ 8A8Ch

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXCRR (i) ➡➡ R of Luminance

D[15:8] TTXCRG (i) ➡➡ G of Luminance

D[7:0] TTXCRB (i) ➡➡ B of Luminance

Texture Border Color Register

Register Type: Read/Write

Read/Write Port: 8A93h ~ 8A90h

Default: xx xx xx xxh

D[31:24] TXCTBA (i) ➡➡ A of Texture Border

D[23:16] TXCTBR (i) ➡➡ R of Texture Border

D[15:8] TXCTBG (i) ➡➡ G of Texture Border

D[7:0] TXCTBB (i) ➡➡ B of Texture Border

Texture Index Palette Register 0

Register Type: Read/Write

Read/Write Port: 8A97h ~ 8A94h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX0B (i) ➡➡ B of Index 0

D[15:8] TTXIDX0G (i) ➡➡ G of Index 0

D[7:0] TTXIDX0R (i) ➡➡ R of Index 0

Texture Index Palette Register 1

Register Type: Read/Write

Read/Write Port: 8A9Bh ~ 8A98h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX1B (i) ➡➡ B of Index 1

D[15:8] TTXIDX1G (i) ➡➡ G of Index 1

D[7:0] TTXIDX1R (i) ➡➡ R of Index 1

Texture Index Palette Register 2

Register Type: Read/Write

Read/Write Port: 8A9Fh ~ 8A9Ch

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX2B (i) ➡➡ B of Index 2

D[15:8] TTXIDX2G (i) ➡➡ G of Index 2

D[7:0] TTXIDX2R (i) ➡➡ R of Index 2

Texture Index Palette Register 3

Register Type: Read/Write

Read/Write Port: 8AA3h ~ 8AA0h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX3B (i) ➡➡ B of Index 3

D[15:8] TTXIDX3G (i) ➡➡ G of Index 3

D[7:0] TTXIDX3R (i) ➡➡ R of Index 3

Texture Index Palette Register 4

Register Type: Read/Write

Read/Write Port: 8AA7h ~ 8AA4h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX4B (i) ➡➡ B of Index 4

D[15:8] TTXIDX4G (i) ➡➡ G of Index 4

D[7:0] TTXIDX4R (i) ➡➡ R of Index 4

Texture Index Palette Register 5

Register Type: Read/Write

Read/Write Port: 8AABh ~ 8AA8h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX5B (i) ➡➡ B of Index 5

D[15:8] TTXIDX5G (i) ➡➡ G of Index 5

D[7:0] TTXIDX5R (i) ➡➡ R of Index 5

Texture Index Palette Register 6

Register Type: Read/Write

Read/Write Port: 8AAFh ~ 8AACh

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX6B (i) ➡➡ B of Index 6

D[15:8] TTXIDX6G (i) ➡➡ G of Index 6

D[7:0] TTXIDX6R (i) ➡➡ R of Index 6

Texture Index Palette Register 7

Register Type: Read/Write

Read/Write Port: 8AB3h ~ 8AB0h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX7B (i) ➡➡ B of Index 7

D[15:8] TTXIDX7G (i) ➡➡ G of Index 7

D[7:0] TTXIDX7R (i) ➡➡ R of Index 7

Texture Index Palette Register 8

Register Type: Read/Write

Read/Write Port: 8AB7h ~ 8AB4h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX8B (i) ➡➡ B of Index 8

D[15:8] TTXIDX8G (i) ➡➡ G of Index 8

D[7:0] TTXIDX8R (i) ➡➡ R of Index 8

Texture Index Palette Register 9

Register Type: Read/Write

Read/Write Port: 8ABBh ~ 8AB8h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX9B (i) ➡➡ B of Index 9

D[15:8] TTXIDX9G (i) ➡➡ G of Index 9

D[7:0] TTXIDX9R (i) ➡➡ R of Index 9

Texture Index Palette Register 10

Register Type: Read/Write

Read/Write Port: 8ABFh ~ 8ABCh

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX10B (i) ➡➡ B of Index 10

D[15:8] TTXIDX10G (i) ➡➡ G of Index 10

D[7:0] TTXIDX10R (i) ➡➡ R of Index 10

Texture Index Palette Register 11

Register Type: Read/Write

Read/Write Port: 8AC3h ~ 8AC0h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX11B (i) ➡➡ B of Index 11

D[15:8] TTXIDX11G (i) ➡➡ G of Index 11

D[7:0] TTXIDX11R (i) ➡➡ R of Index 11

Texture Index Palette Register 12

Register Type: Read/Write

Read/Write Port: 8AC7h ~ 8AC4h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX12B (i) ➡➡ B of Index 12

D[15:8] TTXIDX12G (i) ➡➡ G of Index 12

D[7:0] TTXIDX12R (i) ➡➡ R of Index 12

Texture Index Palette Register 13

Register Type: Read/Write

Read/Write Port: 8ACBh ~ 8AC8h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX13B (i) ➡➡ B of Index 13

D[15:8] TTXIDX13G (i) ➡➡ G of Index 13

D[7:0] TTXIDX13R (i) ➡➡ R of Index 13

Texture Index Palette Register 14

Register Type: Read/Write

Read/Write Port: 8ACFh ~ 8ACCh

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX14B (i) ➡➡ B of Index 14

D[15:8] TTXIDX14G (i) ➡➡ G of Index 14

D[7:0] TTXIDX14R (i) ➡➡ R of Index 14

Texture Index Palette Register 15

Register Type: Read/Write

Read/Write Port: 8AD3h ~ 8AD0h

Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX15B (i) ➡➡ B of Index 15

D[15:8] TTXIDX15G (i) ➡➡ G of Index 15

D[7:0] TTXIDX15R (i) ➡➡ R of Index 15

Reserved Registers

Register Type: Read/Write

Read/Write Port: 8AFEh ~ 8AD4h

Default: xx xx xx xxh

D[31:0] Reserved

9.13.14.END OF PRIMITIVE SETTING REGISTER

Register Type: Read/Write

Read/Write Port: 8AFFh

Default: xxh

D[7:0] TEND ➡➡ End of Primitive List

This is a dummy register. The data stored in this register is no meaning.

9.13.15.STIPPLE PATTERN REGISTERS

Stipple Pattern 0 Register

Register Type: Read/Write

Read/Write Port: 8B03h ~ 8B00h

Default: xx xx xx xxh

D[31:0] T0STIP ➡➡ Stipple Pattern 0

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 1 Register

Register Type: Read/Write

Read/Write Port: 8B07h ~ 8B04h

Default: xx xx xx xxh

D[31:0] T1STIP ➡➡ Stipple Pattern 1

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 2 Register

Register Type: Read/Write

Read/Write Port: 8B0Bh ~ 8B08h

Default: xx xx xx xxh

D[31:0] T2STIP ➡➡ Stipple Pattern 2

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 3 Register

Register Type: Read/Write

Read/Write Port: 8B0Fh ~ 8B0Ch

Default: xx xx xx xxh

D[31:0] T3STIP ➡➡ Stipple Pattern 3

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 4 Register

Register Type: Read/Write

Read/Write Port: 8B13h ~ 8B10h

Default: xx xx xx xxh

D[31:0] T4STIP ➡➡ Stipple Pattern 4

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 5 Register

Register Type: Read/Write

Read/Write Port: 8B17h ~ 8B14h

Default: xx xx xx xxh

D[31:0] T5STIP ➡➡ Stipple Pattern 5

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 6 Register

Register Type: Read/Write

Read/Write Port: 8B1Bh ~ 8B18h

Default: xx xx xx xxh

D[31:0] T6STIP ➡➡ Stipple Pattern 6

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 7 Register

Register Type: Read/Write

Read/Write Port: 8B1Fh ~ 8B1Ch

Default: xx xx xx xxh

D[31:0] T7STIP ➡➡ Stipple Pattern 7

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 8 Register

Register Type: Read/Write

Read/Write Port: 8B23h ~ 8B20h

Default: xx xx xx xxh

D[31:0] T8STIP ➡➡ Stipple Pattern 8

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 9 Register

Register Type: Read/Write

Read/Write Port: 8B27h ~ 8B24h

Default: xx xx xx xxh

D[31:0] T9STIP ➡➡ Stipple Pattern 2

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 10 Register

Register Type: Read/Write

Read/Write Port: 8B2Bh ~ 8B28h

Default: xx xx xx xxh

D[31:0] T10STIP ➡➡ Stipple Pattern 10

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 11 Register

Register Type: Read/Write

Read/Write Port: 8B2Fh ~ 8B2Ch

Default: xx xx xx xxh

D[31:0] T11STIP ➡➡ Stipple Pattern 11

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 12 Register

Register Type: Read/Write

Read/Write Port: 8B33h ~ 8B30h

Default: xx xx xx xxh

D[31:0] T12STIP ➡➡ Stipple Pattern 12

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 13 Register

Register Type: Read/Write

Read/Write Port: 8B37h ~ 8B34h

Default: xx xx xx xxh

D[31:0] T13STIP ➡➡ Stipple Pattern 13

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 14 Register

Register Type: Read/Write

Read/Write Port: 8B3Bh ~ 8B38h

Default: xx xx xx xxh

D[31:0] T14STIP ➡➡ Stipple Pattern 14

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 15 Register

Register Type: Read/Write

Read/Write Port: 8B3Fh ~ 8B3Ch

Default: xx xx xx xxh

D[31:0] T15STIP ➡➡ Stipple Pattern 15

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 16 Register

Register Type: Read/Write

Read/Write Port: 8B43h ~ 8B40h

Default: xx xx xx xxh

D[31:0] T16STIP ➡➡ Stipple Pattern 16

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 17 Register

Register Type: Read/Write

Read/Write Port: 8B47h ~ 8B44h

Default: xx xx xx xxh

D[31:0] T17STIP ➡➡ Stipple Pattern 17

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 18 Register

Register Type: Read/Write

Read/Write Port: 8B4Bh ~ 8B48h

Default: xx xx xx xxh

D[31:0] T18STIP ➡➡ Stipple Pattern 18

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 19 Register

Register Type: Read/Write

Read/Write Port: 8B4Fh ~ 8B4Ch

Default: xx xx xx xxh

D[31:0] T19STIP ➡➡ Stipple Pattern 19

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 20 Register

Register Type: Read/Write

Read/Write Port: 8B53h ~ 8B50h

Default: xx xx xx xxh

D[31:0] T20STIP ➡➡ Stipple Pattern 20

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 21 Register

Register Type: Read/Write

Read/Write Port: 8B57h ~ 8B54h

Default: xx xx xx xxh

D[31:0] T21STIP ➡➡ Stipple Pattern 21

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 22 Register

Register Type: Read/Write

Read/Write Port: 8B5Bh ~ 8B58h

Default: xx xx xx xxh

D[31:0] T22STIP ➡➡ Stipple Pattern 22

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 23 Register

Register Type: Read/Write

Read/Write Port: 8B5Fh ~ 8B5Ch

Default: xx xx xx xxh

D[31:0] T23STIP ➡➡ Stipple Pattern 23

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 24 Register

Register Type: Read/Write

Read/Write Port: 8B63h ~ 8B60h

Default: xx xx xx xxh

D[31:0] T24STIP ➡➡ Stipple Pattern 24

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 25 Register

Register Type: Read/Write

Read/Write Port: 8B67h ~ 8B64h

Default: xx xx xx xxh

D[31:0] T25STIP ➡➡ Stipple Pattern 25

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 26 Register

Register Type: Read/Write

Read/Write Port: 8B6Bh ~ 8B68h

Default: xx xx xx xxh

D[31:0] T26STIP ➡➡ Stipple Pattern 26

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 27 Register

Register Type: Read/Write

Read/Write Port: 8B6Fh ~ 8B6Ch

Default: xx xx xx xxh

D[31:0] T27STIP ➡➡ Stipple Pattern 27

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 28 Register

Register Type: Read/Write

Read/Write Port: 8B73h ~ 8B70h

Default: xx xx xx xxh

D[31:0] T28STIP ➡➡ Stipple Pattern28

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 29 Register

Register Type: Read/Write

Read/Write Port: 8B77h ~ 8B74h

Default: xx xx xx xxh

D[31:0] T29STIP ➡➡ Stipple Pattern 29

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 30 Register

Register Type: Read/Write

Read/Write Port: 8B7Bh ~ 8B78h

Default: xx xx xx xxh

D[31:0] T30STIP ➡➡ Stipple Pattern 30

0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 31 Register

Register Type: Read/Write

Read/Write Port: 8B7Fh ~ 8B7Ch

Default: xx xx xx xxh

D[31:0] T31STIP ➡➡ Stipple Pattern 31

0: The pixel should not be written.

1: The pixel should be written.

10. ELECTRICAL CHARACTERISTICS

10.1. ABSOLUTE MAXIMUM RATINGS

Table 10.1- 1 Absolute Maximum Ratings

PARAMETER	MIN.	MAX.	UNIT
Ambient operation temperature	0	70	^0C
Storage temperature	-40	125	^0C
Input voltage	-0.3	5.5	V
Output voltage	-0.5	3.6	V

NOTE:

Stress above these listed may cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

10.2. DC CHARACTERISTICS

T_A = 0 - 70 ^{0}C, V_{DD} = 3.3 V ± 5 %, V_{DD} 5= 5 V ± 5 %,GND = 0 V

Table 10.2- 1 DC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
V_{IL}	Input low voltage	-0.5	0.8	V	
V_{IH}	Input high voltage	2.2	5.5	V	
V_{OL}	Output low voltage	-	0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH} = -1.0 mA
I_{IL}	Input leakage current	-	± 10	uA	
I_{OZ}	tristate leakage current	-	± 20	uA	0.45 < V_{OUT} < V_{DD}

10.3. DC CHARACTERISTICS FOR DAC (ANALOG OUTPUT CHARACTERISTICS)

Table 10.3-1 DC Characteristics for DAC

DESCRIPTION	MIN	TYPICAL	MAX	UNIT
Black Level	-	0	-	V
White Level	-	660	-	mV
ILE	-1.0	-	+1.0	LSB
DLE	-0.5	-	+0.5	LSB
1 LSB	-	2.625	-	mV

Iref	-	8.40	-	mA

10.4. AC CHARACTERISTICS FOR DAC (ANALOG OUTPUT CHARACTERISTICS)

Table 10.4- 1 AC Characteristics for DAC

DESCRIPTION	PARAMETER	CONDITION	TYPICAL	MAX.	UNIT
Settling Time	Tsett	R=37.5 ohm C1=30 pF	-	6	ns

10.5. AC CHARACTERISTICS FOR HOST INTERFACE TIMING SPECIFICATION

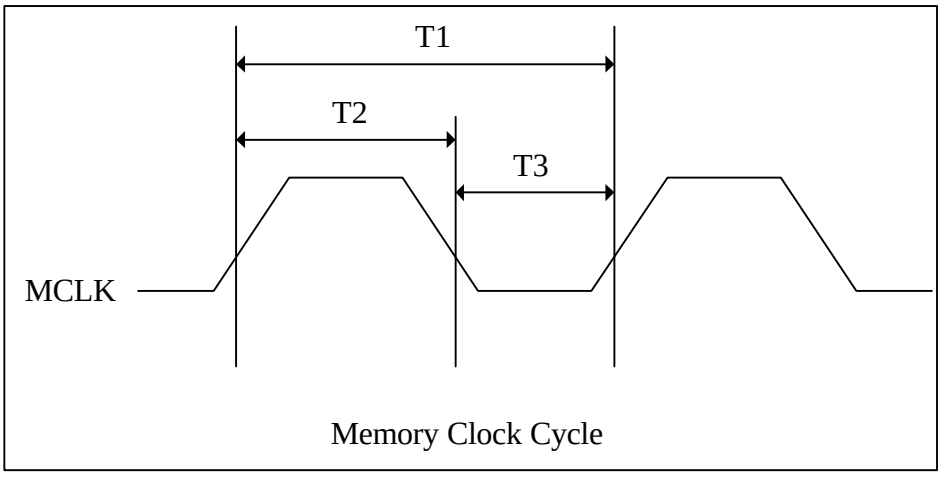
Host Interface 100MHz Timing Table

SYMBOL	PARAMETER	PENTIUM-II PROCESSOR	SiS620
Tco, max	Maximum driver Delay from input clock to output clock	4.71	4.45
Tco, min	Minimum driver Delay from input clock to output clock	0.71	0.80
Tsu	Setup time. The time for which the input data must be valid prior to the input clock	1.62	3.0
Th	Hold time. The time for which the input data must remain valid after the input clock	1.61	-0.1

(Units: ns)

10.6. AC CHARACTERISTICS FOR INTEGRATED 3D VGA CONTROLLER

Figure 10.6-1 Memory Clock Cycle



Memory Clock Cycle

Table 10.6- 1 Memory Clock Timing Table

SYMBOL	PARAMETER	MIN	MAX
T_1	MCLK Period	10	
T_2	MCLK High Time	4	
T_3	MCLK Low Time	4	

(Units: ns)

Table 10.6- 2 Required Timing Table

SYMBOL	PARAMETER	T-VALUE		MCLK 50MHz		MCLK 60MHz	
		Min.	Max.	Min.	Max.	Min.	Max.
T_{CPA}	Data Access Time from DQM Precharge	-	2	-	40	-	33.3
T_{RAC}	Data Access Time from CS#	-	4	-	80	-	66.6
T_{CAC}	Data Access Time from DQM	-	1	-	20	-	33.3
T_{CAA}	Data Access Time form Column Address	-	2	-	40	-	66.6

(Units: ns)

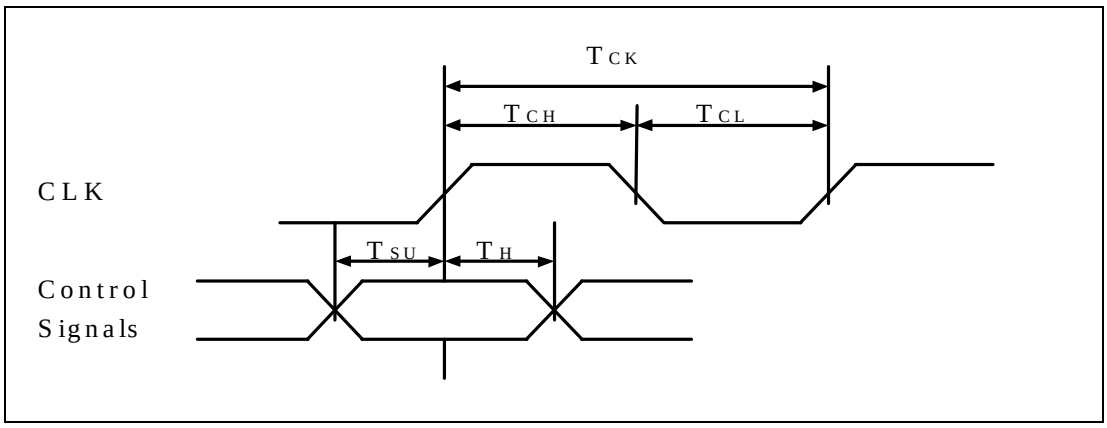


Figure 10.6- 2 SDRAM/SGRAM input/output Timing

Table 10.6- 3 SDRAM/SGRAM Timing Table

SYMBOL	PARAMETER		MIN	MAX.	UNITS
T_{CK}	Clock Cycle Time	latency=3	12 (83.3 MHz)		ns
		latency=2	18 (55 MHz)		ns
T_{CH}	CLK high level width		4		ns
T_{CL}	CLK low level width		4		ns
T_{SU}	Setup Timing		3.5		ns
T_H	Hold Timing		1.5		ns

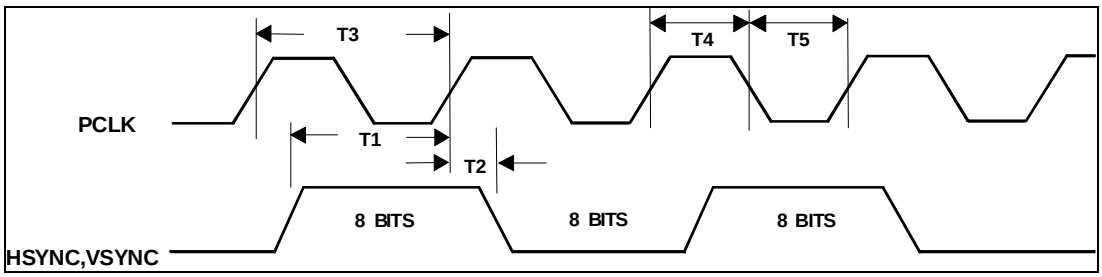


Figure 10.6- 3 Video Timing 4, 8, and 16 Bits/Pixel Modes

Table 10.6- 4 4, 1, 16 BPP Video Timing Table

SYMBOL	PARAMETER	MIN.	MAX.	NOTES
T_1	VSYNC Setup Time	10	-	
T_2	SYNC Hold Time	2	-	
T_3	PCLK Period	20	-	
T_4	PCLK High Time	7	-	
T_5	PCLK Low Time	7	-	

(Units: ns)

11. THERMAL ANALYSIS

11.1. CHIP THERMAL ANALYSIS WITHOUT HEAT SINK

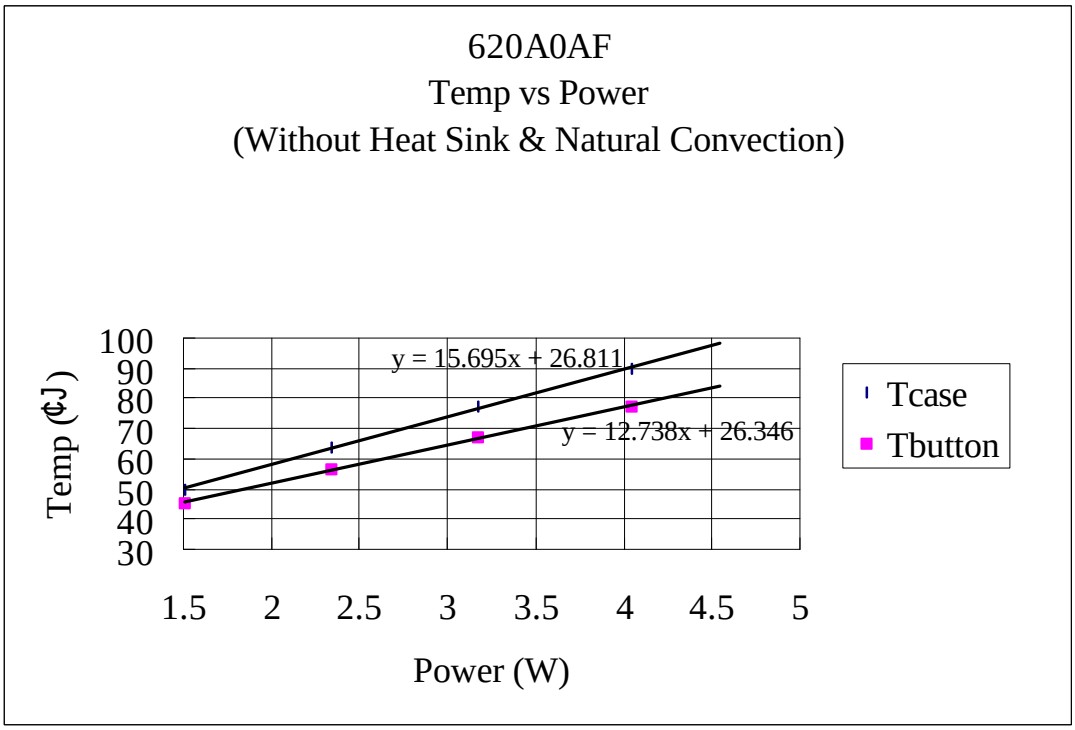
Room Temperature: 25.0¢ J

Result:

Power (W)	1.508	2.342	3.176	4.045
Tcase (¢)	50.0	63.8	77.6	89.6
Tbutton (¢)	45.3	56.3	67.3	77.5

Note: Tcase: Temperature at the molding compound surface.

Tbutton: Temperature at the back side of PCB where thermal balls are directly attached.

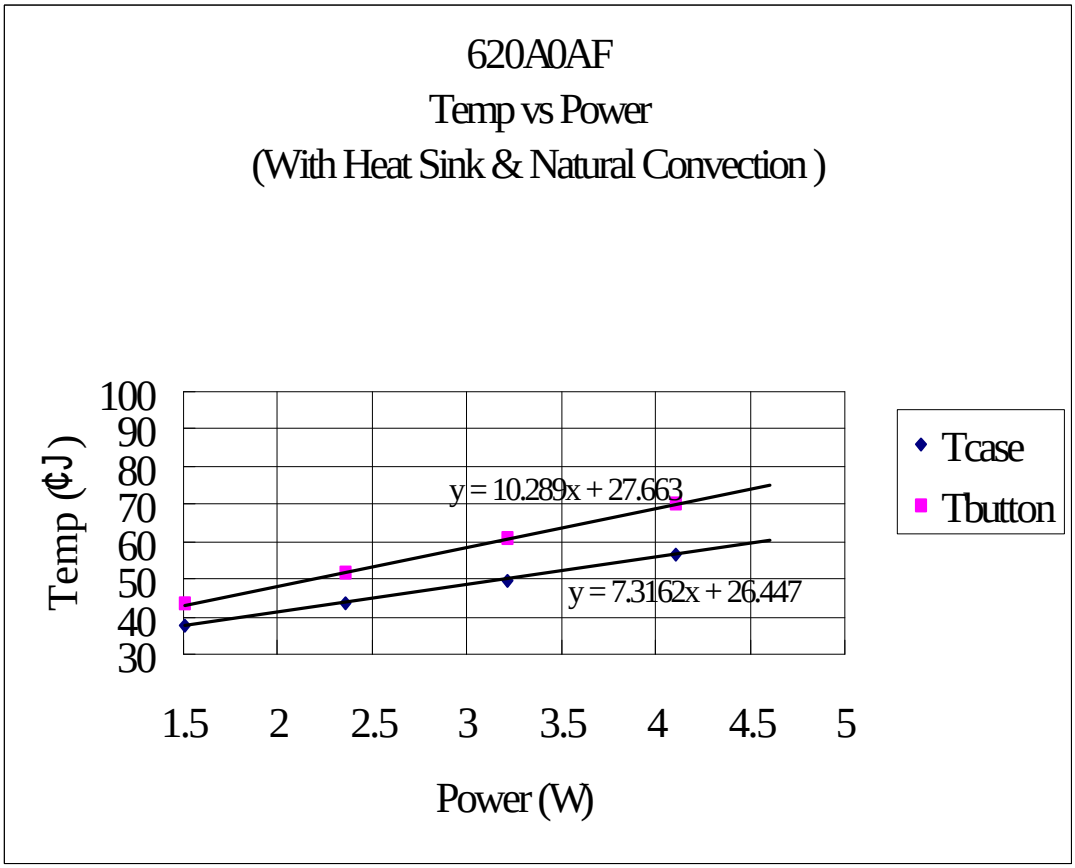


11.2. CHIP THERMAL ANALYSIS WITH HEAT SINK

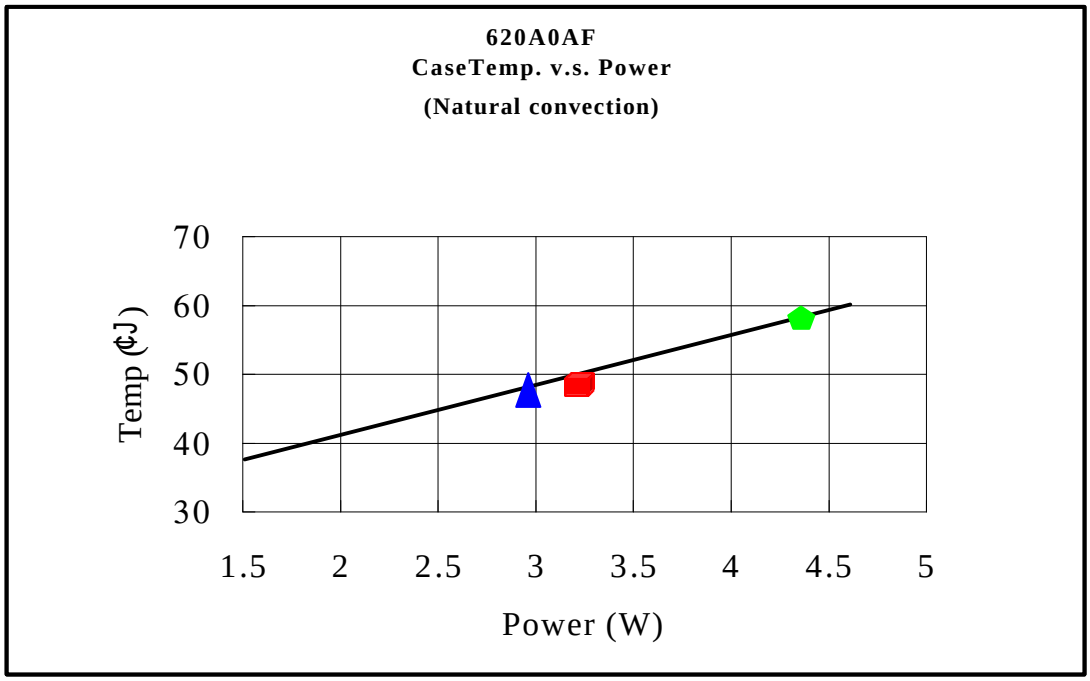
Room Temperature : 25.0¢ J

Result :

Power (W)	1.51	2.355	3.212	4.105
Tcase (¢)	37.8	43.3	49.8	56.7
Tbutton (¢)	43.4	51.6	60.7	70.0



Test Condition:

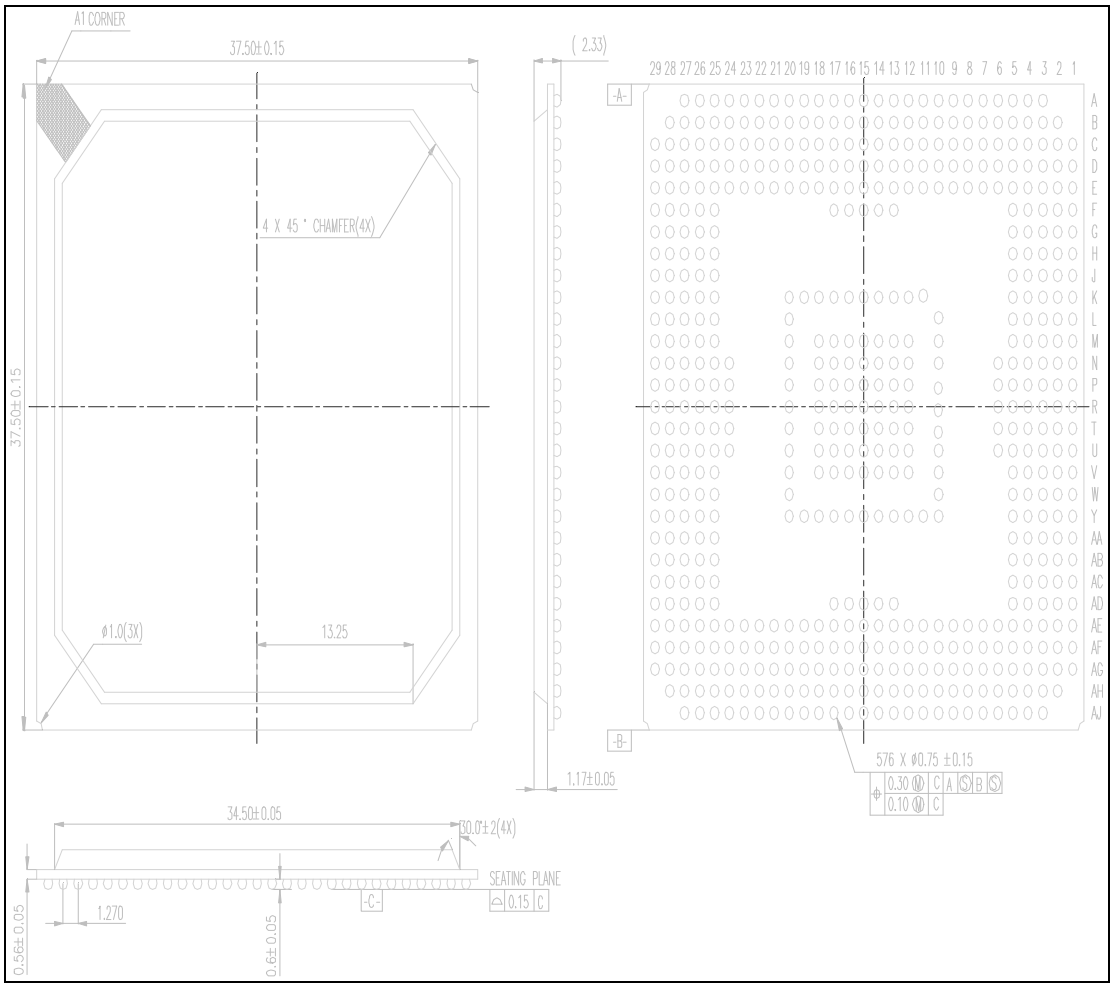


Symble	▲	■	⬟
S/W	3D Winbench / 3D Winmark	3D Winbench / 3D Winmark	3D Winbench / 3D Winmark
CPU Bus /DRAM /LFB Freq.	66/66/83	100/66/83	100/100/83
Period (min)	20	20	20
Resolution (bit)	640x480x16	640x480x16	1024x768x32
Refresh (HZ)	60	60	60
Case Temp. (℃) (With Heat Sink*)	48.3	49.6	58.7
Power Dissipation(W)	2.99	3.16	4.41

620 Thermal Performance Table

* Natural convection with 38mm*38mm aluminum heat sink.

12. MECHANICAL DIMENSION



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