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Figure

Table

Revision History

Date	Rev.	Description
Aug.19,1999	0.95	1.Revision to the Pin Assignment for USB (UV[4:0]) .
		2.GUI Device ID from 5400 to 5300.
		3.Add S3 and Ring Timing table to Chap 6, Function Description
		4.Revisions to Chap.7, Register 7D, Bit 4:1. The original description [43:40] is revisied to [44:41]
		5.Revisions to Chap.10_Register Summary-Legacy.doc
		6.Chap.15_Register Summary-SMBUS Revision to Register 1Ah~1Bh ACPI Fix Feature Control
		7.Chap.15_Register Summary-SMBus Reverse Register 4Ah and 4Bh.
		8.Chap.15_Register Summary-SMBUS Revisions Register 5E, Bit 8 and 9. (I^2C)
		9.Chap.15 Register 20~28h have been changed for USB wake-up function.
		10.Add Chap.22
Nov.30,1999	1.0	Formal Release

1 SiS540 Overview

The single chipset, SiS540, provides a high performance/low cost Desktop solution for the Super Socket 7 series CPUs based system by integrating a high performance North Bridge, advanced hardware 2D/3D GUI engine and Super-South bridge. In addition, SiS540 provides system-on-chip solution that complies with Easy PC Initiative which supports Instantly Available/OnNow PC technology, USB, Legacy Removal and Slotless Design and FlexATX form factor.

By integrating the Ultra-AGP™ technology and advanced 128-bit graphic display interface, SiS540 delivers high performance and up to 2 GB/s memory bandwidth. Furthermore, SiS540 provides powerful slice layer decoding DVD accelerator to improve the DVD playback performance. In addition to providing the standard interface for CRT monitors, SiS540 also provides the Digital Flat Panel Port (DFP) for a standard interface between a personal computer and a digital flat panel monitor. To extend functionality and flexibility, SiS also provides the " Video Bridge" (SiS301) to support the NTSC/PAL Video Output, Digital LCD Monitor and Secondary CRT Monitor, which reduces the external Panel Link transmitter and TV-Out encoder for cost effected solution. SiS540 also adopts Share System Memory Architecture which can flexibly utilize the frame buffer size up to 64MB.

The "Super-South Bridge" in SiS540 integrates all peripheral controllers /accelerators /interfaces. SiS540 provides a total communication solution including 10/100Mb Fast Ethernet for Office requirement. SiS540 offers AC' 97 compliant interface that comprises digital audio engine with 3D-hardware accelerator, on-chip sample rate converter, and professional wavetable along with separate modem DMA controller. SiS540 also provides interface to Low Pin Count (LPC) operating at 33 MHz clock which is the same as PCI clock on the host, and dual USB host controller with four USB ports that deliver better connectivity and 2 x 12Mb bandwidth.

The built-in fast PCI IDE controller supports the ATA PIO/DMA, and the Ultra DMA33/66 function that supports the data transfer rate up to 66 MB/s. It provides a separate data path for two IDE channels that can eminently improve the performance under the multi-tasking environment.

The following illustrates the system block diagram.

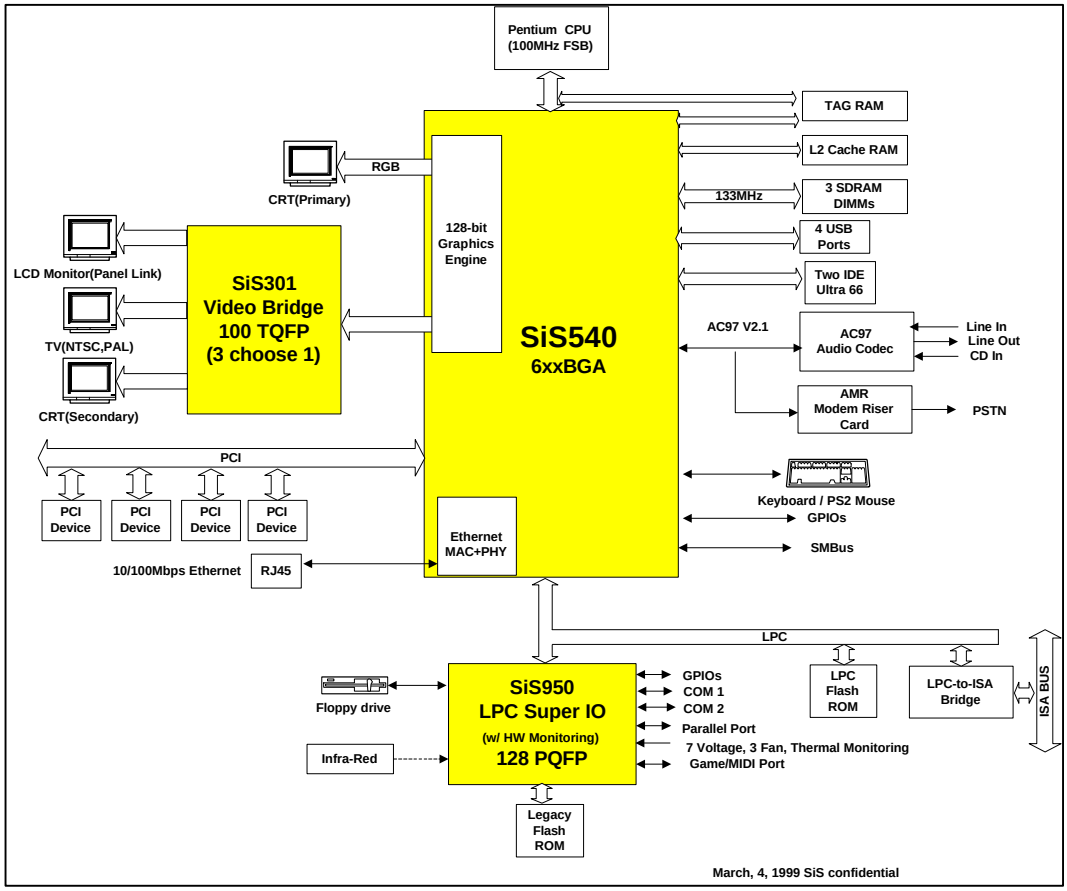


Figure 1-1 SiS540 System Block Diagram

1.1 Function Block Reference

TableBus #	Device #	Function #	Device ID	IDSEL	Device Function
Bus 0	Device 0	Function 0	0540h	AD11	North Bridge
Bus 0	Device 0	Function 1	5513h	AD11	PCI IDE
Bus 1	Device 0	Function 0	5300h	AD11	GUI
Bus 0	Device 1	Function 0	0008h	AD12	LPC
Bus 0	Device 1	Function 1	0900h	AD12	LAN
Bus 0	Device 1	Function 2	7001h	AD12	USB 0
Bus 0	Device 1	Function 3	7001h	AD12	USB 1
Bus 0	Device 1	Function 4	7018h	AD12	H/W Audio
Bus 0	Device 1	Function 6	7013h	AD12	S/W Modem
Bus 0	Device 2	Function 0	0001h	AD13	Virtual PCI-to-PCI Bridge

2 Features

Supports Intel/AMD/Cyrix/IDT Pentium CPU Host Bus at 66/83/90/95/100 MHz with 3.3V Bus Interface

- Supports the Pipelined Address of Pentium Compatible CPU
- 100/100, 95/95, 90/90 and 83/83 MHz Synchronous Host/DRAM Clocking Configuration
- 100/133, 100/66 and 66/100 MHz Asynchronous Host/DRAM Clocking Configuration
- Supports Host Bus Direct Access GUI Engine for Integrated 3D VGA Controller

Integrated Level 2 Cache Controller

- Write Back And Write through Cache Mode
- Direct Mapped Cache Organization
- Supports Pipelined Burst SRAM
- Supports 256K/512K/1M/2M Bytes Cache Sizes
- Cache Hit Read/Write Cycle of 3-1-1-1
- Cache Back-To-Back Read Cycle of 3-1-1-1-1-1-1-1
- Supports Single Read Allocation for L2 Cache
- Supports Concurrency of CPU to L2 Cache and Integrated A.G.P. VGA Master to DRAM Accesses

Integrated DRAM Controller

- Supports up to 3 Double Sided DIMMs (6 Rows Memory)
- Supports PC100/PC133 SDRAM Technology
- Supports NEC Virtual Channel Memory (VC-SDRAM) Technology
- System Memory Size up to 1.5 GB
- Supports Cacheable DRAM Sizes up to 512 Mbytes
- Supports 16Mb, 64Mb, 128Mb, 256Mb, 512Mb SDRAM Technology
- Suspend-To-RAM (STR)
- Relocatable System Management Memory Region
- Programmable Buffer Strength for CS#, DQM[7:0], WE#, RAS#, CAS#, CKE, MA[14:0] and MD[63:0]
- Shadow RAM Size from 640KB to 1MB In 16KB Increments
- Two Programmable PCI Hole Areas

Integrated A.G.P. Compliant Target Host-To-PCI Bridge

- AGP V2.0 Compliant

- Supports Graphic Window Size from 4Mbytes To 256Mbytes
- Supports Pipelined Process in CPU-To-Integrated 3D A.G.P. VGA Access
- Supports 8 Way, 16 Entries Page Table Cache for GART to Enhance Integrated A.G.P. VGA Controller Read/Write Performance
- Supports PCI-To-PCI Bridge Function for Memory Write from 33Mhz PCI Bus to Integrated A.G.P. VGA

Meets PC99 Requirements

PCI 2.2 Specification Compliant

High Performance PCI Arbiter

- Supports up to 4 PCI Masters
- Rotating Priority Arbitration Scheme
- Advanced Arbitration Scheme Minimizing Arbitration Overhead
- Guaranteed Minimum Access Time for CPU And PCI Masters

Integrated Host-To-PCI Bridge

- Zero Wait State Burst Cycles
- CPU-To-PCI Pipeline Access
- 256B to 4KB PCI Burst Length for PCI Masters
- PCI Master Initiated Graphical Texture Write Cycles Re-Mapping
- Reassembles PCI Burst Data Size into Optimized Block Size

Fast PCI IDE Master/Slave Controller

- Supports PCI Bus Mastering
- Native Mode and Compatibility Mode
- PIO Mode 0, 1, 2 , 3, 4
- Multiword DMA Mode 0, 1, 2
- Ultra DMA 33/66
- Two Independent IDE Channels Each with 16 DW FIFO

Virtual PCI-To-PCI Bridge

Integrated Ultra-AGP™ VGA for Hardware 2D/3D Video/Graphics Accelerators

- Supports Tightly Coupled 64 Bits 100Mhz Host Interface to VGA to Speed Up GUI Performance and the Video Playback Frame Rate
- AGP Rev. 2.0 Compliant
- Zero-Wait-State 128x4 Post-Write Buffer with Write Combine Capability
- Zero-Wait-State 128x4 2-Way Read Ahead Cache Capability
- Re-Locatable Memory-Mapped and I/O Address Decoding

- Flexible Design Shared Frame Buffer Architecture for Display Memory
- Shared System Memory Area up to 64MB
- Built-In 8K Bytes Texture Cache
- 32-Bit VLIW Floating-Point Primitive Setup Engine
- Peak Polygon Rate: 4M Polygon/Sec @ 1 Pixel/Polygon with 16bpp, Bilinear Textured, Z Buffered and Alpha Blended
- Supports Flat and Gouraud Shading
- Supports High Quality Dithering
- Supports Z-Test, Stencil Test, Alpha Test and Scissors Clipping Test
- Supports Z Pre-Test for Reducing Texture Read DRAM Bandwidth
- Supports 256 Rops
- Supports Individual Z-Buffer and Render Buffer at the same time
- Supports 16/24/32 BPP Z Buffer Integer/Floating Formats
- Supports 16/32 BPP Render Buffer Format
- Supports 1/2/4/8 Stencil Format
- Supports Per-Pixel Texture/Fog Perspective Correction
- Supports MIPMAP with Point-Sampled, Linear, Bi-Linear and Tri-Linear Texture Filtering
- Supports Single Pass Two MIPMAP Texture, One Texture On Clock
- Supports up to 2048x2048 Texture Size
- Supports 2' S Power of Width and Height Structure Rectangular Texture
- Supports 1/2/4/8 BPP Palletize Texture with 32 Bit ARGB Format
- Supports Palette for High Performance Palette Look Up
- Supports 1/2/4/8 BPP Luminance Texture
- Supports 1/2/4/8 BPP Intensity Texture
- Supports 8/16/24/32 BPP RGB/ARGB Texture Format
- Supports Video YUV Texture in all Supported Texture Formats
- Supports MIP-Mapped Texture Transparency, Blending, Wrapping, Mirror and Clamping
- Supports Fogging and Alpha Blending
- Supports Vertex Fogging, Linear Fogging Table and Non-Linear Fogging Table
- Supports Specula Lighting
- Supports Sort Dependent Edge Anti-Aliasing
- Supports Full Scene Anti-Aliasing

- Supports Hardware Back Face Culling
- Internal Full 32 Bits ARGB Format Ultra Pipelined Architecture for Ultra High Performance and High Rendering Quality
- 128-Bit 2D Engine with a Full Instruction Set
- Built-In 64x64x2 Bit-Mapped Hardware Cursor
- Built-In 32x32x16, 32x32x32 Bit-Mapped Color Hardware Cursor
- Maximum 64 MB Frame Buffer with Linear Addressing
- MPEG-2 ISO/IEC 13818-2 MP@ML and MPEG-1 ISO/IEC 11172-2 Standards Compliant
- Supports Advanced H/W DVD Accelerator
- Direct DVD to TV Playback
- Supports Single Frame Buffer Architecture
- Supports Two Independent Video Windows with Overlay Function and Scaling Factors
- Supports YUV-To-RGB Color Space Conversion
- Supports Bi-Linear Video Interpolation with Integer Increments of Pixel Accuracy
- Supports Graphic and Video Overlay Function
- Supports VCD/DVD to TV Playback Mode
- Simultaneous Graphic and TV Video Playback Overlay
- Supports Current Scan Line Of Refresh Red-Back and Interrupt
- Supports Tearing Free Double/Triple Buffer Flipping
- Supports Input Video Vertical Blank or Line Interrupt
- Supports RGB555, RGB565, YUV422 and YUV420 Video Playback Format
- Supports Filtered Horizontal up and down Scaling Playback
- Supports DVD Sub-Picture Playback Overlay
- Supports DVD Playback Auto-Flipping
- Built-In Two Video Playback Line Buffers
- Supports DCI Drivers
- Supports Direct Draw Drivers
- Built-In Programmable 24-Bit True-Color RAMDAC up to 270 Mhz Pixel Clock RAMDAC Snoop Function
- Built-In Reference Voltage Generator and Monitor Sense Circuit
- Supports Down-Loadable RAMDAC for Gamma Correction In High Color and True Color Modes
- Built-In Dual-Clock Generator

- Supports Multiple Adapters and Multiple Monitors
- Built-In PCI Multimedia Interface
- Built-In VESA Plug and Display for Digital TV-Out Encoder, Panellink™ (TMDS) and LVDS Digital Interface
- Supports Digital Flat Panel Port for Digital Monitor (LCD Panel)
- Built-In Secondary CRT Controller for Independent Secondary CRT, LCD or TV Digital Output
- Supports VESA Standard Super High Resolution Graphic Modes

  640x480 16/256/32K/64K/16M Colors 120 Hz NI

  800x600 16/256/32K/64K/16M Colors 120 Hz NI

  1024x768 256/32K/64K/16M Colors 120 Hz NI

  1280x1024 256/32K/64K/16M Colors 120 Hz NI

  1600x1200 256/32K/64K/16M Colors 100 Hz NI

  1920x1200 256/32K/64K/16M Colors 80 Hz NI

  Low Resolution Modes
- Supports Virtual Screen up to 4096x4096
- Fully DirectX 6.0 Compliant
- Efficient and Flexible Power Management with ACPI Compliance
- Supports DDC1, DDC2B and DDC 3.0 Specifications
- Cooperate with " SiS301 Video Bridge" to Support

  NTSC/PAL Video Output

  Digital LCD Monitor

  Secondary CRT Monitor

Low Pin Count Interface

- Forwards PCI I/O and Memory Cycles into LPC Bus
- Translates 8-/16-Bit DMA Cycles into PCI Bus Cycles

Advanced PCI H/W Audio & S/W Modem

- Advanced Wavetable Synthesizer

  64-Voices Polyphony Wavetable Synthesizer Supports All Combinations of Stereo/Mono, 8-/16-Bits, and Signed/Unsigned Samples

  Per Channel Volume and Envelop Control, Pitch Shift, Left/Right Pan, Tremolo, and Vibrato

  Global Effect Process for Reverb, Chorus and Echo

  DirectMusic™ Support with Unlimited Downloadable Samples in System Memory

DLS-1-Compatible Downloadable Samples Support

- DirectSound™ 3D

  64-Voice DirectSound™ Channels

  32-Voice DirectSound™ 3D Accelerator with IID, IAD and Doppler Effects on 3D Positional Audio Buffer

  DirectSound Accelerator for Volume, Pan and Pitch Shift Control on Streaming or Static Buffers

  VirtualHRTF Interactive 3D Positional Audio Accelerator for DirectX™ 5/6

- Advanced Streaming Architecture

  Microsoft WDM Streaming Architecture Compliant and Re-Routable Endpoint Support

  Three Stereo Capture Channels

  AC' 97/98 Stereo Recording Channel through AC-Link

- High Quality Audio and AC' 97/98 Support

  CD Quality Audio with 90db+ SNR Using External High Quality AC' 97/98 CODEC

  AC' 97/98 Support with Full Duplex, Independent Sample Rate Converter for Audio Recording and Playback

  On-Chip Sample Rate Converter Ensures All Internal Operation At 48khz

  High Precision Internal 26-Bit Digital Mixer with 20-Bit Digital Audio Output

- Full Legacy Compatibility

  SoundBlaster Pro/16

  VirtualFM™ Enhances Audio Experience through Realtime FM-To-Wavetable Conversion

  MPU-401 Compatible UART for External Or Internal Synthesis

- Telephony & Modem

  Full Duplex VirtualPhone Speaker Phone With Modem Capable AC' 97/98

  HSP V.90 Modem

- Software Support

  Complete DirectX Driver Suite (DirectSound3D, DirectSound, DirectMusic, DirectInput) for Windows 98/Windows 2000

  Configuration Installation and Diagnostics Under Real Mode DOS, Windows 98 DOS Box

  Windows 98/ Windows 2000 Configuration, Installation and Mixer Program

- Extras

  2-To-6 Speakers Output with Optional VirtaulFX, VirtualAC3

DirectX Timer for Video/Audio Synchronization

I^2S and SPDIF Interface

Advanced Power Management

- Meets ACPI 1.0 Requirements
- Meets APM 1.2 Requirements
- ACPI Sleep States Include S1, S2, S3, S4, S5
- CPU Power States Include C0, C1, C2, C3
- Power Button with Override
- RTC Day-Of-Month, Month-Of-Year Alarm
- 24-Bit Power Management Timer
- LED Blinking In S0,S1,S2 and S3 States
- System Power-Up Events Include: Power Button, Hot-Key, Keyboard Password/ Hot-Key, RTC Alarm, Modem Ring-In, SMBALT#, LAN, PME#, AC' 97 Wake-Up and USB Wake-Up
- Software Watchdog Timer
- PCI Bus Power Management Interface Spec. 1.0

Integrated DMA Controller

- Two 8237A Compatible DMA Controllers
- 8/16- Bit DMA Data Transfer
- Distributed DMA Support

Integrated Interrupt Controller

- Two 8259A Compatible Interrupt Controllers
- Level- Or Edge-Triggered Programmable Serial IRQ
- Interrupt Sources Re-Routable to Any IRQ Channel

Three 8254 Compatible Programmable 16-Bit Counters

- System Timer Interrupt
- Generate Refresh Request
- Speaker Tone Output

Integrated Keyboard Controller

- Hardwired Logic Provides Instant Response
- Supports PS/2 Mouse Interface
- Password Security and Password Power-Up
- System Sleep and Power-Up By Hot-Key
- KBC and PS/2 Mouse Can Be Individually Disabled

Integrated Real Time Clock (RTC) with 256B CMOS SRAM

- Supports ACPI Day-Of-Month and Month-Of-Year Alarm
- 256 Bytes Of CMOS SRAM
- Provides RTC H/W Year 2000 Solution

Universal Serial Bus Host Controller

- OpenHCI Host Controller with Root Hub
- Two USB Host Controllers
- Four USB Ports
- Supports Legacy Devices
- Over Current Detection

I^2C Bus/SMBUS Series Interface

Integrated Fast Ethernet Controller and 10/100 Megabit Per Second (Mbps) Physical Layer Transceivers for the PCI Local Bus

- Plug and Play Compatible
- High-Performance 32-Bit PCI Bus Master Architecture with Integrated Direct Memory Access (DMA) Controller for Low CPU and Bus Utilization
- Supports An Unlimited PCI Burst Length
- Supports Big Endian and Little Endian Byte Alignments
- Supports PCI Device ID, Vendor ID/Subsystem ID, Subsystem Vendor ID Programming through the EEPROM Interface
- Implements Optional PCI 3.3V Auxiliary Power Source 3.3Vaux Pin and Optional PCI
- IEEE 802.3 and 802.3u Standard Compatible
- IEEE 802.3u Auto Negotiation and Parallel Detection for Automatic Speed Selection
- Full Duplex and Half Duplex Mode for Both 10 and 100 Mbps.
- Fully Compliant ANSI X3.263 TP-PMD Physical Sub-Layer Which Includes Adaptive Equalization and Baseline Wander Correction.
- Automatic Jam and IEEE 802.3x Auto-Negotiation for Flow Control
- Single Access to Complete PHY Register Set
- Built-In Waveform Shaping Requires No External Filters
- Single 25Mhz Clock for 10 and 100 Mbps Operation.
- Power Down Of 10Base-T/100Base-TX Sections When Not In Use
- Jabber Control and Auto-Polarity Correction for 10Base-T.
- User Programmable LED Function Mapping
- Supports Software, Enhanced Software, and Automatic Polling Schemes to Internal

PHY Status Monitor and Interrupt

- Supports 10BASE-T, 100BASE-TX

NAND Tree for Ball Connectivity Testing

618-Balls BGA Package

1.8V Core with Mixed 3.3V and 5V I/O CMOS Technology

3 Pin Assignment

3.1 Pin Assignment (Top View)

3.1.1 SiS540 Pin Assignment (Top View-Left Side)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A			EESK	TXAVDD	REXT	HRTXRXN	AD7	AD12	C/BE1#	IRDY#	AD19	C/BE3#	AD28	PGNT1#	PGNT0#
B		AC_RESET#	EEDI	RXAVDD	OSC25MHI	HRTXRXP	AD5	AD11	AD15	TRDY#	AD17	AD23	AD26	PGNT2#	PREQ1#
C	PMCLK	AC_SDIN1	AC_SDIN0	EEDO	RXAVSS	AD1	AD4	AD10	AD14	DEVSEL#	AD16	AD21	AD25	AD30	PREQ0#
D	ACPILED	KBDAT	KBCLK	PMDAT	PLED0#	EECS	AD3	AD8	AD13	STOP#	C/BE2#	AD20	AD24	AD29	SMI#
E	USBVDD	UV3-	PME#	SMBALT#	PSON#	PCIRST#	AD2	C/BE0#	AD6	PAR	PLOCK#	AD18	AD22	AD31	PREQ2#
F	UV3+	USBVDD	UV2+	PWRBTN#	CKE	RING		AD0		AD9		FRAME#		AD27	INIT#
G	RTCVDD	AUXOK	UV0+	UV1+	UV2-										
H	OSC32KHO	OSC32KHI	PWROK	RTCVSS	UV0-	UV1-								VCC3	VCC3
J	CLK48M	SMCLK	INTD#	INTC#	INTB#				TPI-	TPI+	TPO-	TPO+	VCC3	VCC3	VCC3
K	EXTSMI#	AC_SYNC	AC_SDOUT	SMBDAT	INTA#	BATOK			QVDD(AUX)						
L	VMD63	GPIO7	GPIO1	AC_BIT_CLK	SERR#				IVDD(AUX)						
M	VMD58	VMD60	VMD61	VMD62	GPIO2	GPIO0			VCC3			RXAVSS	TXAVSS	OSC25AVSS	VSS
N	VDQM6	VDQM7	VMD56	VMD57	VMD59			VCC3	VCC3			VSS	VSS	VSS	VSS
P	VMD53	VMD55	VDQM4	VDQM5	VMD54	VCS#		VCC3	VCC3			VSS	VSS	VSS	VSS
R	VMD49	VMD50	VMD51	VMD52	VMD44	VMD48		VCC3	VCC3			VSS	VSS	VSS	VSS
T	VMD47	VMD46	VMD45	VMD43	VMD40	VMD32		VCC3	VCC3			VSS	VSS	VSS	VSS
U	VMD42	VMD41	VMD39	VMD38	VMD31				VCC3			VSS	VSS	VSS	VSS
V	VMD37	VMD36	VMD35	VMD34	VMD27	VDQM3			VCC3			VSS	VSS	VSS	VSS
W	VMD33	VMA10	VMA11	VBA1	VMD23				IVDD						
Y	VMD30	VMD29	VMD28	VMD26	VMD25	VMD15			IVDD						
AA	VMD24	VDQM2	VDQM1	VDQM0	VMD7				IVDD	IVDD	IVDD	VCC3	VCC3	VCC3	VCC3
AB	VMD22	VMD21	VMD20	VMD19	VMD18	SSYNC								VCC3	VCC3
AC	VMD17	VMD16	VMD14	VMD13	VMD12										
AD	VMD11	VMD10	VMD9	VMD8	VMD6	LAD0		IDA8		IDA10		IDA14		CBLIDA	IDB10
AE	VMD5	VMD4	VMD3	VMD2	SPK	LDRQ#	LAD3	IDA3	IDA9	IDACKA#	IDA12	IDREQA	IIRQA	IDB8	IDB12
AF	VMD1	VMD0	VSYNC	COMP	LAD2	SIRQ	LFRAME#	IDA2	IDA15	IDSAA1	IDECSA1#	IDB5	IDB2	IDB14	IDREQB
AG	OSCI	HSYNC	DDCDATA	RSET	LAD1	IDA7	IDA5	IDA13	IIOWA#	IDSAA0	IDB7	IDB4	IDB13	IDB15	IDSAB2
AH		DDCCLK	DCLKAVDD	VREF	ROUT	DACAVDD	IDA4	IDA1	ICHRDYA	IDSAA2	IDB6	IDB11	IDB1	IIOWB#	IDACKB#
AJ			ECLKAVDD	BOUT	GOUT	IDA6	IDA11	IDA0	IIORA#	IDECSA0#	IDB9	IDB3	IDEAVDD	ICHRDYB	IDSAB1
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

3.1.2 SiS540 Pin Assignment (Top View-Right Side)

16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A20M#	NMI	HD11	HD12	HD14	HD22	HD26	HD42	HD46	HD44	HD48	HD51			A
STPCLK#	INTR	HD3	HD7	HD13	HD21	HD28	HD31	HD40	HD45	HD49	HD53	HD55		B
CPURST	HD2	HD5	HD9	HD18	HD19	HD27	HD32	HD37	HD41	HD50	HD54	HD56	HD57	C
IGNE#	HD1	HD6	HD10	HD16	HD23	HD30	HD35	HD39	HD43	HD52	HD58	HD59	HD60	D
FERR#	HD4	HD8	HD20	HD17	HD25	HD29	HD34	HD36	HD47	HD61	HD62	HD63	SMIACT#	E
HD0		HD15		HD24		HD33		HD38	M/IO#	KEN#/INV	AHOLD	BRDY#	BOFF#	F
									D/C#	ADS#	HITM#	CPUAVDD	CPUCLK	G
VCC3								CACHE#	W/R#	EADS#	HBE0#	HBE2#	HBE3#	H
VCC3	VCC3	VCC3	IVDD	IVDD	IVDD				HLOCK#	HBE5#	HBE6#	HBE7#	HA20	J
					IVDD			NA#	HA19	HA17	HA16	HA15	HA13	K
					IVDD				HBE1#	HA9	HA11	HA10	HA5	L
VSS	VSS	VSS			VCC3			HBE4#	HA18	HA8	HA31	HA25	HA27	M
VSS	VSS	VSS			VCC3				HA14	HA21	HA24	HA22	HA4	N
VSS	VSS	VSS			VCC3	VCC3		HA12	HA7	HA3	HA29	KOE#	HA30	P
VSS	VSS	VSS			VCC3	VCC3		HA26	HA23	BWE#	ADV#	ADSC#	HA6	R
VSS	VSS	VSS			VCC3	VCC3		CCS1#	HA28	TA2	TA1	TA0	GWE#	T
VSS	VSS	VSS			VCC3				TA5	TA7	TA6	TA4	TA3	U
VSS	VSS	VSS			VCC3			MD60	TAGWE#	MD62	MD30	MD63	MD31	V
					IVDD				MD56	MD27	MD28	MD61	MD29	W
					IVDD			MD54	MD57	MD25	MD58	MD26	MD59	Y
VCC3	VCC3	VCC3	IVDD	IVDD	IVDD				MD52	MD22	MD55	MD23	MD24	AA
VCC3								DQM6	MD51	MD19	MD20	MD53	MD21	AB
									MA11	MD49	MD17	MD50	MD18	AC
IIORB#		MD36		MD42		SCAS#		CSB0#	DQM2	DQM7	DQM3	MD48	MD16	AD
IDB0	PCICLK	MD34	MD38	MD7	MD44	MD45	MD15	DQM1	MA13	MA14	CSB3#	CSB2#	CSB1#	AE
IIRQB	SDCLK	MD1	MD4	MD39	MD9	MD12	MD47	DQM5	CSA1#	MA8	MA9	MA10	MA12	AF
IDECSB1#	SDAVDD	MD33	MD3	MD6	MD41	MD11	MD14	DQM0	CSA2#	MA1	MA5	MA6	MA7	AG
IDECSB0#	ENTEST	MD0	MD35	MD5	MD8	MD43	MD46	DQM4	CSA3#	MA0	MA3	MA4		AH
IDSAB0	CBLIDB	MD32	MD2	MD37	MD40	MD10	MD13	WE#	SRAS#	CSA0#	MA2			AJ
16	17	18	19	20	21	22	23	24	25	26	27	28	29	

3.2 SiS540 Alphabetical Pin List

SIGNAL NAME	SiS540 BALL No.
A20M#	A16
AC_BIT_CLK	L4
AC_RESET#	B2
AC_SDIN0	C3
AC_SDIN1	C2
AC_SDOUT	K3
AC_SYNC	K2
ACPILED	D1
AD0	F8
AD1	C6
AD10	C8
AD11	B8
AD12	A8
AD13	D9
AD14	C9
AD15	B9
AD16	C11
AD17	B11
AD18	E12
AD19	A11
AD2	E7
AD20	D12
AD21	C12
AD22	E13
AD23	B12
AD24	D13
AD25	C13

SIGNAL NAME	SiS540 BALL No.
AD26	B13
AD27	F14
AD28	A13
AD29	D14
AD3	D7
AD30	C14
AD31	E14
AD4	C7
AD5	B7
AD6	E9
AD7	A7
AD8	D8
AD9	F10
ADS#	G26
ADSC#	R28
ADV#	R27
AHOLD	F27
AUXOK	G2
BATOK	K6
BOFF#	F29
BOUT	AJ4
BRDY#	F28
BWE#	R26
C/BE0#	E8
C/BE1#	A9
C/BE2#	D11
C/BE3#	A12
CACHE#	H24

SIGNAL NAME	SiS540 BALL No.
CBLIDA	AD14
CBLIDB	AJ17
CCS1#	T24
CKE	F5
CLK48M	J1
COMP	AF4
CPUAVDD	G28
CPUCLK	G29
CPURST	C16
CSA0#	AJ26
CSA1#	AF25
CSA2#	AG25
CSA3#	AH25
CSB0#	AD24
CSB1#	AE29
CSB2#	AE28
CSB3#	AE27
D/C#	G25
DACAVDD	AH6
DCLKAVDD	AH3
DDCCLK	AH2
DDCDATA	AG3
DEVSEL#	C10
DQM0	AG24
DQM1	AE24
DQM2	AD25
DQM3	AD27

SIGNAL NAME	SiS540 BALL No.
DQM4	AH24
DQM5	AF24
DQM6	AB24
DQM7	AD26
EADS#	H26
ECLKAVDD	AJ3
EECS	D6
EEDI	B3
EEDO	C4
EESK	A3
ENTEST	AH17
EXTSMI#	K1
FERR#	E16
FRAME#	F12
GOUT	AJ5
GPIO0	M6
GPIO1	L3
GPIO2	M5
GPIO7	L2
GWE#	T29
HA10	L28
HA11	L27
HA12	P24
HA13	K29
HA14	N25
HA15	K28
HA16	K27
HA17	K26
HA18	M25

SIGNAL NAME	SiS540 BALL No.
HA19	K25
HA20	J29
HA21	N26
HA22	N28
HA23	R25
HA24	N27
HA25	M28
HA26	R24
HA27	M29
HA28	T25
HA29	P27
HA3	P26
HA30	P29
HA31	M27
HA4	N29
HA5	L29
HA6	R29
HA7	P25
HA8	M26
HA9	L26
HBE0#	H27
HBE1#	L25
HBE2#	H28
HBE3#	H29
HBE4#	M24
HBE5#	J26
HBE6#	J27
HBE7#	J28
HD0	F16

SIGNAL NAME	SiS540 BALL No.
HD1	D17
HD10	D19
HD11	A18
HD12	A19
HD13	B20
HD14	A20
HD15	F18
HD16	D20
HD17	E20
HD18	C20
HD19	C21
HD2	C17
HD20	E19
HD21	B21
HD22	A21
HD23	D21
HD24	F20
HD25	E21
HD26	A22
HD27	C22
HD28	B22
HD29	E22
HD3	B18
HD30	D22
HD31	B23
HD32	C23
HD33	F22
HD34	E23

SIGNAL NAME	SiS540 BALL No.
HD35	D23
HD36	E24
HD37	C24
HD38	F24
HD39	D24
HD4	E17
HD40	B24
HD41	C25
HD42	A23
HD43	D25
HD44	A25
HD45	B25
HD46	A24
HD47	E25
HD48	A26
HD49	B26
HD5	C18
HD50	C26
HD51	A27
HD52	D26
HD53	B27
HD54	C27
HD55	B28
HD56	C28
HD57	C29
HD58	D27
HD59	D28
HD6	D18

SIGNAL NAME	SiS540 BALL No.
HD60	D29
HD61	E26
HD62	E27
HD63	E28
HD7	B19
HD8	E18
HD9	C19
HITM#	G27
HLOCK#	J25
HRTXRXN	A6
HRTXRXP	B6
HSYNC	AG2
ICHRDYA	AH9
ICHRDYB	AJ14
IDA0	AJ8
IDA1	AH8
IDA10	AD10
IDA11	AJ7
IDA12	AE11
IDA13	AG8
IDA14	AD12
IDA15	AF9
IDA2	AF8
IDA3	AE8
IDA4	AH7
IDA5	AG7
IDA6	AJ6
IDA7	AG6

SIGNAL NAME	SiS540 BALL No.
IDA8	AD8
IDA9	AE9
IDACKA#	AE10
IDACKB#	AH15
IDB0	AE16
IDB1	AH13
IDB10	AD15
IDB11	AH12
IDB12	AE15
IDB13	AG13
IDB14	AF14
IDB15	AG14
IDB2	AF13
IDB3	AJ12
IDB4	AG12
IDB5	AF12
IDB6	AH11
IDB7	AG11
IDB8	AE14
IDB9	AJ11
IDEAVDD	AJ13
IDECSA0#	AJ10
IDECSA1#	AF11
IDECSB0#	AH16
IDECSB1#	AG16
IDREQA	AE12
IDREQB	AF15
IDSAA0	AG10
IDSAA1	AF10

SIGNAL NAME	SiS540 BALL No.
IDSAA2	AH10
IDSAB0	AJ16
IDSAB1	AJ15
IDSAB2	AG15
IGNE#	D16
IIORA#	AJ9
IIORB#	AD16
IIOWA#	AG9
IIOWB#	AH14
IIRQA	AE13
IIRQB	AF16
INIT#	F15
INTA#	K5
INTB#	J5
INTC#	J4
INTD#	J3
INTR	B17
IRDY#	A10
IVDD(AUX)	L9
IVDD	J19
IVDD	J20
IVDD	J21
IVDD	K21
IVDD	L21
IVDD	W9
IVDD	W21
IVDD	Y9
IVDD	Y21
IVDD	AA9

SIGNAL NAME	SiS540 BALL No.
IVDD	AA10
IVDD	AA11
IVDD	AA19
IVDD	AA20
IVDD	AA21
KBCLK	D3
KBDAT	D2
KEN#/INV	F26
KOE#	P28
LAD0	AD6
LAD1	AG5
LAD2	AF5
LAD3	AE7
LDRQ#	AE6
LFRAME#	AF7
M/IO#	F25
MA0	AH26
MA1	AG26
MA10	AF28
MA11	AC25
MA12	AF29
MA13	AE25
MA14	AE26
MA2	AJ27
MA3	AH27
MA4	AH28
MA5	AG27
MA6	AG28
MA7	AG29

SIGNAL NAME	SiS540 BALL No.
MA8	AF26
MA9	AF27
MD0	AH18
MD1	AF18
MD10	AJ22
MD11	AG22
MD12	AF22
MD13	AJ23
MD14	AG23
MD15	AE23
MD16	AD29
MD17	AC27
MD18	AC29
MD19	AB26
MD2	AJ19
MD20	AB27
MD21	AB29
MD22	AA26
MD23	AA28
MD24	AA29
MD25	Y26
MD26	Y28
MD27	W26
MD28	W27
MD29	W29
MD3	AG19
MD30	V27
MD31	V29

SIGNAL NAME	SiS540 BALL No.
MD32	AJ18
MD33	AG18
MD34	AE18
MD35	AH19
MD36	AD18
MD37	AJ20
MD38	AE19
MD39	AF20
MD4	AF19
MD40	AJ21
MD41	AG21
MD42	AD20
MD43	AH22
MD44	AE21
MD45	AE22
MD46	AH23
MD47	AF23
MD48	AD28
MD49	AC26
MD5	AH20
MD50	AC28
MD51	AB25
MD52	AA25
MD53	AB28
MD54	Y24
MD55	AA27
MD56	W25
MD57	Y25

SIGNAL NAME	SiS540 BALL No.
MD58	Y27
MD59	Y29
MD6	AG20
MD60	V24
MD61	W28
MD62	V26
MD63	V28
MD7	AE20
MD8	AH21
MD9	AF21
NA#	K24
NMI	A17
OSC25MHI	B5
OSC25AVSS	M14
OSC32KHI	H2
OSC32KHO	H1
OSCI	AG1
OVDD(AUX)	K9
PAR	E10
PCICLK	AE17
PCIRST#	E6
PGNT0#	A15
PGNT1#	A14
PGNT2#	B14
PLED#	D5
PLOCK#	E11
PMCLK	C1
PMDAT	D4
PME#	E3

SIGNAL NAME	SiS540 BALL No.
PREQ0#	C15
PREQ1#	B15
PREQ2#	E15
PSON#	E5
PWRBTN#	F4
PWROK	H3
REXT	A5
RING	F6
ROUT	AH5
RSET	AG4
RTCVDD	G1
RTCVSS	H4
RXAVDD	B4
RXAVSS	M12
RXAVSS	C5
SCAS#	AD22
SDAVDD	AG17
SDCLK	AF17
SERR#	L5
SIRQ	AF6
SMBALT#	E4
SMBDAT	K4
SMCLK	J2
SMI#	D15
SMIACT#	E29
SPK	AE5
SRAS#	AJ25
SSYNC	AB6

SIGNAL NAME	SiS540 BALL No.
STOP#	D10
STPCLK#	B16
TA0	T28
TA1	T27
TA2	T26
TA3	U29
TA4	U28
TA5	U25
TA6	U27
TA7	U26
TAGWE#	V25
TPI-	J9
TPI+	J10
TPO-	J11
TPO+	J12
TRDY#	B10
TXAVDD	A4
TXAVSS	M13
USBVDD	F2
USBVDD	E1
UV0-	H5
UV0+	G3
UV1-	H6
UV1+	G4
UV2-	G5
UV2+	F3
UV3-	E2
UV3+	F1
VBA1	W4

SIGNAL NAME	SiS540 BALL No.
VCC3	H14
VCC3	H15
VCC3	H16
VCC3	J13
VCC3	J14
VCC3	J15
VCC3	J16
VCC3	J17
VCC3	J18
VCC3	M9
VCC3	M21
VCC3	N8
VCC3	N9
VCC3	N21
VCC3	P8
VCC3	P9
VCC3	P21
VCC3	P22
VCC3	R8
VCC3	R9
VCC3	R21
VCC3	R22
VCC3	T8
VCC3	T9
VCC3	T21
VCC3	T22
VCC3	U9
VCC3	U21

SIGNAL NAME	SiS540 BALL No.
VCC3	V9
VCC3	V21
VCC3	AA12
VCC3	AA13
VCC3	AA14
VCC3	AA15
VCC3	AA16
VCC3	AA17
VCC3	AA18
VCC3	AB14
VCC3	AB15
VCC3	AB16
VCS#	P6
VDQM0	AA4
VDQM1	AA3
VDQM2	AA2
VDQM3	V6
VDQM4	P3
VDQM5	P4
VDQM6	N1
VDQM7	N2
VMA10	W2
VMA11	W3
VMD0	AF2
VMD1	AF1
VMD10	AD2
VMD11	AD1
VMD12	AC5

SIGNAL NAME	SiS540 BALL No.
VMD13	AC4
VMD14	AC3
VMD15	Y6
VMD16	AC2
VMD17	AC1
VMD18	AB5
VMD19	AB4
VMD2	AE4
VMD20	AB3
VMD21	AB2
VMD22	AB1
VMD23	W5
VMD24	AA1
VMD25	Y5
VMD26	Y4
VMD27	V5
VMD28	Y3
VMD29	Y2
VMD3	AE3
VMD30	Y1
VMD31	U5
VMD32	T6
VMD33	W1
VMD34	V4
VMD35	V3
VMD36	V2
VMD37	V1
VMD38	U4

SIGNAL NAME	SiS540 BALL No.
VMD39	U3
VMD4	AE2
VMD40	T5
VMD41	U2
VMD42	U1
VMD43	T4
VMD44	R5
VMD45	T3
VMD46	T2
VMD47	T1
VMD48	R6
VMD49	R1
VMD5	AE1
VMD50	R2
VMD51	R3
VMD52	R4
VMD53	P1
VMD54	P5
VMD55	P2
VMD56	N3
VMD57	N4
VMD58	M1
VMD59	N5
VMD6	AD5
VMD60	M2
VMD61	M3
VMD62	M4
VMD63	L1

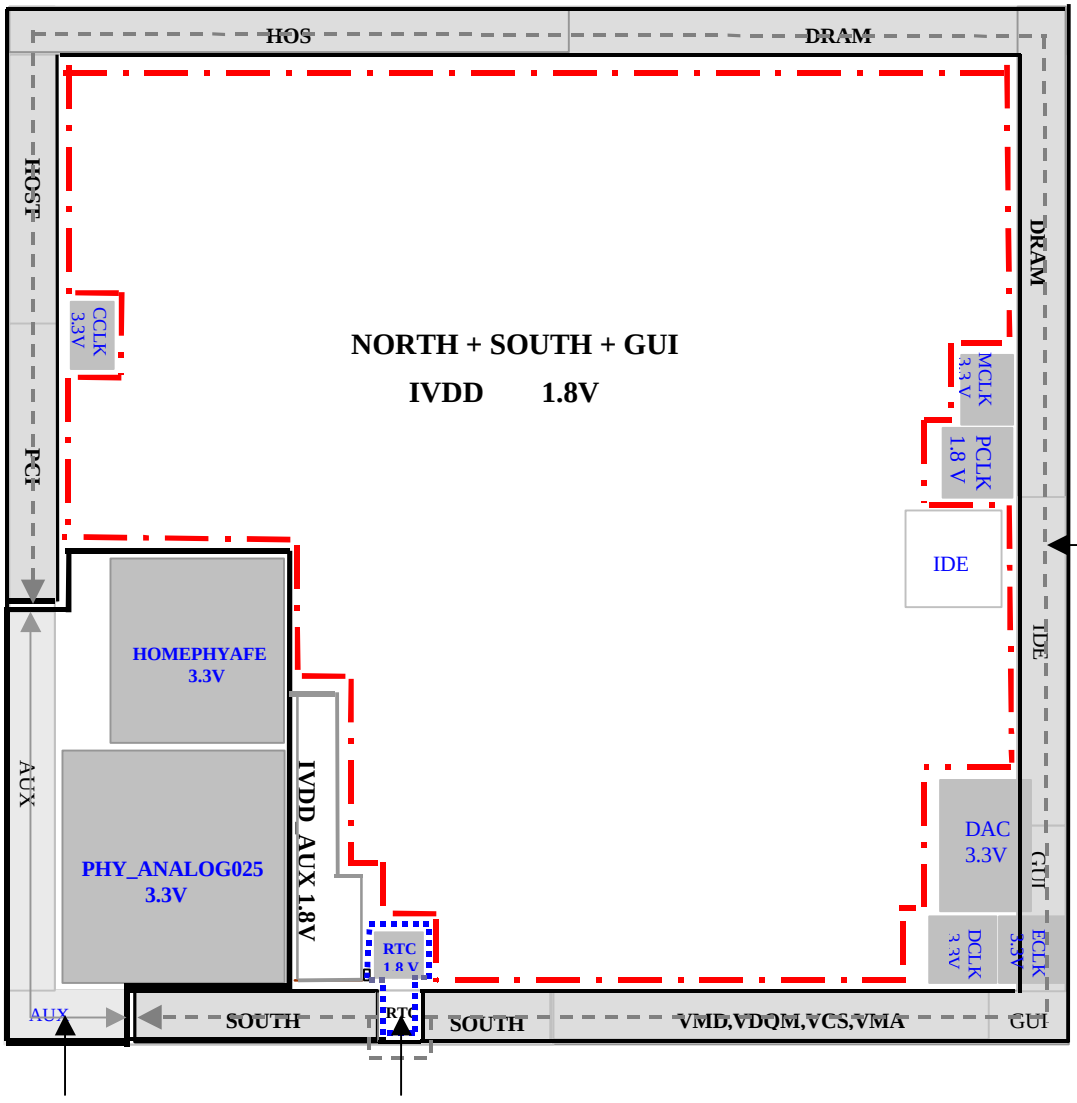
SIGNAL NAME	SiS540 BALL No.
VMD7	AA5
VMD8	AD4
VMD9	AD3
VREF	AH4
VSS	M15
VSS	M16
VSS	M17
VSS	M18
VSS	N12
VSS	N13
VSS	N14
VSS	N15
VSS	N16
VSS	N17
VSS	N18
VSS	P12
VSS	P13
VSS	P14
VSS	P15
VSS	P16
VSS	P17
VSS	P18
VSS	R12
VSS	R13
VSS	R14
VSS	R15
VSS	R16

SIGNAL NAME	SiS540 BALL No.
VSS	R17
VSS	R18
VSS	T12
VSS	T13
VSS	T14
VSS	T15
VSS	T16
VSS	T17

SIGNAL NAME	SiS540 BALL No.
VSS	T18
VSS	U12
VSS	U13
VSS	U14
VSS	U15
VSS	U16
VSS	U17
VSS	U18
VSS	V12

SIGNAL NAME	SiS540 BALL No.
VSS	V13
VSS	V14
VSS	V15
VSS	V16
VSS	V17
VSS	V18
VSYNC	AF3
W/R#	H25
WE#	AJ24

3.3 Power Plane



4 Pin Description (Preliminary)

Power Plane:
AUX: Power exists regardless the system is power down or power up unless the power cord is disconnected.

MAIN: Power exists only the system is power up.

RTC: Battery power.

4.1 Host interface Interface Signals

Name	Tolerance	Power Plane	Type Attr	Description
CPUCLK	3.3V	MAIN	I	**Host Clock :** Primary clock input to drive the part.
ADS#	3.3V	MAIN	I	**Address Status :** Address Status is driven by the CPU to indicate the start of a CPU bus cycle.
M/IO#	3.3V	MAIN	I	**Memory I/O Command Indicator :** Memory I/O definition is an input to indicate an I/O cycle when low, or a memory cycle when high.
D/C#	3.3V	MAIN	I	**Data/Code Command Indicator :** Data/Code is used to indicate whether the current cycle is a data or code access.
W/R#	3.3V	MAIN	I	**Write/Read Command Indicator :** Write/Read from the CPU indicates whether the current cycle is a write or read access.
BRDY#	3.3V	MAIN	O	**Burst Ready :** Burst Ready indicates that data presented is valid during a burst cycle.
CACHE#	3.3V	MAIN	I	**Cacheable Indicator :** The Cache pin indicates an L1 internally cacheable read cycle or a burst write-back cycle. If this pin is driven inactive during a read cycle, the CPU will not cache the returned data, regardless of the state of the KEN# pin.

KEN#/ INV	3.3V	MAIN	O	**Cache Enable/Invalidate :** This functions as both the KEN# signal during CPU read cycles, and the INV signal during L1 snoop cycles. During CPU cycles, KEN#/INV is normally low. KEN#/INV will be driven high during the 1st BRDY# or NA# assertion of a non-L1-cacheable CPU read. KEN#/INV is driven high (low) during the EADS# assertion of a PCI master DRAM write (read) snoop cycle.
NA#	3.3V	MAIN	O	**Next Address :** The SiS Chip always asserts NA# no matter the burst, or pipelined burst SRAMs are used. This signal is connected to CPU and indicates to CPU that it is ready to process a second cycle.
BOFF#	3.3V	MAIN	O	**Back Off :** The SiS Chip asserts BOFF# to stop the current CPU cycle.
AHOLD	3.3V	MAIN	O	**Address Hold :** The SiS Chip asserts AHOLD when a PCI master is performing a cycle to DRAM. AHOLD is held for the duration of PCI burst transfer. The SiS Chip negates AHOLD when the completion of PCI to DRAM read or write cycles complete and during PCI peer transfers.
HLOCK#	3.3V	MAIN	I	**Host Lock :** When CPU asserts HLOCK# to indicate the current bus cycle is locked.
EADS#	3.3V	MAIN	O	**External Address Strobe :** The EADS# is driven to indicate that a valid external address has been driven to the CPU address pins to be used for an inquire cycle.
HITM#	3.3V	MAIN	I	**Hit Modified :** Hit Modified indicates the snoop cycle hits a modified line in the L1 cache of the CPU.

SMIACT#	3.3V	MAIN	I	**System Management Interrupt Active :** The SMIACT# pin is used as the SMI acknowledgement input from the CPU to indicate that the SMI# is being acknowledged and the processor is operating in System Management Mode (SMM).
HBE[7:0]#	3.3V	MAIN	I	**Host Byte Enables :** CPU Byte Enables indicate which byte lanes on the CPU data bus carry valid data during the current bus cycle. HBE7# indicates that the most significant byte of the data bus is valid while HBE0# indicates that the least significant byte of the data bus is valid.
HA[31:3]	3.3V	MAIN	I/O	**Host Address Bus :** The Host Address is driven by the CPU during CPU bus cycles. The SiS Chip forwards it to either the DRAM or the PCI bus depending on the address range. The address bus is driven by the SiS Chip during bus master cycles or Flushing L2 cycle.
HD[63:0]	3.3V	MAIN	I/O	**Host Data Bus :** The Host data is driven by the CPU during CPU write cycle. The Host data is driven by L2 in three conditions. One is the CPU reads cycle and it hits the L2 cache. Another is the flushing L2 cycle. When CPU reading data from DRAM, the Host data is driven by SiS540. The other is the CPU reads cycle but the data does not exist in L2 cache, and it needs to perform a write-back cycle before a burst line fill.
STPCLK#	1.5V~5V	MAIN	OD	**Stop Clock :** STPCLK# will be asserted to inhibit or throttle CPU activities upon a pre-defined power management event occurs.
SMI#	1.5V~5V	MAIN	OD	**System Management Interrupt :** SMI# will be asserted when a pre-defined power management event occurs.

INIT#	1.5V~5V	MAIN	OD	**Initialization :** INIT is used to re-start the CPU without flushing its internal caches and registers. This signal requires an external pull-up resistor tied to 3.3V.
A20M#	1.5V~5V	MAIN	OD	**Address 20 Mask :** When A20M# is asserted, the CPU A20 signal will be forced to "0"
CPURST	1.5V	MAIN	O	**Host Bus Reset:** CPURST is used to keep all the bus agents in the same initial state before valid cycles issued.
FERR#	1.5V~5V	MAIN	I	**Floating Point Error :** CPU will assert this signal upon a floating point error occurring.
NMI	1.5V~5V	MAIN	OD	**Non-Maskable Interrupt :** A rising edge on NMI will trigger a non-maskable interrupt to CPU.
INTR	1.5V~5V	MAIN	OD	**Interrupt Request :** High-level voltage of this signal indicates the CPU that there is outstanding interrupt(s) needed to be serviced.

4.2 L2 Cache Interface Signals

Name	Tolerance	Power Plane	Type Attr	Description
KOE#	3.3V	MAIN	O	**Cache Output Enable :** Cache Output Enable for pipelined burst SRAM to enable data read.

CCS1#	3.3V	MAIN	O	**Cache Chip Select :** A L2 cache consisting of burst SRAMs will power up, if necessary, and perform an access if this signal is asserted when ADSC# is asserted. A L2 cache consisting of burst SRAMs will power down if this signal is negated when ADSC# is asserted. When CCS1# is negated a L2 cache consisting of burst SRAMs ignores ADS#. If CCS1# is asserts when ADS# is asserted a L2 cache consisting burst SRAMs will power up, if necessary, and perform an access.
GWE#	3.3V	MAIN	O	**Global-Write Enable :** GWE# asserted causes a QWORD to be written into the L2 cache. It is used for L2 cache line fills.
BWE#	3.3V	MAIN	O	**Byte-Write Enable :** When GWE#=1, the assertion of BWE# causes the byte lanes that are enabled via the HBE[7:0]# signals to be written into the L2 cache, if they are powered up.
ADSC#	3.3V	MAIN	O	**Cache Address Strobe :** Cache address strobe is for pipelined burst SRAM to load L2 cache address register from the SRAM address pins.
ADV#	3.3V	MAIN	O	**Cache Address Advance :** Cache address advance is for pipelined burst SRAM to advance to the next data into the cache line.
TAGWE#	3.3V	MAIN	O	**TAG RAM Write Enable Output :** When asserted, new state and/or new TAG address are written into the external tag RAM.
TA[7:0]	3.3V	MAIN	I/O	**TAG RAM Data Bus Lines :** The voltage level must be the same as DRAM voltage level.

4.3 DRAM Controller

Name	Tolerance	Power Plane	Type Attr	Description

SDCLK	3.3V/5V	MAIN	I	SDRAM Clock Input
MD[63:0]	3.3V	MAIN	I/O	System Memory Data Bus
MA[14:0]	3.3V	MAIN	O	System Memory Address Bus
CSA[3:0]#	3.3V	MAIN	O	SDRAM Chip Select
CSB[3:0]#	3.3V	MAIN	O	SDRAM Chip Select Signals (Duplicated Copy)
DQM[7:0]#	3.3V	MAIN	O	SDRAM Input/Output Data Mask
WE#	3.3V	MAIN	O	SDRAM Write Enable
SRAS#	3.3V	MAIN	O	SDRAM Row Address Strobe
SCAS#	3.3V	MAIN	O	SDRAM Column Address Strobe
CKE	3.3V	AUX	O	SDRAM Clock Enable During Suspend-to-DRAM mode (ACPI S2 or S3 state), SDRAM can be put into self-refresh mode by asserting CKE.

4.4 PCI Interface

Name	Tolerance	Power Plane	Type Attr	Description
PCICLK	3.3V/5V	MAIN	I	**PCI Clock :** The PCICLK input provides the fundamental timing and the internal operating frequency for the SiS Chip. It runs at the same frequency and skew of the PCI local bus.
C/BE[3:0]#	3.3V/5V	MAIN	I/O	**PCI Bus Command and Byte Enables:** PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. C/BE[3:0]# are outputs when the SiS Chip is a PCI bus master and inputs when it is a PCI slave.

AD[31:0]	3.3V/5V	MAIN	I/O	**PCI Address /Data Bus:** In address phase: 1.When the SiS Chip is a PCI bus master, AD[31:0] are output signals. 2.When the SiS Chip is a PCI target, AD[31:0] are input signals. In data phase: 1.When the SiS Chip is a target of a memory read/write cycle, AD[31:0] are floating. 2.When the SiS Chip is a target of a configuration or an I/O cycle, AD[31:0] are output signals in a read cycle, and input signals in a write cycle.
PAR	3.3V/5V	MAIN	I/O	**Parity :** SiS540 drives out Even Parity covering AD[31:0] and C/BE[3:0]#. It does not check the input parity signal.
FRAME#	3.3V/5V	MAIN	I/O	**Frame#:** FRAME# is an output when the SiS Chip is a PCI bus master. The SiS Chip drives FRAME# to indicate the beginning and duration of an access. When the SiS Chip is a PCI slave device, FRAME# is an input signal.
IRDY#	3.3V/5V	MAIN	I/O	**Initiator Ready :** IRDY# is an output when the SiS Chip is a PCI bus master. The assertion of IRDY# indicates the current PCI bus master's ability to complete the current data phase of the transaction. For a read cycle, IRDY# indicates that the PCI bus master is prepared to accept the read data on the following rising edge of the PCI clock. For a write cycle, IRDY# indicates that the bus master has driven valid data on the PCI bus. When the SiS Chip is a PCI slave, IRDY# is an input pin.

TRDY#	3.3V/5V	MAIN	I/O	**Target Ready :** TRDY# is an output when the SiS Chip is a PCI slave. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, TRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, TRDY# indicates that the target is prepared to accept data from the PCI bus. When the SiS Chip is a PCI master, it is an input pin.
STOP#	3.3V/5V	MAIN	I/O	**Stop# :** STOP# indicates that the bus master must start terminating its current PCI bus cycle at the next clock edge and release control of the PCI bus. STOP# is used for disconnect, retry, and target-abort sequences on the PCI bus.
DEVSEL#	3.3V/5V	MAIN	I/O	**Device Select :** As a PCI target, SiS Chip asserts DEVSEL# by doing positive or subtractive decoding. SiS Chip positively asserts DEVSEL# when the DRAM address is being accessed by a PCI master, PCI configuration registers or embedded controllers' registers are being addressed, or the BIOS memory space is being accessed. The low 16K I/O space and low 16M memory space are responded subtractively. The DEVESEL# is an input pin when SiS Chip is acting as a PCI master. It is asserted by the addressed agent to claim the current transaction.
PLOCK#	3.3V/5V	MAIN	I/O	**PCI Lock :** When PLOCK# is sampled asserted at the beginning of a PCI cycle, SiS540 considers itself being locked and remains in the locked state until PLOCK# is sampled and negated at the following PCI cycle.
PREQ [2:0]#	3.3V/5V	MAIN	I	**PCI Bus Request :** PCI Bus Master Request Signals
PGNT [2:0]#	3.3V	MAIN	O	**PCI Bus Grant :** PCI Bus Master Grant Signals

INT[A:D]#	3.3V/5V	MAIN	I	**PCI interrupt A,B,C,D :** The PCI interrupts will be connected to the inputs of the internal Interrupt controller through the rerouting logic associated with each PCI interrupt.
PCIRST#	3.3V	AUX	O	**PCI Bus Reset :** PCIRST# will be asserted during the period when PWROK is low, and will be kept on asserting until about 10~14ms after PWROK goes high.
SERR#	3.3V/5V	MAIN	I	**System Error :** When sampled active low, a non-maskable interrupt (NMI) can be generated to CPU if enabled.

4.5 PCI IDE Interface

Name	Tolerance	Power Plane	Type Attr	Description
IDA[15:0]	3.3V/5V	MAIN	I/O	Primary Channel Data Bus
IDB[15:0]	3.3V/5V	MAIN	I/O	Secondary Channel Data Bus
IDECSA [1:0]#	3.3V	MAIN	O	Primary Channel CS[1:0]
IDECSB [1:0]#	3.3V	MAIN	O	Secondary Channel CS[1:0]
IIOR [A:B]#	3.3V	MAIN	O	Primary/Secondary Channel IOR# Signals
IIOW [A:B]#	3.3V	MAIN	O	Primary/Secondary Channel IOW# Signals
ICHRDY [A:B]	3.3V/5V	MAIN	I	Primary/Secondary Channel ICHRDY# Signals
IDREQ [A:B]	3.3V/5V	MAIN	I	Primary/Secondary Channel DMA Request Signals
IDACK [A:B]#	3.3V	MAIN	O	Primary/Secondary Channel DMACK# Signals

IIRQ [A:B]	3.3V/5V	MAIN	I	Primary/Secondary Channel Interrupt Signals
IDSAA [2:0]	3.3V	MAIN	O	Primary Channel Address [2:0]
IDSAB [2:0]	3.3V	MAIN	O	Secondary Channel Address [2:0]
CBLID [A:B]	3.3V/5V	MAIN	I	Primary/Secondary Ultra-66 Cable ID

4.6 VGA Interface

Name	Tolerance	Power Plane	Type Attr	Description
HSYNC	3.3V	MAIN	O	Horizontal Sync
VSYNC	3.3V	MAIN	O	Vertical Sync
SSYNC	3.3V	MAIN	O	Stereo Sync
DDCCLK	3.3V/5V	MAIN	I/O	Display Data Channel Clock Line
DDCDATA	3.3V/5V	MAIN	I/O	Display Data Channel Data Line
COMP		MAIN	AI	**Compensation Pin:** Connect this pin to AVDD via a 0.1uF capacitor
RSET		MAIN	AI	**Reference Resistor:** An external resistor is connected between the RSET pin and AGND to control the magnitude of the full-scale current.
VREF		MAIN	AI	**Voltage Reference:** Connect 0.1uF Capacitor to Ground.
VCS#	3.3V	MAIN	I/O	**VGA Frame Buffer Cache Chip Select**
ROUT		MAIN	AO	**Red Signal Output**
GOUT		MAIN	AO	**Green Signal Output**
BOUT		MAIN	AO	**Blue Signal Output**

VBA1/ VBCLK	3.3V	MAIN	O I/O	**Display Memory Bank Select:** When 128bits DRAM interface enable, it represents the Memory Bank Select **Digital Video Clock Input:** When Video Bridge connected, it represents the Digital Video Clock Input
VMA11/ VGCLK	3.3V	MAIN	O O	**Display Memory Address bit 11** When 128bits DRAM interface enable, it represents the Memory Address bit 11 **Digital Video Clock Output:** When Video Bridge connected, it represents the Digital Video Clock Output
VMA10/ VBHCLK	3.3V	MAIN	O O	**Display Memory Address bit 10** When 128bits DRAM interface enable, it represents the Memory Address bit 10 **Control Clock Output:** When Video Bridge connected, it represents the Control Clock Output
VMD[63:60]	3.3V	MAIN	I/O	**Display Memory Data Bus bits [63:60]**
VMD[59:52]/ VBRGB[7:0]	3.3V	MAIN	I/O O	**Display Memory Data Bus bits [59:52]** **Digital Video Data bits [7:0]**
VMD[51:49]/ VBRGB[18:16]	3.3V	MAIN	I/O O	**Display Memory Data Bus bits [51:49]** **Digital Video Data bits [18:16]**
VMD[48:44]/ VBRGB[19:23]	3.3V	MAIN	I/O O	**Display Memory Data Bus bits [48:44]** **Digital Video Data bits [19:23]**
VMD[43:42]/ VBRGB[10:11]	3.3V	MAIN	I/O O	**Display Memory Data Bus bits [43:42]** **Digital Video Data bits [10:11]**
VMD[41:40]/ VBRGB[9:8]	3.3V	MAIN	I/O O	**Display Memory Data Bus bits [41:40]** **Digital Video Data bits [9:8]**
VMD[39:38]/ VBRGB[13:12]	3.3V	MAIN	I/O O	**Display Memory Data Bus bits [39:38]** **Digital Video Data bits [13:12]**
VMD[37:36]/ VBRGB[14:15]	3.3V	MAIN	I/O O	**Display Memory Data Bus bits [37:36]** **Digital Video Data bits [14:15]**

VMD35/ VBBLANKN	3.3V	MAIN	I/O O	**Display Memory Data Bus bit 35** **Digital Video Display Enable**
VMD[34:33]/ VBCTL[0:1]	3.3V	MAIN	I/O O	**Display Memory Data Bus bits [34:33]** **Video Bridge Data Control bits [0:1]**
VMD32/ VBCAD	3.3V	MAIN	I/O I/O	**Display Memory Data Bus bit 32** **Video Bridge Programming Control**
VMD31/ VBHSYNC	3.3V	MAIN	I/O I/O	**Display Memory Data Bus bit 31** **Digital Video Horizontal Sync**
VMD30/ VBVSYNC	3.3V	MAIN	I/O I/O	**Display Memory Data Bus bit 30** **Digital Video Vertical Sync**
VMD29/ DDC2CLK	3.3V	MAIN	I/O I/O	**Display Memory Data Bus bit 29** **Second Display data channel clock line**
VMD28/ DDC2DATA	3.3V	MAIN	I/O I/O	**Display Memory Data Bus bit 28** **Second Display data channel data line**
VMD[27:0]	3.3V	MAIN	I/O	**Display Memory Data Bus bits [27:0]**
VDQM[7:4]	3.3V	MAIN	O	**Display Memory SDRAM Input /Output Mask[7:4]**
VDQM[3:2]/ CS[A:B]5#	3.3V	MAIN	O	**Display Memory SDRAM Input /Output Mask[3:2]** **SDRAM Chip Select Signals**
VDQM[1:0]/ CS[A:B]4#	3.3V	MAIN	O	**Display Memory SDRAM Input /Output Mask[1:0]** **SDRAM Chip Select Signals**
OSCI	3.3V/5V	MAIN	I	**External 14.318MHz Clock Input**
ENTEST	3.3V/5V	MAIN	I	**Test Mode Enable**

4.7 Power management Interface

Name	Tolerance	Power Plane	Type Attr	Description
ACPILED	<=5V	AUX	OD	**ACPILED :** ACPILED can be used to control the blinking of an LED at the frequency of 1 Hz to indicate the system is at power saving mode.

EXTSMI#/ THERM#	3.3V/5V	MAIN	I I	**External SMI#:** EXTSMI# can be used to generate wakeup event, sleep event, or SCI/SMI#/GPEIRQ event to the ACPI-compatible power management unit. **Thermal Detect :** THERM# is connected to the internal ACPI-compatible power management unit as an indication of outstanding thermal event. An active THERM# event can be used to generate SCI/SMI#/GPEIRQ. If THERM# is activated for more than 2 second, a thermal override event will occur and the system will enter CPU thermal throttling mode automatically.
PME#	3.3V/5V	AUX	I/O	**PME# :** When the system is in power-down mode, an active low event on PME# will cause the PSON# to go low and hence turn on the power supply. When the system is in suspend mode, an active PME# event will cause the system wakeup and generate an SCI/SMI#/GPEIRQ.
PSON#	<=5V	AUX	OD	**ATX Power ON/OFF control:** PSON# is used to control the on/off state of the ATX power supply. When the ATX power supply is in the OFF state, an activated power-on event will force the power supply to ON state.
PWRBTN#	3.3V/5V	AUX	I	**Power Button:** This signal is from the power button switch and will be monitored by the ACPI-compatible power management unit to switch the system between working and sleeping states.
RING	3.3V/5V	AUX	I	**Ring Indication :** An active RING pulse and lasting for more than 4ms will cause a wakeup event for system to wake from S1~S5.

4.8 SMBus Interface

Name	Tolerance	Power Plane	Type Attr	Description

SMBDAT/ I²CDAT	3.3V/5V	MAIN	I/OD I/OD	**SMBus Data :** SMBus data input/output pin. **I²C Data :** I²C data input/output pin.
SMCLK/ I²CCLK	3.3V/5V	MAIN	I/OD I/OD	**SMBus Clock :** SMBus clock input/output pin. **I²C Clock :** I²C clock input/output pin.
SMBALT# /I²CALT# /GPIO15	3.3V/5V	AUX	I/OD I/OD I/O/OD	**SMBus Alert :** This pin is used for SMBus device to wake up the system from sleep state or to generate SCI/SMI#/GPEIRQ. **I²C Alert :** This pin is used for I²C device to wake up the system from sleep state or to generate SCI/SMI#/GPEIRQ. **General Purpose Input/Output 15 :** Refer to GPIO description.

4.9 Keyboard controller Interface

Name	Tolerance	Power Plane	Type Attr	Description
KBDAT/ GPIO10	3.3V/5V	AUX	I/OD I/O/OD	**Keyboard Dada :** When the internal keyboard controller is enabled, this pin is used as the keyboard data signal. **General Purpose Input/Output 10 :** Refer to GPIO description.
KBCLK/ GPIO11	3.3V/5V	AUX	I/OD I/O/OD	**Keyboard Clock :** When the internal keyboard controller is enabled, this pin is used as the keyboard clock signal. **General Purpose Input/Output 11 :** Refer to GPIO description.

PMDAT/ GPIO12	3.3V/5V	AUX	I/OD I/O/OD	**PS/2 Mouse Data:** When the internal keyboard and PS/2 mouse controllers are enabled, this pin is used as PS/2 mouse data signal. **General Purpose Input/Output 12 :** Refer to GPIO description.
PMCLK/ GPIO13	3.3V/5V	AUX	I/OD I/O/OD	**PS/2 Mouse Clock:** When the internal keyboard and PS/2 mouse controllers are enabled, this pin is used as the PS/2 mouse clock signal. **General Purpose Input/Output 13 :** Refer to GPIO description.

4.10 LPC Interface

Name	Tolerance	Power Plane	Type Attr	Description
LAD[3:0]	3.3V/5V	MAIN	I/O	**LPC Address/Data Bus :** LPC controller drives these four pins to transmit LPC command, address, and data to LPC device.
LDRQ#	3.3V/5V	MAIN	I	**LPC DMA Request 0:** This pin is used by LPC device to request DMA cycle.
LFRAME#	3.3V	MAIN	O	**LPC Frame :** This pin is used to notify LPC device that a start or a abort LPC cycle will occur.
SIRQ	3.3V/5V	MAIN	I/OD	**Serial IRQ :** This signal is used as the serial IRQ line signal.

4.11 RTC Interface

Name	Tolerance	Power Plane	Type Attr	Description

AUXOK	1.8V	RTC	I	**Auxiliary Power OK :** This signal is supplied from the power source of resume well. It is also used to reset the logic in resume power well. If there is no auxiliary power source on the system, this pin should be tied together with PWROK.
BATOK	1.8V	RTC	I	**Battery Power OK:** When the internal RTC is enabled, this signal is used to indicate that the power of RTC well is stable. It is also used to reset the logic in RTC well. If the internal RTC is disabled, this pin should be tied low.
OSC32KHI	1.8V	RTC	I	**RTC 32.768 KHz Input :** When internal RTC is enabled, this pin provides the 32.768 KHz clock signal from external crystal or oscillator.
OSC32KHO	<1.8V	RTC	O	**RTC 32.768 KHz Output :** When internal RTC is enabled, this pin should be connected the other end of the 32.768 KHz crystal or left unconnected if an oscillator is used.
PWROK	1.8V	RTC	I	**Main Power OK :** A high-level input to this signal indicates the power being supplied to the system is in stable operating state. During the period of PWROK being low, CPURST and PCIRST# will all be asserted until after PWROK goes to high for 24 ms.

4.12 AC'97 interface

Name	Tolerance	Power Plane	Type Attr	Description
AC_BIT_CLK	3.3V/5V	MAIN	I	**AC'97 Bit Clock :** This signal is a 12.288MHz serial data clock, which is generated by primary Codec.
AC_RESET#	3.3V	AUX	O	**AC'97 Reset :** Hardware reset signal for external Codecs.

AC_SDIN[1:0]	3.3V/5V	AUX	I	**AC' 97 Serial Data input :** Serial data input from primary Codec and secondary Codec.
AC_SDOUT	3.3V	MAIN	O	**AC' 97 Serial Data output :** Serial data output to Codecs.
AC_SYNC	3.3V	MAIN	O	**AC' 97 Syncronization :** This is a 48KHz signal, which is used to syncronize the Codecs.
SPDIF/ GPIO7	3.3V/5V	MAIN	O I/O/OD	**S/PDIF Transmitter Output** **General Purpose Input/Output 7 :** Refer to GPIO description.

4.13 Fast Ethernet and Home Networking interface

Name	Tolerance	Power Plane	Type Attr	Description
EECS/ GPIO6	3.3V	AUX	O/ I/O/OD	**Serial EEPROM Chip Select :** This enables the EEPROM during loading of the Ethernet configuration data. **General Purpose Input/Output 6 :** Refer to GPIO description.
EEDI/ GPIO4	3.3V	AUX	O I/O/OD	**Serial EEPROM Data Input :** During serial EEPROM access cycle, the SiS540 will use this pin to serially write OP codes, addresses and data into the serial EEPROM. **General Purpose Input/Output 4 :** Refer to GPIO description.
EEDO/ GPIO3	3.3V/5V	AUX	I I/O/OD	**Serial EEPROM Data Output :** During serial EEPROM access cycle, the SiS540 will read the contents of the EEPROM serially through this pin. *Requires external pull-up resistor**.** **General Purpose Input/Output 3 :** Refer to GPIO description.

EESK/ GPIO5	3.3V/5V	AUX	O I/O/OD	**Serial EEPROM Clock :** This pin provides the clock for the serial EEPROM. **General Purpose Input/Output 5 :** Refer to GPIO description.
OSC25MHI	3.3V	AUX	I	**PHY 25MHz Clock Input :** This pin is supplied the 25MHz clock signal input from the external crystal or an oscillator.
PLED#/ OC2#/ GPIO8	3.3V	AUX	OD I I/O/OD	**Programmable LED Output :** (A)Select 10/100Mbps LAN Mode: This pin is used as an ACTIVITY indication output. (B)Select Home Networking Mode: This pin is also an ACTIVITY indication output. **OC2# :** When this pin is configured as OC2#, it can detects USB Port 2 over current condition. **General Purpose Input/Output 8 :** Refer to GPIO description.
REXT		AUX	I	**Transmit Current Set :** An external resistor connected between this pin and GND will set the output current level for the twisted pair outputs.
TPIP		AUX	I	**Twisted Pair Receive Positive Input**
TPIN		AUX	I	**Twisted Pair Receive Negative Input**
TPOP		AUX	O	**Twisted Pair Transmit Positive Output**
TPON		AUX	O	**Twisted Pair Transmit Negative Output**
HRTXRXP		AUX	I/O	**Twisted Pair Transmit / Receive Positive Data**
HRTXRXN		AUX	I/O	**Twisted Pair Transmit / Receive Negative Data**

4.14 USB interface

Name	Tolerance	Power Plane	Type Attr	Description

CLK48M	3.3V/5V	MAIN	I	**USB 48 MHz clock input :** This signal provides the fundamental clock for the USB Controller.
OC0#/ PCIREQ3#/ GPIO0	3.3V/5V	MAIN	I I I/O/OD	**USB Port 0 Over Current Detection :** OC0# is used to detect the over current condition of USB Port 0. **External PCI Master Request 3:** PCIREQ3# is used for PCI Device on PCI Slot 3 to assert its request to hold PCI Bus. **General Purpose Input/Output 0 :** Refer to GPIO description.
OC1#/ PCIGNT3#/ GPIO1	3.3V/5V	MAIN	I O I/O/OD	**USB Port 1 Over Current Detection :** OC1# is used to detect the over current condition of USB Port 1. **External PCI Master Grant 3 :** PCIGNT3# is used to indicate PCI Device on PCI Slot 3 the PCI Bus has been granted. **General Purpose Input/Output 1 :** Refer to GPIO description.
LDRQ1#/ GPIO2	3.3V/5V	MAIN	I I/O/OD	**LPC DMA Request 1 :** LDRQ1# is the second LPC DMA request signal used by LPC Device to request DMA cycles. **General Purpose Input/Output 2 :** Refer to GPIO description.
UV[3:0]+	3.3V	AUX	I/O	**USB Port [3:0] Positive Input/Output**
UV[3:0]-	3.3V	AUX	I/O	**USB Port [3:0] Negative Input/Output**

4.15 Legacy I/O and Miscellaneous Signals

Name	Tolerance	Power plane	Type Attr	Description
SPK	3.3V	MAIN	O	**Speaker output :** The SPK is connected to the system speaker.

4.16 Power and Ground Signals

Name	Tolerance	Power plane	Type Attr	Description
VSS		GND		0V
IVDD		MAIN		1.8V
IVDD (AUX)		AUX		1.8V
OVDD (AUX)		AUX		3.3V
USBVDD		AUX		3.3V
RTCVDD		RTC		1.8V
DCLKAVDD		MAIN		3.3V
ECLKAVDD		MAIN		3.3V
RXAVDD		AUX		3.3V
TXAVDD		AUX		3.3V
DACAVDD		MAIN		3.3V
IDEAVDD		MAIN		1.8V
SDAVDD		MAIN		3.3V
CPUAVDD		MAIN		3.3V
VCC3		MAIN		3.3V

5 Hardware Trap

There are some pins used for trapping purpose to identify the hardware configurations at the power-up stage. These pins will be recognized as "1" if pull-up resistors are used; and will be recognized as "0" if pull-down resistors are used.

The following table is a summary of all the Hardware Trap pins in SiS540.

Name	Description
MD62	**PCI Clock PLL Enable** 0: Enable (Recommend) 1: Disable
MD61	**SDRAM Clock DLL Enable** 0: Enable (Recommend) 1: Disable
MD60	**CPU Clock DLL** 0: Enable (Recommend) 1: Disable
MD[59:58]	**SDRAM Clock DLL's Damping Resistor Control**
MD[57:56]	**CPU Clock DLL's Damping Resistor Control**
MD[55:54]	**PCI Clock PLL's Damping Resistor Control**
MD[52:50] (Internal Use Only)	**Selection for Internal Signals Probing** MD[52:50] Group 000 Core Arbiter 001 GUI Arbiter 010 PCC 011 SDRAM 100 VCSDRAM 101 HOST/PMR 110 PSL 111 Write FIFO
MD49 (Internal Use Only)	**Probing Signals Output Control** 0: Output internal signals 1: Output internal clock
MD48 (Internal Use Only)	**Probing Enable** 0: Disable 1: Enable

<table>
<tr><td>MD[44:41]</td><td>HD Clock Control
This field controls the phase of HD clock that ahead of CPUCLK.
Bit[3:0] Descriptions Bit[3:0] Descriptions
1111 -2.5ns 0111 +1.5ns
1110 -2.0ns 0110 +2.0ns
1101 -1.5ns 0101 +2.5ns (Recommend)
1100 -1.0ns 0100 +3.0ns
1011 -0.5ns 0011 +3.5ns
1010 +0.0ns 0010 +4.0ns
1001 +0.5ns 0001 +4.5ns
1000 +1.0ns 0000 +5.0ns</td></tr>
<tr><td>MD40</td><td>Reserved for Auto Reset Function</td></tr>
<tr><td>MD39</td><td>Reserved for VGA</td></tr>
<tr><td>MD38</td><td>VGA Interrupt Function Enable
0: Disable
1: Enable</td></tr>
<tr><td>MD37
(Internal Use Only)</td><td>External CLKGEN Enable
0: Disable
1: Enable</td></tr>
<tr><td>MD36</td><td>Panel Link Enable
0: Disable
1: Enable</td></tr>
<tr><td>MD[34:35]</td><td>Reserved</td></tr>
<tr><td>MD33</td><td>Video Bridge Enable
0: Disable
1: Enable</td></tr>
<tr><td>MD32</td><td>PAL/NTSC Select
0: Select NTSC system
1: Select PAL system</td></tr>
</table>

Note:

1. There are internal pull-down resistors on MD lines.
2. Function description for MD33 and MD36.

MD36	MD33	Function
0	0	Frame Buffer Cache
0	1	Enable SiS301 Video Bridge
1	0	The 3rd Party Panel Link Chip is used
1	1	The 3rd Party TV Encoder is used

6 Function Description

6.1 MA mapping table

6.1.1 SDRAM/System Memory

SDRAM (NBAXNRAXNCA)																	
TYPE		**1X11X8**	**1X13X8**	**2X12X8**	**2X13X8**	**1X11X9**	**1X13X9**	**2X12X9**	**2X13X9**	**1X11X10**	**1X13X10**	**2X12X10**	**2X13X10**	**2X11X8**	**1X13X11**	**2X12X11**	**2X13X11**
DIMM	SDM chip	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA
MA0	MA0	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
MA1	MA1	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
MA2	MA2	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
MA3	MA3	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6
MA4	MA4	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
MA5	MA5	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
MA6	MA6	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9
MA7	MA7	10@	10@	10@	10@	10@	10@	10@	10@	10@	10@	10@	10@	10@	10@	10@	10@
MA8	MA8					23#/23	23	23	23	23	23	23	23		23	23	23
MA9	MA9									24#/24	24	24	24		24	24	24
MA10	AP	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]
MA11	BA0	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11
MA12	BA1	[0]	[0]	12	12	[0]	[0]	12	12	[0]	[0]	12	12	12	[0]	12	12
MA13	MA11														27#/27	27#/27	27
MA14	MA12																
SIDE-MA (SINGLE/ DOUBLE)		[0]/12	[0]/12	[0]/13	[0]/13	[0] /12	[0]/ 12	[0]/13	[0]/13	[0]/12	[0]/12	[0]/13	[0]/ 13	[0]/13	[0]/12	[0]/13	[0]/13

DIMM	**SDM chip**	**RA**	**RA**	**RA**	**RA**	**RA**	**RA**	**RA**	**RA**	**RA**	**RA**	**RA**	**RA**	**RA**	**RA**	**RA**	**RA**
MA0	MA0	13	13	13/25#	13/26#	13	13	13/26#	13/27#	13	13	13/27#	13/ 28#	13/ 24#	13	13/ 28#	13/ 29#
MA1	MA1	14	14	14	14	14	14	14	14	14	14	14	14	14	14	14	14
MA2	MA2	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15
MA3	MA3	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
MA4	MA4	17	17	17	17	17	17	17	17	17	17	17	17	17	17	17	17
MA5	MA5	18	18	18	18	18	18	18	18	18	18	18	18	18	18	18	18

MA6	MA6	19	19	19	19	19	19	19	19	19	19	19	19	19	19	19	19
MA7	MA7	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
MA8	MA8	21	21	21	21	21	21	21	21	21	21	21	21	21	21	21	21
MA9	MA9	22#/22	22	22	22	22	22	22	22	22	22	22	22	22	22	22	22
MA10	AP	12/23#	12/25#	23	23	12/24#	12/26#	25#/25	25	12/25#	12/27#	25	27#/27	23#/23	12/28#	25	25
MA11	BA0	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11
MA12	BA1	[0]	[0]	12	12	[0]	[0]	12	12	[0]	[0]	12	12	12	[0]	12	12
MA13	MA11		24#/ 24	24#/ 24	24		24	24	26#/ 26		26#/ 26	26#/ 27	26		26	26	26
MA14	MA12		23		25#/ 25		25#/ 25		24		25		25		25		28#/ 28
Rank Size		8MB	32MB	32MB	64MB	16MB	64MB	64MB	128MB	32MB	128MB	128MB	256MB	16MB	256MB	256MB	512MB
System Reg.		{0000}	{0001}	{0010}	{0011}	{0100}	{0101}	{0110}	{0111}	{1000}	{1001}	{1010}	{1011}	{1100}	{1101}	{1110}	{1111}

Note: 1.@ for page hit comparator, #for rank decoder.

1. Constant Page Size: 2K byte (4Kbyte for GUI-128 BITs ACCESS)
2. A1,2:A1 for single sided DIMM, A2 for double-sided DIMM.

6.1.2 SDRAM/FBC

SDRAM		**(N**BA**XN**RA**XN**CA**)**							
TYPE		*1x9x8*	*1x10x8*	*1X11X8*	*2X12X8*	1X11X9	1X11X10	2X11X8	*1X12X8*
DIMM	SDM chip	CA	CA	CA	CA	CA	CA	CA	CA
MA0	MA0	3	3	3	3	3	3	3	3
MA1	MA1	4	4	4	4	4	4	4	4
MA2	MA2	5	5	5	5	5	5	5	5
MA3	MA3	6	6	6	6	6	6	6	6
MA4	MA4	7	7	7	7	7	7	7	7
MA5	MA5	8	8	8	8	8	8	8	8
MA6	MA6	9	9	9	9	9	9	9	9
MA7	MA7	10@	10@	10@	10@	10@	10@	10@	10@
MA8	MA8					23#	23		
MA9	MA9						24#		
MA10	AP	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]
MA11	BA0	11	11	11	11	11	11	11	11
MA12	BA1	[0]	[0]	[0]	12	[0]	[0]	12	[0]
MA13	MA11								
MA14	MA12								

DIMM	SDM chip	RA	RA	RA	RA	RA	RA	RA	RA
MA0	MA0	13	13	13	13	13	13	13	13
MA1	MA1	14	14	14	14	14	14	14	14
MA2	MA2	15	15	15	15	15	15	15	15
MA3	MA3	16	16	16	16	16	16	16	16
MA4	MA4	17	17	17	17	17	17	17	17
MA5	MA5	18	18	18	18	18	18	18	18
MA6	MA6	19	19	19	19	19	19	19	19
MA7	MA7	20#	20	20	20	20	20	20	20
MA8	MA8		21#	21	21	21	21	21	21
MA9	MA9			22#	22	22	22	22	22
MA10	AP	12	12	12	23	12	12	23#	12
MA11	BA0	11	11	11	11	11	11	11	11
MA12	BA1	[0]	[0]	[0]	12	[0]	[0]	12	[0]
MA13	MA11				24#				23#
MA14	MA12								
Rank Size		2MB	4MB	8MB	32MB	16MB	32MB	16MB	16MB
System Reg.		{0000}	{0001}	{0010}	{0011}	{0100}	{0101}	{0110}	{0111}

Note: 1. Additional Configurations:1x9x8, 1x10x8, 1x12x8, and the other configurations are the same as system configurations.

2.Additional PinS for 128-bit solution are “GUI_AP”,”GUI_BA1”,”GUI_MA11”

6.1.3 VCM/System Memory

VC SDRAM TYPE	(N**BA**XN**RA**XN**CA**XN**SA**)		
	1X13X6X2	**1X13X7X2**	**1X13X8X2**
	CA	CA	CA
MA0	**3**	**3**	**3**
MA1	**4**	**4**	**4**
MA2	**5**	**5**	**5**
MA3	**6**	**6**	**6**
MA4	**7**	**7**	**7**
MA5	**8@**	**8**	**8**
MA6	(9)*	**9@**	**9**
MA7	(10)*	(10)*	**10@**
MA8(CH0)			
MA9(CH1)			

MA10/AP	[0]	[0]	[0]
MA11/BA0(BA)	[0]	[0]	[0]
MA12/BA1	[0]	[0]	[0]
MA13/MA11(CH2)			
MA14/MA12(CH3)			

	SA	SA	SA
MA0(SEG0)	**11**	**11**	**11**
MA1(SEG1)	**12**	**12**	**12**
MA2			
MA3			
MA4			
MA5			
MA6			
MA7			
MA8(CH0)			
MA9(CH1)			
MA10/AP	[1]	[1]	[1]
MA11/BA0(BA)	**13**	**13**	**13**
MA12/BA1			
MA13/MA11(CH2)			
MA14/MA12(CH3)			

MA-CS	[0] /14	[0] /14	[0]/14

	RA	RA	RA
MA0	**15**	**15**	**15**
MA1	**16**	**16**	**16**
MA2	**17**	**17**	**17**
MA3	**18**	**18**	**18**
MA4	**19**	**19**	**19**
MA5	**20**	**20**	**20**
MA6	**21**	**21**	**21**
MA7	**22**	**22**	**22**
MA8	**23**	**23**	**23**
MA9	**24**	**24**	**24**
MA10/AP	**9**	**25**	**25**

MA11/BA0	**13**	**13**	**13**
MA12/BA1			
MA13/MA11	**14 / 25**	**14 / 26**	**14 / 27**
MA14/MA12	**10**	**10**	**26**
Rank/DIMM Size	32MB	64MB	128MB
System Reg.	{0000}	{0001}	{0010}

Note: 1. @ for boundary page hit comparator, #for rank decoder.
Page Size is programmable (0.5k, 1k, 2k), and constant for all VC-SDRAM rank.
2 .A1/A2: A1 for single sided DIMM or 128-bit mode, A2 for double-sided & 64-bit mode.

6.1.4 VCM/FBC

VC SDRAM	
TYPE	**1X13X6X2**
	CA
MA0	**3**
MA1	**4**
MA2	**5**
MA3	**6**
MA4	**7**
MA5	**8**
MA6	(9)*
MA7	(10)*
MA8(CH0)	
MA9(CH1)	
MA10/AP	[0]
MA11/BA0(BA)	[0]
MA12/BA1	[0]
MA13/MA11(CH2)	
MA14/MA12(CH3)	

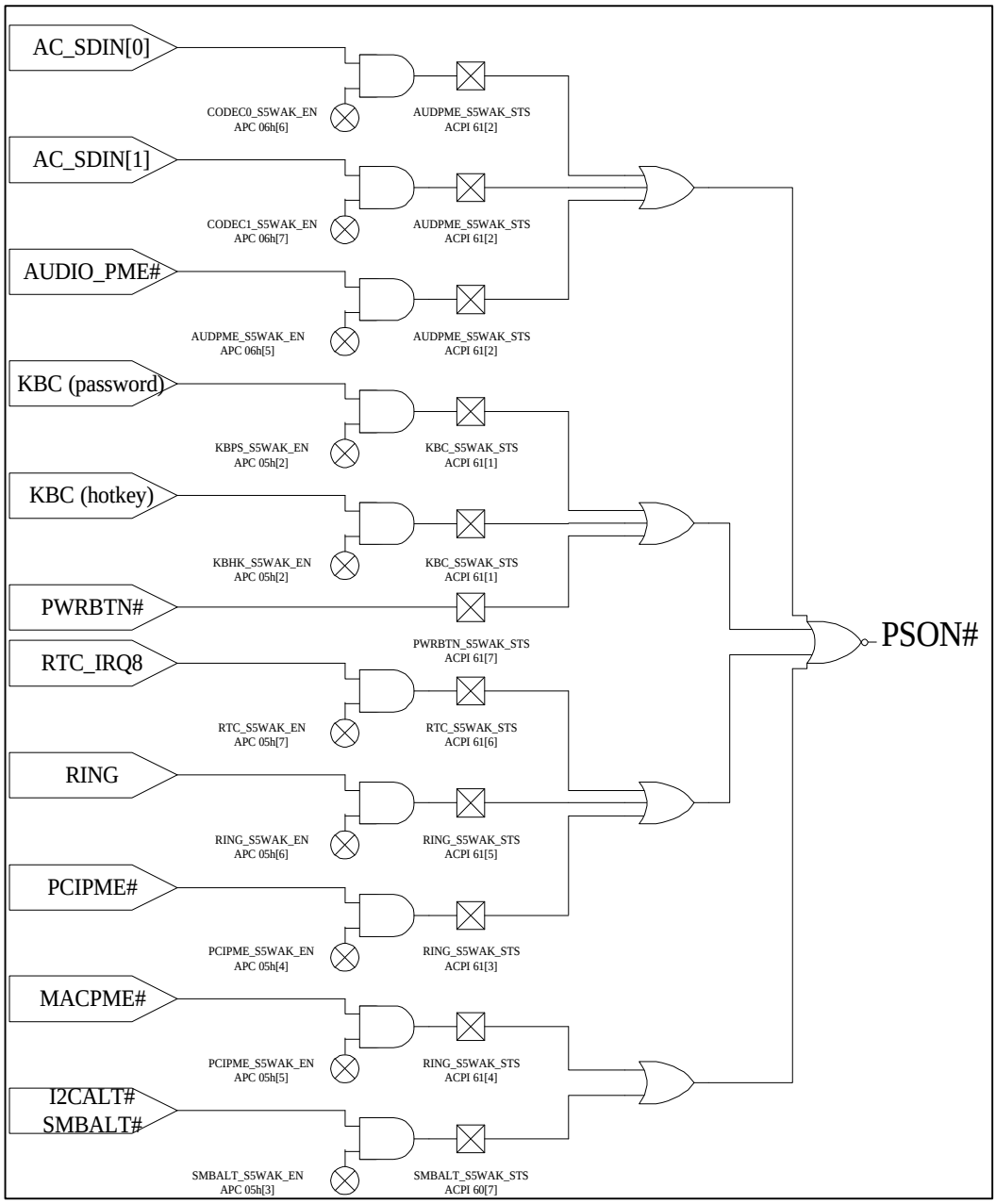
	SA
MA0(SEG0)	**11**
MA1(SEG1)	**12**
MA2	
MA3	
MA4	
MA5	
MA6	
MA7	
MA8(CH0)	
MA9(CH1)	
MA10/AP	[1]
MA11/BA0(BA)	**13**
MA12/BA1	
MA13/MA11(CH2)	
MA14/MA12(CH3)	
MA14/MA12(CH3)	

	RA
MA0	**15**
MA1	**16**
MA2	**17**
MA3	**18**
MA4	**19**
MA5	**20**
MA6	**21**
MA7	**22**
MA8	**23**
MA9	**24**
MA10/AP	**9**
MA11/BA0	**13**
MA12/BA1	
MA13/MA11	**14**
MA14/MA12	**10**

GUI Size: 32MB

GUI Reg. {0000}

6.2 PSON# and ACPILED Description:



Pin Name	Buffer Type	Description
PSON#	Auxiliary / Open Drain	PS_ON# is an active low signal that turns on all of the main power rails. When a power-up event occurs, SiS540 would assert PSON# to turn on the power supply. When a power-down event occurs, SiS540 would deassert PSON# to turnoff the power supply. This signal should be held at +5VDC by a pullup resistor internal to the power supply.

Pin Name	Buffer Type	Description
ACPILED	Auxiliary/ Open Drain	ACPILED is used to denote that the computer is in the sleep mode.

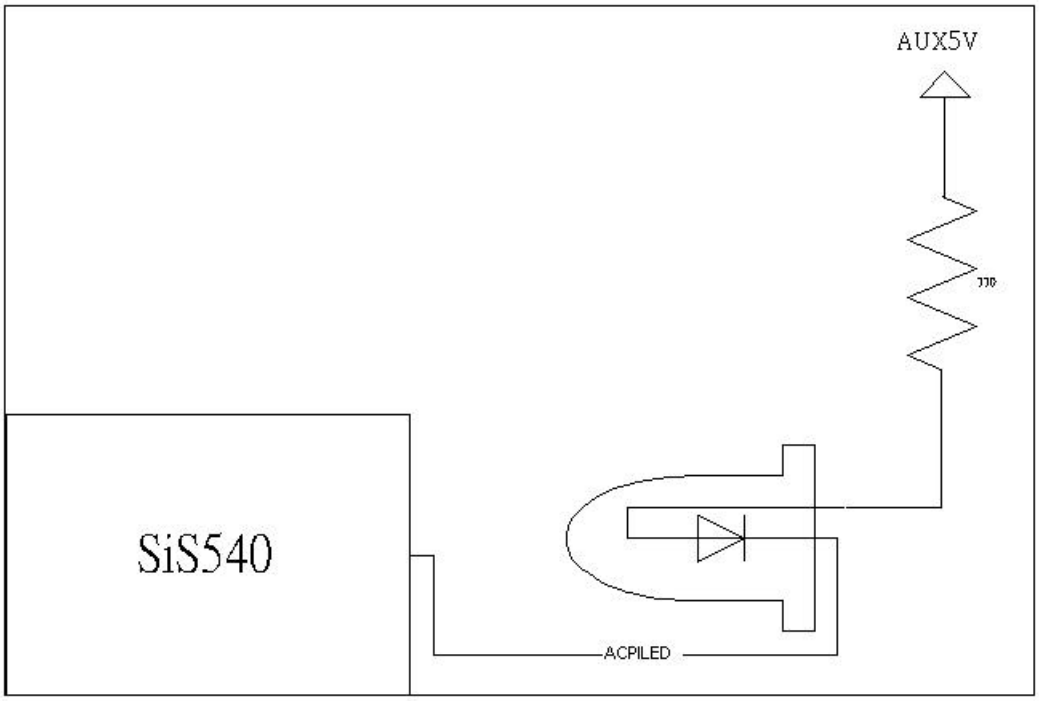
6.3 ACPILED Control

Register 62h~63h System Wakeup form S3/S4/S5 Control Register (S5WAK_CNT)

Default Value: 0000h

Access: Read/Write

7:6	RO	**ACPILED Output State Control** The output state of ACPILED can be controlled by the following combination when system is in S0/S1/S2/S3 states. If the system is in S4/S5 state, ACPILED will be set to high impedance. 00 : Output low 01 : Blink 10 : High impedance 11 : Reversed



6.4 Power States for 540 Signals

Term	Pin Type	Description
In	INPUT	When PCIRST# is asserted, the I/O pin would be set to input mode.
Fixed	INPUT	Can't be changed.
Driven	INPUT	The pin is driven by external resistors. The logic value is allowed to be changed.
--	INPUT	The logic value of the input pin is independent of PCIRST#.
Running	INPUT/OUTPUT	Clocks.
High	INPUT/OUTPUT	SiS540 drives the pin to a logic high level, or the pin is driven to a high logic level by external components.
Low	INPUT/OUTPUT	SiS540 drives the pin to a logic low level, or the pin is driven to a low logic level by external components..
Defined	OUTPUT	SiS540 drives the pin to a logic level, that depends on the function.
Off	OUTPUT	The output buffer is powered off.

High-Z	OUTPUT	The output buffer is high impedance.

Signal Name	Buffer Type	Power Plane	During PCIRST#	After PCIRST#	S1	S3	S4/S5
PCI Interface							
PCICLK	I	Core	Running	Running	Running	Low	Low
SERR#	I	Core	--	--	High	Low	Low
INT[A:D]#	I	Core	--	--	Driven	Low	Low
AD[31:0]	I/O	Core	High-Z	High	High-Z	Off	Off
C/BE[3:0]#	I/O	Core	High-Z	High	High-Z	Off	Off
FRAME#	I/O	Core	High-Z	High-Z	High-Z	Off	Off
IRDY#	I/O	Core	High-Z	High-Z	High-Z	Off	Off
TRDY#	I/O	Core	High-Z	High-Z	High-Z	Off	Off
DEVSEL#	I/O	Core	High-Z	High-Z	High-Z	Off	Off
STOP#	I/O	Core	High-Z	High-Z	High-Z	Off	Off
PAR	I/O	Core	High-Z	Low	Low	Off	Off
PCIRST#	O	Resume	Low	High	High	Low	Low
CPU Interface							
CPURST	OD	Core	Low	Keep Low 10ns	High	Off	Off
INIT#	OD	Core	High-Z	High-Z	High-Z	Off	Off
A20M#	OD	Core	Defined	High-Z	High-Z	Off	Off
SMI#	OD	Core	High-Z	High-Z	High-Z	Off	Off
STPCLK#	OD	Core	High-Z	High-Z	Low	Off	Off
CPUSLP#	OD	Core	High-Z	High-Z	High-Z	Off	Off
INTR	OD	Core	Defined	Low	Low	Off	Off
NMI	OD	Core	Defined	Low	Low	Off	Off
IGNE#	OD	Core	Defined	High-Z	High-Z	Off	Off
FERR#	I	Core	--	--	High	Off	Off
ACPI							
PWRBTN#	I	Resume	Driven	Driven	Driven	Driven	Driven
EXTSMI#/ THERM#	I	Core	Driven	Driven	Driven	Low	Low
RING	I	Resume	Driven	Driven	Driven	Driven	Driven
PME#	I	Resume	Driven	Driven	Driven	Driven	Driven
PSON#	OD	Resume	Low	Low	Low	High	High

CKE	O	Resume	High-Z	High-Z	High-Z	Low	High-Z
ACPILED	OD	Resume	High-Z	High-Z	High-Z	Defined	High-Z
SM Bus							
SMBDAT	I/OD	Core	High-Z	High-Z	High-Z	Off	Off
SMBCLK	I/OD	Core	High-Z	High-Z	High-Z	Off	Off
LPC Interface							
LAD[3:0]	I/O	Core	High	High	High	Off	Off
LFRAME#	O	Core	High	High	High	Off	Off
LDRQ#	I	Core	--	--	High	Low	Low
SIRQ	I/O	Core	High-Z	High-Z	High-Z	Off	Off
RTC							
OSC32KHI	I	RTC	Running	Running	Running	Running	Running
OSC32KHO	O	RTC	Running	Running	Running	Running	Running
PWROK	I	RTC	High	High	High	Low	Low
AUXOK	I	RTC	High	High	High	High	High
BATOK	I	RTC	High	High	High	High	High
Audio Modem Interface							
AC_RESET#	O	Resume	Low	Low	Defined	Low	Low
AC_SYNC	O	Core	Low	Low	Low	Off	Off
AC_CLK	I	Core	--	--	Low	Low	Low
AC_SDOUT	O	Core	Low	Low	Low	Off	Off
AC_SDIN[1:0]	I	Resume	Driven	Driven	Driven	Driven	Driven
PHY Interface							
OSC25MHI CLK25M	I I	Resume	Running	Running	Running	Running	Running
HRTXRXP	I/O	Resume	High-Z	High-Z	High-Z	High-Z	High-Z
HRTXRXN	I/O	Resume	High-Z	High-Z	High-Z	High-Z	High-Z
REXT	I	Resume	High	High	High	High	High
TPO+	O	Resume	Defined	Defined	Defined	Defined	Defined
TPO-	O	Resume	Defined	Defined	Defined	Defined	Defined
TPI+	I	Resume	Driven	Driven	Driven	Driven	Driven
TPI-	I	Resume	Driven	Driven	Driven	Driven	Driven
USB Interface							
UV[0,1,2,3]+	I/O	Resume	High-Z	High-Z	High-Z	High-Z	High-Z
UV[0,1,2,3]-	I/O	Resume	High-Z	High-Z	High-Z	High-Z	High-Z
CLK48M	I	Core	Running	Running	Running	Low	Low

Legacy I/O							
SPK	O	Core	Low	Low	Low	Off	Off
CLK14M	I	Core	Running	Running	Running	Off	Off
GPIO							
GPIO0/ PCIREQ3#/ OC0#	I/O/OD I I	Core	In -- High	In -- High	Defined High High	Off Off Off	Off Off Off
GPIO1/ PCIGNT3#/ OC1#	I/O/OD O I	Core	In High High	In High High	Defined High High	Off Off Off	Off Off Off
GPIO2/OC2# /LDRQ1#	I/O/OD I	Core	In High	In High	Defined High	Off Low	Off Low
GPIO3/ EEDO	I/O/OD I	Resume	In --	In --	Defined Driven	Off Driven	Off Driven
GPIO4/ EEDI	I/O/OD O	Resume	In Low	In Low	Defined Low	Off Low	Off Low
GPIO5/ EESK	I/O/OD O	Resume	In Low	In Low	Defined Low	Off Low	Off Low
GPIO6/ EECS	I/O/OD O	Resume	In Low	In Low	Defined Low	Off Low	Off Low
GPIO7/ SPDIF	I/O/OD O	Core	In Low	In Low	Defined Low	Off Off	Off Off
GPIO8/ PLED	I/O/OD OD I	Resume	In Defined High	In Defined High	Defined Defined High	Off Defined High	Off Defined High
GPIO10/ KBDAT	I/O/OD I/OD	Resume	In Driven	In Driven	Defined Driven	Off High-Z	Off High-Z
GPIO11/ KBCLK	I/O/OD I/OD	Resume	In Driven	In Driven	Defined Driven	Off High-z	Off High-Z
GPIO12/ PMDAT	I/O/OD I/OD	Resume	In Driven	In Driven	Defined Driven	Off High-Z	Off High-Z
GPIO13/ PMCLK	I/O/OD I/OD	Resume	In Driven	In Driven	Defined Driven	Off High-Z	Off High-Z
GPIO15/ SMBALT#/ I^2CALT#	I/O/OD I I	Resume	In High High	In High High	Defined High High	Off High High	Off High High

6.5 Power Sequence in SiS540

If the system doesn't support AUXVDD, AUXOK must be connected with PWROK. There is no well-defined sequence for RTCVDD, AUXVDD, and VDD. Note that AUXOK and PWROK signal pins are powered by RTCVDD. These two pins must have their own pull-down resistors to prevent them from floating if AUXVDD or VDD is not presented.

In SiS540, BATOK is used to reset some power management registers in RTC power plane. If it goes low, all registers in RTC power plane will be reset. By the time of next booting up, the BIOS will shows "CMOS Checksum Fail" to indicate that the RTCVDD had been absent.

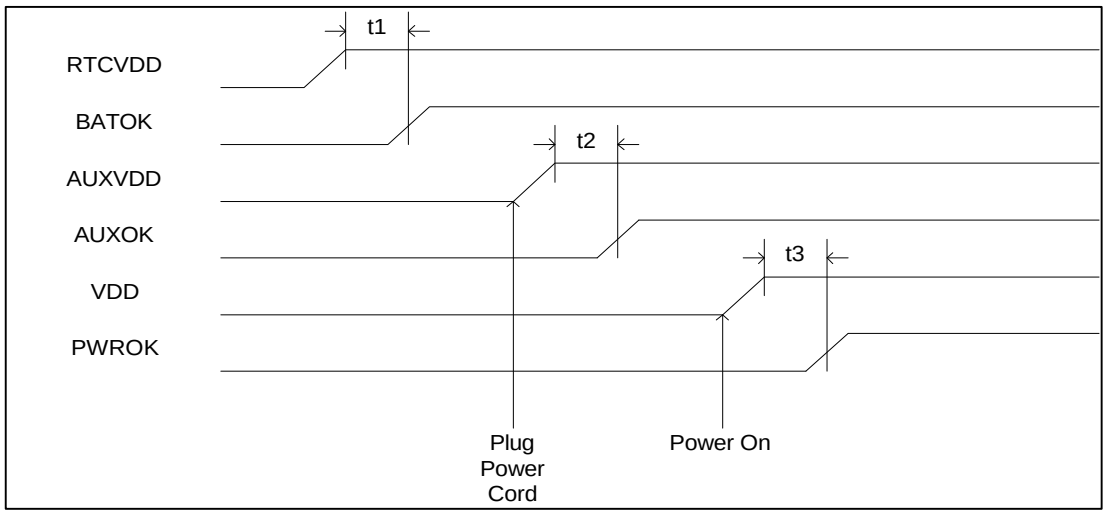
AUXOK is used to reset the power management registers in AUX power plane. If AUXOK goes low for some reason, the registers in AUX power plane will be reset to their default state. If the system is in power-off state, only PWRBTN# can power up the system under this circumstance. If the system is ON and AUXOK go low for some strange reason, the power will be shutdown immediately.

Finally, PWROK is use to generate CPURST# and PCIRST#. If this signal is de-asserted, PCIRST# and CPURST# will be asserted and the system will be reset by these two reset signal. Note that CPURST# and PCIRST# won't reset the registers which locate in RTC and AUX power planes.

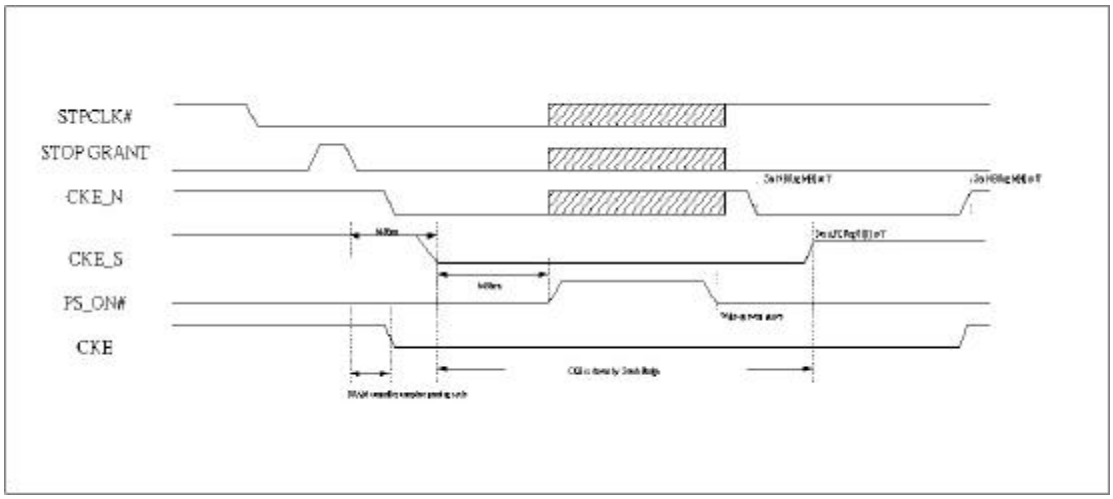
T1 > 1ms

T2 > 10ms

T3 > 100ms



6.6 S3 Timing Table



6.7 Multi-function Pins Relational Data Table

BALL NO	NAME	MUX	DEFAULT FUNCTION	CONTROLLED BY
D6	EECS	GPIO6	GPIO6	APC_R02B1
B3	EEDI	GPIO4	GPIO4	APC_R02B1
C4	EEDO	GPIO3	GPIO3	APC_R02B0
A3	EESK	GPIO5	GPIO5	APC_R02B1
K1	EXTSMI#	THERM#	EXTSMI#	APC_R01B3
M6	GPIO0	PREQ3#/OC0#	GPIO0	APC_R03B[5:4]
L3	GPIO1	PGNT3#/OC1#	GPIO1	APC_R03B[5:4]
M5	GPIO2	LDRQ1#/OC2#	GPIO2	APC_R03B[7:6]
L2	GPIO7	SPDIF	GPIO7	APC_R02B2
D3	KBCLK	GPIO11	GPIO11	APC_R02B[6:5]
D2	KBDAT	GPIO10	GPIO10	APC_R02B[6:5]
D5	PLED#	GPIO8	GPIO8	APC_R02B[4:3]
C1	PMCLK	GPIO13	GPIO13	APC_R02B[6:5]
D4	PMDAT	GPIO12	GPIO12	APC_R02B[6:5]
E3	PME#	DCLK_EXT	PME#	H/W MD37

E4	SMBALT#	GPIO15	GPIO15	APC_R02B7
W4	VBA1	VBCLK	VBCLK	H/W MD36&MD33
AA4	VDQM0	CSB4#	VDQM0	Host_R64B7&4
AA3	VDQM1	CSA4#	VDQM1	Host_R64B7&4
AA2	VDQM2	CSB5#	VDQM2	Host_R64B7&4
V6	VDQM3	CSA5#	VDQM3	Host_R64B7&4
W2	VMA10	VBHCLK	VMA10	H/W MD36&MD33
W3	VMA11	VGCLK	VMA11	H/W MD36&MD33
Y3	VMD28	DDC2DATA	VMD28	H/W MD36&MD33
Y2	VMD29	DDC2CLK	VMD29	H/W MD36&MD33
Y1	VMD30	VBVSYNC	VMD30	H/W MD36&MD33
U5	VMD31	VBHSYNC	VMD31	H/W MD36&MD33
T6	VMD32	VBCAD	VMD32	H/W MD36&MD33
W1	VMD33	TVCTL1	VMD33	H/W MD36&MD33
V4	VMD34	TVCTL0	VMD34	H/W MD36&MD33
V3	VMD35	VBBLANKN	VMD35	H/W MD36&MD33
V2	VMD36	VBRGB15	VMD36	H/W MD36&MD33
V1	VMD37	VBRGB14	VMD37	H/W MD36&MD33
U4	VMD38	VBRGB12	VMD38	H/W MD36&MD33
U3	VMD39	VBRGB13	VMD39	H/W MD36&MD33
T5	VMD40	VBRGB8	VMD40	H/W MD36&MD33
U2	VMD41	VBRGB9	VMD41	H/W MD36&MD33
U1	VMD42	VBRGB11	VMD42	H/W MD36&MD33
T4	VMD43	VBRGB10	VMD43	H/W MD36&MD33
R5	VMD44	VBRGB23	VMD44	H/W MD36&MD33
T3	VMD45	VBRGB22	VMD45	H/W MD36&MD33
T2	VMD46	VBRGB21	VMD46	H/W MD36&MD33
T1	VMD47	VBRGB20	VMD47	H/W MD36&MD33
R6	VMD48	VBRGB19	VMD48	H/W MD36&MD33
R1	VMD49	VBRGB16	VMD49	H/W MD36&MD33
R2	VMD50	VBRGB17	VMD50	H/W MD36&MD33

R3	VMD51	VBRGB18	VMD51	H/W MD36&MD33
R4	VMD52	VBRGB0	VMD52	H/W MD36&MD33
P1	VMD53	VBRGB1	VMD53	H/W MD36&MD33
P5	VMD54	VBRGB2	VMD54	H/W MD36&MD33
P2	VMD55	VBRGB3	VMD55	H/W MD36&MD33
N3	VMD56	VBRGB4	VMD56	H/W MD36&MD33
N4	VMD57	VBRGB5	VMD57	H/W MD36&MD33
M1	VMD58	VBRGB6	VMD58	H/W MD36&MD33
N5	VMD59	VBRGB7	VMD59	H/W MD36&MD33

6.8 Ball Connectivity Testing

SiS Chip will provide a NAND chain Test Mode by TEST# signal is pull low. In order to ensure the connections of balls to tracks of main board, SiS Chip provides a simple way to do connective measurements. Basically, an additional 2-input-NAND gate is added into the I/O buffer cells. And, one of inputs of NAND gate is connected to input pin of I/O buffer as test input port in test mode. To monitor the test result at test output port, the output of the NAND gate is connected to the other input of the next NAND gate. Such that, the test result could be propagated and it forms a NAND tree, as depicted in Figure 6.8-1. To adapt to the scheme, all output buffers of SiS Chip are changed to bi-direction buffers to accept test signals.

6.8.1 Test Scheme

There is one NAND tree chains is provided by SiS Chip. Each NAND tree chain has several test-input pins and one output pin.

The following description is an example on 4-test-input pins to explain a NAND tree chain test scheme.

First of all, logic LOW is driven into TESTIN1 pin from track on main board. If logic HIGH could be observed at TESTOUT pin, it means that the connection of TESTIN1 pin to track is good, as shown in Figure 6.8-2. To test TESTIN2 pin, TESTIN2 pin should be driven LOW also. And, TESTIN1 pin should be kept at logic HIGH, such that the test result could be passed to TESTOUT pin and so on. Although SiS Chip operates at 3.3V, all input buffers of SiS Chip are 5V-input tolerance. Hence, all test signals could go up to 5V.

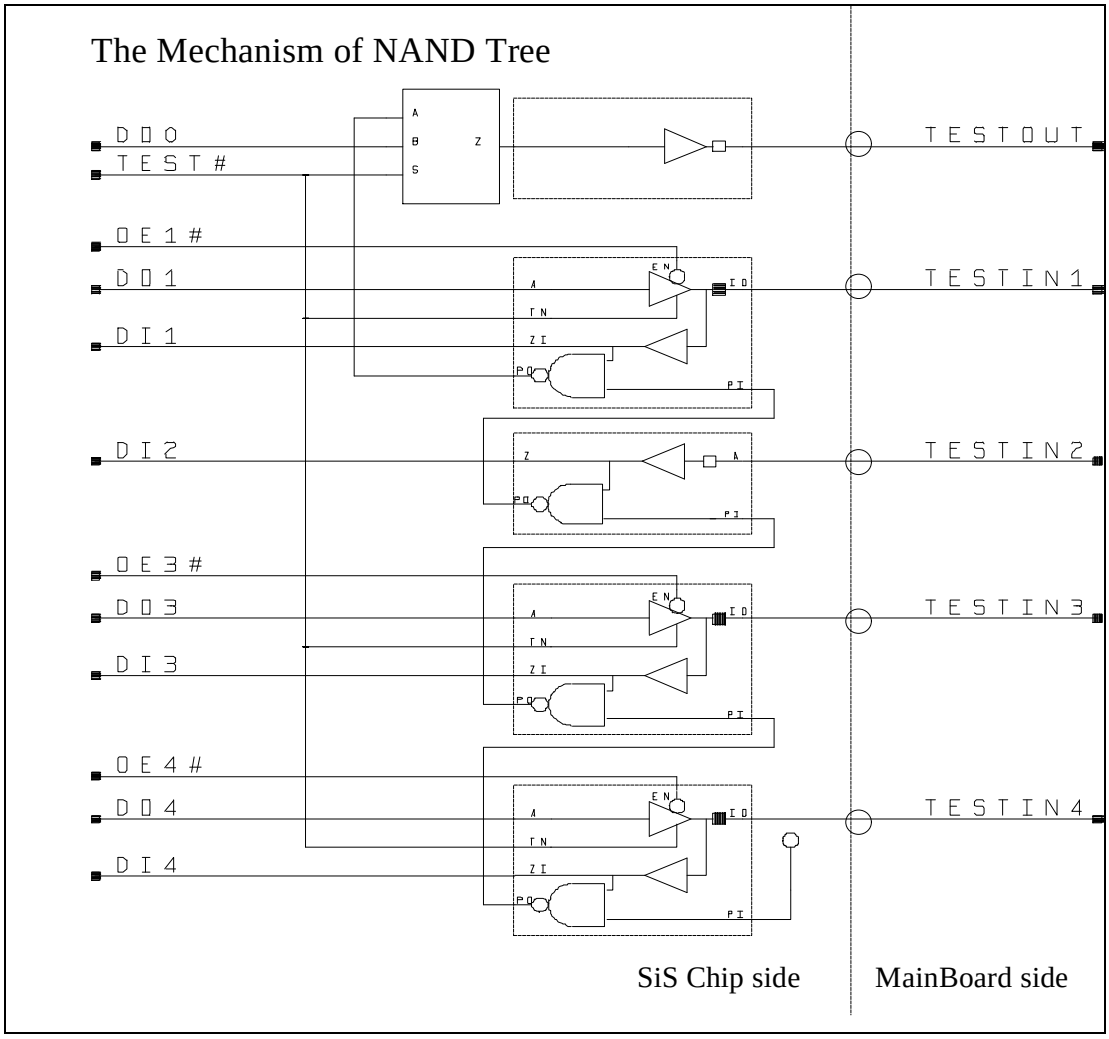


Figure 6.8-1 The Mechanism of NAND Tree

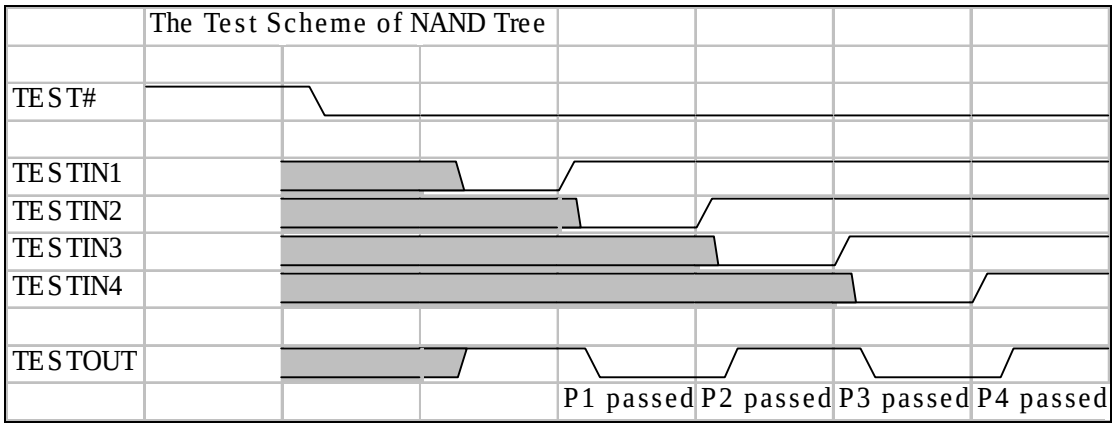


Figure 6.8-2 The Test Scheme of NAND Tree

6.8.2 Measurements

During test process, this scheme requires all test inputs to be driven simultaneously. To decrease the amount of test probes, SiS Chip divides pins into one branch. Meanwhile, some noise sensitive signals or analogue signals, i.e. RTC, and power signals, are excluded.

Table 6.8-1 NAND Tree List for SiS540

TEST VECTORS	TEST INPUT BALL NAME LIST	TEST OUTPUT BALL NAME
NAND Tree	PLED0#, EECS, PCIRST#, EEDO, EESK, EEDI, AC_RESET#, AC_SDIN0, AC_SDIN1, PMCLK, PMDAT, KBCLK, KBDAT, ACPILED, PSON#, SMBALT#, PME#, RING, PWRBTN#, CKE, UV3-, UV3+, UV2-, UV2+, UV1-, UV1+, UV0-, UV0+, INTA#, INTB#, INTC#, INTD#, SERR#, SMCLK, CLK48M, SMBDAT, AC_SDOUT, AC_SYNC, AC_BIT_CLK, GPIO0, GPIO1, GPIO2, GPIO7, VMD63, VMD62, VMD61, VMD60, VMD59, VMD58, VMD57, VMD56, VCS#, VDQM7, VDQM6, VDQM5, VDQM4, VMD55, VMD54, VMD53, VMD52, VMD51, VMD50, VMD49, VMD48, VMD47, VMD46, VMD45, VMD44, VMD43, VMD42, VMD41, VMD40, VMD39, VMD38, VMD37, VMD36, VMD35, VMD34, VMD33, VMD32, VMA10, VMA11, VBA1, VMD31, VMD30, VMD29, VMD28, VMD27, VMD26, VMD25, VMD24, VDQM3, VDQM2, VDQM1, VDQM0, VMD23,	EXTSMI#

	VMD22, VMD21, VMD20, VMD19, VMD18, VMD17, VMD16, VMD15, VMD14, VMD13, VMD12, VMD11, VMD10, VMD9, VMD8, VMD7, VMD6, VMD5, VMD4, VMD3, VMD2, VMD1, VMD0, SSYNC, OSCI, VSYNC, HSYNC, DDCCLK, DDCDATA, SPK, LAD3, LAD2, LAD1, LAD0, LFRAME#, LDRQ#, SIRQ, IDA7, IDA8, IDA6, IDA9, IDA5, IDA10, IDA4, IDA11, IDA3, IDA12, IDA2, IDA13, IDA1, IDA14, IDA0, IDA15, IIOWA#, IDREQA, ICHRDYA, IIORA#, IDACKA#, IIRQA, IDSAA1, IDSAA0, IDSAA2, CBLIDA, IDECSA0#, IDECSA1#, IDB7, IDB8, IDB6, IDB9, IDB5, IDB10, IDB4, IDB11, IDB3, IDB12, IDB2, IDB13, IDB1, IDB14, IDB0, IDB15, IIOWB#, IDREQB, IIORB#, ICHRDYB, IDACKB#, IDSAB1, IDSAB0, IDSAB2, IDECSB0#, IDECSB1#, IIRQB, CBLIDB, PCICLK, SDCLK, MD32, MD0, MD33, MD1, MD34, MD2, MD35, MD3, MD36, MD4, MD37, MD5, MD38, MD6, MD39, MD7, MD40, MD8, MD41, MD9, MD42, MD10, MD43, MD11, MD44, MD12, MD45, MD13, MD46, MD14, MD47, MD15, SCAS#, WE#, DQM4, DQM0, DQM5, DQM1, SRAS#, CSA3#, CSA2#, CSA1#, CSA0#, MA0, MA1, MA2, MA3, MA4, MA5, MA6, MA7, MA8, MA9, MA10, MA11, MA12, MA13, MA14, CSB3#, CSB2#, CSB1#, CSB0#, DQM6, DQM2, DQM7, DQM3, MD48, MD16, MD49, MD17, MD50, MD18, MD51, MD19, MD52, MD20, MD53, MD21, MD54, MD22, MD55,MD23, MD56, MD24, MD57, MD25, MD58, MD26, MD59, MD27, MD60, MD28, MD61, MD29, MD62, MD30, MD63, MD31, TAGWE#, TA7, TA6, TA5,TA4, TA3, TA2, TA1, TA0, CCS1#, GWE#, BWE#, ADV#, ADSC#, KOE#, HA30, HA6, HA4, HA29, HA3, HA28, HA22, HA24, HA26, HA21, HA27, HA23, HA25, HA31, HA7, HA8, HA5, HA10, HA11, HA9, HA12, HA13, HA15, HA14, HA16, HA17, HA18, HA19, HA20, HBE7#, HBE6#, HBE5#, HBE4#, HBE3#, HBE2#, HBE1#, HBE0#, EADS#, NA#, W/R#, CPUCLK, HITM#, ADS#, HLOCK#, D/C#, BOFF#, BRDY#, AHOLD, KEN#/INV, CACHE#, M/IO#, SMIACT#, HD63, HD62, HD61, HD60, HD59, HD58, HD57, HD56, HD55, HD54, HD53, HD51, HD52, HD50, HD49,	

	HD48, HD47, HD43, HD41, HD45, HD44, HD46, HD40, HD42, HD38, HD36, HD39, HD37, HD34, HD35, HD32, HD33, HD31, HD29, HD30, HD27, HD28, HD25, HD26, HD23, HD24, HD19, HD21, HD20, HD22, HD17, HD16, HD18, HD15, HD13, HD14, HD12, HD11, HD10, HD9, HD8, HD7, HD6, HD5, HD4, HD3, HD1, HD2, HD0, INTR, NMI, IGNE#, FERR#, CPURST, STPCLK#, A20M#, INIT, SMI#, PREQ0#, PREQ1#, PREQ2#, AD31, AD30, AD29, AD28, AD27, AD26, AD25, AD24, C/BE3#, AD23, AD22, AD21, AD20, AD19, AD18, AD17, AD16, C/BE2#, FRAME#, IRDY#, TRDY#, DEVSEL#, PLOCK#, STOP#, PAR, C/BE1#, AD15, AD14, AD13, AD12, AD11, AD10, AD9, AD8, C/BE0#, AD7, AD6, AD5, AD4, AD3, AD2, AD1, AD0	

7 Register Summary / Description – Core Logic

7.1 Host-to-PCI Bridge Configuration Space (Device 0, Function 0)

7.1.1 Host-to-PCI Bridge Configuration Space Header

Register Address	Register Name	Default Value	Access type
00-01h	Vendor ID	1039h	RO
02-03h	Device ID	0540h	RO
04-05h	PCI Command Register	0005h	RO,R/W
06-07h	PCI Status Register	0210h	RO,WC
08h	Revision ID	01h	RO
09h	Programming Interface	00h	RO
0Ah	Sub-Class Code	00h	RO
0Bh	Base Class Code	06h	RO
0Ch	Cache Line Size	00h	RO
0Dh	Master Latency Timer	FFh	R/W
0Eh	Header Type	80h	RO
0Fh	BIST	00h	RO
10-13h	Graphic Window Base Address	00000000h	RO,R/W
14-33h	Reserved	0	RO
34h	Capability Pointer	C0h	RO

7.1.2 Host/L2 Cache/DRAM

Register Address	Register Name	Default Value	Access Type
50h	CPU Interface Control	00h	R/W
51h	L2 Cache Control Register	00h	R/W
52h	DRAM Refresh Control	00h	R/W
53h	DRAM' s Queue Depth Control	00h	R/W
54-56h	DRAM Timing Control (I, II, III)	000000h	R/W
57h	SDRAM/VCM Initialization Control	00h	R/W
58h	Memory Buffer Pre-driver Slew Rating	00h	R/W

59-5Ah	Memory Buffer Strength and Current Rating	0000h	R/W
5Bh	PCI Buffer Strength and Current Rating	00h	R/W
5C	MISC Control	00h	R/W
5D-5Fh	Reserved	000000h	R/W
60-62h	DRAM Types of DIMM 0/1/2	0000h	R/W
63h	DRAM Status Register	00h	R/W
64h	Frame Buffer Cache Control	00h	R/W
65h	DIMMs Location for SMA	00h	R/W
66-67h	Reserved	000000h	RO

7.1.3 Power Management

Register Address	Register Name	Default Value	Access Type
68-69h	ACPI I/O Base Address Register	0000h	R/W
6Ah	SMRAM Access Control	00h	R/W
6Bh	CKE Control	00h	R/W
6Ch	DRAM Self-Refresh Control for Power Management	00h	R/W
6D-6Fh	Reserved	000000h	RO

7.1.4 Shadow RAM & Non-cacheable Area

Register Address	Register Name	Default Value	Access Type
70-75h	Shadow RAM Register	00000000h	R/W
76h	BIOS Shadow Attribute	00h	R/W
77h	Non-cacheable Area Characteristics	00h	R/W
78-79h	Allocation of Non-cacheable area I	0000h	R/W
7A-7Bh	Allocation of Non-cacheable area II	0000h	R/W

7.1.5 Hardware Trapping Control

Register Address	Register Name	Default Value	Access Type
7Ch	Hardware Trapping for GUI	00h	R/W

7Dh	Hardware Trapping for HD Clock	00h	R/W
7Eh	Hardware Trapping for Internal Signal Probing	00h	R/W
7Fh	Hardware Trapping for North Bridge	00h	R/W

7.1.6 Host Bridge & PCI Arbiter

Register Address	Register Name	Default Value	Access Type
80h	Burst Length for Delay Transaction	01h	R/W
81h	PCI Target Bridge Characteristics	00h	R/W
82h	PCI Target Bridge Bus Characteristics	00h	R/W
83h	CPU to PCI Characteristics	00h	R/W
84-85h	PCI Grant Timer	FFFFh	R/W
86h	CPU Idle Timer for PCI	FFh	R/W
87h	Reserved	00h	R/W
88-89h	CPU Discard Timer	0000h	R/W
8A-8Bh	PCI Discard Timer for Delay Transaction	FFFFh	R/W

7.1.7 Clock Control

Register Address	Register Name	Default Value	Access Type
8C-8Dh	SDRCLK/SDWCLK Control (I, II, III)	AA2Ah	R/W
8Eh	TAGWE# Signal Control	50h	R/W
8Fh	FBCRCLK/FBCWCLK Control	2Ah	R/W

7.1.8 GART and Page Table Cache

Register Address	Register Name	Default Value	Access Type
90-93h	GART Base Address for Re-mapping	00000000h	RO,R/W
94h	Graphic Window Control	00h	R/W
95h	Integrated VGA Control	00h	R/W
96h	Reserved	00h	RO
97h	Page Table Cache Control	00h	R/W

98h	Page Table Cache Invalidation Control	00h	R/W
99-9Fh	Reserved	0	RO

7.1.9 DRAM Priority Timer

Register Address	Register Name	Default Value	Access type
A0h	CPU/PCI Privilege Timer	00h	R/W
A1h	GUI Privilege Timer	00h	R/W
A2h	CPU/PCI-GUI Privilege Timer Control	00h	R/W
A3h	GUI Grant Timer	00h	R/W

7.1.10 A.G.P. and Host Bridge

Register Address	Register Name	Default Value	Access type
C0-C3h	A.G.P. Capability Identify Register	00200002h	RO
C4-C7h	A.G.P. Status Register	1F000207h	RO
C8-CBh	A.G.P. Command Register	00000000h	R/W, RO

7.1.11 Device 2 (Virtual PCI-to-PCI Bridge)

Register Address	Register Name	Default Value	Access type
00-01h	Vendor ID	1039h	RO
02-03h	Device ID	0001h	RO
04-05h	PCI Command Register	0000h	RO,R/W
06-07h	PCI Status Register	0000h	RO
08h	Revision ID	00h	RO
09h	Programming Interface	00h	RO
0Ah	Sub-Class Code	04h	RO
0Bh	Base Class Code	06h	RO
0Ch	Cache Line Size	00h	RO
0Dh	Master Latency Timer	00h	RO
0Eh	Header Type	01h	RO
0Fh	BIST	00h	RO

10-18h	Reserved	0	RO
19h	Secondary Bus Number	00h	R/W
1Ah	Subordinate Bus Number	00h	R/W
1Bh	Reserved	00h	RO
1Ch	I/O Base	F0h	RO,R/W
1Dh	I/O Limit	00h	RO,R/W
1Eh	Secondary PCI-PCI Status	0000h	RO,R/W
20-21h	Non-prefetchable Memory Base Address	FFF0h	RO,R/W
22-23h	Non-prefetchable Memory Limit Address	0000h	RO,R/W
24-25h	Prefetchable Memory Base Address	FFF0h	RO,R/W
26-27h	Prefetchable Memory Limit Address	0000h	RO,R/W
28-3Dh	Reserved	0	RO
3Eh	PCI to PCI Bridge Control	0000h	R/W,RO

7.2 Register Description -- Core logic

7.2.1 Host Bridge Registers (Device 0, Function 0)

7.2.1.1 Host-to-PCI Bridge Configuration Space Header

Register 00h Vendor ID

Default Value: 1039h

Access: Read Only

The register identifies the manufacturer of the device. SiS is allocated as 1039h by PCI SIG.

Bit	Access	Description
15:0	RO	**Vendor Identification Number**

Register 02h Device ID

Default Value: 0540h

Access: Read Only

The device identifier is allocated as 0540h by Silicon Integrated Systems Corp.

Bit	Access	Description
15:0	RO	**Device Identification Number**

Register 04h PCI Command

Default Value: 0005h

Access: Read/Write, Read Only

The Command register provides coarse control over a device's ability to generate and respond to PCI cycles.

Bit	Access	Description
15:3	RO	**Reserved**
2	RO	**Bus Master** This bit is read-only and the default value is 1. That means the bus master function of the host bridge can not be disabled.
1	R/W	**Memory Space** The bit controls the response to memory space accesses. When the bit is disabled, the host bridge neglect all accesses from PCI masters. 0: Disable 1: Enable
0	RO	**I/O Space** Default value is 1. The host bridge only respond to the addresses 0CF8h and 0CF9h in I/O space, and the I/O transaction must be generated by the host bridge itself.

Register 06h PCI Status

Default Value: 0210h

Access: Read Only, Write Clear

The Status register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a 1. For instance, to clear bit 14 and not affect any other bits, write the value 0100_0000_0000_0000b to the register.

Bit	Access	Description
15:14	RO	**Reserved**
13	WC	**Received Master Abort** This bit is set by SiS540 whenever it terminates a transaction with master abort. This bit is cleared by writing a 1 to it.
12	WC	**Received Target Abort** This bit is set by SiS540 whenever it terminates a transaction with target abort. This bit is cleared by writing a 1 to it.

11	RO	**Reserved**
10:9	RO	**DEVSEL# Timing DEVT** The two bits define the timing to assert DEVSEL#. SiS540 always asserts DEVSEL# within two clocks after the assertion of FRAME#. Default value is DEVT=01.
8:5	RO	**Reserved**
4	RO	**CAP_LIST Bit** The default value is 1 to indicate the configuration space of SiS540 implements new capability mechanism.
3:0	RO	**Reserved**

Register 08h Revision ID

Default Value: 01h

Access: Read Only

The Revision ID is 01h for SiS540 A1 stepping.

Bit	Access	Description
7:0	RO	**Revision Identification Number**

Register 09h Programming Interface

Default Value: 00h

Access: Read Only

The default value is 00h since no specific register-level programming interface is provided.

Bit	Access	Description
7:0	RO	**Programming Interface**

Register 0Ah Sub Class Code

Default Value: 00h

Access: Read Only

The Sub Class Code is 00h for host bridge.

Bit	Access	Description
7:0	RO	**Sub Class Code**

Register 0Bh Base Class Code

Default Value: 06h

Access: Read Only

The value of 06h in this field identifies a bridge device.

Bit	Access	Description
7:0	RO	**Base Class Code**

Register 0Ch Cache Line Size

Default Value: 00h

Access: Read Only

The value of this register is always 00h since the host bridge would not generate the Memory Write and Invalidate command.

Bit	Access	Description
7:0	RO	**Cache Line Size**

Register 0Dh Master Latency Timer (MLT)

Default Value: FFh

Access: Read/Write

The MLT is used in conjunction with PGT(Register 84h) and CIT(Register 86h) to provide a fair and efficient system arbitration mechanism. The value of MLT guarantees the minimum system bandwidth for CPU when both CPU and PCI masters are all craving for system resources (system memory or PCI bus).

Bit	Access	Description
7:0	R/W	**Initial Value for Master Latency Timer** Power-on default value is FFh but it is recommended to set its value to 20h. Unit: PCI clock

Register 0Eh Header Type

Default Value: 80h

Access: Read Only

The value of 80h implies that SiS540 is a multiple function device.

Bit	Access	Description
7:0	RO	**Header Type**

Register 0Fh BIST

Default Value: 00h

Access: Read Only

The value is 00h since SiS540 do not support Build-In Self Test.

Bit	Access	Description
7:0	RO	**BIST**

Register 10h Graphic Window Base Address (GWBA)

Default Value: 00000000h

Access: Read/Write, Read Only

The register defines the starting address of the graphic window for integrated 3D VGA controller. Accessibility and effectiveness of this register is controlled by the Graphic Window Control Register(Register 94h).

Bit	Access	Description
31:22	R/W RO	**Define A[31:22] of Graphic window base address** The accessibility of this bits[31:22] are controlled by graphic window size(Bits[6:4], Register 94h).
21:0	RO	**Reserved and read as zeroes.**

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Size
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	4M
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	8M
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	16M
R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	32M
R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	0	64M
R/W	R/W	R/W	R/W	R/W	0	0	0	0	0	128M
R/W	R/W	R/W	R/W	0	0	0	0	0	0	256M

Register 34h Capability Pointer (CAPPTR)

Default Value: C0h

Access: Read Only

The value of C0h indicates that the A.G.P. bus standard register block is started from Register C0h.

Bit	Access	Description
7:0	RO	**Capability Pointer** Pointer to the Start of A.G.P. bus standard register block.

7.2.1.2 Host/L2 Cache/DRAM Control Register

Register 50h CPU Interface Control

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**NA# Assert Control** When this bit is disabled, SiS540 would not assert NA# under any circumstance. When this bit is enabled, SiS540 asserts NA# for all burst read cycles and I/O cycles. However, I/O address 0CF8h and 0CFCh are the only exceptions and SiS540 would not asserts NA# for these I/O cycles. Bits[6:4] control how and when SiS540 asserts NA# if this bit is enabled. 0: Disable 1: Enable
6	R/W	**NA# Assert for Non-on-board Memory Cycle** When this bit is enabled, SiS540 asserts NA# for all memory cycles that forward to PCI/AGP bus. 0: Disable 1: Enable
5	R/W	**NA# Timing for Burst Read Hit L2 Cycle** This bit controls when SiS540 asserts NA# for burst read hit L2 cycles. When this bit is "0", SiS540 asserts NA# and the 1st BRDY# for the burst read cycle exactly at the same time. When this bit is "1", SiS540 asserts NA# one clock after the 1st BRDY# is returned to CPU. It is recommended to set this bit to "1" if there are two banks of PB SRAM in the system. 0: Normal 1: Delay 1 CPU clock
4	R/W	**NA# Assert for I/O Cycle** When this bit is enabled, SiS540 asserts NA# for all I/O cycles. 0: Disable 1: Enable
3	R/W	**Timing for Read Hit L2 Cycle** When this bit is set to 1, SiS540 will have one more clock for cache-hit decoding. So all the following operations will then delay one clock. It is recommended to set this bit to "1" when the TAG RAM output is not fast enough for SIS540's cache-hit decoding. 0: Normal 1: Delay 1 CPU clock

2	R/W	**Single Read Allocation (L2 Update) Control** When this bit is enabled, any memory single read cycle will cause the corresponding memory line to be updated to L2 cache. 0: Disable 1: Enable
1	R/W	**ADS# Control** When this bit is set to 1, SiS540 will sample the ADS# at the first clock and then proceed the following operations. 0: Sample ADS# by clock 1: Normal
0	R/W	**Reserved**

Register 51h L2 Cache Control

Default Value: 00h

Access: Read/Write

This register controls the L2 cache status and the mode setting for the policy & addressing

Bit	Access	Description
7	R/W	**L2 Cache Enable** When no L2 exists, this bit should be programmed to "0". 0: Disable 1: Enable
6	R/W	**Reserved**
5:4	R/W	**L2 Cache Size** The register specifies the L2 cache size of the system. **Bits[5:4] Size** 00 256K 01 512K 10 1M 11 2M

3	R/W	**L2 Cache WT/WB Policy** The register specifies the coherence policy for L2 cache and system DRAM. This bit must set to 0 when BIOS is sizing the L2 cache. This bit can be set to "1" to support L2 cache in write back mode after L2 cache sizing mode is finished. Note that in write back mode, there are 7 bits tag and 1 dirty bit. And in write through mode, there are 8 bit tag and no dirty bit. 0: Write Through Mode 1: Write Back Mode
2:1	R/W	**Reserved**
0	R/W	**L2 Cache Sizing Mode** SiS540 enters its L2 cache sizing mode when this bit is set to 1. In the sizing mode, TAG addresses are neglected and all accesses to system memory are treated as L2 cache hit cycles. This bit should be set to 0 after the L2 cache sizing procedure has finished. 0: Disable 1: Enable

Register 52h DRAM Refresh Control

Default Value: 00h

Access: Read/Write

This register defines the control timing for the refresh cycle and Queue depth.

Bit	Access	Description
7:6	R/W	**DRAM Refresh Queue Depth** These two bits control the depth of refresh queue. To minimize the performance penalty caused by refresh cycles, the concept of refresh queue is introduced. Refresh request is arbitrated with other DRAM request, if a refresh request does not get served, it enters the refresh queue. The priority of refresh request is promoted to highest when the refresh queue is full. **Bits[5:4] Depth** 00 0 01 4 10 8 11 12

5:4	R/W	**DRAM Refresh Period Control** These two bits are used to determine how often the refresh request will occur. It is timed with a counter based on PCI clock. **Bits[3:2] Rate** 00 15.6us 01 7.8us 10 3.9us 11 Reserved
3	R/W	**Starting Point Control for Ahead Refresh** This bit controls how long should the DRAM arbiter wait before issuing the first ahead refresh request when the bus is idle. For further reducing the performance penalty caused by refresh cycles, SIS540 provides ahead refresh function. When the bus is idle, if no DRAM request is issued during a specific time, the DRAM arbiter will issue refresh request to utilize the bus. In the following 10T, if no other request is issued, another ahead refresh request will be issued. And so on. The maximum number of ahead refresh cycles could be issued is 32. 0: 10T 1: 40T
2	R/W	**Ahead Refresh Function Control** This bit enables the ahead refresh function. 0: Disable 1: Enable
1	R/W	**DRAM Refresh Test Mode** This bit is used to test internal refresh circuit. In test mode, refresh request will be issued per 0.5us. For normal operation, it must be programmed with 0. 0: Normal Mode 1: Test Mode
0	R/W	**Refresh Cycle Enable** When disabled, the normal refresh cycle issued by SIS540 will be prohibited. This function is used by BIOS to perform SDRAM / VCM initialization, during which period SDRAM / VCM can still be refreshed by programming register 57h bit 5. For normal operation, this bit should be programmed with 1. 0: Disable 1: Enable

Register 53h DRAM' s Queue Depth Control

Default Value: 00h

Access: Read/Write

This register controls the queue depth used in DRAM controller.

Bit	Access	Description
7:6	R/W	**Host WFIFO Depth** Bits[7:6] defines the depth of WFIFO in the data path. **Bits[7:6] Depth** 00 8 01 12 10 16 11 20
5	R/W	**CPU-to-MEM Cycle Pipelined Control** 0: Normal 1: Slower
4	R/W	**Host / AGP Command Queue Depth** This bit defines the depth of command queue in DRAM arbiter. 0: 2-level 1: 1-level
3:1	R/W	**Foreground Queue Depth** Bits[3:1] defines the depth of foreground queue in memory controller. **Bits[3:1] Depth** 000 6 001 5 010 4 011 3 100 2 101 1 Others Reserved
0	R/W	**Background Queue Depth** Bit 0 defines the depth of background queue in memory controller. 0: 2-level 1: 1-level

Register 54h DRAM Timing Control (I)

Default Value: 00h

Access: Read/Write

This register controls the timing for SDRAM.

Bit	Access	Description
7:6	R/W	**SDRAM RAS Active Time** Bits[7:6] defines SDRAM ACT to PRE command period, tRAS. **Bits[7:6] Pulse Width** 00 6T 01 7T 10 5T 11 4T
5:4	R/W	**SDRAM RAS# Precharge Time** Bits[5:4] defines SDRAM PRE to ACT command period, tRP. **Bits[5:4] Pulse Width** 00 3T 01 2T 10 4T 11 Reserved
3:2	R/W	**SDRAM RAS to CAS Delay** Bits[3:2] defines SDRAM ACT to Read/Write command period, tRCD. **Bits[3:2] Pulse Width** 00 3T 01 2T 10 4T 11 Reserved
1	R/W	**SDRAM Refresh Cycle Time** Bit 1 defines SDRAM REF to REF/ACT command period, tRC. 0: tRC = tRAS + tRP 1: tRC = tRAS + tRP + 1T

0	R/W	**SDRAM Refresh Cycle Time** When this bit is enabled, refresh commands to different DRAM ranks initiated by SiS540 will be staggered one clock apart, such that simultaneous-switching noise can be reduced. When disabled, SiS540 will issue refresh commands to different DRAM ranks simultaneously. 0: Simultaneous 1: Staggered one clock apart

Register 55h DRAM Timing Control (II)

Default Value: 00h

Access: Read/Write

This register controls the timing for DRAM.

Bit	Access	Description
7	R/W	**Invalidate VCM Table** When this bit is enabled, VCM table will be invalidated. BIOS should disable this bit after it was enabled. This bit is used during FBC initialization sequence when FBC's type is VCM. 0: Disable 1: Enable
6	R/W	**VCM ACT to Prefetch Command Delay Time** This bit defines VCM ACT to Prefetch command period, tAPD. 0: 2T 1: 3T
5:4	R/W	**VCM ACT to ACT/REF Delay** These two bits define VCM REF to REF/ACT command period, tRC. **Bits[5:4] Cycle Time** 00 10T 01 9T 10 8T 11 Reserved
3	R/W	**VCM REF to REF/ACT Delay** This bit defines VCM REF to REF/ACT command period, tRCF. 0: 10T 1: 9T

2	R/W	**Write Recovery Time** This bit defines the Data-in to PRE command period, tWR**.** 0: 1T 1: 2T
1	R/W	**SDRAM ACT to ACT Delay** Bit 1 defines SDRAM ACT(one) to ACT(another) command period, tRRD. 0: 2T 1: 3T
0	R/W	**MDOE# Enable Control** When enabled, SIS540 could drive output data to DRAM. Before SDRAM / VCM initialization sequence, BIOS should turn on this bit. 0: Disable 1: Enable

Register 56h DRAM Timing Control (III)

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Memory Command Output Timing Control** This bit is used to control the timing to drive memory command onto memory bus. When heavy loading memory is used, signal propagation delay may be more than 1 clock. In this case, enable this bit will force all memory command delay 1 clock and the reference clocks are adjustable clocks defined in register 8Ch and 8Dh. 0: Normal 1: Delay 1T
6	R/W	**Lead-off Time Control for DRAM Background Command** When set to 0, background commands are issued 1 clock behind memory address (MA) been issued. When set to 1, background command and MA are issued at the same time. 0: Delay 1T 1: Normal

5	R/W	**Lead-off Time Control for DRAM Read/Write Cycles** When set to 0, memory Read/Write command is issued 1 clock behind memory address (MA) been issued. When set to 1, read command and MA are issued at the same time. 0: Delay 1T 1: Normal
4	R/W	**VCM ACT to RSTA Command Delay Control** When set to 1, the ACT to RSTA timing constraint will be delayed one more clock. 0: Normal 1: Delay 1 Clock
3	R/W	**Reserved**
2	R/W	**One Page/Channel Control** When set to 1, at the same time only one SDRAM page or one VCM channel will be activated (opened) during DRAM access. 0: Normal 1: Only One Page/Channel
1	R/W	**Foreground and Background Command Out-of-Order Control** When set to 0, background commands may go ahead than foreground commands for increasing DRAM utilization. When set to 1, background and foreground commands operate in sequence. 0: Out-of-Order 1: In-Order
0	R/W	**Read / Write Combine Function Control** When set to 0, contiguous single R/W and double read cycles may be combined into a burst cycle. When set to 1, this function is disabled. 0: Enable 1: Disable

Register 57h SDRAM/VCM Initialization Control

Default Value: 00h

Access: Read/Write

This register controls SDRAM / VCM initialization process and timing.

Bit	Access	Description

7	R/W	**Precharge Command** When this bit is set, SiS540 will issue the precharge command to SDRAM / VCM. This bit is automatically cleared after the precharge command is completed. 0: Disable 1: Enable
6	R/W	**Mode Register Set Command** When this bit is set, SiS540 will issue mode register setting command to SDRAM / VCM. This bit is automatically cleared after the mode register setting command is completed. 0: Disable 1: Enable
5	R/W	**Refresh Command** When this bit is set, SiS540 will issue refresh command to SDRAM / VCM. This bit is automatically cleared after the refresh command is completed. 0: Disable 1: Enable
4	R/W	**VCM Set Channel Control Register Command** When this bit is set, SiS540 will issue SCCR command to VCM. This bit is automatically cleared after the refresh command is completed. 0: Disable 1: Enable
3	R/W	**Reserved**
2	R/W	**Do No Operation Command Control** When this bit is set to 1, precharge command set by R57b7 will be turned into No Operation (NOP) command. When this bit is set to 0, precharge command operates normally. 0: Normal 1: Precharge command turn into NOP Command
1	R/W	**VCM Command Truth Table Select** This bit selects the version of VCM command truth table that will be used in memory controller. 0: NEC version 1: JEDEC version

0	R/W	**SDRAM CAS# Latency (CL) Setting** This bit contains the information for SDRAM initialization procedure. 0: 2T 1: 3T

Register 58h Memory Buffer Pre-driver Slew Rating

Default Value 00h

Access Read/Write

This register controls the pre-driver slew rate of DRAM related signals.

Bit	Access	Description
7	R/W	**VDQM[7:0] / VMD[63:0] Pre-driver Slew Rating** 0: Slow 1: Fast
6	R/W	**VCS# / VBA1 / VMA[11:10] Pre-driver Slew Rating** 0: Slow 1: Fast
5	R/W	**CKE Pre-driver Slew Rating** 0: Slow 1: Fast
4	R/W	**CSB[5:0]# Pre-driver Slew Rating** 0: Slow 1: Fast
3	R/W	**CSA[5:0]# Pre-driver Slew Rating** 0: Slow 1: Fast
2	R/W	**DQM[7:0] Pre-driver Slew Rating** 0: Slow 1: Fast
1	R/W	**MD[63:0] Pre-driver Slew Rating** 0: Slow 1: Fast

0	R/W	**SRAS# / SCAS# / WE# / MA[14:0] Pre-driver Slew Rating** 0: Slow 1: Fast

Register 59h Memory Buffer Strength and Current Rating

Default Value 00h

Access Read/Write

This register controls the buffer strength of DRAM related signals.

Bit	Access	Description
7:6	R/W	**VDQM[7:0] / VMD[63:0] Current Rating** 00: Weak 01: Normal 10: Strong 11: Strongest
5:4	R/W	**VCS# / VBA1 / VMA[11:10] Current Rating** 00: Weak 01: Normal 10: Strong 11: Strongest
3:2	R/W	**CKE Current Rating** 00: Weak 01: Normal 10: Strong 11: Strongest
1:0	R/W	**CSB[5:0]# Current Rating** 00: Weak 01: Normal 10: Strong 11: Strongest

Register 5Ah Memory Buffer Strength and Current Rating

Default Value 00h

Access Read/Write

This register controls the buffer strength of DRAM related signals.

Bit	Access	Description

7:6	R/W	**CSA[5:0]# Current Rating** 00: Weak 01: Normal 10: Strong 11: Strongest
5:4	R/W	**DQM[7:0] Current Rating** 00: Weak 01: Normal 10: Strong 11: Strongest
3:2	R/W	**MD[63:0] Current Rating** 00: Weak 01: Normal 10: Strong 11: Strongest
1:0	R/W	**SRAS# / SCAS# / WE# / MA[14:0] Current Rating** 00: Weak 01: Normal 10: Strong 11: Strongest

Register 5Bh PCI Buffer Strength and Current Rating

Default Value 00h

Access Read/Write

This register controls the buffer strength of PCI bus related signals.

Bit	Access	Description
7:2	R/W	**Reserved**
1	R/W	**AD[31:0] Current Rating** This bit controls the buffer strength of AD[31:0] on PCI bus. 0: Weak 1: Strong

0	R/W	**PCI Control Signals Current Rating** This bit controls the buffer strength of FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, C/BE[3:0]# and GNT[2:0]#. 0: Weak 1: Strong

Register 5Ch MISC Control

Default Value 00h

Access Read/Write

Bit	Access	Description
7:3	R/W	**Reserved**
2	R/W	**Interrupt Lock cycle when PCI Master Snoop CPU** 0: Normal 1: Interrupt Lock cycle
1	R/W	**Request Timing Control in DRAM Arbiter** This bit controls the timing of decoding in DRAM arbiter. 0: Delay 1T 1: No delay
0	R/W	**Synchronous Enable** When CPUCLK and SDCLK has the same frequency and phase, then it could be set to synchronous mode to get better performance. 0: Asynchronous mode 1: Synchronous mode

Register 60h/61h/62h DRAM Type Registers for DIMM 0/1/2

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**DRAM Mode Selection** 0: SDRAM 1: VCM
6	R/W	**Reserved**

5	R/W	**DRAM Configuration Selection** 0: Single side 1: Double side
4	R/W	**Reserved**
3:0	R/W	**DRAM Type Selection** **SDRAM NBAxNRAxNCA (Size/Side)** **Bits[3:0] Type** **Bits[3:0] Type** 0000 1x11x8(8M) 1000 1x11x10(32M) 0001 1x13x8(32M) 1001 1x13x10(128M) 0010 2x12x8(32M) 1010 2x12x10(128M) 0011 2x13x8(64M) 1011 2x13x10(256M) 0100 1x11x9(16M) 1100 2x11x 8(16M) 0101 1x13x9(64M) 1101 1x13x11(256M) 0110 2x12x9(64M) 1110 2x12x11(256M) 0111 2x13x9(128M) 1111 2x13x11(512M) **VCM NBAxNRAxNCAxNSA (Size/Side)** **Bits[3:0] Type** **Bits[3:0] Type** 0000 1x13x6x2(32M) 0001 1x13x7x2(64M) 0010 1x13x8x2(128M) others Reserved

Register 63h DRAM Status Register

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Shared Memory Control** 0: Disable 1: Enable
6:4	R/W	**Shared Memory Size** **Bits[6:4] Size Total shared size for 128-bit Mode** 000 2M 4M 001 4M 8M 010 8M 16M 011 16M 32M 100 32M 64M 101 64M Not Support Others Reserved

3	R/W	**Reserved**
2	R/W	**DRAM DIMM2 Status** 0: Absent 1: Installed
1	R/W	**DRAM DIMM1 Status** 0: Absent 1: Installed
0	R/W	**DRAM DIMM0 Status** 0: Absent 1: Installed

Register 64h Frame Buffer Cache (FBC) Control Register

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**FBC Sizing Control** This bit is used by BIOS during FBC initialization sequence. Before FBC sizing sequence, this bit is set to 1. After FBC sizing sequence is finished, BIOS should set this bit to 0. 0: Disable 1: Enable
6	R/W	**Force Two Banks Control** After initialization sequence, if FBC is populated and its internal bank number is different from DIMM0, then this bit should be set to 1. 0: Disable 1: Enable
5	R/W	**Graphics Memory Data Bus Width Control** This bit controls graphics memory data bus width. If FBC is not populated, it should be programmed with 0. If FBC is populated, it could be programmed with 1. 0: 64-bits 1: 128-bits
4	R/W	**FBC Status** 0: Absent 1: Installed

3:0	R/W	**FBC Type Selection** FBC mode is the same as DIMM0. Bits[3:0] defines FBC type. **SDRAM NBAxNRAxNCA (Size)** **Bits[3:0] Type** — **Bits[3:0] Type** 0000 1x 9x8(2M) — 0001 1x10x 8(4M) 0010 1x11x8(8M) — 0011 2x12x 8(32M) 0100 1x11x9(16M) — 0101 1x11x10(32M) 0110 2x11x8(16M) — 0111 1x12x 8(16M) Others Reserved **VCM NBAxNRAxNCAxNSA (Size)** 0000: 1x13x6x2(32M) Others : Reserved

Register 65h DIMMs location for SMA

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:2	R/W	**Reserved**
1:0	R/W	**DIMMs location for SMA** The Share memory used by GUI can be located at any bank which is determined by BIOS during DRAM Detection Sequence. Please refer to BIOS Programming Guide for detail.

7.2.2 Power Management Control Register

Register 68h ACPI I/O Space Base Address Register

Default Value: 0000h

Access: Read/Write

The register specifies the ACPI I/O space base address, and SiS540 may monitor ACPI I/O accesses if the validity bit of this register is set to 1.

Bit	Access	Description
15:5	R/W	**A[15:5] for ACPI I/O Space Base Address** This register provides A[15:5] for the start address of the ACPI I/O space.
4:1	R/W	**Reserved**

0	R/W	**Validity** If this bit is set to 1, the base address contained in Bit[15:5] is valid. Otherwise the base address defined in Bit[15:5] is ignored. 0: Invalid 1: Valid

Register 6Ah SMRAM Access Control

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:5	R/W	**SMRAM Area Re-mapping Control** This field controls how the address on the host bus is mapped to the system memory address when the SMRAM access control bit is enabled or CPU is in the system management mode. **Bits[7:5] Host Address System Memory Address** 000 E0000h~E7FFFh E0000h~E7FFFh (32K) 010 E0000h~E7FFFh A0000h~A7FFFh (32K) 100 E0000h~E7FFFh B0000h~B7FFFh (32K) 110 A0000h~AFFFFh A0000h~AFFFFh (64K) 001 B0000h~BFFFFh B0000h~BFFFFh (64K) 111 A0000h~BFFFFh A0000h~BFFFFh (128K)
4	R/W	**SMRAM Access Control** When the bit is enabled, SMRAM area can be used even when SMIACT# is not asserted. If the bit is disabled, SMRAM area can only be accessed during the SMI handler. 0: Disable 1: Enable
3:0	R/W	**Reserved**

Register 6Bh CKE Control

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:1	R/W	**Reserved**

0	R/W	**CKE Output Timing Control** This bit is used to control the timing of CKE. When heavy loading memory is used, signal propagation delay may be more than 1 clock. In this case, enable this bit will force CKE delay 1 clock and the reference clocks are adjustable clocks defined in register 8Ch. 0: Normal 1: Delay 1T

Register 6Ch DRAM Self-Refresh Control for Power Management

Default Value: 00h

Access: Read/Write

This register controls in what degree that SiS540 support ACPI function and also controls the behavior of CKE.

Bit	Access	Description
7	R/W	**ACPI S3 State Support** 0: Disable 1: Enable
6	R/W	**ACPI S2 State Support** 0: Disable 1: Enable
5	R/W	**CKE Output Enable Control** When this bit is enabled, SiS540 drives CKE. When this bit is disable, SiS540 floats its CKE output. 0: Disable 1: Enable
4	R/W	**CKE Selection** When the value of this bit is 1, SiS540 always drives CKE to low provided CKE Output Enable Control bit is enabled. When the value of this bit is 0, SiS540 drives CKE to low only when it entered self-refresh mode (S2 or S3 state and stop grant cycle issued). 0: Normal Mode 1: Force Low

3:1	R/W	**Early CKE Delay Adjustment** These bits control the timing for CKE. Various delay options are provided to ensure that CKE can meet SDRAM setup time and hold time specification when CKE is driven out. **Bit[3:1] Delay** 000 1ns 001 2ns 010 3ns 011 4ns 100 5ns 101 6ns 110 7ns 111 8ns
0	R/W	**Early CKE Delay 1T Control** When this bit is enabled, CKE is driven out from flip-flop. It is used when system operates under low frequency and CKE delay adjustment method defined in Bits[3:1] can not meet setup time and hold time requirement. 0: Normal 1: Delay 1T

7.2.2.1 Shadow Ram & Non-Cacheable Area Control Register

Register 70h to register 76h define the attribute of the Shadow RAM from 640 KBytes to 1 MBytes. All of the registers 70h to 75h are defined as below, and each register defines the corresponding memory segment's attribute which are listed in the following table.

Register	Defined Range	Register	Defined Range
Register 70h bits 7:5	0C0000h-0C3FFFh	Register 73h bits 7:5	0D8000h-0DBFFFh
Register 70h bits 3:1	0C4000h-0C7FFFh	Register 73h bits 3:1	0DC000h-0DFFFFh
Register 71h bits 7:5	0C8000h-0CBFFFh	Register 74h bits 7:5	0E0000h-0E3FFFh
Register 71h bits 3:1	0CC000h-0CFFFFh	Register 74h bits 3:1	0E4000h-0E7FFFh
Register 72h bits 7:5	0D0000h-0D3FFFh	Register 75h bits 7:5	0E8000h-0EBFFFh
Register 72h bits 3:1	0D4000h-0D7FFFh	Register 75h bits 3:1	0EC000h-0EFFFFh

Register 70/ 71/ 72/ 73/ 74/ 75h Shadow RAM Registers

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Read enable**
6	R/W	**L1/L2 cacheable**
5	R/W	**Write enable**
4	R/W	**Reserved**
3	R/W	**Read enable**
2	R/W	**L1/L2 cacheable**
1	R/W	**Write enable**
0	R/W	**Reserved**

Register 76h Attribute of Shadow RAM for BIOS Area

Default Value: 00h

Access: Read/Write

The 8-bit register controls the access of shadow RAM on BIOS area (F0000h~FFFFFh). When a bit is enabled, the type of the access defined by the bit is allowed.

Bit	Access	Description
7	R/W	**Read Control** When this bit is enabled, any read access for BIOS shadow RAM area is forwarded to system memory. 0: Disable 1: Enable
6	R/W	**Cacheable Control** This bit controls the cacheability for BIOS shadow RAM area 0: Disable 1: Enable
5	R/W	**Write Control** When this bit is enabled, any write access for BIOS shadow RAM area is forwarded to system memory. 0: Disable 1: Enable
4	R/W	**Reserved**

3	R/W	**Shadow RAM enable for PCI access** When this bit is enabled, accesses from PCI masters toward shadow RAM area is allowed. 0: Disable 1: Enable
2:0	R/W	**Reserved**

Register 77h Characteristics of Non-cacheable Area

Default Value: 00h

Access: Read/Write

This register controls the characteristics of the non-cacheable areas defined in Register78h and Register 7Ah.

Bit	Access	Description
7:4	R/W	**Reserved**
3	R/W	**Location of Non-cacheable Area I** This bit specifies whether the non-cacheable area I is located on system memory or PCI bus. 0: System Memory 1: PCI Bus.
2	R/W	**Non-cacheable Area I Enable Control** This bit controls whether the address and size specified on Register 78h are valid or not. When this bit is enable, the range defined by Register 78h is non-cacheable. 0: Disable 1: Enable
1	R/W	**Location of Non-cacheable Area II** This bit specifies whether the non-cacheable area II is located on system memory or PCI bus. 0: System Memory 1: PCI Bus.
0	R/W	**Non-cacheable Area II Enable Control** This bit controls whether the address and size specified on Register 7Ah are valid or not. When this bit is enable, the range defined by Register 7Ah is non-cacheable. 0: Disable 1: Enable

Register 78h Allocation of Non-Cacheable Area I

Default Value: 0000h

Access: Read/Write

This register defines the size and the base address of the first non-cacheable area.

Bit	Access	Description
15:13	R/W	**Size of Non-cacheable Area I** **Bits[15:13] Size** 000 64KB 001 128KB 010 256KB 011 512KB 100 1MB 101 2MB 110 4MB 111 8MB
12:0	R/W	**Base Address of Non-cacheable Area I (Within 512Mbytes)** This field specifies A[28:16] for the base address of the non-cacheable area I. The upper 3 bits of the base address are always regarded as zeros.

Register 7Ah Allocation of Non-cacheable Area II

Default Value: 0000h

Access: Read/Write

This register defines the size and the base address of the second non-cacheable area.

Bit	Access	Description
15:13	R/W	**Size of Non-cacheable Area II** **Bits[15:13] Size** 000 64KB 001 128KB 010 256KB 011 512KB 100 1MB 101 2MB 110 4MB 111 8MB

12:0	R/W	**Base Address of Non-cacheable Area II (Within 512Mbytes)** This field specifies A[28:16] for the base address of the non-cacheable area II. The upper 3 bits of the base address are always regarded as zeros.

Register 7Ch Hardware Trapping for GUI

Default Value: 00h if there is no pull-high resisters on MD[39:32]

Access: Read/Write

Bit	Access	Description
7	R/W	**Reserved**
6	R/W	**MD38: VGA Interrupt Function Enable** 0: Disable 1: Enable
5	R/W	**MD37: External CLKGEN Enable** 0: Disable 1: Enable
4	R/W	**MD36: Panel Link Enable** 0: Disable 1: Enable
3	R/W	**MD35: VGA Multi-Function Select** 0: Select Function 0 1: Select Function 1
2	R/W	**MD34: VGA Multi-Function Enable** 0: Disable 1: Enable
1	R/W	**MD33: Video Bridge Enable** 0: Disable 1: Enable
0	R/W	**MD32: PAL/NTSC Select** 0: Select NTSC system 1: Select PAL system

Register 7Dh Hardware Trapping for HD Clock

Default Value: 00h if there is no pull-high resisters on MD[47:40]

Access: Read/Write

Bit	Access	Description
7:5	R/W	**Reserved**
4:1	R/W	**MD[44:41]: HD Clock Control** This field controls the phase of HD clock that ahead of CPUCLK. **Bit[3:0] Descriptions / Bit[3:0] Descriptions** 1111 -2.5ns / 0111 +1.5ns 1110 -2.0ns / 0110 +2.0ns 1101 -1.5ns / 0101 +2.5ns 1100 -1.0ns / 0100 +3.0ns 1011 -0.5ns / 0011 +3.5ns 1010 0.0ns / 0010 +4.0ns 1001 +0.5ns / 0001 +4.5ns 1000 +1.0ns / 0000 +5.0ns
0	R/W	**MD40: Auto Reset**

Register 7Eh Hardware Trapping for Internal Signal Probing

Default Value: 00h if there is no pull-high resisters on MD[55:48]

Access: Read/Write

Bit	Access	Description
7:5	R/W	**Reserved**
4:2	R/W	**MD[52:50]: Selection for Internal Signals Probing** **Bits[4:2] Group** 000 Core Arbiter 001 GUI Arbiter 010 PCC 011 SDRAM 100 VCSDRAM 101 HOST/PMR 110 PSL 111 Write FIFO
1	R/W	**MD49: Probing Signals Output Control** 0: Output internal signals 1: Output internal clock
0	R/W	**MD48: Probing Enable** 0: Disable 1: Enable

Register 7Fh Hardware Trapping for North Bridge

Default Value: 00h if there is no pull-high resisters on MD[63:56]

Access: Read/Write

Bit	Access	Description
7	R/W	**Reserved**
6	R/W	**MD62: PCI PLL Enable** 0: Enable 1: Disable
5	R/W	**MD61: SDRAM DLL Enable** 0: Enable 1: Disable
4	R/W	**MD60 : CPU DLL** 0: Enable 1: Disable
3:2	R/W	**MD[59:58]: SDRAM DLL's Damping Resister Control**
1:0	R/W	**MD[57:56]: CPU DLL's Damping Resister Control**

7.2.2.2 HOST Bridge and PCI Arbiter Control Register

Register 80h Burst Length for Delay Transaction

Default Value: 01h

Access: Read/Write

The counter is used to prevent one particular PCI master from being serviced with delay-transaction for an unexpected long time while other outstanding PCI requests cannot be served.

Bit	Access	Description
7:0	R/W	**Burst Length for Delay Transaction** Recommended value for this timer is 01h. Unit: One data phase on PCI bus

Register 81h PCI Target Bridge Characteristics

Default Value: 00h

Access: Read/Write

This register controls the characteristics for PCI target bridge.

Bit	Access	Description

7	R/W	**Improved Snoop Function Control for Write cycle** This bit controls whether or not the PCI target bridge does improve snoop function for write cycles. 0: Disable 1: Enable
6	R/W	**Improved Snoop Function Control for Read Cycle** This bit controls whether or not the PCI target bridge does improves snoop function for read cycles. 0: Disable 1: Enable
5	R/W	**Request DRAM Preemption Control** When this bit is enabled, SiS540 will assert STOP# to terminate PCI transaction after arrive the cache line boundary or immediately according the relational register setting if the DRAM is preempted by other requests with higher priority. Otherwise, PSL will keep holding CPU until latency timeout. 0: Disable 1: Enable
4	R/W	**Burst Write Control** When this bit is enabled, SiS540 will issue burst write cycle to retire the CP_WFF data into CS_WFF or write back data to L2. 0: Disable 1: Enable
3	R/W	**Timing of Writing L2** 0: 2-2-2.. 1: 3-3-3..
2	R/W	**PCI-to-AGP GUI Concurrency** 0: Disable 1: Enable
1	R/W	**Hold Acknowledge & WFF Empty** 0: Whenever CS_WFF is empty or not 1: Only after CS_WFF is empty
0	R/W	**Enable Pipe Function between front-end and back-end stage** 0: Disable 1: Enable

Register 82h PCI Target Bridge Bus Characteristics

Default Value: 00h

Access: Read/Write

This register controls the characteristics for 33Mhz PCI target bridge.

Bit	Access	Description
7	R/W	**PCI Peer Concurrency** When this bit is enabled, CPU to L2/DRAM accesses are allowed to perform concurrently with PCI-to-PCI accesses. 0: Disable 1: Enable
6	R/W	**Prefetch Buffer Control** When this bit is set to 1, SiS540 asserts its first TRDY# for a transaction after it prefetched 1quadword of data from system memory. Otherwise, SiS540 asserts its first TRDY# after 2 quadwords are prefetched. 0: Assert TRDY# after prefetching 2 Qws 1: Assert TRDY# after prefetching 1 Qws
5	R/W	**Reserved**
4	R/W	**Memory Read Command Prefetch Control** This bit controls whether or not SiS540 prefetch data for memory read command. Please note that Memory Read Multiple and Memory Read Line commands always do prefetch. The semantic of this bit is different to others. The value of 0 means enable for this bit. 0: Enable 1: Disable
3:2	R/W	**Initial Latency Control** This field controls the target initial latency of the PCI target bridge. If SiS540 is unable to assert TRDY# for a transaction within the target initial latency defined by this field, SiS540 asserts STOP# to retry this cycle. **Bit[3:2] Initial Lantency** 00 Disable 01 16 PCI Clocks 10 24 PCI Clocks 11 32 PCI Clocks

1	R/W	**Subsequent Latency Control** When this bit is enabled, SiS540 terminates a transaction with STOP# if it fails to assert TRDY# for the subsequent block within 8 clocks. 0: Disable 1: Enable
0	R/W	**Address Decoding Time Extension Control** This bit controls the decoding time for deciding whether the PCI transaction is destining to the system memory or not. 0: 1 CPU Clocks 1: 2 CPU Clocks

Register 83h CPU to PCI Characteristics

Default Value: 00h

Access: Read/Write

This register controls miscellaneous functions supported by the CPU-to-PCI bridge of SiS540. The setting of this register may affect PCI performance in various degree.

Bit	Access	Description
7	R/W	**Tri-state Control for Secondary IDE Channel** When this bit is set to '1', the control signals of secondary IDE channel will be floated. 0: Enable mode 1: Tri-state mode
6	R/W	**Tri-state Control for Primary IDE Channel** When this bit is set to '1', the control signals of primary IDE channel will be floated. 0: Enable mode 1: Tri-state mode
5	R/W	**PCI Grant Timer / Discard Timer Testing Mode** For internal usage only, please program this bit with 0. 0: Disable 1: Enable

4	R/W	**Lock Control** When this bit is enabled, a 64-bit memory read cycle from CPU toward 33Mhz PCI bus is converted into locked PCI memory read cycles. 0: Disable 1: Enable
3	R/W	**CPU Involved Arbitration on PCI** PGT(Register 84h), CIT(Register 86h) and MLT(Register 0Dh) can only take effect when this bit is enable. When this bit is enable, SiS540 does not block CPU from operation longer than the period defined by PGT to serve PCI masters, and minimum access time for CPU is guaranteed by MLT. 0: Disable 1: Enable
2	R/W	**64-bit Access Retry Behavior Control** When the value of this bit is 0 and the second half non-post PCI cycle(or the second data phase) of a 64-bit access is retried by a PCI target, SiS540 tries to issue the second half cycle again and again until it completes successfully on PCI bus. When this bit is set to 1, retry for any non-post cycle issued by the host bridge results in the assertion of BOFF#. It is recommended to set this bit to 0. 0: Continue Retry 1: Back-Off CPU
1	R/W	**Memory Burst Control** This bit controls whether or not the host bridge generates memory burst cycles. 0: Disable 1: Enable
0	R/W	**Memory Post Write Control** When this bit is enable, all CPU to PCI memory write cycles are posted. 0: Disable 1: Enable

Register 84h PCI Grant Timer

Default Value: FFFFh

Access: Read/Write

The timer is used to prevent PCI masters from seizing the PCI bus too long. When the timer expired, PCI arbiter forces the master that is currently occupying PCI bus to relinquish PCI bus by removing its grant.

Bit	Access	Description
15:0	R/W	**PCI Grant Timer** The setting of this register should consider the overall system configuration and the value of MLT(Register 1Dh). For a system that has many PCI master devices, the value should be higher. For a system with fewer master devices, the value should be smaller. Typical value of this timer is 60h if MLT is set to 20h. Unit: PCI clock

Register 86h CPU Idle Timer for PCI

Default Value: FFh

Access: Read/Write

The timer is used to prevent CPU from idling too long while outstanding PCI requests cannot be served.

Bit	Access	Description
7:0	R/W	**CPU Idle Timer** Recommended value for this timer is 03h. Unit: PCI clock

Register 87h Reserved

Register 88h CPU Discard Timer

Default Value: 0000h

Access: Read/Write

The timer is used to keep PCI hold when PCI read is retried due to the CPU-to-PCI post write FIFO is not empty.

Bit	Access	Description
15:0	R/W	**PCI Discard Timer** This timer is used to keep PCI hold when PCI read is retried due to the CPU-to-PCI post write FIFO is not empty. The recommended value for this timer is 0800h. Unit: PCI clock

Register 8Ah PCI Discard Timer for Delay Transaction

Default Value: FFFFh

Access: Read/Write

The timer is used to prevent PCI master from seizing PCI bus too long when PCI master encounter timeout. When the timer expires, SIS 540 will flush CPU-to-PCI FIFO to abort the current PCI transaction.

Bit	Access	Description
15:0	R/W	**PCI Discard Timer for Delay transaction** This timer is used to guarantee PCI read transaction is completed in the timer. If not, the read data is discard. The recommended value for this timer is FFFFh. **Unit**: **PCI clock**

7.2.2.3 Clock Control Register

Register 8Ch SDRCLK/SDWCLK(I) Control Register

Default Value: 2Ah

Access: Read/Write

To improve the setup time of MD for read/write DRAM, SiS540 introduces two clocks, SDRCLK and SDWCLK, that have some phase differences from SDCLK, which is the clock that applies to SDRAM. Adjusting these two clocks lets the target to have more setup time budget. However, it decreases the hold time.

Bit	Access	Description
7:4	R/W	**SDRCLK Control** This field controls the phase of SDRCLK that lags behind SDCLK.

Bit[7:4]	Descriptions	Bit[7:4]	Descriptions
1111	+6.5ns	0111	+2.5ns
1110	+6.0ns	0110	+2.0ns
1101	+5.5ns	0101	+1.5ns
1100	+5.0ns	0100	+1.0ns
1011	+4.5ns	0011	+0.5ns
1010	+4.0ns	0010 (default)	0ns
1001	+3.5ns	0001	-0.5ns
1000	+3.0ns	0000	-1.0ns

3:0	R/W	**SDWCLK(I) Control for CS# / CKE** This field controls the phase of SDWCLK used for CS# / CKE signals that lags ahead SDCLK.

Bit[7:4]	Descriptions	Bit[7:4]	Descriptions
1111	-2.5ns	0111	+1.5ns
1110	-2.0ns	0110	+2.0ns
1101	-1.5ns	0101	+2.5ns
1100	-1.0ns	0100	+3.0ns
1011	-0.5ns	0011	+3.5ns
1010	0ns	0010	+4.0ns
1001	+0.5ns	0001	+4.5ns
1000	+1.0ns	0000	+5.0ns

Register 8Dh SDWCLK(II),(III) Control Register

Default Value: AAh

Access: Read/Write

Bit	Access	Description
7:4	R/W	**SDWCLK(II) Control for MA / SRAS# / SCAS# / RAMW#** This field controls the phase of SDWCLK used for MA / SRAS# / SCAS# / RAMW# signals that lags ahead SDCLK.

Bit[7:4]	Descriptions	Bit[7:4]	Descriptions
1111	-2.5ns	0111	+1.5ns
1110	-2.0ns	0110	+2.0ns
1101	-1.5ns	0101	+2.5ns
1100	-1.0ns	0100	+3.0ns
1011	-0.5ns	0011	+3.5ns
1010	0ns	0010	+4.0ns
1001	+0.5ns	0001	+4.5ns
1000	+1.0ns	0000	+5.0ns

3:0	R/W	**SDWCLK(III) Control for DQM / MD** This field controls the phase of SDWCLK used for DQM / MD signals that lags ahead SDCLK. **Bit[7:4] Descriptions Bit[7:4] Descriptions** 1111 -2.5ns 0111 +1.5ns 1110 -2.0ns 0110 +2.0ns 1101 -1.5ns 0101 +2.5ns 1100 -1.0ns 0100 +3.0ns 1011 -0.5ns 0011 +3.5ns 1010 0ns 0010 +4.0ns 1001 +0.5ns 0001 +4.5ns 1000 +1.0ns 0000 +5.0ns

Register 8Eh TAGWE# Signal Control Register

Default Value: 50h

Access: Read/Write

Bit	Access	Description
7:4	R/W	**TAGWE Pulse Width** **Bit[7:4] Descriptions Bit[7:4] Descriptions** 1111 T/2+8.0ns 0111 T/2+4.0ns 1110 T/2+7.5ns 0110 T/2+3.5ns 1101 T/2+7.0ns 0101 T/2+3.0ns 1100 T/2+6.5ns 0100 T/2+2.5ns 1011 T/2+6.0ns 0011 T/2+2.0ns 1010 T/2+5.5ns 0010 T/2+1.5ns 1001 T/2+5.0ns 0001 T/2+1.0ns 1000 T/2+4.5ns 0000 T/2+0.5ns Where T is CPU clock.
3:1	R/W	**Reserved**
0	R/W	**TAGWE Pulse Width Control** 0: Depend on Reg 8E Bits [7:4], but no more than 1T. 1: Depend on Reg 8E Bits [7:4].

Register 8Fh FBCRCLK/FBCWCLK Control Register

Default Value: 2Ah

Access: Read/Write

Bit	Access	Description
7:4	R/W	**FBCRCLK Control** This field controls the phase of FBCRCLK that lags behind SDCLK. **Bit[7:4] Descriptions Bit[7:4] Descriptions** 1111 +6.5ns 0111 +2.5ns 1110 +6.0ns 0110 +2.0ns 1101 +5.5ns 0101 +1.5ns 1100 +5.0ns 0100 +1.0ns 1011 +4.5ns 0011 +0.5ns 1010 +4.0ns 0010 (default) 0ns 1001 +3.5ns 0001 -0.5ns 1000 +3.0ns 0000 -1.0ns
3:0	R/W	**FBCWCLK Control** This field controls the phase of FBCWCLK that lags ahead SDCLK. **Bit[7:4] Descriptions Bit[7:4] Descriptions** 1111 -2.5ns 0111 +1.5ns 1110 -2.0ns 0110 +2.0ns 1101 -1.5ns 0101 +2.5ns 1100 -1.0ns 0100 +3.0ns 1011 -0.5ns 0011 +3.5ns 1010 0ns 0010 +4.0ns 1001 +0.5ns 0001 +4.5ns 1000 +1.0ns 0000 +5.0ns

7.2.2.4 GART and Page Table Cache Control Register

Register 90h GART Base Address

Default Value: 00000000h

Access: Read Only, Read/Write

This register specifies the starting address of the Graphics Address Re-mapping Table. The Re-mapping table is resided in system memory and it translates graphic address into the system memory address.

Bit	Access	Description

31:12	R/W	**A[31:12] for GART Base Address** This register provides the starting address of the Graphics Address Re-mapping Table which is always located in system memory. Please note that although there is no register that directly specifies the size of GART, the size of GART can still be known via graphic window size(Bits[6:4] of Register 94h) (Please note that the address provided via GART Base is 4KB aligned)
11:0	RO	**Reserved**

Register 94h Graphic Window Control

Default Value: 00h

Access: Read/Write

This register specified the size of the graphic window and indicates that whether the Graphic Window Base Address Register and Re-mapping GART Base Address Register contain valid information or not.

Bit	Access	Description
7	R/W	**Reserved**
6:4	R/W	**Graphic Window Size** This field defines the size of the graphic window. The accessibility of GWBA register (Register 10h) is also controlled by this field. **Bits[6:4] Size** 000 4Mbyte 001 8Mbyte 010 16Mbyte 011 32Mbyte 100 64Mbyte 101 128Mbyte 110 256Mbyte 111 Reserved
3:2	R/W	**Reserved**
1	R/W	**Graphic Window Base Address Validity** The value of "1" for this bit indicates that the Graphic Window Base Address specified in GWBA Register(Register 10h) is valid. Otherwise, the address specified in GWBA Register is invalid. 0: Invalid 1: Valid

0	R/W	**GART Base Address Validity** The value of "1" for this bit indicates that the GART Base Address specified in Register 90h is valid. Otherwise, the address specified in Register 90h is invalid. 0: Invalid 1: Valid

Register 95h Integrated VGA Control

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:3	R/W	**Reserved**
2	R/W	**VGA Configuration Access Control** When this bit set to 0, VGA configuration access can be read and written. When set to 1, VGA configuration can not be accessed. 0: Enable 1: Disable
1	R/W	**Reserved**
0	R/W	**Monochrome Device Adapter (MDA) Existence Register** 0: Not exist 1: Exist

Register 96h Reserved

Register 97h Page Table Cache Control

Default Value: 00h

Access: Read/Write

Page Table Cache is used to speedup the address translation process from graphic address to system memory address. It stores recently used GART entries in the core logic to prevent traffics toward system memory during address translation process. This register controls the characteristic of the page table cache and the address translation mechanism.

Bit	Access	Description
7:3	R/W	**Reserved**

2	R/W	**GART-Write Invalidate Page Table Cache Control** This bit controls SiS540 to avoid using stalled page table cache. When this bit is enabled, SiS540 automatically detects write accesses toward all GART entries and it invalidates the entire page table cache immediately once it observes such an event. If disabled, memory write cycle hits page table entry won't invalidate the table. 0: Disable 1: Enable
1	R/W	**Reserved**
0	R/W	**Page Table Cache Enable** When this bit is enabled, page table cache will be used for accelerating the address translation process. When this bit is disable, no GART entries are cached into the page table cache and any address translation is done after getting the GART entry by a memory read. 0: Disable 1: Enable

Register 98h Page Table Cache Invalidation Control

Default Value: 00h

Access: Read/Write

The register controls the invalidation of page table cache.

Bit	Access	Description
7:2	R/W	**Reserved**
1	R/W	**Invalidate Whole Page Table Cache** Invalidate whole page table cache entries when write 1 to this bit. This bit is cleared after the invalidation process completed.
0	R/W	**Reserved**

7.2.2.5 DRAM Priority Timer Control Register

SiS540 maintains the privilege of DRAM usage between CPU/PCI and GUI. When both CPU/PCI and GUI are craving for the resource of system memory, this set of timers provides the adjustment of DRAM bandwidth between these two agents. The operation of the set of timers is explained below.

If GUI data transfer has higher privilege over CPU/PCI, GUI high privilege timer decreases every clock when GUI access toward system memory is undergoing. If CPU/PCI privilege is higher than GUI, CPU/PCI high privilege timer decreases every clock when CPU/PCI accesses system memory. The privilege relationship between CPU/PCI and GUI is

exchanged after the timer expired. CPU/PCI accesses do not affect any one of these two timers if CPU/PCI does not have higher privilege than GUI. In the same way, GUI low priority accesses do not affect timers if GUI device does not have higher privilege than CPU/PCI.

Register A0h CPU/PCI Privilege Timer

Default Value: 00h

Access: Read/Write

BIT	Access	Description
7:0	R/W	**Initial Value for CPU/PCI High Privilege Timer** The timer controls how long the CPU/PCI has higher privilege over GUI data transfer for DRAM accesses. **Unit**: DRAM clock * 4

Register A1h GUI Privilege Timer

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**Initial Value for GUI High Privilege Timer** The timer controls how long the GUI has higher privilege over CPU/PCI data transfer for DRAM accesses. **Unit**: DRAM clock * 4

Register A2h CPU/PCI-GUI Privilege Timer Control

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:6	R/W	**CPU/PCI-GUI Privilege Timer Control** **Bits[7:6] Privilege** 00 CPU/PCI High Privilege 01 GUI High Privilege 1x Enable CPU/PCI-GUI Privilege Timer
5:2	R/W	**Reserved**

1	R/W	**Enhance 3D Performance Control** In order to enhance 3D performance, when one of 3D request acquires the DRAM bus, arbiter will mask all other 3D requests until present transaction is finished. 0: Disable 1: Enable
0	R/W	**Rising AGP Request priority to shorten CPU High Request Waiting time** When CPU high priority request is bounded by AGP requests, arbiter will mask the requests that between CPU high priority request and AGP requests until CPU request isn't bound by AGP requests. 0: Disable 1: Enable

Register A3h GUI Grant Timer

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:4	R/W	**Reserved**
3:0	R/W	**Initial Value of GUI Grant Timer** The timer determines the maximum transactions will be done when GUI gets the DRAM and it's a GUI multi-transaction.

Bit[3:0]	Transactions	Bit[3:0]	Transactions
0000	1	1000	9
0001	2	1001	10
0010	3	1010	11
0011	4	1011	12
0100	5	1100	13
0101	6	1101	14
0110	7	1110	15
0111	8	1111	16

7.2.2.6 A.G.P. and Host Bridge Control Registers

Register C0h A.G.P. Capability Identify Register (ACAPID)

Default Value: 00200002h

Access: Read Only

Bit	Access	Description
31:24	RO	**Reserved**
23:20	RO	**A.G.P revision Major** Default value is 0010b to indicate that SiS540 conforms to the major revision 2 of internal A.G.P. bus interface specification.
19:16	RO	**A.G.P revision Minor** Default value is 0000b to indicate that SiS540 conforms to the minor revision 0 of internal A.G.P. interface specification.
15:8	RO	**Next Capability** Default value is 00h to indicate the final item.
7:0	RO	**A.G.P. Capability ID** Default value is 02h to indicate the list item as pertaining to A.G.P. registers.

Register C4h A.G.P. Status Register

Default Value: 1F000207h

Access: Read Only

Bit	Access	Description
31:24	RO	**RQ Field** The RQ field contains the maximum number of A.G.P. command requests SiS540 can manage. Default value is 1Fh to indicate that the maximum number of A.G.P. command requests SiS540 can manage is 32.
23:10	RO	**Reserved**
9	RO	**SBA** Default value is 1 to indicate that SiS540 supports side band addressing.
8:3	RO	**Reserved**
2:0	RO	**Data Rate** The RATE field indicates the data transfer rates supported by this device. Default value is 111b to indicate SiS540 support both 1X, 2X and 4X mode.

Register C8h A.G.P. Command Register

Default Value: 00000000h

Access: Read/Write, Read Only

Bit	Access	Description
31:10	RO	**Reserved**
9	R/W	**SBA_ENABLE** When set, the side band address mechanism is enabled.
8	R/W	**A.G.P._ENABLE** Setting the bit allows the target to accept A.G.P. operations. When cleared, the target ignores incoming A.G.P. operations. Please note that the target must be enabled before the master.
7:3	RO	**Reserved**
2:0	R/W	**Data Rate** One (and only one) bit in the DATA_RATE field must be set to indicate the desired data transfer rate. <Bit0: 1X, Bit1: 2X, Bit2: 4X>. The same bit must be set on both master and target. The DATA_RATE field applies to AD and SBA buses. **Bits[2:0] Data Rate** 001 1X mode 010 2X mode 100 4X mode Others Reserved

7.2.3 Virtual PCI-to-PCI Bridge Registers (Device 2)

Register 00h Vendor ID

Default Value: 1039h

Access: Read Only

The register identifies the manufacturer of the device. SiS is allocated as 1039h by PCI SIG.

Bit	Access	Description
15:0	RO	**Vendor Identification Number**

Register 02h Device ID

Default Value: 0001h

Access: Read Only

The device identifier is allocated as 0001h by Silicon Integrated Systems Corp.

Bit	Access	Description

15:0	RO	**Device Identification Number**

Register 04h Command

Default Value: 00h

Access: Read/Write, Read Only

The Command register provides coarse control over a device's ability to generate and respond to PCI cycles.

Bit	Access	Description
15:6	RO	**Reserved**
5	R/W	**VGA Palette Snoop Enable** Controls the behavior in the case of CPU access destining to VGA compatible address. The bit affects the destinations of I/O writes issued by the CPU with address 3C6h, 3C8h, 3C9h. 0: Disable 1: Enable
4:3	RO	**Reserved**
2	R/W	**Bus Master Enable** Controls the bridge's response to PCI cycles on A.G.P. When this bit is disabled, the bridge does not response to any transaction on A.G.P. 0: Disable 1: Enable
1	R/W	**Memory Space Enable** Controls the forwarding of memory accesses from CPU to internal A.G.P. bus When the bit is disabled, the bridge would not forward any memory accesses to internal A.G.P. bus. When the bit is enabled, the bridge forwards CPU memory cycles toward internal A.G.P. bus according to standard PCI-to-PCI bridge forwarding rule. 0: Disable 1: Enable

0	R/W	**I/O Space Enable** Controls the forwarding of I/O accesses from CPU to internal A.G.P. bus When the bit is disabled, the bridge would not forward any I/O accesses to internal A.G.P. bus. When the bit is enabled, the bridge forwards CPU I/O cycles toward internal A.G.P. bus according to standard PCI-to-PCI bridge forwarding rule. 0: Disable 1: Enable

Register 06h Status

Default Value: 00h

Access: Read Only

This register is reserved since the status information of the primary bus is stored in the status register of Device 0.

Bit	Access	Description
15:0	RO	**Reserved**

Register 08h Revision ID

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	**Revision Identification Number**

Register 09h Programming Interface

Default Value: 00h

Access: Read Only

The default value is 00h since no specific register-level programming interface is provided.

Bit	Access	Description
7:0	RO	**Programming Interface**

Register 0Ah Sub Class Code

Default Value: 04h

Access: Read Only

The Sub Class Code is 04h for PCI-to-PCI bridge.

Bit	Access	Description

7:0	RO	**Sub Class Code**

Register 0Bh Base Class Code

Default Value: 06h

Access: Read Only

The value of 06h in this field identifies a bridge device.

Bit	Access	Description
7:0	RO	**Base Class Code**

Register 0Ch Cache Line Size

Default Value: 00h

Access: Read Only

The value of this register is always 00h since the host bridge would not generate the Memory Write and Invalidate command.

Bit	Access	Description
7:0	RO	**Cache Line Size**

Register 0Dh Master Latency Timer (MLT)

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	**Master Latency Timer**

Register 0Eh Header Type

Default Value: 01h

Access: Read Only

The value of 01h identifies PCI-to-PCI bridge header is being used.

Bit	Access	Description
7:0	RO	**Header Type**

Register 0Fh BIST

Default Value: 00h

Access: Read Only

The value is 00h since we do not support Build-In Self Test.

Bit	Access	Description
7:0	RO	**BIST**

Register 19h Secondary Bus Number (SBUSN)

Default Value: 00h

Access: Read/Write

This register identifies the bus number assigned to the second bus side of the virtual PCI-to-PCI Bridge. This field is programmed by the PCI configuration software to allow mapping of configuration cycles to A.G.P. bus.

Bit	Access	Description
7:0	R/W	**Secondary Bus Number**

Register 1Ah Subordinate Bus Number (SUBUSN)

Default Value: 00h

Access: Read/Write

This register is used to record the number of the highest numbered PCI bus that is behind A.G.P. bus.

Bit	Access	Description
7:0	R/W	**Subordinate Bus Number**

Register 1Bh Reserved

Register 1Ch I/O Base

Default Value: F0h

Access: Read/Write, Read Only

The I/O Base register defines the bottom address of an address range that is used by SiS540 to determine when to forward I/O transactions from CPU to host VGA bus.

Bit	Access	Description
7:4	R/W	**I/O Address Base A[15:12]** Bits[7:4] control the CPU to internal host VGA bus I/O access. SiS540 forwards I/O cycle initiated by CPU to internal host VGA bus if the address of the cycle meets the following requirement. **I/O_BASE** ≤ address ≤ **I/O_LIMIT**
3:0	RO	**Reserved**

Register 1Dh I/O Limit

Default Value: 00h

Access: Read/Write, Read Only

The I/O Limit register defines the top address of an address range that is used by SiS540 to determine when to forward I/O transactions from CPU to internal host VGA bus.

Bit	Access	Description
7:4	R/W	**I/O Address Limit A[15:12]** Bits[7:4] control the CPU to internal VGA controller I/O access. SiS540 forwards I/O cycle initiated by CPU to host VGA bus if the address of the cycle meets the following requirement. **I/O_BASE** ≤ address ≤ **I/O_LIMIT**
3:0	RO	**Reserved**

Register 1Eh Secondary PCI-PCI Status (SSTS)

Default Value: 0000h

Access: Read/Write, Read Only

The Secondary Status register is similar in function and bit definition to the Status register of device 0 function 0 of SiS540.

Bit	Access	Description
15:14	RO	**Reserved**
13	WC	**Receiver Master Abort** When SiS540 terminates a cycle on host VGA bus with master abort, this bit is set to 1. This bit can be cleared by writing a 1 to it.
12:0	RO	**Reserved**

Register 20h Non-prefetchable Memory Base Address (MBASE)

Default Value: FFF0h

Access: Read/Write, Read Only

The register defines the bottom address of a non-prefetchable memory address range that is used by SiS540 to determine when to forward memory transactions from CPU to host VGA bus.

Bit	Access	Description
15:4	R/W	**Memory Address Base A[31:20].** Bits[15:4] control the CPU to internal VGA controller memory access. SiS540 forwards I/O cycle initiated by CPU to host VGA bus if the address of the cycle meets the following requirement. **MBASE** ≤ address ≤ **MLIMIT**

3:0	RO	**Reserved**

Register 22h Non-prefetchable Memory Limit Address (MLIMIT)

Default Value: 0000h

Access: Read/Write, Read Only

The register defines the top address of a non-prefetchable memory address range that is used by SiS540 to determine when to forward memory transactions from CPU to host VGA bus

Bit	Access	Description
15:4	R/W	**Memory Address Limit A[31:20].** Bits[15:4] control the CPU to integrated VGA controller memory access. SiS540 forwards I/O cycle initiated by CPU to host VGA bus if the address of the cycle meets the following requirement. **MBASE** ≤ address ≤ **MLIMIT**
3:0	RO	**Reserved**

Register 24h Prefetchable Memory Base Address (PMBASE)

Default Value: FFF0h

Access: Read/Write, Read Only

The register defines the bottom address of a prefetchable memory address range that is used by SiS540 to determine when to forward memory transactions from CPU to host VGA

Bit	Access	Description
15:4	R/W	**Memory Address Base A[31:20].** Bits[15:4] control the CPU to integrated VGA controller memory access. SiS540 forwards I/O cycle initiated by CPU to host VGA bus if the address of the cycle meets the following requirement. **PMBASE** ≤ address ≤ **PMLIMIT**
3:0	RO	**Reserved**

Register 26h Prefetchable Memory Limit Address (PMLIMIT)

Default Value: 0000h

Access: Read/Write, Read Only

The register defines the top address of a prefetchable memory address range that is used by SiS540 to determine when to forward memory transactions from CPU to host VGA bus.

Bit	Access	Description

15:4	R/W	**Memory Address Limit A[31:20].** Bits[15:4] control the CPU to integrated VGA controller memory access. SiS540 forwards I/O cycle initiated by CPU to host VGA bus if the address of the cycle meets the following requirement. **PMBASE** ≤ address ≤ **PMLIMIT**
3:0	RO	**Reserved**

Register 3Eh PCI to PCI Bridge Control (BCTRL)

Default Value: 0000h

Access: Read/Write, Read Only

The Bridge Control register provides control extensions to the Command register.

Bit	Access	Description
15:4	RO	**Reserved.**
3	R/W	**VGA Enable** The bit controls the response by bridge to VGA compatible memory and I/O address. VGA compatible memory and I/O address will be forwarded to host VGA bus when this bit is set to "1". 0 : Disable 1 : Enable
2	R/W	**ISA Enable** When this bit is enabled, IO transactions addressing the last 768 bytes in each 1KB block will be forwarded to primary PCI bus even if the address are within the range defined by the IOBASE and IOLIMIT. 0 : Disable 1 : Enable
1:0	RO	**Reserved**

8 PCI IDE Configuration Space Register

Device	IDSEL	Function Number
IDE	AD11	0001b

Register 00h Vendor ID

Default Value: 1039h

Access: Read Only

The register identifies the manufacturer of the device. SiS is allocated as 1039h by PCI SIG.

Bit	Access	Description
15:0	RO	**Vendor Identification Number**

Register 02h Device ID

Default Value: 5513h

Access: Read Only

The device identifier is allocated as 5513h by Silicon Integrated Systems Corp.

Bit	Access	Description
15:0	RO	**Device Identification Number**

Register 04h Command

Default Value: 0000h

Access: Read/Write, Read Only

The Command register provides coarse control over a device ability to generate and respond to PCI cycles.

Bit	Access	Description
15:3	RO	**Reserved**
2	R/W	**Bus Master** When set, the Bus master function is enabled. It is disabled by default.
1	R/W	**Memory Space** The bit controls the response to memory space accesses. This bit should be programmed as "0".

0	R/W	**I/O Space** When enabled, the built-in IDE will respond to any access of the IDE legacy ports in the compatibility mode, or to any access of the IDE relocated ports in the native mode. Also, any access to the PCI bus master IDE registers are allowed. This bit is zero (disabled) on reset.

Register 06h Status

Default Value: 0000h

Access: Read/Write, Read Only, Write Clear

The Status register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a 1. For instance, to clear bit 14 and not affect any other bits, write the value 0100_0000_0000_0000b to the register.

Bit	Access	Description
15:14	RO	**Reserved** These bits are hardware to zero.
13	WC	**Master Abort Asserted** This bit is set when a PCI bus master IDE transaction is terminated by master abort. While this bit is set, IDE will issue an interrupt request. This bit can be cleared by writing a 1 to it.
12	WC	**Received Target Abort** The bit is set whenever PCI bus master IDE transaction is terminated with target abort.
11	RO	**Signaled Target Abort** The bit will be asserted when IDE terminates a transaction with target abort.
10:9	RO	**DEVSEL# Timing DEVT** These two bits define the timing of asserting DEVSEL#. The built-in IDE always asserts DEVSEL# in fast timing, and thus the two bits are hardwired to 0 per PCI Spec.
8	RO	**Reserved, Read as "0".**
7:0	RO	**Reserved** Default value is 00h

Register 08h Revision ID

Default Value: D0h

Access: Read Only

Bit	Access	Description
7:0	RO	**Revision Identification Number**

Register 09h Programming Interface

Default Value: 00h

Access: Read Only, Read/Write

The default value is 00h since no specific register-level programming interface is provided.

Bit	Access	Description
7	RO	**Master IDE Device** This bit is hardwired to one to indicate that the built-in IDE is capable of supporting bus master function.
6:4	RO	**Reserved**
3	RO	**Secondary IDE Programmable Indicator** When the bit is programmed as "1", it means that the primary channel can be programmed to operate in compatible or native mode. When the bit is programmed as "0", the mode is fixed and is determined by the value of bit 2. This bit should be programmed as "1" during the BIOS boot up procedures.
2	R/W	**Secondary IDE Operating Mode** This bit defines the mode that the secondary IDE channel is operating in. Zero corresponds to 'compatibility' while one means native mode. By default, this bit is 0 and is programmable.
1	RO	**Primary IDE Programmable Indicator** When the bit is programmed as "1", it means that the primary channel can be programmed to operate in compatible or native mode. When the bit is programmed as "0", the mode is fixed and is determined by the value of bit 0. This bit should be programmed as "1" during the BIOS boot up procedures.
0	R/W	**Primary IDE Operating Mode** This bit defines the mode that the primary IDE channel is operating in. Zero corresponds to 'compatibility' while one means native mode. By default, this bit is 0 and is programmable.

Register 0Ah Sub Class Code

Default Value: 01h

Access: Read Only

Bit	Access	Description

7:0	RO	**Sub Class Code**

Register 0Bh Base Class Code

Default Value: 01h

Access: Read Only

Bit	Access	Description
7:0	RO	**Base Class Code**

Register 0Ch Cache Line Size

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	**Cache Line Size**

Register 0Dh Latency Timer

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**Initial Value for Latency Timer** The default value is 0. Unit: PCI clock

Register 0Eh Header Type

Default Value: 80h

Access: Read Only

Bit	Access	Description
7:0	RO	**Header Type**

Register 0Fh BIST

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	**BIST**

Register 10h~13h Primary Channel Command Block Base Address Register

Register 14h~17h Primary Channel Control Block Base Address Register

Register 18h~1Bh Secondary Channel Command Block Base Address Register

Register 1Ch~1Fh Secondary Channel Control Block Base Address Register

In the native mode, above four registers define the IDE base address for each of the two IDE devices in both the primary and secondary channels respectively. In the compatible mode, the four registers can still be programmed and read out, but it does not affect the IDE address decoding.

Register 20h~23h Bus Master IDE Control Register Base Address

Offset Register	Register Access
00h	Bus Master IDE Command Register (Primary)
01h	Reserved
02h	Bus Master IDE Status Register(Primary)
03h	Reserved
04-07h	Bus Master IDE PRD (*) Table Pointer (Primary)
08h	Bus Master IDE Command Register (Secondary)
09h	Reserved
0Ah	Bus Master IDE Status Register (Secondary)
0Bh	Reserved
0C-0Fh	Bus Master IDE PRD (*) Table Pointer (Secondary)

*PRD: Physical Region Descriptor

Register 24h~2Bh Reserved

Register 2C~2Dh Subsystem Vendor ID

Default Value: 0000h

Access: Read/Write

This register can be written once and is used to identify vendor of the subsystem.

Register 2Eh~2Fh Subsystem ID

Default Value: 0000h

Access: Read/Write

This register can be written once and is used to identify subsystem ID.

Register 30h~3Bh Reserved

Register 3Ch Interrupt Line

Default value: 00h

Access: Read/Write

Register 3Dh Interrupt Pin

Default value: 00h

Access: RO

This register is used to tell the drivers or operation systems that which interrupt pin the IDE controller uses. The value of this register is read only and depends on the IDE controller's operating mode. If either IDE channel operates in Native mode, then this register will be read as "1", else it will be read as "0" to indicate no interrupt pin is used.

Register 3Eh~3Fh Reserved

Register 40h IDE Primary Channel/Master Drive Data Recovery Time Control

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Test mode for internal use only** 0: Normal mode 1: Test mode This test mode for recovery and active timer counter.
6	R/W	**Test mode for internal use only** 0: Normal mode 1: Test mode This test mode for prefetch byte counter.
5:4	RO	**Reserved**
3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 41h IDE Primary Channel/Master Drive Data Active Time Control

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Ultra DMA Mode Control** 0: Disable 1: Enable
6:4	R/W	**Ultra DMA 33/66 cycle time Select** 000: Reserved 001: Cycle time of 2 CLK clocks for data out 010: Cycle time of 3 CLK clocks for data out 011: Cycle time of 4 CLK clocks for data out 100: Cycle time of 5 CLK clocks for data out 101: Cycle time of 6 CLK clocks for data out 110: Cycle time of 7 CLK clocks for data out 111: Cycle time of 8 CLK clocks for data out Note : 2 CLK = 1 PCICLK
3	RO	Reserved
2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 42h IDE Primary Channel/Slave Drive Data Recovery Time Control

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:4	RO	**Reserved**

3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 43h IDE Primary Channel/Slave Drive Data Active Time Control

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Ultra DMA Mode Control** 0: Disable 1: Enable
6:4	R/W	**Ultra DMA 33/66 cycle time Select** 000: Reserved 001: Cycle time of 2 CLK clocks for data out 010: Cycle time of 3 CLK clocks for data out 011: Cycle time of 4 CLK clocks for data out 100: Cycle time of 5 CLK clocks for data out 101: Cycle time of 6 CLK clocks for data out 110: Cycle time of 7 CLK clocks for data out 111: Cycle time of 8 CLK clocks for data out Note : 2 CLK = 1 PCICLK
3	RO	**Reserved**
2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 44h IDE Secondary Channel/Master Drive Data Recovery Time Control

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:4	RO	**Reserved**
3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 45h IDE Secondary Channel/Master Drive Data Active Time Control

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Ultra DMA Mode Control** 0: Disable 1: Enable
6:4	R/W	**Ultra DMA 33/66 cycle time Select** 000: Reserved 001: Cycle time of 2 CLK clocks for data out 010: Cycle time of 3 CLK clocks for data out 011: Cycle time of 4 CLK clocks for data out 100: Cycle time of 5 CLK clocks for data out 101: Cycle time of 6 CLK clocks for data out 110: Cycle time of 7 CLK clocks for data out 111: Cycle time of 8 CLK clocks for data out Note : 2 CLK = 1 PCICLK
3	RO	**Reserved**

2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 46h IDE Secondary Channel/Slave Drive Data Recovery Time Control

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:4	RO	**Reserved**
3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 47h IDE Secondary Channel/Slave Drive Data Active Time Control

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Ultra DMA Mode Control** 0: Disable 1: Enable

6:4	R/W	**Ultra DMA 33/66 cycle time Select** 000: Reserved 001: Cycle time of 2 CLK clocks for data out 010: Cycle time of 3 CLK clocks for data out 011: Cycle time of 4 CLK clocks for data out 100: Cycle time of 5 CLK clocks for data out 101: Cycle time of 6 CLK clocks for data out 110: Cycle time of 7 CLK clocks for data out 111: Cycle time of 8 CLK clocks for data out Note : 2 CLK = 1 PCICLK
3	RO	**Reserved**
2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 48h IDE Status Register

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:6	RO	**Reserved**
5	RO	**Channel 1 Cable Type Status (via CBLIDB signal)** 0: 80 pins cable type 1: 40 pins cable type
4	RO	**Channel 0 Cable Type Status (via CBLIDA signal)** 0: 80 pins cable type 1: 40 pins cable type

3:2	R/W	**PCI Read Request Threshold Setting** 00: PCI Request asserted when FIFO is 62.5% full during prefetch cycles. 01: PCI Request asserted when FIFO is 50.0% full during prefetch cycles. 10: PCI Request asserted when FIFO is 25.0% full during prefetch cycles. 11: PCI Request asserted when FIFO is 12.5% full during prefetch cycles.
1:0	R/W	**PCI Write Request Threshold Setting** 00: PCI Request asserted when FIFO is 12.5% full during prefetch cycles. 01: PCI Request asserted when FIFO is 25.0% full during prefetch cycles. 10: PCI Request asserted when FIFO is 50.0% full during prefetch cycles. 11: PCI Request asserted when FIFO is 62.5% full during prefetch cycles.

Register 49h Reserved

Register 4Ah IDE General Control Register 0

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Bus Master generates PCI burst cycles Control** 0: Disable 1: Enable
6	R/W	**Reserved**
5	R/W	**Fast post-write control** 0: Disabled 1: Enabled (Recommended)

4	R/W	**Test Mode for internal use only** 0: Normal Mode 1: Test Mode When this bit is set 1, the IRQ of HD drive would pass direct to 8259. On the others hand, IDE would gate IRQ until IDE FIFO is empty under abnormal operation.
3	R/W	**Reserved**
2	R/W	**IDE Channel 1 Enable Bit** 0: Disabled 1: Enabled
1	R/W	**IDE Channel 0 Enable Bit** 0: Disabled 1: Enabled
0	R/W	**Reserved**

Register 4Bh IDE General Control register 1

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Enable Postwrite of the Slave Drive in Channel 1** 0: Disabled 1: Enabled
6	R/W	**Enable Postwrite of the Master Drive in Channel 1** 0: Disabled 1: Enabled
5	R/W	**Enable Postwrite of the Slave Drive in Channel 0** 0: Disabled 1: Enabled
4	R/W	**Enable Postwrite of the Master Drive in Channel 0** 0: Disabled 1: Enabled

3	R/W	**Enable Prefetch of the Slave Drive in Channel 1** 0: Disabled 1: Enabled
2	R/W	**Enable Prefetch of the Master Drive in Channel 1** 0: Disabled 1: Enabled
1	R/W	**Enable Prefetch of the Slave Drive in Channel 0** 0: Disabled 1: Enabled
0	R/W	**Enable Prefetch of the Master Drive in Channel 0** 0: Disabled 1: Enabled

(Following two 16-bit wide registers define the prefetching length of each IDE channel respectively.)

Register 4Ch~4Dh Prefetch Count of Primary Channel

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:0	R/W	**Prefetch Count of Primary Channel** The Count (in bytes) of IDE prefetch. The maximum value can be programmed is 512. (Default value is 512)

Register 4Eh~4Fh Prefetch Count of Secondary Channel

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:0	R/W	**Prefetch Count of Secondary Channel** The Count (in bytes) of IDE prefetch. The maximum value can be programmed is 512. (Default value is 512)

Register 50h~51h Reserved

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:0	R/W	**Reserved**

Register 52h IDE Miscellaneous Control Register

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:5	RO	**Reserved**
4	R/W	**IDE I/O Buffer Driving Strength Control** 0: Strong 1: Weak
3	R/W	**Reserved**
2	R/W	**Control of IDE Programmable Indicator (Reg. 09 bit 1 and 3)** 0: IDE register 09 bit 1 and 3 would be read as "1¡ ¨ 1: IDE register 09 bit 1 and 3 would be read as "0", and register 09 bit 0 and 2 would be read as "0". It means IDE controller can only operate in Compatibility mode.
1	R/W	**Test Mode for internal use only** 0 : Normal Mode 1 : Test Mode If this bit is set as 1, IDE controller would reset IDE FIFO pointer when 8 bit command is forward to HDs driver. This bit would work on the condition that the transferring byte count of OS is not equal to the byte count received by HDs driver.
0	R/W	**Test mode for Internal use only** 0: The value of register 3D bit 0 would depend on both channels' operating mode. 1: The value of register 3D bit 0 would be read as "0".

8.1 Offset Registers for PCI Bus Master IDE Control Registers

The PCI Bus master IDE Registers use 16 bytes of I/O Space. These registers can be accessed through I/O R/W to the address defined in the Bus Master IDE control register Base Address in the PCI IDE Configuration space. The base address is also defined in Register 20h~23h of PCI IDE configuration space.

Register 00h Bus Master Primary IDE Command Register

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:4	RO	**Reserved. Return 0 on reads.**
6:5	R/W	**Read or Write Control** This bit defines the R/W control of the bus master transfer. When set to zero, PCI bus master reads are conducted. When set to one, PCI bus master writes are conducted.
2:1	RO	**Reserved**
0	R/W	**Start/Stop Bus Master** The SiS Chip built-in IDE Controller enables its bus master operation whenever it detects this bit changing from a zero to a one. The operation can be halted by writing zero to this bit.

Register 01h Reserved

Register 02h Bus Master Primary IDE Status Register

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	RO	**Simplex Only** This bit is hardwired to zero to indicate that both bus master channels can be operated at a time.
6	R/W	**Drive 1 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 1 for this channel is capable of DMA transfers.
5	R/W	**Drive 0 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 0 for this channel is capable of DMA transfers.
4:3	RO	**Reserved. Return 0 on reads**
2	R/W	**Interrupt** The bit is set by the rising edge of the IDE interrupt line to indicate that all data transferred from the drive is visible in the system memory. Writing a '1' to this bit can reset it.
1	RO	**Error** This bit is set when the IDE controller encounters an error during data transferring to/from memory.

0	R/W	**Bus Master IDE Device Active** This bit is set when the start bit in the command register is set. It can be cleared when the last transfer of a region is performed, or the start bit is reset.

Register 03h Reserved

Register 04h~07h Bus Master Primary IDE PRD Table Pointer Register

This 32-bit register contains address pointing to the starting address of the PRD table.

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:2	R/W	**Base Address of the PRD Table**
1:0	R/W	**Reserved**

***PRD: Physical Region Descriptor**

Register 08h Bus Master Secondary IDE Command Register

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:4	RO	**Reserved. Return 0 on reads.**
3	R/W	**Read or Write Control.** This bit defines the R/W control of the bus master transfer. When set to "0", PCI bus master reads are conducted. When set to "1", PCI bus master writes are conducted.
2:1	RO	**Reserved**
0	R/W	**Start/Stop Bus Master** The SiS chip built-in IDE Controller enables its bus master operation whenever it detects this bit changing from a zero to a one. The operation can be halted by writing a zero to this bit.

Register 09h Reserved

Register 0Ah Bus Master Secondary IDE Status Register

Default Value: 00h

Access: Read/Write

Bit	Access	Description

7	RO	**Simplex Only** This bit is hardwired to zero to indicate that both bus master channels can be operated at a time.
6	R/W	**Drive 1 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 1 for this channel is capable of DMA transfers.
5	R/W	**Drive 0 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 0 for this channel is capable of DMA transfers**.**
4:3	RO	**Reserved. Return 0 on reads**
2	R/W	**Interrupt** The bit is set by the rising edge of the IDE interrupt line to indicate that all data transferred from the drive is visible in the system memory. Writing a '1' to this bit can reset it.
1	RO	**Error** This bit is set when the IDE controller encounters an error during data transferring to/from memory.
0	R/W	**Bus Master IDE Device Active** This bit is set when the start bit in the command register is set. It can be cleared when the last transfer of a region is performed, or the start bit is reset.

Register 0Bh Reserved

Register 0Ch~0Fh Bus Master Secondary IDE PRD Table Pointer Register

This 32-bit register contains address pointing to the starting address of the PRD table.

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:2	R/W	**Base Address of the PRD Table**
1:0	R/W	**Reserved**

*PRD: Physical Region Descriptor

9 Register Summary / Description – Graphics

9.1 General Registers

Miscellaneous Output Registers

Register Type: Read/Write

Read Port: 3CC

Write Port: 3C2

Default: 00h

D7 Vertical Sync Polarity

0: Select 'positive vertical sync'

1: Select 'negative vertical sync'

D6 Horizontal Sync Polarity

0: Select 'positive horizontal sync'

1: Select 'negative horizontal sync'

Table 9.1-1 Sync Polarity vs. Vertical Screen Resolution

D7	D6	EGA	VGA
0	0	200 Lines	Invalid
0	1	350 Lines	400 Lines
1	0	Invalid	350 Lines
1	1	Invalid	480 Lines

D5 Odd/Even Page

0: Select low page of memory

1: Select high page of memory

D4 Reserved

D[3:2] Clock Select

Table 9.1-2 Table for Video Clock Selection

D3	D2	DCLK
0	0	25.175 MHz
0	1	28.322 MHz

1	0	Don't Care
1	1	For internal clock generator.

D1 Display RAM Enable

0: Disable processor access to video RAM

1: Enable processor access to video RAM

D0 I/O Address Select

0: Sets addresses for monochrome emulation

1: Sets addresses for color graphics emulation

Feature Control Register

Register Type: Read/Write

Read Port: 3CA

Write Port: 3BA/3DA

Default: 00h

D[7:4] Reserved (0)

D3 Vertical Sync Select

0: Normal Vertical Sync output to monitor

1: [Vertical Sync OR Vertical Display Enable] output to monitor

D[2:0] Reserved (0)

Input Status Register 0

Register Type: Read only

Read Port: 3C2

Default: 00h

D7 Vertical Retrace Interrupt Pending

0: Cleared

1: Pending

D[6:5] Reserved

D4 Switch Sense

D[3:0] Reserved

Input Status Register 1

Register Type: Read only

Read Port: 3BA/3DA

Default: 00h

D[7:6] Reserved

D[5:4] Diagnostic

Table 9.1-3 Table for Video Read-back Through Diagnostic Bit (I)

Color Plane Enable Register		Input Status Register 1	
D5	**D4**	**D5**	**D4**
0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Unused	Unused

Table 9.1-4 Table for Video Read-back Through Diagnostic Bit (II)

Color Plane Enable Register		Input Status Register 1	
D5	**D4**	**D5**	**D4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

D3 Vertical Trace

0: Inactive

1: Active

D[2:1] Reserved

D0 Display Enable Not

0: Display period

1: Retrace period

VGA Enable Register

Register Type: Read/Write

Read/Write Port: 3C3

Default: 00h

D0 VGA Enable

0: Disable

1: Enable

Segment Selection Register 0

Register Type: Read/Write

Read/Write Port: 3CD

Default: 00h

D[7:0] Segment Selection Write Bit[7:0]

Segment Selection Register 1

Register Type: Read/Write

Read/Write Port: 3CB

Default: 00h

D[7:0] Segment Selection Read Bit[7:0]

9.2 CRT Controller Registers

CRT Controller Index Register

Register Type: Read/Write

Read/Write Port: 3B4/3D4

Default: 00h

D[7:0] CRT Controller Index

- 00h ~ 18h for standard VGA
- 19h ~ 26h for SiS extended CRT registers

Table 9.2-1 Table of CRT Controller Registers

Index (3B4/3D4)	CRT Controller Registers (3B5/3D5)
00h	Horizontal Total
01h	Horizontal Display Enable End
02h	Horizontal Blank Start
03h	Horizontal Blank End
04h	Horizontal Retrace Start
05h	Horizontal Retrace End

06h	Vertical Total
07h	Overflow Register
08h	Preset Row Scan
09h	Max Scan Line/Text Character Height
0Ah	Text Cursor Start
0Bh	Text Cursor End
0Ch	Screen Start Address High
0Dh	Screen Start Address Low
0Eh	Text Cursor Location High
0Fh	Text Cursor Location Low
10h	Vertical Retrace Start
11h	Vertical Retrace End
12h	Vertical Display Enable End
13h	Screen Offset
14h	Underline Location
15h	Vertical Blank Start
16h	Vertical Blank End
17h	Mode Control
18h	Line Compare
1Bh	CRT horizontal counter read-back
1Ch	CRT vertical counter read back
1Dh	CRT overflow counter read back
22h	Graphics Data Latch Read-back Register
24h	Attribute Controller Toggle Read-back Register
26h	Attribute Controller Index Read-back Register

CR0: Horizontal Total

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 00h

Default: 00h

D[7:0] Horizontal Total Bit[7:0]

CR1: Horizontal Display Enable End

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 01h

Default: 00h

D[7:0] Horizontal Display Enable End Bit[7:0]

CR2: Horizontal Blank Start

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 02h

Default: 00h

D[7:0] Horizontal Blank Start Bit[7:0]

CR3: Horizontal Blank End

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 03h

Default: 00h

D7 Reserved

D[6:5] Display Skew Control Bit[1:0]

00: No skew

01: Skew 1 character

10: Skew 2 characters

11: Skew 3 characters

D[4:0] Horizontal Blank End Bit[4:0]

CR4: Horizontal Retrace Start

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 04h

Default: 00h

D[7:0] Horizontal Retrace Start Bit[7:0]

CR5: Horizontal Retrace End

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 05h

Default: 00h

D7 Horizontal Blank End Bit[5]

D[6:5] Horizontal Retrace Delay Bit[1:0]

00: Skew 0 character clock

01: Skew 1 character clock

10: Skew 2 character clocks

11: Skew 3 character clocks

D[4:0] Horizontal Retrace End Bit[4:0]

CR6: Vertical Total

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 06h

Default: 00h

D[7:0] Vertical Total Bit[7:0]

CR7: Overflow Register

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 07h

Default: 00h

D7 Vertical Retrace Start Bit[9]

D6 Vertical Display Enable End Bit[9]

D5 Vertical Total Bit[9]

D4 Line Compare Bit[8]

D3 Vertical Blank Start Bit[8]

D2 Vertical Retrace Start Bit[8]

D1 Vertical Display Enable End Bit[8]

D0 Vertical Total Bit[8]

CR8: Preset Row Scan

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 08h

Default: 00h

D7 Reserved

D[6:5] Byte Panning Control Bit[1:0]

D[4:0] Preset Row Scan Bit[4:0]

CR9: Maximum Scan Line/Text Character Height

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 09h

Default: 00h

D7 Double Scan

0: Disable

1: Enable 400 lines display

D6 Line Compare Bit[9]

D5 Vertical Blank Start Bit[9]

D[4:0] Character Cell Height Bit[4:0]

CRA: Text Cursor Start

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 0Ah

Default: 00h

D[7:6] Reserved

D5 Text Cursor Off

0: Text Cursor On

1: Text Cursor Off

D[4:0] Text Cursor Start Bit[4:0]

CRB: Text Cursor End

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 0Bh

Default: 00h

D7 Reserved

D[6:5] Text Cursor Skew

00: No skew

01: Skew one character clock

10: Skew two character clocks

11: Skew three character clocks

D[4:0] Text Cursor End Bit[4:0]

CRC: Screen Start Address High

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 0Ch

Default: 00h

D[7:0] Screen Start Address Bit[15:8]

CRD: Screen Start Address Low

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 0Dh

Default: 00h

D[7:0] Screen Start Address Bit[7:0]

CRE: Text Cursor Location High

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 0Eh

Default: 00h

D[7:0] Text Cursor Location Bit[15:8]

CRF: Text Cursor Location Low

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 0Fh

Default: 00h

D[7:0] Text Cursor Location Bit[7:0]

CR10: Vertical Retrace Start

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 10h

Default: 00h

D[7:0] Vertical Retrace Start Bit[7:0]

CR11: Vertical Retrace End

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 11h

Default: 00h

D7 Write Protect for CR0 to CR7

0: Disable Write Protect

1: Enable Write Protect

D6 Alternate Refresh Rate

0: Selects three refresh cycles per scanline

1: Selects five refresh cycles per scanline

D5 Vertical Interrupt Enable

0: Enable

1: Disable

D4 Vertical Interrupt Clear

0: Clear

1: Not Clear

D[3:0] Vertical Retrace End Bit[3:0]

CR12: Vertical Display Enable End

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 12h

Default: 00h

D[7:0] Vertical Display Enable End Bit[7:0]

CR13: Screen Offset

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 13h

Default: 00h

D[7:0] Screen Offset Bit[7:0]

CR14: Underline Location Register

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 14h

Default: 00h

D7 Reserved

D6 Double-Word Mode Enable

0: Disable

1: Enable

D5 Count by 4

0: Disable

1: Enable

D[4:0] Underline Location Bit[4:0]

CR15: Vertical Blank Start

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 15h

Default: 00h

D[7:0] Vertical Blank Start Bit[7:0]

CR16: Vertical Blank End

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 16h

Default: 00h

D[7:0] Vertical Blank End Bit[7:0]

CR17: Mode Control Register

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 17h

Default: 00h

D7 Hardware Reset

0: Disable horizontal and vertical retrace outputs

1: Enable horizontal and vertical retrace outputs

D6 Word/Byte Address Mode

0: Set the memory address mode to word

1: Set the memory address mode to byte

D5 Address Wrap

0: Disable the full 256K of memory

1: Enable the full 256K of memory

D4 Reserved

D3 Count by Two

0: Byte refresh

1: Word refresh

D2 Horizontal Retrace Select

0: Normal

1: Double Scan

D1 RA1 replace MA14

0: Enable

1: Disable

D0 RA0 replace MA13

0: Enable

1: Disable

CR18: Line Compare Register

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 18h

Default: 00h

D[7:0] Line Compare Bit[7:0]

CR1B: CRT Horizontal Counter Read Back

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 1Bh

Default: xxh

D[7:0] CRT horizontal counter bit[7:0]

CR1C: CRT Vertical Counter Read Back

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 1Ch

Default: xxh

D[7:0] CRT vertical counter bit[7:0]

CR1D: CRT Overflow Counter Read Back

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 1Dh

Default: xxh

D[7:5] Reserved

D4 CRT horizontal counter bit 8

D3 Reserved

D[2:0] CRT vertical counter bit[10:8]

Note: The horizontal and vertical counter value will be latched when read register CR20. So the three registers value should be read after read CR20.

CR1E: Extended Signature Read-Back Register 2

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 1Eh

Default: xxh

D[7:0] Signature read-back bit[23:16]

CR20: CRT Counter Trigger Port

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 20h

Default: xxh

D[7:0] Reserved

CR24: Attribute Controller Toggle Read-back Register

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 24h

Default: xxh

D7 Attribute Controller Toggle

D[6:0] Reserved

CR26: Attribute Controller Index Read-back Register

Register Type: Read Only

Read/Write Port: 3B5/3D5, Index 26h

Default: xxh

D[7:6] Reserved

D5 Video Enable

D[4:0] Attribute Controller Index bit[8:4]

9.3 Sequencer Registers

Sequencer Index Register

Register Type: Read/Write

Read/Write Port: 3C4

Default: 00h

D[7:6] Reserved

D[5:0] Sequencer Index Bit[5:0]

Table 9.3-1 Table of Sequencer Registers

Index (3C4)	Sequencer Register (3C5)
00	Reset Register
01	Clock Mode
02	Color Plane Write Enable
03	Character Generator Select
04	Memory Mode

SR0: Reset Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 00h

Default: 00h

D[7:2] Reserved

D1 Synchronous reset

0: Reset

1: Normal

D0 Asynchronous reset

0: Reset

1: Normal

SR1: Clock Mode Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 01h

Default: 00h

D[7:6] Reserved

D5 Screen Off

0: Display On

1: Display Off

D4 Shifter Load 32 enable

0: Disable

1: Data shifter loaded every 4th Character Clock

D3 Dot Clock Divide by 2 enable
0: Disable
1: Video Clock is divided by 2 to generate Dot Clock

D2 Shifter Load 16 (while D4=0)
0: Disable
1: Data shifter loaded every 2nd Character Clock

D1 Reserved

D0 8/9 Dot Clock
0: Dot Clock is divided by 9 to generate Character Clock
1: Dot Clock is divided by 8 to generate Character Clock

SR2: Color Plane Write Enable Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 02h

Default: 00h

D[7:4] Reserved

D3 Plane 3 write enable
0: Disable
1: Enable

D2 Plane 2 write enable
0: Disable
1: Enable

D1 Plane 1 write enable
0: Disable
1: Enable

D0 Plane 0 write enable
0: Disable
1: Enable

SR3: Character Generator Select Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 03h

Default: 00h

D[7:6] Reserved

D5 Character generator table B select Bit[2]

D4 Character generator table A select Bit[2]

D[3:2] Character generator table B select Bit[1:0]

D[1:0] Character generator table A select Bit[1:0]

Table 9.3-2 Table of Selecting Active Character Generator

D5	D3	D2	Used when text attribute bit 3 is 1
D4	D1	D0	Used when text attribute bit 3 is 0
0	0	0	Character Table 1
0	0	1	Character Table 2
0	1	0	Character Table 3
0	1	1	Character Table 4
1	0	0	Character Table 5 (VGA only)
1	0	1	Character Table 6 (VGA only)
1	1	0	Character Table 7 (VGA only)
1	1	1	Character Table 8 (VGA only)

SR4: Memory Mode Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 04h

Default: 00h

D[7:4] Reserved

D3 Chain-4 Mode enable

0: Disable

1: Enable

D2 Odd/Even Mode enable

0: Enable

1: Disable

D1 Extended Memory

0: Select 64K

1: Select 256K

D0 Reserved

9.4 Graphics Controller Registers

Graphics Controller Index Register

Register Type: Read/Write

Read/Write Port: 3CE

Default: 00h

D[7:4] Reserved

D[3:0] Graphics Controller Index Bit[3:0]

Table 9.4-1 Table of Graphics Controller Registers

Index (3CE)	Graphics Controller Register (3CF)
00	Set/Reset Register
01	Set/Reset Enable Register
02	Color Compare Register
03	Data Rotate & Function Select
04	Read Plane Select Register
05	Mode Register
06	Miscellaneous Register
07	Color Don't Care Register
08	Bit Mask Register

GR0: Set/Reset Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 00h

Default: 00h

D[7:4] Reserved

D3 Set/Reset Map for plane 3

D2 Set/Reset Map for plane 2

D1 Set/Reset Map for plane 1

D0 Set/Reset Map for plane 0

GR1: Set/Reset Enable Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 01h

Default: 00h

D[7:4] Reserved

D3 Enable Set/Reset for plane 3

0: Disable

1: Enable

D2 Enable Set/Reset for plane 2

0: Disable

1: Enable

D1 Enable Set/Reset for plane 1

0: Disable

1: Enable

D0 Enable Set/Reset for plane 0

0: Disable

1: Enable

GR2: Color Compare Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 02h

Default: 00h

D[7:4] Reserved

D3 Color Compare Map for plane 3

D2 Color Compare Map for plane 2

D1 Color Compare Map for plane 1

D0 Color Compare Map for plane 0

GR3: Data Rotate/Function Select Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 03h

Default: 00h

D[7:5] Reserved

D[4:3] Function Select

Table 9.4-2 Table of Function Select

D4	D3	Function

0	0	write data unmodified
0	1	write data AND processor latches
1	0	write data OR processor latches
1	1	write data XOR processor latches

D[2:0] Rotate Count

Table 9.4-3 Table of Rotate Count

D2	D1	D0	Right Rotation
0	0	0	none
0	0	1	1 bits
0	1	0	2 bits
0	1	1	3 bits
1	0	0	4 bits
1	0	1	5 bits
1	1	0	6 bits
1	1	1	7 bits

GR4: Read Plane Select Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 04h

Default: 00h

D[7:2] Reserved

D[1:0] Read Plane Select bit 1, 0

00: Plane 0

01: Plane 1

10: Plane 2

11: Plane 3

GR5: Mode Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 05h

Default: 00h

D7 Reserved

D6 256-color Mode

0: Disable

1: Enable

D5 Shift Register Mode

0: Configure shift register to be EGA compatible

1: Configure shift register to be CGA compatible

D4 Odd/Even Addressing Mode enable

0: Disable

1: Enable

D3 Read Mode

0: Map Select Read

1: Color Compare Read

D2 Reserved

D[1:0] Write mode

Table 9.4-4 Table for Write Mode

D1	D0	Mode Selected
0	0	Write Mode 0: Direct processor write (Data Rotate, Set/Reset may apply).
0	1	Write Mode 1: Use content of latches as write data.
1	0	Write Mode 2: Color Plane n(0-3) is filled with the value of bit m in the processor write data.
1	1	Write Mode 3: Color Plane n(0-3) is filled with 8 bits of the color value contained in the Set/Reset Register for that plane. The Enable Set/Reset Register is not effective. Processor data will be AND with Bit Mask Register content to form new bit mask pattern. (data rotate may apply).

GR6: Miscellaneous Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 06h

Default: 00h

D[7:4] Reserved

D[3:2] Memory Address Select

Table 9.4-5 Table of Memory Address Select

D3	D2	Address range
0	0	A0000 to BFFFF
0	1	A0000 to AFFFF
1	0	B0000 to B7FFF
1	1	B8000 to BFFFF

D1 Chain Odd And Even Maps

0: Disable

1: Enable

D0 Graphics Mode Enable

0: Select alphanumeric mode

1: Select graphics mode

GR7: Color Don't Care Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 07h

Default: 00h

D[7:4] Reserved

D3 Plane 3 Don't Care

0: Disable color comparison

1: Enable color comparison

D2 Plane 2 Don't Care

0: Disable color comparison

1: Enable color comparison

D1 Plane 1 Don't Care

0: Disable color comparison

1: Enable color comparison

D0 Plane 0 Don't Care

0: Disable color comparison

1: Enable color comparison

GR8: Bit Mask Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 08h

Default: 00h

D[7:0] Bit Mask Enable Bit[7:0]

9.5 Attribute Controller and Video DAC Registers

Attribute Controller Index Register

Register Type: Read/Write

Read Port: 3C0

Write Port: 3C0

Default: 00h

D[7:6] Reserved

D5 Palette Address Source

0: From CPU

1: From CRT

D[4:0] Attribute Controller Index Bit[4:0] (00h-14h)

Table 9.5-1 Table of Attribute Controller Registers

Index (3C0)	Attribute Controller Register (3C0)
00h	Color Palette Register 0
01h	Color Palette Register 1
02h	Color Palette Register 2
03h	Color Palette Register 3
04h	Color Palette Register 4
05h	Color Palette Register 5
06h	Color Palette Register 6
07h	Color Palette Register 7
08h	Color Palette Register 8
09h	Color Palette Register 9
0Ah	Color Palette Register 10
0Bh	Color Palette Register 11
0Ch	Color Palette Register 12
0Dh	Color Palette Register 13

0Eh	Color Palette Register 14
0Fh	Color Palette Register 15
10h	Mode Control Register
11h	Screen Border Color
12h	Color Plane Enable Register
13h	Pixel Panning Register
14h	Color Select Register (VGA)

AR0~ARF: Palette Registers

Register Type: Read/Write

Read Port: 3C1, Index 00h ~ 0Fh

Write Port: 3C0, Index 00h ~ 0Fh

Default: 00h

D[7:6] Reserved

D[5:0] Palette Entries

AR10: Mode Control Register

Register Type: Read/Write

Read Port: 3C1, Index 10h

Write Port: 3C0, Index 10h

Default: 00h

D7 P4, P5 Source Select

0: AR0-F Bit[5:4] are used as the source for the Lookup Table Address Bit[5:4]

1: AR14 Bit[1:0] are used as the source for the Lookup Table Address Bit[5:4]

D6 Pixel Double Clock Select

0: The pixels are clocked at every clock cycle

1: The pixels are clocked at every other clock cycle

D5 PEL Panning Compatibility with Line Compare

0: Disable

1: Enable

D4 Reserved

D3 Background Intensity or Blink enable (while the Character Attribute D7=1)

0: Background Intensity attribute enable

1: Background Blink attribute enable

D2 Line Graphics enable

0: The ninth bit of nine-bit-wide character cell will be the same as the background.

1: The ninth bit of nine-bit-wide character cell will be made be the same as the eighth bit for character codes in the range C0h through DFh.

D1 Display Type

0: The contents of the Attribute byte are treated as color attribute.

1: The contents of the Attribute byte are treated as MDA-compatible attribute.

D0 Graphics/Text Mode

0: The Attribute Controller will function in text mode.

1: The Attribute Controller will function in graphics mode.

AR11: Screen Border Color

Register Type: Read/Write

Read Port: 3C1, Index 11h

Write Port: 3C0, Index 11h

Default: 00h

D[7:6] Reserved

D[5:0] Palette Entry

AR12: Color Plane Enable Register

Register Type: Read/Write

Read Port: 3C1, Index 12h

Write Port: 3C0, Index 12h

Default: 00h

D[7:6] Reserved

D[5:4] Display Status MUX Bit[1:0]

These bits select two of the eight bits color outputs to be available in the status register. The output color combinations available on the status bits are as follows:

Table 9.5-2 Table for Video Read-back Through Diagnostic Bit (I)

Color Plane Enable Register		Input Status Register 1 (Refer to 7.1.4)	
D5	D4	D5	D4

0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Unused	Unused

Table 9.5-3 Table for Video Read-back Through Diagnostic Bit (II)

Color Plane Enable Register		Input Status Register 1 (Refer to 7.1.4)	
D5	D4	D5	D4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

D[3:0] Enable Color Plane Bit[3:0]

AR13: Pixel Panning Register

Register Type: Read/Write

Read Port: 3C1, Index 13h

Write Port: 3C0, Index 13h

Default: 00h

D[7:4] Reserved

D[3:0] Pixel Pan Bit[3:0]

This field specifies the number of pixels the display data will be shifted to the left. This field is interpreted as indicated in the following table:

Table 9.5-4 Table of Pixel Panning

D3	D2	D1	D0	Monochrome Text	VGA Mode 13	All others
0	0	0	0	8	0	0
0	0	0	1	0	Invalid	1
0	0	1	0	1	1	2
0	0	1	1	2	Invalid	3
0	1	0	0	3	2	4
0	1	0	1	4	Invalid	5

0	1	1	0	5	3	6
0	1	1	1	6	Invalid	7
1	0	0	0	7	Invalid	Invalid
1	0	0	1	Invalid	Invalid	Invalid
1	0	1	0	Invalid	Invalid	Invalid
1	0	1	1	Invalid	Invalid	Invalid
1	1	0	0	Invalid	Invalid	Invalid
1	1	0	1	Invalid	Invalid	Invalid
1	1	1	0	Invalid	Invalid	Invalid
1	1	1	1	Invalid	Invalid	Invalid

AR14: Color Select Register

Register Type: Read/Write

Read Port: 3C1, Index 14h

Write Port: 3C0, Index 14h

Default: 00h

D[7:4] Reserved

D[3:2] Color Bit[7:6]

These two bits are concatenated with the six bits from the Palette Register to form the address into the LUT and to drive P[7:6].

D[1:0] Color Bit[5:4]

If AR10 D7 is programmed to a '1', these two bits replace the corresponding two bits from the Palette Register to form the address into the LUT and to drive P[5:4]. If AR10 D7 is programmed to a '0', these two bits are ignored.

9.6 Color Registers

DAC Status Register

Register Type: Read Only

Read Port: 3C7

Default: 00h

D[7:2] Reserved

D[1:0] DAC State Bit[1:0]

00: Write Operation in progress

11: Read Operation in progress

DAC Index Register (Read Mode)

Register Type: Write Only

Write Port: 3C7

Default: 00h

D[7:0] DAC Index Bit[7:0]

DAC Index Register (Write Mode)

Register Type: Read/Write

Read/Write Port: 3C8

Default: 00h

D[7:0] DAC Index Bit[7:0]

DAC Data Register

Register Type: Read/Write

Read/Write Port: 3C9

Default: 00h

When SR7 D2 = 1

D[7:6] Reserved

D[5:0] DAC Data [5:0]

Before writing to this register, 3C8h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue values for the DAC entry are written. After the third value is written, the values are transferred to the LUT and the DAC index is incremented in case new values for the next DAC index are to be written.

Before reading from this register, 3C7h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue value for the DAC entry may be read from this DAC index. After the third value is read, the DAC index is incremented in case the value for the next DAC index to be read.

When SR7 D2 = 0

D[7:0] DAC Data [7:0]

When SR7 D2 = 0, the 24-bit LUT is enabled. This LUT can translate the R, G, B values into new R, G, B values independently. This LUT can be used for performing GAMMA correction function. The programming procedure is same as standard LUT when SR7 D2 = 1.

PEL Mask Register

Register Type: Read/Write

Read/Write Port: 3C6

Default: 00h

D[7:0] Pixel Mask Bit[7:0]

This field is the Pixel Mask for the palette DAC. If a bit in this field is programmed to '0', the corresponding bit in the pixel data will be ignored in looking up an entry in the LUT.

9.7 Extended Registers

Register Type: Read/Write

Read/Write Port: 3C4

Default: 00h

D[7:6] Reserved

D[5:0] Extended Register Index Bit[5:0] (05h ~ 3Fh)

Table 9.7-1 Table of Extended Registers

Index (3C4)	Extended Enhanced Register (3C5)
05h	Extended Password/Identification Register
06h	Extended graphics mode register
07h	RAMDAC control register
08h	CRT threshold register I
09h	CRT threshold register II
0Ah	Extended vertical overflow register
0Bh	Extended horizontal overflow register I
0Ch	Extended horizontal overflow register II
0Dh	Extended CRT starting address register
0Eh	Extended CRT pitch register
0Fh	CRT misc. control register
10h	Display line width register
11h	DDC register
12h	Reserved
13h	Reserved

14h	Reserved
15h	Reserved
16h	Reserved
17h	Reserved
18h	Reserved
19h	Reserved
1Ah	Reserved
1Bh	Reserved
1Ch	Reserved
1Dh	Segment Selection Overflow Register
1Eh	Module enable register
1Fh	Power management register
20h	GUI address decoder setting register
21h	GUI HostBus state machine setting register
22h	GUI HostBus controller timing register
23h	GUI HostBus timer register I
24h	Reserved
25h	Reserved
26h	Turbo Queue base address register
27h	Turbo Queue control register
28h	Reserved
29h	Reserved
2Ah	Reserved
2Bh	Extended DCLK clock generator register I
2Ch	Extended DCLK clock generator register II
2Dh	Extended DCLK clock generator register III
2Eh	Extended ECLK clock generator register I
2Fh	Extended ECLK clock generator register II
30h	Extended ECLK clock generator register III
31h	Extended clock generator misc. register
32h	Extended clock source selection register

33h	Reserved
34h	Interrupt status register
35h	Interrupt enable register
36h	Interrupt reset register
37h	Reserved
38h	Power on trapping register I
39h	Power on trapping register II
3Ah	Power on trapping register III
3Bh	Reserved
3Ch	Synchronous reset register
3Dh	Testing enabling register
3Eh	Reserved
3Fh	Reserved

9.8 Video/TV Extended Registers

The following list is the registers of SiS540 relocate I/O:

The index port of SiS540 video playback registers is RIO+02h
The data port of SiS540 video playback registers is RIO+03h
The index port of SiS540 digital video interface registers is RIO+04h
The data port of SiS540 digital video interface registers is RIO+05h
The index port of SiS301 TV encoder registers is RIO+10h
The data port of SiS301 TV encoder registers is RIO+11h
The index port of SiS301 MacroVison™ registers is RIO+12h
The data port of SiS301 MacroVison™ registers is RIO+13h
The index port of SiS301 VGA2 registers is RIO+0014h
The data port of SiS301 VGA2 registers is RIO+0015h
The SiS301 palette address port register is RIO+0016h
The SiS301 palette data port register is RIO+0017h
"RIO" is the configuration space base address register CNFG18 D[15:0] value

9.9 Video Playback Index Registers

Register Type: Read/Write

Read/Write Port: RIO+02

Default: 00h

D[7:0] Video playback register index Bit[7:0] (00h ~ 65h)

Table 9.9-1 Table of Video Playback Registers

Index (RIO+02)	Video Playback Register (RIO+03)
00h	Password/Identification Register
01h	Video Window Horizontal Display Start Low Register
02h	Video Window Horizontal Display End Low Register
03h	Video Window Horizontal Display Start/End High Register
04h	Video Window Vertical Display Start Low Register
05h	Video Window Vertical Display End Low Register
06h	Video Window Vertical Display Start/End High Register
07h	Video Display/Y Plane Frame Buffer Starting Address Low Register
08h	Video Display/Y Plane Frame Buffer Starting Address Middle Register
09h	Video Display/Y Plane Frame Buffer Starting Address High Register
0Ah	Video U Plane Frame Buffer Starting Address Low Register
0Bh	Video U Plane Frame Buffer Starting Address Middle Register
0Ch	Video U Plane Frame Buffer Starting Address High Register
0Dh	Video V Plane Frame Buffer Starting Address Low Register
0Eh	Video V Plane Frame Buffer Starting Address Middle Register
0Fh	Video V Plane Frame Buffer Starting Address High Register
10h	Video Display/Y Plane Frame Buffer Pitch Low Register
11h	Video UV Plane Frame Buffer Pitch Low Register
12h	Video Display/Y Plane/UV Plane Frame Buffer Pitch High Register
13h	Video Display/Y Plane Frame Buffer Preset Low Register
14h	Video Display/Y Plane Frame Buffer Preset Middle

	Register
15h	Video UV Plane Frame Buffer Preset Low Register
16h	Video UV Plane Frame Buffer Preset Middle Register
17h	Video Display/Y Plane/UV Plane Frame Buffer Preset High Register
18h	Video Horizontal Post Scaling Factor Fraction Low Register
19h	Video Horizontal Post Scaling Factor Fraction High Register
1Ah	Video Vertical Scaling Factor Fraction Low Register
1Bh	Video Vertical Scaling Factor Fraction High Register
1Ch	Video Horizontal/Vertical Scaling Control Register
1Dh	Video Playback Threshold Low Value Register
1Eh	Video Playback Threshold High Value Register
1Fh	Video Playback Line Buffer Maximum Size Register
20h	Video Overlay Color Key Red Minimum Value Register
21h	Video Overlay Color Key Green Minimum Value Register
22h	Video Overlay Color Key Blue Minimum Value Register
23h	Video Overlay Color Key Red Maximum Value Register
24h	Video Overlay Color Key Green Maximum Value Register
25h	Video Overlay Color Key Blue Maximum Value Register
26h	Video Chroma Key Red/Y Minimum Value Register
27h	Video Chroma Key Green/U Minimum Value Register
28h	Video Chroma Key Blue/V Minimum Value Register
29h	Video Chroma Key Red/Y Maximum Value Register
2Ah	Video Chroma Key Green/U Maximum Value Register
2Bh	Video Chroma Key Blue/V Maximum Value Register
2Ch	Video Contrast Enhancement Mean Value Sampling Rate Factor Register
2Dh	Video Brightness Value Register
2Eh	Video Contrast Enhancement Control Register
2Fh	Video Key Overlay Operation Mode Register

30h	Video Control Miscellaneous Register 0
31h	Video Control Miscellaneous Register 1
32h	Video Control Miscellaneous Register Register 2
33h	Subpicture Frame Buffer Starting Address Low Register
34h	Subpicture Frame Buffer Starting Address Middle Register
35h	Subpicture Frame Buffer Starting Address/Preset High Register
36h	Subpicture Frame Buffer Preset Low Register
37h	Subpicture Frame Buffer Preset Middle Register
38h	Subpicture Frame Buffer Pitch Register
39h	Subpicture Horizontal Scaling Factor Fraction Low Register
3Ah	Subpicture Horizontal Scaling Factor Fraction High Register
3Bh	Subpicture Vertical Scaling Factor Fraction Low Register
3Ch	Subpicture Vertical Scaling Factor Fraction High Register
3Dh	Subpicture Horizontal/Vertical Scaling Factor Integer Register
3Eh	Subpicture Threshold Value Register
3Fh	Subpicture FIFO Maximum Size Register
40h	Subpicture Color Palette Color0 Low Register
41h	Subpicture Color Palette Color0 High Register
42h	Subpicture Color Palette Color1 Low Register
43h	Subpicture Color Palette Color1 High Register
44h	Subpicture Color Palette Color2 Low Register
45h	Subpicture Color Palette Color2 High Register
46h	Subpicture Color Palette Color3 Low Register
47h	Subpicture Color Palette Color3 High Register
48h	Subpicture Color Palette Color4 Low Register
49h	Subpicture Color Palette Color4 High Register
4Ah	Subpicture Color Palette Color5 Low Register
4Bh	Subpicture Color Palette Color5 High Register

4Ch	Subpicture Color Palette Color6 Low Register
4Dh	Subpicture Color Palette Color6 High Register
4Eh	Subpicture Color Palette Color7 Low Register
4Fh	Subpicture Color Palette Color7 High Register
50h	Subpicture Color Palette Color8 Low Register
51h	Subpicture Color Palette Color8 High Register
52h	Subpicture Color Palette Color9 Low Register
53h	Subpicture Color Palette Color9 High Register
54h	Subpicture Color Palette ColorA Low Register
55h	Subpicture Color Palette ColorA High Register
56h	Subpicture Color Palette ColorB Low Register
57h	Subpicture Color Palette ColorB High Register
58h	Subpicture Color Palette ColorC Low Register
59h	Subpicture Color Palette ColorC High Register
5Ah	Subpicture Color Palette ColorD Low Register
5Bh	Subpicture Color Palette ColorD High Register
5Ch	Subpicture Color Palette ColorE Low Register
5Dh	Subpicture Color Palette ColorE High Register
5Eh	Subpicture Color Palette ColorF Low Register
5Fh	Subpicture Color Palette ColorF High Register
60h	MPEG Auto-Flipping Control Read-Back Register 0
61h	MPEG Auto-Flipping Control Read-Back Register 1
62h	MPEG Auto-Flipping Control Read-Back Register 2
63h	MPEG Auto-Flipping Control Read-Back Register 3
64h	MPEG Auto-Flipping Field Display Vertical Scaling Factor Fraction Low Register
65h	MPEG Auto-Flipping Field Display Vertical Scaling Factor Fraction High Register

9.10 Digital Video Interface Registers

Register Type: Read/Write

Read/Write Port: RIO+04

Default: 00h

D[5:0] Digital Video Interface Register Index Bit[7:0] (00h ~ 28h)

Table 9.10-1 Table of digital video interface registers

Index (RIO+04)	digital video interface Register (RIO+05)
00h	Function Control Register
01h	Mode Selection and FIFO Threshold High
02h	Mode Selection, PCI Bus Clock and FIFO Threshold Low
03h	FIFO Stop Operation
04h	Access Memory Starting Address High
05h	Access Memory Starting Address Median
06h	Access Memory Starting Address Low
07h	Access Memory Line Offset
08h	CRT2 Horizontal Total
09h	Overflow Register
0Ah	CRT2 Horizontal Display Enable End
0Bh	CRT2 Horizontal Retrace Start
0Ch	Overflow Register
0Dh	CRT2 Horizontal Retrace End
0Eh	CRT2 Vertical Total
0Fh	CRT2 Vertical Display Enable End
10h	CRT2 Vertical Retrace Start
11h	CRT2 Vertical Retrace End and Enable CRC Check and Overflow Register
12h	Hardware Cursor Test Mode and Overflow Register
13h	Software Command Reset, Panel Link Delay Compensation, Power Saving
14h	Panel Link Horizontal Retrace Start
15h	Panel Link Horizontal Retrace End/Skew
16h	Panel Link Horizontal Display Enable Start
17h	Panel Link Horizontal Display Enable End
18h	Panel Link Vertical Retrace Start

19h	Panel Link Vertical Retrace End/Misc.
1Ah	Panel Link Control Signal and Vertical Retrace Start
1Bh	Panel Link Vertical Display Enable Start
1Ch	Panel Link Vertical Display Enable End
1Dh	Panel Link Control Signal / High Bits of Vertical Display Control
1Eh	Panel Link Vertical Scaling Factor
1Fh	Panel Link DDA Operational Number In Each Horizontal Line
20h	Overflow Register
21h	Panel Link Vertical Accumulator Length
22h	Panel Link Horizontal Scaling Factor High
23h	Panel Link Horizontal Scaling Factor Low
24h	CRT2 Enable Write Register
25h	CRT2 Vertical Retrace /Display Enable
26h	CRT2 Horizontal Counter Read Back
27h	CRT2 Vertical Counter Read Back
28h	CRT2 Horizontal Display Enable and Counter Overflow Read Back

9.11 PCI Configuration Registers

CNFG00: Configuration Register 00h

Register Type: Read

Read Port: 0000h

Default: 53001039h

D[31:16] Device ID

SiS540 Device ID is 5300h

D[15:0] Vendor ID

SiS Vendor ID is 1039h

CNFG04: Configuration Register 04h

Register Type: Read/Write

Read Port: 0004h

Default: 02200004h

D[26:25]	DEVSEL* timing (= 01, Read Only)
	00: fast
	01: medium (fixed at this value)
	10: slow
D23	Fast back-to-back capable (=0 read only)
	0: capable
	1: not capable
D21	66 MHz Capable
	0: Support 33MHz
	1: Support 66 MHz (fixed at this value)
D12	Capabilities List
	0: does not implement a list of capabilities
	1: implements a list of capabilities
D9	Fast back-to-back enable
	0: disable
	1: enable
D5	VGA Palette Snoop
	0: Disable
	1: Enable
D3	Bus Master
	0: Device is not a bus master (fixed at this value)
	1: Device is a bus master
D1	Memory Space
	0: Disable
	1: Enable
D0	I/O Space
	0: Disable
	1: Enable

CNFG08: Configuration Register 08h

Register Type: Read

Read Port: 0008h

Default: 0300000Xh

D[31:8] Class Code (= 030000h)

D[7:0] Revision ID (= 0xh)

Note: The revision ID is 01h for 540 A1 stepping.

CNFG10: Configuration Register 10h

Register Type: Read/Write

Read Port: 0010h

Default: 00000008h

D[31:0] 32-bit memory base register for 128MB linear frame buffer

CNFG14: Configuration Register 14h

Register Type: Read/Write

Read Port: 0014h

Default: 00000000h

D[31:0] 32-bit memory base register for 128KB memory mapped I/O

CNFG18: Configuration Register 18h

Register Type: Read/Write

Read Port: 0018h

Default: 00000001h

D[31:0] 32-bit I/O base register for 128 I/O space

CNFG2C: Configuration Register 2Ch

Register Type: Read/Write Once Only

Read Port: 002Ch

Default: 00000000h

D[31:16] Subsystem ID

D[15:0] Subsystem Vendor ID

CNFG30: Configuration Register 30h

Register Type: Read/Write

Read Port: 0030h

Default: 000C0000h

D[31:11] Expansion ROM Base Address

D0 ROM Enable Bit

0: Disable

1: Enable

CNFG3C: Configuration Register 3Ch

Register Type: Read/Write

Read Port: 003Ch

Default: 00000100h

D[15:8] Interrupt Pin (= 00h, Read Only)

D[7:0] Interrupt Line (= 00h)

9.12 AGP Configuration Registers

Note: All the registers described in this section can be accessed only when AGP is enable.

CNFG34: Configuration Register 34h

Register Type: Read Only

Read Port: 0034h

Default: 00000050h

D[7:0] Capabilities list offset pointer (Read Only)

CNFG50: Configuration Register 50h

Register Type: Read Only

Read Port: 0050h

Default: 00105c02h

D[23:20] Major revision number

D[19:16] Minor revision number

D[15:8] Pointer to next item

D[7:0] Cap_ID: value 02h identifies the list item as pertaining to AGP register

CNFG54: Configuration Register 54h

Register Type: Read Only

Read Port: 0054h

Default: 01000003h

D[31:24] Maximum number of AGP command requests

D9 Side band addressing support

0: Not support

1: Support

D1 4X mode support

0: Not support

1: Support

D1 2X mode support

0: Not support

1: Support

D0 1X mode support

0: Not support

1: Support

CNFG58: Configuration Register 58h

Register Type: Read/Write

Read Port: 0058h

Default: 00000000h

D[31:24] Maximum number of AGP requests can be enqueued

D9 1: sideband address mode enable

0: sideband address mode disable

D8 1: AGP enable

0: AGP disable

D2 1: 4X mode enable

0: 4X mode disable

D1 1: 2X mode enable

0: 2X mode disable

D0 1: 1X mode enable

0: 1X mode disable

CNFG5C: Configuration Register 5Ch

Register Type: Read

Read Port: 005Ch

Default: 00000000h

D[15:8] NULL: 00h indicates final item in the capability list

10 Register Summary / Description -- Legacy

10.1 Legacy ISA Registers

10.1.1 DMA Registers

Address	Access	Register Name
0000h	R/W	DMA1 CH0 Base and Current Address Register
0001h	R/W	DMA1 CH0 Base and Current Count Register
0002h	R/W	DMA1 CH1 Base and Current Address Register
0003h	R/W	DMA1 CH1 Base and Current Count Register
0004h	R/W	DMA1 CH2 Base and Current Address Register
0005h	R/W	DMA1 CH2 Base and Current Count Register
0006h	R/W	DMA1 CH3 Base and Current Address Register
0007h	R/W	DMA1 CH3 Base and Current Count Register
0008h	R/W	DMA1 Status(r) Command(w) Register
0009h	R/W	DMA1 Request Register
000Ah	R/W	DMA1 Command(r) Write Single Mask Bit (w) Register
000Bh	R/W	DMA1 Mode DMA Register
000Ch	WO	DMA1 Clear Byte Pointer
000Dh	WO	DMA1 Master Clear
000Eh	WO	DMA1 Clear Mask Register
000Fh	R/W	DMA1 Write All Mask Bits(w) Mask Status(r) Register
00C0h	R/W	DMA2 CH0 Base and Current Address Register
00C2h	R/W	DMA2 CH0 Base and Current Count Register
00C4h	R/W	DMA2 CH1 Base and Current Address Register
00C6h	R/W	DMA2 CH1 Base and Current Count Register
00C8h	R/W	DMA2 CH2 Base and Current Address Register
00CAh	R/W	DMA2 CH2 Base and Current Count Register
00CCh	R/W	DMA2 CH3 Base and Current Address Register
00CEh	R/W	DMA2 CH3 Base and Current Count Register
00D0h	R/W	DMA2 Status(r) Command(w) Register
00D2h	R/W	DMA2 Request Register

00D4h	R/W	DMA2 Command(r) Write Single Mask Bit(w) Register
00D6h	R/W	DMA2 Mode Register
00D8h	WO	DMA2 Clear Byte Pointer
00DAh	WO	DMA2 Master Clear
00DCh	WO	DMA2 Clear Mask Register
00DEh	R/W	DMA2 Write All Mask Bits(w) Mask Status Register(r)

Address	Access	Register Name
0080h	R/W	Reserved
0081h	R/W	DMA Channel 2 Low Page Register
0082h	R/W	DMA Channel 3 Low Page Register
0083h	R/W	DMA Channel 1 Low Page Register
0084h	R/W	Reserved
0085h	R/W	Reserved
0086h	R/W	Reserved
0087h	R/W	DMA Channel 0 Low Page Register
0088h	R/W	Reserved
0089h	R/W	DMA Channel 6 Low Page Register
008Ah	R/W	DMA Channel 7 Low Page Register
008Bh	R/W	DMA Channel 5 Low Page Register
008Ch	R/W	Reserved
008Dh	R/W	Reserved
008Eh	R/W	Reserved
008Fh	R/W	Reserved

Address	Access	Register Name
00480h	R/W	Reserved
00481h	R/W	DMA Channel 2 High Page Register
00482h	R/W	DMA Channel 3 High Page Register
00483h	R/W	DMA Channel 1 High Page Register
00484h	R/W	Reserved

00485h	R/W	Reserved
00486h	R/W	Reserved
00487h	R/W	DMA Channel 0 High Page Register
00488h	R/W	Reserved
00489h	R/W	DMA Channel 6 High Page Register
0048Ah	R/W	DMA Channel 7 High Page Register
0048Bh	R/W	DMA Channel 5 High Page Register
0048Ch	R/W	Reserved
0048Dh	R/W	Reserved
0048Eh	R/W	Reserved
0048Fh	R/W	Reserved

10.1.2 Interrupt Controller Registers

Address	Access	Register Name
0020h	R/W	INT 1 Base Address Register
0021h	R/W	INT 1 Mask Register
00A0h	R/W	INT 2 Base Address Register
00A1h	R/W	INT 2 Mask Register

10.1.3 Timer Registers

Address	Access	Register Name
0040h	R/W	Interval Timer 1 - Counter 0
0041h	R/W	Interval Timer 1 - Counter 1
0042h	R/W	Interval Timer 1 - Counter 2
0043h	WO	Interval Timer 1 - Control Word Register

10.1.4 Other Registers

Address	Access	Register Name
0061h	R/W	NMI Status Register
0070h	WO	CMOS RAM Address and NMI Mask Register
0092h	R/W	INIT and A20 Register
00F0h	WO	Coprocessor Error Register

04D0h	R/W	IRQ Edge/Level Control Register 1
04D1h	R/W	IRQ Edge/Level Control Register 2

11 Register Summary / Description – LPC Summary

11.1 LPC Bridge Configuration Registers

Address	Access	Register Name
00-01h	RO	Vendor ID
02-03h	RO	Device ID
04-05h	RO	Command Register
06-07h	RO	Status register
08h	RO	Revision ID
09-0Bh	RO	Class Code
0Ch	RO	Cache Line Size
0Dh	RO	Master Latency Timer
0Eh	RO	Header Type
0Fh	RO	Built-in Self Test
10-3Ch	RO	Reserved
40h	R/W	BIOS Control Register
41-44h	R/W	PCI INTA#/B#/C#/D# Remapping Register
45h	R/W	Flash ROM Control Register
46h	R/W	INIT Enable Register
47h	R/W	Keyboard Controller Register
48h	R/W	RTC Control Register
49h	R/W	Individual Distributed DMA Channel Enable Register
4A-4Bh	R/W	Distributed DMA Master Configuration Register
4C-4Fh	RO	Shadow Register of ICW1 to ICW4 of the INT1
50-53h	RO	Shadow Register of ICW1 to ICW4 of the INT2
54-55h	RO	Shadow Register of OCW 2&3 of INT1
56-57h	RO	Shadow Register of OCW 2&3 of the INT2
58h-5Fh	RO	CTC Shadow Registers 1 to 8
60h	RO	Shadow Register for ISA Port 70
61h	R/W	IDEIRQ Remapping Register
62h	R/W	Reserved.

63h	R/W	GPEIRQ Remapping Register
64h	R/W	Priority Timer
65h	R/W	PHOLD# Timer
66h	R/W	Reserved
67h	R/W	Clear SIRQ1 and SIRQ12
68-69h	R/W	Reserved
6Ah	R/W	ACPI/SCI IRQ Remapping Register
6Bh	R/W	Reserved
6Ch	R/W	SMBUS IRQ Remapping Register
6Dh	R/W	Software Watchdog IRQ Remapping Register
6E-6Fh	R/W	Software-Controlled Interrupt Requests
70h	R/W	Serial Interrupt Control Register
71-73h	R/W	Serial Interrupt Enable Register
74-75h	R/W	ACPI Base Address Register

11.2 LPC Bridge Configuration Registers

Device	IDSEL	Function Number
LPC Bridge	AD12	0000b

Register 00h~01h Vendor ID

Default Value: 1039h

Access: Read Only

Bit	Access	Description
15:0	RO	**Vendor Identification Number** Default value is 1039h

Register 02h~03h Device ID

Default Value: 0008h

Access: Read Only

Bit	Access	Description
15:0	RO	**Device Identification Number** Default value is 0008h

Note: Write a 1 to Reg40 bit 6 will change the Device ID to 0018h.

Register 04h~05h Command Register

Default Value: 000Ch

Access: Read Only

Bit	Access	Description
15:4	RO	**Reserved** Read as 0
3	RO	Read as 1 to indicate that the device is allowed to monitor special cycles.
2	RO	Read as 1 to indicate that the device is able to become PCI bus master.
1	RO	Response to Memory Space Accesses (default=0) This bit is hardwired to1.
0	RO	Response to Memory Space Accesses (default=0) This bit is hard wired to 1.

Register 06h~07h Status

Default Value: 0200h

Access: Read Only

Bit	Access	Description
15:14	RO	**Reserved** Read as 0
13	RO	**Received Master-Abort** This bit will be set to 1 when the current transaction is terminated with master-abort. This bit can be cleared to 0 by writing a 1 to it.
12	RO	**Received Target-Abort** This bit will be set to 1 when the current transaction is terminated with target-abort. This bit can be cleared to 0 by writing a 1 to it.
11	RO	**Reserved.** Read as 0.
10:9	RO	**DEVSEL# Timing** The two bits are hardwired to 01 to indicate positive decode with medium timing.
8:0	RO	**Reserved.** Read as 0.

Register 08h Revision ID

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	**Revision Identification Number**

Register 09h~0Bh Class Code

Default Value: 060100h

Access: Read Only

Bit	Access	Description
23:0	RO	**Class Code** Default value is 060100h.

Register 0Ch Cache Line Size

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	**Cache Line Size**

Register 0Dh Master Latency Timer

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	**Master Latency Timer**

Register 0Eh Header Type

Default Value: 80h

Access: Read Only

Bit	Access	Description
7:0	RO	**Header Type** Default value is 80h

Register 0Fh BIST

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	**BIST** Default value is 00h

Register 10h~3Ch Reserved. Read as 0.

Register 40h BIOS Control Register

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**ACPI Enable** 0 : Disable 1 : Enable When enabled, ACPI register at IO space address as defined in ACPI base registers (Reg 74h~75h) can be accessed.
6	R/W	**Device ID Selection** 0 : LPC Bridge Device ID is 0008 1 : LPC Bridge Device ID is 0018
5	R/W	**Reserved.**
4	R/W	**PCI Posted Write Buffer Enable** 0 : Disable (default) 1 : Enable
3	R/W	**Subtractive Decode to Internal registers Enable** 0 : Disable 1 : Enable When this bit is enabled, SiS540 will do subtractive decode on addresses for internal registers.
2	R/W	**Reserved.**
1	R/W	**BIOS positive Decode Enable** 0 : Disable 1 : Enable When enabled, SiS540 will positively respond to PCI memory cycles toward E segment and F segment. Otherwise, it will respond subtractively.

0	R/W	**Extended BIOS Enable. (FFF80000~FFFDFFFF)** When enabled, SiS540 will positively respond to PCI cycles toward the Extended segment. Otherwise, it will have no response.

Register 41/42/43/44h PCI INTA#/B#/C#/D# Remapping Register

Default Value: 80/80/80/80h

Access: Read/Write

Bit	Access	Description
7	R/W	**Remapping enable** 0: Enable 1 : Disable When enabled, PCI INTA#/B#/C#/D# will be remapped to the IRQ channel specified below.
6:4	RO	**Reserved.** Read as 0
3:0	R/W	**IRQ Remapping Table**

Bits	IRQx#	Bits	IRQx#	Bits	IRQx#
0000	Reserved	0110	IRQ6	1100	IRQ12
0001	Reserved	0111	IRQ7	1101	Reserved
0010	Reserved	1000	Reserved	1110	IRQ14
0011	IRQ3	1001	IRQ9	1111	IRQ15
0100	IRQ4	1010	IRQ10		
0101	IRQ5	1011	IRQ11		

Note: More than one of INT[A:D]# can be remapped to the same IRQ line, but that IRQ line should be programmed to level-triggered mode.

Table 11.2-1 Interrupt Pin Reroute Table

Function	Interrupt Pin	Function	Interrupt Pin
GUI	INTA	MAC	INTC
AUDIO	INTB	USB0	INTD
MODEM	INTB	USB1	INTD

Register 45h Flash ROM Control Register

Default Value: 40h

Access: Read/Write

Bit	Access	Description
7:6	R/W	**Flash EPROM Control Bit** If bit 7 is set to '0' after CPURST de-asserted, EPROM can be flashed when bit 6 is set to '1'. Once bit 7 is set to '1', EPROM can not be flashed until the system is reset.
5:0	R/W	**Reserved.**

Register 46h INIT Enable Register

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:6	R/W	**Hardware reset initiated by software** When both set to 1, hardware reset will be generated to CPU.
5	R/W	**INIT Enable** 0: Drives CPURST 10ms during S/W reset and INIT is inactive. 1 : Drives INIT during S/W reset
4	R/W	**Fast Gate 20 Emulation** 0 : Disable 1 : Enable
3	R/W	**Fast Reset Latency Control** 0 : 2us 1 : 6us
2	R/W	**Fast Reset Emulation** 0 : Disable 1 : Enable
1	R/W	**A20M# Output Control** 0: Enable the assertion of A20M# if applicable. 1: Disable the assertion of A20M#, i.e., A20M# will be high at all times.

0	R/W	**Enable Keyboard Hardware Reset** 0 : Disable 1 : Enable

Note: Write a 1 to Port 92 bit 0 will cause SiS540 to drive INIT if INIT Enable bit is 1, and Port 92 bit 1 will be set to 1 concurrently to Disable the assertion of A20M#.

Register 47h Keyboard Controller Register

Default Value: 51h

Access: Read/Write

Bit	Access	Description
7	R/W	**USB Legacy Support Interface Enable** 0 : Disable 1 : Enable
6	R/W	**PS/2 Mouse Lock Enable** 0 : Disable 1 : Enable
5	R/W	**Internal Keyboard Controller Clock Selection** 0 : PCICLK/4 1 : 7.159MHz
4	R/W	**Keyboard Lock Enable** 0 : Disable 1 : Enable
3	R/W	**Integrated Keyboard Controller Enable** 0 : Disable 1 : Enable
2	R/W	**Integrated PS/2 Mouse Enable** 0 : Disable 1 : Enable This bit is meaningful only when Bit3 is enabled.
1	R/W	**Keyboard Hot Key Status** This bit is set when hot key (Ctrl+Alt+Backspace) is pressed and should be cleared at the end of SMI# handler. This bit is meaningful only when internal KBC is enabled.

0	R/W	**Keyboard Hot Key Control** 0 : Disable 1 : Enable This bit is meaningful only when internal KBC is enabled.

Register 48h RTC Control Register

Default Value: 10h

Access: Read/Write

Bit	Access	Description
7	R/W	**RTC Extended Bank Enable (EXTEND_EN)** 0 : Disable 1 : Enable When this bit is enabled, the upper 128 bytes of RTC SRAM can be accessed.
6	R/W	**Automatic Power Control Registers (APCREG_EN) Enable** 0 : Disable 1 : Enable When this bit is enabled, APC registers can be accessed.
5	R/W	**Instant Power_Off Enable (INSTOFF_EN)** Before enabling this function, the bit1 at APC Register 04h should be enabled. System will be powered off if GPIO2_STS is set.
4	RO	**Internal RTC Status** 0 : Disable 1 : Enable
3:0	R/W	**Reserved.**

Register 49h Individual Distributed DMA Channel Enable

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Channel 7 DDMA Enable**
6	R/W	**Channel 6 DDMA Enable**
5	R/W	**Channel 5 DDMA Enable**

4	R/W	**Reserved** This bit must be programmed to 0.
3	R/W	**Channel 3 DDMA Enable**
2	R/W	**Channel 2 DDMA Enable**
1	R/W	**Channel 1 DDMA Enable**
0	R/W	**Channel 0 DDMA Enable** 0 : Disable 1 : Enable

Register 4A~4Bh Distributed DMA Master Configuration Register

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:4	R/W	**DDMA slave base address bits[15:4]** The DMA slave channels must be grouped into a 128 bytes block with 16 bytes per channel. The DMA slave channel 0 will be located at the base address specified here.
3:1	R/W	**Reserved** This bit must be programmed to 0.
0	R/W	**DDMA Function Enable** 0 : Disable (default) 1 : Enable

Register 4C~4Fh Shadow Register of ICW1 to ICW4 of INT1

Default Value: 00000000h

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect ICW1 to ICW4 of the master interrupt controller

Register 50~53h Shadow Register of ICW1 to ICW4 of INT2

Default Value: 00000000h

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect ICW1 to ICW4 of the slave interrupt controller

Register 54~55h Shadow Register of OCW2 to OCW3 of INT1

Default Value: 0000h

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect OCW2 to OCW3 of the master interrupt controller

Register 54~55h Shadow Register of OCW2 to OCW3 of INT2

Default Value: 0000h

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect OCW2 to OCW3 of the slave interrupt controller

Register 58h CTC Shadow Register 1

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect low byte of the initial count number of CTC Counter 0

Register 59h CTC Shadow Register 2

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect high byte of the initial count number of CTC Counter 0

Register 5Ah CTC Shadow Register 3

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect low byte of the initial count number of CTC Counter 1

Register 5Bh CTC Shadow Register 4

Default Value: 00h

Access: Read Only

Bit	Access	Description

7:0	RO	Reflect high byte of the initial count number of CTC Counter 1

Register 5Ch CTC Shadow Register 5

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect low byte of the initial count number of CTC Counter 2

Register 5Dh CTC Shadow Register 6

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect high byte of the initial count number of CTC Counter 2

Register 5Eh CTC Shadow Register 7

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect Control word (43h) of the built-in CTC

Register 5Fh Shadow Register 8

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:6	RO	**Reserved.**
5	RO	**CTC counter2 Write count pointer status**
4	RO	**CTC counter1 Write count pointer status**
3	RO	**CTC counter0 Write count pointer status**
2	RO	**CTC counter2 Read count pointer status**
1	RO	**CTC counter1 Read count pointer status**
0	RO	**CTC counter0 Read count pointer status** 0 : LSB 1 : MSB

Register 60h Shadow Register for ISA port 70h

Default Value: FFh

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect the content of ISA port 70h register

Register 61h IDEIRQ Remapping Register

Default Value: 80h

Access: Read/Write

Bit	Access	Description
7	R/W	**IDEIRQ Remapping Enable** 0 : Enable 1 : Disable (default)
6:5	R/W	**Reserved**
4	R/W	**IDE Channel Remapping Selection** 0 : Primary IDE channel 1 : Secondary IDE channel
3:0	R/W	**IRQ Remapping Table**

Bits	IRQx#	Bits	IRQx#	Bits	IRQx#
0000	Reserved	0110	IRQ6	1100	IRQ12
0001	Reserved	0111	IRQ7	1101	Reserved
0010	Reserved	1000	Reserved	1110	IRQ14
0011	IRQ3	1001	IRQ9	1111	IRQ15
0100	IRQ4	1010	IRQ10		
0101	IRQ5	1011	IRQ11		

Register 62h Reserved.

Default Value: 80h

Note: Bit 7 should be programmed to 1.

Register 63h GPEIRQ Remapping Register

Default Value: 80h

Access: Read/Write

Bit	Access	Description

7	R/W	**GPEIRQ Remapping Enable** 0 : Enable 1 : Disable (default)
6:4	R/W	**Reserved.**
3:0	R/W	**IRQ Remapping Table**

Bits	**IRQx#**	**Bits**	**IRQx#**	**Bits**	**IRQx#**
0000	Reserved	0110	IRQ6	1100	IRQ12
0001	Reserved	0111	IRQ7	1101	Reserved
0010	Reserved	1000	Reserved	1110	IRQ14
0011	IRQ3	1001	IRQ9	1111	IRQ15
0100	IRQ4	1010	IRQ10		
0101	IRQ5	1011	IRQ11		

Register 64h Priority Timer

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**Priority Timer** There are four PCI maser candidates inside the south bridge competing for the PCI bus. They are LPC/DMA master, DDMA, PCI MASTER2 and PCI MASTER3 .The local arbiter with rotating scheme is adopted to coordinate their requests to become PCI master. The candidate that issues request to the arbiter with a higher priority is the winner and is eligible to become PCI master when PCI grant is received. The priority timer is used to set a lower limit in terms of PCI clock for the winning candidate to continue its PCI transactions. The timer will start counting as soon as the winning candidate receives the PCI grant. Upon expiration, the winning candidate' s priority will become lowest among the four and, if the requests issued by the other masters are outstanding, it will lose the ownership of PCI grant. The maximum allowable value is FFh and the minimum allowable value is 00h.

Register 65h PHOLD# Timer

Default Value: 01h

Access: Read/Write

Bit	Access	Description

7:0	R/W	**PHOLD# Timer** The PHOLD# timer sets an upper limit in terms of PCI clock for the assertion time of PHOLD# initiated by LPC/DMA Master, DDMA, PCI MASTER2 and PCI MASTER3. The timer starts and continues the counting when south bridge receives PCI grant. Upon expiration, the chip will be forced to de-assert PCI request to system arbiter . The maximum allowable value is FFh and the minimum allowable value is 01h. If a larger value is programmed, the master will be able to complete more PCI transactions by preventing the system arbiter from issuing grant to other PCI master candidates. The PCI bus bandwidth can be fairly shared by all PCI master candidates by properly program this timer.

Register 66h Reserved. Read as 0.

Register 67h Clear SIRQ1 and SIRQ12

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**ISR bits clear SIRQ1 and SIRQ 12 Latches Enable** When set to 1, the internal latches for SIRQ1 and SIRQ12 will be cleared when the corresponding ISR bits are set in Interrupt Controller. The latches only take effective when either register 64h bit 7 or bit 6 is set to 1.The latches will always be cleared by a IO read cycle with address=60h.
6:5	R/W	**SMC37C673 Super I/O Compatible Mode** These two bits should be programmed to 1 if a SMC37C673 Super IO chip is connected to SiS540 via serial IRQ line. Bit_6 enables the chipset to latch SIRQ1, while Bit_5 enables the chipset to latch SIRQ12. For all other super IO chips, the two bits should be programmed to 0
4	R/W	**Serial IRQ sampled IOCHK phase control** 0: The sampled IOCHK on serial IRQ will be inverted. 1: The sampled IOCHK on serial IRQ will not be inverted. (Recommended)
3:0	R/W	**Reserved**

Register 68h~69h Reserved. Read as 0.

Register 6Ah ACPI/SCI IRQ Remapping Register

Default Value: 80h

Access: Read/Write

Bit	Access	Description
7	R/W	**ACPI/SCI IRQ Remapping Enable** 0 : Enable 1 : Disable (default)
6:4	R/W	**Reserved**
3:0	R/W	**IRQ Remapping Table**

Bits	**IRQx#**	**Bits**	**IRQx#**	**Bits**	**IRQx#**
0000	Reserved	0110	IRQ6	1100	IRQ12
0001	Reserved	0111	IRQ7	1101	Reserved
0010	Reserved	1000	Reserved	1110	IRQ14
0011	IRQ3	1001	IRQ9	1111	IRQ15
0100	IRQ4	1010	IRQ10		
0101	IRQ5	1011	IRQ11		

Register 6Bh Reserved. Read as 0.

Register 6Ch SMBUS IRQ Remapping Register

Default Value: 80h

Access: Read/Write

Bit	Access	Description
7	R/W	**SMBUS IRQ Remapping Enable** 0 : Enable 1 : Disable (default)
6:5	R/W	**Reserved**
4	RO	**SMBus IRQ Status**
3:0	R/W	**IRQ Remapping Table**

		Bits	**IRQx#**	**Bits**	**IRQx#**	**Bits**	**IRQx#**
		0000	Reserved	0110	IRQ6	1100	IRQ12
		0001	Reserved	0111	IRQ7	1101	Reserved
		0010	Reserved	1000	Reserved	1110	IRQ14
		0011	IRQ3	1001	IRQ9	1111	IRQ15
		0100	IRQ4	1010	IRQ10		
		0101	IRQ5	1011	IRQ11		

Register 6Dh Software Watchdog IRQ Remapping Register

Default Value: 80h

Access: Read/Write

Bit	**Access**	**Description**					
7	R/W	**Software Watchdog IRQ Remapping Enable** 0 : Enable 1 : Disable (default)					
6:4	R/W	**Reserved**					
3:0	R/W	**IRQ Remapping Table**					
		Bits	**IRQx#**	**Bits**	**IRQx#**	**Bits**	**IRQx#**
		0000	Reserved	0110	IRQ6	1100	IRQ12
		0001	Reserved	0111	IRQ7	1101	Reserved
		0010	Reserved	1000	Reserved	1110	IRQ14
		0011	IRQ3	1001	IRQ9	1111	IRQ15
		0100	IRQ4	1010	IRQ10		
		0101	IRQ5	1011	IRQ11		

Register 6Eh Software-Controlled Interrupt Request, Channels 7-0

Default Value: 00h

Access: Read/Write

Bit	**Access**	**Description**
7	R/W	**Interrupt Channel 7**
6	R/W	**Interrupt Channel 6**
5	R/W	**Interrupt Channel 5**
4	R/W	**Interrupt Channel 4**

3	R/W	**Interrupt Channel 3**
2	R/W	**Interrupt Channel 2**
1	R/W	**Interrupt Channel 1**
0	R/W	**Interrupt Channel 0** Writing a 1 to these bits will cause the corresponding interrupt requests to be outstanding. The default value to all is 0.

Register 6Fh Software-Controlled Interrupt Request, Channels 15-8

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Interrupt Channel 15**
6	R/W	**Interrupt Channel 14**
5	R/W	**Interrupt Channel 13**
4	R/W	**Interrupt Channel 12**
3	R/W	**Interrupt Channel 11**
2	R/W	**Interrupt Channel 10**
1	R/W	**Interrupt Channel 9**
0	R/W	**Interrupt Channel 8** Writing a 1 to these bits will cause the corresponding interrupt requests to be outstanding. The default value to all is 0.

Register 70h Serial Interrupt Control Register

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Serial Interrupt (SIRQ) Control** 0 : Disable (default) 1 : Enable
6	R/W	**Quiet/Continuous Mode** 0 : Continuous (default) 1 : Quiet

5:2	R/W	**SIRQ Sample Period** 0000: 17 slots (default) 0001: 18 slots 0010: 19 slots :::::::::::: 1111: 32 slots
1:0	R/W	**Start Cycle length** 00: 4 PCI clocks (default) 01: 6 PCI clocks 10: 8 PCI clocks 11: Reserved

Register 71h Serial Interrupt Enable Register 1

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**INV-SIRQ**
6	R/W	**Serial SMI# Enable**
5	R/W	**Serial IOCHCK# Enable**
4	R/W	**Serial INTD Enable**
3	R/W	**Serial INTC Enable**
2	R/W	**Serial INTB Enable**
1	R/W	**Serial INTA Enable** 0 : Disable (default) 1 : Enable
0	R/W	**Reserved**

Register 72h Serial Interrupt Enable Register 2

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Serial IRQ7 Enable**

6	R/W	**Serial IRQ6 Enable**
5	R/W	**Serial IRQ5 Enable**
4	R/W	**Serial IRQ4 Enable**
3	R/W	**Serial IRQ3 Enable**
2	R/W	**Reserved**
1	R/W	**Serial IRQ1 Enable**
0	R/W	**Reserved** 0 : Disable (default) 1 : Enable

Register 73h Serial Interrupt Enable Register 3

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Serial IRQ15 Enable**
6	R/W	**Serial IRQ14 Enable**
5	R/W	**Serial IRQ13 Enable**
4	R/W	**Serial IRQ12 Enable**
3	R/W	**Serial IRQ11 Enable**
2	R/W	**Serial IRQ10 Enable**
1	R/W	**Serial IRQ9 Enable**
0	R/W	**Serial IRQ8 Enable** 0 : Disable (default) 1 : Enable

Register 74~75h ACPI BASE Register

Default Value: 00h

Access: Read/Write

Bit	Access	Description
15:8	R/W	**ACPI Base Register A[15:8]** ACPI registers will be located at the address specified here.

7:0	RO	**Reserved** Read as 0.

Register 76h Reserved

Register 77h Two USB Controllers selection

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:2	R/W	**Reserved**
1:0	R/W	**USB Controllers selection** **Bits [1:0] USB1 USB0** 00 Enable Enable 01 Enable Disable 10 Disable Enable 11 Disable Disable Note: These bits will be valid when Reg. 7Ch bit3 must be enabled first.

Register 7Ch Dual USB Controllers Control Register

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:4	R/W	**Reserved**
3	R/W	**Two USB Controllers Control** 0 : Enable 1 : Disable
2:0	R/W	**Reserved**

12 Register Summary / Description –USB Summary

There are two USB Host Controllers embedded in the SiS540 chipset. One is assigned as function2 and the other one is function3. Both of them are designed base on the Open Host Controller Interface Specification for USB Release 1.0a. The Host Controller of function2 supports a 3-port RootHub and only two of them are used. The Host Controller of function3 supports a 2-port RootHub. Each of these two Host Controllers contains a set of Configuration Space, Operational Registers and Legacy Support Registers

12.1 USB OpenHCI Host Controller Configuration Space

12.1.1 USB Configuration Space

Configuration. Offset	Access	Mnemonic Register
00-01h	RO	VID Vendor ID
02-03h	RO	DID Device ID
04-05h	R/W	CMD Command Register
06-07h	R/W	STS Status register
08h	RO	RID Revision ID
09-0Bh	RO	CD Class Code
0Ch	RO	CL Cache Line Size
0Dh	R/W	MLT Master Latency Timer
0Eh	RO	HT Header Type
0Fh	RO	BIST Built-in Self Test
10-13h	R/W	Base address
13-3Bh	RO	Reserved
3Ch	R/W	INTL Interrupt line
3Dh	RO	INTP Interrupt pin
3Eh	RO	MINGNT Min Gnt
3Fh	RO	MAXLAT Max Latency

12.2 USB OpenHCI Host Controller Operational Registers

The base address of these registers is programmable by the memory base address register (USB PCI configuration register offset 10-13h). These registers should be written as Dword. Bytes write to these registers have unpredictable effects.

The OpenHCI Host Controller (HC) contains a set of on-chip operational registers that are mapped into a non-cacheable portion of the system addressable space. These registers are used by the Host Controller Driver (HCD). According to the functions of these registers, they are divided into four partitions, specifically for Control and Status, Memory Pointer, Frame Counter and Root Hub. All of the registers should be read and written as Dwords.

Reserved bits may be allocated in future releases of this specification. To ensure

interoperability, the Host Controller Driver that does not use a reserved field should not assume that the reserved field contains 0. Furthermore, the Host Controller Driver should always preserve the value(s) of the reserved field. When a R/W register is modified, the Host Controller Driver should first read the register, modify the bits desired, then write the register with the reserved bits still containing the read value. Alternatively, the Host Controller Driver can maintain an in-memory copy of previously written values that can be modified and then written to the Host Controller register. When a write to set/clear register is written, bits written to reserved fields should be 0.

12.2.1 Host Controller Operational Registers

Offset	3100
0	HcRevision
4	HcControl
8	HcCommandStatus
C	HcInterruptStatus
10	HcInterruptEnable
14	HcInterruptDisable
18	HcHCCA
1C	HcPeriodCurrentED
20	HcControlHeadED
24	HcControlCurrentED
28	HcBulkHeadED
2C	HcBulkCurrentED
30	HcDoneHead
34	HcFmInterval
38	HcFmRemaining
3C	HcFmNumber
40	HcPeriodicStart
44	HcLSThreshold
48	HcRhDescriptorA
4C	HcRhDescriptorB
50	HcRhStatus
54	HcRhPortStatus[1]
58	HcRhPortStatus[2]
5C	HcRhPortStatus[3] (Only for Function 2)
100	HceControl
104	HceInput
108	HceOutput
10C	HceStatus

12.2.1.1 Control and Status Partition

Register 00h HcRevision Register

Default Value: 00000110h

Access: Read

Bit	Access	Description
31:9		**Reserved**
8	RO	**Legacy** This read-only field is 1 to indicate that the legacy support registers are present in this HC.
7:0	RO	**Revision** This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 11h corresponds to version 1.1. All of the HC implementations that are compliant with current OpenHCI 1.0 specification will have a value of 10h.

Register 04h HcControl Register

Default Value: 00000000h

Access: Read/Write

The HcControl register defines the operating modes for the Host Controller. Only the Host Controller Driver, except Host Controller Functional State and Remote Wakeup Connected modifies most of the fields in this register.

Bit	Access	Description
31:11		**Reserved**
10	R/O	**RemoteWakeupEnable** This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signalling. When this bit is set and the Resume Detected bit in Hc Interrupt Status is set, a remote wakeup is signalled to the host system. Setting this bit has no impact on the generation of hardware interrupt. Since there is no remote wakeup supported, this bit is ignored.

9	RO	**Remote Wakeup Connected** This bit indicates whether HC supports remote wakeup signalling or not. If remote wakeup is supported and used by the system, it is the responsibility of system firmware to set this bit during POST. HC clears the bit upon a hardware reset but does not alter it upon software reset. Remote wakeup signalling of the host system is host-bus-specific and is not described in this specification. This bit is hard-coded to '0'.
8	R/W	**Interrupt Routing** This bit determines the routing of interrupts generated by events registered in Hc Interrupt Status. If clear, all interrupts are routed to the normal host bus interrupt mechanism. If set, interrupts are routed to the System Management Interrupt. HCD clears this bit upon hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.
7:6	R/W	**HostControllerFunctionalState for USB** 00b: UsbReset 01b: UsbResume 10b: UsbOperational 11b: UsbSuspend A transition to UsbOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartofFrame field of HcInterruptStatus. This field may be changed by HC only in the UsbSuspend state. HC may move from the UsbSuspend state to the UsbResume state after detecting the resume signal from a downstream port. HC enters UsbSuspend after a software reset, whereas it enters UsbReset after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signal to downstream ports.
5	R/W	**BulkListEnable** This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcBulkCurrentED is pointing to a ED to be removed, HCD must advance the pointer by updating HcBulkCurrentED before re-enabling the processing of the list.

4	R/W	**ControlListEnable** This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, the processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to a ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling the processing of the list.
3	R/W	**IsochronousEnable** This bit is used by HCD to enable/disable the processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).
2	R/W	**PeriodicListEnable** This bit is set to enable the processing of the periodic list in the next Frame. If cleared by HCD, the processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.
1:0	R/W	**ControlBulkServiceRatio** This specifies the service ratio between Control and Bulk EDs. Before processing any of the non-periodic lists, HC must compare the ratio specified with its internal count on how many non-empty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value. **CBSR** — **No. of Control EDs Over Bulk EDs Served** 0 — 1:1 1 — 2:1 2 — 3:1 3 — 4:1

Register 08h HcCommandStatus Register

Default Value: 00000000h

Access: Read/Write

The HcCommandStatus register is used by the Host Controller to receive commands issued by the Host Controller Driver, as well as reflecting the current status of the Host Controller. To the Host Controller Driver, it appears to be a "write to set" register. The Host Controller must ensure those "written as '1'" bits become set in the register while those "written as '0'" bits remain unchanged in the register. The Host Controller Driver may issue multiple distinct commands to the Host Controller without concern for corrupting previously issued commands. The Host Controller Driver has normal read access to all bits.

The **SchedulingOverrunCount** field indicates the number of frames with which the Host Controller has detected the scheduling overrun error. This occurs when the Periodic list does not complete before EOF. When a scheduling overrun error is detected, the Host Controller increments the counter and sets the **SchedulingOverrun** field in the HcInterruptStatus register.

Bit	Access	Description
31:18		**Reserved**
17:16	RO	**SchedulingOverrunCount** These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if Scheduling Overrun in Hc Interrupt Status has already been set. This is used by HCD to monitor any persistent scheduling problems.
15:4		**Reserved**
3	R/W	**OwnershipChangeRequest** This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the Ownership Change field in HcInterrupt Status. After the changeover, this bit is cleared and remains so until the next request from OS HCD.
2	R/W	**BulkListFilled** This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.

1	R/W	**ControlListFilled** This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop
0	R/W	**HostControllerReset** This bit is set by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the UsbSuspend state in which most of the operational registers are reset except those stated otherwise; e.g., the InterruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 µs. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signal should be asserted to its downstream ports.

Register 0Ch *HcInterruptStatus* Register

Default Value: 00000000h

Access: Read/Write

This register provides status on various events that cause hardware interrupts. When an event occurs, Host Controller sets the corresponding bit in this register. When a bit is set, a hardware interrupt is generated if the interrupt is enabled in the *HcInterruptEnable* register and the **MasterInterruptEnable** bit is set. The Host Controller Driver may clear specific bits in this register by writing '1'to bit positions to be cleared. The Host Controller Driver may not set any of these bits. The Host Controller will never clear the bit.

Bit	Access	Description
31		**Reserved**
30	R/W	**Ownership Change Status** This bit is set by HC when HCD sets the Ownership Change Request field in HcCommandStatus. This event, when unmasked, will always generate an System Management Interrupt (SMI#) immediately.
29:7		**Reserved**

6	R/W	**RootHubStatusChange Status** This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus[NumberofDownstreamPort] has changed.
5	R/W	**FrameNumberOverflow Status** This bit is set when the MSb of HcFmNumber (bit 15) changes value, from 0 to 1 or from 1 to 0, and after HccaFrameNumber has been updated.
4	RO	**UnrecoverableError Status** This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset. This event is not implemented and is hard-coded to '0'.
3	R/W	**ResumeDetected Status** This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the UsbResume state.
2	R/W	**StartofFrame Status** This bit is set by HC at each start of a frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	R/W	**WritebackDoneHead Status** This bit is set immediately after HC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead.
0	R/W	**SchedulingOverrun Status** This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun will also cause the SchedulingOverrunCount of HcCommandStatus to be incremented.

Register 10h *HcInterruptEnable* Register

Default Value: 00000000h

Access: Read/Write

Each enable bit in the *HcInterruptEnable* register corresponds to an associated interrupt bit in the *HcInterruptStatus* register. The *HcInterruptEnable* register is used to control those events generate a hardware interrupt. When a bit is set in the *HcInterruptStatus* register

and the corresponding bit in the *HcInterruptEnable* register is set AND the **MasterInterruptEnable** bit is set, then a hardware interrupt is requested on the host bus.

Writing a '1' to a bit in this register sets the corresponding bit, whereas writing a '0' to a bit in this register leaves the corresponding bit unchanged. On read, the current value of this register is returned.

Bit	Access	Description
31	R/W	**MasterInterrupt Enable** A '0' written to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as a Master Interrupt Enable.
30	R/W	**OwnershipChange Enable** 0 : Ignore 1 : Enable interrupt generation due to Ownership Change.
29:7		**Reserved**
6	R/W	**RootHubStatusChange Enable** 0 : Ignore 1 : Enable interrupt generation due to Root Hub Status Change.
5	R/W	**FrameNumberOverflow Enable** 0 : Ignore 1 : Enable interrupt generation due to Frame Number Overflow.
4	R/W	**UnrecoverableError Enable** This event is not implemented. All writes to this bit will be ignored.
3	R/W	**ResumeDetected Enable** 0 : Ignore 1 : Enable interrupt generation due to Resume Detect.
2	R/W	**StartofFrame Enable** 0 : Ignore 1 : Enable interrupt generation due to Start of Frame.
1	R/W	**WritebackDoneHead Enable** 0 : Ignore 1 : Enable interrupt generation due to HcDoneHead Writeback

0	R/W	**SchedulingOverrun Enable** 0 : Ignore 1 : Enable interrupt generation due to Scheduling Overrun.

Register 14h *HcInterruptDisable* Register

Default Value: 00000000h

Access: Read/Write

Each disable bit in the *HcInterruptDisable* register corresponds to an associated interrupt bit in the *HcInterruptStatus* register. The *HcInterruptDisable* register is coupled with the *HcInterruptEnable* register. Thus, writing a '1' to a bit in this register clears the corresponding bit in the *HcInterruptEnable* register, whereas writing a '0' to a bit in this register leaves the corresponding bit in the *HcInterruptEnable* register unchanged. On read, the current value of the *HcInterruptEnable* register is returned.

Bit	Access	Description
31	R/W	**MasterInterrupt Disable** A '0' written to this field is ignored by HC. A '1' written to this field disables interrupt generation due to events specified in the other bits of this register. This field is set after a hardware or software reset.
30	R/W	**OwnershipChange Disable** 0 : Ignore 1 : Disable interrupt generation due to Ownership Change.
29:7		**Reserved**
6	R/W	**RootHubStatusChange Disable** 0 : Ignore 1 : Disable interrupt generation due to Root Hub Status Change.
5	R/W	**FrameNumberOverflow Disable** 0 : Ignore 1 : Disable interrupt generation due to Frame Number Overflow.
4	R/W	**UnrecoverableError Disable** This event is not implemented. All writes to this bit will be ignored.
3	R/W	**ResumeDetected Disable** 0 : Ignore 1 : Disable interrupt generation due to Resume Detect.

2	R/W	**StartofFrame Disable** 0 : Ignore 1 : Disable interrupt generation due to Start of Frame.
1	R/W	**WritebackDoneHead Disable** 0 : Ignore 1 : Disable interrupt generation due to HcDoneHead Writeback.
0	R/W	**Scheduling Overrun Disable** 0 : Ignore 1 : Disable interrupt generation due to Scheduling Overrun.

12.2.1.2 Memory Pointer Partition

Register 18h HcHCCA Register

Default Value: 00000000h

Access: Read/Write

The *HcHCCA* register contains the physical address of the Host Controller Communication Area. The Host Controller Driver determines the alignment restrictions by writing all 1s to *HcHCCA* and reading the content of *HcHCCA*. The alignment is evaluated by examining the number of zeroes in the lower order bits. The minimum alignment is 256 bytes; therefore, bits 0 through 7 must always return '0' when read. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.

Bit	Access	Description
31:8	R/W	This is the base address of the Host Controller Communication Area.
7:0		**Reserved**

Register 1Ch HcPeriodCurrentED Register

Default Value: 00000000h

Access: Read/Write

The HcPeriodCurrentED register contains the physical address of the current Isochronous or Interrupt Endpoint Descriptor.

Bit	Access	Description

31:4	R/W	**PeriodCurrentED** This is used by HC to point to the head of one of the Periodic lists that will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
3:0		**Reserved**

Register 20h *HcControlHeadED* Register

Default Value: 00000000h

Access: Read/Write

The *HcControlHeadED* register contains the physical address of the first Endpoint Descriptor of the Control list.

Bit	Access	Description
31:4	R/W	**ControlHeadED** HC traverses the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0		**Reserved**

Register 24h HcControlCurrentED Register

Default Value: 00000000h

Access: Read/Write

The HcControlCurrentED register contains the physical address of the current Endpoint Descriptor of the Control list.

Bit	Access	Description
31:4	R/W	**ControlCurrentED** This pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.
3:0		**Reserved**

Register 28h HcBulkHeadED Register

Default Value: 00000000h

Access: Read/Write

The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list.

Bit	Access	Description
31:4	R/W	**BulkHeadED** HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0		**Reserved**

Register 2Ch HcBulkCurrentED Register

Default Value: 00000000h

Access: Read/Write

The HcBulkCurrentED register contains the physical address of the current endpoint of the Bulk list. As the Bulk list will be served in a round-robin fashion, the endpoints will be ordered according to their insertion to the list.

Bit	Access	Description
31:4	R/W	**BulkCurrentED** This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of HcControl. If set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of HcControl is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3:0		**Reserved**

Register 30h HcDoneHead Register

Default Value: 00000000h

Access: Read/Write

The HcDoneHead register contains the physical address of the last completed Transfer Descriptor that was added to the Done queue. In normal operation, the Host Controller Driver should not need to read this register as its content is periodically written to the HCCA.

Bit	Access	Description

31:4	R/W	**DoneHead** When a TD is completed, HC writes the content of HcDoneHead to the NextTD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the WritebackDoneHead of HcInterruptStatus.
3:0		**Reserved**

12.2.1.3Frame Counter Partition

Register 34h HcFmInterval Register

Default Value: 00002EDFh

Access: Read/Write

The HcFmInterval register contains a 14-bit value which indicates the bit time interval in a Frame, (i.e., between two consecutive SOFs), and a 15-bit value indicating the Full Speed maximum packet size that the Host Controller may transmit or receive without causing scheduling overrun. The Host Controller Driver may carry out minor adjustment on the **FrameInterval** by writing a new value over the present one at each SOF. This provides the programmability necessary for the Host Controller to synchronize with an external clocking resource and to adjust any unknown local clock offset.

Bit	Access	Description
31	R/W	**FrameIntervalToggle** HCD toggles this bit whenever it loads a new value to FrameInterval.
30:16	R/W	**FSLargestDataPacket** This field specifies a value that is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15:14		**Reserved**

13:0	R/W	**FrameInterval** This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of HcCommandStatus as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

Register 38h HcFmRemaining Register

Default Value: 00000000h

Access: Read Only

The HcFmRemaining register is a 14-bit down counter showing the bit time remaining in the current Frame.

Bit	Access	Description
31	RO	**FrameRemainingToggle** This bit is loaded from the FrameIntervalToggle field of HcFmInterval whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.
30:14		**Reserved**
13:0	RO	**FrameRemaining** This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in HcFmInterval at the next bit time boundary. When entering the UsbOperational state, HC re-loads the content with the FrameInterval of HcFmInterval and uses the updated value from the next SOF.

Register 3Ch HcFmNumber Register

Default Value: 00000000h

Access: Read

The HcFmNumber register is a 16-bit counter. It provides a timing reference among events occurring in the Host Controller and the Host Controller Driver. The Host Controller Driver may use the 16-bit value specified in this register and generate a 32-bit frame number without requiring frequent access to the register.

Bit	Access	Description
31:16		**Reserved**

15:0	RO	**FrameNumber** This is incremented when HcFmRemaining is re-loaded. It will be rolled over to 0h after ffffh. When entering the UsbOperational state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the StartofFrame in HcInterruptStatus.

Register 40h HcPeriodicStart Register

Default Value: 00000000h

Access: Read/Write

The HcPeriodicStart register has a 14-bit programmable value that determines when is the earliest time HC should start processing the periodic list.

Bit	Access	Description
31:14		**Reserved**
13:0	R/W	**PeriodicStart** After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from HcFmInterval. A typical value will be 3E67h. When HcFmRemaining reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

Register 44h HcLSThreshold Register

Default Value: 00000000h

Access: Read/Write

The HcLSThreshold register contains an 11-bit value used by the Host Controller to determine whether to commit to the transfer of a maximum of 8-byte LS packet before EOF. Neither the Host Controller nor the Host Controller Driver is allowed to change this value.

Bit	Access	Description
31:12		**Reserved**
11:0	R/W	**LSThreshold** This field contains a value that is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining ≥ this field. The value is calculated by HCD with the consideration of transmission and set-up overhead.

12.2.1.4 Root Hub Partition

All registers included in this partition are dedicated to the USB Root Hub which is an integral part of the Host Controller though still a functionally separate entity. The HCD emulates USBD accesses to the Root Hub via a register interface. The HCD maintains many USB-defined hub features that are not required to be supported in hardware. For example, the Hub's Device, Configuration, Interface, and Endpoint Descriptors are maintained only in the HCD as well as some static fields of the Class Descriptor. The HCD also maintains and decodes the Root Hub's device address as well as other trivial operations that are better suited to software than hardware.

The Root Hub register interface is otherwise developed to maintain similarity of bit organization and operation to typical hubs that are found in the system. Below are four register definitions: HcRhDescriptorA, HcRhDescriptorB, HcRhStatus, and HcRhPortStatus [5:1]. Each register is read and written as a Dword. These registers are only written during initialization to correspond with the system implementation. The HcRhDescriptorA and HcRhDescriptorB registers should be implemented such that they are writable regardless of the HC USB state. HcRhStatus and HcRhPortStatus must be writable during the UsbOperational state.

Register 48h HcRhDescriptorA Register

Default Value: 01000003h (function2)/ 01000002h (function3)

Access: Read/Write

The HcRhDescriptorA register is the first register of two describing characteristics of the Root Hub. Reset values are implementation-specific. The descriptor length (11), descriptor type (TBD), and hub controller current (0) fields of the hub Class Descriptor are emulated by the HCD. All other fields are located in the HcRhDescriptorA and HcRhDescriptorB registers.

Bit	Access	Description
31:24	R/W	**PowerOnToPowerGoodTime** This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2 ms.
23: 13		**Reserved**
12	R/W	**NoOverCurrentProtection** This bit describes how the overcurrent status for the Root Hub ports is reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting. 0 : Over-current status is reported collectively for all downstream ports 1 : No overcurrent protection supported

11	R/W	**OverCurrentProtectionMode** This bit describes how the overcurrent status for the Root Hub ports is reported. At reset, this field should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared. 0 : over-current status is reported collectively for all downstream ports 1 : over-current status is reported on a per-port basis
10	RO	**DeviceType** This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.
9	R/W	**NoPowerSwitching** These bits are used to specify whether power switching is supported or ports are always powered. SiS540 USB HC supports global power switching mode. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching. 0 : Ports are power switched 1 : Ports are always powered on when the HC is powered on
8	R/W	**PowerSwitchingMode** This bit is used to specify how the power switching of the Root Hub ports is controlled. SiS540 USB HC supports global power switching mode. This field is only valid if the NoPowerSwitching field is cleared. 0: all ports are powered at the same time. 1: Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ Clear Global Power).
7:0	RO	**NumberDownstreamPorts** These bits specify the number of downstream ports supported by the Root Hub. One of the USB HC (function 2) supports three downstream ports, another (function 3) supports two downstream ports.

Register 4Ch HcRhDescriptorB Register

Default Value: 00000000h

Access: Read/Write

The HcRhDescriptorB register is the second register of two describing the characteristics of the Root Hub. These fields are written during initialization to configure the Root Hub.

Bit	Access	Description
31:16	R/W	**PortPowerControlMask** Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode=0), this field is not valid. SiS540 USB HC implements global power switching. bit 0: Reserved bit 1: Ganged-power mask on Port #1 bit 2: Ganged-power mask on Port #2 ... bit15: Ganged-power mask on Port #15
15:0	R/W	**DeviceRemovable** Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. bit 0: Reserved bit 1: Device attached to Port #1 bit 2: Device attached to Port #2 ... bit15: Device attached to Port #15

Register 50h HcRhStatus Register

Default Value: 00000000h

Access: Read/Write

The HcRhStatus register is divided into two parts. The lower word of a Dword represents the Hub Status field and the upper word represents the Hub Status Change field. Reserved bits should always be written '0'.

Bit	Access	Description
31	WO	**ClearRemoteWakeupEnable(Write)** Writing a '1' clears DeviceRemoveWakeupEnable. Writing a '0' has no effect.
30:18		**Reserved**

17	R/W	**OverCurrentIndicatorChange** This bit is set by hardware when a change has occurred to the OCI field of this register. The HCD clears this bit by writing a '1'.Writing a '0' has no effect.
16	R/W	**LocalPowerStatusChange(Read)** The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. **SetGlobalPower(Write)** In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.
15	R/W	**DeviceRemoteWakeupEnable(Read)** This bit enables a ConnectStatusChange bit as a resume event, causing a UsbSuspend to UsbResume state transition and setting the ResumeDetected interrupt. 0 : **ConnectStatusChange** is not a remote wakeup event. 1 : **ConnectStatusChange** is a remote wakeup event. **SetRemoteWakeupEnable(Write)** Writing a '1' sets DeviceRemoveWakeupEnable. Writing a '0' has no effect.
14:2		**Reserved**
1	RO	**OverCurrentIndicator** This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always '0'
0	R/W	**LocalPowerStatus((Read))** The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. **ClearGlobalPower(Write)** In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.

Register 54h/58h HcRhPortStatus [2:1] Register

Default Value: 00000000h

Access: Read/Write

The HcRhPortStatus[2:1] register is used to control and report port events on a per-port basis. Three/Two HcRhPortStatus registers are implemented in two Host Controller, respectively. And only two of three ports of function2 are used. The lower word is used to reflect the port status, whereas the upper word reflects the status change bits. Some status bits are implemented with special write behavior (see below). If a transaction (token through handshake) is in progress when a write to change port status occurs, the resulting port status change must be postponed until the transaction completed. Reserved bits should always be written '0'.

Bit	Access	Description
31:21		**Reserved**
20	R/W	**PortResetStatusChange** This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 : port reset is not complete 1 : port reset is complete
19	R/W	**PortOverCurrentIndicatorChange** This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 : no change in PortOverCurrentIndicator 1 : PortOverCurrentIndicator has changed
18	R/W	**PortSuspendStatusChange** This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when ResetStatusChange is set. 0 : resume is not completed 1 : resume completed
17	R/W	**PortEnableStatusChange** This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 : no change in **PortEnableStatus** 1 : change in PortEnableStatus

16	R/W	**ConnectStatusChange** This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared when a SetPortReset, SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. 0 : no change in CurrentConnectStatus 1 : change in CurrentConnectStatus Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.
15:10		**Reserved**
9	R/W	**LowSpeedDeviceAttached((Read))** This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set. 0 : full speed device attached 1 : low speed device attached

8	R/W	**Port Power Status((Read))** This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing Set Port Power or Set Global Power. HCD clears this bit by writing Clear Port Power or Clear Global Power. Which power control switches will be enabled is determined by Power Switching Mode and Port Power Control Mask[NDP]. In global switching mode (Power Switching Mode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (Power Switching Mode=1), if the Port Power Control Mask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ Clear Global Power commands are enabled. When port power is disabled, Current Connect Status, Port Enable Status, Port Suspend Status, and Port Reset Status should be reset. 0 : port power is off 1 : port power is on **SetPortPower(Write)** The HCD writes a '1' to set the PortPowerStatus bit. Writing a '0' has no effect. Note: This bit is always reads '1b' if power switching is not supported.
7:5		**Reserved**
4	R/W	**PortResetStatus(Read)** When this bit is set by a write to SetPortReset, port reset signalling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared. 0 : port reset signal is not active 1 : port reset signal is active **SetPortReset(Write)** The HCD sets the port reset signalling by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.

3	R/W	**PortOverCurrentIndicator(Read)** This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal 0 : no overcurrent condition. 1 : overcurrent condition detected. **ClearSuspendStatus(Write)** The HCD writes a '1' to initiate a resume. Writing a '0' has no effect. A resume is initiated only if PortSuspendStatus is set.
2	R/W	**PortSuspendStatus(Read)** This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the UsbResume state. If an upstream resume is in progress, it should propagate to the HC. 0 : port is not suspended 1 : port is suspended **SetPortSuspend(Write)** The HCD sets the PortSuspendStatus bit by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.

1	R/W	**PortEnableStatus(Read)** This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set. 0 : port is disabled 1 : port is enabled **SetPortEnable(Write)** The HCD sets PortEnableStatus by writing a '1'.Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected port.
0	R/W	**CurrentConnectStatus(Read)** This bit reflects the current state of the downstream port. 0 : no device connected 1 : device connected **ClearPortEnable(Write)** The HCD writes a '1' to this bit to clear the PortEnableStatus bit. Writing a '0' has no effect. The CurrentConnectStatus is not affected by any write. Note: This bit is always read ' 1b' when the attached device is nonremovable (DeviceRemoveable[NDP]).

12.3 Legacy Support Registers

Four operational registers are used to provide the legacy support. Each of these registers is located on a 32-bit boundary. The offset of these registers is relative to the base address of the Host Controller operational registers with HceControl located at offset 100h.

Table 12.3-1 Legacy Support Registers

Offset	Register	Description
100h	HceControl	Used to enable and control the emulation hardware and report various status informations.

104h	HceInput	Emulation side of the legacy Input Buffer register.
108h	HceOutput	Emulation side of the legacy Output Buffer register where keyboard and mouse data is to be written by software.
10Ch	HceStatus	Emulation side of the legacy Status register.

Three of the operational registers (HceStatus, HceInput, HceOutput) are accessible at I/O address 60h and 64h when emulation is enabled. Reads and writes to the registers using I/O addresses have side effects as outlined in the Table 12.3-2 Emulated Registers

Table 12.3-2 Emulated Registers

I/O Address	Cycle Type	Register Contents Accessed/ Modified	Side Effects
60h	IN	HceOutput	IN from port 60h will set OutputFull in HceStatus to 0
60h	OUT	HceInput	OUT to port 60h will set InputFull to 1 and CmdData to 0 in HceStatus.
64h	IN	HceStatus	IN from port 64h returns current value of HceStatus with no other side effect.
64h	OUT	HceInput	OUT to port 64h will set InputFull to 0 and CmdData in HceStatus to 1.

Register 100h HceControl Register

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:9		**Reserved**
8	R/W	**A20State** Indicates current state of Gate A20 on keyboard controller. Used to compare value to 60h when GateA20Sequence is active.
7	R/W	**IRQ12Active** Indicates that a positive transition on IRQ12 from keyboard controller has occurred. SW may write a 1 to this bit to clear it (set it to 0). SW write of a 0 to this bit has no effect.
6	R/W	**IRQ1Active** Indicates that a positive transition on IRQ1 from keyboard controller has occurred. SW may write a 1 to this bit to clear it (set it to 0). SW write of a 0 to this bit has no effect.

5	R/W	**GateA20Sequence** Set by HC when a data value of D1h is written to I/O port 64h. Cleared by HC on write to I/O port 64h of any value other than D1h.
4	R/W	**ExternalIRQEn** When set to 1, IRQ1 and IRQ12 from the keyboard controller causes an emulation interrupt. The function controlled by this bit is independent of the setting of the **EmulationEnable** bit in this register.
3	R/W	**IRQEn** When set, the HC generates IRQ1 or IRQ12 as long as the **OutputFull** bit in *HceStatus* is set to 1. If the **AuxOutputFull** bit of *HceStatus* is 0, then IRQ1 is generated; if it is 1, then an IRQ12 is generated.
2	R/W	**CharacterPending** When set, an emulation interrupt is generated when the **OutputFull** bit of the *HceStatus* register is set to 0.
1	RO	**EmulationInterrupt** This bit is a static decode of the emulation interrupt condition
0	R/W	**EmulationEnable** When set to 1, the HC is enabled for legacy emulation. The HC decodes accesses to I/O registers 60h and 64h and generates IRQ1 and/or IRQ12 when appropriate. Additionally, the HC generates an emulation interrupt at appropriate times to invoke the emulation software.

Register 104h HceInput Register

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:8		**Reserved**

7:0	R/W	**InputData** This register holds data that is written to I/O ports 60h and 64h. I/O data that is written to ports 60h and 64h is captured in this register when emulation is enabled. This register may be read or written directly by accessing it with its memory address in the Host Controller' s operational register space. When accessed directly with a memory cycle, reads and writes of this register have no side effects.

Register 108h HceOutput Register

Default Value: 00000000h

Access: Read/write

Bit	Access	Description
31:8		**Reserved**
7:0	R/W	**OutputData** This register hosts data that is returned when an I/O read of port 60h is performed by application software. The data placed in this register by the emulation software is returned when I/O port 60h is read and emulation is enabled. On a read of this location, the OutputFull bit in HceStatus is set to 0.

Register 10Ch HceStatus Register

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:8		**Reserved**
7	R/W	**Parity** Indicates parity error on keyboard/mouse data.
6	R/W	**Time-out** Used to indicate a time-out
5	R/W	**AuxOutputFull** IRQ12 is asserted whenever this bit is set to 1 and **OutputFull** is set to 1 and the **IRQEn** bit is set.
4	R/W	**Inhibit Switch** This bit reflects the state of the keyboard inhibit switch and is set if the keyboard is NOT inhibited.

3	R/W	**CmdData** The HC sets this bit to 0 on an I/O write to port 60h and to 1 on an I/O write to port 64h
2	R/W	**Flag** Nominally used as a system flag by software to indicate a warm or cold boot.
1	R/W	**InputFull** Except for the case of a Gate A20 sequence, this bit is set to 1 on an I/O write to address 60h or 64h. While this bit is set to 1 and emulation is enabled, an emulation interrupt condition exists.
0	R/W	**OutputFull** The HC sets this bit to 0 on a read of I/O port 60h. If **IRQEn** is set and **AuxOutputFull** is set to 0, then an IRQ1 is generated as long as this bit is set to 1. If **IRQEn** is set and **AuxOutputFull** is set to 1, then an IRQ12 is generated as long as this bit is set to 1. While this bit is 0 and **CharacterPending** in *HceControl* is set to 1, an emulation interrupt condition exists. The contents of the *HceStatus* Register are returned on an I/O Read of port 64h when emulation is enabled. Reads and writes of port 60h and writes to port 64h can cause changes in this register. Emulation software can directly access this register through its memory address in the Host Controller's operational register space. Accessing this register through its memory address produces no side effects.

13 Register Summary / Description – Fast Ethernet / Home Networking Summary

13.1 MAC and PHY Registers

13.1.1 MAC Configuration Space (Function 1)

Configuration. Offset	Access	Mnemonic Register
00-01h	RO	Vendor ID
02-03h	RO	Device ID
04-05h	R/W	Command Register
06-07h	R/W	Status Register
08h	RO	Revision ID
09-0Bh	RO	Class Code
0Ch	RO	Cache Line Size
0Dh	R/W	Master Latency Timer
0Eh	RO	Header Type
0Fh	RO	Built-in Self Test
10-13h	R/W	Configuration IO Base Address Register
14-17h	R/W	Configuration Memory Address Register
18-28h	RO	RESERVED (reads return zero)
2C-2Fh	R/W	Configuration Subsystem Identification Register
30-33h	R/W	Configuration Expansion ROM Base Address Register
34-37h	R/W	Configuration Capabilities Pointer Register
38-3Bh	RO	RESERVED (reads return zero).
3C-3Fh	R/W	Configuration Interrupt Select Register
40-43h	R/W	Configuration Power Management Capabilities Register
44-47h	R/W	Configuration Power Management Control and Status Register
48-FFh	RO	RESERVED (reads return zero)

13.1.2 MAC Operational Registers

Configuration. Offset	Access	Mnemonic Register
00-03h	R/W	Command Register
04-07h	R/W	Configuration Register
08-0Bh	R/W	EEPROM Access Register
0C-0Fh	R/W	PCI Test Control Register
10-13h	R/W	Interrupt Status Register
14-17h	R/W	Interrupt Mask Register
18-1Bh	R/W	Interrupt Enable Register
1C-1Fh	R/W	Enhanced PHY Access Register
20-23h	R/W	Transmit Descriptor Pointer Register
24-27h	R/W	Transmit Configuration Register
28-2Fh	R/W	RESERVED
30-33h	R/W	Receive Descriptor Pointer Register
34-37h	R/W	Receive Configuration Register
38-3Bh	R/W	Flow Control Register
3C-47h	RO	RESERVED
48-4Bh	R/W	Receive Filter Control Register
4C-4Fh	R/W	Receive Filter Data Register
50-AFh	RO	RESERVED
B0-B3h	R/W	Power Management Control Register
B4-B7h	R/W	Power Management Wake-up Event Register
B8-BBh	R/W	RESERVED
BC-BFh	R/W	Wake-up Sample Frame CRC Register
C0-EFh	R/W	Wake-up Sample Frame Mask Registers
F0-FFh	R/W	RESERVED

13.1.3 PHY Configuration Registers

Configuration. Offset	Access	Mnemonic Register
00h	R/W	MI Register 0 Control Register
01h	R/W	MI Register 1 Status Register
02h	R/W	MI Register 2 PHY ID#1

03h	R/W	MI Register 3 PHY ID#2
04h	R/W	MI Register 4 Auto Negotiation Advertisement
05h	R/W	MI Register 5 Auto Negotiation Remote End Capability
10h	R/W	MI Register 16 Configuration 1
11h	R/W	MI Register 17 Configuration 2
12h	R/W	MI Register 18 Status Output
13h	R/W	MI Register 19 Mask
14h	R/W	MI Register 20 Reserved

1.2. 10M/100M Ethernet Controller Registers

The SiS Ethernet Controller is configured and controlled through registers. There are three categories of control/status registers implemented inside the SiS Ethernet Controller, which includes PCI Configuration Registers, MAC Operational Registers and MII PHY Registers. The PCI Configuration registers are mapped into PCI configuration space and accessed using PCI configuration bus cycles. The MAC Operational registers can be mapped into either PCI memory or PCI IO space. MII PHY Registers are accessed through MAC Operational Register ENPHY (Enhanced PHY access register, offset 1Ch). The SiS Ethernet Controller requires an allocation of 256 bytes of operational register space, and 72 bytes of PCI configuration register space.

Acronyms mentioned in the PCI configuration registers and MAC Operational registers are defined as follows:

RO :Read Only

R/W :Read Write

Acronyms mentioned in the MII PHY registers that are defined as follows:

Sym.	Name	Definition	
		Write Cycle	Read Cycle
W	Write	Input	No Operation
R	Read	No Operation	Output
R/W	Read/Write	Input	Output
R/WSC	Read/Write Self Cleaning	Input	Output Clears itself After Operation Complete

R/LL	Read/Latching Low	No Operation	Output When Bit Goes Low, Bit Latched. When Bit is Read, Bit Updated.
R/LH	Read/Latching High	No Operation	Output When Bit Goes High, Bit Latched. When Bit is Read, Bit Updated.
R/LT	Read/Latching on Transition	No Operation	Output When Bit Transitions, Bit Latched And Interrupt Set When Bit is Read, Interrupt Clear And Bit Updated.

13.2 PCI Configuration Registers

The SiS Ethernet Controller implements a PCI version 2.1 configuration register space. This allows PCI BIOS to "soft" configure the SiS Ethernet Controller. Software Reset has no effect on configuration registers. Hardware Reset returns all configuration registers to their hardware reset state. For all reserved registers, a write are ignored, and a read return 0.

Table 13.2-1 Configuration Register Map

Offset	Tag	Description	Access
00h	CFGID	Configuration Identification Register	RO
04h	CFGCS	Configuration Command and Status Register	R/W
08h	CFGRID	Configuration Revision ID Register	RO
0Ch	CFGLAT	Configuration Revision ID Register	R/W
10h	CFGIOA	Configuration IO Base Address Register	R/W
14h	CFGMA	Configuration Memory Address Register	R/W
18h-28h		RESERVED (reads return zero).	
2Ch	CFGSID	Configuration Subsystem Identification Register	RO
30h	CFGEROMA	Configuration Expansion ROM Base Address Register	R/W

34h	CFGCAP	Configuration Capabilities Pointer Register	RO
38h		RESERVED (reads return zero).	
3Ch	CFGINT	Configuration Interrupt Select Register	R/W
40h	CFGPMC	Configuration Power Management Capabilities Register	RO
44h	CFGPMCSR	Configuration Power Management Control and Status Register	R/W
48-FFh		RESERVED (reads return zero).	

Register 00h Configuration Identification

Default Value: 09001039h

Access: Read Only

This register identifies The SiS Ethernet Controller to PCI system software.

Bit	Access	Description
31:16	RO	**Device ID** This field is read-only and is set to the device ID 0900h assigned by SiS if auto load is not enabled. If auto load is enabled, it is set to the device ID stored in Serial EEPROM.
15:0	RO	**Vendor ID** This field is read-only and is set to a value of 1039h that is SiS' s PCI Vendor ID if auto load is not enabled. If auto load is enabled, it is set to the vendor ID stored in EEPROM.

Register 04h Configuration Command and Status

Default Value: 02900000h

Access: Read/Write

This register has two parts. The upper 16-bits (31-16) is devoted to device status. The lower 16-bits (15-0) is devoted to command and are used to configure and control the device.

Bit	Access	Description
31	R/W	**Detected Parity Error** The SiS Ethernet Controller sets this bit whenever a parity error is detected, even if the parity error handling is disabled (controlled by command register bit 6). SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.

30	R/W	**Signalled SERR** This bit is set whenever the SiS Ethernet Controller asserts SERR#. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
29	R/W	**Received Master Abort** The SiS Ethernet Controller sets this bit whenever its master transaction is terminated with Master-Abort. SW writes '0' to this bit leaves this bit unchanged.
28	R/W	**Received Target Abort** The SiS Ethernet Controller sets this bit whenever its master transaction is terminated with Target-Abort. SW writes '0' to this bit leaves this bit unchanged.
27	R/W	**Sent Target Abort** The SiS Ethernet Controller sets this bit whenever it terminates a target transaction with Target-Abort. SW writes '0' to this bit leaves this bit unchanged.
26:25	RO	**DEVSEL Timing** This field will always be set to 01 indicating that the SiS Ethernet Controller supports "medium" DEVSEL timing.
24	R/W	**Data Parity Detected** This bit is set when three conditions are met: (1) the bus agent asserted PERR# itself or observed PERR# asserted; (2) The SiS Ethernet Controller acted as the bus master for the operation in which the error occurred; and (3) the Parity Error Response bit in command register is set. SW writes '0' to this bit leaves this bit unchanged.
23	RO	**Fast Back-to-Back Capable** The SiS Ethernet Controller will set this bit to 1.
22	RO	**User Definable Features Supported** The SiS Ethernet Controller does not support User Definable Features, and therefore reads will return a 0.
21	RO	**66MHz Capable** The SiS Ethernet Controller is not 66MHz capable. Reads will return a 0.
20	RO	**Capabilities** The SiS Ethernet Controller will set this bit to 1 indicating implementation of extended capabilities (PCI power management).

19:10		**Reserved** Reads return 0.
9	R/W	**Fast Back-to-Back Enable** Set to 1 by the PCI BIOS to enable the SiS Ethernet Controller to do Fast Back-to-Back transfers (FBB transfers as a master is not implemented in the current revision).
8	R/W	**SERR# Enable** When set, the SiS Ethernet Controller will generate SERR# when an address parity error is detected.
7	RO	**Address Data Stepping** This bit is hardwired to 0 for the SiS Ethernet Controller never do stepping.
6	R/W	**Parity Error Response** When set, The SiS Ethernet Controller will assert PERR# on the detection of a data parity error when acting as the target, and will sample PERR# when acting as the initiator. When reset, data parity errors are ignored. The action taken is specified by CFG: PESEL.
5	RO	**VGA Palette Snoop** The SiS Ethernet Controller does not implement this bit. Reads will return a 0.
4	RO	**Memory Write and Invalidate Enable** Set to 0 indicating that The SiS Ethernet Controller will not generate the Memory Write and Invalidate command.
3	RO	**Special Cycles** Set to 0 indicating that The SiS Ethernet Controller will ignore all Special Cycle operations.
2	R/W	**Bus Master Enable** When set, The SiS Ethernet Controller is allowed to act as a PCI bus master. When reset, The SiS Ethernet Controller is prohibited from acting as a PCI bus master.
1	R/W	**Memory Space Access** When set, The SiS Ethernet Controller responds to memory space accesses. When reset, The SiS Ethernet Controller ignores memory space accesses.

0	R/W	**IO Space Access** When set, The SiS Ethernet Controller responds to IO space accesses. When reset, The SiS Ethernet Controller ignores IO space accesses.

Register 08h Configuration Revision ID

Default Value: 02000080h

Access: Read Only

This register stores silicon revision number, revision number of software interface specification and lets the configuration software know that it is an Ethernet controller in the class of network controllers.

Bit	Access	Description
31:24	RO	**Base Class** Returns 02 which specifies a network controller.
23:16	RO	**Sub Class** Returns 00, which specifies an Ethernet controller.
15:8	RO	**Programming IF** Returns 00, which specifies the first release of The SiS Ethernet Controller Software Interface Specification.
7:0	RO	**Silicon Revision** Returns 80, which specifies the silicon revision.

Register 0Ch Configuration Latency Timer

Default Value: 00000000h

Access: Read/Write

This register gives status and controls such miscellaneous functions as BIST, Latency timer and Cache line size.

Bit	Access	Description
31:24	RO	**Built-in Self Test** The SiS Ethernet Controller do not support BIST. Read will return 0, write is ignored.
23:16	RO	**Header Type** 00h
15:8	R/W	**Latency Timer** Set by software to the number of PCI clocks that The SiS Ethernet Controller may hold the PCI bus.

7:0	RO	**Cache Line Size** Ignored by The SiS Ethernet Controller.

Register 10h Configuration IO Base Address

Default Value: 00000001h

Access: Read/Write

This register specifies the Base I/O address that is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that it can be mapped into I/O space.

Bit	Access	Description
31:8	R/W	**Base IO Address** This is set by software to the base IO address for the Operational Register Map.
7:2	RO	**Size indication** Read back as 0. This allows the PCI bridge to determine that The SiS Ethernet Controller requires 256 bytes of IO space.
1		**Reserved** Reads return 0.
0	RO	**IO Space Indicator** Set to 1 by The SiS Ethernet Controller to indicate that The SiS Ethernet Controller is capable of being mapped into IO space.

Register 14h Configuration Memory Address

Default Value: 00000000h

Access: Read/Write

This register specifies the Base Memory address that is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that it can be mapped into memory space.

Bit	Access	Description
31:12	R/W	**Memory Base Address** This is set by software to the base address for the Operational Register Map.
11:4	RO	**Memory Size** These bits return 0, which indicates that The SiS Ethernet Controller requires 4096 bytes of Memory Space (the minimum recommended allocation)

3	RO	**Prefetchable** Set to 0 by The SiS Ethernet Controller to indicate that The SiS Ethernet Controller does not support this feature.
2:1	RO	**Location Selection** Set to 00 by The SiS Ethernet Controller. This indicates that the base register is 32-bits wide and can be placed anywhere in the 32-bit memory space
0	RO	**Memory Space Indicator** Set to 0 by The SiS Ethernet Controller to indicate that The SiS Ethernet Controller is capable of being mapped into memory space.

Register 2Ch Configuration Subsystem Identification

Default Value: 09001039h

Access: Read Only

This register allows system software to distinguish between different subsystems based on the same PCI silicon.

Bit	Access	Description
31:16	RO	**Subsystem Device ID** This field is set to the device ID 0900h assigned by SiS if auto load is not enabled. If auto load is enabled, it is set to the subsystem ID stored in EEPROM.
15:0	RO	**Subsystem Vendor ID** This field is set to a value of 1039h, which is SiS' s PCI Vendor ID if auto load is not enabled. If auto load is enabled, it is set to the subvendor ID stored in EEPROM.

Register 30h Configuration Expansion ROM Base Address

Default Value: 00000000h

Access: Read/Write

This register specifies the Base Expansion ROM address that is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that the device accepts accesses to its expansion ROM.

Bit	Access	Description
31:17	R/W	**Expansion ROM Base Address** This is set by software to the base address for the Expansion ROM.

16:1		**Reserved** Reads return 0.
0	R/W	**Expansion ROM address decode enable** This The SiS Ethernet Controller will respond to access its expansion ROM when this bit is set and the Memory Space Access bit is set.

Register 34h Configuration Capabilities Pointer

Default Value: 00000040h

Access: Read Only

Bit	Access	Description
31:8		**Reserved** Reads return 0.
7:0	RO	**Capabilities Pointer** It provides an offset into PCI configuration space for the location of the first item in the capabilities linked list. Hardwired to 40' hin The SiS Ethernet Controller to point to CFGPMC.

Register 3Ch Configuration Interrupt Select

Default Value: 0b340300h

Access: Read/Write

This register stores the interrupt line number as identified by the POST software that is connected to the interrupt controller as well as The SiS Ethernet Controller desired settings for maximum latency and minimum grant.

Bit	Access	Description
31:24	RO	**Maximum Latency** The SiS Ethernet Controller desired setting for Max Latency. The SiS Ethernet Controller will initialize this field to 0B (2.75 µsec).
23:16	RO	**Minimum Grant** The SiS Ethernet Controller desired setting for Minimum Grant. The SiS Ethernet Controller will initialize this field to 34 (13 µsec).
15:8	RO	**Interrupt Pin** Always return 0000 0011 (INTC).
7:0	R/W	**Interrupt Line** Set to which line on the interrupt controller that The SiS Ethernet Controller's interrupt pin is connected to.

Register 40h Configuration Power Management Capabilities

Default Value: fe010001h

Access: Read Only

The SiS Ethernet Controller supports both PCI Bus Power Management Interface specifications. revision 1.0 and revision 1.0a. If auto load is enabled, the CFGPMC register is 1.0a version, otherwise it is 1.0 version.

1.0 version:

Bit	Access	Description
31:27	RO	**PME Support** Indicates PME# may be asserted from which power state. If Auxiliary Power Source is present, this 5-bit field is 11111b indicating PME# can be asserted from D0, D1, D2, D3hot and D3cold. If Auxiliary Power Source is absent, this 5-bit field is 01111b indicating PME# can be asserted from D0, D1, D2 and D3hot but cannot be asserted from D3cold.
26	RO	**D2 Support** Set to 1 by The SiS Ethernet Controller to indicate that The SiS Ethernet Controller supports D2 Power Management State.
25	RO	**D1 Support** Set to 1 by The SiS Ethernet Controller to indicate that The SiS Ethernet Controller supports D1 Power Management State.
24:22		**Reserved** Reads return 0.
21	RO	**Device Specific Initialization** Set to 0 by The SiS Ethernet Controller to indicate that The SiS Ethernet Controller does not require a device specific initialization sequence following transition to the D0 uninitialized state.
20		**Reserved** Reads return 0.
19	RO	**PME Clock** Set to 0 by The SiS Ethernet Controller to indicate that no PCI clock is required for The SiS Ethernet Controller to generate PME#.
18:16	RO	**PCI PM Spec. Version** Set to 001b indicates that The SiS Ethernet Controller complies with Revision 1.0 of the PCI Power Management Interface Specification.

15:8	RO	**Next Item Pointer** Set to 00h by The SiS Ethernet Controller to indicate that no additional items in the Capabilities List.
7:0	RO	**Capability ID** Set to 01h by The SiS Ethernet Controller to indicate that the linked list item as being the PCI Power Management registers.

1.0a version:

Bit	Access	Description
31:27	RO	**PME Support** Indicates PME# may be asserted from which power state. If Auxiliary Power Source is present, this 5-bit field is 11111b indicating PME# can be asserted from D0, D1, D2, D3hot and D3cold. If Auxiliary Power Source is absent, this 5-bit field is 01111b indicating PME# can be asserted from D0, D1, D2 and D3hot but cannot be asserted from D3cold.
26	RO	**D2 Support** Set to 1 by The SiS Ethernet Controller to indicate that The SiS Ethernet Controller supports D2 Power Management State.
25	RO	**D1 Support** Set to 1 by The SiS Ethernet Controller to indicate that The SiS Ethernet Controller supports D1 Power Management State.
24:22	RO	**Auxiliary Current** This field reports the 3.3Vaux auxiliary current requirements for The SiS Ethernet Controller.
21	RO	**Device Specific Initialization** Set to 0 by The SiS Ethernet Controller to indicate that The SiS Ethernet Controller does not require a device specific initialization sequence following transition to the D0 uninitialized state.
20		**Reserved** Reads return 0.
19	RO	**PME Clock** Set to 0 by The SiS Ethernet Controller to indicate that no PCI clock is required for The SiS Ethernet Controller to generate PME#.

18:16	RO	**PCI PM Spec. Version** Set to 010b indicates that The SiS Ethernet Controller complies with Revision 1.0a of the PCI Power Management Interface Specification.
15:8	RO	**Next Item Pointer** Set to 00h by The SiS Ethernet Controller to indicate that no additional items in the Capabilities List.
7:0	RO	**Capability ID** Set to 01h by The SiS Ethernet Controller to indicate that the linked list item as being the PCI Power Management registers.

Register 44h Configuration Power Management Control/Status

Default Value: 00000000h

Access: Read/Write

This register is used to manage The SiS Ethernet Controller' s power management state as well as to enable/monitor PME

Bit	Access	Description
31:24	RO	**State Dependent Data** Not implemented in The SiS Ethernet Controller (reads return 0).
23:16	RO	**PMCSR PCI to PCI Bridge Support Extensions** Not implemented in The SiS Ethernet Controller (reads return 0).
15	R/W	**PME Status** This bit is set when The SiS Ethernet Controller would normally assert the PME# signal independent of the state of the PME_EN bit. Writing a ' 1' to this bit will clear it and cause The SiS Ethernet Controller to stop asserting a PME# (if enabled). Writing a ' 0' has no effect. If Auxiliary Power Source is present, i.e. PME# can be asserted from D3cold, then this bit must be explicitly cleared by the operating system each time the operating system is initially loaded. Unchanged by hardware reset.
14:13	RO	**Data Scale** Not implemented in The SiS Ethernet Controller (reads return 0).
12:9	RO	**Data Select** Not implemented in The SiS Ethernet Controller (reads return 0).

8	R/W	**PME Enable** Writing a '1' enables The SiS Ethernet Controller to assert PME#. Writing a '0', PME# assertion is disabled. If Auxiliary Power Source is present, i.e. PME# can be asserted from D3cold, then this bit must be explicitly cleared by the operating system each time the operating system is initially loaded. Unchanged by hardware reset.
7:2		**Reserved** Reads return 0
1:0	R/W	**Power State** This 2-bit field is used both to determine the current power state of The SiS Ethernet Controller and to set The SiS Ethernet Controller into a new power state. The hardware reset value is 00b. The definition of the field values is given below. 00b D0 01b D1 10b D2 11b D3hot

13.3 MAC Operational Registers

The SiS Ethernet Controller provides the following set of operational registers mapped into PCI memory space or I/O space. Writes to reserved register locations may result in unexpected behavior. Reads to reserved register locations will return unspecified value.

Table 13.3-1 Operational Register Map

Register	Tag	Description	Access
00h	CR	Command Register	R/W
04h	CFG	Configuration Register	R/W
08h	EROMAR	EEPROM Access Register	R/W
0Ch	PTSCR	PCI Test Control Register	R/W
10h	ISR	Interrupt Status Register	R/W
14h	IMR	Interrupt Mask Register	R/W
18h	IER	Interrupt Enable Register	R/W
1Ch	ENPHY	Enhanced PHY Access Register	R/W
20h	TXDP	Transmit Descriptor Pointer Register	R/W
24h	TXCFG	Transmit Configuration Register	R/W

28-2Ch		RESERVED	
30h	RXDP	Receive Descriptor Pointer Register	R/W
34h	RXCFG	Receive Configuration Register	R/W
38h	FLOWCTL	Flow Control Register	R/W
3C-44h		RESERVED	
48h	RFCR	Receive Filter Control Register	R/W
4Ch	RFDR	Receive Filter Data Register	R/W
50-ACh		RESERVED	
B0h	PMCTL	Power Management Control Register	R/W
B4h	PMEVT	Power Management Wake-up Event Register	R/W
B8h		RESERVED	
BCh	WAKECRC	Wake-up Sample Frame CRC Register	R/W
C0-ECh	WAKEMASK	Wake-up Sample Frame Mask Registers	R/W
F0-FCh		RESERVED	

Register 00h Command

Default Value: 00000000h

Access: Read/Write

This register is used for issuing commands to The SiS Ethernet Controller. These commands are issued by setting the corresponding bits for the function. Global software reset along with individual reset and enable/disable switches for transmitter and receiver are provided here.

Bit	Access	Description
31-10		**Reserved**
9	R/W	**HomePHY Software Reset** Set to 1 to reset HomePHY and set to 0 to clear reset.

8	R/W	**Reset** Set to 1 to force The SiS Ethernet Controller to a soft reset state, which disables the transmitter and receiver, reinitializes the FIFOs, and resets all affected registers to their soft reset state. This operation implies both a TXR and a RXR. This bit will read back a 1 during the reset operation, and be cleared to 0 by the hardware when the reset operation is complete.
7	R/W	**Software Interrupt** Setting this bit to a 1 forces The SiS Ethernet Controller to generate a hardware interrupt. This interrupt is maskable via the IMR.
6		**Reserved**
5	R/W	**Receiver Reset** When set to a 1, this bit causes the current packet reception to be aborted, the receiver data and status FIFOs to be flushed, and the receiver state machine to enter the idle state (RXE goes to 0). This is a write-only bit and is always read back as 0.
4	R/W	**Transmit Reset** When set to a 1, this bit causes the current transmission to be aborted, the transmitter data and status FIFOs to be flushed, and the transmitter state machine to enter the idle state (TXE goes to 0). This is a write-only bit and is always read back as 0.
3	R/W	**Receiver Disable** Disable the receiver's state machine after any current packets in progress. When this operation has been completed the RXE bit will be cleared to 0. This is a write-only bit and is always read back as 0. If the programmer is silly enough to set both RXD and RXE in the same write, the RXE will be ignored, and RXD will have precedence.
2	R/W	**Receiver Enable** When set to a 1, and the receiver's state machine is idle, then the receiver's machine becomes active. This bit will read back as a 1 whenever the receive state machine is active. After initial power-up, software must insure that the receiver has completely reset before setting this bit (see ISR:RXRCMP)

1	R/W	**Transmit Disable** When set to a 1, halts the transmitter after the completion of the current packet. This is a write-only bit and is always read back as 0. If the programmer is silly enough to set both TXD and TXE in the same write, the TXE will be ignored, and TXD will have precedence.
0	R/W	**Transmit Enable** When set to a 1, and the transmit state machine is idle, then the transmit state machine becomes active. This bit will read back as a 1 whenever the transmit state machine is active. After initial power-up, software must insure that the transmitter has completely reset before setting this bit (see ISR:TXRCMP)

Register 04h Configuration

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31-8		**Reserved**
7	R/W	**PCI Bus Request Algorithm** Selects mode for making requests for the PCI bus. When set to 0 (default), The SiS Ethernet Controller will use an aggressive Request scheme. When set to a 1, The SiS Ethernet Controller will use a more conservative scheme.
6	R/W	**Single Backoff** Setting this bit to 1 forces the transmitter backoff state machine to always backoff for a single 802.3 slot time instead of following the 802.3 random backoff algorithm. 0 (default) allows normal transmitter backoff operation.
5	R/W	**Program Out of Window Timer** This bit controls when the Out of Window collision timer begins counting its 512-bit slot time. A 0 causes the timer to start after the SFD is received. A 1 causes the timer to start after the first bit of the preamble is received.
4	R/W	**Excessive Deferral Timer disable** Setting this bit to 1 will inhibit transmit errors due to excessive deferral. This will inhibit the setting of the ED status.

3	R/W	**Parity Error Detection Action** This bit control the assertion of SERR when a data parity error is detected while The SiS Ethernet Controller is acting as the bus master. When set, parity errors will not result in the assertion of SERR. When reset, parity errors will result in the assertion of SERR, indicating a system error.
2-1		**Reserved**
0	R/W	**Big Endian Mode** When set, The SiS Ethernet Controller will perform bus-mastered data transfers in "big endian" mode. Note that access to register space is unaffected by the setting of this bit.

Register 08h Serial EEPROM Access

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31-8		**Reserved**
7	R/W	**HomePHY Register Access** Set to 1 to access HomePHY registers and set to 0 to access EEPROM.
6-4		**Reserved**
3	R/W	**EEPROM Chip Select / HomePHY Register Select** In EEPROM chip select mode, it controls the value of the EECS pin. When set, the EECS pin is 1; when clear the EECS pin is 0. In HomePHY register select mode, set to 0 to enable access.
2	R/W	**EEPROM Serial Clock / HomePHY Register Serial Clock** In EEPROM chip select mode, it controls the value of the EESK pin. When set, the EESK pin is 1; when clear the EESK pin is 0. In HomePHY register select mode, when set, serial clock is 1; when clear, serial clock is 0.
1	RO	**EEPROM Data Out / HomePHY Register Data Out** In EEPROM chip select mode, it returns the current state of the EEDO/PA2 pin when EECS is 1. When EECS is 0, this bit returns 0. In HomePHY register select mode, it returns the data of HomePHY register.

0	R/W	**EEPROM Data In / HomePHY Register Data In** In EEPROM chip select mode, it controls the value of the EEDI pin. In HomePHY register select mode, it controls the data input of HomePHY register.

Register 08h PCI Test Control

Default Value: 34000000h

Access: Read/Write

Bit	Access	Description
31		**Reserved**
30	R/W	**Discard Timer Test Mode** Setting this bit to 1, the discard timer for delay transaction will have an initial value of 3ff0h. Setting this bit to 0, the initial value of the discard timer will be 0 and the counter expires when up-count to 3fffh. Default value is set to 0.
29-28		**Reserved**
27-24	R/W	**Boot ROM Access Time** This field adjusts the boot ROM access time. The default value is 0100b that equal to 4 PCI clocks.
23-21		**Reserved**
20-12	R/W	**TX/RX RAM address** Used as the address for the Transmit/Receive data FIFO when accessed through TXCFG/RXCFG during RAM test mode.
11-10		**Reserved**
9	R/W	**Bus Master Test Enable** When enabled (set to 1), the bus master test mode allows the TX buffer manager to be used as a bus master read cycle generator, and the RX buffer manager to be used as a bus master write cycle generator. While in this test mode, normal buffer manager operation is inhibited. The BMTEN bit should only be set to 1 after the TX and RX have been reset and disabled. After setting BMTEN to 0, the TX and RX must be reset and reconfigured to allow normal operation to resume.
8		**Reserved**

7	R/W	**Receive RAM Test Mode Enable** Set this bit to 1 to enable Receive RAM Test mode, which will allow read/write access to the RX data FIFO. The address is specified in bit20-12 RAM address field. The data is written to or read from the RXCFG register.
6	R/W	**Transmit RAM Test Mode Enable** Set this bit to 1 to enable Transmit RAM Test mode, which will allow read/write access to the TX data FIFO. The address is specified in bit20-12 RAM address field. The data is written to or read from the TXCFG register.
5	R/W	**Status RAM Test Mode Enable** Set this bit to 1 to enable Status RAM Test mode, which will allow read/write access to the RX status FIFO. The address is specified in bit4-0 Status RAM address field. The data is written to or read from the RXCFG register.
4-0	R/W	**Status RAM address** Used as the address for the receiver status FIFO when accessed through RXCFG during RAM test mode.

Bus Master Read Cycle Test Mode Generation

When the BMTEN bit is set to 1, the TX buffer manager will generate bus master read cycles on command. Several of the TX operational register bit fields are redefined to facilitate control of this mode.

TXDP Read cycle starting address (dword aligned only).

TXCFG:DRTH Length of read cycle in bytes (1-335 bytes). The actual length value is derived as follows: length[8:0] = {DRTH[5], 0, DRTH[4], 0, 0, DRTH[3:0]}.

NOTE: TXCFG:MXDMA is still utilized while in this test mode to control the maximum DMA size. It is recommended that TXCFG:MXDMA be set to 0 so that the byte count in TXCFG:DRTH will control the DMA length.

CR:TXE Write a "1" to this bit will invoke the read cycle.

The sequence required to generate bus master read cycle is as follows:

Write a 1 to CR:TXR (not necessary if this mode is invoked immediately after reset)

Write a 1 to PTSCR:BMTEN

Write a Dword aligned starting address to the TXDP reg

Write a byte length to the TXCFG:DRTH

Write a 1 to the CR:TXE

All data read during this bus master cycle is discarded (bit bucket). Read cycles can be initiated repetitively without resetting TX between cycles. TXDP, and TXCFG data are retained between cycles.

Bus Master Write Cycle Test Mode Generation

When the BMTEN bit is set to 1, the RX buffer manager will generate bus master write

cycles on command. Several of the RX operational register bit fields are redefined to facilitate control of this mode.

RXDP	Write cycle starting address (Dword aligned only).
RXCFG:DRTH	Length of write cycle in bytes (1-335 bytes). The actual length value is derived as follows: length[8:0] = {DRTH[5], 0, DRTH[4], 0, 0, DRTH[3:0]}. **NOTE**: RXCFG:MXDMA is still utilized while in this test mode to control the maximum DMA size. It is recommended that RXCFG:MXDMA be set to 0 so that the byte count in the RXCFG:DRTH bits will control the DMA length.
RXstatus[22:0]	Write cycle data (this data byte value is used for all byte lanes – see below for data pattern)
CR:RXE	Writing a "1" to this bit will invoke the write cycle

Data from the Receive status FIFO is used to provide the bus data for the write cycles. A location in the RX status FIFO must be written and read using RAM test mode to initialize the desired data pattern. The status data mapping used for each byte lane (little endian) during the generated write cycles is as follows:

byte 0 : status[7:0]

byte 1 : status[15:8]

byte 2 : {status[0], status[22:16]}

byte 3 : status[8:1]

The sequence required to generate bus master write cycle is as follows:

Write a 1 to CR:RXR (not necessary if this mode is invoked immediately after reset)

Write a 1 to PTSCR:SRTMEN and 00000 to PTSCR:SRAMADR[4:0]

Write desired data pattern to RXCFG (Note: Only bits 22-0 are used)

Read RXCFG

Write a 1 to PTSCR:BMTEN

Write a dword aligned starting address to the RXDP register

Write a byte length to the RXCFG:DRTH

Write a 1 to the CR:RXE

Write cycles can be initiated repetitively without resetting RX between cycles. RXDP, RX status, and RXCFG data are retained between cycles.

The sequence from step 1 to step 4 also describes the status RAM test mode procedure, as a example with address 00000. Similarly, Transmit and Receive RAM test mode can be achieved as follows:

1. Write a 1 to CR:TXR (not necessary if this mode is invoked immediately after reset)
2. Write a 1 to PTSCR:TRTMEN and the address to PTSCR:TRRAMADR[20:12]
3. Write desired data pattern to TXCFG
4. Read RXCFG

Register 10h Interrupt Status

Default Value: 03008000h

Access: Read Only

This register indicates the source of an interrupt when the INTA pin goes active. Enabling the corresponding bits in the Interrupt Mask Register (IMR) allows bits in this register to produce an interrupt. When an interrupt is active, one or more bits in this register are set to a "1". The Interrupt Status Register reflects all current pending interrupts, regardless of the state of the corresponding mask bit in the IMR. Reading the ISR clears all interrupts. Writing to the ISR has no effect.

Bit	Access	Description
31-29		**Reserved**
28	RO	**Wake Up Event** Indicates that there is wake-up event occurs. This bit is a wired version of PM Event registers bits, it's not a registered one. So this bit will not be cleared by read operation like others status bits do, it is read as '0' when all PM Event registers bits are cleared.
27	RO	**End of Transmission Pause** Indicates pause command is completed when pause timer expires.
26	RO	**Start of Transmission Pause** Indicates data transmission is paused.
25	RO	**Transmit Reset Complete** Indicates that a requested transmit reset operation is complete.
24	RO	**Receive Reset Complete** Indicates that a requested receive reset operation is complete.
23	RO	**Detected Parity Error** This bit is set whenever CFGCS:DPERR is set, but cleared (like all other ISR bits) when the ISR register is read.
22	RO	**Signaled System Error** The SiS Ethernet Controller signaled a system error on the PCI bus.
21	RO	**Received Master Abort** The SiS Ethernet Controller received a master abort on the PCI bus.
20	RO	**Received Target Abort** The SiS Ethernet Controller received a target abort on the PCI bus.
19-17		**Reserved**

16	RO	**RX Status FIFO Overrun** Set when an overrun condition occurs on the RX Status FIFO.
15	RO	**High Bits Error Set** A logical OR of bits 25-16
14-13		**Reserved**
12	RO	**Software Interrupt** Set whenever the SWI bit in the CR register is set.
11		**Reserved**
10	RO	**TX Underrun** Set when a transmit data FIFO underrun condition occurs.
9	RO	**TX Idle** This event is signaled when the transmit state machine enters the idle state from a non-idle state. This will happen whenever the state machine encounters an "end-of-list" condition (NULL link field or a descriptor with OWN clear).
8	RO	**TX Packet Error** This event is signaled after the last transmit descriptor in a failed transmission attempt that has been updated with valid status.
7	RO	**TX Descriptor** This event is signaled after a transmitter descriptor with the INTR bit set in the CMDSTS field that has been updated.
6	RO	**TX Packet OK** This event is signaled after the last transmit descriptor in a successful transmission attempt has been updated with valid status
5	RO	**RX Overrun** Set when a receive data FIFO overrun condition occurs.
4	RO	**RX Idle** This event is signaled when the receive state machine enters the idle state from a running state. This will happen whenever the state machine encounters an "end-of-list" condition (NULL link field or a descriptor with OWN set).

3	RO	**RX Early Threshold** Indicates that the initial RX Drain Threshold has been met by the incoming packet, and the transfer of the number of bytes specified by the DRTH field in the RXCFG register has been completed by the receive DMA engine. This interrupt condition will occur only once per packet.
2	RO	**RX Packet Error** This event is signaled after the last receive descriptor in a failed packet reception that has been updated with valid status.
1	RO	**RX Descriptor** This event is signaled after a receiver descriptor with the INTR bit set in the CMDSTS field that has been updated.
0	RO	**RX OK** Set by the receive state machine following the update of the last receive descriptor in a good packet.

Register 14h Interrupt Mask

Default Value: 00000000h

Access: Read/Write

This register masks the interrupts that can be generated from the ISR. Writing a "1" to the bit enables the corresponding interrupt. During hardware reset, all mask bits are cleared.

Bit	Access	Description
31-29		**Reserved**
28	R/W	**Wake Up Event** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
27	R/W	**End of Transmission Pause** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
26	R/W	**Start of Transmission Pause** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
25	R/W	**Transmit Reset Complete** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.

24	R/W	**Receive Reset Complete** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
23	R/W	**Detected Parity Error** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
22	R/W	**Signaled System Error** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
21	R/W	**Received Master Abort** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
20	R/W	**Received Target Abort** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
19-17		**Reserved**
16	R/W	**RX Status FIFO Overrun** Set when an overrun condition occurs on the RX Status FIFO.
15	R/W	**High Bits Error Set** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
14-13		**Reserved**
12	R/W	**Software Interrupt** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
11		**Reserved**
10	R/W	**TX Underrun** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
9	R/W	**TX Idle** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
8	R/W	**TX Packet Error** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.

7	R/W	**TX Descriptor** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
6	R/W	**TX Packet OK** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
5	R/W	**RX Overrun** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
4	R/W	**RX Idle** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
3	R/W	**RX Early Threshold** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
2	R/W	**RX Packet Error** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
1	R/W	**RX Descriptor** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
0	R/W	**RX OK** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.

The Interrupt Mask Register provides a mechanism for enabling individual interrupt sources in the Interrupt Status Register (ISR). Setting a mask bit allows the corresponding bit in the ISR to cause an interrupt. ISR bits are always set to 1, however, if the condition is present, regardless of the state of the corresponding mask bit.

Register 18h Interrupt Enable

Default Value: 00000000h

Access: Read/Write

The Interrupt Enable Register controls the hardware INTR signal.

Bit	Access	Description
31-1		**Reserved**

0	R/W	**Interrupt Enable** When set to 1, the hardware INTR signal is enabled. When set to 0, the hardware INTR signal will be masked, and no interrupts will be generated. The setting of this bit has no effect on the ISR or IMR. This provides the ability to disable the hardware interrupt to the host with a single access (eliminating the need for a read-modify-write cycle).

Register 1Ch Enhanced PHY Access

Default Value: 00000000h

Access: Read/Write

The SiS Ethernet Controller provides ten internal MII PHY registers for internal PHY configuration settings and status readings. Driver can access the ten internal MII registers by defining the command, Register offset, desired data from the ENPHY resister listed below.

Bit	Access	Description
31-16	R/W	**R/W PHY Data** When write, this field specifies the data written to PHY register. When read, this field contains the data returned by PHY.
15-11		**Reserved**
10-6	R/W	**Register Address of PHY** Indicates the offset of PHY register.
5	R/W	**Access CMD to PHY** When '1', HW will issue a read operation to PHY registers, when '0', HW will issue a write operation. This field is valid only when bit 4 is '1'.
4	R/W	**SW Access Request/HW Done** When SW wants to access PHY register, it sets this bit to request HW. For such operation, HW will perform the access operation in a proper time, when finished, it clears this bit. SW can't change the PHY access contents if the current access is not done.
3-0		**Reserved**

Register 20h Transmit Descriptor Pointer

Default Value: 00000000h

Access: Read/Write

This register points to the current Transmit Descriptor.

Bit	Access	Description

31-2	R/W	**Transmit Descriptor Pointer** The current value of transmitter descriptor pointer. When the transmit state machine is idle, software must set TXDP to the address of a completed transmit descriptor. While the transmit state machine is active, TXDP will follow the state machine as it advances through a linked list of active descriptors. If the link field of the current transmit descriptor is NULL (signifying the end of the list), TXDP will not advance, but will remain on the current descriptor. Any subsequent writes to the TXE bit of the CR register will cause the transmit state machine to reread the link field of the current descriptor to check for new descriptors that may have been appended to the end of the list. Transmit descriptors must be aligned on an even 32-bit boundary in host memory (A1-A0 must be 0).
1-0		**Reserved**

Register 24h Transmit Configuration

Default Value: 00800102h

Access: Read/Write

This register defines the Transmit Configuration for The SiS Ethernet Controller. It controls such functions as Loopback, Auto Transmit Padding, Fill & Drain Thresholds, and maximum DMA burst size.

Bit	Access	Description
31	R/W	**Carrier Sense Ignore** Setting this bit to 1 causes the transmitter to ignore carrier sense activity, which inhibits reporting of CRS status to the transmitter status register. When this bit is 0 (default), the transmitter will monitor the CRS signal during transmission and reflect valid status in the transmitter status register. This bit must be set to enable full-duplex operation.
30	R/W	**HeartBeat Ignore** Setting this bit to 1 causes the transmitter to ignore the heartbeat (CD) pulse that follows the packet transmission. When this bit is set to 0 (default), the transmitter will monitor the heartbeat pulse. This bit must be set to enable full-duplex operation

29	R/W	**MAC Loopback** Setting this bit to a 1 places The SiS Ethernet Controller into a controller loopback state which routes all transmit traffic to the receiver, and disables the transmit and receive interfaces of the MII. A 0 in this bit allows normal MAC operation. The transmitter and receiver must be disabled before enabling the loopback mode. (Packets received during MLB mode will reflect loopback status in the receive descriptor' s CMDSTS.LBP field.)
28	R/W	**Automatic Transmit Padding** Setting this bit to 1 causes the MAC to automatically pad small (runt) transmit packets to the Ethernet minimum size of 64 bytes. This allows driver software to transfer only actual packet data. Setting this bit to 0 disables the automatic padding function, forcing software to control runt padding.
27-25		**Reserved**
24-23		**Writes are ignored, reads return 01.**
22-20	R/W	**Max DMA Burst Size per TX DMA Burst** This field sets the maximum size of transmit DMA data bursts according to the following table: 000 128 x 32-bit words (512 bytes) 001 1 x 32-bit word (4 bytes) 010 2 x 32-bit words (8 bytes) 011 4 x 32-bit words (16 bytes) 100 8 x 32-bit words (32 bytes) 101 16 x 32-bit words (64 bytes) 110 32 x 32-bit words (128 bytes) 111 64 x 32-bit words (256 bytes)
19-14		**Reserved**
13-8	R/W	**TX Fill Threshold** Specifies the fill threshold in units of 32 bytes. When the number of available bytes in the transmitter FIFO reaches this level, the transmit bus master state machine will be allowed to request the PCI bus for transmit packet fragment reads. A value of 0 in this field will produce unexpected results and must not be used.
7-6		**Reserved**

5-0	R/W	**TX Drain Threshold** Specifies the drain threshold in units of 32 bytes. When the number of bytes in the FIFO reaches this level (or the FIFO contains at least one complete packet) the MAC transmit state machine will begin the transmission of a packet. NOTE: In order to prevent a deadlock condition from occurring, the transmit drain threshold should never be set higher than the (TXFIFOSize – TXCFG:FLTH). A value of 0 in this field will produce unexpected results and must not be used.

Register 30h This register points to the current Receive Descriptor.

Default Value: 00000000h

Access: Read/Write

This register points to the current Receive Descriptor.

Bit	Access	Description
31-2	R/W	**Receive Descriptor Pointer** The current value of the receiver descriptor pointer. When the receive state machine is idle, software must set RXDP to the address of an available receive descriptor. While the receive state machine is active, RXDP will follow the state machine as it advances through a linked list of available descriptors. If the link field of the current receive descriptor is NULL (signifying the end of the list), RXDP will not advance, but will remain on the current descriptor. Any subsequent writes to the RXE bit of the CR register will cause the receive state machine to reread the link field of the current descriptor to check for new descriptors that may have been appended to the end of the list. Software should not write to this register unless the receive state machine is idle. Receive descriptors must be aligned on 32-bit boundaries (A1-A0 must be zero).
1-0		**Reserved**

Register 34h Receive Configuration

Default Value: 00000002h

Access: Read/Write

This register is used to set the receiver configuration for The SiS Ethernet Controller. Receive properties such as accepting error packets, runt packets, setting the receive drain threshold etc. are controlled here.

Bit	Access	Description

31	R/W	**Accept Errors Packets** When set to 1, all packets with CRC, alignment, and/or collision errors will be accepted. When set to 0, all packets with CRC, alignment, and/or collision errors will be rejected if possible. Note that depending on the type of error, some packets may be received with errors, regardless of the setting of AEP. These errors will be indicated in the CMDSTS field of the last descriptor in the packet.
30	R/W	**Accept Runt Packets** When set to 1, all packets under 64 bytes in length without errors are accepted. When this bit is 0, all packets less than 64 bytes in length will be rejected if possible.
29		**Reserved**
28	R/W	**Accept Transmit Packets** When set to 1, data received simultaneously to a local transmission (such as during a PMD loopback or full duplex operation) will be accepted as valid received data. Additionally, when set to 1, the receiver will ignore collision activity. When set to 0 (default), all data receive simultaneous to a local transmit will be rejected. This bit must be set to 1 for PMD loopback and full duplex operation.
27	R/W	**Accept Jabber Packets** When set to 1, all packets over 1518 bytes in length (to a maximum of 2046 bytes) will be accepted and placed in the receive data buffers (if buffers that large are specified in the receive descriptor list). When set to 0, packets larger than 1518 bytes (CRC inclusive) will be rejected if possible. A byte count of 2046 indicates that the packet may have been truncated.
26-23		**Reserved**

22-20	R/W	**Max DMA Burst Size per RX DMA Burst** This field sets the maximum size of receive DMA data bursts according to the following table: 000 128 x 32-bit words (512 bytes) 001 1 x 32-bit word (4 bytes) 010 2 x 32-bit words (8 bytes) 011 4 x 32-bit words (16 bytes) 100 8 x 32-bit words (32 bytes) 101 16 x 32-bit words (64 bytes) 110 32 x 32-bit words (128 bytes) 111 64 x 32-bit words (256 bytes)
19-6		**Reserved**
5-1	R/W	**RX Drain Threshold** Specifies the drain threshold in units of 8 bytes. When the number of bytes in the receiver FIFO reaches this value (times 8), or the FIFO contains a complete packet, the receive bus master state machine will begin the transfer of data from the FIFO to host memory. Care must be taken when setting DRTH to a value lower than the number of bytes needed to determine if packet should be accepted or rejected. In this case, the packet might be rejected after the bus master operation to begin transferring the packet into memory has begun. When this occurs, neither the OK bit nor any error status bit in the descriptor' s CMDSTS will be set. A value of 0 is illegal, and the results are undefined. This value is also used to compare with the accumulated packet length for early receive indication. When the accumulated packet length meets or exceeds the DRTH value, the RXEARLY interrupt condition is generated.
0		**Reserved**

Register 38h Flow Control

Default Value: 00000000h

Access: Read/Write

The FLOWCTL register is used to control and configure The SiS Ethernet Controller Flow Control logic. The Flow Control Logic is used to detect PAUSE frame packets and control data frame transmission.

Bit	Access	Description
31-2		**Reserved**

1	R/W	**PAUSE Flag** When "1" indicates data frame transmission is paused. When "0" transmission is normal. This bit is reset by H/W reset, 900 soft reset, transmit reset, pause timer expires or S/W write 0 to this bit.
0	R/W	**Flow Control Enable** Set to 1, enable the PAUSE frame detection. Set to 0, disable the PAUSE frame detection. This bit is reset only by H/W reset.

Register 48h Receive Filter Control

Default Value: 00000000h

Access: Read/Write

The RFCR register is used to control and configure The SiS Ethernet Controller Receive Filter Control logic. The Receive Filter Control Logic is used to configure destination address filtering of incoming packets.

Bit	Access	Description
31	R/W	**RX Filter Enable** When this bit is set to 1, the RX Filter is enabled to qualify incoming packets. When set to 0, receive packet filtering is disabled (i.e. all receive packets are rejected).
30	R/W	**Accept All Broadcast** When set to 1, this bit causes all broadcast address packets to be accepted. When set to 0, no broadcast address packets will be accepted.
29	R/W	**Accept All Multicast** When set to 1, this bit causes all multicast address packets to be accepted. When set to 0, multicast destination addresses must have the appropriate bit set in the multicast hash table mask in order for the packet to be accepted.
28	R/W	**Accept All Physical** When set to 1, this bit causes all physical address packets to be accepted. When set to 0, the destination address must match the node address register in order for the packet to be accepted.
27	R/W	**HomePHY Or 802.3u PHY Select** When set to 1, HomePHY is selected and set to 0 to select 802.3u PHY.
26-20		**Reserved**

19-16	R/W	**Receive Filter Address** Selects which internal receive filter register is accessible via RFDR: 0000 node address octets 1-0 0001 node address octets 3-2 0010 node address octets 5-4 0011 RESERVED 0100 multicast hash table bits 15-0 0101 multicast hash table bits 31-16 0110 multicast hash table bits 47-32 0111 multicast hash table bits 63-48 1000 multicast hash table bits 79-64 1001 multicast hash table bits 95-80 1010 multicast hash table bits 111-96 1011 multicast hash table bits 127-112 others RESERVED
15-0		**Reserved**

Register 4Ch Receive Filter Data

Default Value: 00000000h

Access: Read/Write

The RFDR register is used for reading from and writing to the internal receive filter registers (unique address register, and the hash table register).

Bit	Access	Description
31-16		**Reserved**
15-0	R/W	Receiver Filter Data

The Receive Filter Logic uses the following algorithm when qualifying incoming packets for reception:

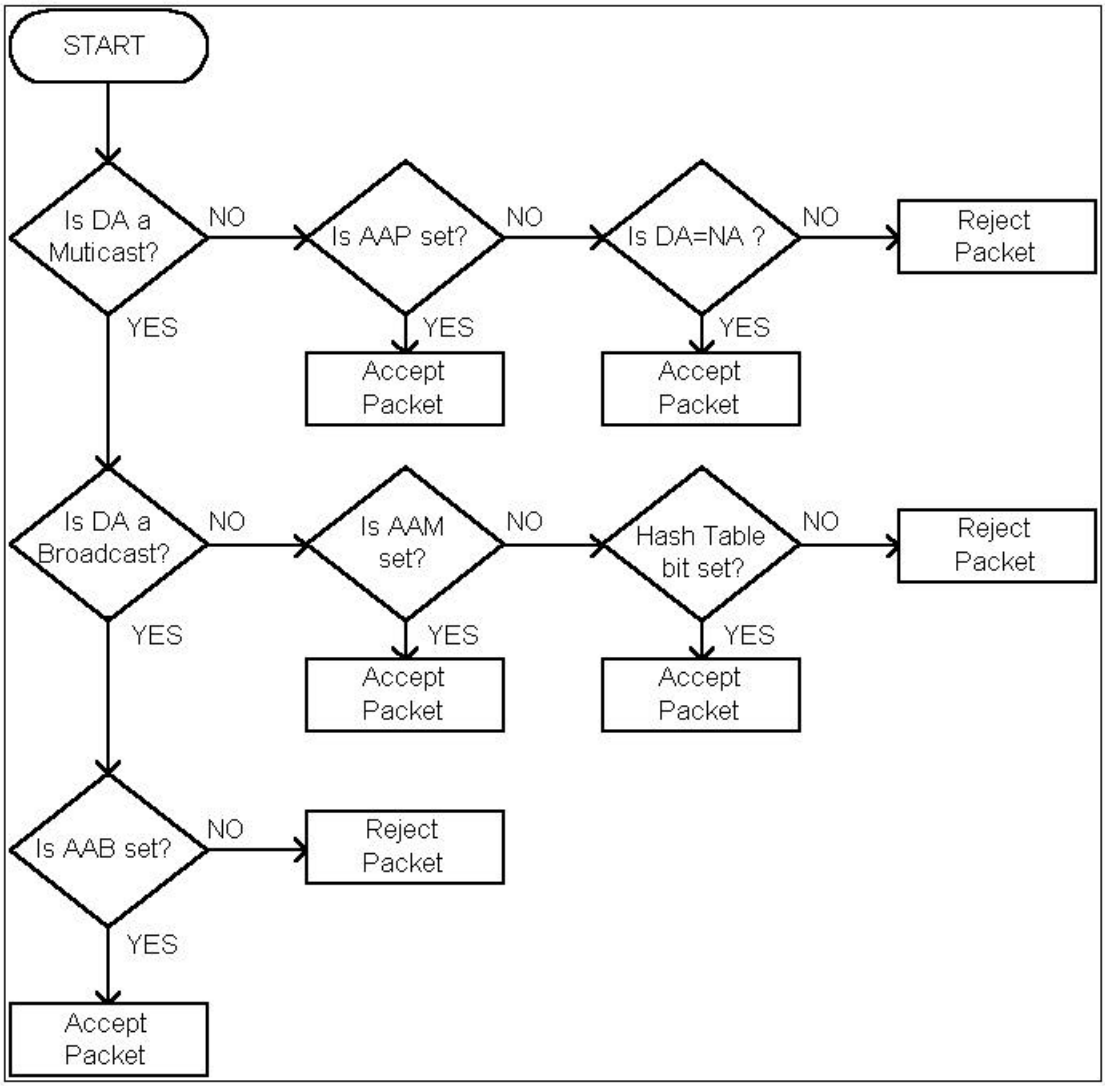


Figure 13.3-1 Receive Filter Algorithm

The *Node Address* register is a 48-bit register internal to the Receive Filter logic. When RFCR:AAP is clear, then the receive filter logic will only accept unicast packets which match the contents of the node address register. Octet 0 of the node address register corresponds to the first octet of the packet as it appears on the wire. Octet 5 of the node address register corresponds to the last octet of the destination address as it appears on the wire. For example, to configure a node address of 00-E0-06-07-28-55,

octet	0	1	2	3	4	5
	00000000	11100000	00000110	00000111	00101000	01010101
	00	E0	06	07	28	55

(as it appears on the wire)

Software would need to execute the following series of register operations:

```
out32( RFCR, 0x00000000 );     /* disable receive filter, NA(0) */
out32( RFDR, 0x0000E000 );     /* load octets 0 and 1 */
out32( RFCR, 0x00010000 );     /* select NA[1] */
out32( RFDR, 0x00000706 );     /* load octets 2 and 3 */
out32( RFCR, 0x00020000 );     /* select NA[2] */
out32( RFDR, 0x00005528 );     /* load octets 4 and 5 */
out32( RFCR, 0xC0000000 );     /* enable receive filter, accept broadcasts */
```

The *Multicast Hash Table* register can be configured to perform imperfect filtering of multicast packets. If the receive packet's destination address is a multicast address (but not the broadcast address) and the RFCR:AAM is not set, then the receive filter logic will use the 7 most significant bits of the destination address's CRC as an index into the Multicast Hash Table register. If the corresponding bit is set, then the packet is accepted, otherwise the packet is rejected. Refer to Appendix B - Hash Table Index Computation.

Register B0h Power Management Control

Default Value: 00000000h

Access: Read/Write

This register provides SW an interface to control which Power Management Event to assert PME# / INTA#. The contents of this register should be well-programmed before set the Ethernet Controller into power saving state, and will not be affected by PCI HW reset. It can be reset by software reset (OP register offset 00h bit8) except ISOSEL.

Bit	Access	Description
31	R/W	**Gate Dual Target Clock Enable** When '1', the clock of dual powered blocks will be gated when in (D3cold and (not PME_EN)). When '0', the clock of dual powered blocks will never be gated.
30	R/W	**Wake-up While Receive OK Packet** When '1', any packet that passed the RXFilter with no error will cause a wake-up event. This may include any broadcast, multicast, or direct addressed packet depending on how RXFilter is programmed.
29-27		**Reserved**
26	R/W	**3rd Wake-up Frame Access** When '1', access to WAKECRC is indirectly mapped to the 3rd wake-up frame CRC register. FRM3ACS, FRM2ACS, and FRM1ACS are supposed not to be set at the same time for read access.

25	R/W	**2nd Wake-up Frame Access** When '1', access to WAKECRC is indirectly mapped to the 2nd wake-up frame CRC register. FRM3ACS, FRM2ACS, and FRM1ACS are supposed not to be set at the same time for read access.
24	R/W	**1st Wake-up Frame Access** When '1', access to WAKECRC is indirectly mapped to the 1st wake-up frame CRC register. FRM3ACS, FRM2ACS, and FRM1ACS are supposed not to be set at the same time for read access.
23		**Reserved**
22	R/W	**3rd Wake-up Frame Match Enable** When this bit is '1', and PME_EN is '1', the 3rd wake-up mechanism of receipt of a network wake-up frame is enabled.
21	R/W	**2nd Wake-up Frame Match Enable** When this bit is '1', and PME_EN is '1', the 2nd wake-up mechanism of receipt of a network wake-up frame is enabled.
20	R/W	**1st Wake-up Frame Match Enable** When this bit is '1', and PME_EN is '1', the 1st wake-up mechanism of receipt of a network wake-up frame is enabled.
19-12		**Reserved**
11	R/W	**Magic PacketTM Match Algorithm** When '1', a strict magic packet match algorithm is used when detect magic packet. When '0', a loose magic packet match algorithm is used when detects magic packet.
10	R/W	**Magic PacketTM Match Enable** When this bit is '1', and PME_EN is '1', the wake-up mechanism of receipt of a Magic Packet is enabled.
9-2		**Reserved**
1	R/W	**Link On Monitor Enable** When this bit is '1', and PME_EN is '1', the wake-up mechanism of detection the link on state is enabled.
0	R/W	**Link Loss Monitor Enable** When this bit is '1', and PME_EN is '1', the wake-up mechanism of detection the link loss state is enabled.

Register B4h Power Management Wake-up Event

Default Value: 00000000h

Access: Read/Write

This register records which wake-up event wake up the system. This register is not affected by PCI HW reset. It can be reset only by software reset (OP register offset 00h bit8). SW writes 1 will clear the individual bits. SW writes 0 will leave the individual bits unchanged.

Bit	Access	Description
31		**Reserved**
30	R/W	**Receive OK Packet** H/W sets this bit whenever bit30 of PM Control Register is '1' and an incoming packet passes the RXFilter with no error. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
29-23		**Reserved**
22	R/W	**Match 3rd Wake-up Sample Frame** H/W sets this bit whenever bit22 of PM Control Register is '1' and receipt of the pre-defined 3rd wake-up frame with no error. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
21	R/W	**Match 2nd Wake-up Sample Frame** H/W sets this bit whenever bit21 of PM Control Register is '1' and receipt of the pre-defined 2nd wake-up frame with no error. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
20	R/W	**Match 1st Wake-up Sample Frame** H/W sets this bit whenever bit20 of PM Control Register is '1' and receipt of the pre-defined 1st wake-up frame with no error. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
19-11		**Reserved**
10	R/W	**Magic Packet™ Match** H/W sets this bit whenever bit10 of PM Control Register is '1' and receipt of a magic packet with no error. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
9-2		**Reserved**

1	R/W	**Link On Event** H/W sets this bit whenever bit1 of PM Control Register is '1' and link status changes from loss to on. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
0	R/W	**Link Loss Event** H/W sets this bit whenever bit0 of PM Control Register is '1' and link status changes from on to loss. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.

Register BCh Wake-up Sample Frame CRC

Default Value: 00000000h

Access: Read/Write

This register provides an access window to the CRC values of the mask bytes in wake-up sample frames. When FRM3ACS, FRM2ACS, or FRM1ACS is '1', the CRC value of the mask bytes in the corresponding wake-up sample frame can be accessed through this register. FRM3ACS, FRM2ACS, and FRM1ACS are supposed not to be set at the same time for read access. If the CRC value of those incoming bytes, whose byte mask is set to 1 in the sample frame, equals to the CRC value in the sample frame, then the incoming frame is considered a wake-up frame. This register is not affected by PCI HW reset. It can be reset only by software reset (OP register offset 00h bit8).

Bit	Access	Description
31-0	R/W	**Wake-up Frame CRC Value** This field specifies the CRC value of the mask bytes in the corresponding wake-up sample frame specified by FRM3ACS, FRM2ACS, and FRM1ACS. H/W uses this 32-bit CRC value to match the 32-bit CRC value of incoming frame mask bytes. If matched, the incoming frame is a wake-up frame and PME# will be asserted if enabled.

13.3.1 Wake-up Sample Frame Byte Mask Register

These registers provide the mask bytes in wake-up sample frames. These registers are not affected by PCI HW reset. They can be reset by software reset (OP register offset 00h bit8).

Register	Size	R/W	Description
C0h	32	R/W	The 1st 32 byte mask in the 1st Wake-up sample frame.
C4h	32	R/W	The 2nd 32 byte mask in the 1st Wake-up sample frame.
C8h	32	R/W	The 3rd 32 byte mask in the 1st Wake-up sample frame.

CCh	32	R/W	The 4th 32 byte mask in the 1st Wake-up sample frame.
D0h	32	R/W	The 1st 32 byte mask in the 2nd Wake-up sample frame.
D4h	32	R/W	The 2nd 32 byte mask in the 2nd Wake-up sample frame.
D8h	32	R/W	The 3rd 32 byte mask in the 2nd Wake-up sample frame.
DCh	32	R/W	The 4th 32 byte mask in the 2nd Wake-up sample frame.
E0h	32	R/W	The 1st 32 byte mask in the 3rd Wake-up sample frame.
E4h	32	R/W	The 2nd 32 byte mask in the 3rd Wake-up sample frame.
E8h	32	R/W	The 3rd 32 byte mask in the 3rd Wake-up sample frame.
ECh	32	R/W	The 4th 32 byte mask in the 3rd Wake-up sample frame.

13.4 MII PHY Registers

SiS540 has eleven internal MII PHY 16 bit registers. Ten registers are available for setting configuration inputs and reading status outputs and one register is reserved for factory use. The ten accessible registers consist of six registers that are defined by IEEE 802.3 specification (MI Register 0-5) and four registers that are unique to SiS540 (MI Register 16-19).

The accesses of the ten MI PHY Registers are through MAC Operational Register ENPHY (offset 1Ch). Users can define the command (RWCMD, ENPHY bit 5), the Register Offset (REGADDR, ENPHY bit 10-6), and the Data contents (PHYDATA, ENPHY bit 31-16). And then the driver issue the access command bit by writing '1' to register ENPHY bit 4, ACCESS, and wait for SiS540 complete the operation which should return '0' when completed.

Table 13.4-1 PHY Configuration Register Map

Register	Tag	Description	Access
00h	CONTROL	MI Register 0 Control Register	RO
01h	STATUS	MI Register 1 Status Register	R/W
02h	PHYID1	MI Register 2 PHY ID#1	RO
03h	PHYID2	MI Register 3 PHY ID#2	R/W
04h	AUTOADV	MI Register 4 Auto Negotiation Advertisement	R/W
05h	AUTOREC	MI Register 5 Auto Negotiation Remote End Capability	R/W
10h	CONFIG1	MI Register 16 Configuration 1	R/W
11h	CONFIG2	MI Register 17 Configuration 2	R/W
12h	STSOUT	MI Register 18 Status Output	R/LT
13h	MASK	MI Register 19 Mask	R/W

14h	RESERVED	MI Register 20 Reserved	R/W

Register 00h CONTROL

Default Value: 3000h

Access: Read/Write

Bit	Access	Description
15	R/WSC	**PHY Reset** 1: Reset, Bit Self Cleaning After Reset Completed 0: Normal
14	R/W	**Loopback** 1: Loopback Mode Enabled 0: Normal
13	R/W	**Speed** 1: 100 Mbps Selected (100Base TX) 0: 10 Mbps selected (10Base-T)
12	R/W	**Auto-Negotiation** 1: Auto-Negotiation Enabled 0: Normal
11	R/W	**Powerdown** 1: Powerdown 0: Normal
10	R/W	**MII interface** 1: MII Interface Disabled 0: Normal
9	R/WSC	**Auto-Negotiation Reset** 1: Reset Auto-Negotiation Process, Bit Self Clearing After Reset Completed 0: Normal
8	R/W	**Duplex Mode** 1: Full Duplex 0: Half Duplex
7	R/W	**Collision Test** 1: Collision Test Enabled 0: Normal

6-0	R/W	**Reserved**

Register 01h STATUS

Default Value: 7809h

Access: Read Only

Bit	Access	Description
15	RO	0: Not Capable of 100Base-T4 Operation
14	RO	1: Capable of 100Base-TX Full Duplex
13	RO	1: Capable of 100Base-TX Half Duplex
12	RO	1: Capable of 10Base-T Full Duplex
11	RO	1: Capable of 10Base-T Half Duplex
10-7	RO	Reserved
6	R	0: Not Capable of Accepting MI Frames with MI Preamble Suppressed
5	R	1: Auto-Negotiation Acknowledge Process Complete 0: Normal
4	R/LH	1: Remote Fault Detected. This bit is set when Either Interrupt Detect or Auto-Negotiation Remote Fault is set. 0: No Remote Fault
3	R	1: Capable of Auto-Negotiation Operation
2	R/LL	1: Link Detected 0: Link not detected
1	R/LH	1: Jabber Detected 0: Normal
0	R	1: Extended Register Exist

Register 02h PHY ID #1

Default Value: 001Dh

Access: Read

Bit	Access	Description
15-0	R	**Company ID, Bits 3-18** OUI = 00-E0-06

Register 03h PHY ID #2

Default Value: 8000h

Access: Read

Bit	Access	Description
15-10	R	**Company ID, Bits 19-24** OUI = 00-E0-06
9-4	R	**Manufacturer's Part Number** 00_H
3-0	R	**Manufacturer's Revision Number** 00_H

Register 04h Auto-Negotiation Advertisement

Default Value: 05E1h

Access: Read/Write

Bit	Access	Description
15	R/W	1: Next Page Exists 0: No Next Page
14	R	1: Received Auto-Negotiation Word Recognized 0: Not Recognized
13	R/W	1: Auto-Negotiation Remote Fault Detected 0: No Remote Fault
12-11	R/W	Reserved
10	R/W	1: Capable of Pause Operation for Full Duplex Link 0: Not Capable
9	R/W	1: Capable of 100Base-T4 0: Not Capable
8	R/W	1: Capable of 100Base-TX Full Duplex 0: Not Capable
7	R/W	1: Capable of 100Base-TX Half Duplex 0: Not Capable
6	R/W	1: Capable of 10Base-T Full Duplex 0: Not Capable
5	R/W	1: Capable of 10Base-T Half Duplex 0: Not Capable
4-1	R/W	Reserved

0	R/W	1: Capable of 802.3 CSMA Operation 0: Not Capable

NOTE 1: NEXT PAGE CURRENTLY NOT SUPPORTED.

Register 05h Auto-Negotiation Remote End Capability

Default Value: 0000h

Access: Read

Bit	Access	Description
15	R	1: Next Page Exists 0: No Next Page
14	R	1: Received Auto-Negotiation Word Recognized 0: Not Recognized
13	R	1: Auto-Negotiation Remote Fault Detected 0: No Remote Fault
12-11	R	Reserved
10	R	1: Capable of Pause Operation for Full Duplex Link 0: Not Capable
9	R	1: Capable of 100Base-T4 0: Not Capable
8	R	1: Capable of 100Base-TX Full Duplex 0: Not Capable
7	R	1: Capable of 100Base-TX Half Duplex 0: Not Capable
6	R	1: Capable of 10Base-T Full Duplex 0: Not Capable
5	R	1: Capable of 10Base-T Half Duplex 0: Not Capable
4-1	R	Reserved
0	R	1: Capable of 802.3 CSMA Operation 0: Not Capable

Register 10h Configuration 1

Default Value: 0022h

Access: Read/Write

Bit	Access	Description
15	R/W	**Link Disable** 1: Received Link Detect Function Disabled (Force Link Pass) 0: Normal
14	R/W	**Transmit Disable** 1: TP Transmitter Disabled 0: Normal
13	R/W	**Transmit Powerdown** 1: TP Transmitter Powered Down 0: Normal
12	R/W	**TX_EN to CRS Loopback** 1: TX_EN to CRS Loopback Disabled 0: Enabled
11-10	R/W	**Reserved**
9	R/W	**Unscrambled Idle Reception Disable** 1: Disable Auto-Negotiation with devices that transmit unscrambled, idle on power up and various instances 0: Enables Auto-Negotiation with devices that transmit unscrambled, idle on power up and various instances
8	R/W	**Receive Equalizer Select** 1: Received Equalizer Disabled, Set to 0 Length 0: Receive Equalizer On (For 100Base-TX Mode Only)
7	R/W	**Cable Type Select** 1: STP (150 Ohm) 0: UTP (100 Ohm)
6	R/W	**Receive Input Level Adjust** 1: Receive Squelch Levels Reduced By 4.5 dB 0: Normal
5-2	R/W	**Reserved**
1-0	R/W	**Transmitter Rise/Fall Time Adjust** 11 -0.25 ns 10 +0.0 ns 01 +0.25 ns 00 +0.5 ns

Register 11h Configuration 2

Default Value: FF00h

Access: Read/Write

Bit	Access	Description
15-6	R	**Reserved**
5	R/W	**Auto Polarity Disable** 1: Auto Polarity Correction Function Disabled 0: Normal
4	R/W	**Jabber Disable Select** 1: Jabber Disabled 0: Enabled
3-0	R/W	**Reserved**

Register 12h Status Output REGISTER

Default Value: 0080h

Access: Read Only

Bit	Access	Description
15	RO	**Interrupt Detec**t 1: Interrupt Bit(s) Have Changed Since Last Read Operation. 0: No Change
14	R/LT	**Link Fail Detect** 1: Link Not Detected 0: Normal
13	R/LT	**Descrambler Loss of Synchronization Detect** 1: Descrambler Has Lost Synchronization 0: Normal
12	R/LT	**Codeword Error** 1: Invalid 4B/5B Code Detected On Receive Data 0: Normal
11	R/LT	**Start Of Stream Error** 1: No Start Of Stream Delimiter Detected on Received Data 0: Normal

10	R/LT	**End Of Stream Error** 1: No End Of Stream Delimiter Detected On Receive Data 0: Normal
9	R/LT	**Reverse Polarity Detect** 1: Reserve Polarity Detected 0: Normal
8	R/LT	**Jabber Detect** 1: Jabber Detected 0: Normal
7	R/LT	**100/10 Speed Detect** 1: Device in 100 Mbps Mode (100Base-TX) 0: Device in 10 Mbps Mode (10Base-T)
6	R/LT	**Duplex Detect** 1: Device In Full Duplex 0: Device In Half Duplex
5-4	RO	**Auto-Negotiation Status** 11 Auto-Negotiation Detected & Started 10 Auto-Negotiation Detected & Stuck 01 Auto-Negotiation Detected & Done 00 Auto-Negotiation Not Detected
3-0	RO	**Reserved**

Register 13h Mask

Default Value: FFC0h

Access: Read/Write

Bit	Access	Description
15	R/W	1: Mask Interrupt For INT in Register 18 0: No Mask
14	R/W	1: Mask Interrupt For LNK_FAIL in Register 18 0: No Mask
13	R/W	1: Mask Interrupt For LOSS_SYNC in Register 18 0: No Mask
12	R/W	1: Mask Interrupt For CWRD in Register 18 0: No Mask

11	R/W	1: Mask Interrupt For SSD in Register 18 0: No Mask
10	R/W	1: Mask Interrupt For ESD in Register 18 0: No Mask
9	R/W	1: Mask Interrupt For RPOL in Register 18 0: No Mask
8	R/W	1: Mask Interrupt For JAB in Register 18 0: No Mask
7	R/W	1: Mask Interrupt For SPD_DET in Register 18 0: No Mask
6	R/W	1: Mask Interrupt For DPLX_DET in Register 18 0: No Mask
5-3	R/W	Reserved
2-0	R/W	**Link Fail Timer Select** 111 Reserved 110 Bit 18.14 Set to 1 if Link Fail for >32 Sec 101 Bit 18.14 Set to 1 if Link Fail for >16 Sec 100 Bit 18.14 Set to 1 if Link Fail for >8 Sec 011 Bit 18.14 Set to 1 if Link Fail for >4 Sec 010 Bit 18.14 Set to 1 if Link Fail for >2 Sec 001 Bit 18.14 Set to 1 if Link Fail for >1 Sec 000 Bit 18.14 Set to 1 if Link Fail for >0 Sec

Register 14h RESERVED

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15-0	R/W	Reserved for Factory Use. Must to 0 for Normal Operation

13.5 Home SPI Registers

(These registers can be accessed from MAC serial EEPROM interface)

Address	Access	Register Name
01h-00h	R/W	CONTROL Register
03h-02h	R/W	STATUS Register
05h-04h	R/W	IMASK Register

07h-06h	R/W	ISTAT Register
0Bh-08h	R/W	TX_PCOM Register
0Fh-0Ch	R/W	RX_PCOM Register
10h	R/W	NOISE Register
11h	R/W	PEAK Register
12h	R/W	NSE_FLOOR Register
13h	R/W	NSE_CEILING Register
14h	R/W	NSE_ATTACK Register
15h	R/W	NSE_EVENTS Register
19h	R/W	AID_ADDRESS Register
1Ah	R/W	AID_INTERVAL Register
1Bh	R/W	AID_ISBI Register
1Ch	R/W	ISBI_SLOW Register
1Dh	R/W	ISBI_FAST Register
1Eh	R/W	TX_PULSE_WIDTH Register
1Fh	R/W	TX_PULSE_CYCLES Register

Register 00h CONTROL

Default Value: 05

Access: Read / Write

Bit	Access	Description
7	R/W	**Disable AID Address Negotiation** 0 : normal 1 : disable
6	R/W	**Clear the NSE_EVENTS Register** 0 : normal 1 : clear
5	R/W	**Disable SLICE Adaptation** 0 : normal 1 : disable

4	R/W	**Power down** 0 : normal 1 : power down
3	R/W	**Reserved**
2	R/W	**High Speed** 0 : low speed 1 : high speed
1	R/W	**High Power** 0 : low power 1 : high power
0	R/W	**Reserved**

Register 01h CONTROL

Default Value: 00

Access: Read / Write

Bit	Access	Description
7	R/W	**Set Remote Command** 0 : disable 1 : enable
6-4	R/W	**Reserved**
3	R/W	**Command Low Power** 0 : normal 1 : set low power command
2	R/W	**Command High Power** 0 : normal 1 : set high power command
1	R/W	**Command Low Speed** 0 : normal 1 : set low speed command
0	R/W	**Command High Speed** 0 : normal 1 : set high speed command

Register 02h STATUS

Default Value: 00

Access: Read / Write

Bit	Access	Description
7	R/W	**Reserved**
6	R/W	**RX_POWER** 0 : receive low power 1 : receive high power
5	R/W	**RX_SPEED** 0 : receive low speed 1 : receive high speed
4	R/W	**RX_VERSION** 0 : version 0 1 : not version 0
3-0	R/W	**Reserved**

Register 03h STATUS

Default Value: 00

Access: Read / Write

Bit	Access	Description
7-0	R/W	**Reserved**

Register 04h IMASK

Default Value: 00

Access: Read / Write

Bit	Access	Description
7-4	R/W	**Reserved**
3	R/W	**Receive Packet** 0 : mask 1 : no mask
2	R/W	**Transmit Packet** 0 : mask 1 : no mask

1	R/W	**Receive Remote Command** 0 : mask 1 : no mask
0	R/W	**Sent Remote Command** 0 : mask 1 : no mask

Register 05h IMASK

Default Value: 00

Access: Read / Write

Bit	Access	Description
7-2	R/W	**Reserved**
1	R/W	**RxPCOM** 0 : mask 1 : no mask
0	R/W	**TxPCOM** 0 : mask 1 : no mask

Register 06h ISTAT

Default Value: 00

Access: Read / Write

Bit	Access	Description
4-7	R/W	**Reserved**
3	R/W	**Packet Rcv'd** 0 : no receive packet 1 : receive packet done
2	R/W	**Packet Xmt'd** 0 : no transmit packet 1 : transmit packet done
1	R/W	**Receive Remote Command Valid** 0 : no complete 1 : complete

0	R/W	**Sent Remote Command Done** 0 : no complete 1 : complete

Register 05h ISTAT

Default Value: 00

Access: Read / Write

Bit	Access	Description
7-2	R/W	**Reserved**
1	R/W	**RxPCOM Valid** 0 : all 0 data 1 : non-null data
0	R/W	**TxPCOM Ready** 0 : all 0 data 1: non-null data

Register 0Bh~08hTX_PCOM

Default Value: 00000000

Access: Read / Write

Bit	Access	Description
31:0	R/W	The 32-bit transmitted data field to be used for out-of-band communication between HOMEPHY management entities.

Register 0Fh~0ChRX_PCOM

Default Value: 00000000

Access: Read / Write

Bit	Access	Description
31:0	R/W	The 32-bit received data field to be used for out-of-band communication between HOMEPHY management entities.

Register 10h NOISE

Default Value: 04

Access: Read / Write

Bit	Access	Description

7:0	R/W	This is the digital value of the SLICE_LVL_NOISE output. When the bit 5 of the 00h register is false, this register is updated with current NOISE LEVEL every 50ns. When the bit 5 of the 00h register is true, this register is used to genertae both the SLICE_LVL_NOISE and SLICE_LVL_DATA.

Register 11h PEAK

Default Value: FF

Access: Read / Write

Bit	Access	Description
7:0	R/W	This is a measurement of the peak level of the AID received (non-collision).

Register 12h NSE_FLOOR

Default Value: 04

Access: Read / Write

Bit	Access	Description
7:0	R/W	The minimum value of the NOISE measurement.

Register 13h NSE_CEILING

Default Value: FF

Access: Read / Write

Bit	Access	Description
7:0	R/W	The value that is reload into PEAK register if NOISE level exceeds PEAK level.

Register 14h NSE_ATTACK

Default Value: F4

Access: Read / Write

Bit	Access	Description
7:4	R/W	This value define the number of noise events need to raise the SLICE LEVEL immediately.
3:0	R/W	This value define the number of noise events need to raise the SLICE LEVEL at the end of an 870ms period.

Register 15h NSE_EVENTS

Default Value: 00

Access: Read / Write

Bit	Access	Description
7:0	R/W	The value record the number of noise event detected.

Register 19h AID_ADDRESS

Default Value: 00

Access: Read / Write

Bit	Access	Description
7:0	R/W	**The AID address is used for collision detection.** Unless bit 7 of the 00h register is set, the HOMEPHY is assured to select unique AID address.

Register 1Ah AID_INTERVAL

Default Value: 14

Access: Read / Write

Bit	Access	Description
7:0	R/W	The value defines the number of TCLK separating AID symbols.

Register 1Bh AID_ISBI

Default Value: 40

Access: Read / Write

Bit	Access	Description
7:0	R/W	The value defines the number of TCLK between AID pulse for symbol 0.

Register 1Ch ISBI_SLOW

Default Value: 2C

Access: Read / Write

Bit	Access	Description
7:0	R/W	The value defines the number of TCLK between DATA pulse for symbol 0 in low speed.

Register 1Dh ISBI_FAST

Default Value: 1C

Access: Read / Write

Bit	Access	Description
7:0	R/W	The value defines the number of TCLK between DATA pulse for symbol 0 in high speed.

Register 1Eh TX_PULSE_WIDTH

Default Value: 04

Access: Read / Write

Bit	Access	Description
7:0	R/W	The value determines the number of OSC cycles a transmit pulse lasts.

Register 1Fh TX_PULSE_CYCLES

Default Value: 04

Access: Read / Write

Bit	Access	Description
7:4	R/W	The value determines the number of pulse on TXP.
3:0	R/W	The value determines the number of pulse on TXN.

14 Register Summary / Description – AC' 97 / S/W Modem Summary

14.1 Audio Configuration Space (Function 4)

Configuration. Offset	Access	Mnemonic Register
00-01h	R/W	Vendor ID
02-03h	R/W	Device ID
04-05h	R/W	Command
06-07h	R/W	Status
08h	RO	Revision ID
09-0Bh	RO	Class Code
0Ch	R/W	Cache Line Size
0Dh	R/W	Latency Timer
0Eh	R/W	Header Type
0Fh	R/W	BIST
10-13h	R/W	Audio IO Base Address
14-17h	R/W	Audio Memory Base Address
18-2Bh	RO	RSVD
2C-2Dh	R/W	Subsystem Vendor ID
2E-2Fh	R/W	Subsystem ID
30-33h	R/W	RSVD
34h	RO	Power Management Capability List Pointer
35-37h	RO	RSVD
38-3Bh	RO	RSVD
3Ch	R/W	Interrupt Line
3Dh	R/W	Interrupt Pin
3Eh	R/W	MIN_GNT
3Fh	R/W	MAX_LAT
40-43h	R/W	DDMA Slave Configuration
44h	R/W	Legacy I/O base decoding
45h	R/W	Legacy DMA decoding
46h	R/W	Power Management Configuration

47h	R/W	Inactivity Timer Expiration Control
48-49h	R/W	INT Acknowledge Snoop
4A-4Bh	RO	RSVD
4C-DBh	RO	RSVD
DC-DFh	R/W	Power Management Capability Register
E0-E3h	R/W	Power Management Control/Status Register

14.1.1 Audio Operational Registers

Operation. Offset	Access	Mnemonic Register
00h	R/W	Legacy DMA Playback Buffer Base Register Port 1
01h	R/W	Legacy DMA Playback Buffer Base Register Port 2
02h	R/W	Legacy DMA Playback Buffer Base Register Port 3
03h	R/W	Legacy DMA Playback Buffer Base Register Port4
04h	R/W	Legacy DMA Playback Byte Count Register 1
05h	R/W	Legacy DMA Playback Byte Count Register 2
06h	R/W	Legacy DMA Playback Byte Count Register 3
07h	R/W	Legacy DMA Playback Misc. Register
08h	RO	Legacy DMA Controller Command / Status Register
0Ah	WO	Legacy DMA Single Channel Mask Port
0Bh	R/W	Legacy DMA Channel Operation Mode Register
0Ch	WO	Legacy DMA Controller First_Last Flag Clear Port
0Dh	WO	Legacy DMA Controller Master Clear Port
0Eh	WO	Legacy DMA Controller Clear Mask Port
0Fh	WO	Legacy DMA Controller Multi-Channel Mask Register
10h	R/W	Legacy FMMusic Bank 0 Register Index / Legacy FMMusic Status
11h	R/W	Legacy FMMusic Bank 0 Register Data Port

12h	R/W	Legacy FMMusic Bank 1 Register Index
13h	R/W	Legacy FMMusic Bank 1 Register Data Port
14h	R/W	Legacy Sound Blaster Mixer Register Index
15h	R/W	Legacy Sound Blaster Mixer Register Data Port
16h	WO	Legacy Sound Blaster ESP Reset Port
1A or 1Bh	RO	Legacy Sound Blaster ESP Data Port
1C or 1Dh	R/W	Legacy Sound Blaster Command / Status Port
1Eh	RO	Legacy Sound Blaster ESP Data Ready / IRQ Acknowledge Port 1
1Fh	RO	Legacy Sound Blaster ESP Data Ready / IRQ Acknowledge Port 2
40-43h	R/W	AC' 97 Mixer Write Register
44-47h	R/W	AC' 97 Mixer Read Register
48-4Bh	R/W	Serial Interface Control Register
4C-4Fh	R/W	AC' 97 General Purpose IO Register
50-53h	RO	SiS Audio Status Register
54-55h	RO	Legacy Sound Blaster Frequency Read Back Register
56h	RO	Legacy Sound Blaster Time Constant Read Back Register
58-5Bh	R/W	SiS Audio Scratch Register
5Ch	RO	SiS Audio Version Control Register
5Eh	R/W	SB ESP Version High Byte Control Register
5Fh	R/W	SB ESP Version Low Byte Control Register
60-63h	RO	OPL3 Emulation Channel Key on/off Trace Register
70-73h	R/W	S/PDIF Channel Status Register
7C-7Fh	R/W	General Purpose IO Register
80-83h	R/W	START Command and Status Register for Bank A
84-87h	R/W	Channel STOP Command and Status Register for Bank A
88-8Bh	R/W	Delay Flag of Bank A

8C-8Fh	R/W	Sign Bit of CSO
90-93h	RO	Bank A Current Sample Position Flag
94-97h	R/W	Current Envelope Buffer Control
98-9Bh	R/W	Bank A Address Engine Interrupt
9C-9Fh	R/W	Envelope Engine Interrupt Register
A0-A3h	R/W	Global Control & Channel Index
A4-A7h	R/W	Bank A Address Engine Interrupt Enable
A8-ABh	R/W	Global Music Volume & Global Wave Volume
AC-AFh	R/W	Sample Change Step for Legacy Playback & Recording
B0-B3h	R/W	Miscellaneous Int & Status
B4-B7h	R/W	START Command and Status Register for Bank B
B8-BBh	R/W	Channel STOP Command and Status Register for Bank B
BC-BFh	RO	Bank B Current Sample Position Flag
C0-C3h	R/W	Sound Blaster Base Block Length & Current Block Length
C4-C7h	R/W	Sound Blaster Control
C8-CBh	RO	Playback Sample Timer
CC-CFh	R/W	Bank B Low Frequency Oscillator Control
D0-D3h	R/W	Sample Timer Target
D8-DBh	R/W	Bank B Address Engine Interrupt
DC-DFh	R/W	Bank B Address Engine Interrupt Enable
E0-E3h	R/W	CSO & ALPHA & FMS
E4-E7h	R/W	LBA
E8-EBh	R/W	ESO & DELTA
EC-Efh	R/W	For Bank A: LFO_CTRL & LFO_CT & FMC & RVOL & CVOL For Bank B: Bank B ATTRIBUTE & FMC & RVOL & CVOL
F0-F3h	R/W	For Bank A: Bank A GVSEL & PAN & VOL & CTRL & Ec For Bank B: Bank B GVSEL & PAN & VOL &

		CTRL & Bank A LFO_INIT
F4h		EBUF1
F8h		EBUF2

14.2 Audio Processor Register Map:

Table 14.2-1 Audio Processor Register Map

IO Offset	+3h	+2h	+1h	+0h
00h	DMAR3	DMAR2	DMAR1	DMAR0
04h	DMAR7	DMAR6	DMAR5	DMAR4
08h	DMAR11	DMAR10	DMAR9	DMAR8
0Ch	DMAR15	DMAR14	DMAR13	DMAR12
10h	SBR3/SBR1	SBR2	SBR1/SBR3	SBR0
14h	RSVD	SBR6	SBR5	SBR4
18h	RSVD	SBR7	RSVD	RSVD
1Ch	SBR10	SBR9	RSVD	SBR8
20-3Ch	RSVD			
40h	ACWR			
44h	ACRD			
48h	SCTRL			
4Ch	ACGPIO			
50h	ASR0			
54h	RSVD	ASR2	RSVD	ASR1
58h	ASR3			
5Ch	ASR6	ASR5	RSVD	ASR4
60h	AOPLSR0			
70h	SPDIF_CS			
74h	RSVD			
78h	RSVD			
7Ch	RSVD	RSVD	GPO	GPI
80h	START_A			
84h	STOP_A			
88h	DLY			
8Ch	SIGN_CSO			
90h	CSPF_A			
94h	CEBC			

98h	AIN_A			
9Ch	EINT			
A0h	GC			CIR
A4h	AINTEN_A			
A8h	MUSICVOL		WAVEVOL	
ACh	SBDELTA/SBDELTA_R		RSVD	
B0h	MISCINT			
B4h	START_B			
B8h	STOP_B			
BCh	CSPF_B			
C0h	SBDMAL		SBDMAC	
C4h	SBE2R	RSVD	SBDD	SBCTRL
C8h	STIMER			
CCh	LFO_CTRL_B	LFO_CT_B	I^2S_DELTA	
D0h	ST_TARGET			
D4h	RSVD			
D8h	AINT_B			
DCh	AINTEN_B			
Bank A: Channel Register				
ARAM_A (CIR<32)				
E0h	CSO		FMS+ALPHA(11:8)	ALPHA(7:0)
E4h	CPTR + LBA			
E8h	ESO		DELTA	
ECh	LFO_CTRL	LFO_CT	FMC+RVOL[6:1]	RVOL[0]+CVOL
ERAM_A (CIR<32)				
F0h	GVSEL + PAN	VOL	CTRL + Ec(11:8)	Ec(7:0)
F4h	EBUF1			
F8h	EBUF2			
FCh	RSVD			
Bank B: Channel Register				
ARAM_B (CIR>=32)				
E0h	CSO		FMS+ALPHA(11:8)	ALPHA(7:0)
E4h	CPTR + LBA			
E8h	ESO		DELTA	
ECh	ATTRIBUTE		FMC+RVOL[6:1]	RVOL[0]+CVOL

ERAM_B (CIR>=32)				
F0h	GVSEL + PAN	LFO_INIT(Bank A)	CTRL + VOL(11:8)	VOL(7:0)
F4h	RSVD			
F8h	RSVD			
FCh	RSVD			

Register 00h DMAR0 (Legacy DMA Playback Buffer Base Register Port 1)

Legacy Address: DDMASlaveBase + 0h || 0000h / 0002h

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**Legacy DMA Playback Buffer Current Transfer Address 7-0** The PCI bus interface circuit should response to I/O read to 0000h or 0002h on the PCI bus only when DMASnoopEn is active. Write: Legacy DMA Playback Buffer Base Address 7-0 Read: Legacy DMA Playback Buffer Current Transfer Address 7-0

Register 01h DMAR1 (Legacy DMA Playback Buffer Base Register Port 2)

Legacy Address: DDMASlaveBase + 1h || 0000h / 0002h

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**Legacy DMA Playback Buffer Current Transfer Address 15-8** The PCI bus interface circuit should response to I/O read to 0000h or 0002h on the PCI bus only when DMASnoopEn is active. Write: Legacy DMA Playback Buffer Base Address 15-8 Read: Legacy DMA Playback Buffer Current Transfer Address 15-8

Register 02h DMAR2 (Legacy DMA Playback Buffer Base Register Port 3)

Legacy Address: DDMASlaveBase + 2h || 0087h / 0083h

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**Legacy DMA Playback Buffer Current Transfer Address 23-16** The PCI bus interface circuit should response to I/O read to 0087h or 0083h on the PCI bus only when DMASnoopEn is active. Write: Legacy DMA Playback Buffer Base Address 23-16 Read: Legacy DMA Playback Buffer Current Transfer Address 23-16

Register 03h DMAR3 (Legacy DMA Playback Buffer Base Register Port4)

Legacy Address: DDMASlaveBase + 3h

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**Legacy DMA Playback Buffer Current Transfer Address 31-24** Write: Legacy DMA Playback Buffer Base Address 31-24 Read: Legacy DMA Playback Buffer Current Transfer Address 31-24

This register is intended for system which has DDMA Master.

Any time when legacy DMA playback is not running, this register must be reset to 0 by software driver.

Register 04h DMAR4 (Legacy DMA Playback Byte Count Register 1)

Legacy Address: DDMASlaveBase + 4h || 0001h / 0003h

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**Legacy DMA Playback Current Byte Count 7-0** The PCI bus interface circuit should response to I/O read to 0003h or 0001h on the PCI bus only when DMASnoopEn is active. Write: Legacy DMA Playback Byte Base Count 7-0 Read: Legacy DMA Playback Current Byte Count 7-0

Register 05h DMAR5 (Legacy DMA Playback Byte Count Register 2)

Legacy Address: DDMASlaveBase + 5h || 0001h / 0003h

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**Legacy DMA Playback Current Byte Count 15-8** The PCI bus interface circuit should response to I/O read to 0003h or 0001h on the PCI bus only when DMASnoopEn is active. Write: Legacy DMA Playback Byte Base Count 15-8 Read: Legacy DMA Playback Current Byte Count 15-8

Register 06h DMAR6 (Legacy DMA Playback Byte Count Register 3)

Legacy Address: DDMASlaveBase + 6h

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**Legacy DMA Playback Current Byte Count 23-16** Write: Legacy DMA Playback Byte Base Count 23-16 Read: Legacy DMA Playback Current Byte Count 23-16

This register is intended for system which has DDMA Master.

Any time when legacy DMA playback is not running, this register must be reset to 0 by software driver.

Register 07h DMAR7(Legacy DMA Playback Misc. Register)

Legacy Address: DDMASlaveBase + 7h

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	This Register is for internal debugging use.

Register 08h DMAR8(Legacy DMA Controller Command / Status Register)

Legacy Address: DDMASlaveBase + 8h || 0008h

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	**Status register for implemented legacy 8237-A DMA channel.** Implementation of this register maintains the compatibility with legacy 8237-A status register. However, when reading this register, the return value should be different for I/O read to (DDMASlaveBase + 8h) , I/O read to (AudioBase +8h)and I/O read to (0008h). I/O read to (DDMASlaveBase + 08h) is normally initiated by DDMA Master. I/O read to (AudioBase + 08h) is normally initiated by our debug program. The DDMA Master will take the responsibility to combine the return value of each DMA Slave Channel in the system and return the final resultant byte to response to the PCI I/O read to 0008h initiated by Host. The PCI bus interface circuit should response to I/O read to 0008h on the PCI bus only when DMASnoopEn is active.

Register 0Ah DMAR10(Legacy DMA Single Channel Mask Port)

Legacy Address: 000Ah

Default Value: 00h

Access: Write Only

Bit	Access	Description
0	WO	**Channel mask register for implemented legacy 8237-A DMA channel.** Writing to this register will affect the legacy DMA operation of SiS Audio, implementation of this register maintains the register compatibility with legacy 8237-A DMA signal channel mask register. For system which has DDMA Master, it is the DMA Master' s responsibility to update the legacy channel mask bit DMAR15.0 with address (DMASlaveBase + Fh) when a I/O write to 000Ah occurred on PCI Bus. When snooping legacy 8237-A register operation is enabled, any I/O write to 000Ah should be snooped to DMAR15.0 if the channel number matches the snooping legacy DMA channel number.

Register 0Bh DMAR11(Legacy DMA Channel Operation Mode Register)

Legacy Address: DDMASlaveBase + 0Bh || 000Bh

Default Value: 00h

Access: Read / Write

Bit	Access	Description
7:0	R/W	This register can only be read out through AudioBase + 0Bh port channel mode register for implemented legacy 8237-A DMA channel. Writing to this register will affect the legacy DMA operation of SiS Audio , implementation of this register maintains

		the register compatibility with legacy 8237-A DMA channel mode register for system with or without DDMA Master . For system which has DDMA Master, it is the DMA Master's responsibility to update this register when a I/O write to 000Bh occurred on PCI Bus. When snooping legacy 8237-A register operation is enabled, any I/O write to 000Bh should be snooped to this register if the channel number matches the snooping legacy DMA channel number.

Register 0Ch DMAR12(Legacy DMA Controller First_Last Flag Clear Port)

Legacy Address: 000Ch

Default Value:

Access: Write Only

Bit	Access	Description
0	WO	**First_Last flag clear register for implemented legacy 8237-A DMA channel .** Writing to this register will clear the flag signal First_Last. Implementation of this register maintains the register compatibility with legacy 8237-A DMA controller for system without DDMA Master. For system which has DDMA Master, it is the DMA Master's responsibility to implement this flag. When snooping legacy 8237-A register operation is enabled, any I/O write to 000Ch should clear First_Last flag

Register 0Dh DMAR13(Legacy DMA Controller Master Clear Port)

Legacy Address: DDMASlaveBase + 0Dh || 000Dh

Default Value:

Access: Write Only

Bit	Access	Description
0	WO	**Master clear register for implemented legacy 8237-A DMA channel .** Writing to this register has the effect of hardware reset to the implemented legacy 8237-A DMA channel. Implementation of this register maintains the register compatibility with legacy 8237-A DMA controller for system with or without DDMA Master. For system which has DDMA Master, it is the DMA Master's responsibility to write to this register when a write to legacy 8237-A master clear register (I/O write to 000Dh) is on the PCI Bus. When snooping legacy 8237-A register operation is enabled, any I/O write to 000Dh should clear several legacy flags such as First_Last flag.

Register 0Eh DMAR14(Legacy DMA Controller Clear Mask Port)

Legacy Address: 000Eh

Default Value:

Access: Write Only

Bit	Access	Description
0	WO	**Multi-channel mask clear port for implemented legacy 8237-A DMA channel .** Writing to this register will affect the legacy DMA operation of SiS Audio , implementation of this register maintains the register compatibility with legacy 8237-A DMA multi-channel clear mask register . For system which has DDMA Master, it is the DMA Master' s responsibility to update the legacy channel mask bit DMAR15.0 with address (DMASlaveBase + Fh) when a I/O write to 000Eh occurred on PCI Bus. When snooping legacy 8237-A register operation is enabled, any I/O write to 000Eh will reset DMAR15.0 to 0.

Register 0Fh DMAR15(Legacy DMA Controller Multi-Channel Mask Register)

Legacy Address: DDMASlaveBase + 0Fh || 000Fh

Default Value: 0b

Access: Write Only

Bit	Access	Description
1	WO	**Multi-channel mask register for implemented legacy 8237-A DMA channel .** Implementation of this register maintains the register compatibility with legacy 8237-A DMA controller for system with or without DDMA Master. For system which has DDMA Master, it is the DMA Master' s responsibility to write DMAR15 when a write to legacy 8237-A multi-channel mask register (I/O write to 000Fh) is on the PCI Bus. When snooping legacy 8237-A register operation is enabled, any I/O write to 000Fh should update the mask flag for the implemented legacy 8237-A DMA channel.

Register 10h SBR0 (Legacy FMMusic Bank 0 Register Index / Legacy FMMusic Status)

Legacy Address: SBBase + 0h || SBBase + 8h || ADLIBBase + 0h

Default Value: 00h

Access: Read/Write

Bit	Access	Description

7:0	RW	1:FMMusic Timer Interrupt Flag (Equal to Bit 6 + Bit 5) 1:FMMusic Timer 1 Overflowed Flag 1:FMMusic Timer 2 Overflowed Flag 0:Reserved Legacy FMMusic Bank 0 Register Index

Relative Internal Function Register File

In order to emulate the legacy FMMusic(YMF262 or OPL3) function, a 512 bytes register file (RAM) must be implemented. By legacy access method, this register file has two banks and the bank index is specified by SBR0 and SBR2 respectively. This register file is byte-wide format, read/write RAM which has no high speed operation requirement.

Relative Internal Functional Register Extracted From Legacy FMMusic Bank 0 Register File
FMMusic-TIMER1

Bank Index : 02h

Size : 8 bits

Type : read/write

Default : 00h

Bit 7..0 X Timer1 Preset Value

If enabled Timer1 counter, it will increase every 1024 AC97 bitclock (12.288MHz) . When overflow occurs, this value is re-loaded into the counter.

FMMusic-TIMER2

Bank Index : 03h

Size : 8 bits

Type : read/write

Default : 00h

Bit 7..0 X Timer2 Preset Value

If enabled Timer2 counter, it will increase every 4096 AC' 97 bitclock (12.288MHz). When overflow occurs, this value is re-loaded into the counter.

FMMusic-Timer-CONTROL

Bank Index : 04h

Size : 8 bits

Type : read/write

Default : 00h

Bit 7 1 Reset Bit 7-5 of Legacy FMMusic Status Register

Bit 6 1 Reset Timer1 Overflow Flag

Bit 5 1 Reset Timer2 Overflow Flag

Bit 4-2	0	Reserved
Bit 1	1	Enable Timer 2
Bit 0	1	Enable Timer 1

Bit 7-5 must be self-cleared to 0 after it is written as 1.

When bit 1 or 0 is set from 0 to 1, the corresponding timer counter will load its preset value and start counting. When these bits are zero, the respective timer counter will stop counting. If bit 1 is set 1, bit 7 and 5 of FMMusic Status register will be set 1 when timer2 is overflowed. If bit 0 is set 1, bit 7 and 6 of FMMusic Status register will be set 1 when timer1 is overflowed.

Register 11h / 13h SBR1 (Legacy FMMusic Bank 0 Register Data Port)

Legacy Address: SBBase + 1h || SBBase + 9h || ADLIBBase + 1h || SBBase + 3h || ADLIBBase + 3h

Default Value: XXh

Access: read/write

Bit	Access	Description
7:0	R/W	Legacy FMMusic Bank 0 Register(indexed by SBR0) Data

When writing to this register, if SBR0 is B0h-B8h and bit 5 of the content (indexed by SBR0) is changed from 0 to 1 or vice versa, or SBR0 is BDh and any one of bit 4-0 of the content (indexed by SBR0) is changed from 0 to 1 or vice versa, an OPL3 Bank0 Key On/Off Dirty Flag will be set at TSAudio Status Register ASR0 and AOPLSR0.

Register 12h SBR2 (Legacy FMMusic Bank 1 Register Index)

Legacy Address: SBBase + 2h || ADLIBBase + 2h

Default Value: 00h

Access: read/write

Bit	Access	Description
7:0	R/W	Legacy FMMusic Bank 1 Register Index

Register 11h / 13h SBR3 (Legacy FMMusic Bank 1 Register Data Port)

Legacy Address: SBBase + 1h || ADLIBBase + 1h || SBBase + 3h || ADLIBBase + **3h**

Default Value: XXh

Access: read/write

Bit	Access	Description
7:0	R/W	Legacy FMMusic Bank 1 Register(indexed by SBR2) Data

When write to this register, if SBR2 is B0h-B8h and bit 5 of the content (indexed by SBR2) is changed from 0 to 1 or vice versa, an OPL3 Bank1 Key On/Off Dirty Flag will be set at TSAudio Status Register ASR0 and AOPLSR0.

Register 14h SBR4 (Legacy Sound Blaster Mixer Register Index)

Legacy Address: SBBase + 4h

Default Value: 00h

Access: read/write

Bit	Access	Description
7:0	R/W	Legacy SB16 / SBPRO Mixer Register Index

Register 15h SBR5 (Legacy Sound Blaster Mixer Register Data Port)

Legacy Address: SBBase + 5h

Default Value: XXh

Access: read/write

Bit	Access	Description
7:0	R/W	Legacy SB16 / SBPRO Mixer Register (indexed by SBR4) Data Port

Register 16h / 17h SBR6 (Legacy Sound Blaster ESP Reset Port)

Legacy Address: SBBase + 6h || SBBase + 7h

Default Value:

Access: write only

Bit	Access	Description
0	WO	1:Enter Legacy SB16 / SBPRO ESP Reset State 0:Escape From SB16 / SBPRO ESP Reset State

ESP Reset should do the following things:

a. Reset ESP to no operation status and clear ESP Busy Flag.

b. Stop wave engine SB channel operation.

Reset any flags that may affect the next command execution.

Register 1Ah / 1Bh SBR7 (Legacy Sound Blaster ESP Data Port)

Legacy Address: SBBase + Ah || SBBase + Bh

Default Value: 00h

Access: Read only

Bit	Access	Description
7:0	RO	Data returned by Legacy SB16 / SBPRO ESP Read Operation

Register 1Ch / 1Dh SBR8 (Legacy Sound Blaster Command / Status Port)

Legacy Address: SBBase + Ch || SBBase + Dh

Default Value: 00h

Access: read/write

Bit	Access	Description
7:0	WO	The Command (Operator) or Data (Operand) Written to Legacy SB ESP
7	RO	0:Legacy SB ESP is Available For Next Command / Data 1:Legacy SB ESP is Busy.
6:0	RO	Reserved

After the command / data has been written to the ESP Command / DATA port, bit 7 of this status register will be set to 1 (busy) . After ESP has processed the written command / data and waiting for the next one , bit 7 of this status register will be reset to 0 (not busy). Any acknowledge byte must be readback before any new command is issued. ESP will be set busy after this port has ever been written and will be set not busy if the command/status has been read four times.

Register 1Eh SBR9 (Legacy Sound Blaster ESP Data Ready / IRQ Acknowledge Port 1)

Legacy Address: SBBase + Eh

Default Value: 00h

Access: read only

Bit	Access	Description
7	RO	0:Data is not available on SBR7. 1:Data is available on SBR7.
6:0	RO	Reserved

Reading this register will clear the interrupt generated by the ESP for NON-BX type legacy SB DMA command.

After SBR7 has been read, bit 7 of this register will reset to 0 (no data) until the next read data is available and set bit 7 of this register.

Register 1Fh SBR10 (Legacy Sound Blaster ESP Data Ready / IRQ Acknowledge Port 2)

Legacy Address: SBBase + Fh

Default Value: 00h

Access: Read only

Bit	Access	Description
7	RO	0:Data is not available on SBR7. 1:Data is available on SBR7.

6:0	RO	Reserved

Reading this register will clear the interrupt generated by the ESP for BX type legacy SB DMA command.

After SBR7 has been read, bit 7 of this register will reset to 0 (no data). If the next read data is available at SBR7, bit 7 of this register will again be set to 1.

Register 40h ACWR(AC'97 Mixer Write Register)

Default Value: : 00000000h

Access: Read /Write

Bit	Access	Description
31:16	R/W	Data to be written into AC'97 mixer register;
15	R/W	Read 0:ready to write AC'97 mixer register 1:busy writing AC'97 mixer (indexed by Bit 7..0); Write 0:do nothing 1:write AC'97 mixer register (indexed by bit 7..0) with bit 31-16;
14	R/W	Audio_Write_Busy: indicating Audio driver is busy writing AC'97. Write 0 to clear. Write 1: if bit 13 = 0, this bit can be set, else do nothing. Read 0: fail to set Audio_Write_Busy. 1: succeed to set Audio_Write_Busy.
13	RO	Modem_Write_Busy: indicating Modem driver is busy writing AC'97. Write : If BSModem enabled, do nothing, else clear this bit. Read 1: indicating Modem driver is busy writing AC'97. Read 0: Modem driver is not busy writing AC'97.
12:8	R/W	Reserved
7:0	R/W	Index of the AC'97 mixer register to be written; Bit 7=0 for Primary CODEC; Bit 7=1 for Secondary CODEC.

Register 44h ACRD(AC'97 Mixer Read Register)

Default Value: 00000000h

Access: Read /Write

Bit	Access	Description

31:16	R/W	AC' 97 mixer register contents Reserved
15	R/W	Read 0:bit 31..16 is valid data of AC' 97 mixer register (indexed by bit 7..0) 1:busy reading AC' 97 mixer register (indexed by bit 7..0); Write 0:do nothing 1:read AC' 97 mixer register (indexed by bit 7..0) to bit 31..16;
14	R/W	Audio_Read_Busy: indicating Audio driver is busy reading AC' 97. Write 0 to clear. Write 1: if bit 13 = 0, this bit can be set, else do nothing. Read 0: fail to set Audio_Read_Busy. 1: succeed to set Audio_Read_Busy.
13	RO	Modem_Read_Busy: indicating Modem driver is busy reading AC' 97. Write : If BSModem enabled, do nothing, else clear this bit. Read 1: indicating Modem driver is busy reading AC' 97. Read 0: Modem driver is not busy reading AC' 97.
12:8	R/W	**Reserved**
7:0	R/W	Index of the AC' 97 mixer register to be read; Bit 7=0 for Primary CODEC; Bit 7=1 for Secondary CODEC.

Register 48h SCTRL (Serial INTF Control Register)

Default Value: 00014000h

Access: Read /Write

Bit	Access	Description
26	RO	**CODEC Power Down State Flag** 0:Normal 1:CODEC is in power down mode When PM_ST enters D3, this bit will be set.
25	RO	**Secondary CODEC Ready Flag** 0: Not ready

		1: Ready
24	RO	**Primary CODEC Ready Flag** 0: Not ready 1: Ready
23	R/W	**GPIOOUT Slot Enable** 0: Disable 1: Enable (If DBLRATE_EN is 0)
22	R/W	**HSETOUT Slot Enable** 0: Disable 1: Enable (If DBLRATE_EN is 0)
21	R/W	**LINE2OUT Slot Enable** 0: Disable 1: Enable (If DBLRATE_EN is 0)
20	R/W	**LINE1OUT Slot Enable** 0: Disable 1: Enable
19	R/W	**LFEOUT Slot Enable** 0: Disable 1: Enable
18	R/W	**CENTEROUT Slot Enable** 0: Disable 1: Enable
17	R/W	**SURROUT L/R Slot Enable** 0: Disable 1: Enable
16	R/W	**PCMOUT L/R Slot Enable**, Default: 1 0: Disable 1: Enable (Default)
15:14	R/W	**Secondary CODEC ID** Default: 01
13	R/W	**GPIOIN Slot Select** 0: Primary CODEC GPIOIN slot input to GPIOIN buffer

		1: Secondary CODEC GPIOIN slot input to GPIOIN buffer
12	R/W	**HSETIN Slot Select** 0: Primary CODEC HSETIN slot input to HSETIN buffer 1: Secondary CODEC HSETIN slot input to HSETIN buffer
11	R/W	**LINE2IN Slot Select** 0: Primary CODEC LINE2IN slot input to LINE2IN buffer 1: Secondary CODEC LINE2IN slot input to LINE2IN buffer
10	R/W	**MIC Slot Select** 0: Primary CODEC MIC slot input to MIC buffer 1: Secondary CODEC MIC slot input to MIC buffer
9	R/W	**LINE1IN Slot Select** 0: Primary CODEC LINE1IN slot input to LINE1IN buffer 1: Secondary CODEC LINE1IN slot input to LINE1IN buffer
8	R/W	**PCMIN Slot Select** 0: Primary CODEC PCMIN slot input to PCMIN_A buffer 1: Secondary CODEC PCMIN slot input to PCMIN_A buffer
7	R/W	**I2S Input Function Enable** 0: Disable If disabled, the clocks of I2S receiver should be shut down. 1: Enable
6	R/W	**I2S Output Function Enable** 0: Disable If disabled, the clocks of I2S transmitter should be shut down. 1: Enable
5	R/W	**S/PDIF Output Function Enable** 0:Disable If disabled, the clocks of S/PDIF transmitter should be shut down. 1: Enable
4	R/W	**CODEC Double Rate Enable** 0: Disable 1: Enable
3	R/W	**PCM Output Select** (Primary/Secondary)

		0: PCM Output up to Primary CODEC request 1: PCM Output up to Secondary CODEC request
2	R/W	**MCLK clock rate select for I2S Output** 0: MCLK = 12.288M 1: MCLK = 6.144M
1	R/W	**CODEC Cold Reset Command** 0: Normal 1: Cold Reset CODEC When write '1' to this bit, pin ACRST# should be driven to low for at least 1us. After Power up, this bit will set to issue AC'97 cold reset, SW must write 0 to stop issuing AC'97 cold reset.
0	R/W	**CODEC Warm Reset Command** 0: Normal 1: Warm Reset CODEC When write '1' to this bit, pin ACSYNC should be driven to high for at least 1us.

Register 4Ch ACGPIO (AC'97 General Purpose IO Register)

Default Value: 00000000h

Access: Read /Write

Bit	Access	Description
31:16	R/W	Data to be written into AC'97 through output Slot 12;
15	R/W	This bit is status when read. 0:ready to output AC'97 Slot 12 1:busy This bit is command when write 0:do nothing 1:output AC'97 Slot 12
14:5	R/W	**Reserved**
4	R/W	**Secondary CODEC GPIO_INT Enable** 0:Disable 1:Enable

3	R/W	**Primary CODEC GPIO_INT Enable** 0:Disable 1:Enable
2	R/W	**Secondary CODEC GPIO_INT Register** This bit will be updated with Secondary input Slot 12 bit 0 of every AC' 97 frame.
1	R/W	**Primary CODEC GPIO_INT Register** This bit will be updated with Primary input Slot 12 bit 0 of every AC' 97 frame.
0	R/W	**Reserved**

Register 50h ASR0 (SiS Audio Status Register)

Default Value: 00000000h

Access: Read Only

Bit	Access	Description
31:30	RO	**Reserved**
29	RO	**MPU401 Output Buffer Select** 0: 8-byte 1: 128-byte
28	RO	**Legacy Recording IRQ MASK** 0:Generate IRQ when legacy recording block length expired 1:Don't generate IRQ when legacy recording block length expired
27	RO	1:SB ESP is at special DMA mode
26:25	RO	00:SB ESP is at get operator state 01:SB ESP is at get first operand state 11:SB ESP is at get second operand state 10:SB ESP is at get third operand state
24	RO	1:SB Mixer Soft-Reset
23	RO	1:SB PRO Command Captured Most Recently (Non-Bx or Cx Type Command Captured)
22	RO	1:SB16 Command Captured Most Recently (Bx or Cx Type Command Captured)
21	RO	1:SB Engine Sample Rate Set By Frequency Most Recently
20	RO	1:SB Engine Sample Rate Set By Time Constant Most Recently

19	RO	1:SB16 Mixer Register Update
18	RO	1:SB PRO Mixer Register Update
17	RO	1:OPL3 Bank1 Key On/Off
16	RO	1:OPL3 Bank0 Key On/Off
15	RO	0:AC' 97 codec is not ready 1:AC' 97 codec is ready
14	RO	0:SB Mixer Register MX0E.1 is 0 1:SB Mixer Register MX0E.1 is 1
13	RO	0:SB ESP is not at Direct Recording Mode 1:SB ESP is at Direct Recording Mode
12	RO	0:SB ESP has no ack byte 1:SB ESP has ack byte that needs to be read out
11	RO	0:SB ESP DMA Command is not valid 1:SB ESP DMA command is valid
10	RO	0:SB ESP Engine at Digital Audio Off State 1:SB ESP Engine at Digital Audio On State
9:8	RO	00:SB ESP Engine Command Port Not Busy 01:SB ESP Engine Command Port Busy 10:SB ESP DMA Test Busy 11:SB ESP Command Buffer Full
7	RO	0:8 bit data format 1:16 bit data format
6	RO	0:mono 1:stereo
5	RO	0:unsigned data format 1:signed data format
4	RO	0:playback 1:recording
3	RO	0:SB DMA loop disable 1:SB DMA loop enable
2:0	RO	**LegacyCMD** 000 stop : No any operation. No contribution to Digital Mixer

		001 run : Normal operation. 010 silent_DMA: SBCL will count; CA, CBC won't count. No data fetching. No interpolation. No contribution to Digital Mixer 011 reserved 100 silent_SB : SBCL, CA & CBC will count as the same as run mode.No data fetching. No interpolation. No contribution to Digital Mixer 101 pause : SBCL, CA & CBC don't change. Let SBALPHA unchanged, CACHE_HIT=1 drive current LD (or LD_L, LD_R) to Digital Mixer 110 reserved 111 direct play : SBCL, CA & CBC don't change. drive SBDD to Digital Mixer

Only one bit of Bit 21 and Bit 20 can be set 1 by implemented SB ESP Engine at any time.

Only one bit of Bit 23 and Bit 22 can be set 1 by implemented SB ESP Engine at any time.

Register 54h ASR1 (Legacy Sound Blaster Frequency Read Back Register)

Default Value: 00h

Access: Read Only

Bit	Access	Description
15:0	RO	Sample Frequency Set by SB Command 41h or 42h

Register 56h ASR2 (Legacy Sound Blaster Time Constant Read Back Register)

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	Time Constant Value Set by SB Command 40h

Register 58h ASR3 (SiS Audio Scratch Register)

Default Value: 00000000h

Access: Read / Write

Bit	Access	Description
31:0	R/W	

Register 5ch ASR4 (SiS Audio Version Control Register)

Default Value: 88h

Access: Read Only

Bit	Access	Description
7:0	RO	

Register 5Eh ASR5 (SB ESP Version High Byte Control Register)

Default Value: 4h

Access: Read /Write

Bit	Access	Description
3:0	R/W	

Register 5Fh ASR6 (SB ESP Version Low Byte Control Register)

Default Value: 2h

Access: Read / Write

Bit	Access	Description
3:0	R/W	

Register 60h AOPLSR0 (OPL3 Emulation Channel Key on/off Trace Register)

Default Value: 00000000h

Access: Read Only

Bit	Access	Description
31:25	RO	**Reserved**
24:16	RO	Bank1 channel 8-0 key on/off event captured
15	RO	Read only 0:Bank0 1:Bank1
14	RO	**Reserved**
13:9	RO	1:OPL3 rhythm channel 4-0 key on/off event captured
8:0	RO	1:Bank0 channel 8- 0 key on/off event captured.

All the flag will be cleared after this register is read.

Register 70h SPDIF_CS (S/PDIF Channel Status Register)

Default Value: 02000000h

Access: Read/Write

Bit	Access	Description

31:30	R/W	**Reserved** Hardwired to 00b
29:28	R/W	**Clock Accuracy** Read/Write, Default: 00b
27:24	R/W	**Sample rate** Read/Write, Default: 2h (48kHz)
23:20	R/W	Read/Write, Default: 0h
19:16	R/W	Read/Write, Default: 0h
15:8	R/W	Read/Write, Default: 00h
7:6	R/W	Read/Write, Default: 00b
5:3	R/W	Read/Write, Default: 000b
2	R/W	**Copyright** Read/Write, Default: 00b
1	R/W	**Audio Content Flag** Read/Write, Default: 0
0	R/W	**Professional Flag** Read/Write, Default: 0

Register 7Ch GPIO(General purpose IO Register)

Default Value: 00000000h

Access: Read /Write

Bit	Access	Description
31:10	R/W	**Reserved**
9	R/W	Set to indicate BSModem that SiS Audio has issued AC' 97 power down command.
8	R/W	After Audio driver has initialized AC' 97, it must set this bit to inform BSModem.
7:1	R/W	**Reserved**
0	RO	Read 1 indicating that BSModem has initialized AC' 97.

All reserved bits return 0 when read.

14.2.1 Wave Engine Register:

64 voice channels are classified into two banks.

Bank A: channel 0-31 (optimized for MIDI)

Bank B: channel 32-63 (optimized for Wave, WDM Stream, DirectX buffer, I2S, S/PDIF, MODEM, Handset, Recording, Microphone, Main Mixer Capture, Reverb Send, Chorus Send, AC' 97 SURR, AC' 97 CENTER/LFE)

Each channel in Bank A can only be programmed as a playback channel with individual EM(envelope modulation), individual LFO AM and individual LFO FM.

Channels in Bank B have more flexibility. Each of them can be programmed as a Normal PB channel with global LFO AM and LFO FM but without EM, or as a Special PB channel, or as a REC channel, or as a REC_PB channel. Bit[31:19] of RegEC_B is Channel ATTRIBUTE.

Register 80h STAR_A (START command and status register for Bank A)

Default Value: 00000000h

Access: Read / Write

Bit	Access	Description
31:0	R/W	This register and STOP_A are used as Bank A channel start/stop command register when they are written, and used as Bank A channel running/stopped status register when they are read. bit n is for channel n. Reading from this I/O port will return the running/stopped status of Bank A 32 voice channels. 0:Stopped. When bit n is read as '0', it means any operation of channel n, including address generation, sample data fetching, interpolation, and envelope calculation is stopped. And this channel has no contribution to the digital mixer. This bit will be reset from '1' to '0' in four cases. When a '1' is written to the corresponding bit in register STOP_A . When out of data, i.e. when sample loop disabled and CSO (Current Sample Offset) >= ESO (End Sample Offset). When Ec (current envelope) drops down to -63.984375 dB. When current envelope buffer is in delay-stop mode, and EDLY count down to '0'. 1:Running. When bit n is read as '1', it means channel n is working. This bit will be set from '0' to '1' only when a '1' is written to the corresponding bit in register START_A. Writing to this I/O port means issuing a start command to address engine and envelope engine in expected channel.

		0:Ignore. A '0' written to bit n will not change the status of channel n. 1:Start. A '1' written to bit n will start channel n's address engine and envelope engine and also set the status bit n to '1'.

Register 84h STOP_A (Channel STOP command and status register for Bank A)

Default Value: 00000000h

Access: Read / Write

Bit	Access	Description
31:0	R/W	Reading from this I/O port will return the same value as from the last register START_A. Writing to this I/O port means issuing a stop command to address engine and envelope engine in expected channel. 0:Ignore. A '0' written to bit n will not change the status of channel n. 1:Stop. A '1' written to bit n will stop channel n's address engine and envelope engine, and also reset the corresponding status bit to '0'.

Register 88h DLY (Delay flag of Bank A)

Default Value: 00000000h

Access: Read / Write

Bit	Access	Description
31:0	R/W	When read, this register will show the delay status of each channel of Bank A. Bit n is for channel n. 0:Normal This bit will toggle from '1' to '0' when envelope engine change from a delay mode buffer to a non-delay mode buffer. When channel n is stopped, bit n will be reset to '0'. 1:Channel is currently in delay mode (address engine keep stopped but envelope engine is running). This bit will toggle from '0' to '1' only when envelope engine begin to deal with a delay mode buffer. When write,

		0:Ignore (don't change) 1:Set to '1'

Register 8Ch SIGN_CSO (Sign bit of CSO) (for Bank A only)

Default Value: 00000000h

Access: Read / Write

Bit	Access	Description
31:0	R/W	This register is used to store the sign bits of 32 channel's CSO of Bank A, with '0' means current sample address is greater than or equal to LBA(Loop Begin Address), while '1' means current sample address is little than or equal to LBA. This register can be programmed with an initial status and will be updated by address engine. Write '0':ignore (don't change) Write '1':set to '1' When channel n is stopped, bit n will be reset to '0'.

Register 90h CSPF_A(Bank A Current Sample Position Flag)

Default Value: 00000000h

Access: Read only

Bit	Access	Description
31:0	RO	This register will show a flag which indicates the Bank A's current sample is in a range between ESO/2 to ESO or in a range before ESO/2 (ESO is offset from loop begin to loop end). And this flag will be used for sample data double buffering control. Bit n is for channel n. 0:Before ESO/2 1:From ESO/2 to ESO When channel n is stopped, bit n will be reset to '0'.

Register 94h CEBC (Current Envelope Buffer Control) (for Bank A only)

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:0	R/W	Reading from this register will return current envelope buffer flags of 32 channels of Bank A, which indicate currently envelope engine is using parameters from EBUF1 or EBUF2. Bit n is for channel n.

		0:Buffer 1 1:Buffer 2 Writing '1' to bit n of this register will toggle the flag in channel n and force envelope engine to change buffer. Writing '0' to bit n won't change anything in channel. 0:Ignore 1:Toggle When channel n is stopped, bit n will be reset to '0'.

Register 98h AINT_A (Bank A address engine interrupt)

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:0	R/W	Any bits toggled from '0' to '1' will result in a IRQ. Reading from this I/O port will return the address INT status of Bank A's 32 channels. Bit n is for channel n. 0:No INT 1:INT This bit will be set in 2 cases: When CSO (current sample offset) >= ESO (end sample offset), and ENDLP_IE (end of loop INT enable bit in Global Control register) =1 and AINTEN_A bit n is set 1 for channel n. When CSO (current sample offset) >= ESO/2 (middle of ESO), and MIDLP_IE (middle of loop INT enable bit in Global Control register) =1 and AINTEN_A bit n is set 1 for channel n. Writing '1' to bit n of this register will reset this bit. 0:Ignore. A '0' written to bit n will not change the status of this bit. 1:Reset A '1' written to bit n will reset this bit.

Register 9Ch EINT(Envelope engine interrupt register) (for Bank A only)

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description

31:0	R/W	Any bits toggled from '0' to '1' will result in a IRQ. Reading from this I/O port will return the envelope INT status of 32 channels of Bank A. Bit n is for channel n. 0:No INT 1:INT This bit will be set in 2 cases: When envelope buffer toggled, and ETOG_IE (envelope toggle INT enable bit in Global Control register) =1. When Ec (current envelope) <= FFFh (-63.984375 dB), and EDROP_IE (envelope dropping to -63.984375dB INT enable bit in Global Control register) =1. Writing '1' to bit n of this register will reset this bit. 0:Ignore. A '0' written to bit n will not change the status of this bit. 1:Reset A '1' written to bit n will reset this bit.

Register A0h GC & CIR (Global Control & Channel Index)

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:30	R/W	This bits are used to control Legacy Recording channel when record to mono sample. 00:Left 01:Right 10:(left+right+1)/2 11:Reserved.
29:28	R/W	This bits are IO 0008-read handling control bits. 00:Never assert StatusRDY 01:StatusRDY = DMATCReached 10:StatusRDY = DMATCReached | LegacyDRQ 11:In this case, handshaking with StatusWR and manipulation of return byte should been done. StatusRDY keep '0' when initialization. If(StatusWR ==1) {

		StatusRDY = 1;
		if(DMAChannel==0) {
		ReturnByte[7:0] =
		{InputByte[7:5], DMAR8[4], InputByte[3:1], DMAR8[0]};
		}
		else {
		ReturnByte[7:0] =
		{InputByte[7:6], DMAR8[5], InputByte[4],
		InputByte[3:2], DMAR8[1], InputByte[0]};
		}
		}
		if(DMASNOOPCS_==0 & ADR[7:0] = 8 & Data_rdy_ == 0 & StatusRDY==1)
		StatusRDY = 0;

27	R/W	Test_loopback: This bit is used for wave engine loopback testing. 0:Normal 1:Force recording engine get new data from playback FIFO instead of aclink.
26	R/W	**Debugging Mode** 0:Normal 1:Chip is in Debugging Mode. In Debugging Mode, 20 pins (including 8 pins of GPIO, 1 pin of SPDIF , 6 pins of I2S and 5 NC pins) are used as output to monitor 40 internal important signals.
25:24	R/W	**EXPROM Map Mode** 00: 000h-1FFh of EXPROM is mapped to AudioMemBase 800h-FFFh low 16 bits; 800h-9FFh of EXPROM is mapped to AudioMemBase 800h-FFFh high 16 bits; 01: 200h-3FFh of EXPROM is mapped to AudioMemBase 800h-FFFh low 16 bits; A00h-BFFh of EXPROM is mapped to AudioMemBase 800h-FFFh high 16 bits; 10: 400h-5FFh of EXPROM is mapped to AudioMemBase 800h-FFFh low 16 bits;

		C00h-DFFh of EXPROM is mapped to AudioMemBase 800h-FFFh high 16 bits; 11: 600h-7FFh of EXPROM is mapped to AudioMemBase 800h-FFFh low 16 bits; E00h-FFFh of EXPROM is mapped to AudioMemBase 800h-FFFh high 16 bits.
23	R/W	**EXPROM Dump Mode Enable** 0:Disable 1:Enable If enabled, EXPROM(4096x12bit) is mapped to AudioMemBase according to bit[25:24], i.e. the content of EXPROM can be read out through AudioMem Read cycle.
22:21	R/W	**Test mode bits** 00:normal mode (chip works normally in this mode) 01:test mode 1 10:test mode 2 11:test mode 3
20	R/W	**Main Mixer Output Control** 0:Main Mixer L/R → PCM L/R Output FIFO 1:Main Mixer L/R → MMC L/R Output Buffer
19	R/W	**S/PDIF Out Control** 0:S/PDIF L/R Output Buffer → S/PDIF L/R transmitter 1:PCM L/R Output FIFO → S/PDIF L/R transmitter
18	R/W	**I2S Out Control** 0:I2S L/R Output Buffer → I2S transmitter 1:SURR L/R Output FIFO → I2S transmitter
17	R/W	**PCMIN_B Mixing Enable/Disable** 0:PCMIN_B Mixing Disable 1:PCMIN_B Mixing Enable Note: Controlled by PCMIN_SEL in Reg48h, either of Primary CODEC PCMIN slot or Secondary CODEC PCMIN slot will come into 3-level PCMIN_A buffer. And if PCMIN_B Mixing bit is enabled, the other slot will come into 1-level PCMIN_B buffer and will be mixed into Main Mixer.
16	R/W	**64-Channel Mode**

		0:Legacy Mode 1:64 Channel Mode
15	R/W	This bit is INT enable bit for current envelope dropping to -63.984375dB. 0:Disable 1:Enable
14	R/W	This bit is INT enable bit for envelope buffer toggling. 0:Disable 1:Enable
13	R/W	This bit is INT enable bit for middle of loop. 0:Disable 1:Enable
12	R/W	This bit is INT enable bit for end of loop. 0:Disable 1:Enable
11	R/W	This bit is INT enable bit for playback underrun. 0:Disable 1:Enable When playback FIFO is empty, if this bit is set as '1', a IRQ will be issued.
10	R/W	This bit is INT enable bit for recording overrun. 0:Disable 1:Enable When recording FIFO is full, if this bit is set as '1', a IRQ will be issued.
9	R/W	This bit is Pause/Resume command bit. Read 0:Engine hasn't been paused yet. 1:Engine has been paused already. Write 0:Resume Engine. 1:Pause Engine. When host writes '1', this bit may not show '1' immediately. Engine will try to get paused as soon as possible. After engine has been paused already, this bit will be set to '1'. Once host writes '0', this bit will be reset to '0' immediately and engine will work normally.

8	R/W	This bit is used to reset playback sample timer counter. When read , return 0;write 1 will reset STimer.
5:0	R/W	This bit is the channel index which is used to select a channel for access. 00h selects channel 0, 1Fh selects channel 31, 3Fh selects channel 63.

All other bits are reserved.

Register A4h AINTEN_A(Bank A Address Engine Interrupt Enable)

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:0	R/W	This register will control address engine interrupt for each channel of Bank A. Bit n is for channel n. 0:Disable address engine interrupt for channel n 1:Enable address engine interrupt for channel n

Register A8h MUSICVOL & WAVEVOL(Global Music Volume & Global Wave Volume)

Default Value: 00008080h

Access: Read/Write

Bit	Access	Description
31:24	R/W	**Music right volume** 0 :0dB(no attenuation) FFh :-63.75dB(mute)
23:16	R/W	**Music left volume** 0 :0dB(no attenuation) FFh :-63.75dB(mute)
15:8	R/W	**Wave right volume** 0 :0dB(no attenuation) 80h :-32dB (default) FFh :-63.75dB(mute)
7:0	R/W	**Wave left volume** 0 :0dB(no attenuation) 80h :-32dB (default)

		FFh :-63.75dB(mute)

Register Ach SBDELTA/DELTA_R (Sample Change Step for Legacy Playback & Recording)

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:16	R/W	**Reserved.**
15:0	R/W	SBDELTA: Fs/F48k in 4.12 format. SBDELTA_R: F48k/Fs in 4.12 format.

Register B0h MISCINT (Miscellaneous Int & Status)

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
24	R/W	(ACGPIO_IRQ) is AC97 GPIO interrupt request. ACGPIO_IRQ = Reg4Ch[1] & Reg4Ch[3] | Reg4Ch[2] & Reg4Ch[4].
23	R/W	(ST_IRQ_En) is ST IRQ enable bit. 0:disable 1:enable
17	R/W	(opltimer_ie) is OPL3 timer interrupt enable bit. 0:disable 1:enable
16	R/W	(PB_24K_MODE) is playback 48k/24k mode control bit. 0:(default)Wave engine drives sample to CODEC at 48Khz 1:Wave engine drives sample to CODEC at 24Khz(in this mode, Delta should be programmed twice as that in 48Khz mode).
15	R/W	(ST_TARGET_REACHED) is a flag with '1' indicates STIMER counter has been equal to ST_TARGET. This bit will be set to '1' once STIMER counter is equal to ST_TARGET. Write '1' will clear this bit.
11	R/W	(mixer_overflow_flag) is a flag which indicates the result of mixer accumulator exceeds 7FFFFh.

		This bit will be set to '1' once accumulator overflows. Write '1' will clear this bit.
10	R/W	(mixer_underflow_flag) is a flag which indicates the result of mixer accumulator is less than 80000h. This bit will be set to '1' once accumulator underflows. Write '1' will clear this bit.
9	R/W	(REC_OVERUN) is recording overrun status bit. Active high. This bit will be set to '1' if recording is running & rec_req_ is active & data_rdy haven't come.
8	R/W	(PB_UNDERUN) is playback FIFO underrun status bit. Active high. This bit will be set to '1' if playback is running & FIFO is empty & f48 clock is coming.
7	R/W	(ST_IRQ) is Sample Timer IRQ bit. Active high. Bit[7] = ST_IRQ_En | ST_TARGET_REACHED
6	R/W	(ENVELOPE_IRQ) is Wave-table Envelope Engine IRQ bit. Active high. Bit[6] = | EINT[31:0]
5	R/W	(ADDRESS_IRQ) is Wave-table Address Engine IRQ bit. Active high. Bit[5] = (| AINT_A[31:0]) | (| AINT_B[31:0])
4	R/W	(OPL3_IRQ) is OPL3 timer IRQ bit. Active high. Bit[4] = timerirq & opltimer_ie
3	R/W	(MPU401_IRQ) is MPU401 IRQ bit. Active high. Bit[3] = mpu401irq (signal from Legacy Audio block)
2	R/W	(SB_IRQ) is sound blaster IRQ bit. Active high. Bit[2] = sbirq (signal from Legacy Audio block)
1	R/W	(REC_OVERUN_IRQ) is recording overrun IRQ bit. Active high. Bit[1] = OVERUN_IE & Bit[9].
0	R/W	(PB_UNDERUN_IRQ) is playback FIFO underrun IRQ bit. Active high. Bit[0] = UNDERUN_IE & Bit[8].

All other bits are reserved bits.

Register B4h STAR_B (START command and status register for Bank B)

Default Value: 0000h

Access: Read / Write

Bit	Access	Description
31:0	R/W	This register and STOP_B are used as Bank B channel start/stop command register when they are written, and used as Bank B channel running/stopped status register when they are read. bit n is for channel n. Reading from this I/O port will return the running/stopped status of Bank B 32 voice channels. 0:Stopped. When bit n is read as '0', it means any operation of channel n, including address generation, sample data fetching, interpolation, and envelope calculation is stopped. And this channel has no contribution to the digital mixer. This bit will be reset from '1' to '0' in four cases. When a '1' is written to the corresponding bit in register STOP_B. When out of data, i.e. when sample loop disabled and CSO (Current Sample Offset) >= ESO (End Sample Offset). When Ec (current envelope) drops down to -63.984375 dB. When current envelope buffer is in delay-stop mode, and EDLY count down to '0'. 1:Running. When bit n is read as '1', it means channel n is working. This bit will be set from '0' to '1' only when a '1' is written to the corresponding bit in register START_B. Writing to this I/O port means issuing a start command to address engine and envelope engine in expected channel. 0:Ignore. A '0' written to bit n will not change the status of channel n. 1:Start. A '1' written to bit n will start channel n's address engine and envelope engine and also set the status bit n to '1'.

Register B8h STOP_B (Channel STOP command and status register for Bank B)

Default Value: 0000h

Access: Read / Write

Bit	Access	Description

31:0	R/W	Reading from this I/O port will return the same value as from the last register START_B. Writing to this I/O port means issuing a stop command to address engine and envelope engine in expected channel. 0:Ignore. A '0' written to bit n will not change the status of channel n. 1:Stop. A '1' written to bit n will stop channel n's address engine and envelope engine, and also reset the corresponding status bit to '0'.

Register BCh CSPF_B(Bank B Current Sample Position Flag)

Default Value: 00000000h

Access: Read only

Bit	Access	Description
31:0	RO	This register will show a flag which indicates the Bank B's current sample is in a range between ESO/2 to ESO or in a range before ESO/2 (ESO is offset from loop begin to loop end). And this flag will be used for sample data double buffering control. Bit n is for channel n. 0: Before ESO/2 1: From ESO/2 to ESO When channel n is stopped, bit n will be reset to '0'.

Register C0h SBBL & SBCL (Sound Blaster Base Block Length & Current Block Length)

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:0	R/W	SBBL(Bit 31-16) is sound blaster base block length SBCL(Bit 15-0) is current value of sound blaster block length counter If sound blaster DMA loop is enabled(SBCTRL[3]=1), every time when SBCL changed from 0 to FFFFh, a INT will be issued, the contents of SBCL is reloaded from SBBL, and DMA operation continues . If sound blaster DMA loop is not enabled(SBCTRL[3]=0), every time when SBCL changed from 0 to FFFFh, a INT will be issued, the contents of SBCL is reloaded from SBBL, and set LegacyCMD

		to 101(pause). SBCTRL bit 7 is used to determine the counter operation mode (byte count or word count). The counter is a count down counter.

Register C4h SBCTRL & SBE2R & SBDD (Sound Blaster Control)

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:24	R/W	This bit is sound blaster DMA testing byte command data port(write only) Any time after Bit31-24 has ever been written, E2Status (source from wave engine) will be set high. E2Status will be cleared after the testing byte has been sent to the system location.
15:8	R/W	This bit is sound blaster direct mode playback data port
7:0	R/W	This bit is legacy sound blaster voice in/out control register
7	R/W	0:8 bit data format 1:16 bit data format
6	R/W	0:mono 1:stereo
5	R/W	0:unsigned data format 1:signed data format
4	R/W	0:playback 1:recording
3	R/W	**Sound blaster DMA loop enable control** 0:loop disabled. 1:loop enabled.
2:0	R/W	**LegacyCMD** 000 stop : No any operation. No contribution to Digital Mixer 001 run : Normal operation. 010 silent_DMA: SBCL will count; CA, CBC won't count. No data fetching. No interpolation. No contribution to Digital Mixer 011 reserved 100 silent_SB : SBCL, CA & CBC will count as the same as run mode. No data fetching. No interpolation. No contribution to Digital Mixer

		101 pause : SBCL, CA & CBC don't change. let SBALPHA unchanged, CACHE_HIT=1 drive current LD (or LD_L, LD_R) to Digital Mixer 110 reserved 111 Direct_playback: SBCL, CA & CBC don't change.drive SBDD to Digital Mixer

Register C8h STimer (Playback Sample Timer)

Default Value: 00000000h

Access: Read only

Bit	Access	Description
31:0	RO	Bit 31-0 (STimer) will show current state of the sample timer counter which will count up every f48k clock and will be reset when RST_Stimer bit being written. Active high.

Register CCh LFO_B And I2S_DELTA (Bank B Low Frequency Oscillator Control)

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:27	R/W	Reserved – Read Only 00000b
26:16	R/W	This bits is used for Bank B LFO control
26	R/W	(LFO_E_B) is Bank B LFO enable bit. 0:Disabled 1:Enabled
25:24	R/W	(LFO_R_B) is clock rate select of Bank B LFO counter. 00:LFO counter clock rate is 48kHz 01:LFO counter clock rate is 48kHz/4 10:LFO counter clock rate is 48kHz/16 11:LFO counter clock rate is 48kHz/64
23:16	R/W	(LFO_INIT_B)is the initial value of the Bank B LFO counter which will count down to 0 then reload.
15:13	R/W	**Reserved**.
12:0	R/W	(I2S_DELTA) (Read only) This register returns the auto-detected DELTA of I2S input (fi2s/f48K).

Register D0h ST_TARGET (Sample Timer Target)

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:0	R/W	Bit 31-0 (ST_TARGET) is used to store a pre-set value. Once STIMER counter reaches that value, an IRQ called ST_IRQ will be issued if ST_IRQ_En = 1.

Register D8h AINT_B (Bank B address engine interrupt)

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:0	R/W	Any bits toggled from '0' to '1' will result in a IRQ. Reading from this I/O port will return the address INT status of Bank B's 32 channels. Bit n is for channel n. 0:No INT 1:INT This bit will be set in 2 cases: When CSO (current sample offset) >= ESO (end sample offset), and ENDLP_IE (end of loop INT enable bit in Global Control register) =1 and AINTEN_B bit n is set 1for channel n. When CSO (current sample offset) >= ESO/2 (middle of ESO), and MIDLP_IE (middle of loop INT enable bit in Global Control register) =1 and AINTEN_B bit n is set 1 for channel n. Writing '1' to bit n of this register will reset this bit. 0:Ignore. A '0' written to bit n will not change the status of this bit. 1:Reset A '1' written to bit n will reset this bit.

Register DCh Power Management Capability Register

Default Value: E6620001h

Access: Read/Only

Bit	Access	Description
31:0	RO	This register will present the status of Power management Capability.

Register E0h E0h (CSO & ALPHA & FMS) (for Bank A & Bank B)

Default Value: XXXXXXXXh

Access: Read/Write

Bit	Access	Description
31:16	R/W	(CSO) is the offset of current sample relative to loop begin sample.
15:4	R/W	(ALPHA) is sample interpolation coefficient, which stands for the linear interpolation ratio between current sample and the next one.
3:0	R/W	(FMS) is Frequency Modulation Step.

Register E4h (LBA) (for Bank A & Bank B)

Default Value: XXXXXXXXh

Access: Read/Write

Bit	Access	Description
31	R/W	(CPTR) is reserved for internal use of cache control
30:0	R/W	This bits is the linear address of loop begin sample. It should be word aligned when sample type is 16-bit Mono or 8-bit Stereo and should be double word aligned when sample type is 16-bit Stereo.

Register E8h (ESO & DELTA) (for Bank A & Bank B)

Default Value: XXXXXXXXh

Access: Read/Write

Bit	Access	Description
31:16	R/W	(ESO) is the offset of loop end sample relative to loop begin sample.
15:0	R/W	(DELTA) is sample change step in format 4.12 (Four bits integer, 12 bits fraction), which stands for the frequency ratio: Fs/48KHz, while Fs is the sum of sample rate and pitch shifting rate

Register ECh (Bank A LFO_CTRL & LFO_CT & FMC & RVOL & CVOL) (Bank A Only)

Default Value: XXXXXXXXh

Access: Read/Write

Bit	Access	Description
31:28	R/W	(SIN) Sine wave value.
27	R/W	(SIN_S) sign bit of sine wave.

		0:positive 1:negative
26	R/W	(SIN_D) counter direction bit. 0:up 1:down
25:24	R/W	(LFO_R) LFO counter clock rate select bits. 00:48kHz 01:48kHz/4 10:48kHz/16 11:48kHz/64
23:16	R/W	(LFO_CT)LFO working counter.
15:14	R/W	(FMC) FM modulation control bits. 00:FMA = (FMS * SIN) >> 3 01:FMA = (FMS * SIN) >> 2 10:FMA = (FMS * SIN) >> 1 11:FMA = (FMS * SIN) >> 0
13:7	R/W	(RVOL)**Reverb Send Linear Volume** format: 1.6, 7Fh stands for 2x gain, 40h stands for no gain no attenuation, 00h stands for mute.
6:0	R/W	**Chorus Send Linear Volume** format: 1.6, 7Fh stands for 2x gain, 40h stands for no gain no attenuation, 00h stands for mute.

Register ECh (Bank B ATTRIBUTE & FMC & RVOL & CVOL) (Bank B Only)

Default Value: XXXXXXXXh

Access: Read/Write

Bit	Access	Description
31:19	R/W	(ATTRIBUTE) **Channel attribute**
31:30	R/W	**PB/REC Select** 00:(Normal PB) Normal playback This is a normal playback channel in Bank B with Global Volume, Channel Volume, PAN, SRC, FM/AM features. In this case, bit[29:19] doesn't matter. 01:(Special PB) Special playback

		This channel can be one of several kinds of special playback channels. Bit[29:26] is used to select special playback type; bit[25:24] is used to select data flow from channel to FIFO; and bit[23:19] is used to enable/disable individual functions. 10:(REC) Recording to system memory This channel can be one of several kinds of recording channels. Bit[29:26] is used to select recording type; bit[25:24] is used to control how MONO sample is generated when recording; bit[23] is used to enable/disable SRC; bit[22:19] doesn't matter. 11:(REC_PB) Recording to system memory and playback to mixer This channel is a Recording channel which records sample data to system memory and playback to Main Mixer in the mean time. In this case, bit[29:26] is used to select recording type; bit[25:24] is used to control how MONO sample is generated when recording; and bit[23:19] is used to enable/disable individual functions.
29:26	R/W	**Channel Type Select** When Bit[31:30] is 00: (Normal PB) xxxx reserverd When Bit[31:30] = 01: (Special PB) 0000 playback to MODEM LINE1 Output FIFO 0001 playback to MODEM LINE2 Output FIFO 0010 playback to PCM L/R Output FIFO 0011 playback to HSET Output FIFO 0100 playback to I2S L/R Output Buffer 0101 playback to CENTER/LFE Output FIFO 0110 playback to SURR L/R Output FIFO 0111 playback to SPDIF L/R Output FIFO other reserved When Bit[31:30] = 1x: (REC or REC_PB) 0000 recording from MODEM LINE1 Input FIFO 0001 recording from MODEM LINE2 Input FIFO 0010 recording from PCM L/R Input FIFO 0011 recording from HSET Input FIFO 0100 recording from I2S L/R Input FIFO 0101 recording from MIC Input FIFO

		0110 main mixer capture from PCM L/R Output FIFO 0111 main mixer capture from MMC L/R Output Buffer 1000 Reverb Send 1001 Chorus Send other reserved
25:24	R/W	Special Playback Channel to FIFO data flow select / Recording to MONO control When channel is in Special PB mode, this register is used to select input source of a stereo playback slot pairs such as PCM L/R, SURR L/R, CENTER/LFE, I2S L/R and SPDIF L/R. The input source of L/R can be from one channel or can be from two independent channels. When channel is in REC or REC_PB mode, this register is used to control how MONO sample is generated. When Bit[31:30] = 00 (Normal PB) xx never used When Bit[31:30] = 01 (Special PB) 00 Channel L/R to FIFO L/R In this case, channel is acting as a stereo channel, data flow is like Channel Left → FIFO Left Channel Right → FIFO Right 01 Channel L to FIFO L Data flow: Channel Left → FIFO Left 10 Channel R to FIFO R Data flow: Channel Right → FIFO Right 11 reserved When Bit[31:30] = 1x (REC or REC_PB) 00: Left, 01: Right 10: (left+right+1)/2 11: Reserved.
23	R/W	**SRC Enable**

		0:Disable 1:Enable
22	R/W	**FM and AM Enable** 0:Disbale 1:Enable
21	R/W	**PAN Enable** 0:Disable 1:Enable
20	R/W	**Channel Volume Enable** 0:Disable 1:Enable
19	R/W	**Global Volume Enable** 0:Disable 1:Enable
18:16	R/W	**Reserved**
15:14	R/W	**FM modulation control bits.** 00:FMA = (FMS * SIN) >> 3 01:FMA = (FMS * SIN) >> 2 10:FMA = (FMS * SIN) >> 1 11:FMA = (FMS * SIN) >> 0
13:7	R/W	**Reverb Send Linear Volume** Format: 1.6, 7Fh stands for 2x gain, 40h stands for no gain no attenuation, 00h stands for mute.
6:0	R/W	**Chorus Send Linear Volume** Format: 1.6, 7Fh stands for 2x gain, 40h stands for no gain no attenuation, 00h stands for mute.

Register F0h (Bank A GVSEL & PAN & VOL & CTRL & Ec) (for Bank A only)

Default Value: XXXXXXXXh

Access: Read/Write

Bit	Access	Description
31	R/W	(GVSEL) is global volume select bit. 0:Select MUSICVOL

		1:Select WAVEVOL
30:24	R/W	(PAN) is Positioning attenuation control.
30	R/W	Selects attenuated channel. 0: left, 1: right
29:24	R/W	This bits is the attenuation value in format of 4.2. 3Fh stand for mute.
23:16	R/W	(VOL) is channel volume attenuation in format of 5.3. 00h stands for 0 dB attenuation, FFh stands for mute.
15	R/W	**Selects 8/16 bit sample data** 0:8-bit data 1:16-bit data
14	R/W	**Selects mono/stereo sample data** 0:Mono 1:Stereo
13	R/W	**Selects unsigned/signed sample data** 0:Unsigned 1:Signed
12	R/W	**This bit is loop mode enable bit.** 0:Disable 1:Enable
11:0	R/W	This bits is current envelope in format of 6.6 (Six bits integer and six bits fraction). 00h stands for 0dB, FFh stands for -63.984375 dB.

Register F0h (Bank B GVSEL & PAN & VOL & CTRL & Bank A LFO_INIT)

Default Value: XXXXXXXXh

Access: Read/Write

Bit	Access	Description
31	R/W	(GVSEL) is global volume select bit. 0:Select MUSICVOL 1:Select WAVEVOL
30:24	R/W	(PAN) is Positioning attenuation control.
30	R/W	Selects attenuated channel. 0: left, 1: right.
29:24	R/W	This bits is the attenuation value in format of 4.2. 3Fh stand for mute

23:16	R/W	(LFO_INIT) is Bank A per channel LFO counter initial and reload value. Note: Any time when host write to RegECh[26:16] (LFO_CT), LFO_INIT should be written with the same value.
15:12	R/W	This bits are control bits.
15	R/W	**Selects 8/16 bit sample data** 0:8-bit data 1:16-bit data
14	R/W	**Selects mono/stereo sample data** 0:Mono 1:Stereo
13	R/W	**Selects unsigned/signed sample data** 0:Unsigned 1:Signed
12	R/W	**This bits is loop mode enable bit.** 0:disable 1:enable
11:0	R/W	(VOL) is channel volume attenuation in format of 6.6. 000h stands for 0 dB attenuation, FFFh stands for mute.

Register F4h (EBUF1) (Bank A Only)

Default Value: XXXXXXXXh

Access: Read/Write

Bit	Access	Description
31:30	R/W	(AMS_H) is Amplitude Modulation Step High part.
29:28	R/W	(EMOD) define operation mode. 00:DEC mode (ramp from 0dB to -64dB) In this mode, bits 7-0 of this register are used as ECNT which stores current state of a 8-bit counter; bits 15-8 of this register are used as EINIT which provides initial value of that 8-bit counter; bits 27-16 of this register are used as EAMT which is the absolute ramping amount with range from 0dB to 63 and 63/64 dB. Every 48KHz clock, ECNT decrease 1; every time when ECNT=00h, it reload EINIT, EAMT decrease 1, and Ec decrease 1; every time when EAMT=00h, envelope engine will

		toggle buffer flag in global register CEBC. 01:INC mode (ramp from -64dB to 0dB) In this mode, the layout of this register is completely the same as in DEC mode. Engine works in the same way except that the ramp direction is from -64dB to 0dB. 10:Delay mode In this mode, bits 27-26 are used to select sub-mode: 00:Delay_hold 01:Delay_start 10:Delay_stop 11:reserved 19-0 is used as EDLY which store the current state of a 20-bit delay counter, bits 25-20 are of no use. Every 48 KHZ clock, EDLY decrease 1. During all the time this buffer active, Ec keep unchanged. In Delay_hold sub-mode, when EDLY =00000h, engine will toggle current buffer flag in global register CEBC. In Delay_start sub-mode, when EDLY =00000h, engine will reset DLY flag register. In Delay_stop sub-mode, when EDLY =00000h, engine will reset start/stop flag register. 11:Still mode In this mode, Ec keep unchanged, buffer never toggle automatically. Only when CEBC is written, buffer may toggle.

Register F8h (EBUF2) (Bank A Only)

Default Value: XXXXXXXXh

Access: Read/Write

Bit	Access	Description
31:0	R/W	EBUF2 is totally as the same as EBUF1except that bits 31-30 are AMS_L (Amplitude Modulation Step Low part).

15 Register Summary / Description – ACPI/SMBus Summaries

15.1 ACPI Configuration Registers

Offset	Byte Length	Access	Name	Abbreviate
00	2	R/WC	Power Management Status	PM1_STS
02	2	R/W	Power Management Enable	PM1_EN
04	2	R/W	Power Management Control	PM1_CNT
06	2	RO	Reserved	
08	4	RO	Power Management Timer	PM_TMR
0C	4	RO	Reserved	
10	4	R/W	Processor Control	P_CNT
14	1	RO	Processor Power State Level 2	P_LVL2
15	1	RO	Processor Power State Level 3	P_LVL3
16	4	RO	Reserved	
1A	2	R/W	Fix Feature Control	FIX_CNT
1C	2	WO	PM1_STS Write Port	PM1_PORT
1E	2	RO	Reserved	
20	2	R/WC	General Purpose Event 0 Status	GPE0_STS
22	2	R/W	General Purpose Event 0 Enable	GPE0_EN
24	4	R/W	GPE0 Interrupt Routing	GPE0_ROUT
28	2	R/W	GPE0 Trigger Mode Select	GPE0_TRG
2A	2	R/W	General Purpose Event Control	GPE_CNT
2C	2	WO	GPE0_STS Write Port	GPE0_PORT
2E	2	RO	Reserved	
30	2	R/WC	General Purpose Event 1 Status	GPE1_STS
32	2	R/W	General Purpose Event 1 Enable	GPE1_EN
34	4	R/W	GPE1 Interrupt Routing	GPE1_ROUT
38	2	R/W	GPE1 Trigger Mode Select	GPE1_TRG
3A	2	R/W	GPE1 Pin Level	GPE1_LVL
3C	2	R/W	GPE1 I/O Mode Select	GPE1_IO
3E	2	R/W	GPE1 Input Polarity Select	GPE1_POL
40	2	R/WC	Legacy Event Status	LEG_STS
42	2	R/W	Legacy Event Enable	LEG_EN
44	2	R/W	Device Activity Status	DEVACT_STS
46	2	RO	Reserved	

48	1	R/W	SMI# Command Port	SMICMD_PORT
49	1	R/W	Mail Box	MAIL_BOX
4A	1	R/W	SFTMR Initial Value	SF_TMR
4B	1	R/W	Software Watchdog Timer Control	SFTMR_CNT
4C	4	RO	High Resolution Timer Value	HR_TMR
50	2	R/W	PIO Port Trap 0 Address	IOTRAP0_PORT
52	2	R/W	PIO Port Trap 1 Address	IOTRAP1_PORT
54	1	R/W	PIO Port Trap 0 Mask	IOTRAP0_MASK
55	1	R/W	PIO Port Trap 1 Mask	IOTRAP1_MASK
56	2	R/W	Legacy Event Control	LEG_CNT
58	2	WO	LEG_STS Write Port	LEG_PORT
5A	2	R/W	IRQ/NMI Wake Control	IOQWAK_CNT
5C	2	RO	I/O Address Track for SMI#	ADDR_TRACK
5E	1	RO	I/O C/BE# Track for SMI	CBE_TRACK
5F	1	R/W	I^2C Bus Control	I^2C_CNT
60	2	RO	System Wakeup From S5 Status	S5WAK_STS
62	2	R/W	System Wakeup From S5 Control	S5WAK_CNT

15.2 Register Summary / Description – SMBus

15.2.1 SMBus Control Registers

Offset	Byte Length	Access	Name	Abbreviate
80	1	R/WC	SMBUS Status	SMB_STS
81	1	R/W	SMBUS Enable	SMB_EN
82	1	R/W	SMBUS Control	SMB_CNT
83	1	R/W	SMBUS Host Control	SMBHOST_CNT
84	1	R/W	SMBUS Address	SMB_ADDR
85	1	R/W	SMBUS Command	SMB_CMD
86	1	RO	SMBUS Processed Byte Count	SMB_PCOUNT
87	1	R/W	SMBUS Byte Count	SMB_COUNT
88	8	R/W	SMBUS Byte0~7	SMB_BYTE0~7
90	1	R/W	SMBUS Device Address	SMBDEV_ADDR
91	1	R/W	SMBUS Device Byte 0	SMB_DB0
92	1	R/W	SMBUS Device Byte 1	SMB_DB1
93	1	R/W	SMBUS Host Slave Alias Address	SMB_SAA

15.3 ACPI Register

The following registers located at I/O base address <Base> + the indicated offset value <Offset>. The base address is programmed in the Register PCI Configuration space.

Register 00h~01h Power Management Status Register (PM1_STS)

Default Value: 0000h

Access: Read/Write Clear

The following registers are all sticky bits and only can be cleared by writing a one to their corresponding fields.

Bit	Access	Description
15	R/WC	**Wake up Status (WAK_STS)** This bit is set when the system is in the sleeping state and an enabled wake-up event occurs. Upon setting this bit, the system will translate form sleep state to S0 state.
14:12	RO	**Reserved**
11	R/WC	**Ignored (Power Button Override Status)**
10	R/WC	**RTC Status (RTC_STS)** This bit is set when the RTC generates an IRQ8#. While both RTC_EN bit and RTC_STS bit are set, a power management event is raised.
9	RO	**Reserved**
8	R/WC	**Power Button Status (PWRBTN_STS)** This bit is set when the power button is pressed (the PWRBTN# signal is asserted Low). If PWRBTN_STS and PWRBTN_EN are both set under S0 state, then a SCI or SMI# is raised. If PWRBTN_STS bit is set under sleeping state, a WAKE event will be generated.
7:6	RO	**Reserved**
5	R/WC	**Global Status (GBL_STS)** When the ACPI software attemps to gain the ownership of the Global Lock, this bit would be set by the access to the BIOS_RLS.
4	R/WC	**Bus Master Status (BM_STS)** This is the bus master status bit. This bit is set when a system bus master is requesting the system bus.
3:1	RO	**Reserved**

0	R/WC	**Power Management Timer Status (PMTMR_STS)** This bit will be set if the MSB of PM_TMR is changed from '1' to '0' or '0' to '1'. While PMTMR_STS and PMTMR_EN bit are set, a power management event (SCI or SMI#) is raised.

Register 02h~03h Power Management Enable Register (PM1_EN)

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:11	RO	**Reserved**
10	R/W	**RTC Enable (RTC_EN)** This bit is used to enable the assertion of the RTC_STS to generate a power management event (Wake and SCI/SMI#).
9	RO	**Reserved**
8	R/W	**Power Button Enable (PWRBTN_EN)** This bit is used to enable the assertion of the PWRBTN_STS bit to generate a power management event (SCI/SMI#). The system always can wake up from Sx by Power Button regardless of the value of this bit.
7:6	RO	**Reserved**
5	R/W	**Global Enable (GBL_EN)** When the BIOS drive releases the lock, this bit is used to enable the assertion of the GBL_STS to generate a SCI.
4:1	RO	**Reserved**
0	R/W	**Power Management Timer Status (PMTMR_EN)** This is PMTMR enable bit. If this bit and PMTMR_STS bit are set, then a power management event is generated (SCI/SMI#).

Register 04h~05h Power Management Control Register (PM1_CNT)

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:14	RO	**Reserved**

13	WO	**Sleep Enable (SLP_EN)** This is a wirte only bit and always returns a zero when read. Setting this bit to one will cause the system to enter the sleep state defined by the SLP_TYP field.
12:10	R/W	**Sleeping Type (SLP_TYP)** Define the power-saving mode that the system should enter when the SLP_EN bit is set to one. 000 : S0 state (***Working***) 001 : S1 state (***STPCLK#***) 010 : S2 state (***STPCLK# and/or CPUSLP#***) 011 : S3 state (***Suspend To RAM***) 100 : S4 state (***Suspend To Disk***) 101 : S5 state (***Soft_Off***)
9:3	RO	**Reserved**
2	WO	**Global Lock Release (GBL_RLS)** This bit is used by the ACPI software to raise a SMI# to the BIOS software. Writing a one to this register will generate a BIOS event to set BIOS_STS in LEG_STS.
1	R/W	**Bus Master Reload Enable (BM_RLD)** If enabled, a bus master request will cause any processor in the C3 state to transition to the C0 state. 0 : Disable 1 : Enable
0	R/W	**SCI Enable (SCI_EN)** Selects the power management event in PM1 to be either SCI or SMI#. When this bit is set, a power management event will generate SCI. When this bit is reset, a power management event will generate SMI#.

Register 06h~07h Reserved

Register 08h~0Bh ACPI Power Management Timer Register (PM_TMR)

Default Value: Free Running

Access: Read Only

Bit	Access	Description
31:24	RO	**Reserved**

23:0	RO	**Power Management Timer Value** This read-only field reflects the current counting of the power management timer. The PM_TMR value will be reset when the system enter one of the sleeping state (S1~S5). Reading to this field will stop the running of PM_TMR.

Register 0Ch~0Fh Reserved

Register 10h~13h ACPI Processor Control Register (P_CNT)

Default Value: 0000 0000

Access: Read/Write

Bit	Access	Description
31:5	RO	**Reserved**
4	R/W	**Throttling Function Enable** This bit enables the C0 clock throttling function.
3:1	R/W	**Throttling Duty Cycle Control** This 3-bit field determines the duty cycle of the STPCLK# signal when the system is in the C0 throttling mode. **Bits** — **Performance Rate** 000 — 100% 001 — 12.5% 010 — 25% 011 — 37.5% 100 — 50% 101 — 62.5% 110 — 75% 111 — 87.5%
0	RO	**Reserved**

Register 14h ACPI Processor Power State Level 2 (P_LVL2)

Default Value: 00

Access: Read Only

Bit	Access	Description

7:0	RO	**Enter C2 Power State Register** Reading to this register returns all zeros; writes to this register have no effect. Reads to this register will also generate a " Enter C2 power state " event.

Register 15h ACPI Processor Power State Level 3 (P_LVL3)

Default Value: 00

Access: Read Only

Bit	Access	Description
7:0	RO	**Enter C3 Power State Register** Reading to this register returns all zeros; writes to this register have no effect. Reads to this register will also generate a " Enter C3 power state " event.

Register 16h~19h Reversed

Register 1Ah~1Bh ACPI Fix Feature Control Register (FIX_CNT)

Default Value: 0040

Access: Read Only

Bit	Access	Description
15:10	RO	**Reserved**
9	R/W	**PM Timer Test Mode Enable** 0 : Disable 1 : Enable
8	R/W	**ACPI Fix Feature Test Mode Enable** 0 : Disable 1 : Enable
7	R/W	**PM1_STS Write Port Enable (PM1PORT_EN)** If this bit is enabled, writing a one to PM1_PORT register will cause the corresponding bit in PM1_STS to be set. 0 : Disable 1 : Enable

6	R/W	**Power Button Override Function Enable** When this bit is reset, the power button override function will be disabled. 0 : Disable 1 : Enable
5:4	R/W	**Power Button Trigger Mode Selection** The value in this field can select the trigger mode of power button. If the level mode is selected, PWRBTN_STS will always be set during the period of pressing power button. If the edge mode is selected, PWRBTN_STS can only be set once according to the power button is pressed or released. 00 : Level Mode 01 : Button press edge mode 10 : Button release edge mode 11 : Reversed
3	RO	**Reserved**
2	RO	**Reserved**
1	WO	**BIOS Release (BIOS_RLS)** The ACPI software can set GBL_STS by writing a one to this field.
0	RO	**Reserved**

Register 1Ch~1Dh PM1_STS Write Port (PM1_PORT)

Default Value: 0000

Access: Write Only

Bit	Access	Description
15:0	WO	**PM1_STS Write Port** Writing a one to this register will cause the corresponding field of PM1_STS to be set. Before writing to this register, PM1PORT_EN must be set.

Register 1Eh~1Fh Reserved

Register 20h~21h General Purpose Event 0 Status Register (GPE0_STS)

Default Value: 0000h

Access: Read/Write Clear

The following registers are all sticky bits and only can be cleared by writing a one to their

corresponding fields. When one of status and their corresponding enable bits are set in S1/S2, a wakeup event is generated. If the status and the corresponding rerouting bits are set during working state (S0), an SCI/SMI#/IRQ will be generated. Note that IRQWAK_STS, USBWAK_STS, and EXTSMIWAK_STS can only be set during sleeping state.

Bit	Access	Description
15	R/WC	**IRQ Wake Status (IRQWAK_STS)** This bit is set when one of the enabled 8259 IRQ wakeup events is generated in S1/S2 state. Note: The IRQ wake-up events are defined in IRQWAK_CNT register.
14	R/WC	**USB0 Wake Status (USB0WAK_STS)** This bit is set when ACPI circuit detects a wake up event in sleeping state (S1/S2). The wake-up event is generated from USB port 0, 1.
13	RO	**Reserved**
12	R/WC	**MAC Power Management Event Status (MACPME_STS)** This bit is set when internal MAC power management event is generated.
11	R/WC	**PCI Power Management Event Status (PCIPME_STS)** This bit is set when PCI power management event is asserted for more than 4ms.
10	R/WC	**BS-Audio Power Management Event Trigger (BSAUDPME_TRG)**
9	R/WC	**Keyboard Controller Status (KBC_STS)** This bit is set when an internal keyboard controller hotkey event (CTRL+DEL+Backspace) is generated.
8	R/WC	**Ring Indication Status (RING_STS)** This bit is set when the RING goes active for more than 4ms. This bit can be choosed as quite or noise mode in GPECNT register. In quite mode, RING_STS can only be set during sleeping state (S1/S2). In noisy mode, RING_STS can be set in working and sleeping states.
7	R/WC	**SMBus Interrupt/I^2C Alert Status (SMBINT_STS/I^2CALT_STS)** If SMBus mode is selected, this bit will be set when a SMB interrupt is generated. If I^2C mode is selected, this bit will be set when I^2CALT# goes active.
6	RO	**Reserved**

5	R/WC	**Audio Controller Power Management Event Status (AUDPME_STS)** This bit is set when an internal AC' 97 power management event is generated.
4	R/WC	**USB1 Wake Status (USB1WAK_STS)** This bit is set when internal USB host controller detects a wake up event in sleeping state (S1/S2). The wake-up event is generated from USB port 2,3.
3	R/WC	**EXTSMI# Wake Status (EXTSMIWAK_STS)** This bit is set when EXTSMI# goes active in sleeping state (S1/S2).
2	R/WC	**EXTSMI# Status (EXTSMI_STS)** This bit is set when EXTSMI# goes active in working state (S0).
1	R/WC	**Thermal Event Override Status (THRMOR_STS)** This bit is set when THERM# goes active for more than 2 seconds. If THRMOR_DTY and THRMOR_THT are set, the system will enter thermal throttling mode.
0	R/WC	**Thermal Event Status (THRM_STS)** This bit is set when THERM# goes active.

Register 22h~23h General Purpose Event 0 Enable Register (GPE0_EN)

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15	R/W	**IRQ Wake Enable (IRQWAK_EN)**
14	R/W	**USB Wake Enable (USBWAK01_EN)**
13	RO	**Reserved**
12	R//W	**MAC Power Management Event Enable (MACPME_EN)**
11	R//W	**PCI Power Management Event Enable (PCIPME_EN)**
10	R/W	**BS-Audio Power Management Event Enable (BSAUDPME_EN)**
9	R/W	**Keyboard Controller Enable (KBC_EN)**
8	R/W	**Ring Indication Enable (RING_EN)**
7	R/W	**SMBus Interrupt/I²C Alert Enable (SMBINT_EN/I²CALT_EN)**
6	RO	**Reserved**

5	R/W	**Audio Controller Power Management Event Enable (AUDPME_EN)**
4	R/W	**USB Wake Enable (USBWAK23_EN)**
3	R/W	**EXTSMI# Wake Enable (EXTSMIWAK_EN)**
2	R/W	**EXTSMI# Enable (EXTSMI_EN)**
1	R/W	**Thermal Event Override Enable (THRMOR_EN)**
0	R/W	**Thermal Event Enable (THRM_EN)**

Register 24h~27h General Purpose Event 0 Interrupt Routing Register (GPE0_ROUT)

Default Value: 0000 0000h

Access: Read/Write

The following registers are GPE0 routing registers. If one of GPE0_STS is set and its corresponding GPE0_ROUT register is routing to SCI/SMI#/GPEIRQ, an SCI/SMI#/GPEIRQ will be generated.

Bit	Access	Description
31:30	R/W	**IRQ Wake Route (IRQWAK_ROUT)** 00 : No effect 01 : SMI# 10 : SCI 11 : GPEIRQ
29:28	R/W	**USB Wake Route (USBWAK01_ROUT)**
27:26	RO	**Reserved**
25:24	R/W	**MAC Power Management Event Route (MACPME_ROUT)**
23:22	R/W	**PCI Power Management Event Route (PCIPME_ROUT)**
21:20	R/W	**BS-Audio Power Management Event Trigger (BSAUDPME_ROUT)**
19:18	R/W	**Keyboard Controller Route (KBC_ROUT)**
17:16	R/W	**Ring Indication Route (RING_ROUT)**
15:14	R/W	**SMBus/I²C Route (SMBINT_ROUT/I²CALT_ROUT)**
13:12	RO	**Reserved**
11:10	R/W	**Audio Controller Power Management Event Route (AUDPME_ROUT)**
9:8	R/W	**USB Wake Route (USBWAK23_ROUT)**

7:6	R/W	**EXTSMI# Wake Route (EXTSMIWAK_ROUT)**
5:4	R/W	**EXTSMI# Route (EXTSMI_ROUT)**
3:2	R/W	**Thermal Event Override Route (THRMOR_ROUT)**
1:0	R/W	**Thermal Event Route (THRM_ROUT)**

Register 28h~29h General Purpose Event 0 Trigger Mode Selection (GPE0_TRG)

Default Value: 0000h

Access: Read/Write

If GPE0 is set to level trigger mode, the GPE0_STS will always be set by the active event as long as the event is not de-asserted. If GPE0_TRG is set to be edge trigger mode, the active event can only set GPE0_STS once before the active event is de-asserted.

Bit	Access	Description
15	R/W	**IRQ Wake Trigger (IRQWAK_TRG)** 0 : Level trigger mode 1 : Edge trigger mode
14	R/W	**USB Wake Trigger (USBWAK01_TRG)**
13	RO	**Reserved**
12	R/W	**MAC Power Management Event Trigger (MACPME_TRG)**
11	R/W	**PCI Power Management Event Trigger (PCIPME_TRG)**
10	R/W	**BS-Audio Power Management Event Trigger (BSAUDPME_TRG)**
9	R/W	**Keyboard Controller Trigger (KBC_TRG)**
8	R/W	**Ring Indication Trigger (RING_TRG)**
7	R/W	**SMBus/I²C Trigger (SMBINT_TRG/I²CALT_TRG)**
6	RO	**Reserved**
5	R/W	**Audio Controller Power Management Event Trigger (AUDPME_TRG)**
4	R/W	**USB Wake Trigger (USBWAK23_TRG)**
3	R/W	**EXTSMI# Wake Trigger (EXTSMIWAK_TRG)**
2	R/W	**EXTSMI# Trigger (EXTSMI_TRG)**
1	R/W	**Thermal Event Override Trigger (THRMOR_TRG)**
0	R/W	**Thermal Event Trigger (THRM_TRG)**

Register 2Ah~2Bh General Purpose Event Control (GPE_CNT)

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:8	RO	**Reserved**
7	R/W	**GPE0_STS Write Port Enable (GPE0PORT_EN)** If this bit is enabled, writing a one to GPE0_PORT register will cause the corresponding bit in GPE0_STS to be set. 0 : Disable 1 : Enable
6	R/W	**RING Indication Quite/Noisy Mode Control (RING_CNT)** If RING is set to be quite mode, RING_STS can only be set in sleeping state (S1/S2). If the noisy mode is selected, RING_STS can be set in working and sleeping state. 0 : Noisy mode 1 : Quite mode
5	R/W	**SMBus/I²C Function Select (SMB_SEL)** If this bit is set to one, SMBDAT/I²CDAT, SMBCLK/I²CCLK, and SMBALT#/I²CALT# will be switched as I²C mode. Otherwise, they will be selected as SMBus mode. 0 : SMBus mode select 1 : I²C mode select
4	RO	**Reserved**
3	R/W	**Thermal Override Throttling Function Enable (THRMOR_THT)** This bit enables the thermal override throttling function. 0 : Disable 1 : Enable

2:0	R/W	**Thermal Override Throttling Duty Cycle Control** This 3-bit field determines the duty cycle of the STPCLK# signal when the thermal override event is generated. **Bits** — **Performance Rate** 000 — 100% 001 — 12.5% 010 — 25% 011 — 37.5% 100 — 50% 101 — 62.5% 110 — 75% 111 — 87.5%

Register 2Ch~2Dh GPE0_STS Write Port (GPE0_PORT)

Default Value: 0000

Access: Write Only

Bit	Access	Description
15:0	WO	**GPE0_STS Write Port** Writing a one to this register will cause the corresponding field of GPE0_STS to be set. Before writing to this register, GPE0PORT_EN must be set.

Register 2Eh~2Fh Reserved

Register 30h~31h General Purpose Event 1 Status Register (GPE1_STS)

Default Value: 0000h

Access: Read/Write Clear

The following registers are all sticky bits and only can be cleared by writing a one to their corresponding fields. When one of status and their corresponding enable bits are set in S1/S2, a wakeup event is generated. If the status and the corresponding rerouting bits are set during working state (S0), an SCI/SMI#/IRQ will be generated. Not that if GPIO[n] are selected as output mode or their mux-ed function, their corresponding status bits must be ignored. So do their enable and route registers must be set to zero.

Bit	Access	Description
15:3,1:0	R/WC	**GPIO[15:3,1:0] Status (GPIO[15:3, 1:0]_STS)** This bit is set when one of GPIO[15:3, 1::0] event goes active.

2	R/WC	**GPIO2/Instant Off Status (GPIO[2]_STS/INSTOFF_STS)** This bit is set when one of GPIO2/Instant Off event goes active. If LPC bridge configuration register 48h bit 5 is enabled, the assertion of GPIO2_STS would power off the machine compulsively.

Register 32h~33h General Purpose Event 1 Enable Register (GPE1_EN)

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:0	R/W	**GPIO[15:0] Enable (GPIO[15:0]_EN)**

Register 34h~37h General Purpose Event 1 Interrupt Routing Register (GPE1_ROUT)

Default Value: 0000 0000h

Access: Read/Write

The following registers are GPE1 routing registers. If one of GPE1_STS is set and its corresponding GPE1_ROUT register is routing to SCI/SMI#/GPEIRQ, an SCI/SMI#/GPEIRQ will be generated.

Bit	Access	Description
31:30	R/W	**GPIO15 Route (GPIO15_ROUT)** 00 : No effect 01 : SMI# 10 : SCI 11 : GPEIRQ
29:0	R/W	**GPIO[14:0] Route (GPIO[14:0]_ROUT)** See the pattern of GPIO15_ROUT.

Register 38h~39h General Purpose Event 1 Trigger Mode Selection (GPE1_TRG)

Default Value: 0000h

Access: Read/Write

If GPE1 is set to level trigger mode, the GPE1_STS will always be set by the active event as long as the event is not de-asserted. If GPE1_TRG is set to be edge trigger mode, the active event can only set GPE1_STS once before the active event is de-asserted.

Bit	Access	Description

15:0	R/W	**GPIO[15:0] Trigger (GPIO[15:0]_TRG)** 0 : Level trigger mode 1 : Edge trigger mode

Register 3Ah~3Bh General Purpose Event 1 Pin Level (GPE1_LVL)

Default Value: 0000h

Access: Read/Write

If GPIO[n] is set to input mode, the input level of its corresponding GPIO pin can be read from this register. If GPIO[n] is set to output mode, the output level can be control through this register. Note that the output value of GPIO[n] must be written to this register before GPIO[n] is switch to output mode.

Bit	Access	Description
15:0	R/W	**GPIO[15:0] Pin Level (GPIO[15:0]_LVL)** 0 : Pin input level low/Pin output level low 1 : Pin input level high/Pin output level high

Register 3Ch~3Dh General Purpose Event 1 Input/Output Mode Select (GPE1_IO)

Default Value: FFFFh

Access: Read/Write

Bit	Access	Description
15:0	R/W	**GPIO[15:0] Input/Output Mode Select (GPIO[15:0]_IO)** 0 : Output Mode 1 : Input Mode

Register 3Eh~3Fh General Purpose Event 1 Input Polarity Select (GPE1_POL)

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:0	R/W	**GPIO[15:0] Input Polarity Select (GPIO[15:0]_POL)** 0 : Active low 1 : Active high

Register 40h~41h Legacy Event Status Register (LEG_STS)

Default Value: 0000h

Access: Read/Write Clear

The following registers are all sticky bits and only can be cleared by writing a one to their corresponding fields.

Bit	Access	Description
15	R/WC	**Software Watch Dog Timer Event 1 Status (SFTMR1_STS)** This bit is set when the software watchdog timer expires the second time. This status bit does not have its corresponding enable bit and can survive under PCIRST#.
14	R/WC	**Software Watch Dog Timer Event 0 Status (SFTMR1_STS)** This bit is set when the software watchdog timer expires the first time. This status bit does not have its corresponding enable bit and can survive under PCIRST#.
13	R/WC	**General Purpose Event Status (GPESMI_STS)** This bit is set when the SMI# is caused by GPE0 or GPE1. This status bit does not have its corresponding enable bit.
12	R/WC	**Power Management Status (PM1SMI_STS)** This bit is set when the SMI# is caused by PM1. This status bit does not have its corresponding enable bit.
11	R/WC	**Legacy USB Status (LEGUSB_STS)** This bit is set when a legacy USB SMI# is activated and only used for port 0,1.
10	R/WC	**Legacy USB Status (LEGUSB_STS)** This bit is set when a legacy USB SMI# is activated and only used for port 2,3.
9	R/WC	**Serial IRQ SMI# Status (SIRQSMI_STS)** This bit is set when internal Serial IRQ decoder asserts an SMI#.
8	R/WC	**LPC SMI# Status (LPCSMI_STS)** This bit is set when internal LPC controller asserts an SMI#.
7	R/WC	**One Minute Status (ONEMIN_STS)** This bit is set every one minute. In legacy power management, ONEMIN_STS and ONEMIN_EN can be used to monitor the device status every one minute.
6	R/WC	**RTC Year 2000 Roll Over Status (RTCY2K_STS)** This bit is set when the 9th bit of RTC time register rolls from 99 to 00. This bit can be used to monitor the Y2K event.
5	R/WC	**SMI# Command Status (SMICMD_STS)** This bit is set when OS write a value to SMI# command port.

4	R/WC	**BIOS Status (BIOS_STS)** This bit is set when the BIOS driver write a one to GBL_RLS in PM1_CNT register.
3	R/WC	**Input/Output Trap 1 Status (IOTRAP1_STS)** This bit is set when software initiates an I/O access to the range of IOTRAP1_PORT and IOTRAP1_MASK
2	R/WC	**Input/Output Trap 0 Status (IOTRAP0_STS)** This bit is set when software initiates an I/O access to the range of IOTRAP0_PORT and IOTRAP0_MASK
1	RO	**Reserved**
0	R/WC	**SMI# Status (SMI_STS)** This bit is set when one of the SMI# source is activated. The SMI# will be masked for 128 PCI clock after clearing this bit.

Register 42h~43h Legacy Event Enable Register (LEG_EN)

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:12	RO	**Reserved**
11	R/W	**USB PORT 0,1 SMI# Enable**
10	R/W	**USB PORT 2,3 SMI# Enable**
9	R/W	**Serial IRQ SMI# Enable (SIRQSMI_EN)**
8	R/W	**LPC SMI# Enable (LPCSMI_EN)**
7	R/W	**One Minute Enable (ONEMIN_EN)**
6	R/W	**RTC Year 2000 Roll Over Enable (RTCY2K_EN)**
5	R/W	**SMI Command Enable (SMICMD_EN)**
4	R/W	**BIOS Enable (BIOS_EN)**
3	R/W	**Input/Output Trap 1 Enable (IOTRAP1_EN)**
2	R/W	**Input/Output Trap 0 Enable (IOTRAP0_EN)**
1	RO	**Reserved**
0	R/W	**SMI Enable (SMI_EN)**

Register 44h~45h Device Activity Status Register (DEVACT_STS)

Default Value: 0000h

Access: Read/Write Clear

The following registers are all sticky bits and only can be cleared by writing a one to their corresponding fields.

Bit	Access	Description
15	R/WC	**Primary IDE Activity Status (IDEPACT_STS)** This bit is set when software initiates an I/O access to the range of 170h~177h and 376h.
14	R/WC	**Secondary IDE Activity Status (IDESACT_STS)** This bit is set when software initiates an I/O access to the range of 1F0h~1F7h and 3F6h.
13:12	RO	**Reserved**
11	R/WC	**Sound Blaster Activity Status (SBACT_STS)** This bit is set when software initiates an I/O access to the range of 220h~233h, 240h~253h, 260h~273h, and 280h~293h.
10	R/WC	**Microsoft Sound Activity Status (MSSACT_STS)** This bit is set when software initiates an I/O access to the range of 530h~537h, 604h~60Bh, E80h~E87h, and F40h~F47h.
9	R/WC	**MIDI Activity Status (MIDIACT_STS)** This bit is set when software initiates an I/O access to the range of 300h~303h, 310h~313h, 320h~323h, and 330h~333h.
8	R/WC	**Keyboard Controller Activity Status (KBCACT_STS)** This bit is set when software initiates an I/O access to the range of 60h and 64h.
7	R/WC	**Game Port Activity Status (GAMEACT_STS)** This bit is set when software initiates an I/O access to the range of 200h~207h and 388h~38Bh.
6	R/WC	**Floopy Activity Status (FLPYACT_STS)** This bit is set when software initiates an I/O access to the range of 3F0h~3F7h and 370h~377h.
5	R/WC	**Serial Port Activity Status (SERACT_STS)** This bit is set when software initiates an I/O access to the range of 2E8h~2EFh, 2F8h~2FFh, 3E8h~3EFh, and 3F8h~3FFh.
4	R/WC	**Parallel Port Activity Status (PARLACT_STS)** This bit is set when software initiates an I/O access to the range of 278h~27Fh, 378h~37Fh, and 3BCh~3BEh.

3	R/WC	**INTD# Activity Status (INTDACT_STS)** This bit is set when PCI INTD# goes active.
2	R/WC	**INTC# Activity Status (INTCACT_STS)** This bit is set when PCI INTC# goes active.
1	R/WC	**INTB# Activity Status (INTBACT_STS)** This bit is set when PCI INTB# goes active.
0	R/WC	**INTA# Activity Status (INTAACT_STS)** This bit is set when PCI INTA# goes active.

Register 46h~47h Reversed

Register 48h SMI# Command Port Register (SMICMD_PORT)

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**SMI# Command Port Value** Writing to this register will generate an SMI# command event.

Register 49h Mail Box Register (MAIL_BOX)

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	Read/Write Free Byte

Register 4Ah Software Watchdog Timer Initial Value (SF_TMR)

Default Value: FFh

Access: Read/Write

Bit	Access	Description
7:0	R/W	**Software Watchdog Timer Initial Value** Writing to this register will reload the software watchdog timer with the value specified in this register. If the software watchdog timer expires the first time, the expired event will set the SFTMR0_STS and the timer will reload its initial value and count again. If the timer expire the second time, the expired event will set the SFTMR1_STS.

Register 4Bh Software Watchdog Timer Control Register (SFTMR_CNT)

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Software Watchdog Timer Counting Enable** The software watchdog timer will start to count when this bit is set to one.
6	RO	**Reserved**
5:4	R/W	**Software Watchdog Timer Clock Select** 00 : 4ms 01 : 1sec 10 : 1min 11 : 1hour
3:2	R/W	**Software Watchdog Timer Expiration Event 1 Routing Select** When SFTMR1_STS is set to one, an SMI#/SFTIRQ/PCIRST# will be generated according to the following combination. 00 : No effect 01 : SMI# 10 : SFTIRQ 11 : PCIRST#
1:0	R/W	**Software Watchdog Timer Expiration Event 0 Routing Select** When SFTMR0_STS is set to one, an SMI#/SFTIRQ/PCIRST# will be generated according to the following combination. 00 : No effect 01 : SMI# 10 : SFTIRQ 11 : PCIRST#

Register 4Ch~4FhHigh Resolution Timer Counting Value (HR_TMR)

Default Value: 0000 0000h

Access: Read Only

Bit	Access	Description

31:0	RO	**High Resolution Timer Value** This read-only field reflects the current counting of HR_TMR. The clock source can be applied from MAC or AC'97. If this timer is disabled, the counting value will be reset to zero. Note: The control register of PM_TMR is located in LEG_CNT.

Register 50h~51h Programmable 16-bits I/O Port Trap 0 Address (IOTRAP0_PORT)

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:0	R/W	**I/O Port Trap 0 Address** Any I/O access to the range of IOTRAP0_PORT and IOTRAP0_MASK will cause IOTRAP0_STS to be set to one.

Register 52h~53h Programmable 16-bits I/O Port Trap 1 Address (IOTRAP1_PORT)

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:0	R/W	**I/O Port Trap 1 Address** Any I/O access to the range of IOTRAP1_PORT and IOTRAP1_MASK will cause IOTRAP1_STS to be set to one.

Register 54h Programmable 16-bits I/O Port Trap 0 Mask (IOTRAP0_MASK)

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**I/O Port Trap 0 Mask** A one in this register will select the low 8-bit mask for IOTRAP0_PORT.

Register 55h Programmable 16-bits I/O Port Trap 1 Mask (IOTRAP1_MASK)

Default Value: 00h

Access: Read/Write

Bit	Access	Description

7:0	R/W	**I/O Port Trap 0 Mask** A one in this register will select the low 8-bit mask for IOTRAP1_PORT.

Register 56h~57h Legacy Event Control (LEG_CNT)

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:8	RO	**Reserved**
7	R/W	**LEG_STS Write Port Enable (LEGPORT_EN)** If this bit is enabled, writing a one to LEG_PORT register will cause the corresponding bit in LEG_STS to be set. 0 : Disable 1 : Enable
6:4	RO	**Reserved**
3:2	R/W	**High Resolution Timer Clock Source Select** 00 : MAC 25MHz/25 (1MHz) 01 : Reserved 10 : AC' 97 12.288MHz/12 (1024KHz) 11 : AC' 97 12.288MHz/16 (768KHz)
1	R/W	**High Resolution Timer Counting Enable** If HR_TMR is disabled, the HR_TMR value will be reset to zero. 0 : Disable 1 : Enable
0	R/W	**SMI# Mask Interval Select** If SMI_STS is cleared, the SMI# will be masked a certain time according to this register. 0 : 128 PCICLK 1 : 8 PCICLK

Register 58h~59h LEG_STS Write Port (LEG_PORT)

Default Value: 0000h

Access: Write Only

Bit	Access	Description

15:0	WO	**LEG_STS Write Port** Writing a one to this register will cause the corresponding field of LEG_STS to be set. Before writing to this register, LEGPORT_EN must be set.

Register 5Ah~5Bh IRQ and NMI Enable for Wake-up Event Control (IRQWAK_CNT)

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:3	R/W	Correspond to the enable bits for IRQ[15:3] to generate a wake-up event
2	R/W	Correspond to the enable bits for NMI to generate a wake-up event
1:0	R/W	Correspond to the enable bits for IRQ[1:0] to generate a wake-up event

Register 5Ch~5Dh I/O Address Track for SMI# (ADDR_TRACK)

Default Value: 0000h

Access: Read Only

Bit	Access	Description
15:0	RO	**I/O Address Track** The reading value in this register reflects the address of last I/O cycle from CPU before the system enter SMI# handler.

Register 5Eh~5Fh I/O Command/Byte Enable Track for SMI# (CBE_TRACK)

Default Value: 0000h

Access: Read Only

Bit	Access	Description
15:10	RO	**Reserved**
9	R/W	**I^2C DATA** When Register 2A[5] is selected as I^2C mode, the level of pin SMBDAT is controlled by this bit.
8	R/W	**I^2C CLOCK** When Register 2A[5] is selected as I^2C mode, the level of pin SMBCLK is controlled by this bit.

7:4	RO	**I/O Command Track** The reading value in this register reflects the command of last I/O cycle from CPU before the system enter SMI# handler.
3:0	RO	**I/O Byte Enable Track** The reading value in this register reflects the byte enable of last I/O cycle from CPU before the system enter SMI# handler.

Register 60h~61h System Wakeup form S3/S4/S5 Status Register (S5WAK_STS)

Default Value: 0000h

Access: Read Only

The following registers are all located in resume well. They can survive as long as the standby power exists. The only way to clear the register is to write S5WAK_CLR or deassert AUXOK.

Bit	Access	Description
15	RO	**Power Button Wakeup Status (PWRBTN_S5WAK_STS)** This bit will be set if power button wakes up the system from S3/S4/S5.
14	RO	**RTC Wakeup Status (RTC_S5WAK_STS)** This bit will be set if a RTC IRQ8# wakes up the system from S3/S4/S5.
13	RO	**RING Wakeup Status (RING_S5WAK_STS)** This bit will be set if RING wakes up the system from S3/S4/S5.
12	RO	**MACPME Wakeup Status (MACPME_S5WAK_STS)** This bit will be set if MAC power management event wakes up the system from S3/S4/S5.
11	RO	**PCIPME Wakeup Status (PCIPME_S5WAK_STS)** This bit will be set if PCI power management event wakes up the system from S3/S4/S5.
10	RO	**AUDPME Wakeup Status (AUDPME_S5WAK_STS)** This bit will be set if AC'97 power management event wakes up the system from S3/S4/S5.
9	RO	**Keyboard Password/Hotkey Wakeup Status (KBC_S5WAK_STS)** This bit will be set if keyboard password or hotkey wakes up the system from S3/S4/S5.

8	RO	**USB Wakeup Status (USB_S5WAK_STS)** This bit will be set if USB wakes up the system from S3/S4/S5.
7	RO	**SMBALT# Wakeup Status (SMBALT_S5WAK_STS)** This bit will be set if SMBALT# wakes up the system from S3/S4/S5.
6	RO	**Power Supply Resume to Previous State Status (RSM_S5WAK_STS)** This bit will be set if power supply resume function wakes up the system from S5.
5:2	RO	**Reserved**
1	RO	**System Suspend to DRAM State Status (S3OFF_STS)** This bit will be set if the system enters to S3 state.
0	R/W	Instant Off status (INSTOFF_STS) This bit will be set if the system is powered off due to the assertion of GPE1B2_STS.

Register 62h~63h System Wakeup form S3/S4/S5 Control Register (S5WAK_CNT)

Default Value: 0000h

Access: Read/Write

The following registers are all located in resume well. They can survive as long as the standby power exists.

Bit	Access	Description
15:10	RO	**Reserved**
9:8	R/W	**Wake Block Counter Test Enable** 0: Disable 1: Enable
7:6	RO	**ACPILED Output State Control** The output state of ACPILED can be controlled by the following combination when system is in S0/S1/S2/S3 states. If the system is in S4/S5 state, ACPILED will be set to high impedience. 00 : Output low 01 : Blink 10 : High impedience 11 : Reversed
5:4	RO	**Reserved**

3	R/W	**AUXGPO6** If the GPIO6 is selected as GPO6 and AUXGPO6_EN is set, then the value of GPO6 pin could be controlled by this bit. The pin can be alive when main power disappears.
2	R/W	**AUXGPO5** If the GPIO5 is selected as GPO5 and AUXGPO5_EN is set, then the value of GPO5 pin could be controlled by this bit. The pin can be alive when main power disappears.
1	R/W	**AUXGPO8** If the GPIO8 is selected as GPO8 and AUXGPO8_EN is set, then the value of GPO8 pin could be controlled by this bit. The pin can be alive when main power disappears.
0	R/W	**S5WAK_STS Clear Status (S5WAK_CLR)** If this register is set to one, all register in S5WAK_STS will be reset to zero

Register 64h~7Fh Reversed

Register 80h SMBus Status (SMB_STS)

Default Value: 00h

Access: Read/Write Clear

The following registers are all sticky bits and only can be cleared by writing a one to their corresponding fields.

Bit	Access	Description
7	R/WC	**SMBus Slave Alert (SMBALT_STS)** This bit is set when the SMBALT# is active.
6	R/WC	**HIT SLAVE Alias Address (SMBALIAS_STS)** This bit is set when the Host Slave received a Write Word from a device master and the address field match the Slave Alias Address register. If this bit is set to one, on more Write Word transaction can be received by SMBus Slave until this bit is cleared to zero.
5	R/WC	**HIT Host Slave (SMBSLAVE_STS)** This bit is set when the Host Slave received a Write Word from a device master and the address field is 10h. . If this bit is set to one, on more Write Word transaction can be received by SMBus Slave until this bit is cleared to zero.

4	R/WC	**Block Array (SMBARY_STS)** This bit is set when he SMBus Host has finished 8 bytes transition for Block Protocol. If the byte count of the Block protocol is 32, then total 4 Interrupt request will occur during the entire block transition. For the first three Interrupt, the service TRGine should program the following 8 data bytes as soon as possible, or the total transfer time may violate SMBus SPEC 1.0 (Timeout < 10ms). After the next eight bytes data are programmed to the SMB_BYTE0~7, the service TRGine should clear this status bit to initiate the following block transition.
3	R/WC	**Host Master (SMBMAS_STS)** This bit is set when the SMBus Host Master transition is complete.
2	R/WC	**SMBus Collision (SMBCOL_STS)** This bit is set when a SMBus Collision condition occurs and SMBus Host loses in the bus arbitration. The software should clear this bit and re-start SMBus operation.
1	R/WC	**Device Error (SMBERR_STS)** This bit is set when a Device Error condition occur. The Device Errors may cause by: Host asserts an unclaimed slave address/data. Host detects a Slave Timeout –may be a Slave error condition Slave detects a Master Timeout
0	RO	**SMBus Interrupt Status (SMBINTR_STS)** A one in this field indicates a SMBus interrupt is generated by any of above Interrupt source.

Register 81h SMBus Enable (SMB_EN)

Default Value: 00h

Access: Read/Write

A SMBus Interrupt can be generated if Register 81h, bit 0 is enabled and the Interrupt Status bit with associated enable bits are set to one.

Bit	Access	Description
7	R/W	**SMBus Slave Alert Interrupt Enable (SMBALT_EN)** When this bit is enabled, a SMBus Interrupt will be generated by the active SMBALERT#. 0 : Disable 1 : Enable

6	R/W	**SMBus Slave Alias Address Interrupt Enable(SMBALIAS_EN)** When this bit is enabled and the Device Address field of the Write Word Protocol received by Host Slave match the Slave Alias Address, a SMBus Interrupt will be generated. 0 : Disable 1 : Enable
5	R/W	**SMBus Slave Interrupt Enable(SMBSLAVE_EN)** When this bit is enabled and the Device Address field of the Write Word Protocol received by Host Slave is 10h, a SMBus Interrupt will be generated. 0 : Disable 1 : Enable
4	R/W	**Block Array Interrupt Enable (SMBARY_EN)** When this bit is enabled and the Host Master has finished 8 bytes transition for Block Protocol, a SMBus Interrupt will be generated. 0 : Disable 1 : Enable
3	R/W	**Host Master Interrupt Enable (SMBMAS_EN)** When this bit is enabled and the Host Master transition is complete, a SMBus Interrupt will be generated. 0 : Disable 1 : Enable
2	R/W	**SMBus Collision Interrupt Enable (SMBCOL_EN)** 0 : Disable 1 : Enable
1	R/W	**Device Error Interrupt Enable (SMBERR_EN)** 0 : Disable 1 : Enable
0	R/W	**SMBus Interrupt Enable (SMBINTR_EN)** This bit is used to enable the SMBus interrupt generation. 0 : Disable 1 : Enable

Register 82h SMBus Control (SMB_CNT)

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**Host Slave Timeout Enable (SLTO_EN)** When this bit is enabled and the Host Slave transition time is over specification, a SMBus Interrupt will be generated. 0 : Disable 1 : Enable
6	R/W	**Host Master Timeout Enable (MSTO_EN)** When this bit is enabled and the Host Master transition time is over specification, a SMBus Interrupt will be generated. 0 : Disable 1 : Enable
5	R/W	**SMBus Host Master Clock Selection (SMBCLK_SEL)** 0 : 14KHz 1 : 56KHz
4:2	RO	**Reserved**
1	R/W	**Slave Busy (SL_BUSY)** Indicate the Host Slave is in idle or active state**.** 1 : Active 0 : Idle
0	R/W	**Host Busy (HOST_BUSY)** Indicate the Host Master is in idle or active state**.** When Host Master is in IDLE state, the Host Master is free for software to control. 1 : Active 0 : Idle

Register 83h SMBus Host Control (SMBHOST_CNT)

Default Value: 00h

Access: Write Only, Read/Write

Bit	Access	Description
7:6	RO	**Reserved**

5	WO	**Kill (SMB_Kill)** This bit is set to stop all SMBus operation, including Host master and slave, all activities are set to initial state. This operation won't effect the values in R/W registers.
4	WO	**Start (SMB_START)** Writing a 1 to this bit which initiate the SMBus Host transition. The SMBus Command Protocol bits (SMB_PTL) and the associated registers should be properly programmed before this bit is set to 1. This is a write-only bit.
3	R/W	**Reserved**
2:0	R/W	**SMBus Command Protocol (SMB_PTL)** Selecting the Protocol that SMBus Host is going to execute. Reading or Writing transition is determined by SMBus Address register bit 0 (R/W bit). **Bit[3:1]** — **Protocol** 000 — Quick command 001 — Send/Receive Byte 010 — Read/Write Byte Data 011 — Read/Write Word Data 100 — Process Call 101 — Read/Write Block Data 110 — Reserved 111 — Reserved

Register 84h SMBus Address (SMB_ADDR)

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:1	R/W	**SMBus Address (SMB_ADDRESS)** The field is the slave address to target device.
0	R/W	**SMBus Read/Write (SMB_RW)** 1 : Execute a read protocol 0 : Execute a write protocol This bit doesn't effect Process Call protocol.

Register 85h SMBus Command (SMB_CMD)

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**SMBus Command (SMB_COMMAND)** This register contains the command code and will be sent to device.

Register 86h SMBus Processed Byte Count (SMB_PCOUNT)

Default Value: 00h

Access: Read Only

Bit	Access	Description
7:5	RO	**Reserved**
4:0	RO	**SMBus Processed Byte Count (SMB_PCNT)** The field is the byte count that Host has transferred for block protocol. The SMBus Interrupt TRGine can read this register to know how many bytes are not transferred yet when the SMB_CNT is over 8 bytes. A 'zero' indicates a maximum of 32 data bytes has transferred.

Register 87h SMBus Byte Count (SMB_COUNT)

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:5	RO	**Reserved**
4:0	R/W	**SMBus Byte Count(SMB_CNT)** The field is the byte count for Block Read/Write protocol. The byte count can not be 0.

Register 88h~8Fh SMBus Byte0~7 (SMB_BYTE0~7)

Default Value: 00h

Access: Read/Write

Bit	Access	Description

7:0	R/W	**SMBus Byte0~7 (SMB_BYTE0~7)** These seven bytes are the data byte field for Block Read/Write protocol. The Byte0 is also used in Byte protocol, including Received Byte, Read/Write Data Byte protocol. In addition, the Byte0 (low byte) and Byte1 (high byte) are combined as word during word protocol, including Read/Write Word, Process Call protocol.

Register 90h SMBus Device Address (SMBDEV_ADDR)

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**SMBus Device Address (SMBDEV_ADDR)** This field stores the Device Address when Host Slave received a Write Word protocol from other SMBus master.

Register 91h SMBus Device Byte0 (SMB_DB0)

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**SMBus Device Byte 0 (SMB_DB0)** This field stores the Data Low Byte when Host Slave received a Write Word protocol from other SMBus master.

Register 92h SMBus Device Byte1 (SMB_DB1)

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**SMBus Device Byte 1 (SMB_DB1)** This field stores the Data High Byte when Host Slave received a Write Word protocol from other SMBus master.

Register 93h SMBus Host Slave Alias Address (SMB_SAA)

Default Value: 00h

Access: Read/Write

Bit	Access	Description

7:1	R/W	**SMBus Host Slave Alias Address (SMB_ALIAS)** When Host Slave receives a Device Address the same as the address in these seven bits and bit 0 is '0', an interrupt will be raised if Alias Interrupt is also enabled.
0	R/W	Read as '0'. The Host Slave accepts master Write Word protocol only.

Register 94h~9Fh Reserved

16 Register Summary / Description – Automatic Power Control Summary

16.1 Automatic Power Control (APC) Registers

Address	Access	Register Name
00h	R/W	APC Register 00h
01h	R/W	APC Register 01h
02h	R/W	APC Register 02h
03h	R/W	APC Register 03h
04h	R/W	APC Register 04h
05h	R/W	APC Register 05h
06h	R/W	APC Register 06h
07h	R/W	APC Register 07h
08h	R/W	APC Register 08h
09h	R/W	Reserved

16.1.1 RTC Registers

Address	Access	Register Name
00h	R/W	Seconds
01h	R/W	Seconds Alarm
02h	R/W	Minutes
03h	R/W	Minutes Alarm
04h	R/W	Hours
05h	R/W	Hours Alarm
06h	R/W	Day of the Week
07h	R/W	Day of the Month
08h	R/W	Month
09h	R/W	Year
0Ah	R/W	Register A
0Bh	R/W	Register B (bit 3 must be set to 0)
0Ch	R/W	Register C
0Dh	R/W	Register D

7Eh	R/W	Day of the Month Alarm
7Fh	R/W	Month Alarm

16.2 APC Register

The following registers located at RTC power well. Before access to these registers, the APCRAM_EN must be set to one and EXPRAM_EN must be set to zero.

Register 00h CPU Frequency and Power Supply Resume Control

Default Value: 04h

Access: Read/Write

Bit	Access	Description
7:2	RO	**Reserved.**
1:0	R/W	**Power Supply ON/OFF State Resume Control** The value in this field determines the power supply state once the standby is suddenly off. 00 : Always Off 01 : Reversed 10 : Always On 11 : Keep previous state

Register 01h MAC and RTC Test Mode Enable

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**MAC Serial ROM Autoload Function Enable** 0 : Disable 1 : Enable
6	R/W	**MII Test Mode Enable** This bit is only for internal use. 0 : Disable 1 : Enable
5	R/W	**Reserved.** **Warning: This bit should be set to 0.**

4	R/W	**RING Input Polarity Control** 0 : Active high 1 : Active low
3	R/W	**EXTSMI#/THERM# Mux-ed function Select** 0: EXTSMI# 1: THERM#
2	R/W	**Select the frequency of the KBC** This bit controls the length of the period which the KBC drives the clock line low after transmitting a byte of data. 0: SYSCLK= 8.1Khz 1: SYSCLK1=16.2Khz
1	R/W	**Deassert CKE_S** After this bit translates to 1 from 0, a pulse would be generated to deassert CKE_S. CKE_S is used in S3 and converts the DRAM to self-refresh mode.
0	R/W	**Test Pin for KBC.** When this bit is set, the clock of KBC can be input from GPIO3. This bit is used to test the power-on function.

Register 02h Mux-ed Function Select

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**GPIO15/SMBALT# Function Select** 0: GPIO15 function select 1: SMBALT# function select
6:5	R/W	**GPIO[14:10]/KBC Function Select** 00: GPIO[14:10] Function Select 01: Reserved 10: KBC function select 11: Reserved

4:3	R/W	**GPIO8/PLED Function Select** 00: GPIO8 function select 01: Reserved 10: Reserved 11: PLED function select
2	R/W	**GPIO7/SPDIF Test Function Select** 0: GPIO7 function select 1: SPDIF test function select
1	R/W	**GPIO[6:4]/EECS, EESK, EEDI Function Select** 0: GPIO[6:4] function select 1: EESK, EEDI Function Select
0	R/W	**GPIO3/EEDO Function Select** 0: GPIO3 function select 1: EEDO function select

Register 03h Mux-ed Function Select

Default Value: 00h

Access: Read/Write

7:6	R/W	**GPIO2/LDRQ1#/OC2# Function Select** 00: GPIO2 function select 01: Reserved 10: OC2# function select 11: LDRQ1# function select
5:4	R/W	**GPIO[1:0]/OC[1:0]/PCI Master Function Select** 00: GPIO[1:0] function select 01: Reserved 10: OC[1:0] function select 11 PCI Master function select
3	R/W	**USB Test function**
2	R/W	**Keyboard ROM Data Test Function Enable** 0: Disable 1: Enable

1:0	R/W	**MII Operation Mode Select** 00: Normal mode 01: Probe mode 10: MAC test mode 11: PHY test mode

Register 04h System Power-Off Control

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:3	R/W	**Reserved**
2	R/W	**USB Plug-in/Pluck-out Wake up from S3/S4/S5** If this bit and the corresponding bit in APC6h are set, the system will be powered due to the "plug-in/pluck-out" action of the USB device.
1	R/W	**ACPI S5 Function Enable (S5OFF_EN)** 0 : Disable 1 : Enable
0	R/W	**ACPI S3 Function Enable (S3OFF_EN)** 0 : Disable 1 : Enable

Register 05h GPE Wakeup Enable

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**RTC IRQ8 Wake from S3/S4/S5 Enable (RTC_S5WAK_EN)** 0 : Disable 1 : Enable
6	R/W	**RING Wake from S3/S4/S5 Enable (RING_S5WAK_EN)** 0 : Disable 1 : Enable

5	R/W	**MACPME Wake from S3/S4/S5 Enable (MACPME_S5WAK_EN)** 0 : Disable 1 : Enable
4	R/W	**PCIPME Wake from S3/S4/S5 Enable (PCIPME_S5WAK_EN)** 0 : Disable 1 : Enable
3	R/W	**SMBALT# Wake from S3/S4/S5 Enable (SMBALT_S5WAK_EN)** 0 : Disable 1 : Enable
2	R/W	**Keyboard Password Wake from S3/S4/S5 Enable (KBPS_S5WAK_EN)** 0 : Disable 1 : Enable
1	R/W	**Keyboard Hotkey Wake from S3/S4/S5 Enable (KBHK_S5WAK_EN)** 0 : Disable 1 : Enable
0	R/W	**Keyboard 8MHz Clock Shutdown** Switch the enable bit of the KBC internal 8Mhz clock generator. 0 : Clock Running 1 : Clock Shutdown

Register 06h Audio and USB Wakeup Enable

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7	R/W	**CODEC1 Wake from S3/S4/S5 Enable (CODEC1_S5WAK_EN)** 0 : Disable 1 : Enable
6	R/W	**CODEC0 Wake from S3/S4/S5 Enable (CODEC0_S5WAK_EN)** 0 : Disable 1 : Enable

5	R/W	**AUDPME Wake from S3/S4/S5 Enable (AUDPME_S5WAK_EN)** 0 : Disable 1 : Enable
4	R/W	**Reserved**
3	R/W	**USB Port3 Wake from S3/S4/S5 Enable (USB3_S5WAK_EN)** 0 : Disable 1 : Enable
2	R/W	**USB Port2 Wake from S3/S4/S5 Enable (USB2_S5WAK_EN)** 0 : Disable 1 : Enable
1	R/W	**USB Port1 Wake from S3/S4/S5 Enable (USB1_S5WAK_EN)** 0 : Disable 1 : Enable
0	R/W	**USB Port0 Wake from S3/S4/S5 Enable (USB0_S5WAK_EN)** 0 : Disable 1 : Enable

Register 07h The Parameters of RTC Oscillator

Default Value: 00h

Access: Read/Write

The following registers are used to modulate the oscillator. The detailed description can be found in another application Note.

7:4	R/W	**Cout[3:0]** These four bits are used to modulate the oscillator capacity.
3:0	R/W	**Cin[3:0]** These four bits are used to modulate the oscillator capacity.

Register 08h The Parameters of RTC Oscillator

Default Value: 00h

Access: Read/Write

7:6	R/W	Reserved.
5:3	R/W	SR[2:0] for oscillator.

2	R/W	OSCSEL
1	R/W	OSC ATE
0	R/W	OSCPROBEN.

Register 09h

Default Value: 00h

Access: Read/Write

7:0	R/W	**Reserved.**

17 Electrical Characteristics

17.1 Absolute maximum Ratings

Table 17.1-1 Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Ambient operation temperature	0	70	^{0}C
Storage temperature	-40	125	^{0}C
Input voltage	-0.3	Vcc+0.3	V
Output voltage	-0.5	3.3	V

NOTE: Stress above these listed may cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

17.2 DC Characteristics

17.2.1 Ta=0-70^{0}C, Gnd=0V, VCC3=3.3V±5%,VCC18=1.8V±5%,,

Table 17.2-1 DC Characteristics of Host, DRAM, PCI and IDE Interface

Symbol	Parameter	Min	Max	Unit	Notes
V_{IH_TTL}	TTL Input High Voltage	2	VCC3+0.3	V	
V_{IL_TTL}	TTL Input Low Voltage	-0.3	0.8	V	
V_{IH}	RTC Input High Voltage	1.4	VCC18+0.3	V	
V_{IL}	RTC Input Low Voltage	-0.3	0.4	V	
V_{OL_TTL}	TTL Output Low Voltage		0.45	V	
I_{OH_TTL}	TTL Output High Current	-2		mA	
I_{OL_TTL}	TTL Output Low Current		3	mA	
I_{IL}	Input Leakage Current		±10	mA	

17.2.2 DC Characteristics for DAC (Analog Output Characteristics)

Table 17.2-1 Table of DC Characteristics for DAC

Description	Min	Typical	Max	Unit
Black Level	-	0	-	V
White Level	-	700	-	mV

ILE	-1.0	-	+1.0	LSB
DLE	-0.5	-	+0.5	LSB
1 LSB	-	2.734	-	mV
Iref	-	8.40	-	mA

17.2.3 Integrated RTC POWER CONSUMPTION

Table 17.2-2 RTC Power Consumption Table

RTCVDD (V)	Operation Current (μA)	Power Consumption (μW)
1.6	3.4	5.44
1.7	3.7	6.29
1.8	4.2	7.56
1.9	4.6	8.74
2.0	5.1	10.2

17.3 AC Characteristics

17.3.1 Host AC Timing

Table 17.3-1 CPU AC Timing Measurement

SIGNAL NAME	L -> H (ns)	H -> L (ns)	LOAD (pf)	AMD SPEC. OF SETUP/HOLD TIME	CLOCK SOURCE
HA[31:3]	4.910	5.660			CPUCLK(from PCI)
HD[63:0]	2.012 ~4.874	3.067 ~ 5.216			CPUCLK(from PCI)
BRDY#	2.645	3.064			CPUCLK
NA#	2.648	3.148			CPUCLK
KEN#/INV	3.105	3.575			CPUCLK
EADS#	3.355	4.075			CPUCLK
BOFF#	2.603	3.254			CPUCLK
AHOLD	2.882	3.252			CPUCLK

Table 17.3-2 Clock Skew

SiS540 CPUCLK ahead CPU CPUCLK	19 ps (Min.)	200 ps (Max.)

Note: All the timing are measured directly from the botton of CPU socket and based on HDWCLK hardware trap 1000h.

17.3.2 CACHE and TAG Signals AC Timing

Table 17.3-3 CACHE and TAG AC Timing Measurement

Signal Name		Min. (ns)	Max. (ns)	Loading (pf)	Measuring point
KOE#	H ¡ Ł	2.90	3.12		SRAM side
	L ¡ Ĥ	2.71	2.89		
CS1#	H ¡ Ł	2.93	3.56		SRAM side
	L ¡ Ĥ	2.41	3.15		
BWE#	H ¡ Ł	2.76	3.29		SRAM side
	L ¡ Ĥ	2.35	2.74		
GWE#	H ¡ Ł	2.70	3.21		SRAM side
	L ¡ Ĥ	2.14	2.80		
ADSC#	H ¡ Ł	2.80	3.39		SRAM side
	L ¡ Ĥ	2.29	2.73		
ADV#	H ¡ Ł	2.90	3.25		SRAM side
	L ¡ Ĥ	2.35	2.78		
TAGWE#	H ¡ Ł	3.58	4.04		TAG side
	L ¡ Ĥ	2.57	3.08		
	Pulse Width	8.97	9.38		
TA[7:0]	H ¡ Ł	430ps	930ps		TAG side
	L ¡ Ĥ	2.02	3.14		

Note: All the timing are based on HDWCLK hardware trap 0110h, and TAGWE# pluse width setting 1100h (T/2+6.5ns)

Table 17.3-4 Clock Skew

Clock Skew		Min. (ps)	Max. (ps)
540CCLK (Chipset Side)	CPUCLK (CPU side)	143ps	351ps
540CCLK(Chipset Side)	SRAMCLK (SRAM side)	140ps	335ps

Note: SiS540CCLK always ahead CPUCLK and SRAMCLK.

17.3.3 DRAM AC Timing

17.3.3.1 Light Loading of SDRAM

SDRAM: SEC KM 416S4030BT-GL (DS63, single-sided 32MB, 4pcs.)
FBC: None

Table 17.3-5 Signal Valid/Invalid Delay of SDRAM from SDRAM Clock

SIGNAL	CURRENT	L TO H		H TO L		CLOCK	NOTE
		min	max	min	max		
MD[63:0]	Weak	1.84	2.5	1.62	2.03	SDCLK	From post write FIFO, x-1-1-1
	Normal	1.49	1.86	1.59	1.99		
	Strong	1.59	2.42	1.73	2.21		
	Strongest	1.67	2.09	1.81	1.88		
MA[14:0]	Weak	3.78	3.97	3.92	4.28	SDCLK	Note
	Normal	3.53	3.84	3.78	4.1		
	Strong	3.59	3.78	3.61	4.23		
	Strongest	3.62	3.79	3.95	4.25		
RAMW#	Weak	3.65	3.97	4.05	4.2	SDCLK	Note
	Normal	3.58	3.88	4.03	4.2		
	Strong	3.69	3.98	4.04	4.24		
	Strongest	3.6	3.95	4	4.17		
CS#	Weak	1.96	2.08	3.88	4.17	SDCLK	
	Normal	1.47	1.64	1.84	2.29		
	Strong	1.47	1.51	1.76	1.93		
	Strongest	1.42	1.69	1.74	1.96		
DQM#	Weak	1.69	1.92	2.39	2.59	SDCLK	
	Normal	1.53	1.64	1.78	1.98		
	Strong	1.56	1.67	1.8	2.08		
	Strongest	1.52	1.63	1.85	2.03		
SDRAS#	Weak	3.89	3.98	4.08	4.23	SDCLK	Note

	Normal	3.57	3.91	3.86	4.15		
	Strong	3.67	3.91	3.93	4.09		
	Strongest	3.67	3.82	4.02	4.17		
SDCAS#	Weak	3.78	4.09	4.09	4.24	SDCLK	Note
	Normal	3.63	3.97	4.02	4.13		
	Strong	3.73	3.84	3.97	4.22		
	Strongest	3.56	3.89	4.03	4.17		

Table 17.3-6 Peak Voltage of SDRAM

SIGNAL	L TO H	H TO L	CURRENT	LOAD	NOTE
MD[63:0]	3.8	-0.48	Weak		From post write FIFO, x-1-1-1
	3.76	-0.62	Normal		
	4.18	-0.66	Strong		
	4	-0.64	Strongest		
MA[14:0]	3.5	-0.52	Weak		Note
	3.72	-0.82	Normal		
	3.88	-0.74	Strong		
	3.96	-0.74	Strongest		
RAMW#	3.52	-0.34	Weak		Note
	3.84	-0.46	Normal		
	3.86	-0.48	Strong		
	4.02	-0.48	Strongest		
CS#	3.4	0.08	Weak		
	3.48	-0.08	Normal		
	3.5	-0.46	Strong		
	3.7	-0.6	Strongest		
DQM#	3.68	0.04	Weak		
	3.58	-0.52	Normal		
	3.96	-0.9	Strong		
	4.18	-0.94	Strongest		
SDRAS#	3.42	-0.24	Weak		Note
	3.68	-0.5	Normal		
	3.8	-0.54	Strong		
	3.88	-0.58	Strongest		
SDCAS#	3.4	-0.08	Weak		Note
	3.72	-0.34	Normal		
	3.76	-0.42	Strong		

	3.96	-0.46	Strongest		

17.3.3.2 Heavy Loading of SDRAM

SDRAM: Micron MT48LC2M8A1 TG-8B (DS 76, doubled-sided 32MB, 18pcs.)
KingMax KSV884T4A1A-07 (DS 167, doubled-sided 128MB, 16pcs.)
FBC: SEC KM416S4030CT-G7 (32M, 4pcs.)

Table 17.3-7 Signal Valid/Invalid Delay of SDRAM from SDRAM Clock

SIGNAL	CURRENT	L TO H		H TO L		CLOCK	NOTE
		min	max	min	max		
MD[63:0]	Weak	3.08	4.41	2.34	2.54	SDCLK	From post write FIFO, x-1-1-1
	Normal	2.19	2.43	1.82	2.21		
	Strong	2.04	2.92	1.97	2.56		
	Strongest	1.93	3.27	1.83	2.61		
MA[14:0]	Weak	7.92	9.41	6.94	7.78	SDCLK	Note
	Normal	6.03	6.7	6.2	6.91		
	Strong	5.75	6.23	6.2	6.78		
	Strongest	5.43	6.12	6.17	6.68		
RAMW#	Weak	8.62	9.52	6.52	8.23	SDCLK	Note
	Normal	6.94	7.77	6.55	7.11		
	Strong	6.48	7.1	6.58	7.32		
	Strongest	6.56	6.97	6.91	7.21		
CS#	Weak	1.63	1.85	4.61	4.81	SDCLK	
	Normal	1.73	1.8	2.14	2.42		
	Strong	1.69	1.89	2.04	2.34		
	Strongest	1.47	1.85	1.98	2.12		
DQM#	Weak	2.6	3.02	4.44	5.34	SDCLK	
	Normal	2.09	2.58	2.86	3.16		
	Strong	1.81	2.22	2.6	2.81		
	Strongest	1.92	3	2.62	2.82		
SDRAS#	Weak	7.88	9.53	6.28	8.6	SDCLK	Note
	Normal	6.25	6.97	5.97	6.98		
	Strong	5.74	6.42	6.42	6.91		
	Strongest	6.13	6.59	6.53	6.81		
SDCAS#	Weak	7.94	9.51	6.16	8.28	SDCLK	Note
	Normal	6.25	7.23	6.35	7.1		

	Strong	5.92	6.92	6.49	6.82		
	Strongest	5.99	6.47	6.14	7.04		

Table 17.3-8 Peak Voltage of SDRAM

SIGNAL	L TO H	H TO L	CURRENT	LOAD	NOTE
MD[63:0]	3.58	-0.46	Weak		From post write FIFO, x-1-1-1
	3.62	-0.38	Normal		
	4.38	-0.72	Strong		
	4.32	-0.76	Strongest		
MA[14:0]	3.2	-0.06	Weak		Note
	3.28	-0.06	Normal		
	3.42	-0.22	Strong		
	3.36	-0.16	Strongest		
RAMW#	3.34	0	Weak		Note
	3.3	-0.04	Normal		
	3.42	-0.08	Strong		
	3.44	-0.1	Strongest		
CS#	3.4	0.28	Weak		
	3.46	-0.06	Normal		
	3.5	-0.22	Strong		
	3.46	-0.44	Strongest		
DQM#	3.48	-0.22	Weak		
	3.82	-0.32	Normal		
	3.74	-0.54	Strong		
	3.66	-0.64	Strongest		
SDRAS#	3.18	0.06	Weak		Note
	3.38	0.06	Normal		
	3.28	0.06	Strong		
	3.32	0.04	Strongest		
SDCAS#	3.32	0.04	Weak		Note
	3.4	0.06	Normal		
	3.5	-0.02	Strong		
	3.5	-0.1	Strongest		

17.3.3.3 Light Loading of FBC

SDRAM: SEC KM416S4030BT-GL (DS63, single-sided, 32MB, 4pcs.)

FBC: SEC KM416S4030CT-G7 (32M, 4pcs.)

Table 17.3-9 Signal Valid/Invalid Delay of FBC from SDRAM Clock

SIGNAL	CURRENT	L TO H		H TO L		CLOCK	NOTE
		min	max	min	max		
VMD[63:0]	Weak	4.06	4.23	3.99	4.23	SDCLK	From post write FIFO, x-1-1-1
	Normal	3.81	4.14	3.88	3.96		
	Strong	3.84	4.18	3.83	4.34		
	Strongest	3.92	4.22	4.01	4.46		
VMA[14:0]	Weak	4.59	5.38	4.96	5.34	SDCLK	Note
	Normal	4.7	5.14	4.5	4.89		
	Strong	4.27	4.61	4.11	5.71		
	Strongest	4.21	4.51	4.23	4.78		
RAMW#	Weak	5.03	5.44	4.21	4.83	SDCLK	Note
	Normal	4.07	4.99	4.02	4.9		
	Strong	4.29	5.14	3.97	4.54		
	Strongest	4.3	4.94	4.01	4.81		
VCS#	Weak	4.04	4.33	7.23	7.57	SDCLK	
	Normal	4.21	4.48	5.22	5.96		
	Strong	4.02	4.6	4.64	5.26		
	Strongest	3.93	4.23	4.56	5.01		
VDQM#	Weak	3.97	4.46	4.71	5.31	SDCLK	
	Normal	3.68	3.98	3.99	4.07		
	Strong	3.7	3.99	3.95	4.35		
	Strongest	3.7	3.85	4.02	4.38		
SDRAS#	Weak	4.84	5	4.97	5.35	SDCLK	Note
	Normal	3.8	4.83	5.11	5.44		
	Strong	4.14	4.61	4.93	5.21		
	Strongest	3.86	4.53	5.04	5.37		
SDCAS#	Weak	4.98	5.09	4.97	5.14	SDCLK	Note
	Normal	3.96	4.72	5.04	5.52		
	Strong	3.99	4.42	4.1	5.03		
	Strongest	3.58	4.04	4.7	5.06		

Table 17.3-10 Peak Voltage of FBC

SIGNAL	L TO H	H TO L	CURRENT	LOAD	NOTE
MD[63:0]	3.4	-0.48	Weak		From post write FIFO, x-1-1-1

	3.74	-0.68	Normal		
	4.04	-0.68	Strong		
	4.14	-0.68	Strongest		
MA[14:0]	3.56	-0.58	Weak		Note
	3.72	-0.92	Normal		
	4	-0.8	Strong		
	4.26	-0.92	Strongest		
RAMW#	3.52	-0.46	Weak		Note
	3.9	-0.56	Normal		
	4.26	-0.6	Strong		
	4.48	-0.74	Strongest		
CS#	3.3	0.42	Weak		
	3.26	0.08	Normal		
	3.28	-0.04	Strong		
	3.38	-0.02	Strongest		
DQM#	3.2	-0.08	Weak		
	3.36	-0.12	Normal		
	3.36	-0.08	Strong		
	3.58	-0.16	Strongest		
SDRAS#	3.44	-0.52	Weak		Note
	3.68	-0.56	Normal		
	4.06	-0.56	Strong		
	4.04	-0.6	Strongest		
SDCAS#	3.48	-0.44	Weak		Note
	3.62	-0.5	Normal		
	3.84	-0.62	Strong		
	4.14	-0.62	Strongest		

17.3.3.4 Heavy Loading of FBC

SDRAM: Micron MT48LC2M8A1 TG-8B (DS 76, doubled-sided 32MB, 18pcs.)
KingMax KSV884T4A1A-07 (DS 167, doubled-sided 128MB, 16pcs.)
FBC: SEC KM416S4030CT-G7 (32M, 4pcs.)

Table 17.3-11 Signal Valid/Invalid Delay of FBC from SDRAM Clock

SIGNAL	CURRENT	L TO H		H TO L		CLOCK	NOTE
		min	max	min	max		

VMD[63:0]	Weak	4.25	4.83	4.16	5.24	SDCLK	From post write FIFO, x-1-1-1
	Normal	3.69	4.12	3.79	4.52		
	Strong	3.81	4.2	3.97	4.23		
	Strongest	3.89	5.5	3.88	4.23		
VMA[14:0]	Weak	7.28	8.34	5.28	5.88	SDCLK	Note
	Normal	5.54	6.26	5.81	6.15		
	Strong	5.38	6.23	5.62	6.35		
	Strongest	5.47	5.81	5.61	5.93		
RAMW#	Weak	8.22	8.96	5.32	7.77	SDCLK	Note
	Normal	5.79	6.71	5.94	6.43		
	Strong	5.41	7.1	5.53	6.36		
	Strongest	5.52	6.48	5.34	6.27		
VCS#	Weak	4.16	4.43	7.23	7.8	SDCLK	
	Normal	4.09	4.48	5.41	5.79		
	Strong	4.02	4.43	4.78	5.26		
	Strongest	4.1	4.34	4.86	5.68		
VDQM#	Weak	4.04	4.45	4.79	4.96	SDCLK	
	Normal	3.87	4.34	3.96	4.44		
	Strong	3.8	4.11	3.98	4.36		
	Strongest	3.91	4.12	3.93	4.17		
SDRAS#	Weak	6.54	9.78	6.27	7.42	SDCLK	Note
	Normal	5.24	6.15	6.07	7.09		
	Strong	5.32	5.69	5.92	6.65		
	Strongest	5.17	5.76	6.41	6.97		
SDCAS#	Weak	7.2	10.3	6.73	7.06	SDCLK	Note
	Normal	5.36	6.01	5.73	6.39		
	Strong	5.2	5.54	5.85	6.11		
	Strongest	5.09	5.58	5.78	6.05		

Table 17.3-12 Peak Voltage of FBC

SIGNAL	L TO H	H TO L	CURRENT	LOAD	NOTE
MD[63:0]	3.52	-0.52	Weak		From post write FIFO, x-1-1-1
	3.96	-0.76	Normal		
	3.98	-0.66	Strong		
	4.1	-0.72	Strongest		
MA[14:0]	3.2	-0.26	Weak		Note

	3.18	-0.34	Normal		
	3.3	-0.52	Strong		
	3.6	-0.34	Strongest		
RAMW#	3.24	-0.14	Weak		Note
	3.4	-0.28	Normal		
	3.36	-0.38	Strong		
	3.44	-0.38	Strongest		
CS#	3.28	0.5	Weak		
	3.28	0.12	Normal		
	3.38	0	Strong		
	3.32	-0.04	Strongest		
DQM#	3.24	-0.06	Weak		
	3.48	0	Normal		
	3.38	-0.16	Strong		
	3.42	-0.28	Strongest		
SDRAS#	3.1	0.08	Weak		Note
	3.1	-0.14	Normal		
	3.38	-0.08	Strong		
	3.34	-0.12	Strongest		
SDCAS#	3.12	0.06	Weak		Note
	3.44	-0.04	Normal		
	3.42	-0.22	Strong		
	3.56	-0.12	Strongest		

Note:

1. The propagation delay margin for these signals is at least 2 memory clocks.
2. The timing and loading are measured from DRAM chip directly.
3. The timing is measured from 1.4V of clock of DRAM to 1.4V of tested signal.
4. These signals are controlled by Register 8Ch, 8Dh, 8Fh.
   The setting for Register 8Fh is 4ah in this case.
   The setting for Register 8Dh is 84h in this case.
   The setting for Register 8Ch is 44h in this case.
5. The clock skew between SDCLK0 ~ SDCLK11 of DRAM chip and SDCLK of SiS540 is around 0.1 ~ 0.428ns. The SDCLK of SiS540 is leading all clocks of DRAM.
6. The clock skew between SDCLK of FBC chip and SDCLK of SiS540 is around 0.496~0.668ns. The SDCLK of SiS540 is leading the clock of FBC.
7. The unit of L to H or H to L delay time is ns.
8. The unit of peak voltage is V.

17.3.4 PCI Signals AC Timing

17.3.4.1 Light Loading

No PCI card plugged except when measuring PGNT # (Seagate ST51080N SCSI HD and AHA-2940 SCSI card is used)

Table 17.3-13 PCI Signals AC Timing

SIGNAL NAME	Low		High		LOADING	CLOCK SOURCE	NOTE
	min(ns)	max(ns)	min(ns)	max(ns)	Pf		
PCIRST#	7.71	8.23	13.21	20.75		PCICLK	
AD[31:0]	6.27	7.00	6.23	7.01		PCICLK	
C/BE[3:0]#	6.08	6.70	5.72	6.33		PCICLK	
FRAME#	5.76	6.41	7.67	8.38		PCICLK	
IRDY#	4.99	5.73	7.15	7.87		PCICLK	
LOCK#	5.24	5.53	5.36	5.78		PCICLK	
PAR	5.72	6.47	6.36	7.06		PCICLK	
TRDY#	5.53	6.22	6.20	6.91		PCICLK	
STOP#	6.12	6.82	5.92	6.57		PCICLK	
DEVSEL#	5.69	6.43	5.97	6.80		PCICLK	
PGNT#	4.43	5.21	4.20	5.09		PCICLK	

17.3.4.2 Heavy Loading

Slot 0: Bt848KPF Video Decoder

Slot 1: AHA-2940 SCSI card

Table 17.3-14 PCI Signals AC Timing

SIGNAL NAME	Low		High		LOADING	CLOCK SOURCE	NOTE
	min(ns)	max(ns)	min(ns)	max(ns)	pf		
PCIRST#	8.80	9.93	17.55	28.63		PCICLK	
AD[31:0]	6.48	7.27	6.74	7.56		PCICLK	
C/BE[3:0]#	6.55	7.34	6.15	6.94		PCICLK	
FRAME#	6.54	7.30	8.50	8.90		PCICLK	
IRDY#	5.67	6.57	7.88	8.98		PCICLK	
LOCK#	5.31	5.66	5.41	5.92		PCICLK	
PAR	5.61	6.60	5.88	6.66		PCICLK	
TRDY#	5.47	6.17	6.10	7.01		PCICLK	
STOP#	6.04	6.87	6.20	7.13		PCICLK	

DEVSEL#	5.77	6.33	6.94	7.69		PCICLK	
PGNT#	4.43	5.08	4.45	5.38		PCICLK	

Table 17.3-15 Clock Skew

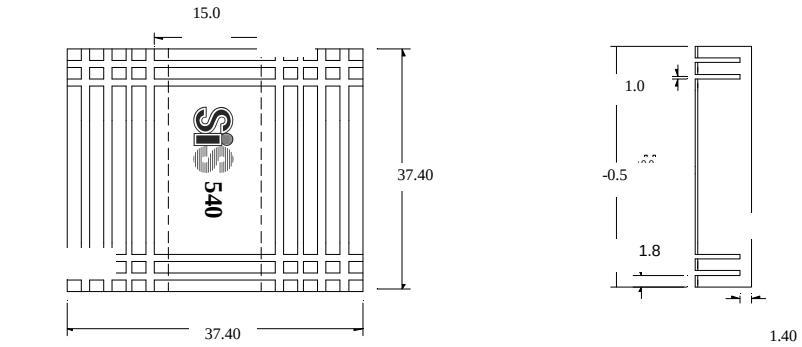
Clock Skew		Min. (ps)	Max. (ps)
540PCLK (Chipset Side)	PCICLK (PCI slot side)	355	700

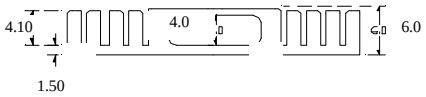
Note: 540PCLK lags PCICLK.

18 Heat Sink Dimension and Topside Mark

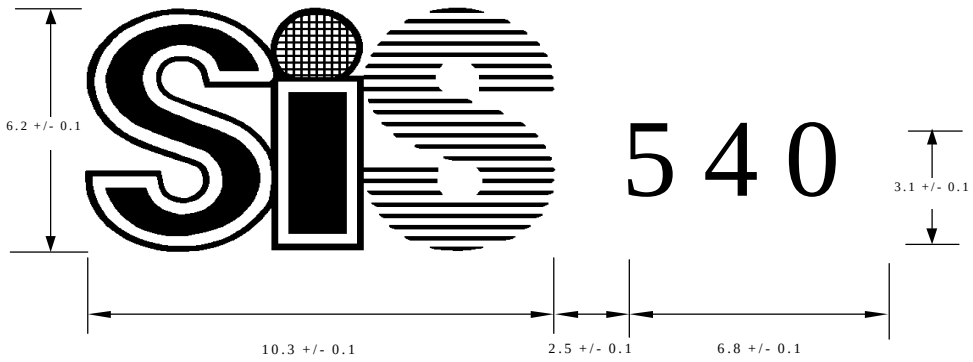
SiS 540 Heat Sink Outline Dimension

Thermal Tape Dimension: 27mm (Length), 27mm (Width)
Thermal Tape Material: SEKISUI #5760

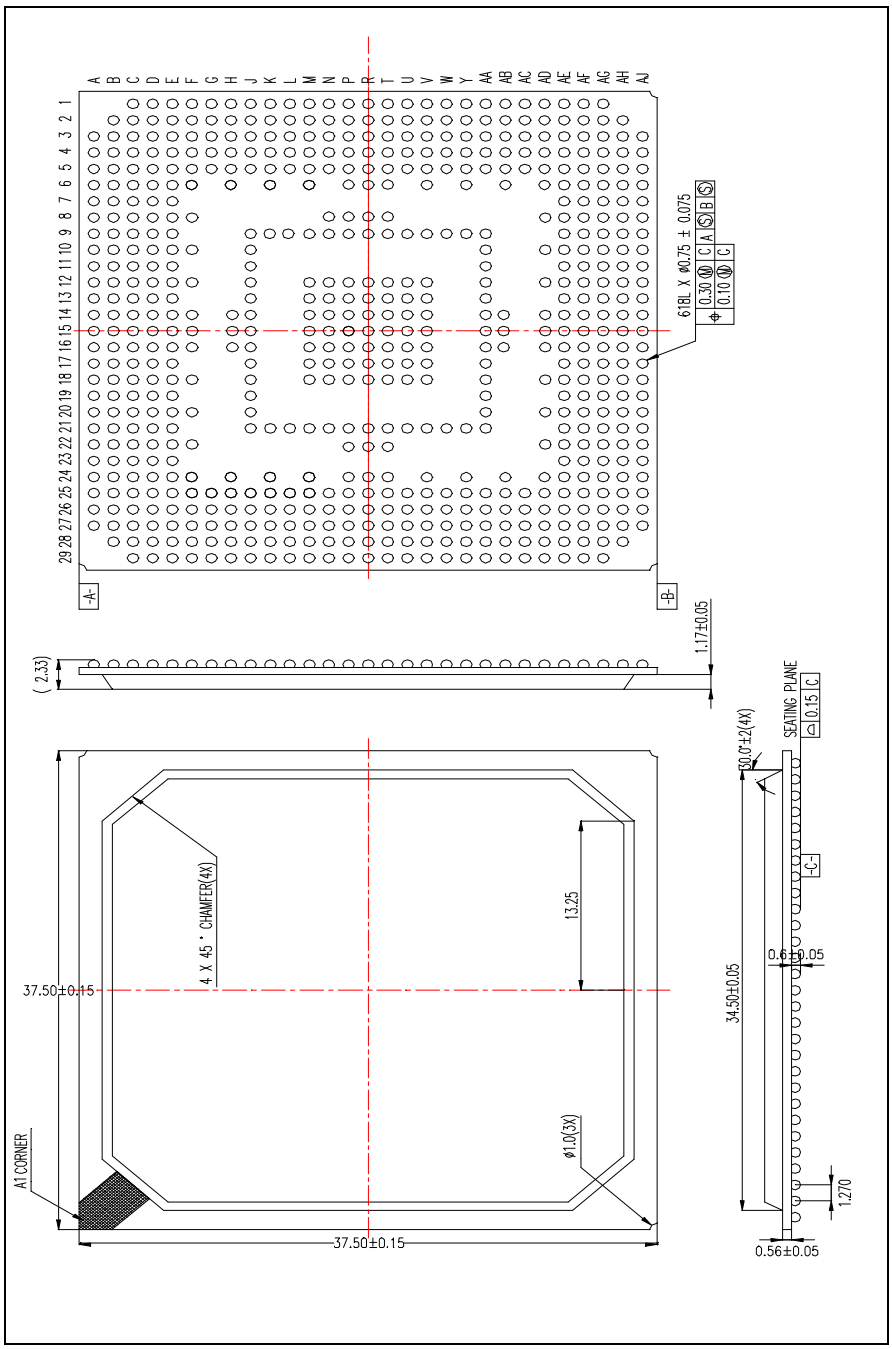




TOLERANCE			
* *	** *	Angular	
+/- 0.15	+/- 0.3	+/- 1°	
SCALE	1:1	FINISH	GREEN
Unit	mm		


6.2 +/- 0.1
540
3.1 +/- 0.1
10.3 +/- 0.1
2.5 +/- 0.1
6.8 +/- 0.1

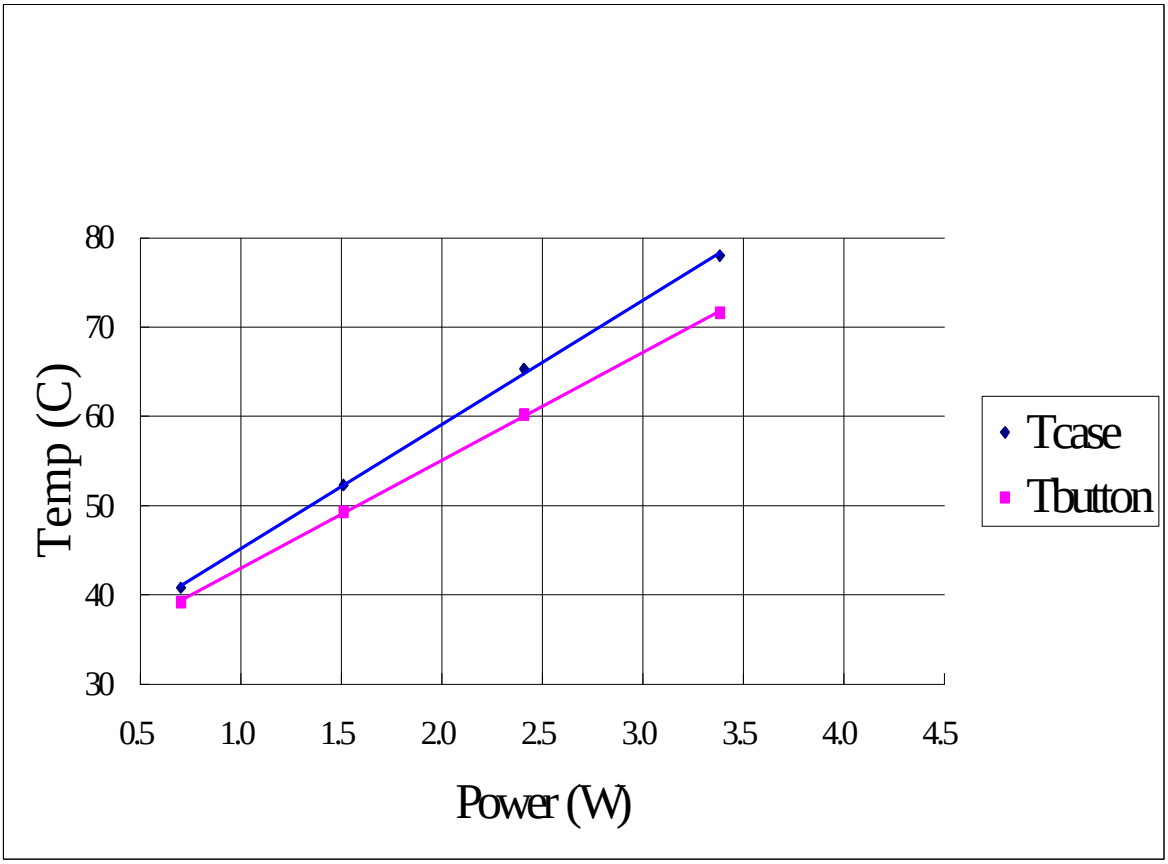
19 Mechanical Dimension



20 THERMAL ANALYSIS

20.1 CHIP THERMAL ANALYSIS WITHOUT HEATSINK

Condition : Room Temperature 32°C (Still air)



Theda ja= 18.4 °C/W

Maximum Power Dissipation = 3.3W

Tcase : Temperature at the of molding compound Surface

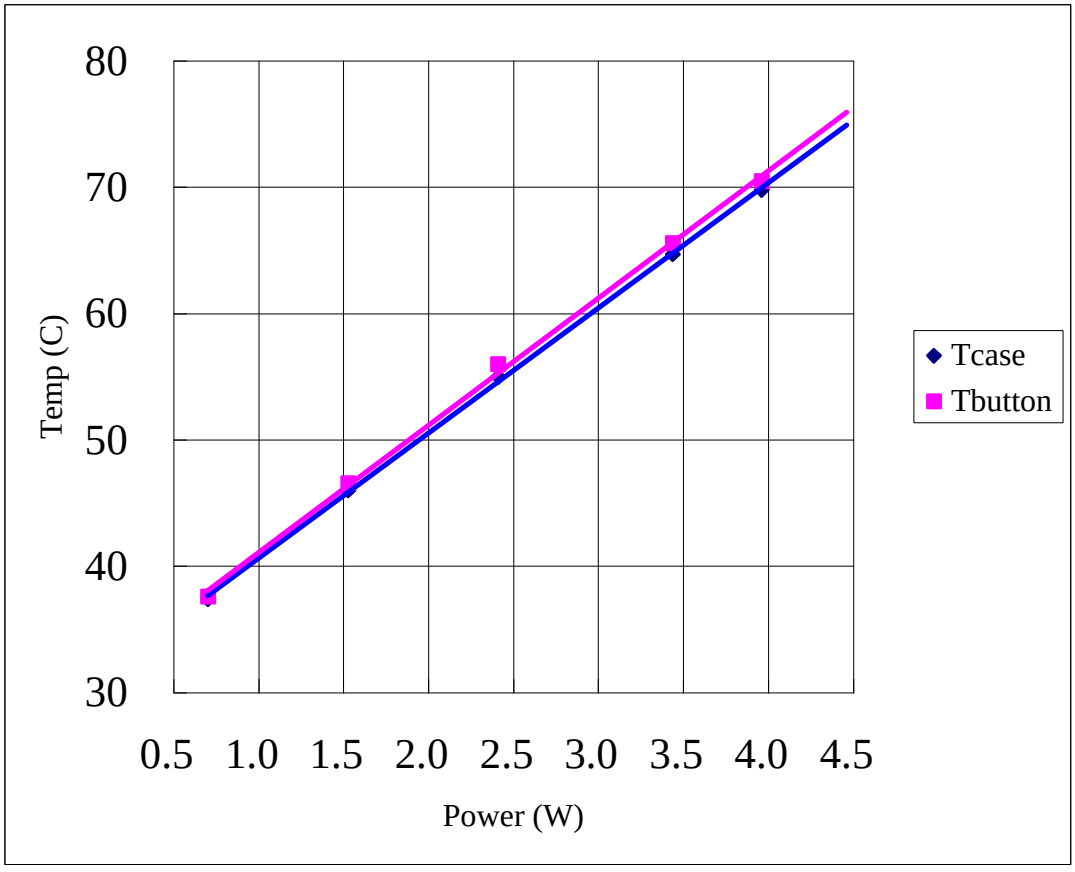
Tbutton : Temperature at the back side of PCB where thermal balls are directly attached

20.2 CHIP THERMAL ANALYSIS WITH HEATSINK

Condition : Room Temperature 32°C (Still air)

With 38mm*38mm Aluminum Heat Sink

Theda ja= 14.0°C/W



Maximum Power Dissipation = 4.3W

Tcase : Temperature at the of molding compound Surface

Tbutton : Temperature at the back side of PCB where thermal balls are directly attached

21 Appendix:

21.1 ACPI Power State

21.1.1 Global System State Definitions

Global system states apply to the entire system and are visible to user. Global system states can be easily defined by the power state of the computer

	G0	G1	G2	G3
VDD3	On	On/Off	Off	Off
AUXVDD	On	On	On	Off

Following is a list of the global states:

G0 – Working:

A computer state where the computer executes the user's applications. In this state, devices are dynamically having their power states changed. The user will be able to select various performance/power characteristics of the system.

G1 – Sleeping:

A computer state where the computer consumes a small amount of power. The user's applications are not being executed, and the system appears to be off. Work can be resumed without rebooting the OS because the context of the system is saved by the hardware.

G2 – Soft off:

A computer state where the computer consumes a minimal amount of power. No user application or system code is run. The system must be restarted to return to the Working state. The system's context will not be preserved by the hardware.

G3 – Mechanical off:

A computer state where the computer only consumes RTC power. This state is entered and left by a mechanical means (e.g. turning off the system's power through unplugging the power cord). No hardware context is retained by hardware and the OS must be restarted to return to the Working state. Only in this state can the hardware be disassembled safely.

21.1.2 Device Power State Definitions

Device power states are states of particular devices and they are generally not visible to the users. For example, some devices may be in the Off state even though the system as a whole is in the Working state. Note that the hardware and software behavior of Device State is not defined in ACPI spec.

Device State	Power Consumption	Device Context Retained	Driver Restoration
D0	As need for operation	All	None
D1	<D0	>D2	<D2
D2	<D1	>D3 Hot	<D3
D3 Hot	<D2	None	Full init and load
D3 Cold	0	None	Full init and load

D0 – Fully on:

The device is completely active and responsive in this state.

D1/D2:

The meaning of D1/D2 Device State is defined by each class of device. In general, D2 is expected to save more power and preserve less device context than D1.

D3 – (Hot/Cold) Off:

The device context is lost when this state is entered. OS must reinitialize the device when it back to D0. In general, Power and Clock have been fully removed from the device when the device is in D3 Cold Off. When the device enters D3 Hot state, Power and Clock may be removed from the device. All classes of devices define this state.

21.1.3 Sleeping State Definitions

Sleeping states (Sx states) are types of sleeping states within the golbal sleeping state, G1. The Sx states are briefly defined as following.

S0/G0 – Working State:

The S0 state is the same as the gobal state, G0. All system context are retained by hardware continuously. All Processor and Device States can only be changed dynamically when system is in this state.

S1/G1 – Sleeping State:

The S1 sleeping state is a low wake-up latency. In this state, no system context is lost.

S2/G1 – Sleeping State:

This state is similar to the S1 sleeping state except the CPU and system cache context is lost.

S3/G1 – Suspend to Ram (STR) State:

The S3 sleeping state is a low wake-up latency sleeping state where all system context is lost except system memory.

S4/G1 – Suspend to Disk (STD) State:

The S4 sleeping state is the lowest power, longest wake-up latency sleeping state supported by ACPI. In order to reduce power to a minimum, the hardware platform has powered off all devices. Platform context is maintained in Hard Disk.

S5/G2 – Soft Off State:

The S5 state is similar to the S4 state except the OS does not save any context nor enable any devices th wake the system. The system is in the soft off state and requires a complete boot when awakened.

21.1.4 Processor Power State Definitions

Processor power states (Cx) are processor power consumption and thermal management states within the global working state, G0.

C0 Processor Power State:

While the processor is in this state, it executes instructions with full/throttling rate.

C1 Processor Power State:

The processor is in a low power state where it is able to maintain the context of the system caches. This state is supported through a native instruction of the processor (HLT for IA-PC), and assumes no hardware support is needed from the chipset.

C2/C3 Processor Power State:

The processor is in a low power state where it is able to maintain the context of the system caches. This state is supported through chipset hardware.

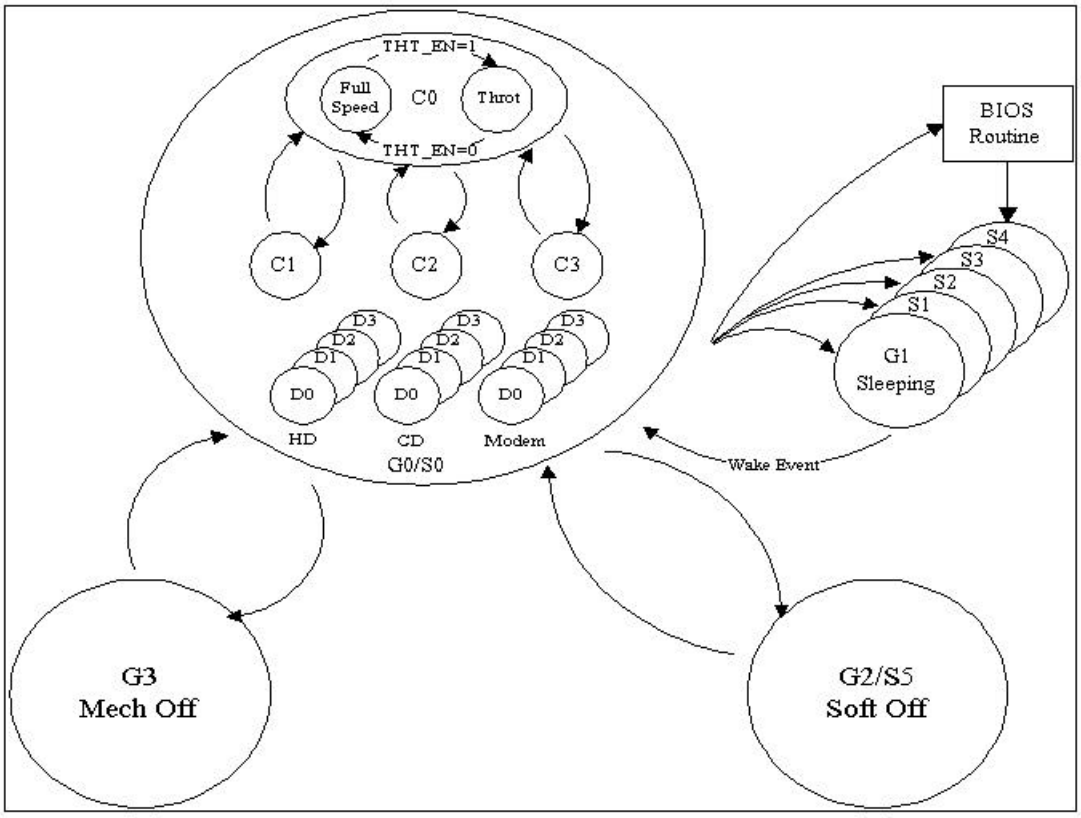


Figure 21.1-1 ACPI Model

21.2 The Hardware Event of ACPI

The ACPI architecture defines mechanisms for hardware to generate events and control logic to sequence the platform between the various global system states. Events are used to notify the OS that some action is needed, and control logic is used by the OS to cause some state transition. ACPI-defined events are "hardware" or "interrupt" events. A hardware event is one that causes the hardware to unconditionally perform some operation. An interrupt event causes the execution of an event handler, which allows the software to make a policy decision based on the event. For example, the AUDPME Event (hardware event) will sequence the system from a sleeping state (S1/S2/S3/S4) to the S0 working. After waking from the sleeping state, an interrupt event will be triggered and the ACPI driver will schedule the execution of an OEM-supplied AML handler associated with the event.

For legacy systems (APM mode under WIN95/98), an event normally generates an OS-transparent interrupt (this means that OS won't aware the existence of the interrupt), such as a System Management Interrupt (SMI#). All power management event are handle by the SMI# handler which is provided by the system BIOS. For ACPI systems the interrupt events need to generate an OS-visible interrupt that is shareable (SCI). Figure 21.2-1 shows the hardware model for ACPI fix feature. Figure 21.2-2 and Figure 21.2-3 show the

hardware model of ACPI feature.

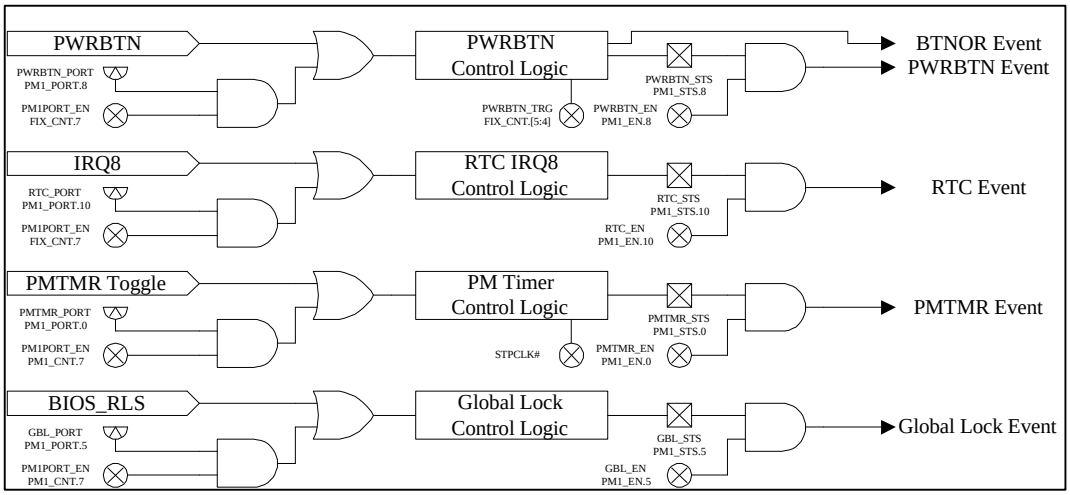


Figure 21.2-1 Hardware Model for Fix Feature

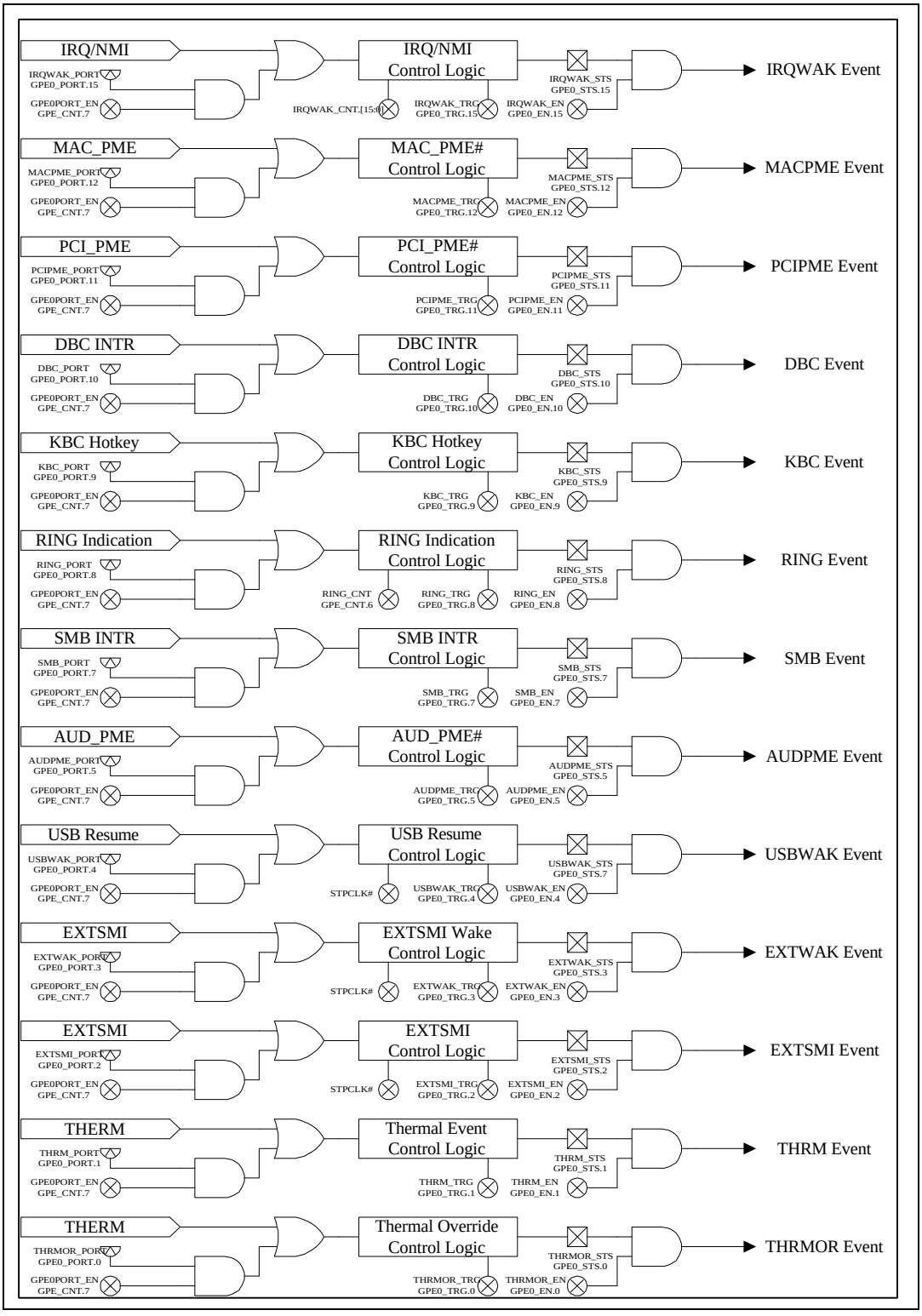


Figure 21.2-2 Hardware Model for Generic Fixture 0 (GPE0)

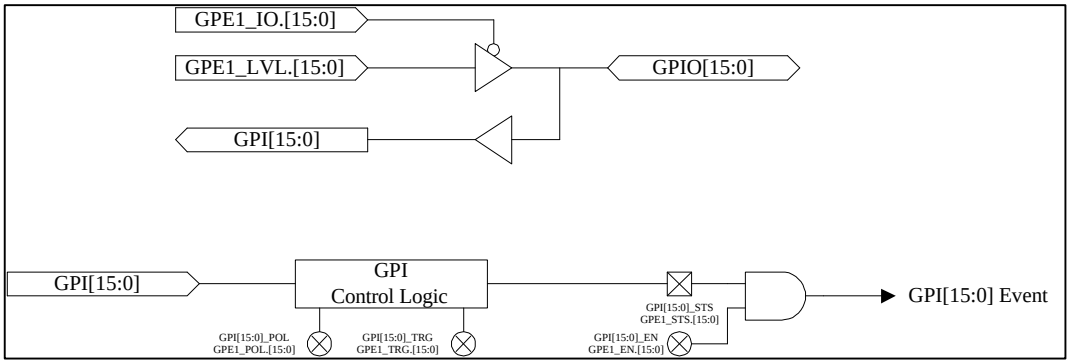


Figure 21.2-3 Hardware Model for Generic Feature 1 (GPE1)

21.3 The Interrupt Event of ACPI

Hardware platforms that want to support both legacy operating system and ACPI systems must provide a way of re-mapping the interrupt events between SMIs and SCIs when switching between ACPI and legacy models. This is illustrated in Figure 21.3-1.

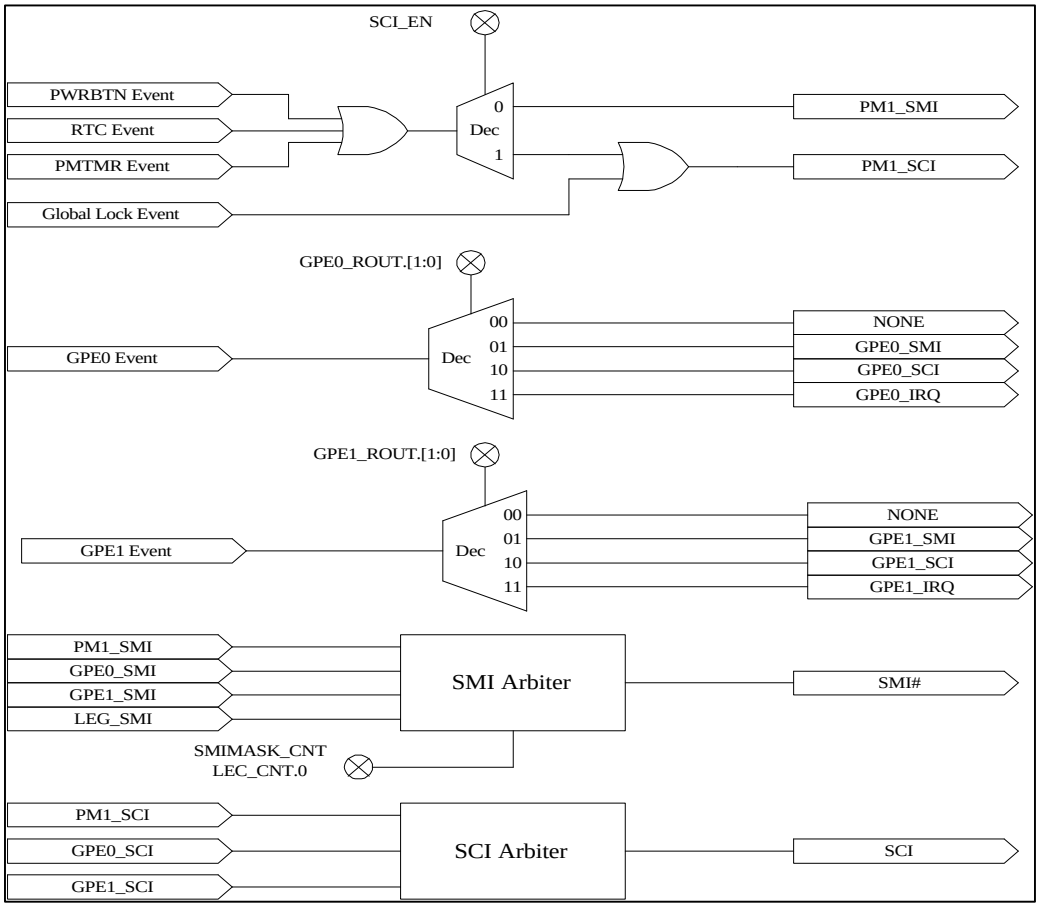


Figure 21.3-1 Interrupt Model for ACPI

21.4 The Sleeping/Wake Event of ACPI

The sleeping/wake logic consists of logic that will sequence the system into the defined low-power hardware sleeping state and will awaken the system back to the working state upon a wake event. While in any of the sleeping state, an enabled "Wake" event will cause the hardware to sequence the system back to the working state and WAK_STS will be set. When waking from the S1 sleeping state, execution control is passed backed to the ACPI driver immediately, whereas when waking from S2-S5 states execution control is passed to the BIOS software. The WAK_STS bit provides a mechanism to separate the ACPI driver's sleeping and waking code during an S1 sequence. Figure 21.4-1 shows the Sleeping/Wake model for ACPI.

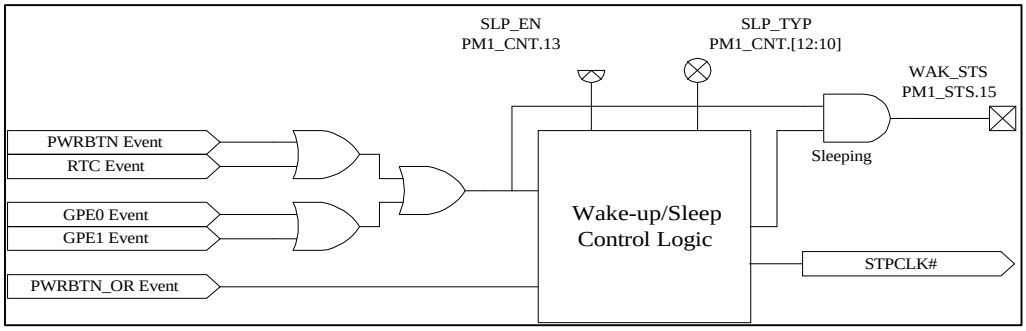


Figure 21.4-1 Sleeping/Wake model for ACPI

21.5 Types of ACPI Events

At the direct ACPI hardware level, two types of events can be signaled by an SCI interrupt:

- Fixed ACPI events
- General-purpose events

21.5.1 Fixed ACPI Events Handling

When the ACPI driver receives a fixed ACPE event, it directly handles the event by itself. The ACPI driver owns all the fixed resource registers, these registers are not manipulated by ASL/AML code. Registers must can be accessed by byte granularity.

21.5.2 General-purpose Events Handling

When the ACPI driver receives a general-purpose event, it either passes control to an ACPI-aware driver (such as PCI bus driver), or uses an OEM-supplied control method to handle the event. **The ACPI driver manages the bits in the GPEx blocks directly**, although the source to those events is not directly known and is connected into the system by control methods. When the ACPI driver receives a general-purpose event, the ACPI driver does the following:

1. Disables the interrupt source (GPEx_EN).
2. If an edge event, clears the status bit.
3. Performs one of the following:

- Dispatches to an ACPI-aware device driver.
- Queues the matching control method for execution
- Manages a wake event using device _PRW objects

4. If a level event, clears the status bits.
5. Enables the interrupt source.

The OEM AML code can perform OEM-specific functions custom to each event the particular platform might generate by executing the control method that matches the event. For GPE events, the ACPI driver will execute the control method of the name _GPE._Txx.

21.6 Examples

To illustrate how these OS native drivers interact in ACPI, consider an integrate modem and a PCI network add-on card. The power states of these two devices are defined as follows:

Integrate Modem:

- D0

Modem controller on

Phone interface on

Speaker on

Can be on hook or off hook

Can be waiting for answer

- D3

Modem controller off (context lost)

Phone interface in low power mode

Speaker off

On hook

- Power Policy for the modem

D0 to D3: Modem put in answer mode

D3 to D0: Application requests dial or the phone rings while the modem is in answer mode

PCI network add-on card

- D0

MAC fully on

PHY fully on

- D3

MAC transmit logic off (context lost)

PHY fully on

- Power Policy for the PCI network add-on card

D0 to D3: Application put MAC in low power mode

D3 to D0: Application request MAC back to normal operation mode or MAC receive an wake up event

21.6.1 Hardware Model of Integrate Modem and PCI Network Card

When a PCI function want to request a change of its power consumption state, it asserts PME#. Typically, a device uses a PME# to request a change from a power savings state to the fully operational state. The PME# is tied GPE11 directly. Each device on PCI Bus must provide its second-level status and enable bit which is defined in PCI PMCSR. The OS enables or disables the PME# wake function by enabling or disabling its corresponding GPE11 and by executing its _PSW control method which is used to take care of the second-level enable bits. When the GPE11 is asserted, the OS still executes the corresponding GPE11 control method that determines which device wakes are asserted and notifies the corresponding device objects. The native OS driver is then notified that its device has asserted wake, for which the driver powers on its device to service it.

When an embedded controller (integrate modem in this case) want to change its power state, it can assert its own power management event which ties to GPE5 directly. The OS will follow the same step as PME# which describe above.

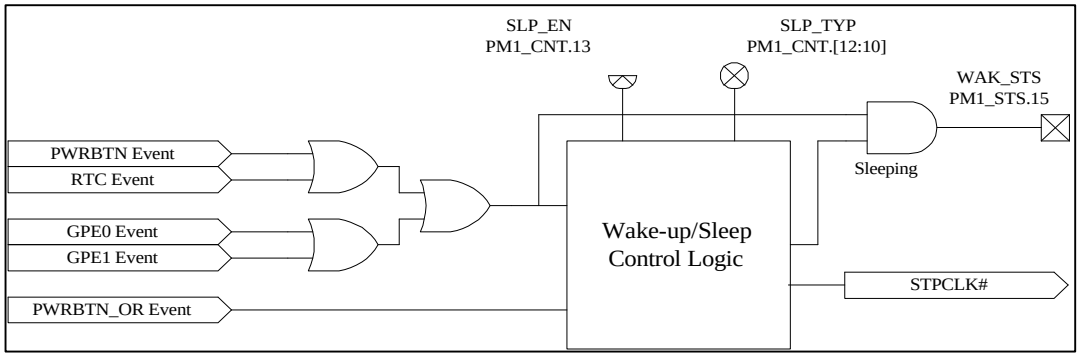


Figure 21.6-1 Hardware Model for PME#

21.6.2 The System Enter S1 Sleeping State

On a transition of the system from S0 state to S1 state, the following occurs:

1. The OS decides to place the system into the sleeping state.
2. The OS examines all devices who are enabled to wake up the system and determines the deepest possible sleeping state the system can enter to support the enabled wakeup functions. The _PRW named object under each device is examined, as well as the power resource object it points to.
3. The OS executes the Prepare to Sleep (_PTS) control method, passing an argument that indicate desired sleeping state (S1 in this case).
4. The OS places all device drivers into their respective Dx state. If the device is enabled for wakeup, it enters the Dx state associated with the wakeup capability. If the device is not enabled to wakeup the system, it enters the D3 state. In this case, the integrate modem

and the PCI network card are capable of waking the system from D3, these two devices will be placed in D3 by their own driver.

5. OS saves the processor's context to memory.
6. OS writes the waking vector into the FACS table in memory.
7. OS clears the WAK_STS in the PM1_STS.
8. OS writes SLP_TYP as "001", then set SLP_EN in PM1_CNT.
9. The system enters the S1 sleeping state.

The IA processor that supports the S1 state through the assertion of the STPCLK# signal. In this case, the system clocks (CPU and PCI) are still running and no power sources are switched off.

21.6.3 The System Exit S1 Sleeping State

When the integrate modem or PCI network card receives its wakeup event and signals its wake signal, the GPE status bit used to track that device is set. Following shows the procedure for a GPE event to sequence the system back to S0.

1. While the corresponding general-purpose enable bit is enabled, the SCI interrupt is asserted.
2. Because the system is sleeping, this will cause the hardware to transition the system into the S0 state and WAK_STS will be set.
3. Once the system is running, ACPI will disable the GPE_EN and dispatch the corresponding GPE handler. In this case, because the integrate modem and PCI network card are all PCI devices, ACPI driver will dispatch PCI bus driver to handle these two events.
4. The PCI bus driver needs to determine which device object has signaled wake, disabled the second level power management event (MDM_EN or LAN_EN), and performs a wake Notify operation on the corresponding device object that have asserted wake. Before PCI bus driver return control to ACPI driver, it must clear the status bit (MDM_STS or LAN_STS) which assert the wake event and enable the power management again (MDM_EN or LAN_EN).
5. In turn the OS will notify the OS native driver(s) for each device that will wake its device to service it. **Note that all devices must be placed in D0 when the system is sequenced to S0 from sleeping state (S1-S5).**

21.6.4 The Integrate Modem enters D3/S0 State

Following shows the procedure when the application decides to place the integrate modem in answer mode (D3 state):

1. The modem driver must send the command to enable the wakeup function of Modem or Network card.

2. The PCI bus driver receive the command from modem driver and decide to enable MDM_EN bit in modem PMCSR register. Then the bus driver calls the ACPI driver to enable the wakeup function of the integrate modem.
3. ACPI driver will run PCI's PSW object and enable the GPE5 event (GPE5_EN).
4. The modem sends the command to put the device in D3 state, and the mini-driver must save all registers of the modem controller.
5. Then PCI driver must set D3 bit in modem's PMCSR register and call ACPI driver.
6. If the integrate modem contain _PS3 and _PW3 under its name space, the ACPI driver will execute them.

21.6.5 The PCI LAN Card enters D3/S0 State

When the LAN driver decides to put the LAN card into D3 state, it takes the same procedure as the integrate modem. Except that it won't contain any object under its name space (_PSx, PWx). The LAN driver must execute all command to put the LAN device into D3 state. The ACPI driver only enable the GPE11_EN and monitor the power state of the system to decide whether the system must enter sleeping state or not.

21.6.6 When The Modem Detects Phone Call

If the integrate modem detects a phone call when it is in answer mode (D3 state), it must take the following procedure to wake the modem controller.

1. The wakeup event detection logic sets MDM_STS, and GPE5_STS will be set by this wakeup event.
2. While GPE5 event asserts, the SCI will be triggered by this event and ACPI driver will handle this general-purpose event.
3. The ACPI driver finds the source of the general-purpose event and disable this event (GPE5_EN). Then ACPI driver dispatches the PCI bus driver.
4. PCI bus driver polls all PMCSR registers on PCI bus and find that the modem asserts the wakeup event. The bus driver clears MDM_EN and calls the modem driver.
5. The modem driver clears MDM_STS and sends command to put the modem controller in D0.
6. The PCI bus driver then set D0 bit in the modem's PMCSR and call the modem driver to service the phone call.

21.6.7 When The PCI LAN Card Detects a Wakeup Event

When the PCI LAN Card detects a wakeup event, it will set LAN_STS and assert PME#. The GPE11 event will be triggered and the ACPI driver will take the same action to service the general-purpose event.

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