Avance Logic, Inc.

ALG2564
Full-Motion Video Plus 64-bit Graphics
Design Manual

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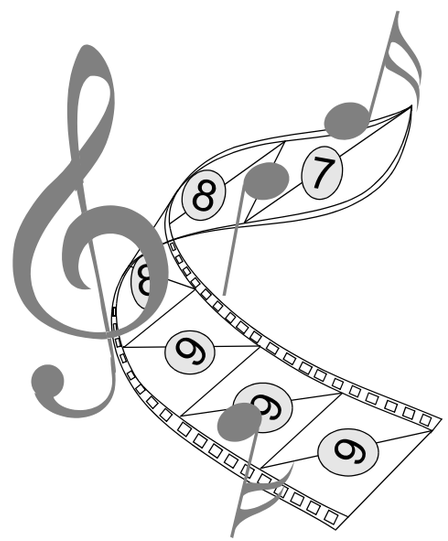

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Document Change History

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Documentation Conventions

The following defines the typographical conventions used throughout this manual.

Hexadecimal Numbers

Hexadecimal numbers are always followed by an “h” (e.g. 4Ah or 2000h).

Binary Numbers

Binary numbers are always followed by a “b” (e.g. 0101 0001b or 11b).

Decimal Numbers

Decimal numbers are followed by a “d” when it is required for clarity (e.g. 12d).

Signal Names

All signal names represent the active state of the signal. When a signal name is preceded by a minus (-) sign, the signal is active at a logic low level. When a signal name is preceded by no sign or a plus (+) sign, the signal is active at a logic high level.

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Chapter 1

Product Description

Introduction

The ALG2564 is a highly advanced graphics and video processor that contains a fully integrated RAMDAC and clock and provides 64-bit performance. The ALG2564 combines a 64-bit pipelined graphics coprocessor with full-motion video support through color space conversion and scaling. Building on the highly successful VideoWizard™ technology, the ALG2564 moves beyond 32-bit graphics with video to 64-bit graphics with video. The ALG2564 offers features previously found only in more expensive mid-range products.

Entry level multimedia systems require more than just graphics, sound, and a CD-ROM to be a successful consumer product. This new breed of computer needs to combine multiple technologies into an affordable package. Software MPEG is the technology of choice for entry-level systems while consumers demand high performance graphics and 30 fps full-motion video playback.

For additional cost savings, system designers can take advantage of the ALG2564's Unified Memory Architecture support that allows the graphics frame buffer to share system memory.

Built-in Video Acceleration

The ALG2564 includes an advanced form of video acceleration consisting of color space conversion and scaling. Color space conversion converts YUV to RGB data and is required for software MPEG and AVI playback applications. The technology used in the ALG2564 allows true-color video in 1024 x 768 resolutions with only one megabyte of DRAM compared to the up to four megabytes of DRAM required by competing products.

To play up to 30 fps in full screen, the ALG2564 uses an advanced XY scaling technology. This scaling technology allows images to be scaled to full screen with no performance degradation while being displayed in true-color.

Highly Integrated Design

The ALG2564 is a single chip graphics and video device that achieves levels of integration not achieved in the past. Using .5 micron full-custom technology, the ALG2564 contains a graphics coprocessor, video functions, 32-bit RAMDAC, dual programmable clock, in a single 208-pin package. A complete graphics and video subsystem can be assembled with only three components: an ALG2564, and two 256k x 16 DRAM devices.

Unified Memory Architecture (UMA) Support

The ALG2564 supports the VESA UMA standard for graphics. Systems that support UMA utilize a portion of the system main memory for their frame buffer storage. This reduces the cost by eliminating the need for a separate graphics memory subsystem.

Window 95 Plug and Play

Using a Windows 95 system along with a DDC compatible monitor assures complete plug and play operation. The ALG2564 automatically detects the monitor type and sets the maximum refresh rate allowed ensuring the user of a flicker free display and simplifies integration of the graphics subsystem.

Features

Feature	Benefit
Video Features	
Integrated video	MPEG and AVI acceleration
XY Zoom	Higher frame rate, full screen
Color space conversion	YUV to RGB color conversion
30 fps full screen video	Interactive multimedia/MPEG at full size
True-color at 1 MB	Best possible viewing experience and cost savings
Graphics Features	
1-2 MB DRAM support	Multiple entry points in performance
64-bit pipelined graphics coprocessor	Highest DRAM performance possible
Accelerated coprocessor	Fast business and home graphics
Integrated RAMDAC	Lower implementation cost
Integrated clock	Fewer external components
Direct draw acceleration	Faster game processing/frame rates
System Features	
UMA support	Money savings through system memory use
PCI bus interface	Best possible video and graphics throughput
DDC 1 and 2 support	Monitor autodetect
Green PC support	Meets EPA guidelines

Technical Specifications

Resolution	Colors	Vertical Refresh Rate	Mode	Memory
1600 x 1200	256	43	Interlaced	2 MB
1280 x 1024	256	75	Non-interlaced	2 MB
1024 x 768	64k	100	Non-interlaced	2 MB
800 x 600	16.7M	100	Non-interlaced	2 MB
1024 x 768	256	100	Non-interlaced	1 MB
800 x 600	256	120	Non-interlaced	1 MB
800 x 600	64k	120	Non-interlaced	1 MB
640 x 480	16.7M	120	Non-interlaced	1 MB
640 x 480	64k	120	Non-interlaced	1 MB
640 x 480	256	120	Non-interlaced	1 MB

Operating System/Application Drivers

- Windows 3.1
- Windows 95
- Windows NT 3.51
- OS/2 2.1
- OS/2 Warp

- Xing MPEG Decoder
- Mediamatics MPEG Decoder
- Compcore Softpeg
- Indeo
- CinePak
- Quicktime

- AutoCAD ADI 4.0, 4.1
- AutoCAD Display List

- VESA BIOS Extensions

Green PC Support

Supports EPA Green PC including:

- On (full power, 3.5 - 4 watts)
- Standby (half power, 1.75 - 2 watts)
- Sleep (low power, <1 watt)
- Resume

Green PC support requires the VBE/PM compatible BIOS from Avance Logic, Inc.

DDC Monitor Support

Will support VESA DDC 1 and DDC 2B standards with the release of the Avance Logic, Inc. driver for Windows 95.

PCI Local Bus Compatibility

Compatible with PCI Specification 2.0/2.1 and chipsets from the following manufacturers:

- Acer Labs
- OPTI
- Intel (Saturn, Mercury, Neptune, Aries, and Triton)
- SIS
- VIA
- And most other PCI Local Bus compatible chipsets

Memory Compatibility

Supports the following:

- 32/64-bit memory interface
- 1 MB and 2 MB memories
- 128k x16 DRAM (45/60/70 ns)
- 256k x 4 DRAM (45/60/70 ns)
- 256k x 8 DRAM (45/60/70 ns)
- 256k x 16 DRAM (45/60/70 ns)
- Fast Page Mode/EDO
- Multiple-level read/write cache

Performance

1 MB frame buffer

- Equal to current 64-bit chips

2 MB frame buffer

- Higher than with a 1 MB frame buffer

Hardware Graphics Functions

- 4, 8, 15, 16, 24,32 bits-per-pixel graphics
- Full 256 Windows ROPS support
- Transparent BitBlt
- Rectangle fill and copy and Polygon area fill
- Monochrome color expansion
- Line draw
- Display list polyline
- Hardware cursor
- Windows mask map

Integrated 32-bit RAMDAC

Introduction

The RAMDAC supports true color display of the desktop image and graphics applications.

The RAMDAC has a built-in 256 x 18 (256,252) color lookup table with triple 8-bit pseudo color video D/A converters. It also supports the AT&T 2020C491, 24-bit color format of 16.7 million simultaneous colors display while maintaining software backward compatibility with Pseudo Color (BT476), Hi Color (SC11482), and XGA Color (ALG1101) RAMDACs.

To further enhance its performance, the RAMDAC has built-in pipeline operations and circuitry to eliminate possible sparkle which may occur during high speed operations.

Features

Supports:

- Photo (true) color with up to 16.7M colors
- 256, 32k, 64k, and 16.7M color modes
- 8 8 8, 5 6 5 XGA, TARGA, and pseudo color formats
- Clock rates of up to 135 MHz for operations on direct color modes with up to 85 MHz Look Up Table, (LUT) operations
- 256 x 18 color LUT for a total of 16.7 million colors
- RS 343A/RS 170 standards

Contains:

- Built-in power on reset defaulting to pseudo color mode
- Built-in noise elimination circuitry
- Current reference circuit design
- Blanking on all three channels (Red, Green, and Blue, RGB)

Functional Description

System Interface

The RAMDAC supports the standard system bus interface, allowing direct access to the color lookup table which is required by some applications.

The RS1 and RS0 control inputs identify whether the system is accessing the address registers or color palette RAM. The RAMDAC uses the 8-bit address register to access the color palette RAM.

Writing Color Palette RAM

When writing color data, the system writes the address register with the address location of the color lookup table. The system performs three successive write cycles with six bits each of red, green, and blue, using RS1 and RS0 to select the color palette RAM. After the blue write cycle, the three bytes of color information are concatenated into an 18-bit word and written to the location specified by the address register.

The address register then increments to the next location which the system may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the starting address and continuing to execute red, green, and blue write cycles until the entire block has been written.

Reading Color Palette RAM

When reading color data, the system loads the address register with the location of the color lookup table. The contents of the color lookup table at the specified address is copied into the RGB registers and the address register is incremented to the next RAM location. The system performs three successive read cycles of six bits each of red, green, and blue, using RS1 and RS0 to select the color lookup table. Following the blue read cycle, the contents of the lookup table specified by the address register is copied into the RGB registers and the address register gets incremented again. A block of color values in consecutive locations may be read by writing the starting address and continuing to execute red, green, and blue read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to 00h following a blue read or write cycle to RAM location FFh. The system interface operates asynchronously to the pixel clock. Data transfers between the color lookup table and the RGB registers are synchronized by internal logic, and occur during the periods between system accesses. To eliminate noise on the monitor during system access to the color palette RAM, hardware circuitry is designed to maintain the previous output color data on the outputs of the three D/A converters while the transfer between the color lookup table RAMs and the RGB registers occurs. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa and ADDRb) that count modulo three. They are reset to zero when the system writes to the address register and are not reset to zero when the system reads the address register. The system does not have access to these bits. The other eight bits of the address register (ADDR0-7) are incremented following a blue read or write cycle, they are accessible to the system, and they are used to address color lookup table locations. ADDR0 is the least significant bit when the system is accessing the RAM. The system may read the address register at any time without modifying its contents or the existing read/write mode.

Data Bus Interface

Color data is contained on the lower six bits of the data bus, with D0 being the least significant bit and D5 the most significant bit of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 are set to zero.

Photo (True) Color Modes

The RAMDAC supports multiple color modes, the 8-bit pseudo, the AL32K high color, the AL64K XGA color, and the AL16.7M true color modes. To access color modes beyond the standard 256 pseudo color, set bit 7 of the Pixel Read Mask Register 3C6H to 1 (0 is the default for the pseudo color mode). Once the higher color mode is activated, the RAMDAC will reformat pixels from Bit0 through Bit7 to support up to a 24 bpp format and will bypass the color lookup table. The following is the register information on how to program the Pixel Read Mask Register to support multiple color modes.

64k Image Color Mode

The RAMDAC supports the 565 mode of 65,536 colors. Each pixel is represented by two bytes containing five bits each of red and blue and six bits of green color intensity information. The input sequence for each pixel is first the low byte and then the high byte. The first low byte is taken on the first rising edge of CLOCK occurring when BLANKn has gone inactive (high). All subsequent bytes are clocked in on the rising edge of CLOCK. The color lookup table is ignored in this mode. The data is presented to the DACs directly as the most significant bits, with the lower bits set to zero.

16.7 Million True Color Mode

The RAMDAC supports the 888 mode of 16,777,216 colors. Each pixel is represented by three bytes containing eight bits each of red, green, and blue color intensity information. The input sequence for each pixel is first the low byte, then the middle byte, and then the high byte. The first low byte is taken on the first rising edge of CLOCK occurring when BLANKn has gone inactive (high). All subsequent bytes are clocked in on the rising edge of CLOCK. The color lookup table is ignored in this mode. The data is presented to the DACs directly and the pixel output is at one third of the CLOCK input rate.

Automatic Monitor Type Detection

The outputs of the three DACs are compared to an internal reference voltage of 335 mV with voltage comparators. The outputs of the three comparators are gated together to generate the signal Sense Output. The status of the Sense Output signal when specific patterns have been sent to the DACs, indicates if a VGA compatible monitor is attached.

Frame Buffer Interface

The P0-P7 inputs are used to address the color palette RAM. The contents of the pixel read mask register, which may be accessed by the system at any time, are logically ANDed with the P0-P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 18 bits of color information to the three D/A converters. The analog outputs of the RAMDAC are capable of directly driving a 37.5 ohm load, such as a doubly terminated 75 ohm coaxial cable.

Integrated Dual Programmable Clock

Introduction

The integrated dual programmable clock generates two output frequencies of up to 135 MHz each, one is the DRAM clock and the other is the Pixel clock. The DRAM clock output frequency is selected by setting AL Extended Clock Select Register 3 (3CE.15h) with the DRAM Clock Frequency Selection byte. If no DRAM Clock Frequency Selection byte is set into this register, the output frequency reverts to the default frequency of 76 MHz. The Pixel clock output frequency is set to one of seven preset frequencies or set to produce a programmed frequency by setting one bit in AL Extended Control Register 4 (3CE.Ch) and two bits in Miscellaneous Register (3C2h (W). If set to produce a programmed frequency, the Pixel clock output frequency is selected by setting AL Extended Clock Select Register 1 (3CE.13h) with the low order byte of the Pixel Clock Frequency Selection word and AL Extended Clock Select Register 2 (3CE.14h) with the high order byte of the Pixel Clock Frequency Selection word.

The dual programmable clock's advanced Phase Locked Loop (PLL) design provides for rapid frequency transition and low phase jitter to ensure a top quality display. The Pixel clock output frequency is compatible with IBM VGA, EGA, CGA, MDA, Hercules, and VESA standards as well as the higher frequencies needed for high resolution display applications.

Features

- Programmable, cost-effective dual clock synthesis
- Phase Locked Loop clock generation
- High frequency operation of up to 135 MHz
- Programmable frequencies for both Pixel and DRAM clocks
- Pixel clock frequencies compatible with IBM VGA/EGA/CGA/ MDA, Hercules and VESA standards

Programming the DRAM Clock Output Frequency

DRAM Clock Frequency Selection Byte Format

Bits	7	6	5	4	3	2	1	0
	M						N	

Where:

M = feedback frequency divider - the binary decode of 1 of the 61 hexadecimal numbers, M(h), in the DRAM Clock table shifted two places to the left

N = reference frequency divider - chosen from the following so that M(i) calculates to a number between 2 and 62 in the Output Frequency formula below

16 (binary code 0 0)
32 (binary code 0 1)
64 (binary code 1 0)
128 (binary code 1 1)

M(i) = an index number calculated with the formula below and used for locating the correct M(h) in the DRAM Clock table

M(h) = a hexadecimal number created from the six M(code) bits (bits 7 through 2) in each DRAM Clock table entry, where bit 7 is the least significant bit (LSB) and bit 2 is the most significant bit (MSB)

Output Frequency Formula

$$\text{Output frequency} = \frac{14.318 * 4 * M(i)}{N}$$

Note: With no DRAM Clock Frequency Selection input, the default DRAM clock output frequency is 76 MHz.

DRAM Clock Frequency Example

The target DRAM clock output frequency is 77 MHz.

$$77 = \frac{14.318 * 4 * M(i)}{32}$$

$$M(i) = 43.0227 = 43$$

Use the value computed for M(i) to index the DRAM Clock table. At entry 43 of the DRAM Clock table, the value of M(h) is 3Ah.

M(i)	M(code) 7 6 5 4 3 2	M(h)
43	0 1 0 1 1 1	3A

Shift the binary decode of 3Ah two places to the left and append the two bit binary code of N (in this example the bits are 0 1 for the N value of 32). The result is the following DRAM Clock Frequency Selection byte.

Bits	7	6	5	4	3	2	1	0
	1	1	1	0	1	0	0	1

or

E9h

If AL Extended Clock Select Register 3 (3CE.15h) is set to the value E9h, the DRAM clock output frequency will be 77 MHz.

DRAM Clock Table

M(i)	M(code) 7 6 5 4 3 2	M(h)
62	0 0 1 0 0 0	04
61	0 0 0 1 0 0	08
60	0 0 0 0 1 0	10
59	1 0 0 0 0 1	21
58	1 1 0 0 0 0	03
57	0 1 1 0 0 0	06
56	0 0 1 1 0 0	0C
55	0 0 0 1 1 0	18
54	1 0 0 0 1 1	31
53	0 1 0 0 0 1	22
52	1 0 1 0 0 0	05
51	0 1 0 1 0 0	0A
50	0 0 1 0 1 0	14
49	1 0 0 1 0 1	29
48	1 1 0 0 1 0	13
47	1 1 1 0 0 1	27
46	1 1 1 1 0 0	0F
45	0 1 1 1 1 0	1E
44	1 0 1 1 1 1	3D
43	0 1 0 1 1 1	3A
42	0 0 1 0 1 1	34
41	0 0 0 1 0 1	28

M(i)	M(code) 7 6 5 4 3 2	M(h)
40	1 0 0 0 1 0	11
39	1 1 0 0 0 1	23
38	1 1 1 0 0 0	07
37	0 1 1 1 0 0	0E
36	0 0 1 1 1 0	1C
35	1 0 0 1 1 1	39
34	0 1 0 0 1 1	32
33	0 0 1 0 0 1	24
32	1 0 0 1 0 0	09
31	0 1 0 0 1 0	12
30	1 0 1 0 0 1	25
29	1 1 0 1 0 0	0B
28	0 1 1 0 1 0	16
27	1 0 1 1 0 1	2D
26	1 1 0 1 1 0	1B
25	1 1 1 0 1 1	37
24	0 1 1 1 0 1	2E
23	1 0 1 1 1 0	1D
22	1 1 0 1 1 1	3B
21	0 1 1 0 1 1	36
20	0 0 1 1 0 1	2C
19	1 0 0 1 1 0	19

M(i)	M(code) 7 6 5 4 3 2	M(h)
18	1 1 0 0 1 1	33
17	0 1 1 0 0 1	26
16	1 0 1 1 0 0	0D
15	0 1 0 1 1 0	1A
14	1 0 1 0 1 1	35
13	0 1 0 1 0 1	2A
12	1 0 1 0 1 0	15
11	1 1 0 1 0 1	2B
10	1 1 1 0 1 0	17
9	1 1 1 1 0 1	2F
8	1 1 1 1 1 0	1F
7	1 1 1 1 1 1	3F
6	0 1 1 1 1 1	3E
5	0 0 1 1 1 1	3C
4	0 0 0 1 1 1	38
3	0 0 0 0 1 1	30
2	0 0 0 0 1 0	20

Programming the Pixel Clock Output Frequency

Pixel Clock Frequency Selection Word Format

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	D	M							N		O	

Where:

D = double frequency feedback divider - chosen from the following so that M(i) calculate to a number between 2 and 126 in the Output Frequency formula below
- 1 (binary code 0)
- 2 (binary code 1)

M = feedback frequency divider - the binary decode of the low order seven bits of 1 of the 126 hexadecimal numbers, M(h), in the Pixel Clock table

N = reference frequency divider - chosen from the following so that when multiplied with O, M(i) calculates to a number between 2 and 126 in the Output Frequency formula below
- 16 (binary code 0 0)
- 32 (binary code 0 1)
- 64 (binary code 1 0)
- 128 (binary code 1 1)

O = output divider - chosen from the following so that when multiplied with N, M(i) calculates to a number between 2 and 126 in the Output Frequency formula below
- 1 (binary code 0 0)
- 2 (binary code 0 1)
- 4 (binary code 1 0)
- 8 (binary code 1 1)

M(i) = an index number calculated with the formula below and used for locating the correct M(h) in the Pixel Clock table

M(h) = a hexadecimal number created from the seven M(code) bits (bits 7 through 1) in each Pixel Clock table entry, where bit 7 is the most significant bit (MSB) and bit 1 is the least significant bit (LSB)

Output Frequency Formula

$$\text{Output frequency} = \frac{14.318 * 2 * M(i) * D}{N * O}$$

Pixel Clock Frequency Example

The target Pixel clock output frequency is 77.8 MHz.

$$77.8 = \frac{14.318 * 2 * M(i) * 1}{32 * 1}$$

$$M(i) = 86.9395 = 87$$

Use the value computed for M(i) to index the Pixel Clock table. At entry 87 of the Pixel Clock table, the value of M(h) is 6 Ah.

M(i)	M(code) 7 6 5 4 3 2 1	M(h)
87	1 1 0 1 0 1 0	6A

Bit 11 is the binary code of D (in this example the bit is 0 for the D value of 1). Bits 10 through 4 are the low order seven bits of M(h) (in this example the bits are 1 1 0 1 0 1 0). Bits 3 and 2 are the binary code for N (in this example the bits are 0 1 for the N value of 32). Bits 1 and 0 are the binary code for O (in this example the bits are 0 0 for the O value of 1). The result is the following Pixel Clock Frequency Selection word.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					D	M							N		O	
	0	0	0	0	0	1	1	0	1	0	1	0	0	1	0	0

or

06A4h

Note: If 16 had been chosen for the value of N and 2 had been chosen for the value of O, the Pixel Clock Frequency Selection word would have been 06A1h. This word will give the same output frequency as the one calculated in this example.

If AL Extended Clock Select Register 2 (3CE.14h) is set to the value 06h and AL Extended Clock Select Register 1 (3CE.13h) is set to the value A4 or A1 (see the note above), the Pixel clock output frequency will be 77.8 MHz.

Pixel Clock Table

M(i)	M(code) 7 6 5 4 3 2 1	M(h)
2	1 0 0 0 0 0 0	40
3	1 1 0 0 0 0 0	60
4	1 1 1 0 0 0 0	70
5	1 1 1 1 0 0 0	78
6	1 1 1 1 1 0 0	7C
7	1 1 1 1 1 1 0	7E
8	1 1 1 1 1 1 1	7F
9	0 1 1 1 1 1 1	3F
10	1 0 1 1 1 1 1	5F
11	0 1 0 1 1 1 1	2F
12	1 0 1 0 1 1 1	57
13	0 1 0 1 0 1 1	2B
14	1 0 1 0 1 0 1	55
15	0 1 0 1 0 1 0	2A
16	0 0 1 0 1 0 1	15
17	1 0 0 1 0 1 0	4A
18	1 1 0 0 1 0 1	65
19	0 1 1 0 0 1 0	32
20	0 0 1 1 0 0 1	19
21	1 0 0 1 1 0 0	4C
22	1 1 0 0 1 1 0	66
23	1 1 1 0 0 1 1	73

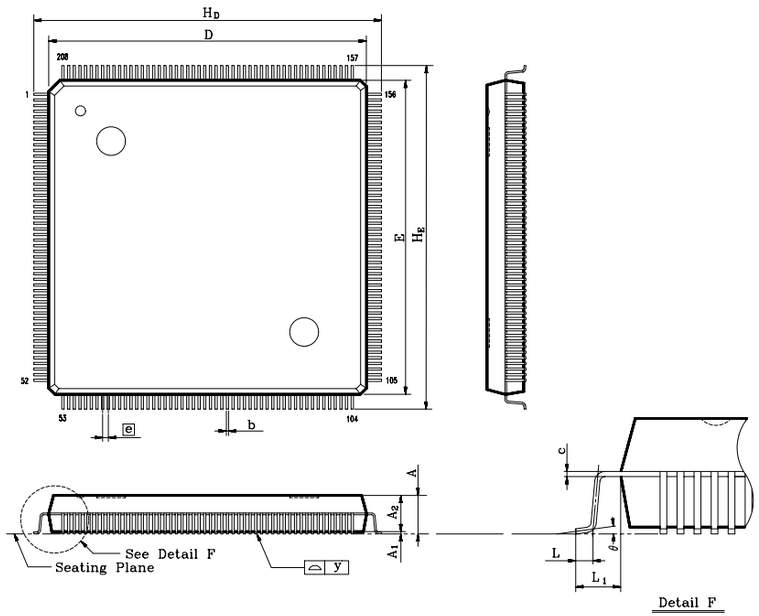
M(i)	M(code) 7 6 5 4 3 2 1	M(h)
24	0 1 1 1 0 0 1	39
25	1 0 1 1 1 0 0	5C
26	1 1 0 1 1 1 0	6E
27	1 1 1 0 1 1 1	77
28	0 1 1 1 0 1 1	3B
29	1 0 1 1 1 0 1	5D
30	0 1 0 1 1 1 0	2E
31	0 0 1 0 1 1 1	17
32	1 0 0 1 0 1 1	4B
33	0 1 0 0 1 0 1	25
34	1 0 1 0 0 1 0	52
35	1 1 0 1 0 0 1	69
36	0 1 1 0 1 0 0	34
37	0 0 1 1 0 1 0	1A
38	0 0 0 1 1 0 1	0D
39	1 0 0 0 1 1 0	46
40	1 1 0 0 0 1 1	63
41	0 1 1 0 0 0 1	31
42	1 0 1 1 0 0 0	58
43	1 1 0 1 1 0 0	6C
44	1 1 1 0 1 1 0	76
45	1 1 1 1 0 1 1	7B

M(i)	M(code) 7 6 5 4 3 2 1	M(h)
46	0 1 1 1 1 0 1	3D
47	1 0 1 1 1 1 0	5E
48	1 1 0 1 1 1 1	6F
49	0 1 1 0 1 1 1	37
50	1 0 1 1 0 1 1	5B
51	0 1 0 1 1 0 1	2D
52	1 0 1 0 1 1 0	56
53	1 1 0 1 0 1 1	6B
54	0 1 1 0 1 0 1	35
55	1 0 1 1 0 1 0	5A
56	1 1 0 1 1 0 1	6D
57	0 1 1 0 1 1 0	36
58	0 0 1 1 0 1 1	1B
59	1 0 0 1 1 0 1	4D
60	0 1 0 0 1 1 0	26
61	0 0 1 0 0 1 1	13
62	1 0 0 1 0 0 1	49
63	0 1 0 0 1 0 0	24
64	0 0 1 0 0 1 0	12
65	0 0 0 1 0 0 1	09
66	1 0 0 0 1 0 0	44
67	1 1 0 0 0 1 0	62

Pixel Clock Table (continued))

M(i)	M(code) 7 6 5 4 3 2	M(h)
68	1 1 1 0 0 0 1	71
69	0 1 1 1 0 0 0	38
70	0 0 1 1 1 0 0	1C
71	0 0 0 1 1 1 0	0E
72	0 0 0 0 1 1 1	07
73	1 0 0 0 0 1 1	43
74	0 1 0 0 0 0 1	21
75	1 0 1 0 0 0 0	50
76	1 1 0 1 0 0 0	68
77	1 1 1 0 1 0 0	74
78	1 1 1 1 0 1 0	7A
79	1 1 1 1 1 0 1	7D
80	0 1 1 1 1 1 0	3E
81	0 0 1 1 1 1 1	1F
82	1 0 0 1 1 1 1	4F
83	0 1 0 0 1 1 1	27
84	1 0 1 0 0 1 1	53
85	0 1 0 1 0 0 1	29
86	1 0 1 0 1 0 0	54
87	1 1 0 1 0 1 0	6A
88	1 1 1 0 1 0 1	75
89	0 1 1 1 0 1 0	3A
90	0 0 1 1 1 0 1	1D
91	1 0 0 1 1 1 0	4E
92	1 1 0 0 1 1 1	67
93	0 1 1 0 0 1 1	33
94	1 0 1 1 0 0 1	59
95	0 1 0 1 1 0 0	2C
96	0 0 1 0 1 1 0	16
97	0 0 0 1 0 1 1	0B
98	1 0 0 0 1 0 1	45
99	0 1 0 0 0 1 0	22
100	0 0 1 0 0 0 1	11
101	1 0 0 1 0 0 0	48
102	1 1 0 0 1 0 0	64
103	1 1 1 0 0 1 0	72
104	1 1 1 1 0 0 1	79
105	0 1 1 1 1 0 0	3C
106	0 0 1 1 1 1 0	1E
107	0 0 0 1 1 1 1	0F
108	1 0 0 0 1 1 1	47
109	0 1 0 0 0 1 1	23
110	1 0 1 0 0 0 1	51
111	0 1 0 1 0 0 0	28
112	0 0 1 0 1 0 0	14
113	0 0 0 1 0 1 0	0A
114	0 0 0 0 1 0 1	05
115	1 0 0 0 0 1 0	42
116	1 1 0 0 0 0 1	61
117	0 1 1 0 0 0 0	30
118	0 0 1 1 0 0 0	18
119	0 0 0 1 1 0 0	0C
120	0 0 0 0 1 1 0	06
121	0 0 0 0 0 1 1	03
122	1 0 0 0 0 0 1	41
123	0 1 0 0 0 0 0	20
124	0 0 1 0 0 0 0	10
125	0 0 0 1 0 0 0	08
126	0 0 0 0 1 0 0	04
127	0 0 0 0 0 1 0	02

Physical Description



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Typ	Max	Min	Typ	Max
A	0.136	0.144	0.152	3.45	3.65	3.85
A_1	0.004	0.020	0.036	0.10	0.51	0.91
A_2	0.119	0.128	0.136	3.02	3.24	3.46
b	0.004	0.008	0.012	0.10	0.20	0.30
c	0.002	0.006	0.010	0.04	0.15	0.26
D	1.093	1.102	1.112	27.75	28.00	28.25
E	1.093	1.102	1.112	27.75	28.00	28.25
e	0.012	0.020	0.031	0.30	0.50	0.80
H_D	1.169	1.205	1.240	29.70	30.60	31.50
H_E	1.169	1.205	1.240	29.70	30.60	31.50
L	0.010	0.020	0.030	0.25	0.50	0.75
L_1	0.041	0.051	0.061	1.05	1.30	1.55
y	-	-	0.004	-	-	0.10
θ	0 to 12°					

Notes:
1. Dimensions D and E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

TITLE : 208L QFP (28x28 mm**2) FOOTPRINT 2.6 mm PACKAGE OUTLINE DRAWING			
LEADFRAME MATERIAL			
APPROVE		DOC. NO.	30008
		VERSION	1.2
		PAGE	1 OF 1
CHECK		DWG NO.	QFP208Y.DOC
		DATE	Sept 06, 1995
Avance Logic, Inc.			

Block Diagram

Chapter 2

Module I/O Pins

I/O Pins Chart

PCI Local Bus Interface

Item	Pin Name	Type	Pin No.	Description
1	PAR	I	32	Parity
2	STOP-	I/O	31	Stop
3	DEVSEL-	O	30	Device Select
4	TRDY-	I/O	29	Target Ready
5	IRDY-	I	27	Initiator Ready
6	FRAME-	I	26	Cycle Frame
7	RESET-	I	3	Reset
8	IDSEL	I	15	Initialization Device Select
9	CBE0-	I	44	C/Byte Enable 0
10	CBE1-	I	33	C/Byte Enable 1
11	CBE2-	I	25	C/Byte Enable 2
12	CBE3-	I	13	C/Byte Enable 3
13	INTA-	O	2	Interrupt Request A
14	AD0	I/O	52	Multiplexed Host Address/Data Bit 0
15	AD1	I/O	51	Multiplexed Host Address/Data Bit 1
16	AD2	I/O	50	Multiplexed Host Address/Data Bit 2
17	AD3	I/O	49	Multiplexed Host Address/Data Bit 3
18	AD4	I/O	48	Multiplexed Host Address/Data Bit 4
19	AD5	I/O	47	Multiplexed Host Address/Data Bit 5
20	AD6	I/O	46	Multiplexed Host Address/Data Bit 6
21	AD7	I/O	45	Multiplexed Host Address/Data Bit 7

Item	Pin Name	Type	Pin No.	Description
22	AD8	I/O	42	Multiplexed Host Address/Data Bit 8
23	AD9	I/O	41	Multiplexed Host Address/Data Bit 9
24	AD10	I/O	40	Multiplexed Host Address/Data Bit 10
25	AD11	I/O	39	Multiplexed Host Address/Data Bit 11
26	AD12	I/O	38	Multiplexed Host Address/Data Bit 12
27	AD13	I/O	36	Multiplexed Host Address/Data Bit 13
28	AD14	I/O	35	Multiplexed Host Address/Data Bit 14
29	AD15	I/O	34	Multiplexed Host Address/Data Bit 15
30	AD16	I/O	24	Multiplexed Host Address/Data Bit 16
31	AD17	I/O	23	Multiplexed Host Address/Data Bit 17
32	AD18	I/O	22	Multiplexed Host Address/Data Bit 18
33	AD19	I/O	21	Multiplexed Host Address/Data Bit 19
34	AD20	I/O	20	Multiplexed Host Address/Data Bit 20
35	AD21	I/O	19	Multiplexed Host Address/Data Bit 21
36	AD22	I/O	18	Multiplexed Host Address/Data Bit 22
37	AD23	I/O	17	Multiplexed Host Address/Data Bit 23
38	AD24	I/O	12	Multiplexed Host Address/Data Bit 24
39	AD25	I/O	11	Multiplexed Host Address/Data Bit 25
40	AD26	I/O	10	Multiplexed Host Address/Data Bit 26
41	AD27	I/O	9	Multiplexed Host Address/Data Bit 27
42	AD28	I/O	8	Multiplexed Host Address/Data Bit 28
43	AD29	I/O	7	Multiplexed Host Address/Data Bit 29
44	AD30	I/O	6	Multiplexed Host Address/Data Bit 30

Item	Pin Name	Type	Pin No.	Description
45	AD31	I/O	5	Multiplexed Host Address/Data Bit 31
46	SCLK	I	4	PCI system clock

DRAM Interface

Item	Pin Name	Type	Pin No.	Description
47	MA0	O	116	DRAM Address Bit 0
48	MA1	O	115	DRAM Address Bit 1
49	MA2	O	114	DRAM Address Bit 2
50	MA3	O	113	DRAM Address Bit 3
51	MA4	O	112	DRAM Address Bit 4
52	MA5	O	111	DRAM Address Bit 5
53	MA6	O	110	DRAM Address Bit 6
54	MA7	O	109	DRAM Address Bit 7
55	MA8	O	108	DRAM Address Bit 8
56	M0D0	I/O	64	DRAM Data Bit 0 MAP 0
57	M0D1	I/O	63	DRAM Data Bit 1 MAP 0
58	M0D2	I/O	62	DRAM Data Bit 2 MAP 0
59	M0D3	I/O	61	DRAM Data Bit 3 MAP 0
60	M0D4	I/O	60	DRAM Data Bit 4 MAP 0
61	M0D5	I/O	59	DRAM Data Bit 5 MAP 0
62	M0D6	I/O	58	DRAM Data Bit 6 MAP 0
63	M0D7	I/O	57	DRAM Data Bit 7 MAP 0

Item	Pin Name	Type	Pin No.	Description
64	M1D0	I/O	73	DRAM Data Bit 0 MAP 1
65	M1D1	I/O	72	DRAM Data Bit 1 MAP 1
66	M1D2	I/O	71	DRAM Data Bit 2 MAP 1
67	M1D3	I/O	70	DRAM Data Bit 3 MAP 1
68	M1D4	I/O	69	DRAM Data Bit 4 MAP 1
69	M1D5	I/O	68	DRAM Data Bit 5 MAP 1
70	M1D6	I/O	67	DRAM Data Bit 6 MAP 1
71	M1D7	I/O	66	DRAM Data Bit 7 MAP 1
72	M2D0	I/O	82	DRAM Data Bit 0 MAP 2
73	M2D1	I/O	81	DRAM Data Bit 1 MAP 2
74	M2D2	I/O	80	DRAM Data Bit 2 MAP 2
75	M2D3	I/O	79	DRAM Data Bit 3 MAP 2
76	M2D4	I/O	77	DRAM Data Bit 4 MAP 2
77	M2D5	I/O	76	DRAM Data Bit 5 MAP 2
78	M2D6	I/O	75	DRAM Data Bit 6 MAP 2
79	M2D7	I/O	74	DRAM Data Bit 7 MAP 2
80	M3D0	I/O	90	DRAM Data Bit 0 MAP 3
81	M3D1	I/O	89	DRAM Data Bit 1 MAP 3
82	M3D2	I/O	88	DRAM Data Bit 2 MAP 3
83	M3D3	I/O	87	DRAM Data Bit 3 MAP 3
84	M3D4	I/O	86	DRAM Data Bit 4 MAP 3
85	M3D5	I/O	85	DRAM Data Bit 5 MAP 3
86	M3D6	I/O	84	DRAM Data Bit 6 MAP 3

Item	Pin Name	Type	Pin No.	Description
87	M3D7	I/O	83	DRAM Data Bit 7 MAP 3
88	M4D0	I/O	134	XBUS Addr Bit 0/DRAM Data Bit 0 Map 4
89	M4D1	I/O	133	XBUS Addr Bit 1/DRAM Data Bit 1 Map 4
90	M4D2	I/O	132	XBUS Addr Bit 2/DRAM Data Bit 2 Map 4
91	M4D3	I/O	131	XBUS Addr Bit 3/DRAM Data Bit 3 Map 4
92	M4D4	I/O	130	XBUS Addr Bit 4/DRAM Data Bit 4 Map 4
93	M4D5	I/O	129	XBUS Addr Bit 5/DRAM Data Bit 5 Map 4
94	M4D6	I/O	128	XBUS Addr Bit 6/DRAM Data Bit 6 Map 4
95	M4D7	I/O	127	XBUS Addr Bit 7/DRAM Data Bit 7 Map 4
96	M5D0	I/O	143	XBUS Addr Bit 8/DRAM Data Bit 0 Map 5
97	M5D1	I/O	142	XBUS Addr Bit 9/DRAM Data Bit 1 Map 5
98	M5D2	I/O	141	XBUS Addr Bit 10/DRAM Data Bit 2 Map 5
99	M5D3	I/O	140	XBUS Addr Bit 11/DRAM Data Bit 3 Map 5
100	M5D4	I/O	139	XBUS Addr Bit 12/DRAM Data Bit 4 Map 5
101	M5D5	I/O	138	XBUS Addr Bit 13/DRAM Data Bit 5 Map 5
102	M5D6	I/O	136	XBUS Addr Bit 14/DRAM Data Bit 6 Map 5
103	M5D7	I/O	135	XBUS Addr Bit 15/DRAM Data Bit 7 Map 5
104	M6D0	I/O	152	DRAM Data Bit 0 MAP 6
105	M6D1	I/O	151	DRAM Data Bit 1 MAP 6
106	M6D2	I/O	150	DRAM Data Bit 2 MAP 6
107	M6D3	I/O	149	DRAM Data Bit 3 MAP 6
108	M6D4	I/O	148	DRAM Data Bit 4 MAP 6
109	M6D5	I/O	147	DRAM Data Bit 5 MAP 6

Item	Pin Name	Type	Pin No.	Description
110	M6D6	I/O	145	DRAM Data Bit 6 MAP 6
111	M6D7	I/O	144	DRAM Data Bit 7 MAP 6
112	M7D0	I/O	161	XBUS Data Bit 0/DRAM Data Bit 0 Map 7
113	M7D1	I/O	160	XBUS Data Bit 1/DRAM Data Bit 1 Map 7
114	M7D2	I/O	159	XBUS Data Bit 2/DRAM Data Bit 2 Map 7
115	M7D3	I/O	158	XBUS Data Bit 3/DRAM Data Bit 3 Map 7
116	M7D4	I/O	156	XBUS Data Bit 4/DRAM Data Bit 4 Map 7
117	M7D5	I/O	155	XBUS Data Bit 5/DRAM Data Bit 5 Map 7
118	M7D6	I/O	154	XBUS Data Bit 6/DRAM Data Bit 6 Map 7
119	M7D7	I/O	153	XBUS Data Bit 7/DRAM Data Bit 7 Map 7
120	RAS-	O	107	DRAM Row Address Strobe
121	MA9	O	103	DRAM Address Bit 9
122	WE-	O	106	Write Enable
123	OE-	O	101	Read Output Enable
124	CAS0-	O	118	DRAM Column Address Strobe 0
125	CAS1-	O	119	DRAM Column Address Strobe 1
126	CAS2-	O	120	DRAM Column Address Strobe 2
127	CAS3-	O	121	DRAM Column Address Strobe 3
128	CAS4-	O	122	DRAM Column Address Strobe 4
129	CAS5-	O	123	DRAM Column Address Strobe 5
130	CAS6-	O	124	DRAM Column Address Strobe 6
131	CAS7-	O	125	DRAM Column Address Strobe 7

VESA Unified Memory Architecture Interface

Item	Pin Name	Type	Pin No.	Description
132	GNT-	I	56	Bus Master Grant
133	REQ0-	O	54	Bus Master Request Bit 0
134	REQ1-	O	55	Bus Master Request Bit 1

Clock and ROM Interface

Item	Pin Name	Type	Pin No.	Description
135	VCLK	I/O	204	External dot clock
136	MCLK	O	201	External memory clock
137	XTLO	O	206	14.318 MHz crystal output
138	XTLI	1	207	14.318 MHz crystal input
139	RSET	1	194	Current reference
140	MFILTER	I/O	202	Low pass filter
141	VFILTER	I/O	203	Low pass filter
142	ROMCS-	O	162	External BIOS ROM chip select

Monitor Interface

Item	Pin Name	Type	Pin No.	Description
143	HSYNC	hiZ	166	Horizontal retrace control
144	VSYNC	hiZ	165	Vertical retrace control
145	RED	O	197	Red
146	GREEN	O	196	Green
147	BLUE	O	195	Blue
148	DQ0	I/O	163	DDC clock for DDC 2
149	DQ1	I/O	164	DDC data for DDC 1 & 2

VFC Interface

Item	Pin Name	Type	Pin No.	Description
150	BLANK-	I/O	190	DAC Blanking control
151	PCLK	O	188	Pixel Clock
152	P0	I/O	184	Pixel Data Bit 0
153	P1	I/O	183	Pixel Data Bit 1
154	P2	I/O	182	Pixel Data Bit 2
155	P3	I/O	181	Pixel Data Bit 3
156	P4	I/O	180	Pixel Data Bit 4
157	P5	I/O	179	Pixel Data Bit 5
158	P6	I/O	178	Pixel Data Bit 6
159	P7	I/O	177	Pixel Data Bit 7

Power Interface I/O Pins Diagram

Item	Pin Name	Type	Pin No.	Description
160	VDD	Power	16	VCC power supply +5 V
161	VDD	Power	37	VCC power supply +5 V
162	VDD	Power	65	VCC power supply +5 V
163	VDD	Power	91	VCC power supply +5 V
164	VDD	Power	117	VCC power supply +5 V
165	VDD	Power	146	VCC power supply +5 V
166	VDD	Power	167	VCC power supply +5 V
167	VDD	Power	185	VCC power supply +5 V
168	AVDD1	Power	189	Analog power supply +5 V
169	AVDD2	Power	199	Analog power supply +5 V
170	AVDD3	Power	208	Analog power supply +5V
171	Gnd	Power	1	Ground pin
172	Gnd	Power	14	Ground pin
173	Gnd	Power	28	Ground pin
174	Gnd	Power	43	Ground pin
175	Gnd	Power	53	Ground pin
176	Gnd	Power	78	Ground pin
177	Gnd	Power	100	Ground pin
178	Gnd	Power	105	Ground pin
179	Gnd	Power	126	Ground pin
180	Gnd	Power	137	Ground pin
181	Gnd	Power	157	Ground pin

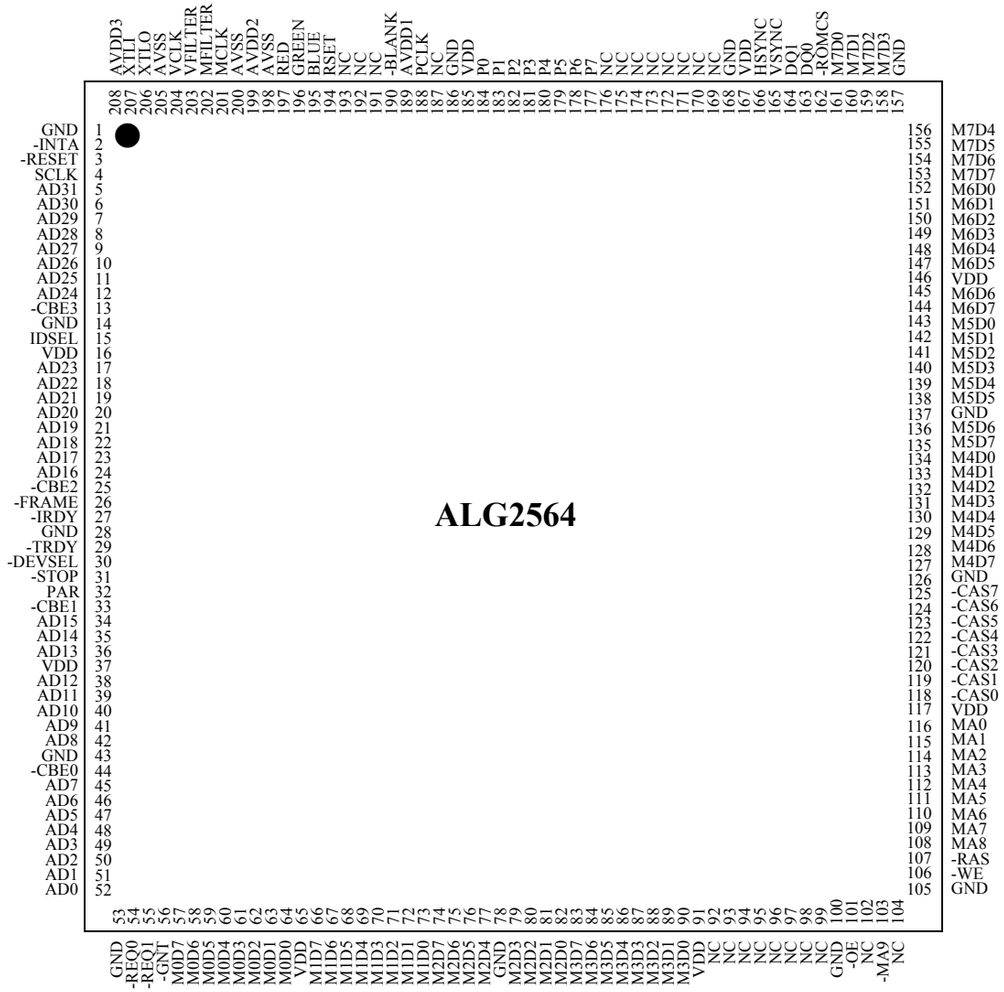
Item	Pin Name	Type	Pin No.	Description
182	Gnd	Power	168	Ground pin
183	Gnd	Power	186	Ground pin
184	AVSS	Power	198	Analog ground pin
185	AVSS	Power	200	Analog ground pin
186	AVSS	Power	205	Analog ground pin

Reserved Pin

Item	Pin Name	Type	Pin No.	Description
187	NC		92	
188	NC		93	
189	NC		94	
190	NC		95	
191	NC		96	
192	NC		97	
193	NC		98	
194	NC		99	
195	NC		102	
196	NC		104	
197	NC		169	
198	NC		170	
199	NC		171	
200	NC		172	
201	NC		173	

Item	Pin Name	Type	Pin No.	Description
202	NC		174	
203	NC		175	
204	NC		176	
205	NC		187	
206	NC		191	
207	NC		192	
208	NC		193	

Reserved Pin



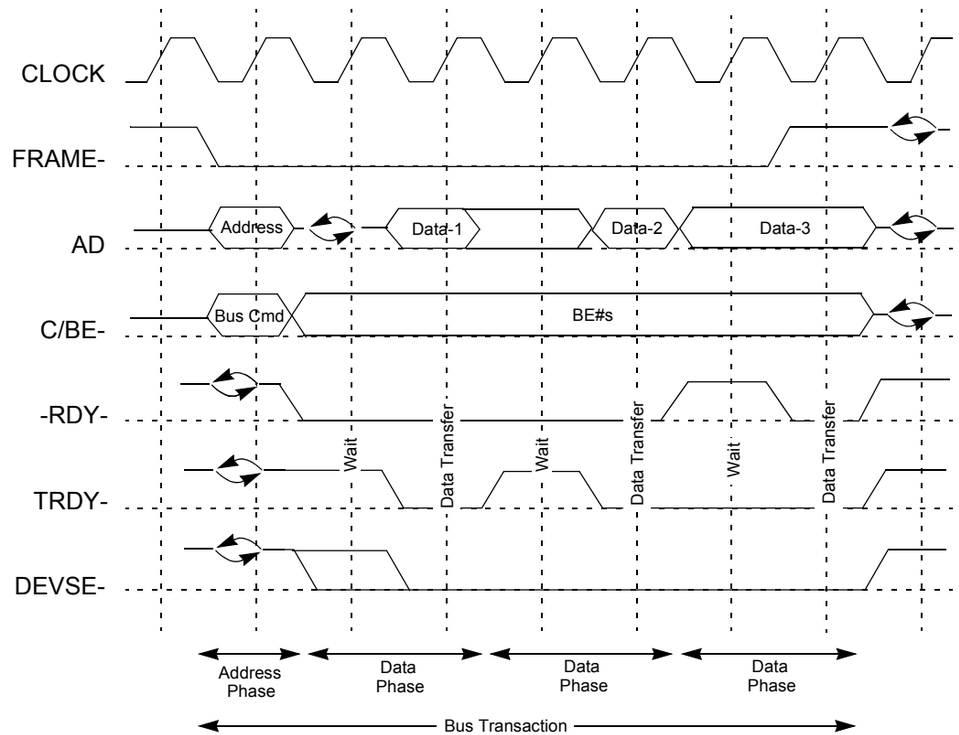
Item	Pin Name	Type	Pin No.	Description

Chapter 3

Timing Diagrams

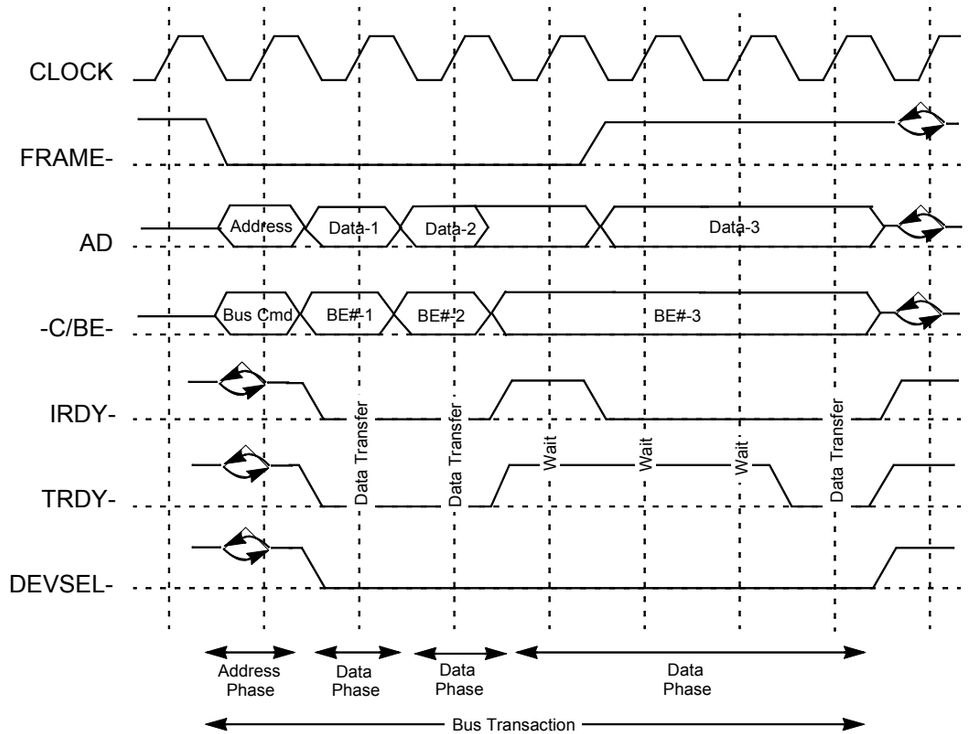
PCI Local Bus Timing Diagrams

PCI Local Bus Read Timing

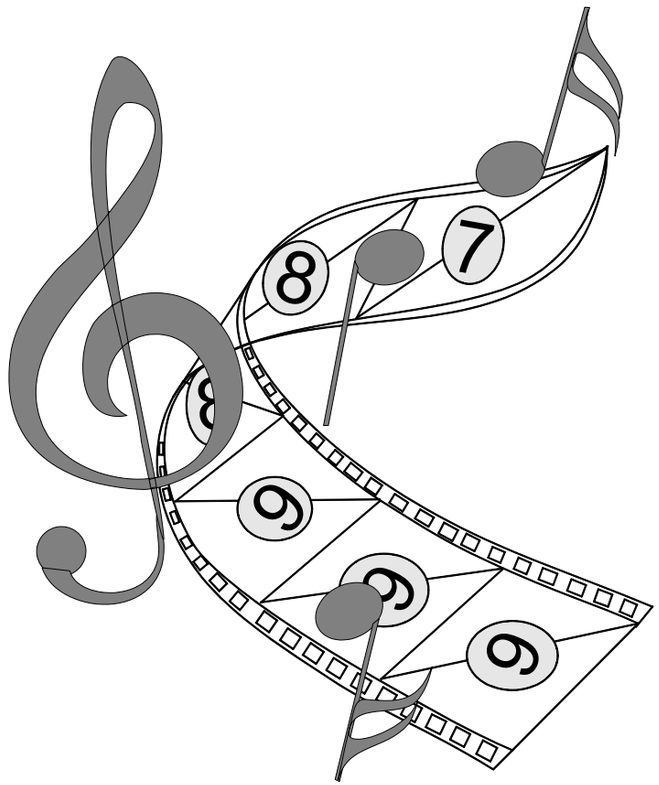


Note: For complete timing information, refer to the PCI Local Bus Specification 2.0/2.1.

PCI Local Bus Write Timing



Note: For complete timing information, refer to the PCI Local Bus Specification 2.0/2.1.


8
7
8
9
9
9

Chapter 5

Video/Graphics Adapter Cards

Introduction

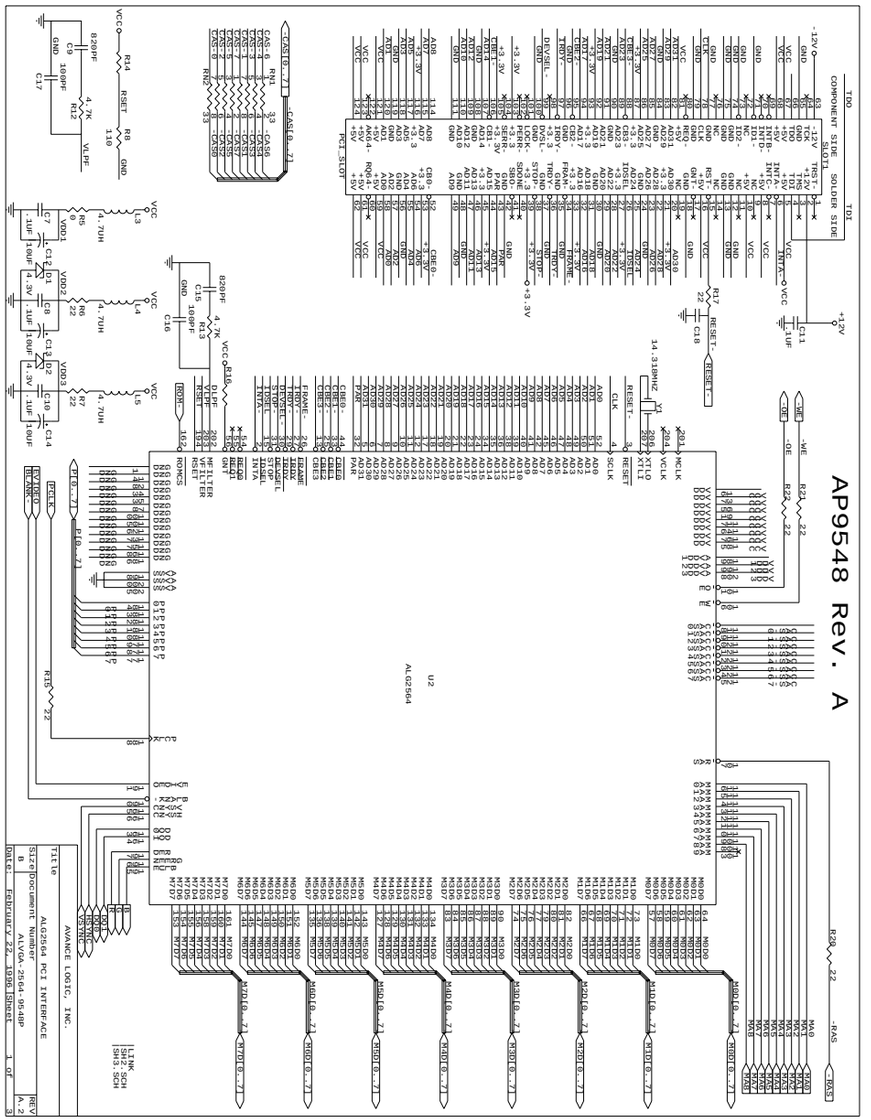
There are two versions of the video/graphics adapter card, the AP9548 and the AP9546. The AP9548 uses dedicated DRAMs for its frame buffer. The AP9546 uses a portion of the system main memory as its frame buffer by implementing Unified Memory Architecture (UMA). The AP9546 hardware is not currently available and therefore is not described here. When the AP9546 hardware becomes available, this manual will be updated to include the hardware description.

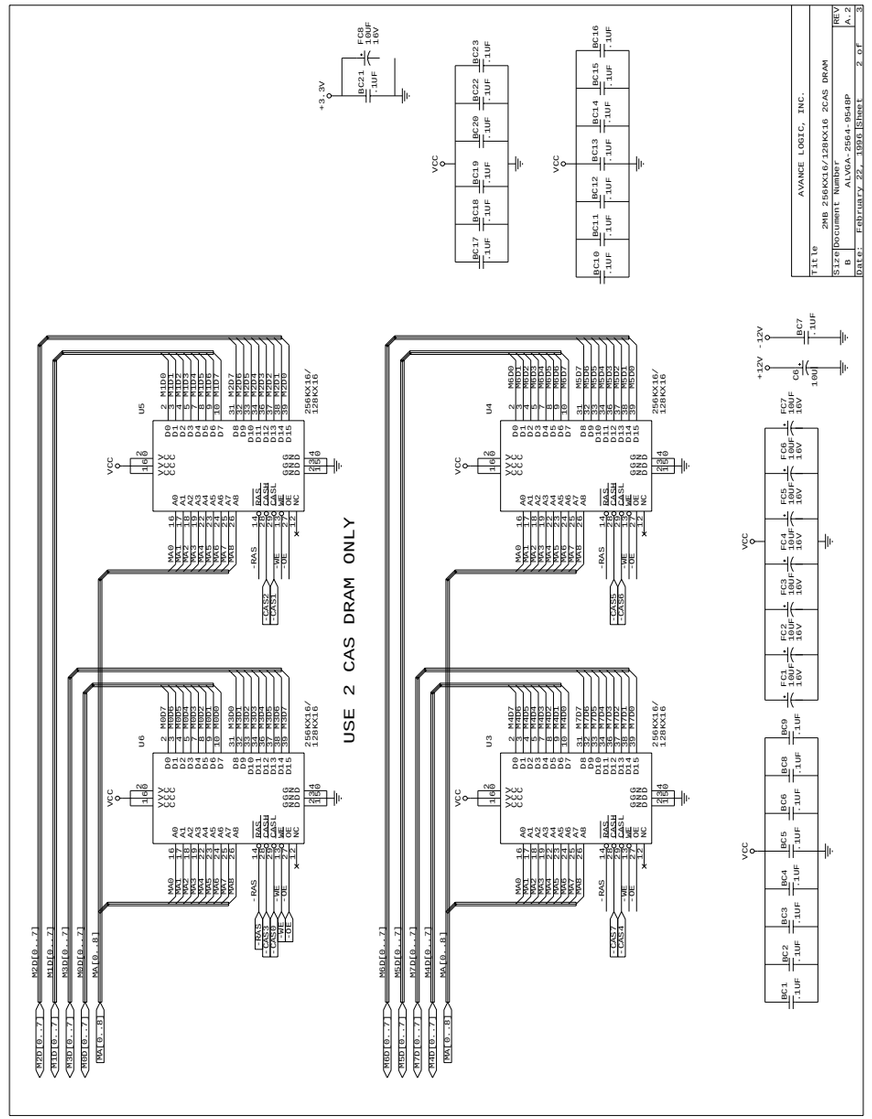
The video/graphics adapter card plugs into a PCI Local Bus expansion slot on the PC motherboard and holds the ALG2564 graphics and video processor, its supporting hardware, and VGA BIOS EPROM.

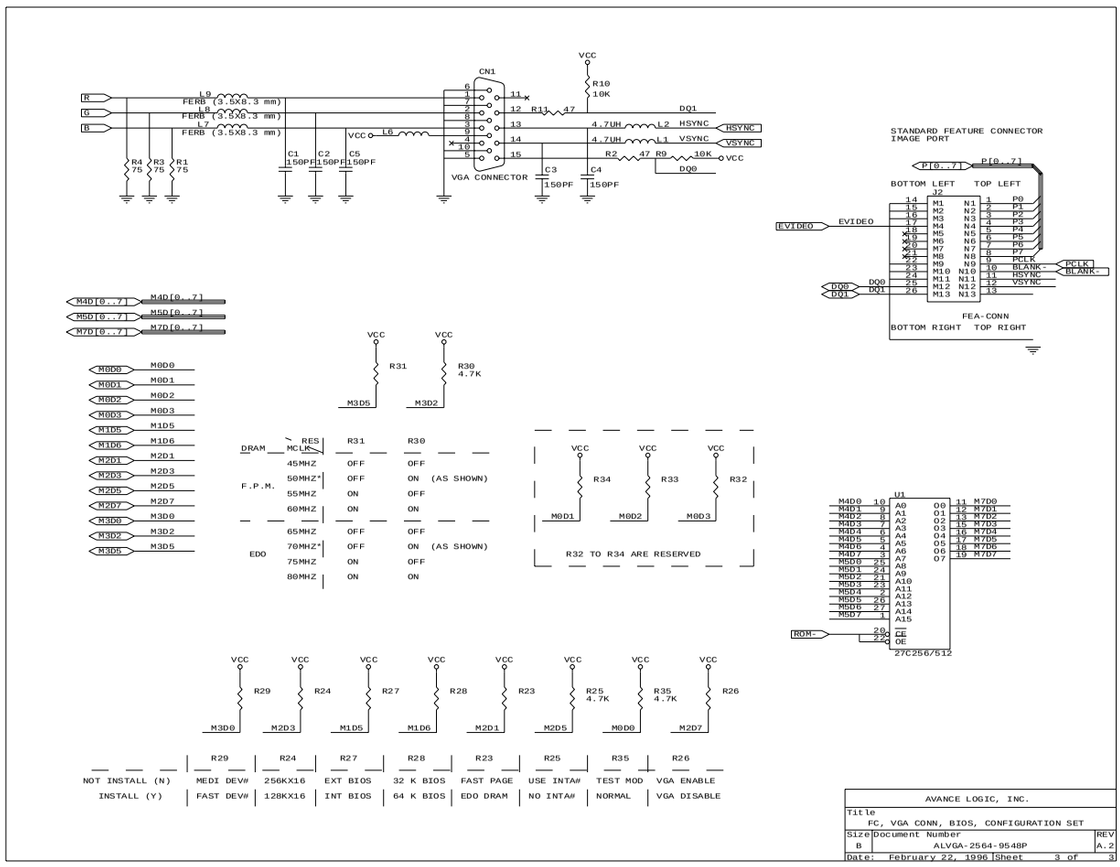
AP9548 Component Layout

AP9548 Block Diagram

AP9548 Schematics




USE 2 CAS DRAM ONLY
AVANCE LOGIC, INC.
Title 2MB 256KX16/128KX16 2CAS DRAM
Size B
Document Number ALV6A-2564-9548P
REV A.2
Date: February 22, 1996 Sheet 2 of 3
256KX16/128KX16
VCC
+3.3V
+12V
-12V


CN1
VCC
R10
10K
R
G
B
L9
L8
L7
FERB (3.5X8.3 mm)
R4
75
R3
75
R1
75
C1
150PF
C2
150PF
C5
150PF
VCC
L6
R11
47
DQ1
4.7UH
L2
HSYNC
4.7UH
L1
VSYNC
R2
47
R9
10K
VCC
DQ0
C3
150PF
C4
150PF
VGA CONNECTOR
STANDARD FEATURE CONNECTOR
IMAGE PORT
P[0..7]
BOTTOM LEFT
TOP LEFT
J2
EVIDEO
PCLK
BLANK-
HSYNC
VSYNC
FEA-CONN
BOTTOM RIGHT
TOP RIGHT
M4D[0..7]
M5D[0..7]
M7D[0..7]
M0D0
M0D1
M0D2
M0D3
M1D5
M1D6
M2D1
M2D3
M2D5
M2D7
M3D0
M3D2
M3D5
R31
R30
4.7K
DRAM
MCLK
RES
F.P.M.
EDO
45MHZ
50MHZ*
55MHZ
60MHZ
65MHZ
70MHZ*
75MHZ
80MHZ
OFF
ON
(AS SHOWN)
R34
R33
R32
R32 TO R34 ARE RESERVED
U1
27C256/512
ROM-
R29
R24
R27
R28
R23
R25
4.7K
R35
4.7K
R26
NOT INSTALL (N)
INSTALL (Y)
MEDI DEV#
FAST DEV#
256KX16
128KX16
EXT BIOS
INT BIOS
32 K BIOS
64 K BIOS
FAST PAGE
EDO DRAM
USE INTA#
NO INTA#
TEST MOD
NORMAL
VGA ENABLE
VGA DISABLE
AVANCE LOGIC, INC.
Title
FC, VGA CONN, BIOS, CONFIGURATION SET
Size
B
Document Number
ALVGA-2564-9548P
REV
A.2
Date: February 22, 1996 Sheet 3 of 3

AP9548 Bill of Materials

ALG2564 PCI Interface
ALVGA-2564-9548P

Revised: February 22 1996
Revision: A. 2

Bill of Materials

ITEM	QUANTITY	REFERENCE	PART	DESCRIPTION
1a	1	U1	27C256/512	28-pin 600mil DIP socket
1b	1	U1	27C256/512-150	150ns 32KX8 DIP EPROM
2	1	U2	ALG2564	208-pin PQFP
3a	2	U5 U6	256KX16 256KX16	256KX16-70 FPM/EDO DRAM SOJ package
3b	2	U3 U4	256KX16 256KX16	40-pin DRAM SOJ socket
4	3	R1 R3 R4	75	75 ohm 0805 SMD res
5	2	R2 R11	47 47	47 ohm 0805 SMD res
6	1	R5	0	0 ohm 0805 SMD res
7	7	R6 R7 R15 R17 R20 R21 R22	22 22 22 22 22 22 22	22 ohm 0805 SMD res
8	1	R8	110	110 ohm 0805 SMD res

Bill of Materials

ITEM	QUANTITY	REFERENCE	PART	DESCRIPTION
9	2	R9 R10	10K 10K	10K ohm 0805 SMD res
10	6	R12 R13 R23* R25* R30% R35	4.7K 4.7K 4.7K 4.7K 4.7K 4.7K	4.7K ohm 0805 SMD res
11	2	RN1 RN2	33X4 33x4	33 ohm 8-pin SIP ISO res net
12	27	BC1thru BC23 C7 C8 C10 C11	.1UF .1UF .1UF .1UF .1UF	.1uF 0805 SMDcap
13	5	C1 thru C5	150PF	150pF 0805 SMD cap
14	2	C9 C15	820PF 820PF	820pF 0805 SMD cap
15	2	C16 C17	100PF 100PF	100pF 0805 SMD cap
16	11	FC1 THRU FC8 C12-C14	10UF 10UF	10uF 16V thru-hole cap
17	2	D1 D2	4. 3V	4. 3V .5W thru-hole zener diode
18	5	L1 thru L5	4. 7UH	4. 7uH thru-hole ind
19	3	L7 thru L9	FERB(3.5X8 .3mm)	ferrite bead

Bill of Materials

ITEM	QUANTITY	REFERENCE	PART	DESCRIPTION
20	1	CN1	VGA CONNEC-TOR	15-pin D-sub VGA con-nector
21	1	J2	FEA-CONN	13X2 dual row straight header
22	1	Y1	14.318MHz	14.31818MHz serial crys-tal

Note:
Revised History:
% DRAM timing definition:

DRAM	RESISTOR MLCK	R31	R30
FPM	45MHz 50MHz 55MHz 60MHz	OFF OFF ON ON	OFF ON (as shown) OFF ON
EDO	65MHz 70MHz 75MHz 80MHz	OFF OFF ON ON	OFF ON (as shown) OFF ON

*Configuration resistor definition:

RESISTOR	NOT INSTALL	INSTALL
R23	F.P.M.	EDO DRAM
R24	256KX16	128KX16
R25	USE INTA-	NO INTA-
R26	VGA ENABLE	VGA DISABLE
R27	EXT BIOS	INT BIOS
R28	32K BIOS	64K BIOS
R29	MEDI DEV	FAST DEV-

AP9548 Part Descriptions

Item	Description	Part Number	Vendor
2	Multimedia accelerator	ALG2564	Avance Logic, Inc.
3a	256k x 16 - 70 FPM/EDO DRAM SOJ package	4C16257	Note 1
3b	40-pin DRAM SOJ socket	SOJ-040-P	PDI
1a	28-pin 600 mil DIP socket	2-641605-5	AMP
1b	150 ns 32k x 8 DIP EPROM	27C256/512-150	AMD
4-10	0805 SMD resistor	Note 3	
11	8-pin SIP ISO resistor network	Note 4	
12-15	0805 SMD capacitor	Note 5	
16	16 V thru-hole capacitor	Note 6	
17	4.3 V .5 W thru-hole zener diode	IN5229B	Motorola/BKC
18	4.7 µH thru-hole inductor	TPF0410-4R7K	TDK
19	3.5 x 8.3 mm ferrite bead	2743001111	Fair-Rite
20	15-pin D-sub VGA connector	CNT-163-00	Actron
21	13 x 2 dual row straight header	10-89-2261	Molex
22	14.31818 MHz series crystal	FOX143	Fox

Notes:

1. Obtain a DRAM compatibility list from Avance Logic, Inc.
2. Except for Item 1, equivalent parts may be substituted for all items.
3. 1/10 W, 5%, 150 V
4. 3/4 W, 100 V
5. ±5%, 50 V
6. ±20%, 16 V

Chapter 6

Unified Memory Architecture

Introduction

Unified Memory Architecture (UMA) is a method by which the host's main memory can be shared by another device. By removing the need for a dedicated memory for a device, the overall system cost is reduced. The ALG2564 is designed to meet the UMA standard for sharing the host's main memory and to also function with a dedicated memory.

This chapter describes how the ALG2564 complies with the UMA standard and interfaces to the host's main memory in a shared main memory application. For this description, the ALG2564 is referred to as the graphics controller and the portion of main memory used by the graphics controller is referred to as the frame buffer.

Graphics Controller Pin Definitions

The following ALG2564 I/O pins are used to implement the VUMA function. See “I/O Pins Diagram” on page 2 - 12 for the pin numbers.

Pin Name	Type	Description
REQ0-	O	Memory Bus Request Bit 0
REQ1-	O	Memory Bus Request Bit 1
GNT-	I	Memory Bus Grant
MA0-9	O	Multiplexed Memory Address Bits 0-9
M0-7D0-7	I/O	Memory Data Bits 0-63
RAS-	O	Row Address Strobe
CAS0-7-	O	Column Address Strobe A Bits 0-7
WE-	O	Write Enable
OE-	O	Output Enable

Request Priority Definitions

Graphics Controller Request Priority Levels

- High priority
  - Screen refresh
- Medium priority
  - Graphics controller write
  - PCI write
  - PCI read
- Low priority
  - Graphics controller read
- No Request

Host Memory Controller Priority Levels

- High priority
  - DRAM pending refresh full
  - CPU cache read miss
  - PCI read
- Medium priority
  - CPU post write FIFO not empty
  - PCI post write FIFO not empty
- Low priority
  - DRAM refresh

Arbitration

Since the host memory controller and the graphics controller share the host's main memory through a common memory bus and the memory bus can only have one master at a time, there must be arbitration for its use. There are two arbitration schemes, one with multiple priority levels and one with a single priority level. Arbitration is accomplished with three signals. For the multiple priority levels scheme, the two bits of the request signal (REQ0- and REQ1-) from the graphics controller are used to indicate a request for mastery of the memory bus and the priority level of that request. For the single priority level scheme, only one bit of the request signal (REQ1-) is used to indicate a request for mastery of the memory bus. The other two signals are the grant signal (GNT-) from the host memory controller that indicates that the request for mastery of the memory bus from the graphics controller is granted, and the clock signal (SCLK) from the CPU that synchronizes the request and the grant signals.

Multiple Priority Levels

Request Priority Level Decode

REQ1-	REQ0-	Priority Level
0	0	High
0	1	Medium
1	0	Low
1	1	No Request

The current memory bus master is preempted and the other controller becomes the master if the other controller's request has a higher priority than that of the current master. See the above table for the decode of the priority levels for the graphics controller. If the other controller's request is of the same priority level as that of the current master and:

- The other controller is the graphics controller, then the graphics controller becomes the master, even if the current master is the host memory controller.
- The current master is the graphics controller, then the graphics controller remains the master, even if the other controller is the host memory controller.

With no request active, the memory bus parks with the current master until a request is made active by either the current master or the other controller.

The worst case delay for a high priority level request is 500 ns. There is no maximum delay for medium and low priority level requests.

The worst case preemption delay for the graphics controller is 100 ns.

Single Priority Level

The graphics controller makes REQ1- active when it has a high or medium priority request. The host memory controller makes GNT- active in response and the graphic controller becomes the current master of the memory bus. The host memory controller can preempt the graphics controller and become the current master of the memory bus if it has a high or medium priority request and the graphics controller has been the current master for more than 500 ns or REQ1- is no longer active.

With no request active, the memory bus parks with the current master until a request is made active by either the current master or the other controller.

The worst case delay for a high or medium priority level request is 500 ns.

The worst case preemption delay for the graphics controller is 500 ns.

Using the Memory Bus

Graphics Controller

When the host memory controller makes GNT- active, the graphics controller becomes the current master of the memory bus. The graphics controller then puts the memory row address on MA0-9, waits two or three memory clock cycles (row address strobe precharge time), and then makes RAS- or active to start the page cycle. If RAS- was inactive for three or four memory clock cycles prior to the time it was to be made active, the row address strobe precharge time can be eliminated. To complete the page cycle, the graphics controller puts the memory column address on MA0-9, makes CASn- active (where n is the appropriate byte), and then makes WE- active to write the contents of M0-7D0-7 (memory data bits 0-63) into the frame buffer.

Release the memory bus when -GNT is inactive

- If RAS- is inactive, the graphics controller applies the tri-state condition to the M0-7D0-7 signal lines.
- If -RAS is active, the graphics controller completes the page cycle, makes RAS-, CAS07-, and WE- inactive for one memory clock cycle, and then applies the tri-state condition to the M0-7D0-7 signal lines.

Memory Row and Column Addresses

Memory Address Bit	Row	Column
MA9	A21	A22
MA8	A20	A11
MA7	A19	A10
MA6	A18	A9
MA5	A17	A8
MA4	A16	A7
MA3	A15	A6
MA2	A14	A5
MA1	A13	A4
MA0	A12	A3

The addresses for the first four megabytes of main memory are A21 through A0. Addresses A19, A20, A21, and A22 are made active for the 1, 2, or 4 megabytes of main memory used by the graphics controller as the frame buffer.

Host Memory Controller

For the host memory controller to become the current master, it makes an internal signal active, makes GNT- inactive, and waits two CPU clock cycles. If at this time the internal signal made active earlier has been active for three CPU clock cycles, the host memory controller then becomes the current master, waits one CPU clock cycle, then makes RAS- active to start the page cycle.

Release the memory bus

- If RAS- is inactive, the host memory controller applies the tri-state condition to the M0-7D0-7 signal lines and makes GNT- active.
- If RAS- is active, the host memory controller completes the page cycle, makes RAS-, CASn-, and WE-, inactive, waits one CPU clock cycle, applies the tri-state condition to the M0-7D0-7 signal lines, and makes GNT- active.

Refresh the memory

The host memory controller must refresh both the system memory and the frame buffer portions of main memory. When sharing main memory, the graphics controller turns off its DRAM refresh request function.

When the host memory controller releases the memory bus to the graphics controller, it must either make all of the non-shared memory signals inactive or apply the inactive tri-state condition to them with external pull up resistors.

Map the frame buffer into main memory

The frame buffer is allocated from the top of the shared bank of memory. Since the graphics controller only uses MA0-9, MA10 and higher must only be used for byte address 23 and higher.

The shared bank must always be above the other memory banks.

The memory reserved for the frame buffer must be mapped outside of the normal system memory address range.

Access the frame buffer through the host memory controller

For the highest performance, the CPU must be able to access the frame buffer in both a cacheable address window and in a non-cacheable address window. If accessing the frame buffer in a cacheable window, the graphics data coherence between the CPU and the graphics controller must be managed by software.

Two access windows can use alias based addresses of the original memory map by using the additional byte addresses A31 and A30.

A31	A30	Definition
0	0	System memory is cacheable, disable the frame buffer.
0	1	System memory and frame buffer are cacheable.
1	0	System memory and frame buffer are non-cacheable.
1	1	Reserved for system BIOS.

The order of the byte addresses to the DRAM row and column addresses needs to be programmed to match the order used by the graphics controller.

Synchronize the request lines for multiple level support

The REQ0- and REQ1- signals from the graphics controller must be synchronized to the CPU clock by the host memory controller. When synchronized and stable for two CPU clock cycles, the host memory controller uses these signals as the valid request signals. This two CPU clock cycle delay allows multiple signals (such as REQ0- and REQ1-) to synchronize from one time base (memory clock) to another time base (CPU clock).

Power on configuration

M0-5D0-7 (memory data bits 0-47) are used for the graphics controller power on value. The host memory controller must not depend on the level of these pins during power on.

The graphics controller samples GNT- during reset. If the host memory controller uses any memory control signals for its power on configuration, it must make GNT- inactive during reset.