TGUI9420DGi PRELIMINARY DATA SHEET

Trident

TGUI9420DGi
INTEGRATED GUI ACCELERATOR

Features

- Hardware acceleration of BitBLTs, line drawing, short stroke vectors, rectangle fills, text transfer and color expansion
- Integrated 24-bit true color DAC
- Integrated 80 MHz programmable clock synthesizer
- Internal hardware cursor
- Pin-compatible with TGUI9400CXi and TVGA9200CXr
- Direct connection to 32-bit VL-Bus (up to 50 MHz)
- "Glueless" connection to PCI rev. 2.0 (33 MHz)
- Supports VESA Display Power Management Signaling
- Feature conector support with VESA palette snooping
- Flexible DRAM configurations: 256Kx4/8/16 and 512Kx8
- Command FIFO
- Supports high resolution including 1280x1024x8, 1024x768x8, 800x600x16/15 and 640x480x24
- 512 KB, 1 MB or 2 MB DRAM design
- Linear addressing up to 64 MB
- Programmable DRAM timing
- Extended text modes: 8/132 columns by 25/30/43/60 rows
- Register level compatible with VGA, EGA and MDA
- 208-pin PQFP package

General Description

The TGUI9420DGi is a high performance DRAM-based Graphical User Interface (GUI) accelerator that combines Trident's proven VGA technology with a 32-bit frame buffer interface, fixed function graphics engine, 24-bit true color DAC and a dual clock synthesizer. The TGUI9420DGi is an ideal solution for mid-range PCs running Microsoft Windows™, Windows NT™, IBM OS/2™ and other graphic interfaces.

The TGUI9420DGi extends the performance range of the TGUI9400CXi and the TVGA9200CXr product family by offering a pin-compatible upgrade path. The TGUI9420DGi is fully compliant with the PCI Rev. 2 and the VL-Bus 2.0 specifications.

The TGUI9420DGi significantly boosts graphics performance through hardware acceleration of the most frequently used GUI operations including: BitBLTs, line drawing, rectangle fills, text transfer, color expansion and hardware cursor support.

Graphics system throughput is further enhanced by a command FIFO that allows maximum bus transfer speed for applications such as Windows™ or AutoCAD™ that directly access video memory. Additionally, 32-bit linear addressing improves main memory access speed by increasing the size of the data segment that can be read, reducing DRAM precharge and bank switch time. Linear addressing can reference any location in the first 64 MB of main memory.

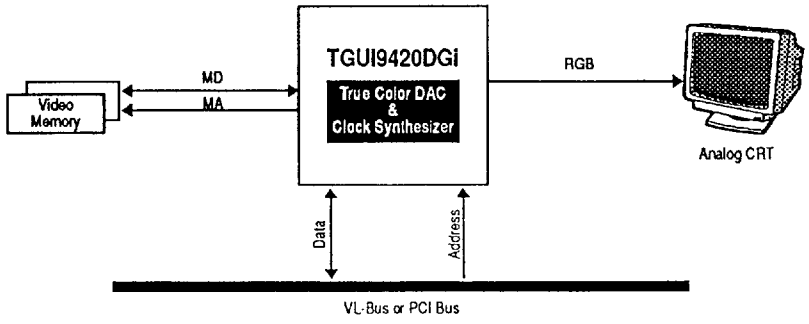

Figure 1. TGUI9420DGi Application Diagram

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The integrated dual clock sythesizer and 24-bit DAC supports resolutions up to 1280x1024x8, 1024x768x8 at 72 Hz refresh, 800x600x15/16 and 640x480x24.

The TGUI9420DGi supports a standard feature connector and is multimedia-ready with built-in palette snooping.

The TGUI9420DGi supports the VESA Display Power Management Signaling (DPMS) specification to decrease energy consumption when the chip is in a temporary idle state. HSYNC and VSYNC control built into the TGUI9420DGi allows DPMS powerdown to occur at the user defined intervals with the included Utility Software. The TGUI9420DGi fully complies with the Environmental Protection Agency's (EPA's) Energy Star campaign.

The TGUI9420DGi's integrated clock synthesizer supplies selectable VCLK frequencies up to 80 MHz and programmable DMCLK frequencies. The integrated triple 8-bit video DAC supports a true color (24-bits/pixel) mode, high color (16- and 15-bit/pixel) modes and includes a 256x18 color look up table for pseudo-color (4- or 8-bit/pixel) mode. The integrated clock synthesizer and DAC combined with the integrated data bus transceivers and feature connector support means that a complete video subsystem solution can be acheived by adding only DRAM.

Compatibility

The TGUI9420DGi is fully compatible with all standard IBM VGA modes and EGA modes, and supports:

- Use of application software that runs in any of the above modes
- Emulation of EGA modes on a VGA monitor

Support is also provided in Trident's standard BIOS for VESA modes. Additionally, the TGUI9420DGi is compatible with VESA palette snooping and Display Power Management Signaling (DPMS).

Extended Graphics and Text Modes

The TGUI9420DGi supports extended text modes of 80-column text with 30, 43, and 60 rows; and 132-column text with 25, 30, 43, and 60 rows.

The extended graphics modes supported by the TGUI9420DGi are outlined in Table 1.

Table 1. Graphics Modes Cross Reference

Resolution	Color Depth Bit	Refresh Rate Hz/I/NI	Min. Memory Required
640x480	4	60NI	512 KB
640x480	4	75NI	512 KB
640x480	8	60NI	512 KB
640x480	8	75NI	512 KB
640x480	15/16	60NI	1 MB
640x480	15/16	75NI	1 MB
640x480	24	60NI	1 MB
640x480	24	75NI	1 MB
800x600	4	60NI	512 KB
800x600	4	75NI	512 KB
800x600	8	60NI	512 KB
800x600	8	75NI	512 KB
800x600	8	60NI	1 MB
800x600	8	75NI	1 MB
800x600	15/16	60NI	1 MB
800x600	15/16	75NI	1 MB
800x600	15/16	60NI	2 MB
800x600	15/16	75NI	2 MB
1024x768	4	60NI	512 KB
1024x768	4	75NI	512 KB
1024x768	8	60NI	1 MB
1024x768	8	75NI	1 MB
1280x1024	4	43I	1 MB
1280x1024	4	60NI	1 MB
1280x1024	8	43I	2 MB
1280x1024	8	60NI	2 MB

TGUI9420DGi Components

The TGUI9420DGi consists of eleven major components: GUI Engine, Sequencer, CRT Controller, Graphics Controller, Attribute Controller, DAC, Clock Synthesizer, Host Bus Interface, Display Memory Bus Interface, Command FIFO and Read cache. These components are used to generate video output and timing for video memory and the monitor. Refer to Figure 2 below for block diagram. A summary of each component function follows.

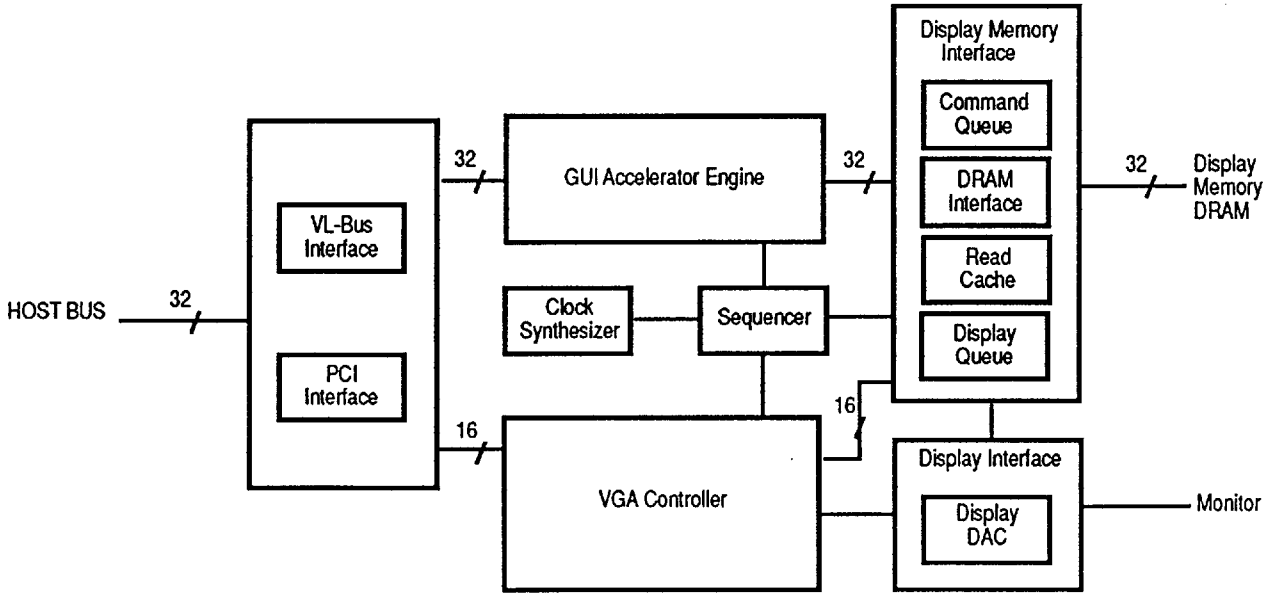


Figure 2. TGUI9420DGi Block Diagram

GUI Functions

The Graphics Engine provides a set of hardware functions specifically designed to accelerate Graphical User Interfaces (GUIs) such as Microsoft Windows, IBM OS/2 PM, and the X-Windowing System. The most common GUI operations involve opening new windows on the display or moving windows within the display. Image Transfer and BitBLT are the graphics functions used to implement these operations. Hardware acceleration of these functions greatly improves GUI performance.

A basic discussion of each of the TGUI9420DGi functional blocks is given below:

Graphics Engine

The Graphics Engine is a key to the high performance of the TGUI9420DGi. Implementation of the Graphics Engine boosts performance in three ways:

First, specialized drawing hardware performs the graphics functions much faster than software algorithms, even on todays high speed CPUs. Second, the data transfer rate has been increased in several ways. In most systems, the CPU must transfer all the display data to the graphics subsystem across a bus (usually ISA, Micro Channel or direct local CPU bus), which in turn, transfers the data into the display memory. Since the CPU now has only to calculate the setup information for each operation, only these few bytes must be transferred across the system bus. In addition, the data transfer rate to the display memory is much faster, as discussed in the Display Memory Interface Unit section. Third, a degree of parallelism has been achieved. In SVGA systems, the CPU must calculate every pixel to be drawn or moved. In this case, the CPU is free to proceed to the next task while the TGUI9420DGi performs the graphics operation. The enhanced functions implemented in the Graphics Engine are summarized here:

BitBLT

BitBLT is one of the most important operations in accelerating Windows performance. Whenever a new window is opened on the display, or an existing window is moved within the display, a large amount of pixel information must be moved. BitBLT is the operation which moves blocks of data within display memory. Hardware acceleration of BitBLT directly improves Windows performance.

Several types of BitBLT are provided. Pixel Block Transfer moves pixel data from a source block on the screen to a destination block on the screen. In this case, the source and destination block widths and heights are the same. Another version of BitBLT is the Pattern Block Transfer with Variable Size Source. This operation transfers pixel data from a source block to a destination block on the screen. When used as a pattern map, the source map is typically smaller than the destination map. The source data is repetitively used to fill the destination block. Still another version of BitBLT is the Color Expanded Block Transfer, in which a 1 bit per pixel source block is converted into 16, 256, or 64K color (4 , 8 or 16 bits per pixel respectively) data and used to fill a destination block on the screen. Each bit of the monochrome image is expanded into 4, 8 or 16 bits according to the foreground and background colors.

In all cases, raster operations may be performed between the new pixel data and the destination block old pixel data.

Area Fill

This operation is most commonly used to fill in the background color for windows or the general screen area behind a window. Since a large screen area is usually being filled, hardware Area Fill is an important feature in improving Windows performance.

This operation fills a destination block area in display memory with either a solid color or a two color style pattern. The style pattern is held in a 16-bit style pattern register. Pixel colors are defined by the foreground and background color registers. Raster operations may be performed between the new pixel data and the destination block old pixel data.

Line Draw

Line drawing is most commonly used in CAD and desktop publishing applications. Complex drawings can be composed of a large number of lines. Speeding up line drawing primarily improves performance of "redraw" functions, which are used to move or rotate images.

This operation draws a straight line of any slope in display memory. The line may be either a solid color or a two color style pattern. The colors are defined by the foreground and background color registers. The style pattern is held in a 16-bit style pattern register. Raster operations may be performed between the new pixel data and the destination block old pixel data.

Image and Text Transfer from the CPU

A new window is opened on the screen by transferring the display data from system memory to display memory. Just as in the Pixel BLT, hardware acceleration allows GUI environments to quickly open new windows. Text is written to the screen with the Text Transfer operation, which is used to move font data from system memory to the display.

Image Transfer is similar to the Pixel Block Transfer and Text Transfer is similar to the Color Expanded Block Transfer. In both cases the source pixel data comes from the CPU rather than the Graphics Engine.

Short Stroke Vector Draw

This operation is another version of Line Drawing and is used in a similar way.

Short Stroke Vectors are straight lines drawn in one of the eight octants. Each line is defined only by its direction and length, and may be either a solid color or a two color style pattern. Raster operations may be performed between the new pixel data and the destination block old pixel data. Short Stroke Vector Draw is particularly useful in MCAD applications.

Hardware Cursor

Cursor performance is improved by this operation by eliminating the software and CPU load overhead associated with manipulating the cursor. Cursor movement is one of the most interactive and noticeable operations in a windowing environment. The hardware cursor provides an enhanced "look and feel", as well as performance gain.

The hardware cursor is a 64x64 pixel image stored in packed pixel format in an off screen area of display memory. The pattern is stored at 2-bits per pixel, allowing each pixel in the displayed cursor to assume one of four values: Cursor Color 0 or Cursor Color 1 (as defined in the cursor color registers), Transparent (the underlying pixel color is displayed), or Complement (the "ones" complement of the underlying pixel color is displayed).

Cursor positioning on the active display area is defined by vertical and horizontal position registers. When active, the cursor is automatically overlaid at the correct position in the display.

Sequencer

The sequencer provides basic memory timing for the DRAM interface, and a character clock for the CRTC and for controlling regenerative memory fetch. The sequencer uses a 64 byte video cache to let the CPU access display memory during active display intervals. Video data from the cache can be output to the video screen while the CPU accesses video memory. This greatly increases performance over standard implementations for CPU access.

CRT Controller

The CRT (Cathode Ray Tube) Controller provides complete control for horizontal and vertical synchronous timing, address interface between video memory and display screen, cursor and underline timing, and refresh addressing for dynamic RAMs.

Graphics Controller

During the active display interval, the Graphics Controller directs data from video memory to the Attribute Controller. In graphics modes, memory data is formatted into serialized form and sent to the Attribute Controller. In text mode, the parallel attribute byte goes directly to the Attribute Controller without going through the Graphics Controller. During video memory read/write operations, the Graphics Controller acts as an interface to the CPU. The Graphics Controller can perform logic operations on memory data before it reaches the display memory or system data bus.

Attribute Controller

The Attribute Controller takes in data from video memory and formats it for output on the display monitor. In addition, the Attribute Controller takes care of blinking, underlining, cursor insertion, and PEL panning. In text mode, 16 bits of code are divided into 8 bits of character code and 8 bits of attribute code. The character code is used as a look-up into a font table. The attribute code is used to determine character color, blinking, bold, etc. In graphics mode, the Graphics Controller serializes memory bits. Each output color is translated through the internal color palettes and then sent to the DAC. Here it is used as an address to the 18/24-bit color look-up table. The value read from the color look-up table is converted into three analog signals (R, G, B) for driving an analog display.

DAC

The integrated true color DAC provides support for 640x480-16, 256, 32K, 64K, and 16M color modes, 800x600-16, 256, 32K, and 64K color modes, 1024x768-16 and 256 color modes, and 1280x1024-16 and 256 color modes. For pseudo-color mode, 16 or 256 colors can be selected out of a total of 256K or 16M color palette. Bypass versions of true color and 15/16-bit pixel modes are available. The DAC module outputs RGB analog signals to directly drive an analog VGA or Super VGA monitor.

Clock Synthesizer

The Clock Synthesizer module is powered by an external 14.318 MHz quartz crystal or oscillator. The integrated Clock Synthesizer provides 16 selectable video frequencies up to 80 MHz. The Clock Synthesizer also provides 16 selectable DRAM clock frequencies. The frequencies may be programmed by BIOS or by direct access to internal chip registers.

Host Bus Interface

The TGUI9420DGi directly supports VL-Bus and PCI bus interfaces. Both interfaces are 32-bits wide and require no glue logic. VL-Bus speeds up to 50 MHz are supported. PCI bus speeds up to 33 MHz are supported.

The TGUI9420DGi's VL-Bus interface offers bus transfer protocols for bus speeds less that or equal to 33 MHz and bus speeds greater than 33 MHz. BIOS may be run over the ISA bus for peripheral solutions, or be integrated into system ROM for motherboard solutions.

The TGUI9420DGi's PCI bus interface supports standard memory read/write cycles, I/O read/write cycles, and configuration read/write cycles. For peripheral solutions, BIOS may be run over a dedicated bus attached to the TGUI9420DGi. For motherboard solutions, the BIOS may be integrated into system ROM.

Display Memory Bus Interface

The TGUI9420DGi can address up to 2 MB of DRAM. The memory data bus interface is 16 or 32-bits wide. Fast Page Mode access cycles are used whenever possible to maximize bandwidth. Display memory is divided up into two banks. Configurations of 256Kx4, 256Kx8, 256Kx16, 512Kx4 and 512Kx8 DRAM are supported. Nineteen address pins and RAS, CAS and WE signals are used to control memory data access. Address pins MAA8-MAA0 are used for memory Bank A, address pins MAB8-MAB0 for memory Bank B, and MA9 is used for 512Kx4 and 512Kx8, configurations.

Memory data bits RMD6, RMD5 configure the memory data bus width. Various memory data bits select DRAM type and configuration. MD31 and MD30 can be used to configure for "non-conforming" 512Kx4 DRAM. MD28 defines pins 153,143,130, and 120 as WE or CAS. MD19-MD18 select base DRAM configuration (512K, 1 MB, 2 MB) and type. Reference Table 1 for additional information.

The TGUI9420DGi also allows programmable DRAM timing. Programmable DRAM timing provides added flexibility to the DRAM interface. Designers may configure the DRAM timing to support slower speed DRAM and achieve a cost saving solution. Programmable DRAM timing is controlled through bits 3-0 of the DRAM Timing register (3x5.23). An additional State Machine clock may be inserted for CAS active and for CAS precharge. Up to 3 additional State Machine clocks may be inserted for RAS precharge. Linear addressing of up to 2 MB of video memory is supported. The base address for the linear addressing windows may be set anywhere in a 64 MB linear memory space. The TGUI9420DGi allows a linear addressing window and the standard VGA memory space to be active at the same time. This allows great flexibility in adapting non-linear addressed drivers to the linear addressing environment.

VGA Core

The high performance Super VGA core provides full hardware level VGA and EGA compatibility. At reset, the TGUI9420DGi is in hardware level VGA mode. All of the standard VGA subsections (Sequencer, Graphics Controller, Attribute Controller, etc.) are implemented.

Vertical refresh rates up to 72 Hz at 800x600 and 70 Hz at 1024x768 are supported.
Extended text modes of 80 columns with 30, 43, or 60 rows, and 132 columns with 25, 30, 43, or 60 rows are supported.

Command FIFO

The FIFO enhances memory write performance. CPU write data can be loaded to the FIFO, eliminating the CPU's need to wait while the memory is busy with other tasks. When the memory bus is available, data is written into memory from the FIFO.

TGUI9420DGi Applications

The TGUI9420DGi works with your hardware to allow you to develop a high performance, integrated video subsystem. The small footprint design is ideal for motherboard applications and high performance add-on cards.

A minimum 512K Byte add on board configuration requires a TGUI9420DGi, four 256Kx4 DRAM chips, 32 KB EPROM and one TTL (VL-Bus solutions only).

A minimum 1 MB motherboard VGA system requires only three ICs for a complete VL-Bus or PCI solution. Only one TGUI9420DGi and two 256Kx16 DRAM chips are required.

Software Drivers Supported

Extended graphics and text modes are supported by software application drivers developed by Trident. The TGUI9420DGi supports the following applications:

- AutoCAD
- Autoshade
- CADKEY
- Framework
- GEM
- Lotus
- MS Word
- MS NT™
- MS Windows™
- OS/2
- P-CAD
- Quattro Pro
- Symphony
- Ventura
- VersaCAD
- Wordstar
- WordPerfect
- SCO X-Windows (contact SCO)

Contact Trident for the latest releases of high-resolution software.

MD and RMD Definitions at System Reset

Tables 2, 3, and 4 list the definitions for MD31-MD13, MD7-MD0 and RMD7-RMD0 at system reset.

Table 2. MD31-MD13 Definitions

MD	Logic Value[1]	Definition
MD31	0	For "non-conforming" 512Kx4 DRAM (MA9 forced to logical 0)
	1	For "non-conforming" 512Kx4 DRAM (MA9 forced to logical 1)
MD30	0	Selects "non-conforming" 512Kx4 DRAM
	1	Selects standard DRAM
MD29	-	Reserved
MD28	0	Pins $\overline{WE3}$-$\overline{WE0}$ defined as $\overline{CASA3}$-$\overline{CASA0}$
	1	Default
MD27-MD24	-	Reserved
MD23	0	Enables PCI configuration registers
	1	Disables PCI configuration registers
MD22	0	Tied to ground
MD21	0	Selects PCI Bus
	1	Selects VL-Bus
MD20	0	Selects 1x clock as VL-Bus time base
	1	Selects 2x clock as VL-Bus time base
MD19-MD18	00	Supports 256Kx16 DRAM configurations. Pin 134 is used as MA9 for asymmetric DRAM case
	01	Supports 512Kx4 or 512Kx8 DRAM. Pin 134 used as MA9.
	10	Supports 2 MB 256Kx4 or 256Kx8 DRAM. Pin 134 is used as $\overline{MCASB}$.
	11	Supports 256Kx4 or 256Kx8 DRAM up to 1 MB. Also supports up to 2 MB 256Kx16 DRAM. Pin 134 is used as $\overline{NMI}$.
standard		
MD17	-	Reserved
MD16	-	Reserved
MD15	-	Reserved
MD14-MD13	-	Reserved

[1]Set a logical 0 value by pulling-down to GND through 4.7K-10K resistor. No pull-up resistor required for a Logical 1 value.

Table 3. MD7-MD0 Definitions

MD	Logic Value[1]	Definition
MD7	0	8-bit BIOS
	1	16-bit BIOS
MD6	0	ROM on ISA Bus (VL-Bus only) or in motherboard BIOS (VL-Bus or PCI Bus)
	1	ROM on RMD bus (PCI Bus only)
MD5	-	Reserved
MD4	-	Reserved
MD3	0	Add two extra State Machine clocks to $\overline{RAS}$ precharge
	1	Standard DRAM interface
MD2	0	Selects 1024x768-16, 256 color interlaced and 800x600-16, 256 at 56 Hz
	1	Selects 1024x768-16, 256 non-interlaced and 800x600-16, 256 at 72 Hz
MD1	-	General purpose MD bit
MD0	0	Graphics mode DMCLK = 75 MHz
	1	Graphics mode DMCLK = 80 MHz

[1]Set a logical 0 value by pulling-down to GND through 4.7K-10K resistor. No pull-up resistor required for a Logical 1 value.

Table 4. RMD7-RMD0 Definitions

MD	Logic Value[1]	Definition
RMD7	1	Reserved
RMD6-RMD5	00	Reserved
	01	Reserved
	10	16-bit DRAM Data bus
	11	32-bit DRAM Data bus
RMD4	-	Reserved
RMD3	0	Selects on-chip clock synthesizer
	1	Selects off-chip clock synthesizer
RMD2	1	Reserved
RMD1	0	Reduced BIOS wait states (for BIOS on RMD Bus)
	1	Standard BIOS wait states (for BIOS on RMD Bus)
RMD0	1	Reserved

[1]Set a logical 0 value by pulling-down to GND through 4.7K-10K resistor. No pull-up resistor required for a Logical 1 value.

PCI Configuration Space

In accordance with the PCI Specification, TGUI9420DGi provides 64 bytes of PCI Configuration space. The register space is byte addressable. A description of the Configuration Register Space and default values for the Configuration registers is provided in Table 5.

Table 5. Configuration Register Space

Register	Type	Size	Offset(h)	Default Value (h)
Vendor ID	Read only	Word	00-01	1023
Device ID	Read only	Word	02-03	9420
Command	Read/Write	Word	04-05	0023
Status	Read/Write	Word	06-07	0000
Revision ID[1]	Read only	Byte	08	73
Class Code	Read only	24 bits (31:8)	09-0B	030000
Memory Base	Read/Write	Double Word	10-13	00000000
ROM Base	Read/Write	Double Word	30-33	00000001

[1]Contents of this register are the same as that of the Chip Version Register (3C5.0B). Reading or writing the Revision ID register will not change selected TGUI9420DGi Special Register definitions (e.g. Old/New Mode Control Register 1) as does reading or writing 3C5.0B.

Reference the TGUI9420DGi Technical Reference Manual for additional discussion of the PCI Configuration Space and a detailed bit level breakdown of the Configuration Space Registers.

Chip Specifications

Table 6. Absolute Maximum Ratings[1]

Parameter	Symbol	Minimum	Typ.	Maximum	Units
Power Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input Voltage	V^{IN}	GND		V_{DD}	V
Operating Temperature	T_{OP}	0		70	°C
Storage Temperature	T_{STO}	-40		100	°C

[1]Stresses above those limits under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

Table 7. DC Specifications

Parameter	Symbol	Minimum	Maximum	Units	Conditions
Input Low Voltage	V_{IL}	GND	0.8	V	V_{DD}=5V
Input High Voltage	V_{IH}	2.0	VDD	V	V_{DD}=5V
Input Low Current	I_{IL}	-	-0.5	µA	V_{IN}=0.0V
Input High Current	I_{IH}	-	20	µA	V_{IN}=V_{DD}
Ouput Low Voltage	V_{OL}	-	0.4	V	See Notes 1, 2
Output High Voltage	V_{OH}	2.4	-	V	See Notes 1, 2
High Impendance Leakage	I_{OZ}	-	10.0	µA	V_{SS}<V_{OUT}<V_{DD}
Supply Current	I_{OC}	-	100.0	mA	V_{DD}=5.25V (V_{DD}MAX.)

Note 1: I_{OL}/I_{OH}(DC)=-4/4MA for RS0/RMAD, RS1/RMA1, $\overline{\text{BLANK}}$, PCLK, CLK0, CLK1/SC3, CLK2/SC1, CLK3/SC2, MC4-MC1

= -6/6MA for MAA8-MAA0, MAB8-MAB0

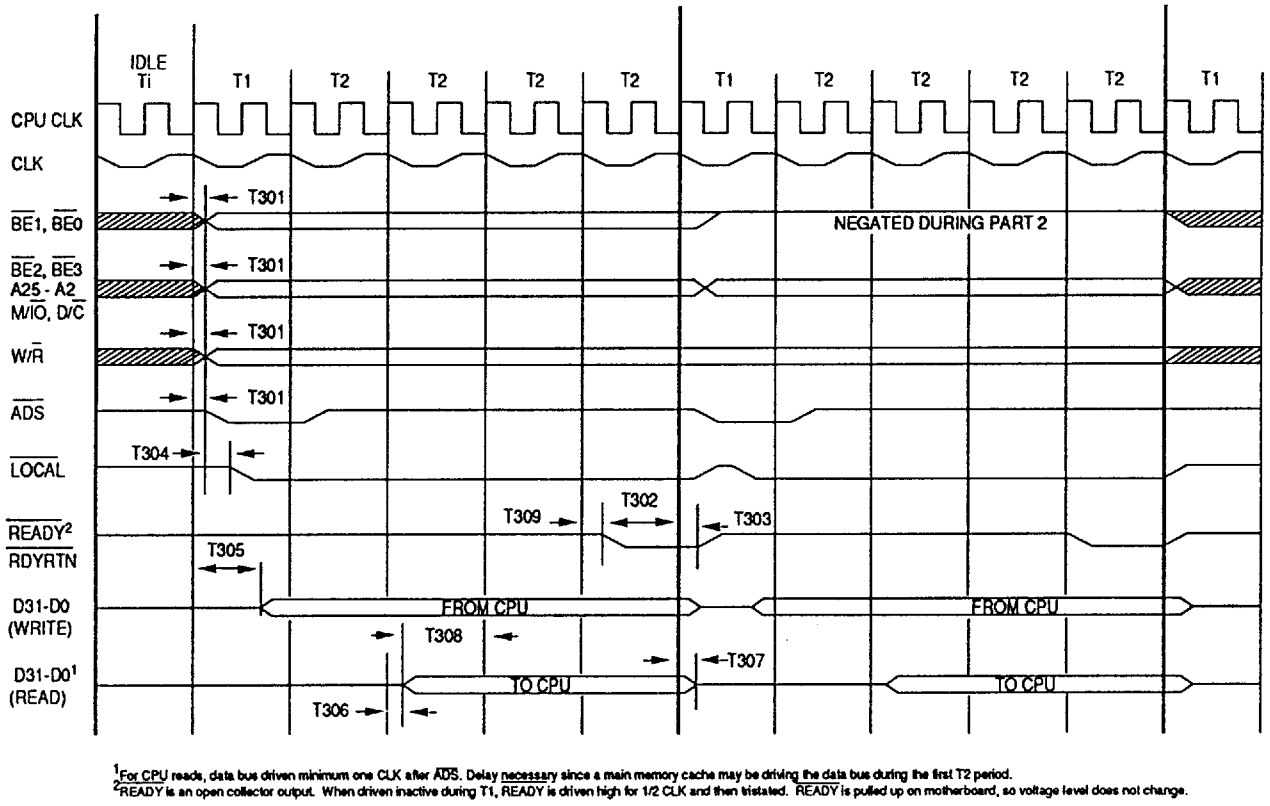
= -8/8MA for RMD7-RMD0, MD31-MD0, $\overline{\text{CASB3}}$-$\overline{\text{CASB0}}$, $\overline{\text{WE3}}$-$\overline{\text{WE0}}$, HSYNC, VSYNC, INTR

= -12/12MA for D31-D0

= -16/16 for $\overline{\text{RAS}}$, $\overline{\text{MCASA}}$, $\overline{\text{LOCAL}}$, $\overline{\text{READY}}$

Note 2: I_{OL}/I_{OH}(AC) specifications for a PCI Bus configuration will be supplied in subsequent releases of this data sheet.

Timing

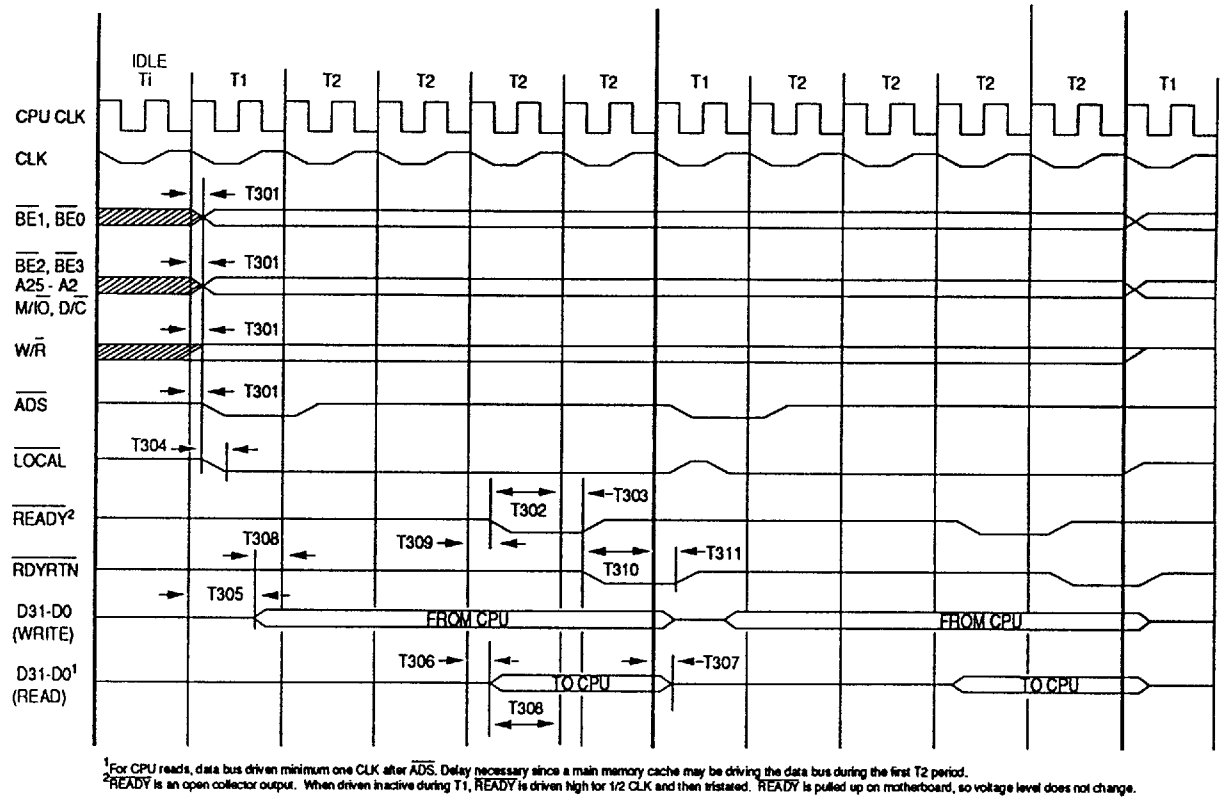


[1]For CPU reads, data bus driven minimum one CLK after ADS. Delay necessary since a main memory cache may be driving the data bus during the first T2 period.
[2]READY is an open collector output. When driven inactive during T1, READY is driven high for 1/2 CLK and then tristated. READY is pulled up on motherboard, so voltage level does not change.

Figure 3. 386DX VL-Bus Timing (33 MHz)

Table 8. 386DX VL-Bus Timing (33 MHz CPU)

SYM	Description	Min (ns)	Max (ns)	SYM	Description	Min (ns)	Max (ns)
Ti	Idle period	30		T304	$\overline{\text{LOCAL}}$ ready to $\overline{\text{ADS}}$ low		20
T1	1st clock period	30		T305	Write data valid delay	7	24
T2	2nd clock period	30		T306	Read data bus drive to		
T301	$\overline{\text{ADS}}$, A25-A2, M/$\overline{\text{IO}}$, D/$\overline{\text{C}}$,				CPU CLK rising edge		5
	$\overline{\text{BE3}}$-$\overline{\text{BE0}}$ valid delay	4	15	T307	Read data hold time	3	
T302	$\overline{\text{READY}}$ setup time	20		T308	Data read/write setup time	5	
T303	$\overline{\text{READY}}$ hold time	4		T309	$\overline{\text{READY}}$ valid delay		10

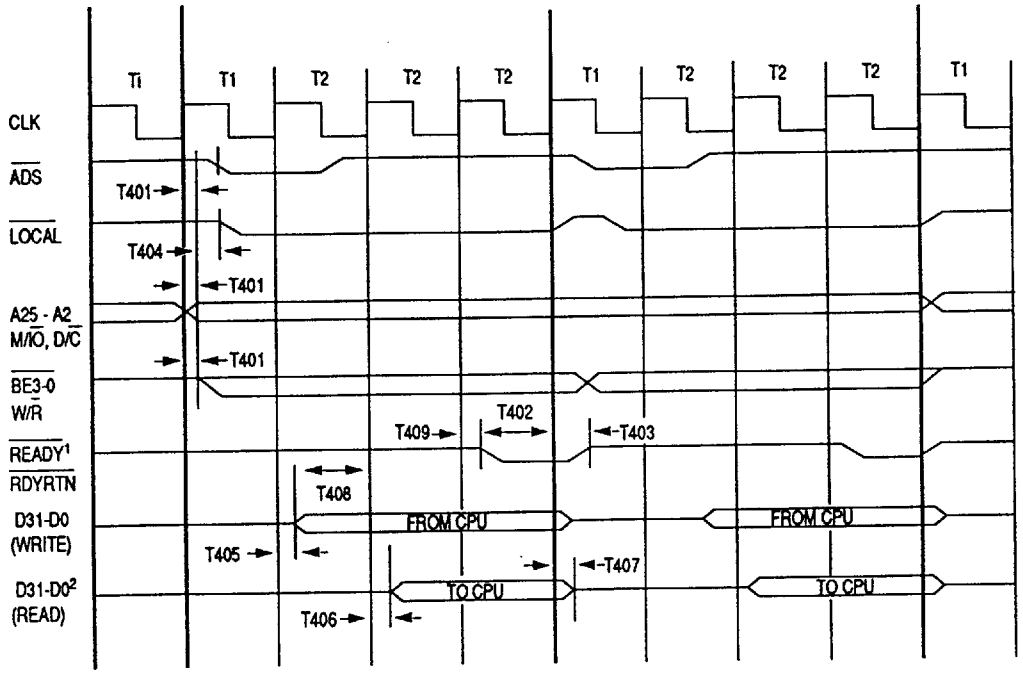


¹For CPU reads, data bus driven minimum one CLK after ADS. Delay necessary since a main memory cache may be driving the data bus during the first T2 period.
²READY is an open collector output. When driven inactive during T1, READY is driven high for 1/2 CLK and then tristated. READY is pulled up on motherboard, so voltage level does not change.

Figure 4. 386DX VL-Bus Timing (40 MHz)

Table 9. 386DX VL-Bus Timing (40 MHz)

SYM	Description	Min (ns)	Max (ns)	SYM	Description	Min (ns)	Max (ns)
Ti	Idle period	25		T306	Read data bus drive to CPU CLK rising edge		5
T1	1st clock period	25		T307	Read data hold time	3	
T2	2nd clock period	25		T308	Data read setup time	5	
T301	ADS, A25-A2, M/IO, D/C, BE3-BE0 valid delay	4	13	T309	READY valid delay		10
T302	READY setup time	15		T310	RDYTRN setup time (TGUI9420DGi & CPU)	7	
T303	READY hold time	4		T311	RDYTRN hold time (TGUI9420DGi & CPU)	4	
T304	LOCAL ready to ADS low		20				
T305	Write data valid delay	7	18				

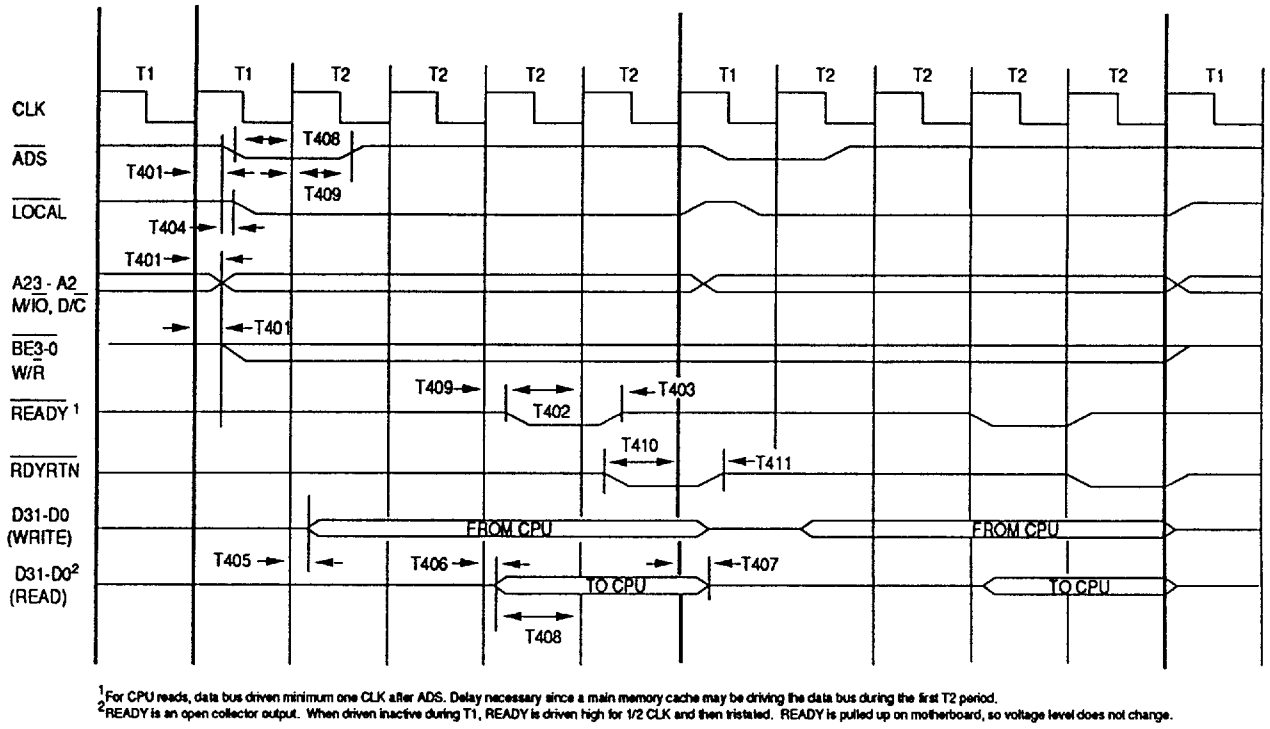


[1]For CPU reads, data bus driven minimum one CLK after ADS. Delay necessary since a main memory cache may be driving the data bus during the first T2 period.
[2]READY is an open collector output. When driven inactive during T1, READY is driven high for 1/2 CLK and then tristated. READY is pulled up on motherboard, so voltage level does not change.

Figure 5. 486SX and 486DX VL-Bus Timing (33 MHz)

Table 10. 486SX and 486DX VL-Bus Timing (33 MHz CPU)

SYM	Description	Min (ns)	Max (ns)	SYM	Description	Min (ns)	Max (ns)
Ti	Idle period	30		T404	$\overline{\text{LOCAL}}$ ready to $\overline{\text{ADS}}$ low		20
T1	1st clock period	30		T405	Write data valid delay	3	18
T2	2nd clock period	30		T406	Read data bus drive to CPU CLK rising edge		5
T401	$\overline{\text{ADS}}$, A25-A2, M/$\overline{\text{IO}}$, D/$\overline{\text{C}}$, $\overline{\text{BE3}}$-$\overline{\text{BE0}}$ valid delay		20	T407	Read data hold time	3	
T402	$\overline{\text{READY}}$ setup time	20		T408	Data read/write setup time	5	
T403	$\overline{\text{READY}}$ hold time	4		T409	$\overline{\text{READY}}$ valid delay		10



[1]For CPU reads, data bus driven minimum one CLK after ADS. Delay necessary since a main memory cache may be driving the data bus during the first T2 period.
[2]READY is an open collector output. When driven inactive during T1, READY is driven high for 1/2 CLK and then tristated. READY is pulled up on motherboard, so voltage level does not change.

Figure 6. 486DX VL-Bus Timing (50 MHz)

Table 11. 486SX and 486DX VL-Bus Timing (50 MHz)

SYM	Description	Min (ns)	Max (ns)	SYM	Description	Min (ns)	Max (ns)
Ti	Idle period	20		T406	Read data bus drive to		
T1	1st clock period	20			CPU CLK rising edge		5
T2	2nd clock period	20		T407	Read data hold time	3	
T401	ADS, A25-A2, M/IO, D/C,			T408	Data read setup time	5	
	BE3-BE0 valid delay	3	12	T409	READY valid delay		13
T402	READY setup time	10		T410	RDYTRN setup time		
T403	READY hold time	4			(TGUI9420DGi & CPU)	5	
T404	LOCAL ready to ADS low		20	T411	RDYTRN hold time		
T405	Write data valid delay	3	12		(TGUI9420DGi & CPU)	2	

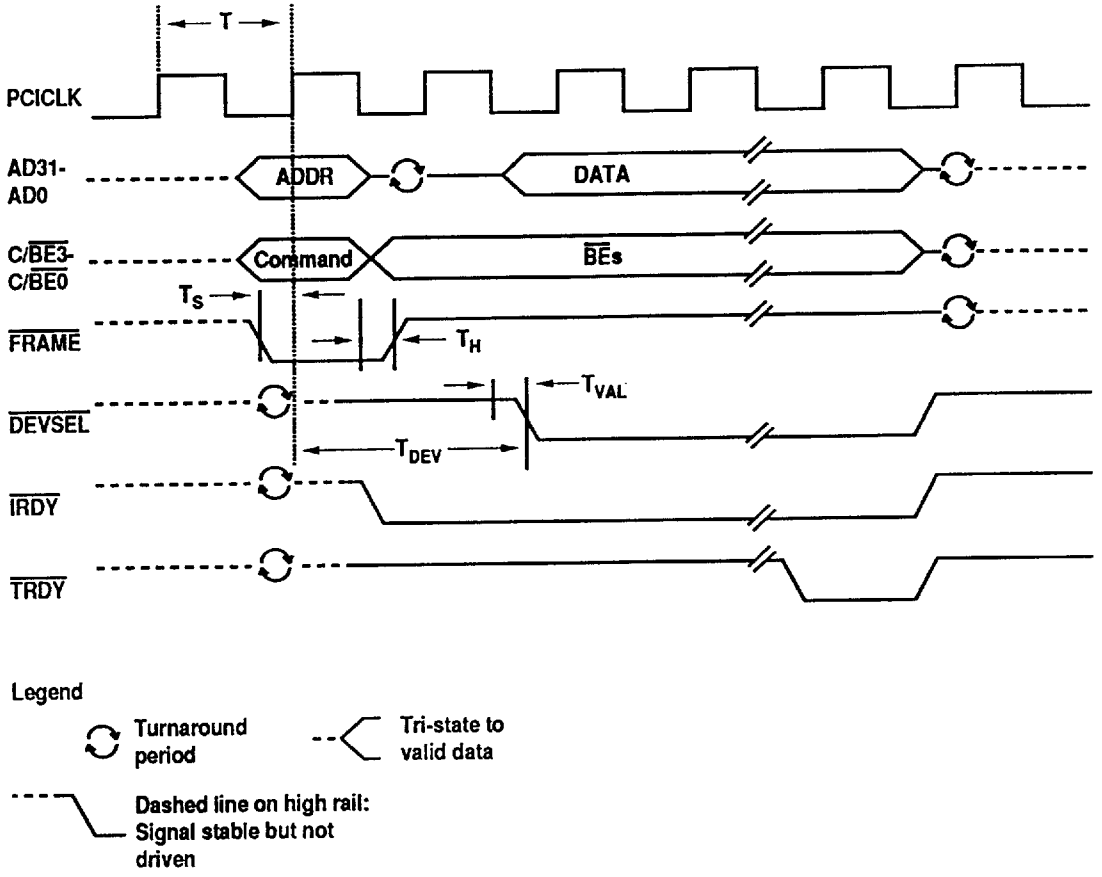


Figure 7. PCI Bus Memory or I/O Read Cycle Timing

Table 12. PCI Bus Memory or I/O Read Cycle Timing

SYM	Description	Min (ns)	Max (ns)	SYM	Description	Min (ns)	Max (ns)
T	Clock period	30					
T_{DEV}	Address phase to $\overline{DEVSEL}$	2*PCICLK		T_H	Input signal hold time	0	
T_S	Input signal setup time	7		T_{VAL}	PCICLK to output signal valid delay	2	11

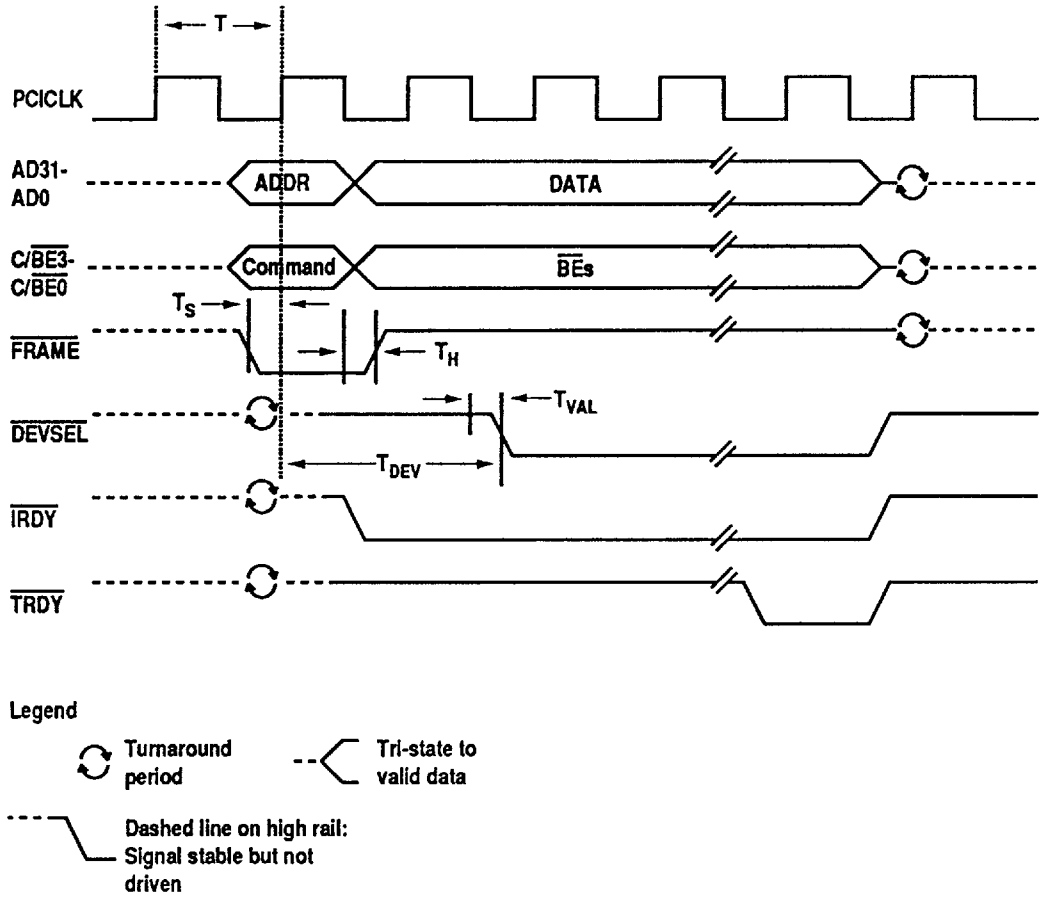


Figure 8. PCI Bus Memory or I/O Write Cycle Timing

Table 13. PCI Bus Memory or I/O Write Cycle Timing

SYM	Description	Min (ns)	Max (ns)	SYM	Description	Min (ns)	Max (ns)
T	Clock period	30		T_H	Input signal hold time	0	
T_{DEV}	Address phase to $\overline{DEVSEL}$	2*PCICLK		T_{VAL}	PCICLK to output signal valid delay	2	11
T_S	Input signal setup time	7					

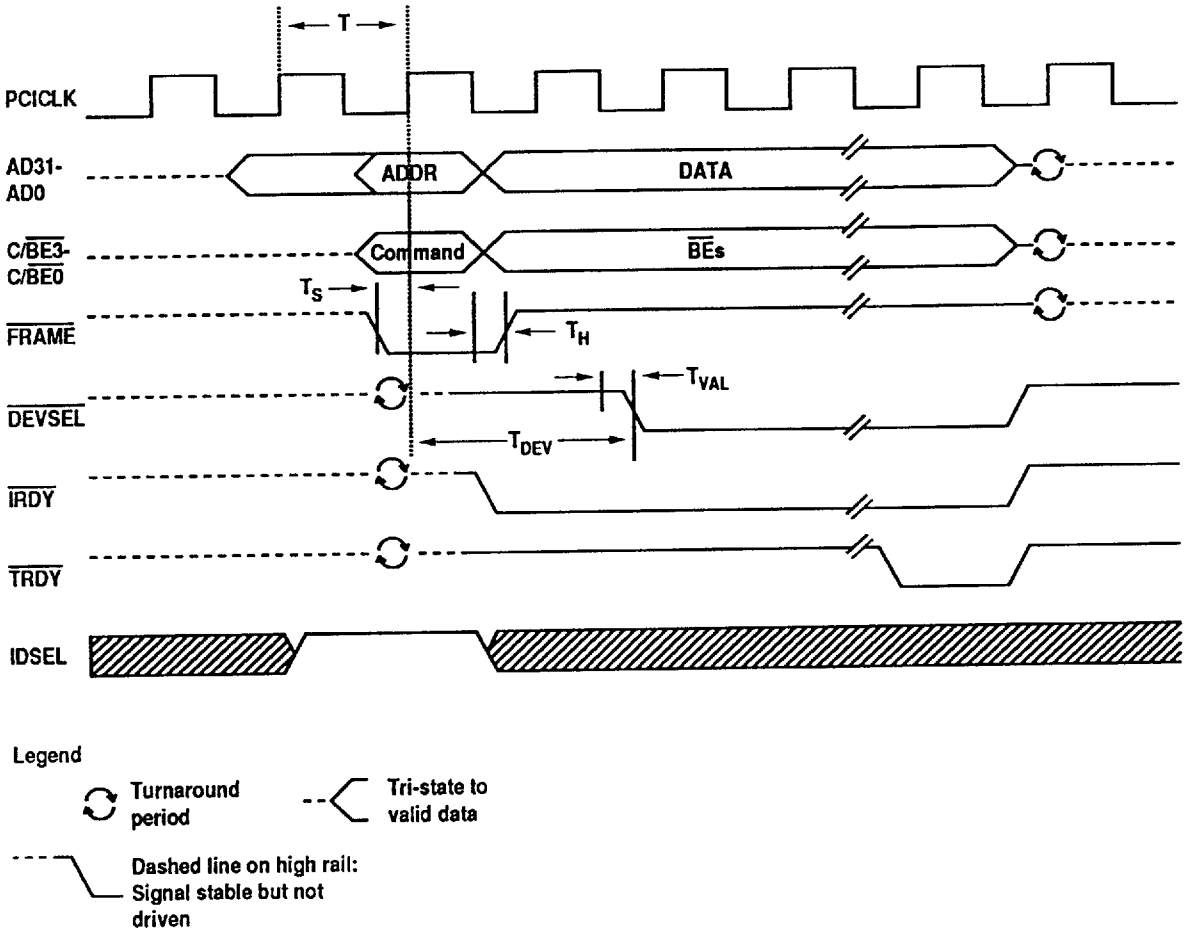


Figure 9. PCI Configuration Write Cycle Timing

Table 14. PCI Configuration Write Cycle Timing

SYM	Description	Min (ns)	Max (ns)	SYM	Description	Min (ns)	Max (ns)
T	Clock period	30		T_H	Input signal hold time	0	
T_{DEV}	Address phase to $\overline{DEVSEL}$	2*PCICLK		T_{VAL}	PCICLK to output signal valid delay	2	11
T_S	Input signal setup time	7					

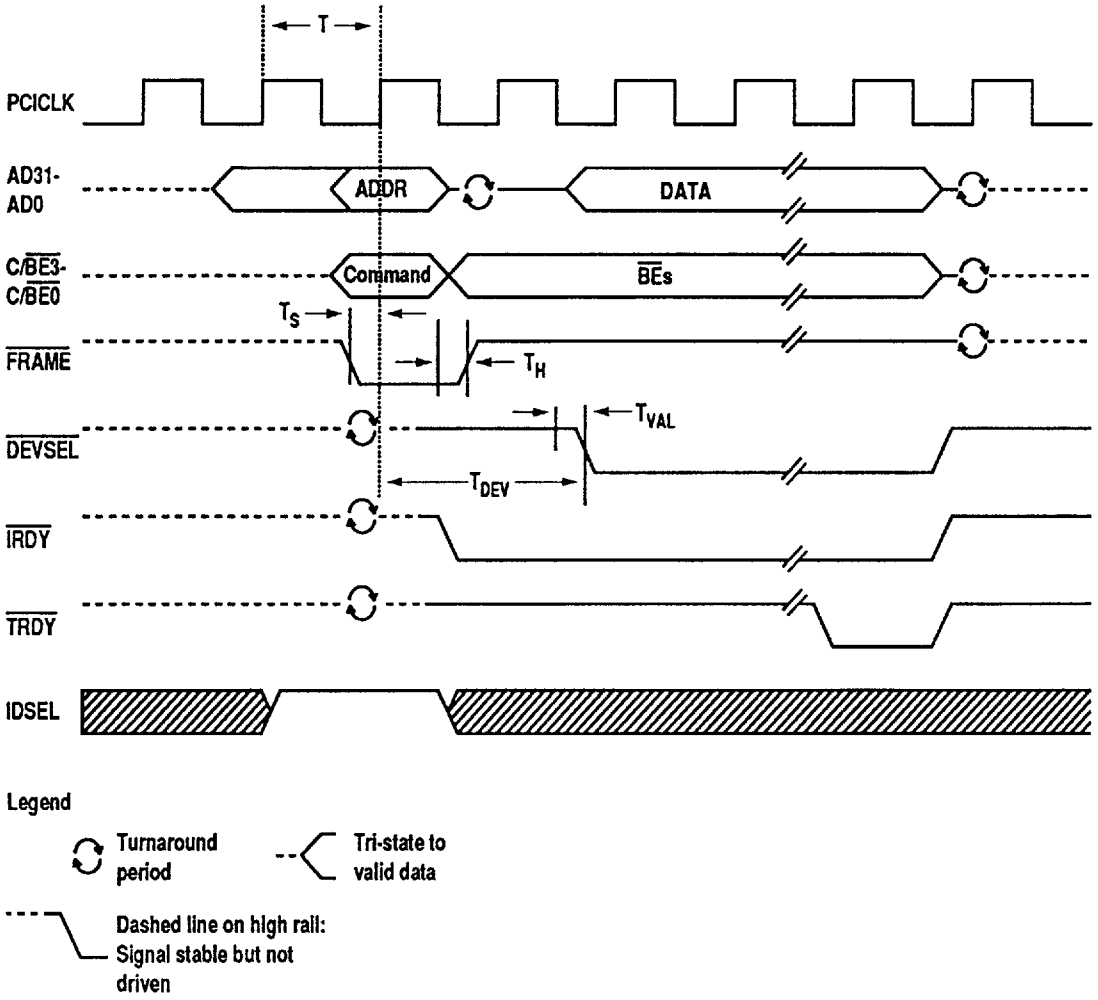


Figure 10. PCI Configuration Read Cycle Timing

Table 15. PCI Configuration Read Cycle Timing

SYM	Description	Min (ns)	Max (ns)	SYM	Description	Min (ns)	Max (ns)
T	Clock period	30		T_H	Input signal hold time	0	
T_{DEV}	Address phase to DEVSEL	2*PCICLK		T_{VAL}	PCICLK to output signal valid delay	2	11
T_S	Input signal setup time	7					

Table 16. Vertical Timing (m sec)

Mode	CLK	Type	Display	Max Colors	T1	T2	T3	T4	T5	T6	Polarity
0,1	25.2	A/N	40x25	16	1.577	12.711	0.413	14.268	0.064	1.08	+
2,3	25.2	A/N	80x25	16	1.577	12.711	0.413	14.268	0.064	1.08	+
0*,1*	25.2	A/N	40x25	16	3.146	11.122	1.208	14.268	0.064	1.87	-
2*,3*	25.2	A/N	80x25	16	3.146	11.122	1.208	14.268	0.064	1.87	-
0+,1+	28.3	A/N	40x25	16	1.577	12.711	0.413	14.268	0.064	1.08	+
2+,3+	28.3	A/N	80x25	16	1.577	12.711	0.413	14.268	0.064	1.08	+
4,5	25.2	APA	320x200	4	1.577	12.711	0.413	14.268	0.064	1.08	+
6	25.2	APA	640x200	2	1.577	12.711	0.413	14.268	0.064	1.08	+
7	28.3	A/N	80x25	Mono	3.146	11.122	1.208	14.268	0.064	1.87	+
7+	28.3	A/N	80x25	Mono	1.577	12.711	0.413	14.268	0.064	1.08	+
D	25.2	APA	320x200	16	1.577	12.711	0.413	14.268	0.064	1.08	+
E	25.2	APA	640x200	16	1.577	12.711	0.413	14.268	0.064	1.08	+
F	25.2	APA	640x350	Mono	3.146	11.122	1.208	14.268	0.064	1.87	-
10	25.2	APA	640x350	16	3.146	11.122	1.208	14.268	0.064	1.87	-
11	25.2	APA	640x480	2	1.430	15.253	0.350	16.683	0.064	1.02	-
12	25.2	APA	640x480	16	1.430	15.253	0.350	16.683	0.064	1.02	-
13	25.2	APA	320x200	256	1.577	12.711	0.413	14.268	0.064	1.08	+
50	25.2	A/N	80x30	16	1.430	15.253	0.350	16.683	0.064	1.02	-
51	25.2	A/N	80x43	16	1.652	15.031	0.540	16.683	0.064	1.05	-
52	25.2	A/N	80x60	16	1.430	15.253	0.350	16.683	0.064	1.02	--
53	40.0	A/N	132x25	16	3.168	11.200	1.248	14.368	0.064	1.86	-
54	40.0	A/N	132x30	16	1.376	15.360	0.352	16.736	0.064	0.60	-
55	40.0	A/N	132x43	16	1.600	15.136	0.576	16.736	0.064	0.96	-
56	40.0	A/N	132x60	16	1.376	15.360	0.352	16.736	0.064	0.60	-
57	44.9	A/N	132x25	16	3.079	11.225	1.219	14.304	0.064	1.80	-
58	44.9	A/N	132x30	16	1.315	15.394	0.321	16.709	0.064	0.93	-
59	44.9	A/N	132x43	16	1.539	15.170	0.417	16.709	0.064	1.06	-
5A	44.9	A/N	132x60	16	1.315	15.394	0.321	16.709	0.064	0.93	-
5B	36.0	APA	800x600	16	0.711	17.067	0.028	17.715	0.057	0.56	-
5C[3]	50.35	APA	640x400	256	1.557	12.711	0.413	14.268	0.064	1.08	+
5C[4]	25.2	APA	640x400	256	11.02	.557	12.711	0.413	14.268	1.08	+
5D[3]	50.35	APA	640x480	256	1.430	15.253	0.350	16.683	0.064	1.02	-
5D[4]	25.2	APA	640x480	256	1.430	12.253	0.350	16.683	0.064	1.02	-
5E[3]	72.0	APA	800x600	256	0.711	17.067	0.028	17.778	0.057	0.86	-
5E[4]	36.0	APA	800x600	256	0.711	17.067	0.028	17.778	0.057	0.56	-
5E[2]	50.3	APA	800x600	256	1.395	12.489	0.479	13.883	0.125	0.79	+
5F	44.9	APA	1024x768 (I)	16	0.873	10.810	0.155	11.683	0.056	0.66	+
5F	65.0	APA	1024x768 (NI)	16	0.945	15.785	0.329	16.731	0.041	0.58	+
5F[2,5]	75.0	APA	1024X768 (HR)	16	0.673	13.599	0.053	14.272	0.106	0.51	+
60	44.9	APA	1024X768(I)	4	0.873	10.810	0.155	11.683	0.056	0.66	+
61	44.9	APA	768x1024 (I)	16	0.791	13.501	0.119	14.292	0.040	0.63	+
62	44.9	APA	1024x768 (I)	256	0.873	10.810	0.155	11.683	0.056	0.66	+
62	65.0	APA	1024x768 (NI)	256	0.945	15.785	0.329	16.731	0.041	0.58	+
62[2,5]	75.0	APA	1024x768 (HR)	256	0.673	13.599	0.053	14.272	0.106	0.51	+
63	75.0	APA	1280X1024 (I)	16	1.120	10.705	0.379	11.835	0.084	0.67	+
64	75.0	APA	1280X1024 (I)	256	1.120	10.705	0.379	11.835	0.084	0.67	+
6C	75.0	APA	640x480	16M	1.430	15.253	0.350	16.683	0.064	1.02	-
70/71[1]	77.0	APA	512x480	32/64K	1.430	15.253	0.350	16.683	0.064	1.02	-
74/75[1]	50.35	APA	640x480	32/64K	1.430	15.253	0.350	16.683	0.064	1.02	-
76/77[1]	72.0	APA	800x600	32/64K	1.430	15.253	0.350	16.683	0.064	0.56	-

[1]Same timing on 32K and 64K color modes.

[2]Based on VESA (Video Electronics Standards Association) standards VS900502 and VS910801.

[3]16-bit DRAM bus version of mode.

[4]32-bit DRAM bus version of mode.

[5]HR=High refresh or 70 Hz vertical refresh.

Table 17. Horizontal Timing (μ sec)

Mode	CLK	Type	Display	Max Colors	T7	T8	T9	T10	T11	T12	Polarity
0,1	25.2	A/N	40x25	16	6.356	25.422	0.636	1.907	3.813	31.778	-
2,3	25.2	A/N	80x25	16	6.356	25.422	0.636	1.907	3.813	31.778	-
0*,1*	25.2	A/N	40x25	16	6.356	25.422	0.636	1.907	3.813	31.778	+
2*,3*	25.2	A/N	80x25	16	6.356	25.422	0.636	1.907	3.813	31.778	+
0+,1+	28.3	A/N	40x25	16	6.356	25.422	0.636	1.907	3.813	31.778	-
2+,3+	28.3	A/N	80x25	16	6.356	25.422	0.636	1.907	3.813	31.778	-
4,5	25.2	APA	320x200	4	6.356	25.422	0.636	1.907	3.813	31.778	-
6	25.2	APA	640x200	2	6.356	25.422	0.636	1.907	3.813	31.778	-
7	28.3	A/N	80x25	Mono	6.356	25.422	0.636	1.907	3.813	31.778	+
7+	28.3	A/N	80x25	Mono	6.356	25.422	0.636	1.907	3.813	31.778	+
D	25.2	APA	320x200	16	6.356	25.422	0.636	1.907	3.813	31.778	-
E	25.2	APA	640x200	16	6.356	25.422	0.636	1.907	3.813	31.778	-
F	25.2	APA	640x350	Mono	6.356	25.422	0.636	1.907	3.813	31.778	+
10	25.2	APA	640x350	16	6.356	25.422	0.636	1.907	3.813	31.778	+
11	25.2	APA	640x480	2	6.356	25.422	0.636	1.907	3.813	31.778	-
12	25.2	APA	640x480	16	6.356	25.422	0.636	1.907	3.813	31.778	-
13	25.2	APA	320x200	256	6.356	25.422	0.477	2.066	3.813	31.778	-
50	25.2	A/N	80x30	16	6.356	25.422	0.636	1.907	3.813	31.778	-
51	25.2	A/N	80x43	16	6.356	25.422	0.636	1.907	3.813	31.778	-
52	25.2	A/N	80x60	16	6.356	25.422	0.636	1.907	3.813	31.778	-
53	40.0	A/N	132x25	16	5.600	26.400	0.000	1.800	3.800	32.000	+
54	40.0	A/N	132x30	16	5.600	26.400	0.000	1.800	3.800	32.000	-
55	40.0	A/N	132x43	16	5.600	26.400	0.000	1.800	3.800	32.000	-
56	40.0	A/N	132x60	16	5.600	26.400	0.000	1.800	3.800	32.000	-
57	44.9	A/N	132x25	16	5.612	26.459	-0.200	1.804	4.009	32.071	+
58	44.9	A/N	132x30	16	5.612	26.459	-0.200	1.804	4.009	32.071	-
59	44.9	A/N	132x43	16	5.612	26.459	-0.200	1.804	4.009	32.071	-
5A	44.9	A/N	132x60	16	5.612	26.459	-0.200	1.804	4.009	32.071	-
5B	36.0	APA	800x600	16	6.222	22.222	0.667	3.500	2.028	28.660	-
5B[2]	50.35	APA	800x600	16	4.926	15.889	0.794	2.066	2.066	20.814	+
5C[3]	50.35	APA	640x400	256	6.356	25.422	0.556	1.668	4.131	31.778	-
5C[4]	25.2	APA	640x400	256	6.356	25.422	0.636	1.907	3.813	31.778	-
5D[3]	50.35	APA	640x480	256	6.356	25.422	0.556	1.668	4.131	31.778	-
5D[4]	25.2	APA	640x480	256	6.356	25.422	0.636	1.907	3.813	31.778	-
5E[3]	72.0	APA	800x600	256	6.222	22.222	0.667	3.500	2.028	28.660	+
5E[4]	36.0	APA	800x600	256	6.222	22.222	0.667	3.500	2.028	28.660	-
5E[2]	50.3	APA	800x600	256	4.926	15.889	0.794	2.066	2.066	20.814	+
5F	44.9	APA	1024x768 (I)	16	5.345	22.806	0.204	1.260	3.956	28.151	+
5F	65.0	APA	1024x768 (NI)	16	4.800	15.754	0.615	1.108	3.077	20.554	+
5F[2,5]	75.0	APA	1024X768 (HR)	16	4.053	13.653	0.320	1.920	1.813	17.707	+
60	44.9	APA	1024X768(I)	4	5.345	22.806	1.069	1.782	2.494	28.151	+
61	44.9	APA	768x1024 (I)	16	9.265	17.105	-1.782	4.633	4.811	26.370	+
62	44.9	APA	1024x768 (I)	256	5.345	22.806	-0.178	2.851	2.316	28.151	+
62	65.0	APA	1024x768 (NI)	256	4.800	15.754	0.615	1.108	3.077	20.544	+
62[2,5]	75.0	APA	1024x768 (HR)	256	4.053	13.653	0.320	1.920	1.813	17.707	+
63	75.0	APA	1280X1024 (I)	16	3.965	17.035	0.255	0.205	3.400	21.000	+
64	75.0	APA	1280X1024 (I)	256	3.965	17.035	0.255	0.205	3.400	21.000	+
6C	75.0	APA	640x480	16M	6.356	25.422	0.636	1.907	3.813	31.778	-
70/71[1]	77.0	APA	512x480	32/64K	6.356	25.422	0.636	1.907	3.813	31.778	-
74/75[1]	50.35	APA	640x480	32/64K	6.356	25.422	0.636	1.907	3.813	31.778	-
76/77[1]	72.0	APA	800x600	32/64K	6.222	22.222	0.667	3.500	2.028	28.660	-

[1]Same timing on 32K and 64K color modes.

[2]Based on VESA (Video Electronics Standards Association) standards VS900502 and VS910801.

[3]16-bit DRAM bus version of mode.

[4]32-bit DRAM bus version of mode.

[5]HR=High refresh or 70 Hz vertical refresh.

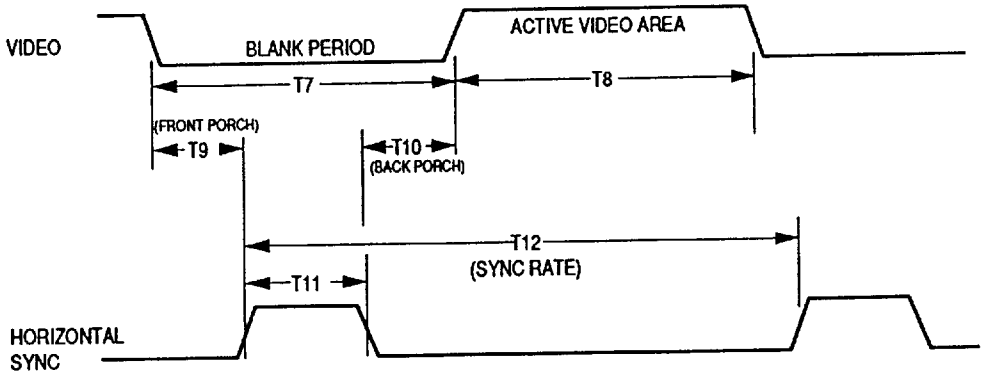


Figure 11. TGUI9420DGi Horizontal Timing

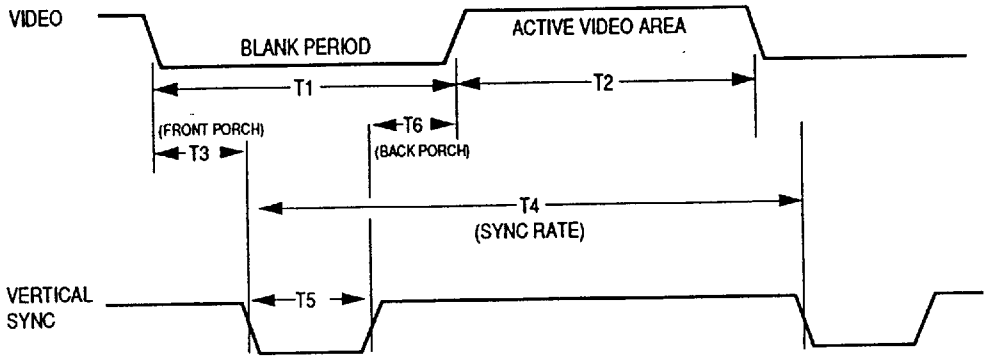


Figure 12. TGUI9420DGi Vertical Timing

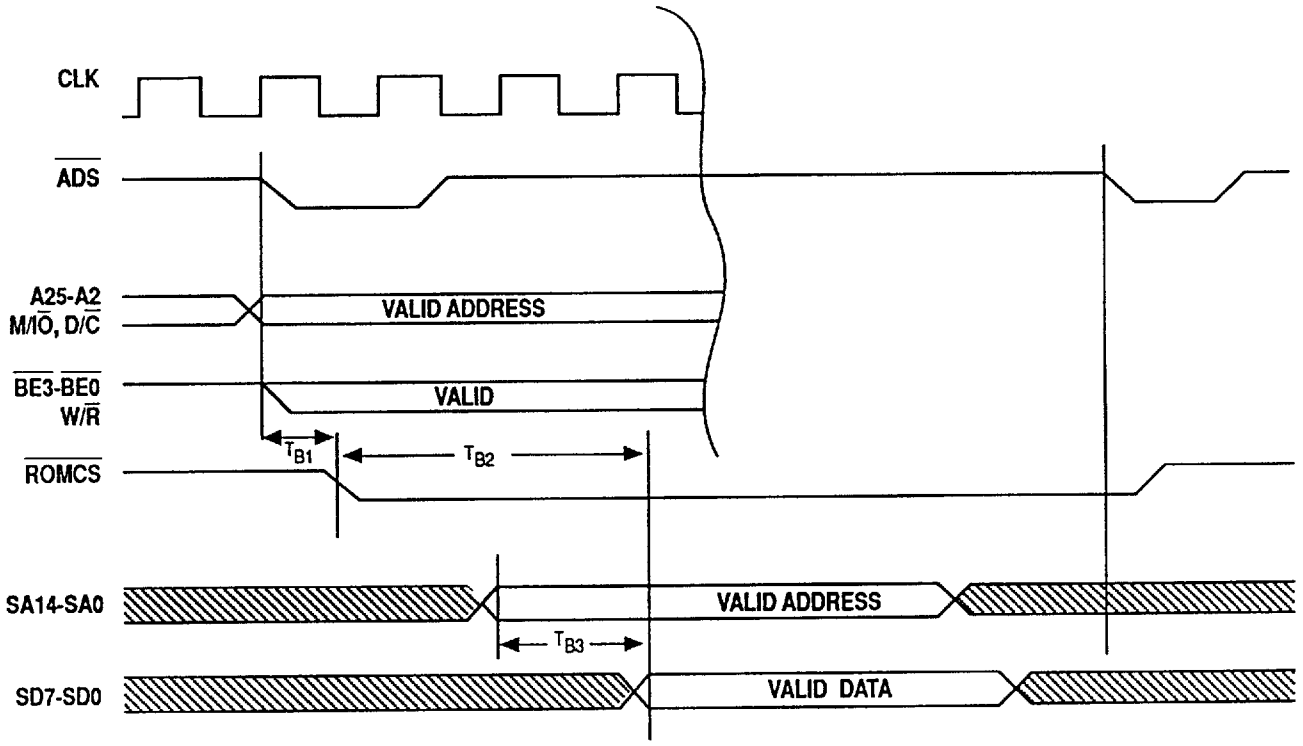


Figure 13. BIOS Access Over ISA Bus (VL-Bus Configuration Only)

Table 18. BIOS Access Over ISA Bus

SYM	Description	Min (ns)	Max (ns)
TB1	ROMCS to VL-Bus Address		8
TB2	ROMCS to Data Valid	68	
TB3	ISA Address to Data Valid	50	

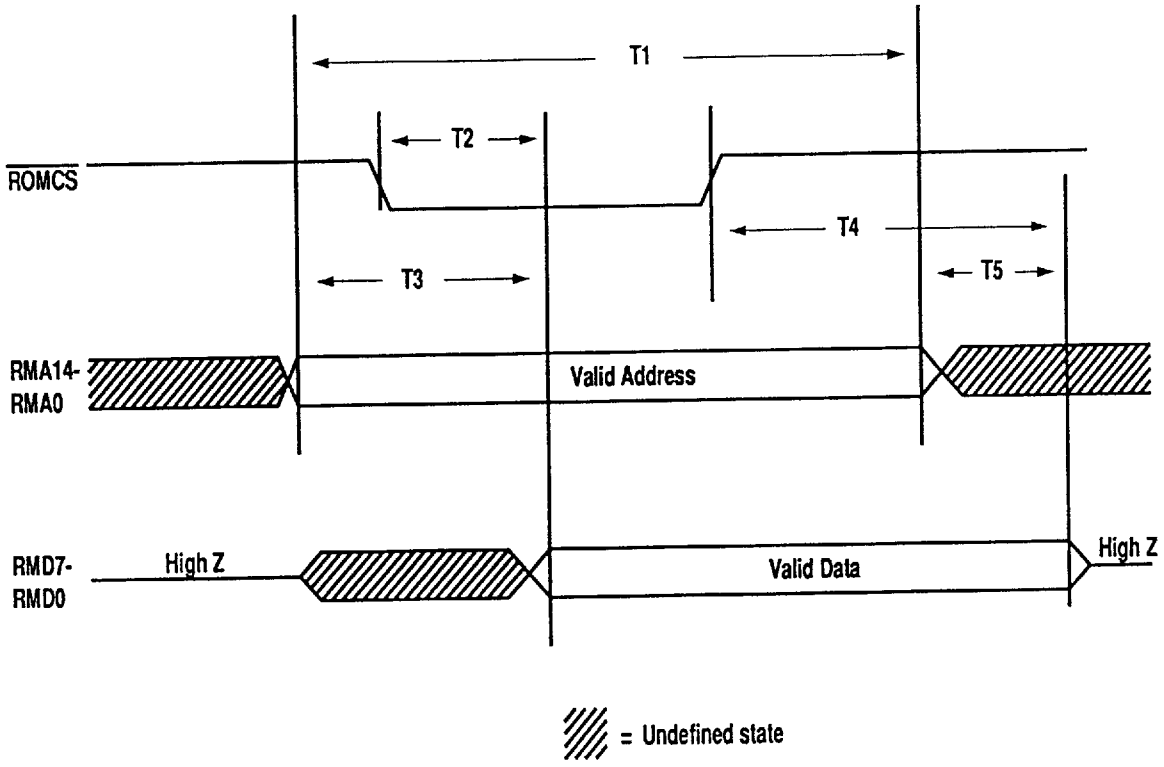


Figure 14. ROM Access Timing for PCI Implementation

Table 19. PCI Configuration ROM Access Timing

SYM	Description	Min (ns)	Typ (ns)	Max (ns)
T1	Cycle time		32 DMCLKs	
T2	Chip enable access time			150
T3	Address access time			150
T4	Data to high Z delay time			85
T5	Valid data from invalid address hold time	10		

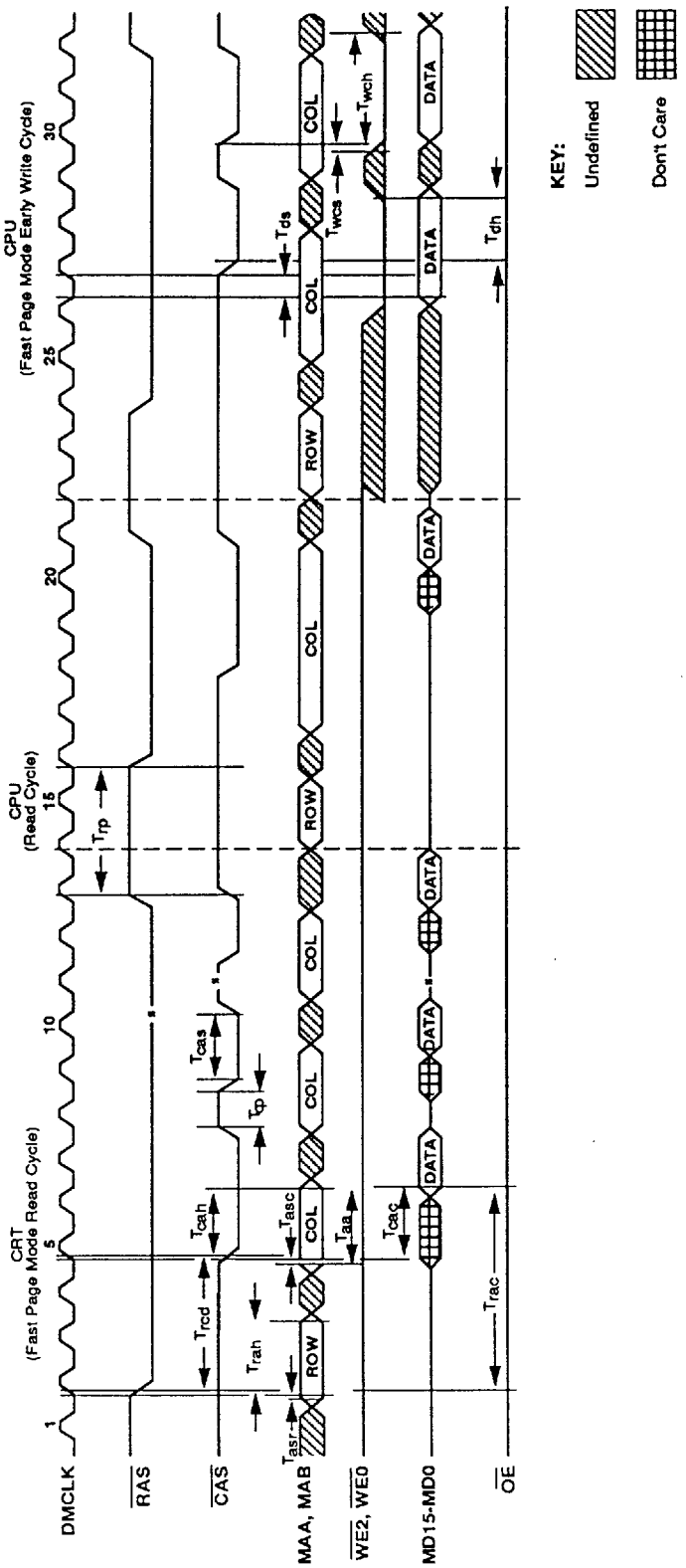


Figure 1 5. 256Kx4 DRAM (512K Solution)

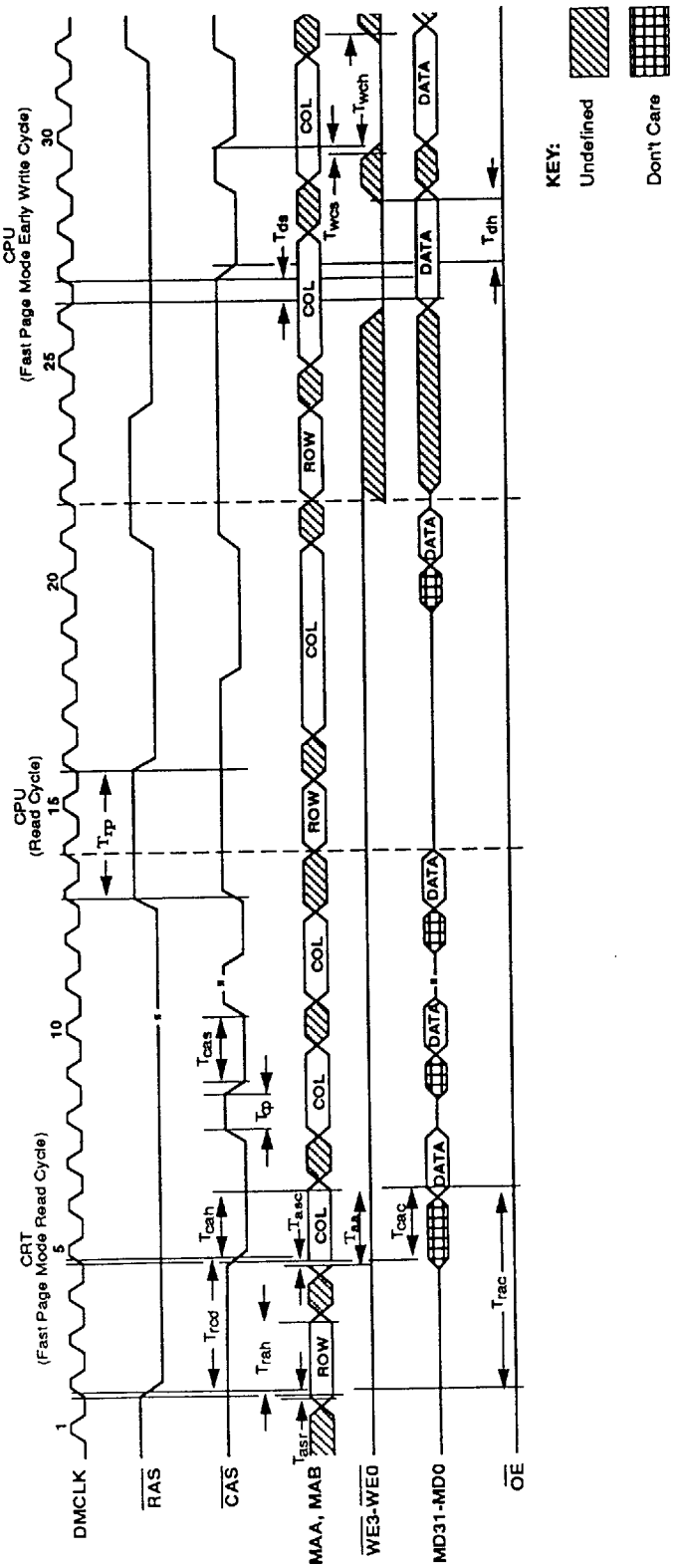


Figure 16. 256Kx4 DRAM (1MB Solution)

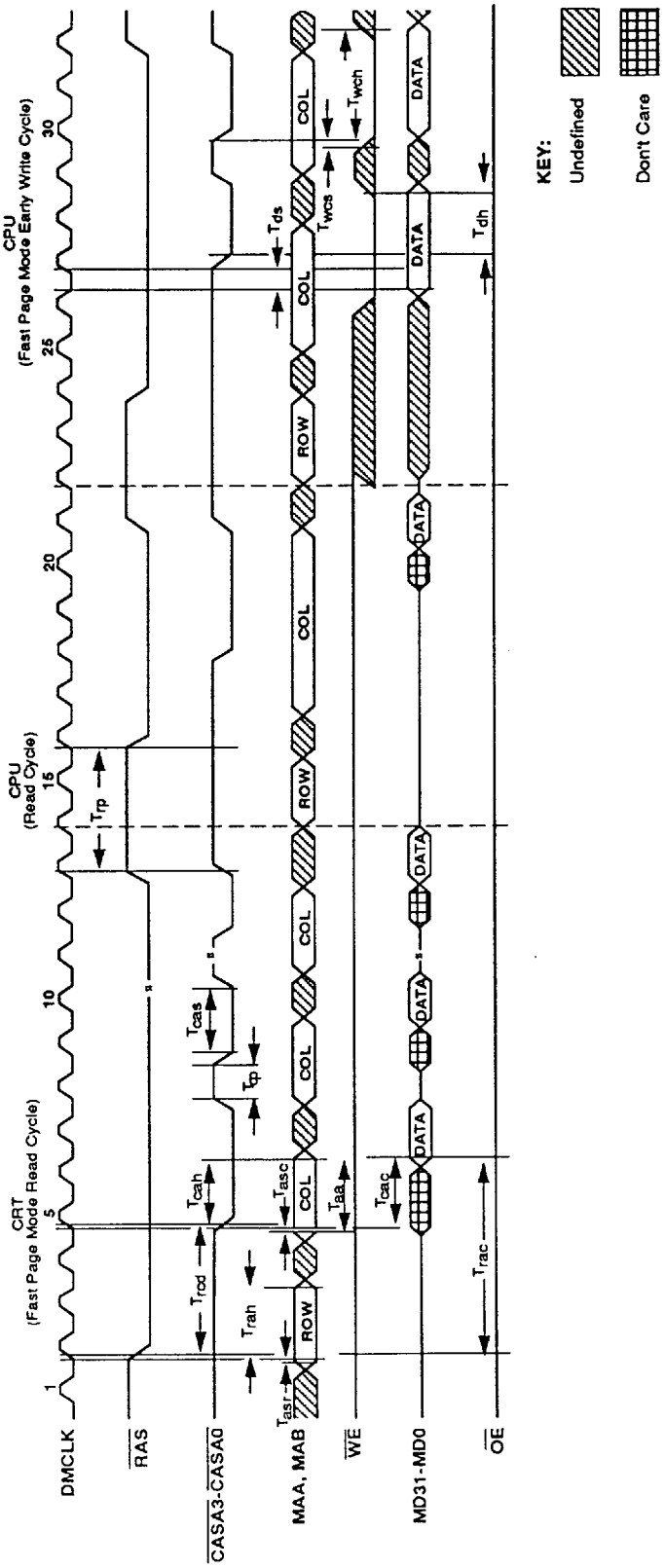


Figure 17. 256Kx16 Multiple CAS DRAM (1MB or 2MB Solution)

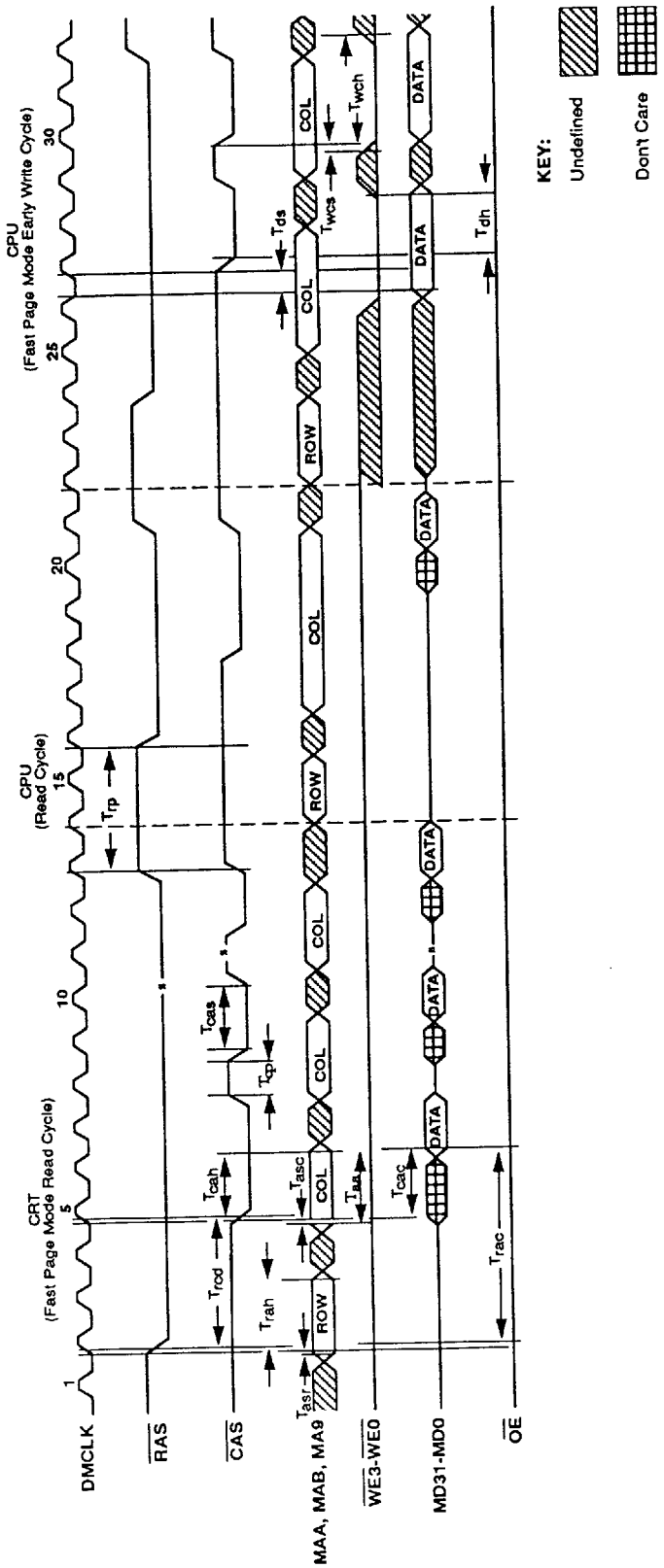


Figure 18. 512Kx4 or 512Kx8 DRAM (2MB Solution)

Table 20. Worst Case Timing Parameters[1]

Parameter	16-Bit DRAM Interface	32-Bit DRAM Interface
Trcd	3t+2ns	2t+2ns
Trah	2t+2ns	t+1.5ns
Tasr	≥0	≥0
Tasc	≥0	≥0
Tcah	2t	2t
Tcp[2]	t + 1ns	t + 1ns
Tcas[2]	2t - 2ns	2t - 2ns
Tds	≥0	≥0
Trp[2]	3t - 4ns	3t - 6ns
Taa	3t - 2ns	3t + 4ns
Tcac	2t - 2.5ns	2t + 7ns
Trac	4t + 3ns	5t + 1.5ns
Tdh	2t + 1ns	2t - 1ns
Twcs	2t	+
Twch	2t - 5ns	2t - 3ns
Test Load	50pf	85pf

[1] t=1/DMCLK

[2] These parameters are programmable via chip registers

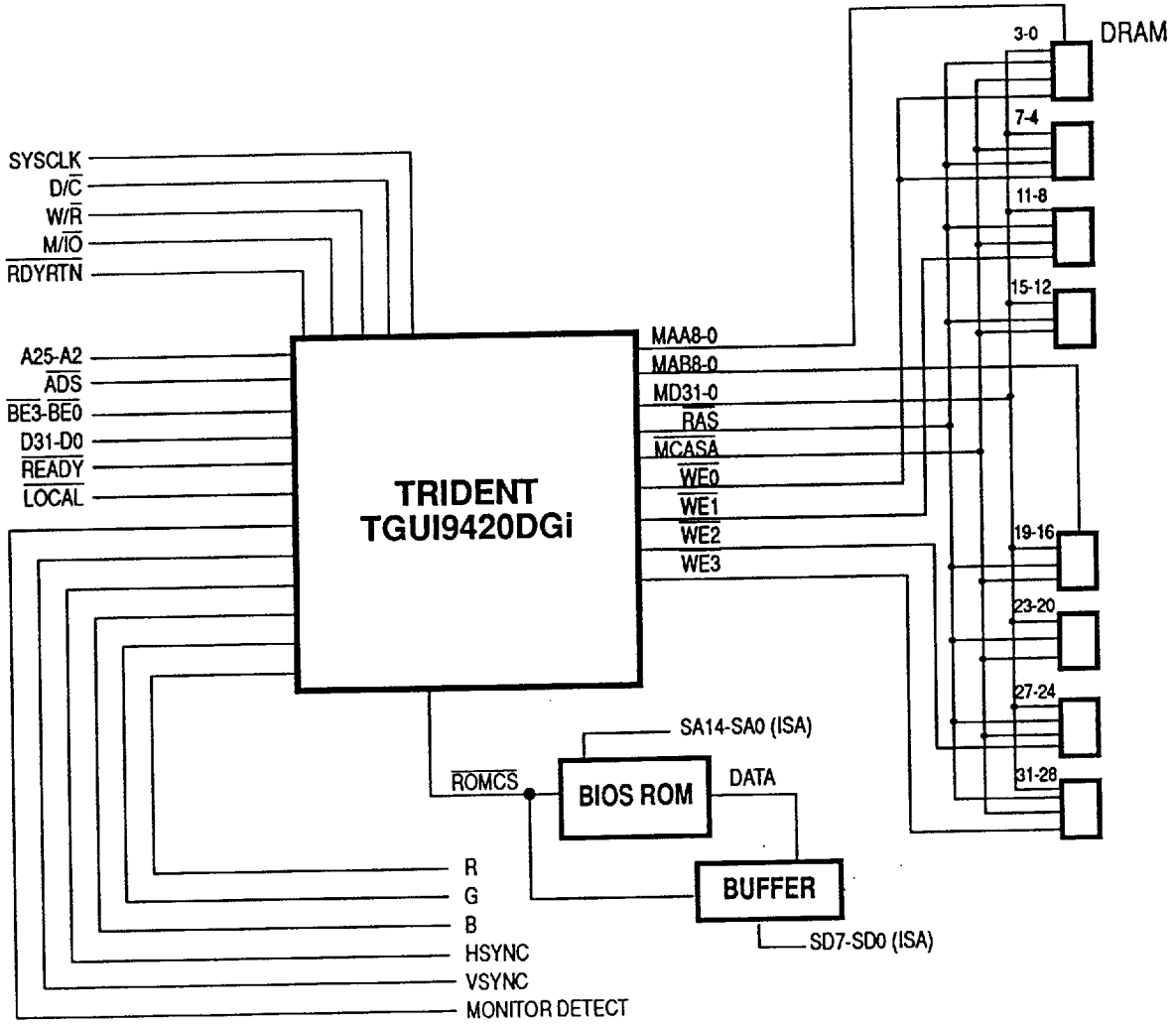


Figure 19. Application for 1MB 256Kx4 DRAM (486DX VL-Bus)

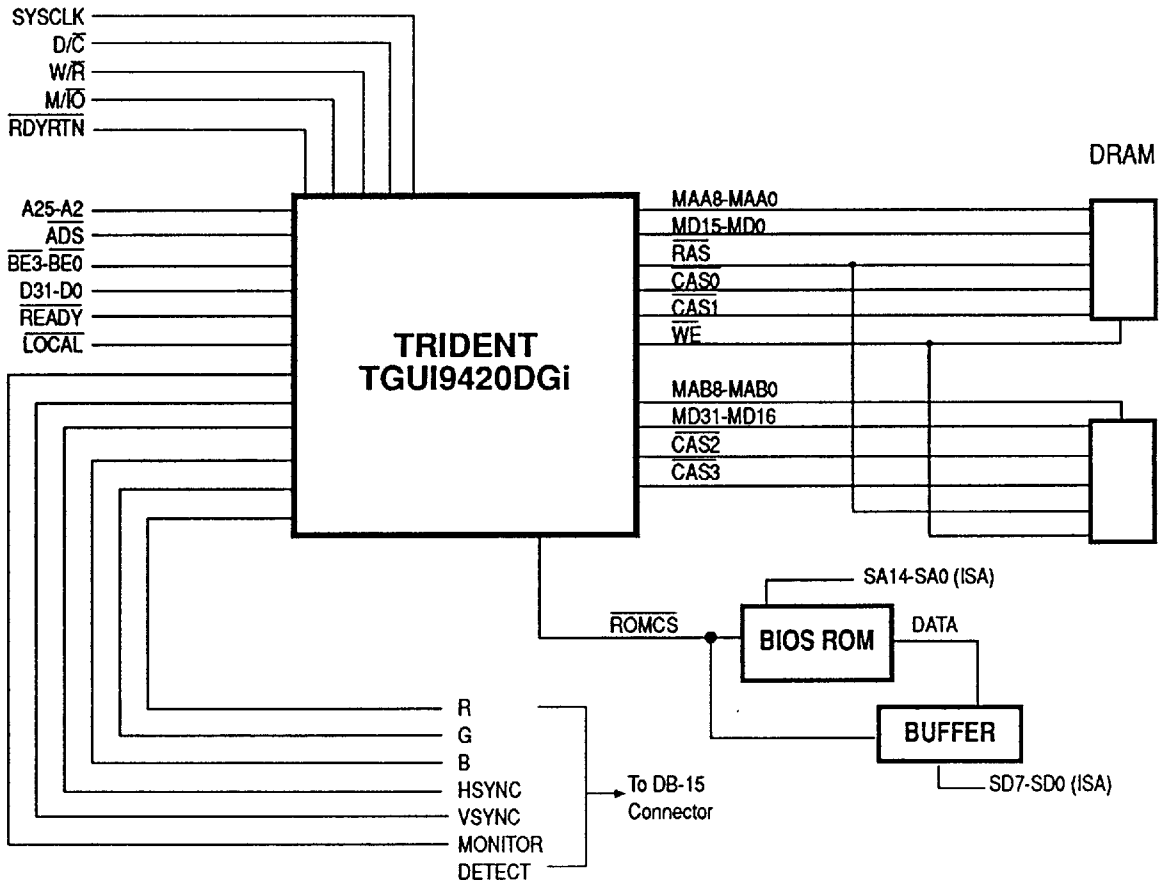


Figure 20. Application for 1MB 256Kx16 DRAM (486DX VL-Bus)

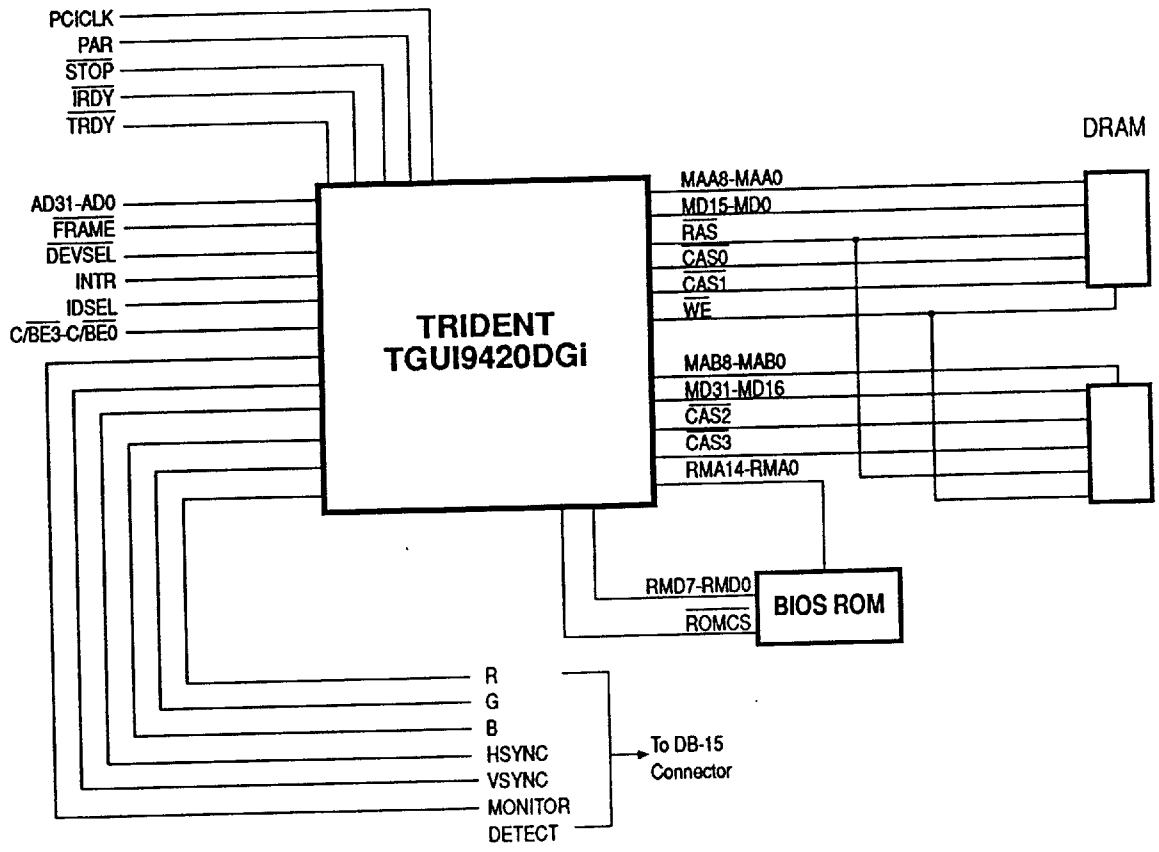


Figure 21. Application for 1MB 256Kx16 DRAM (PCI Bus)

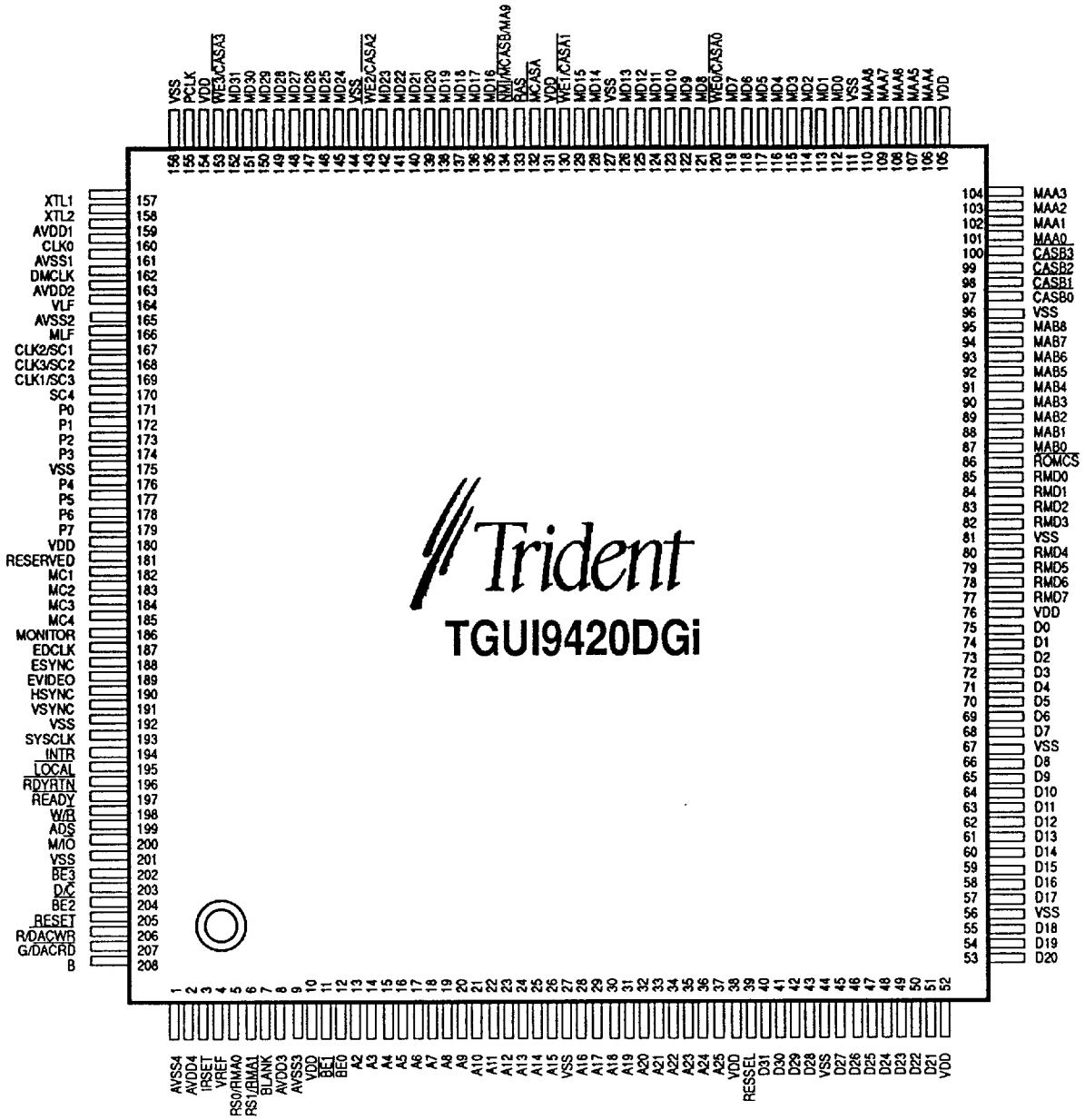
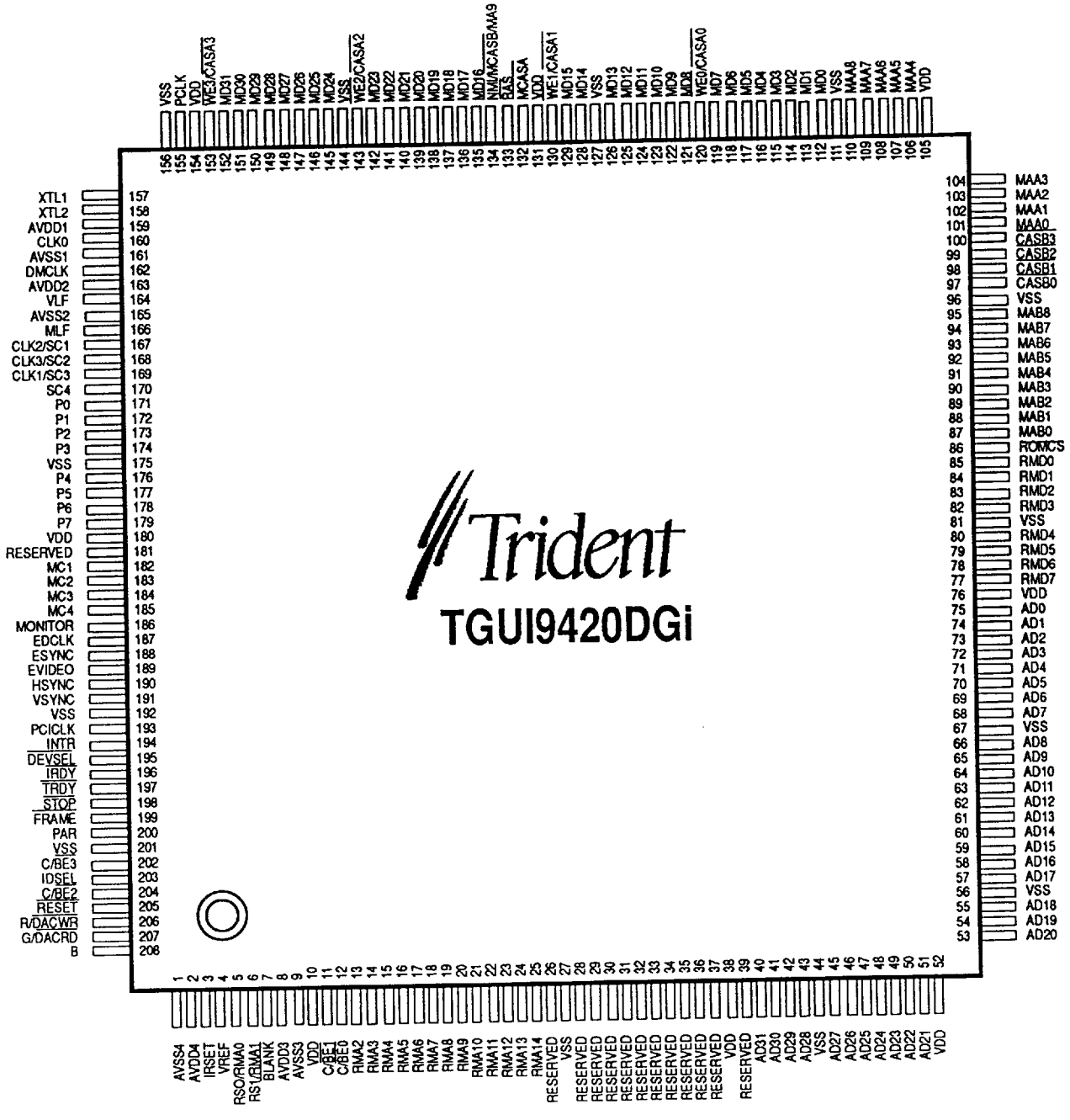


Figure 22. TGUI9420DGi Pin Out (VL-Bus)

Trident



[1] These pins should be tied to V_{DD}

Figure 22. TGUI9420DGi Pin Out (PCI Bus)

Table 21. TGUI9420DGi Pin Description

Pin	Pin Type	Pin Number	Description
Host Interface - VL-Bus Signals			
D/$\overline{C}$	I	203	Local bus data or control cycle
M/$\overline{IO}$	I	200	Local bus memory or I/O cycle
W/$\overline{R}$	I	198	Local bus write or read access
$\overline{READY}$	O	197	Local bus cycle ready
$\overline{ADS}$	I	199	System status
SYSCLK	I	193	System clock
A25-A2	I	37-28, 26-13	Address bus, bit 25 to bit 2 (386DX, 486DX)
$\overline{BE3}$-$\overline{BE2}$	I	202, 204	Byte enable for D31-D24 and D23-D16 (386DX, 486DX only)
$\overline{BE1}$-$\overline{BE0}$	I	11, 12	Byte enable for D15-D8 and D7-D0
$\overline{RDYRTN}$	I	196	Ready return; terminate VL-Bus transaction
D31-D0	I/O	40-43, 45-51, 53-55 57-66, 68-75	Data bus, bit 31 to bit 0
INTR	O	194	Interrupt request
RESET	I	205	System reset; the falling or rising edge latches configuration information into internal registers from memory data lines and RMD7-RMD0. RESET polarity is chosen using RESSEL
$\overline{LOCAL}$	O	195	CPU Local Bus cycle. A logical 0 indicates a Local Bus cycle.
RESSEL	I	39	Selects RESET Polarity; If RESSEL =0, RESET is active low. If RESSEL=1, RESET is active high
$\overline{NMI}$/$\overline{MCASB}$/MA9	O	134	Non-maskable interrupt/drive $\overline{CAS}$ for 2MB 256Kx4 or 256Kx8 DRAM/tenth address pin for 512Kx4 or x8, or 2MB 256Kx16 DRAM
Host Interface - PCI Signals			
AD31-AD0	I/O	40-43, 45-51 53-55, 57-66 68-75	Multiplexed address/data bus pins. During the first clock of a PCI bus transaction, these lines act as address inputs to the TGUI9420DGi. During subsequent clocks, these lines act as data inputs/outputs. Byte ordering is Little Endian. These signals are tri-stated at $\overline{RESET}$.
ROMA14-ROMA0	I	25-13, 6, 5	ROM address signals for ROM access. ROMA1 and ROMA0 are shared with RS1 and RS0.
$\overline{FRAME}$	I	199	Cycle Frame. Driven by bus master to indicate the beginning and duration of an access.
IDSEL	I	203	Initialization Device Select. Used as a chip select (instead of the upper 24 bits of address) for configuration read/writes.
PAR	O	200	Parity bit. Bit set to give even parity across AD31-AD0 and C/$\overline{BE3}$-C/$\overline{BE0}$. Driven by the TGUI9420DGi for read data phases. It is asserted one PCICLK after $\overline{TRDY}$. This signal is tri-stated at $\overline{RESET}$.

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Table 21. TGUI9420DGi Pin Description- continued

Pin	Pin Type	Pin Number	Description
Host Interface - PCI Signals - Continued			
$\overline{\text{STOP}}$	O	198	Stop signal. Issued by TGUI9420DGi to request that the bus master terminate the current transaction.
C/$\overline{\text{BE3}}$ - C/$\overline{\text{BE0}}$	I	202, 204 11,12	Bus Command and Byte Enable signals. During the address phase of a PCI bus transaction, these signals define the bus command. During the data phase of the transaction, these signals indicate which byte lanes are carrying valid data.
$\overline{\text{IRDY}}$	I	196	Initiator Ready. Used in conjunction with $\overline{\text{TRDY}}$ to complete a bus transaction. A logical 0 indicates the bus master is ready to accept data (read operation) or that valid data is on the bus (write operation).
$\overline{\text{TRDY}}$	O	197	Target Ready. Used in conjunction with $\overline{\text{IRDY}}$ to complete a bus transaction. Logical 0 indicates the TGUI9420DGi has issued valid data to the bus (read operation) or that the TGUI9420DGi is ready to accept data (write operation).
INTR	O	194	Interrupt Request. Indicates that the TGUI9420DGi has gen erated an interrupt and needs to be serviced. This signal is not used for peripheral solutions.
PCICLK	I	193	System Clock. Timing for all PCI interface signals is based on the rising edge of PCICLK.
$\overline{\text{DEVSEL}}$	O	195	Device Select. Logical 0 indicates the TGUI9420DGi has decoded the incoming address as its own and is claiming the cycle.
$\overline{\text{RESET}}$	I	205	System Reset. Signal is active low. Forces TGUI9420DGi to a known state. Signal must be held low for at least two PCICLKs in order to be recognized by the TGUI9420DGi.
Display Memory Interface			
$\overline{\text{MCASA}}$	O	132	Column address strobe for Bank A
$\overline{\text{WE3}}$-$\overline{\text{WE0}}$/ $\overline{\text{CASA3}}$-$\overline{\text{CASA0}}$	O	153, 143, 130, 120	Write enable pins 3-0/Column access strobe pins 3-0 for Bank A (for 1MB DRAM configurations which require multiple $\overline{\text{CAS}}$)
$\overline{\text{CASB3}}$-$\overline{\text{CASB0}}$	O	100-97	Column access strobe pins 3-0 for Bank B (for 2MB DRAM configurations which require multiple $\overline{\text{CAS}}$)
$\overline{\text{RAS}}$	O	133	Row address strobe
MAA8-MAA0	O	110-106, 104-101	Multiplexing address bus of display memory Bank A
MAB8-MAB0	O	95-87	Multiplexed address bus of display memory Bank B
MD31-MD0	I/O	152-145, 142-135, 129, 128, 126-121, 119-112	Memory data bus (bit 31 to bit 0)
DMCLK	I	162	DRAM clock input from external clock synthesizer
MC4-MC1	O	185-182	DRAM clock select pins for external clock synthesizer

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Table 21. TGUI9420DGi Pin Description - Continued

Pin	Pin Type	Pin Number	Description
Video Interface			
VSYNC	O	191	Vertical synchronization pulse, polarity programmable
HSYNC	O	190	Horizontal synchronization pulse, polarity programmable
RMD7-RMD0	I/O	77-80, 82-85	ROM data bus for PCI implementations. May also be used to connect an external RAMDAC.
RS1/RMA1	I/O	6	DAC register select bit 1 (for external RAMDAC)/ROM address bit 1 (PCI case). Not connected to ROM when ROM on ISA Bus.
RS0/RMA0	I/O	5	DAC register select bit 0 (for external RAMDAC)/ROM address bit 0 (PCI case). Not connected to ROM when ROM on ISA Bus.
P7-P0	I/O	179-176, 174-171	Pixel data bits 7-0 to/from feature connector or for external DAC
PCLK	I/O	155	Pixel clock input from feature connector/Pixel clock output to feature connector for external DAC
$\overline{\text{BLANK}}$	I/O	7	Blank input from feature connector/Blank output to feature con nector for external DAC
R/$\overline{\text{DACWR}}$	O	206	Red output/Write strobe for external DAC
G/$\overline{\text{DACRD}}$	O	207	Green output/Read strobe for external DAC
B	O	208	Blue output
VREF	I	4	External voltage reference pin
IRSET	I	3	Full scale RGB output voltage adjust control
Clock Synthesizer Interface			
CLK1/SC3	I/O	169	Video clock input 1 from external oscillator/Clock select output 3 to external clock synthesizer
CLK2/SC1	I/O	167	Video clock input 2 from external oscillator/Clock select output 1 to external clock synthesizer
CLK3/SC2	I/O	168	Video clock input 3 from external oscillator/Clock select output 2 to external clock synthesizer
CLK0	I	160	Video clock input from an external oscillator or clock synthesizer
SC4	O	170	Clock select output 4 to an external clock synthesizer
XTL2-XTL1	I	158, 157	Quartz crystal inputs 1 and 2, connect to 14.318 MHz crystal. Connect only XTL1 if using a 14.318 MHz oscillator.
VLF	I	164	Video PLL filter
MLF	I	166	Memory PLL filter
BIOS Interface			
RMD7-RMD0	I/O	77-80, 82-85	ROM/External DAC data bus bits 7-0. Not connected to ROM when ROM on ISA Bus.
$\overline{\text{ROMCS}}$	O	86	BIOS EPROM chip select. Not connected to ROM when ROM on ISA Bus.
RS0/RMA0	O	5	External DAC register select bit 0/ROM address bit 0 (ROM for VL-Bus enabled). Not connected to ROM when ROM on ISA Bus.

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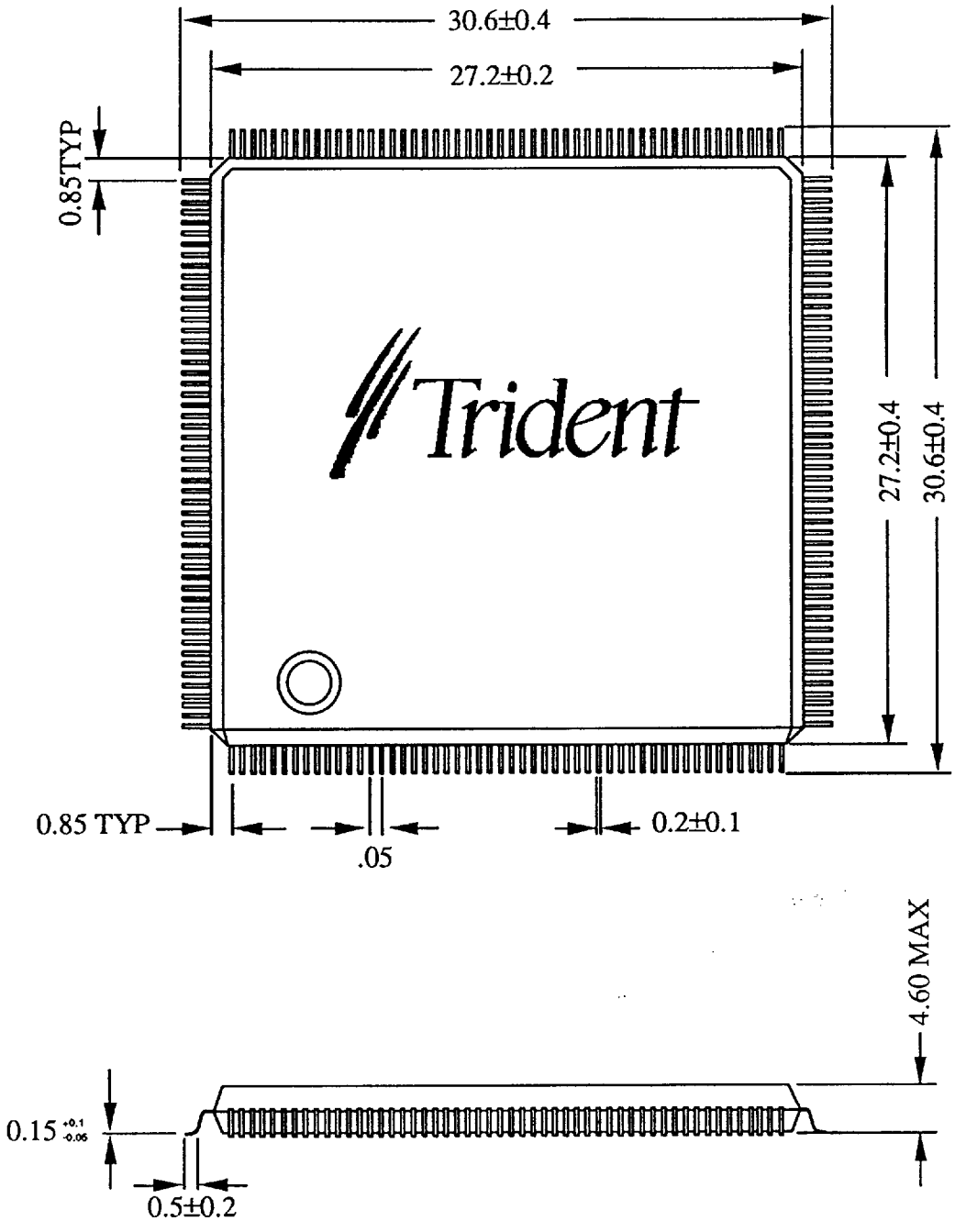
Table 20. TGUI9420DGi Pin Description- continued

Pin	Pin Type	Pin Number	Description
BIOS Interface - Continued			
RS1/RMA1	O	6	External DAC register select bit 1/ROM address bit 1 (ROM for VL-Bus enabled)Not connected to ROM when ROM on ISA Bus.
Other External Interfaces			
EVIDEO	I	189	External pixel data enable (feature connector)
EDCLK	I	187	External clock enable (feature connector)
ESYNC	I	188	External sync enable (feature connector)
MONITOR	I	186	Monitor type detect (analog monitors)
Power Pins			
AVSS4-1	GND	1, 9, 165, 161	Analog Ground
AVDD4-1	PWR	2, 8, 163, 159	Analog Power
VSS	GND	27, 44, 56, 67, 81, 96,111, 127, 144, 156,175, 192, 201	Digital Ground
VDD	PWR	10, 38, 52, 76 105, 131, 154, 180	Digital Power



Lead positional tolerance: 0.08 mm for maximum lead width (0.3 mm)

Figure 22. TGUI9420DGi Packaging - PFP 208 Pins (dimensions in mm)