about 60% of which will be for multiuser environments supporting the maximum eight terminals. Colony adds, however, that IBM should still outsell Digital's MicroVAX II in 1986; he projects DEC will sell 9,000 to 12,000 units this year. Since DEC introduced the MicroVAX II in May 1985, it has sold 12,000 units—said to be roughly the total number of work stations Apollo has sold in its three years of operation.

The n-MOS RT processor executes 84 of its 118 instructions in a single 170-ns cycle. IBM claims benchmark processing speeds of 1.6 million to 2.1 million instructions/s—considerably faster than the MicroVAX II. But benchmark comparisons have more than their share of critics. Among them is Frank Lynch, director of marketing for Silvar-Lisco, which also supports Apollo and DEC with its schematic design software.

"IBM is saying the RT can run around 2 mips. The MicroVAX II runs at 0.9 mips. But when you are running an interactive program, what really counts is the operator's speed, and the quality of the display and keyboard," Lynch says.

Still, others rave about the new system's speed. Says Boucher, whose company—Interleaf—has adapted its software to work stations from DEC, Apollo, and Sun as well as IBM: "It's a very fast machine, certainly in the 68020 class. It's about as fast as anything we've seen." *–Tobias Naegele*

GRAPHICS

TI GRABS EARLY LEAD IN ADVANCED GRAPHICS ICs

HOUSTON

The bell is about to ring for the next round of competition in color-graphics chips, as silicon houses aim to cut the cost of work-station display-processing hardware by as much as 90% and to tap emerging graphics-software standards.

Leading the way is a fast 32-bit graphics-oriented microprocessor from Texas Instruments Inc. that is slated for sampling in six weeks. Delayed a bit, and now expected to arrive in May, is Intel Corp.'s 16-bit graphics coprocessor, the 82786. Out of the picture is a 16-bit raster graphics display processor from Motorola Inc.; the company has dropped the planned product in favor of a new graphics strategy centered around its general-purpose 32-bit 68020 processor.

The developments are all part of what computer-graphics vendors hope will be a revolution in high-resolution color personal computers for the office and more-affordable work stations for the engineer. In addition, major IC manufacturers in both the U. S. and Japan are striking alliances with independent software houses to offer interfaces to industry standards, such as the Computer Graphics Interface (CGI) and the emerging Graphics Kernel System (GKS).

The target end-equipment market should grow from 5.23 million units in 1985 to 9.12 million units in 1988, according to forecasts compiled by TI's Programmable Products Division in Houston.

The Dallas company is pulling the wraps off its 1.8-μm CMOS graphics signal processor, the TMS34010. The 68-pin chip marries the architecture of a general-purpose 32-bit microprocessor to a graphics-oriented reduced-instruction-set computer. The 34010 executes 6 million instructions/s, addresses a gigabit of storage, performs quickly with standard low-speed dynamic random-access memories, and completes raster-manipulating operations in a single cycle.

TI says the 34010 is as programmable as a general-purpose microprocessor but unmatched when it comes to raster operations. The RISC block performs raster operations 2 to 12 times faster than Motorola's 68020, says Kevin McDonough, TI graphics products manager. "About 30% of the GSP is dedicated to manipulations of pixel-size fields," he says. One of the chip's two buses connects to the system host microprocessor; the other—a 16-bit bus—is for memory. (TI plans eventually to offer a second-generation chip with full 32-bit memory bus.)

The 34010's 256-byte cache memory lets the core of the chip run full speed at 50 MHz with 6-mips performance while using slower DRAMs and dual-ported video RAMs. Alongside the chip's 6-mips general-purpose core, a number of graphics-management functions are implemented, such as a barrel shifter.

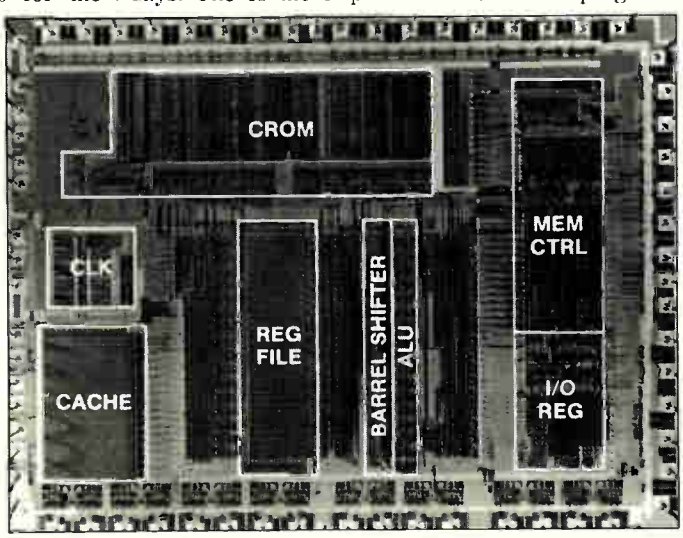
When samples are available March 1, TI will sell the 34010, housed in plastic leaded chip carriers, for $500 in single quantities. Volume deliveries are expected in the fourth quarter. Software-development-system support will also be available in March and a library of graphics functions is due in April. TI has also aligned third-party software support using the CGI standard from Graphics Software Systems Inc. of Beaverton, Ore., and Nova Graphics International Corp. of Austin, Texas.

SIX-MONTH LEAD. "There are other companies working on graphics processors, but we think it will be a minimum of six months before they have silicon," TI's McDonough says. "As a matter of fact, we have been approached by some [for second sourcing] now that the word is getting out."

Competing chips are progressing through design and early conceptual phases. The players include the likes of Hitachi, NEC, NCR, and Inmos, which plans to unveil its transputer-based graphics processor, the G412, later this year. Advanced Micro Devices Inc. plans to introduce its Am95C60 quad-pixel data-flow-manager IC during the third quarter.

"The architectures are significantly different and I cannot say a lot about them, but any of them could solve the problem," notes Harold Blair, president of Nova Graphics. "Some are easier to program than others. Some have much higher bandwidth. Timing studies show you can get anywhere from 10- to 100-times performance improvement over board implementations. These new graphics processors will replace two to three boards, now costing $2,000 to $3,000, and will cost in the $300 range." Nova Graphics has contracts with TI, Intel, and Motorola. Blair leaves this week for Japan to discuss CGI interfaces with several Japanese chip companies.

Intel is providing samples of its 16-bit graphics coprocessor to selected customers under nondisclosure



PICTURE POWER. TI's 34010 graphics processor executes 6 million instructions/s and works with low-speed memory chips.

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pacts. But officially, the graphics-components operation in Santa Cruz, Calif., has pushed back introduction of the CMOS 82786 from March to May to ensure that development support is ready.

In Austin this month, Motorola's Microprocessor Products Group dropped the 16-bit raster graphics display processor, known as RGDP. Last summer, Motorola announced it would introduce in 1986 a high-performance graphics device to operate in the CGI environment. Officials of the microprocessor group have now opted to place the general-purpose 68020 squarely in the center of the high-resolution graphics movement. The support will come from additional graphics software "hooks" and hardware peripherals intended to "tie the 68020 or a future 32-bit processor into a graphics system," explains James Lovegrove, a product manager in the high-end microprocessor operation.

"Most of the customers we see in the work-station and business markets have spent 1985—in addition to surviving—trying to investigate graphics," Lovegrove says. He believes the graphics arena is still in a very early stage of its evolution. *–J. Robert Lineback*

IC PROCESSING

TI TO UNVEIL 1-MICRON CMOS FOR LOGIC

DALLAS

Texas Instruments Inc. will soon launch a 1-μm advanced high-speed CMOS logic family aimed at matching the performance of the fastest bipolar-Schottky components. TI made its entry into advanced high-speed-CMOS standard logic last year [*Electronics Week*, May 27, 1985, p. 19] when it began focusing its new 1-μm CMOS process on small- and medium-scale integration logic after spawning the technology for 1-Mb dynamic random-access memories.

When formally introduced by TI—along with a second-source announcement—the 1-μm silicon-gate logic technology will be called Enhanced Performance Implanted CMOS, or EPIC.

Epic also describes the struggle that TI process engineers faced in 1981 in developing a 1-μm DRAM technology equally applicable to the fabrication flow of high-performance logic.

"The criteria put some very severe restrictions on how we designed the cell of the megabit dynamic RAM," recalls Greg Armstrong, manager of CMOS technology in the TI Semiconductor Group's Advanced Development Division. The task was to create a universal 1-μm fabrication flow, lumping together all the steps for building DRAM-cell capacitors so they could be easily skipped when processing logic.

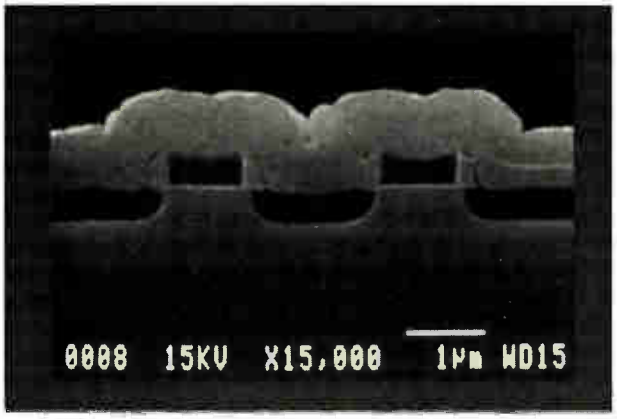
The concept of universal process flow could lead the way to mixed-lot processing of logic and commodity-memory wafers. Each wafer type would sit out certain processing steps.

Armstrong credits the idea to Mohan Rao, semiconductor vice president and manager of advanced development. "He said we are doing our processes in the wrong order," says Armstrong. "In his assessment, a time would come when commodity parts running in large volume would not be as important as the ability to flexibly attack specific markets with a unifying technology. So he said to put one together." The first reaction of many TI process engineers was that the project might have been aimed at too many IC product types.

"It turned out to be quite a challenge, because typically the sequences that go into fabricating the DRAM capacitors are high-temperature steps and thermal cycles that affect diffusions and other structures out in the periphery," says Armstrong.

Four years after its launch, the 1-μm CMOS technology emerged as a promising unifier for TI's broad product portfolio. It was aimed initially at large-scale and very large-scale integration of logic. But a year ago, TI process lab engineers tried the 1-μm process on some existing high-speed CMOS 74-series logic designs. "It then became clear that this process was applicable not only to VLSI, such as microprocessors and digital signal processors, but it could be retrofitted on MSI-type parts," says Armstrong. TI is now attempting to extend the process-development concept to analog circuits and erasable programmable read-only memories. It is also extending the universal-CMOS strategy with its latest efforts on a 4-Mb DRAM trench-transistor-cell process.

"It is important that in the final analysis all products be optimized for the highest performance. But what has been a pleasant surprise is what evolved from the DRAM is what we would have come up with for MSI or VLSI logic," says Armstrong. "That's partly because when you get down to the 1-μm level, you are pushing against the same fundamental limitations of basic physical laws, such as quantum-mechanical tunneling through thin oxides, high-intensity fields due to hot-electron effects, and the need for high-density CMOS without latchup." Those needs are expected to increase below 1 μm.



VERSATILE. Logic wafers can sit out process steps needed only for DRAM fabrication on TI's 1-μm EPIC CMOS production line.

TI is now readying a new family of advanced high-speed CMOS (AHC) logic consisting of SSI, MSI, and some LSI parts. EPIC will be applied to a variety of VLSI products as well, including bit-slice processors, multipliers, and the Lisp processor that TI is developing for the Department of Defense.

The EPIC-based logic family will have 2-ns gate delays, equaling the speeds of TI's own Advanced Schottky bipolar line and a competing FAST family from Fairchild Semiconductor Corp. of Mountain View, Calif. The process has been designed to achieve 0.8- to 1-μm effective gate lengths and potentially can reach subnanosecond gate delays. The process for logic builds silicon gates and source-drain structures and adds a second layer of metal to the memory process for higher logic densities and maximum speeds. EPIC also features a two-layer p and p$^+$ epitaxial substrate and a twin-well structure for latchup suppression.

To enhance early yields, the transistor contacts have been relaxed to 1.5 μm in the AHC parts, as silicon real estate is not as critical for SSI and MSI products as for high-density DRAMs. The gate lengths, however, remain at 1 μm for high speeds.

TI will be aiming the AHC family directly at Fairchild's advanced CMOS technology (FACT). FACT is a sub-2-μm, double-level-metal, single-level-polysilicon process. Fairchild says it has introduced more than 15 parts. And RCA Corp. now says it is delivering samples of some parts from its 2-μm Fast CMOS line. *–J. Robert Lineback*

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