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STG 2000

MULTIMEDIA ACCELERATOR

DESCRIPTION

The STG2000 Multimedia Accelerator delivers a complete array of advanced multimedia functions, including real-time photorealistic 3D graphics, full-motion video, video-based special effects and concurrent high-fidelity audio - all combined in a single chip with a single coherent architecture. The STG2000 is the first in a family of Multimedia Accelerators based on the NV Architecture™.

Delivering a powerful, low-cost solution to the current problems of consumer multimedia computing, the STG2000 provides:

■ Key enabling technologies needed for advanced interactive multimedia.

■ The industry's first coherent multimedia architecture. Everything needed for compelling, realistic multimedia is provided on one chip, with one consistent programming interface. With the STG2000, application developers no longer develop to the lowest common denominator.

KEY FEATURES

■ Single-chip Multimedia Accelerator

■ Coherent Multimedia Architecture

■ Industry-leading GUI Acceleration

■ Wave-Table Synthesis Audio

■ Real-time Photorealistic 3D Graphics

■ Video Texturing

■ Full-Motion Video Acceleration

■ Enhanced Digital Game Port

■ Concurrent Media Processing and Synchronization

■ Real-time Performance under Windows™

■ Consumer Price Point
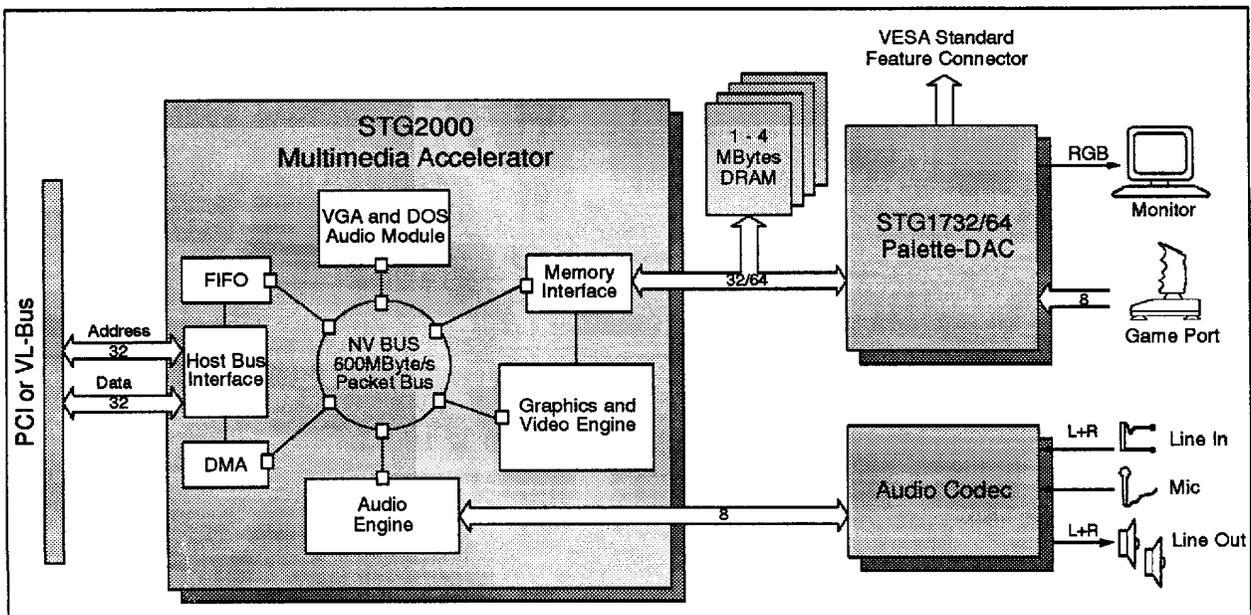
■ Support for Industry Standards

BLOCK DIAGRAM

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1 DEVICE PINOUTS

Power and ground pins are denoted by shading in the following diagrams.

1.1 STG2000 VL-BUS DRAM PIN-OUT

STG2000 208-pin PQFP

Top edge (pins 208–157):
208 VDD, 207 MD[4], 206 MD[11], 205 MD[5], 204 MD[10], 203 MD[6], 202 MD[9], 201 MD[7], 200 MD[8], 199 GND, 198 MD[31], 197 MD[16], 196 MD[30], 195 MD[17], 194 MD[29], 193 MD[18], 192 GND, 191 MD[28], 190 MD[19], 189 MD[27], 188 MD[26], 187 VDD, 186 MD[26], 185 MD[25], 184 MD[21], 183 MD[22], 182 MD[24], 181 MD[20], 180 MD[23], 179 VDD, 178 MA02[8], 177 MA02[0], 176 MA02[7], 175 MA02[1], 174 MA02[6], 173 MA02[2], 172 MA02[5], 171 GND, 170 MA02[3], 169 MA02[4], 168 MA13[8], 167 MA13[0], 166 MA13[7], 165 MA13[1], 164 MA13[6], 163 MA13[2], 162 MA13[5], 161 MA13[3], 160 MA13[4], 159 ALTCS#, 158 ROMCS#, 157 RAS# / GND

Left edge (pins 1–52):
1 GND
2 MD[12]
3 MD[3]
4 MD[13]
5 MD[2]
6 MD[14]
7 MD[1]
8 MD[15]
9 MD[0]
10 AUPD#
11 AUA[0]
12 AUA[1]
13 AUD[0]
14 AUD[1]
15 AUD[2]
16 AUD[3]
17 GND
18 AUD[4]
19 AUD[5]
20 AUD[6]
21 AUD[7]
22 AUW#
23 AUR#
24 BRDY#
25 LDEV#
26 VDD
27 LRDY#
28 A[4]
29 A[6]
30 A[8]
31 A[10]
32 A[12]
33 A[14]
34 A[16]
35 A[18]
36 A[20]
37 A[22]
38 A[24]
39 GND
40 A[26]
41 A[28]
42 A[30]
43 LCLK
44 RESET#
45 LGNT#
46 LREQ#
47 D[31]
48 D[30]
49 D[29]
50 D[28]
51 D[27]
52 VDD

Right edge (pins 156–105):
156 VDD
155 OE0#
154 OE1#
153 OE2#
152 OE3#
151 GND
150 CAS02[0]#
149 CAS02[1]#
148 CAS02[2]#
147 CAS02[3]#
146 VDD
145 CAS13[0]#
144 CAS13[2]#
143 CAS13[1]#
142 CAS13[3]#
141 GND
140 DACCS#
139 NIC
138 NIC
137 WE03#
136 WE12#
135 VSYNC
134 HSYNC
133 LOADCLK
132 VDD
131 BLANK#
130 VCLK
129 GND
128 MCLKx2
127 EN64
126 EECS
125 EESCLK
124 EESD
123 IRQA
122 IRQB
121 IRQC
120 IRQD
119 GND
118 A[2]
117 A[3]
116 A[5]
115 A[7]
114 VDD
113 A[9]
112 A[11]
111 A[13]
110 A[15]
109 A[17]
108 A[19]
107 A[21]
106 A[23]
105 GND

Bottom edge (pins 53–104):
53 GND, 54 D[26], 55 D[25], 56 D[24], 57 BE[3]#, 58 A[31], 59 D[23], 60 D[22], 61 D[21], 62 D[20], 63 D[19], 64 D[18], 65 VDD, 66 D[17], 67 GND, 68 D[16], 69 BE[2]#, 70 ADS#, 71 RDYRTN#, 72 BLAST#, 73 LEADS#, 74 W/R#, 75 WBACK#, 76 D/C#, 77 GND, 78 IOCHCK#, 79 NIO#, 80 BE[1]#, 81 D[15], 82 D[14], 83 D[13], 84 D[12], 85 D[11], 86 D[10], 87 D[9], 88 D[8], 89 VDD, 90 BE[0]#, 91 GND, 92 D[7], 93 D[6], 94 D[5], 95 D[4], 96 D[3], 97 D[2], 98 D[1], 99 D[0], 100 A[29], 101 A[27], 102 A[25], 103 VDD, 104 ...

NOTE

1 VDD=3.3V

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1.2 STG2000 PCI DRAM PIN-OUT

Top pins (208–157):
VDD, MD[4], MD[11], MD[5], MD[10], MD[6], MD[9], MD[7], MD[8], GND, MD[31], MD[16], MD[30], MD[17], MD[29], MD[18], VDD, MD[28], MD[19], MD[27], MD[20], GND, MD[26], MD[21], MD[25], MD[22], MD[24], MD[23], VDD, MA02[8], MA02[0], MA02[7], MA02[1], MA02[6], MA02[2], MA02[5], GND, MA02[3], MA02[4], MA13[0], MA13[7], MA13[1], MA13[6], MA13[2], MA13[5], MA13[3], MA13[4], ALTCS#, ROMCS#, RAS#, GND

Left pins (1–52):
1 GND
2 MD[12]
3 MD[3]
4 MD[13]
5 MD[2]
6 MD[14]
7 MD[1]
8 MD[15]
9 MD[0]
10 AUPD#
11 AUA[0]
12 AUA[1]
13 AUD[0]
14 AUD[1]
15 AUD[2]
16 AUD[3]
17 GND
18 AUD[4]
19 AUD[5]
20 AUD[6]
21 AUD[7]
22 ALW#
23 AUR#
24 NIC
25 NIC
26 VDD
27 NIC
28 NIC
29 NIC
30 NIC
31 NIC
32 NIC
33 NIC
34 NIC
35 NIC
36 NIC
37 NIC
38 NIC
39 GND
40 NIC
41 NIC
42 NIC
43 CLK
44 RST#
45 GNT#
46 REQ#
47 AD[31]
48 AD[30]
49 AD[29]
50 AD[28]
51 AD[27]
52 VDD

Center:
STG2000
208-pin PQFP

Right pins (156–105):
156 VDD
155 OE0#
154 OE1#
153 OE2#
152 OE3#
151 GND
150 CAS02[0]#
149 CAS02[1]#
148 CAS02[2]#
147 CAS02[3]#
146 VDD
145 CAS13[0]#
144 CAS13[2]#
143 CAS13[1]#
142 CAS13[3]#
141 GND
140 DACCS#
139 NIC
138 NIC
137 WE03#
136 WE12#
135 VSYNC
134 HSYNC
133 LOADCLK
132 VDD
131 BLANK#
130 VCLK
129 GND
128 MCLKx2
127 EN64
126 EECS
125 EESCLK
124 EESD
123 INTA#
122 IRQB
121 IRQC
120 IRQD
119 GND
118 NIC
117 NIC
116 NIC
115 NIC
114 VDD
113 NIC
112 NIC
111 NIC
110 NIC
109 NIC
108 NIC
107 NIC
106 NIC
105 GND

Bottom pins (53–104):
GND, AD[26], AD[25], AD[24], C/BE#[3], IDSEL, AD[23], AD[22], AD[21], AD[20], AD[19], AD[18], VDD, AD[17], GND, AD[16], C/BE#[2], FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, NIC, NIC, VDD, GND, SERR#, PAR, C/BE#[1], AD[15], AD[14], AD[13], AD[12], AD[11], AD[10], AD[9], AD[8], VDD, GND, AD[7], AD[6], AD[5], AD[4], AD[3], AD[2], AD[1], AD[0], NIC, NIC, NIC, VDD

NOTES

1 NIC = No Internal Connection. Do not connect to these pins.

2 VDD=3.3V

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2 PIN DESCRIPTIONS

2.1 VL-BUS INTERFACE

Signal	I/O	Description
RESET#	I	System reset signal asserted after system power-up and before any valid CPU cycles occur. The memory configuration and system bus interface are latched on the rising (trailing) edge of RESET#.
LCLK	I	Local CPU clock. A ×1 clock following the same phase as a 486-type CPU.
RDYRTN#	I	Ready Return. This signal is driven by the VL-Bus controller to establish a handshake indicating to the VL-Bus slave devices that the cycle has ended.
WBACK#	I	WBACK# is an output of the VL-Bus Controller which indicates to the STG2000, while acting as a bus master, that the current cycle should be backed off. This is typically done for the controller to perform a memory coherency operation (i.e. write a cache line back into system DRAM). It is sampled on the rising edge of LCLK.
A[31:2]	I/O	30-bit address bus.
D[31:0]	I/O	32-bit data bus.
BE[3:0]#	I/O	Byte enable signals indicating which byte streams of the 32-bit data bus contain valid data in the current bus transfer. These signals are driven by the STG2000 when acting as a bus master.
M/IO#	I/O	Indicates if an I/O or memory access is currently executing on the VL-Bus. M/IO# = 1 indicates a memory cycle, M/IO# = 0 indicates an I/O cycle. This signal is driven by the STG2000 when acting as a bus master.
W/R#	I/O	Indicates if a read or write access is currently executing on the VL-Bus. W/R# = 1 indicates a write access, W/R# = 0 indicates an read access. This signal is driven by the STG2000 when acting as a bus master.
D/C#	I/O	Data/code status. This signal indicates whether the current cycle is transferring data or code. When a master, STG2000 always drives this signal high (data).
BLAST#	I/O	Burst last. This signal indicates that the next time BRDY# is asserted, the burst cycle will complete. This signal is driven by the STG2000 when acting as a bus master.
ADS#	I/O	Address data strobe. This signal is strobed by the VL-Bus controller for one clock cycle after validation of the address bus and status lines on the VL-Bus. This signal is driven by the STG2000 when acting as a bus master
LEADS#	I/O	Local External Address Data Strobe. The VL-Bus controller or active VL-Bus master asserts this signal whenever an address that performs a CPU cache invalidation cycle is present on the bus. This signal is driven by the STG2000 when acting as a bus master.
LGNT#	I	Local Bus Grant. This signal is used in conjunction with LREQ# to establish a VL-Bus arbitration protocol. When the STG2000 asserts LREQ#, the VL-Bus controller responds by asserting LGNT# for that slot. The active VL-Bus master then has control of the bus until released by the bus master or until the bus controller removes LGNT#.
LDEV#	O	Local Device. This signal is asserted when in slave mode by the STG2000 to inform the VL-Bus controller that the current cycle is a VL-Bus cycle.
LRDY#	O	Local Ready. This signal begins the handshake terminating the current active bus cycle. LRDY# is driven by the STG2000 only when in slave mode.
BRDY#	I/O	Burst Ready. This signal terminates the current active burst cycle. BRDY# is asserted low for one LCLK period at the end of each burst cycle.

Signal	I/O	Description
LREQ#	O	Local request. This signal is used in conjunction with LGNT# to gain gontrol of the bus and become an active bus master. When the STG2000 asserts LREQ#, the VL-Bus controller responds by asserting LGNT# for that slot. The VL-Bus device then has control of the VL-Bus and may hold the bus until the controller removes LGNT#.
IRQA, IRQB, IRQC, IRQD	O	Interrupt Request Lines. These interrupt signals are active high, level triggered interrupts that are connected to the IRQ lines on the ISA bus.

2.2 PCI BUS INTERFACE

Signal	I/O	Description
CLK	I	PCI clock. This signal provides timing for all transactions on the PCI bus, except for RST# and INTA#. All PCI signals are sampled on the rising edge of CLK and all timing parameters are defined with respect to this edge.
RST#	I	PCI reset. This signal is used to bring PCI-specific registers, sequencers and signals to a consistent state. When RST# is asserted all PCI output signals are tristated.
AD[31:0]	I/O	32-bit multiplexed address and data bus. A bus transaction consists of an address phase followed by one or more data phases.
C/BE[3:0]#	I/O	Multiplexed bus command and byte enable signals. During the address phase of a transaction C/BE[3:0]# define the bus command, during the data phase C/BE[3:0]# are used as byte enables. The byte enables are valid for the entire data phase and determine which byte lanes contain valid data. C/BE[0]# applies to byte 0 (LSB) and C/BE[3]# applies to byte 3 (MSB).
PAR	I/O	Parity. This signal is the even parity bit generated across AD[31:0] and C/BE[3:0]#. PAR is stable and valid one clock after the address phase. For data phases PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after completion of the current data phase. The master drives PAR for address and write data phases; the target drives PAR for read data phases.
FRAME#	I/O	Cycle frame. This signal is driven by the current master to indicate the beginning of an access and its duration. FRAME# is asserted to indicate that a bus transaction is beginning. Data transfers continue while FRAME# is asserted. When FRAME# is deasserted, the transaction is in the final data phase.
IRDY#	I/O	Initiator ready. This signal indicates the initiator's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are sampled as being asserted. During a write, IRDY# indicates that valid data is present on AD[31:0]. During a read, it indicates that the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	I/O	Target ready. This signal indicates the target's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock when both TRDY# and IRDY# are sampled as being asserted. During a read, TRDY# indicates that valid data is present on AD[31:0]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	I/O	STOP# indicates that the current target is requesting the master to terminate the current transaction.
IDSEL	I	Initialization device select. This signal is used as a chip select during configuration read and write transactions.

Signal	I/O	Description
DEVSEL#	I/O	Device select. When acting as an output **DEVSEL#** indicates that the STG2000 has decoded the PCI address and is claiming the current access as the target. As an input **DEVSEL#** indicates whether any other device on the bus has been selected.
REQ#	O	Request. This signal is asserted by the STG2000 to indicate to the arbiter that it desires to become master of the bus.
GNT#	I	Grant. This signal indicates to the STG2000 that access to the bus has been granted and it can now become bus master.
SERR#	O	System error. This signal is used by the STG2000 to report parity errors and significant system errors. **SERR#** is pure open drain and is actively driven for a single PCI clock, the assertion of **SERR#** being synchronous to that clock.
INTA#	O	Interrupt request line. This open drain output is asserted and deasserted asynchronously to **CLK**.
IRQB, IRQC, IRQD	O	Interrupt Request Lines. These interrupt signals are active high, level triggered interrupts that may be connected to the IRQ lines on the ISA bus.

2.3 DRAM MEMORY INTERFACE

Signal	I/O	Description
MD[31:0]	I/O	The 32-bit memory data bus. **MD[31:0]** are also used to load pixel data into the Palette-DAC, **MD[7:0]** to access the 8-bit EPROM, **MD[15:8]** to access the Palette-DAC and **MD[30:16]** to address the 32KByte EPROM.
MA02[8:0]	O	Memory Address bus for DRAM banks 0 and 2. Supports symmetric address 256K x n memory architectures.
MA13[8:0]	O	Memory Address bus for DRAM banks 1 and 3. Supports symmetric address 256K x n memory architectures.
RAS#	O	Row Address Strobe for all memory banks.
CAS02[3:0]#	O	Column Address Strobe for each byte in DRAM banks 0 and 2.
CAS13[3:0]#	O	Column Address Strobe for each byte in DRAM banks 1 and 3.
WE03#	O	Write Enable for DRAM banks 0 and 3.
WE12#	O	Write Enable for DRAM banks 1 and 2.
OE0#, OE1#, OE2#, OE3#	O	Output Enable for each DRAM bank.
EN64	O	This output is used in 2 and 4MByte framestores which interface to the STG1764. When high this pin tri-states external bus transceivers between two 32-bit interfaces to the 64-bit Pixel Port of the STG1764. When low this pin enables the connection between the two 32-bit interfaces.
MCLKx2	I	Memory Clock x 2. This signal provides a timing reference to all internal functions of the STG2000. This clock is sourced from the STG1732/64 memory clock output. **MCLKx2** runs at twice the frequency of the internal memory clock.

2.4 EEPROM INTERFACE

Signal	I/O	Description
EECS	O	EEPROM chip select. This signal requires an external 50KΩ pull-down to hold the EEPROM in a quiescent state during reset.
EESD	I/O	EEPROM bidirectional data.

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Signal	I/O	Description
EESCLK	O	EEPROM Clock. Data is clocked into/out of the 93C46A based on the rising edge of this clock as defined by the Microwire protocol.

2.5 DISPLAY INTERFACE

Signal	I/O	Description
DACCS#	O	Enables the Palette-DAC to be accessed via the data bus. This pin is used in conjunction with MD[31:0] to load pixel data and MD[15:8] to access the Palette-DAC register.
LOADCLK	O	Connects to the Palette-DAC LOADCLK pin. The rising edge of this signal controls sampling on the Palette-DAC LOADEN# and pixel input pins.
BLANK#	O	Blanking signal sampled by the Palette-DAC on the rising edge of VCLK. A '0' sampled will, after a pipeline delay, turn the DAC outputs off. A special protocol on the Palette-DAC BLANK# and VCLK pins enables the controller to reset various functions of the Palette-DAC at the start of frame flyback.
VCLK	I	Video Clock. This clock is sourced from the Palette-DAC memory clock output. The VCLK frequency is the video frequency at the DACs divided by 1, 2, 4, 8, or 16, depending on the selected mode.
VSYNC	O	Vertical sync supplied to the display monitor. No buffering is required to drive a local monitor.
HSYNC	O	Horizontal sync supplied to the display monitor. No buffering is required to drive a local monitor.

2.6 AUDIO CODEC INTERFACE

Signal	I/O	Description
AUW#	O	Audio Write command strobe.
AUR#	O	Audio Read command strobe.
AUA[1:0]	O	Audio Address outputs.
AUD[7:0]	I/O	Audio Data bus. These pins transfer data and control information between the Audio Codec and the STG2000.
AUPD#	O	Places the Audio Codec in its low power consumption mode.

2.7 DEVICE ENABLE SIGNALS

Signal	I/O	Description
ROMCS#	O	Enables reads from an external 32Kx8 EPROM or Flash ROM. This signal is used in conjunction with MD[7:0] for the ROM data bus, MD[30:16] for the 15-bit address, and MD[31] for the R/W# select.
ALTCS#	O	Allows an 8-bit external device with up to 32KBytes of address space to be accessed via the memory data bus. This signal is used in conjunction with MD[7:0] for an 8-bit data bus, MD[30:16] for the 15-bit address bus, and MD[31] for the R/W# select.

3 OVERVIEW OF THE STG2000

3.1 COHERENT MULTIMEDIA ARCHITECTURE

The STG2000 is the first in a family of Multimedia Accelerators based on the NV Architecture™. The NV Architecture is a media I/O architecture, created to provide a coherent and high-performance foundation for multimedia peripherals, such as audio, video, 3D graphics, input and communication devices. The NV Architecture provides the benefits of high interactivity, concurrency, and quality for today's and tomorrow's multimedia applications.

3.2 GUI ACCELERATION

- The STG2000's graphics engine delivers industry-leading Windows acceleration performance
- Optimized for minimal software overhead
- Accelerated primitives including BLT, transparent BLT, stretchBLT, points, lins, lines, polylines, polygons, fills, patterns, text, and arbitrary rectangular clipping
- 200-400MBytes/s rendering bandwidth
- Pipeline optimized for multiple color depths including 8, 15, 24, and 30 bits per pixel
- Execution of all 256 Raster Operations (as defined by Microsoft Windows) at 8, 15, 24 and 30-bit color depths
- Data may be rendered into the frame buffer or system memory via bus-mastering DMA
- Hardware accelerated color dithering

3.3 CONCURRENT HIGH-FIDELITY AUDIO SYNTHESIS

The STG2000 Multimedia Accelerator integrates a high performance audio engine to deliver the highest fidelity and realism for today's interactive multimedia applications. With support for dynamic downloadable samples, developers can utilize custom samples for exciting sound and MIDI effects. Additionally, the NV Architecture's native synchronization capability allows developers to precisely control the relationship of audio playback to 3D graphics, video, or other audio streams. This capability is necessary for a truly interactive experience.

- On-chip 350MIPS audio engine and bus-mastering DMA accelerates synthesis and

mixing of high-fidelity audio with little CPU overhead

- Up to 32 channels of 16 bits wavetable-synthesized sound
- Concurrent playback and mixing of up to 50 channels digital audio
- Playback and recording of 16-bit samples at sampling rates up to 48 KHz
- Wavetable samples stored in system memory instead of expensive ROM or dedicated RAM
- Each voice has independent envelope and effects generator, volume control, and sample rate conversion with interpolation
- Concurrent playback (audio out) and record (audio in) ideal for telephony applications
- Audio effects:
  - Effects processing such as tremolo, vibrato, and portamento on any audio stream without performance degradation
  - Precise control of phase-shifting and delay to enable effects such as reverb and 3D audio creation
- Support for industry audio standards:
  - Multimedia APIs in Windows 3.1 and Windows 95
  - MPU-401, General MIDI, Miles Audio Interface Library (AIL), HMI Sound Operating System (SOS)
  - Compatibility with DOS audio standards

3.4 REAL-TIME PHOTOREALISTIC 3D GRAPHICS

The STG2000 Multimedia Accelerator hardware provides acceleration for rendering real-time texture-mapped 3D graphics. The 3D graphics algorithms were created specifically for the needs of the consumer multimedia market, where the primary application is interactive entertainment.

The requirements of the Consumer 3D market are fundamentally different than that of MCAD 3D. Consumer 3D requires the highest possible frame rate and realism in order to create an entertainment experience that "suspends the player in total disbelief." The traditional MCAD 3D market, on the other hand, requires ease of model creation and scalable performance. Fundamentally, the Consumer 3D market is a playback market, whereas the MCAD 3D market is an authoring market. The professional is looking to increase productivity.

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The consumer is looking for compelling interactivity and reality in an entertainment application. STG2000 achieves the needs of Consumer 3D with the following capabilities:

• Fast polygon rendering

• Texture-mapping engine accelerates rendering of photorealistic environments

• Quadratic texture-mapping for perspective correction and rendering of curved surfaces. Curved surfaces for realistic rendering of complex 3D objects.

• Bilinear texture-mapping

• Surface effects such as diffused lighting and reflection mapping

• Alpha blending for fog, smoke, and transparency

• Anti-aliased sprite animation

• Double buffer for smooth animation

The STG2000 achieves a peak rendering performance of 75 million pixels per second. This level of 3D graphics performance will allow interactive entertainment software to produce photorealistic environments rendered at 800x600 resolution, 64 thousand colors, and 30 frames per second.

3.5 VIDEO TEXTURING

An exciting new feature of the STG2000 Multimedia Accelerator is a capability called video texturing. This unique ability allows the mapping of video onto a surface as if it were a texture. Video in the NV Architecture is treated as a graphics texture which changes at 30 frames/s, and benefits from all of the same powerful warping and lighting functions of the 3D pipeline. (For example mapping video onto a bouncing ball.)

3.6 FULL-MOTION VIDEO ACCELERATION

The STG2000 graphics engine accelerates full-motion video playback and can sustain 30 frames per second of true-color digital video. Hardware video acceleration provides image enhancement and scaling of video streams to full-screen display.

• Horizontal and vertical interpolation for enhanced image quality

• Interframing for reduced flicker

• Integration of graphics and video enabling special effects

• Accelerate playback of industry standard CO-DECs such as MPEG, Indeo, and Cinepak

3.7 ENHANCED DIGITAL GAME PORT

The STG2000 is the first product to feature a digital game port. Where standard game ports demand the near-constant intervention of the PC's microprocessor, STG2000's digital game port DMA-bursts the joystick's position without interrupting the processor. The benefit is better overall system performance, a crucial advantage in multimedia applications. The STG2000 game port also provides higher resolution and sampling rates than standard game ports, enabling a finer degree of joystick control and quicker response to user actions.

• 8-channel digital game port with advanced analog/digital sampler

• 13-bit resolution and programmable sample rate up to 92Hz (versus a typical game port of 8-bit resolution and 1Hz sample rate)

• Frees up to 12% of a Pentium class CPU's bandwidth

3.8 HOST INTERFACE

The STG2000 Multimedia Accelerator has a full 32-bit glueless interface to both the VL and PCI buses. The STG2000 host interface includes a asynchronous FIFO and bus-mastering DMA. Pinouts are organized so that direct trace routes are possible between all pins and edge connector fingers.

3.9 CONCURRENT MEDIA PROCESSING AND SYNCHRONIZATION

The STG2000 can process multiple media streams while running under Windows. For example, a multimedia title could simultaneously render 3D graphics, play back multiple channels of audio, and respond to the control of the user. Furthermore, a 64-bit timer and notifier allows for precise synchronization of audio and graphics for example.

3.10 REAL-TIME PERFORMANCE UNDER WINDOWS

Today, multimedia software developers must choose between the ease of Windows and the speed and concurrency of DOS. For makers of performance-intensive multimedia software, DOS is a necessity. Users get more responsive gameplay, but at the expense of ease-of-use. With the STG2000, developers and users get the best of both worlds. Programs can take advantage of the Windows interface while benefiting from the

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STG2000's hardware acceleration and concurrent media processing.

3.11 CONSUMER PRICE POINT

The STG2000 combines a full suite of advanced multimedia capabilities on a single low-cost chip. It further reduces system costs by allowing the use of the computer's main memory for wavetable samples - unlike most wavetable products, which require expensive additional memory for the purpose. This is made possible by the STG2000's use of the fast local (PCI or VL) bus and an on-chip bus-mastering direct memory access (DMA) controller that communicates with system memory without help from the PC's microprocessor. Overall, the STG2000 makes possible a complete high-performance multimedia subsystem price easily affordable to most consumers and far below the aggregate cost of today's specialized multimedia components.

3.12 SUPPORT FOR STANDARDS

- Multimedia support for MS-DOS, Windows 3.1, Windows 95 and OS/2
- Acceleration for Windows 95 Direct APIs: DirectDraw, DirectSound, and DirectInput
- Major 3D interface (API) support includes Microsoft's 3D-DDI and Rendermorphics, Intel's 3DR and Criterion's RenderWare
- DOS audio standards
- VGA & SVGA: The STG2000 has an industry standard VGA core and BIOS support. The VGA is the standard output device during system boot. In PCI configuration space the VGA can be enabled and disabled independently of the NV device.
- PCI 2.0 bus or VL 2.0 bus interfaces
- VESA Feature Connector
- VESA DPMS Power Management
- IBM game port

3.13 SCREEN RESOLUTIONS

Screen resolutions and refresh rates supported by the STG1732 135MHz 32-bit Palette-DAC include:

Pixel depth	Resolutions and refresh rate supported				
	640× 480	800× 600	1024× 768	1152× 864	1280× 1024
8	96Hz	96Hz	96Hz	85Hz	75Hz
15	96Hz	96Hz	85Hz	70Hz	
24/30	96Hz	75Hz			

Screen resolutions and refresh rates supported by the STG1764 170MHz 64-bit Palette-DAC include:

Pixel depth	Resolutions and refresh rate supported*				
	800× 600	1024× 768	1152× 864	1280× 1024	1600× 1280
8	96Hz	96Hz	96Hz	75Hz	60Hz
15	96Hz	96Hz	96Hz	75Hz	60Hz
24/30	96Hz	85Hz	72Hz		

* STG1764 currently only available at 135MHz

3.14 ADVANCED SEMICONDUCTOR PROCESS

The STG2000 is manufactured on SGS-THOMSON's advanced 0.5 micron, 3 layer metal, 3.3V process with SURE 6 quality and reliability standards. The low power dissipation and reduced output switching noise significantly increases system reliability. Output drivers are 5V-tolerant process compensated for PCI compatibility.

3.15 HIGH-PERFORMANCE MULTIMEDIA SUBSYSTEM

The STG2000 Multimedia Accelerator brings together an unrivaled level of multimedia functionality which previously required dozens of components and multiple PCBs. The parts count for 1, 2 and 4MByte DRAM implementations are as follows:

	1MByte	2MByte	4Mbyte
STG2000	1	1	1
STG1732/64	1	1	1
256K×16 DRAM	2	4	8
Audio CODEC	1	1	1
EPROM	1	1	1
EEPROM	1	1	1
Dual Op-Amp	2	2	2
Total*	9	11	15

*Active components.

3.16 REFERENCE DESIGN KIT

A Reference Design Kit (RDK) is available for the STG2000. This includes all necessary information required to design and manufacture a family of high performance PC Multimedia Accelerator Cards based on the STG2000 with different memory options.

The RDK includes:

- STG2000 and STG1732/64 Palette-DAC Databook

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- 1, 2 & 4 MBytes DRAM Board Schematics
- Gerber/Aperture/Drill files
- Bill of Materials for each board
- BIOS, drivers, utilities/diagnostics

3.17 SOFTWARE DEVELOPMENT KIT

A Software Development Kit (SDK) (which includes header files, sample code, manuals and on-line documentation) is available for Developers taking advantage of the capabilities of NV Architecture.

3.18 OTHER PRODUCTS BASED ON NV ARCHITECTURE™

NVIDIA Corporation provides the NV1, an advanced Multimedia Accelerator supporting VRAM, based on the NV Architecture. For further information on the NV1 contact NVIDIA.

4 HOST BUS INTERFACES

4.1 PCI BUS INTERFACE

PCI capability

The STG2000 supports a glueless interface to PCI (2.0) with both master and slave capabilities. The host interface is fully compliant with the 32-bit PCI (2.0) specification.

The Multimedia Accelerator supports operation up to 33MHz with zero-wait state capability for bursts exceeding 128 bytes and full bus mastering capability handling 32-byte burst reads and 16-byte burst writes.

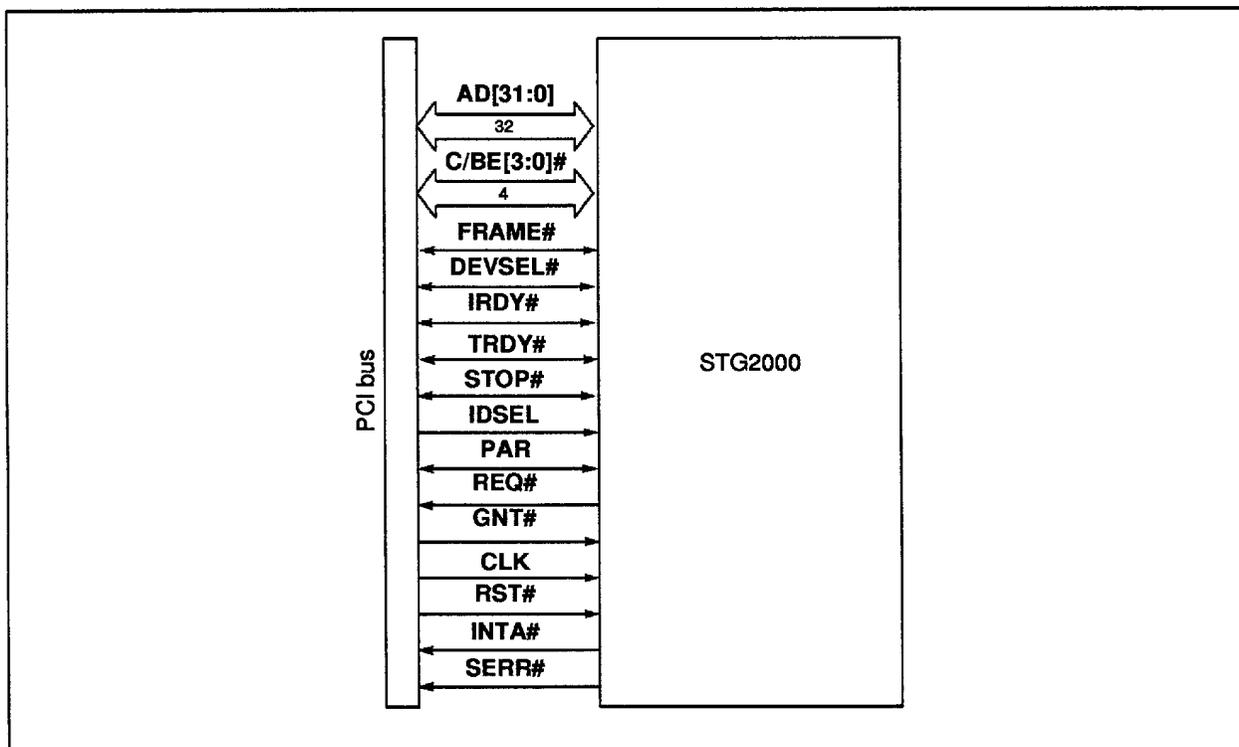**Figure 1.** PCI interface pin connections

Table 1. PCI bus commands supported by the STG2000

Bus master	Bus slave
Memory read and write	Memory read and write
Memory read line	I/O read and write
	Configuration read and write
	Memory read multiple
	Memory read line
	Memory write invalidate

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PCI timing parameters

The timing specification of the PCI interface takes the form of generic setup, hold and delay times of transitions to and from the rising edge of **CLK** as shown in Figure 2.
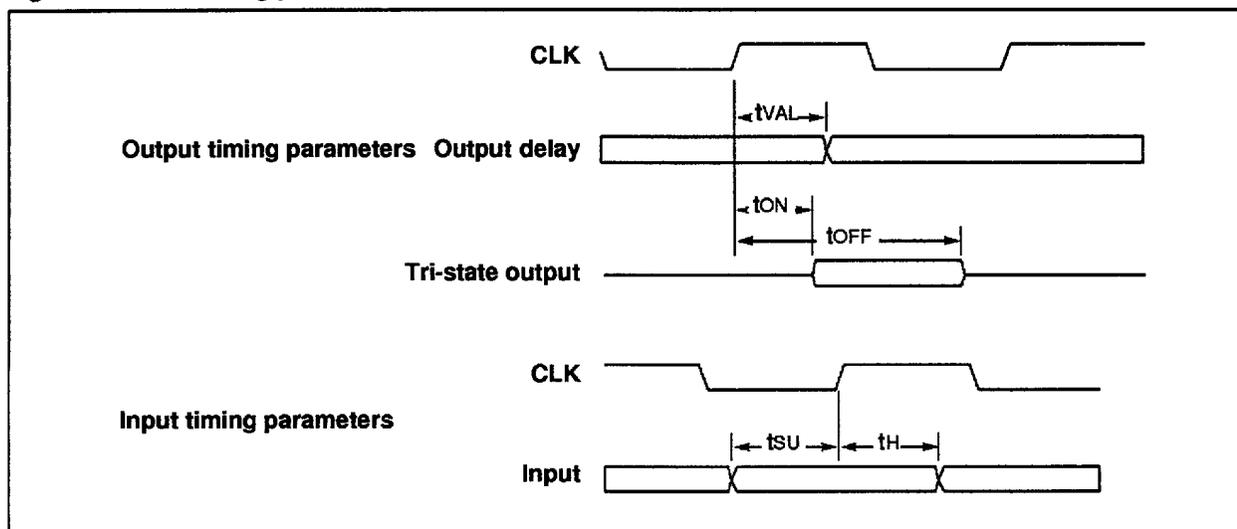
Figure 2. PCI timing parameters

Table 2. PCI timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tVAL	**CLK** to signal valid delay (bussed signals)	2	11	ns	1
tVAL$^{(PTP)}$	**CLK** to signal valid delay (point to point)	2	12	ns	1
tON	Float to active delay	2		ns	
tOFF	Active to float delay		28	ns	
tSU	Input set up time to **CLK** (bussed signals)	7		ns	1
tSU$^{(PTP)}$	Input set up time to **CLK** (GNT#)	10		ns	1
tH	Input hold time from **CLK**	0		ns	

NOTE

    1   **REQ#** and **GNT#** are point to point signals and have different valid delay and input setup times than bussed signals. All other signals are bussed.

Figure 3. PCI Target write - Slave Write (single 32-bit with 1-cycle **DEVSEL#** response)
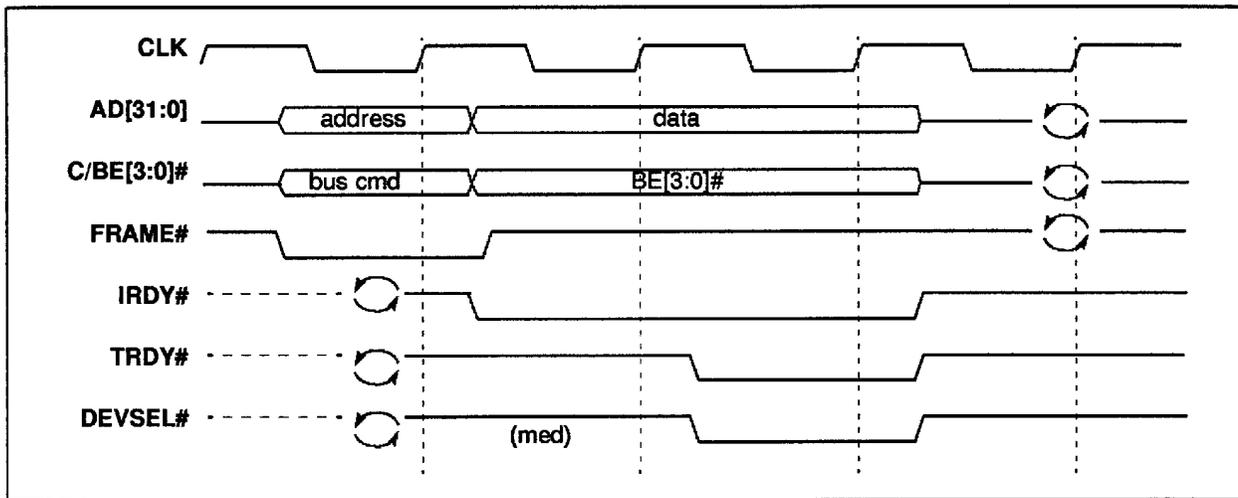
Figure 4. PCI Target write - Slave Write (multiple 32-bit with zero wait state **DEVSEL#** response)

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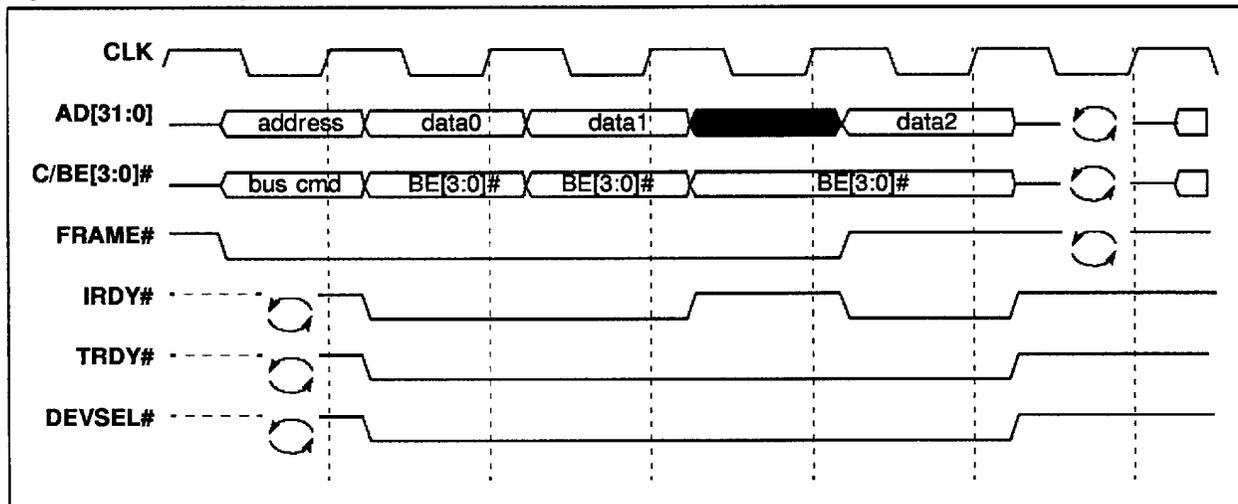
Figure 5. PCI Target read - Slave Read (1-cycle single word read)
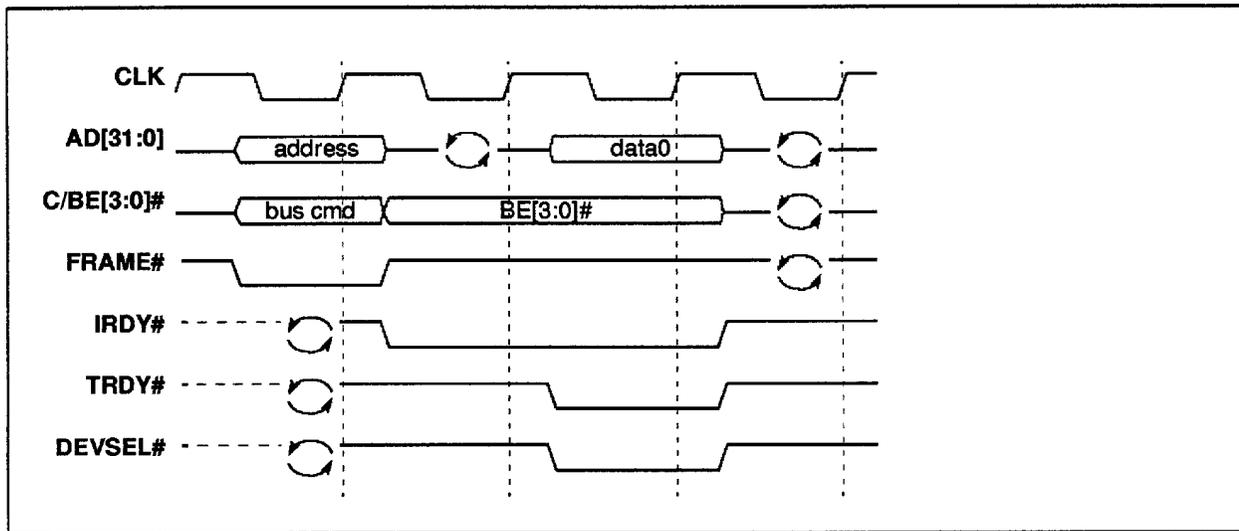
Figure 6. PCI Target read - Slave Read (slow single word read)

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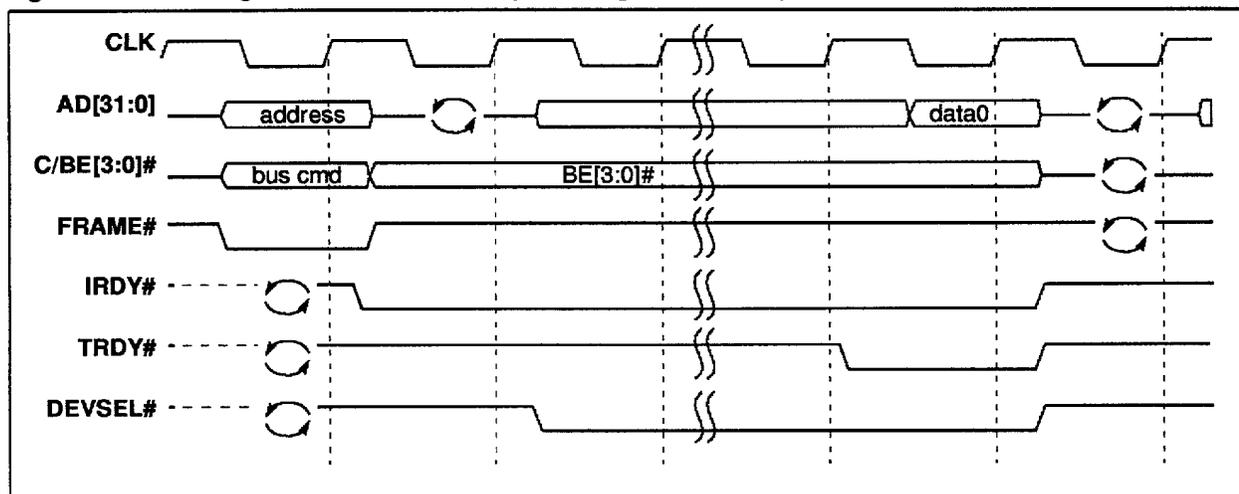
Figure 7. PCI Master write - multiple word
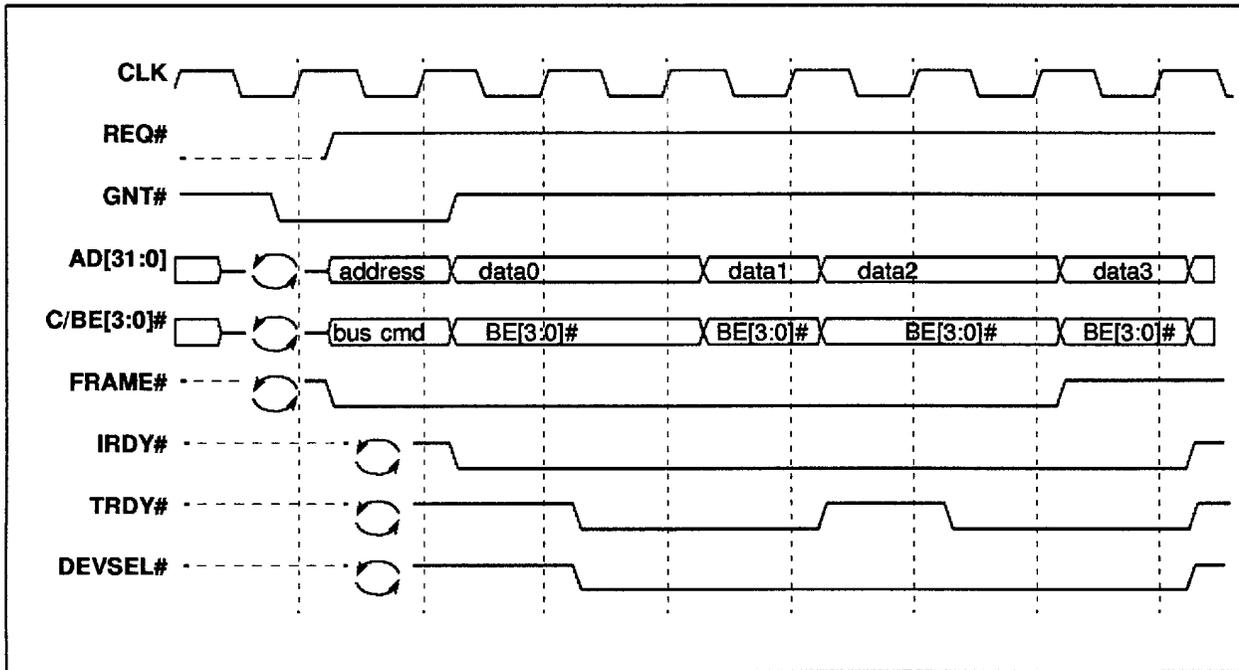
Figure 8. PCI Master read - multiple word
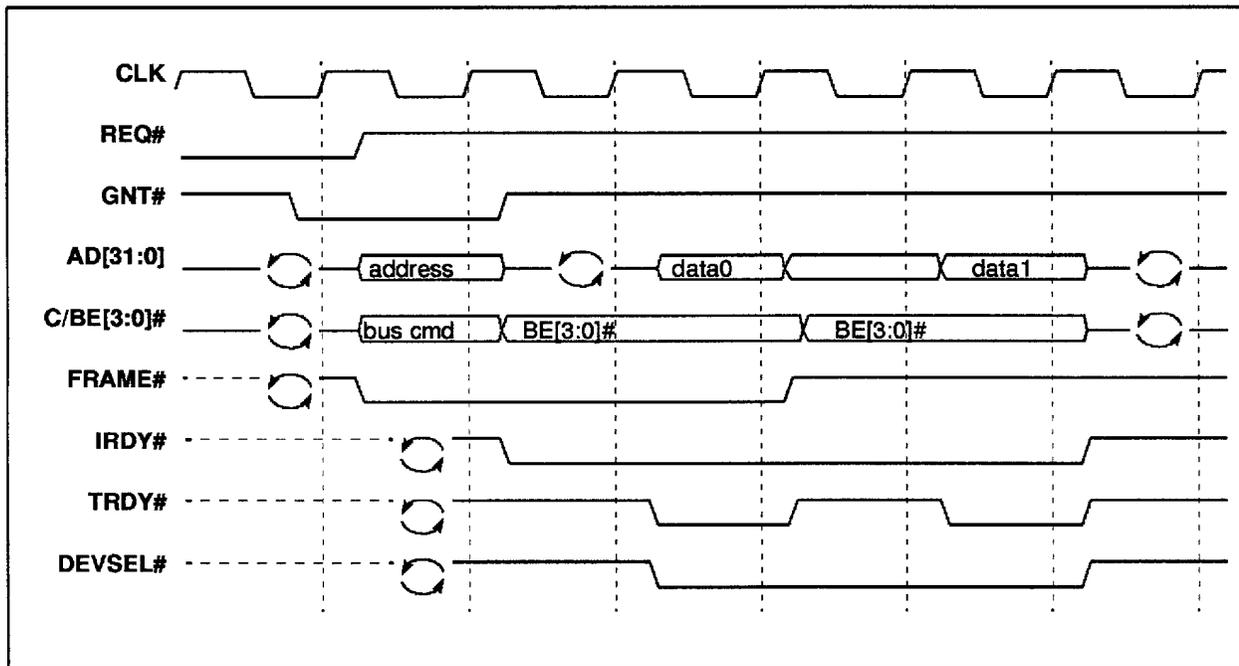
Note: The STG2000 does not generate fast back to back cycles as a bus master

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Figure 9. PCI Target configuration cycle - Slave Configuration Write
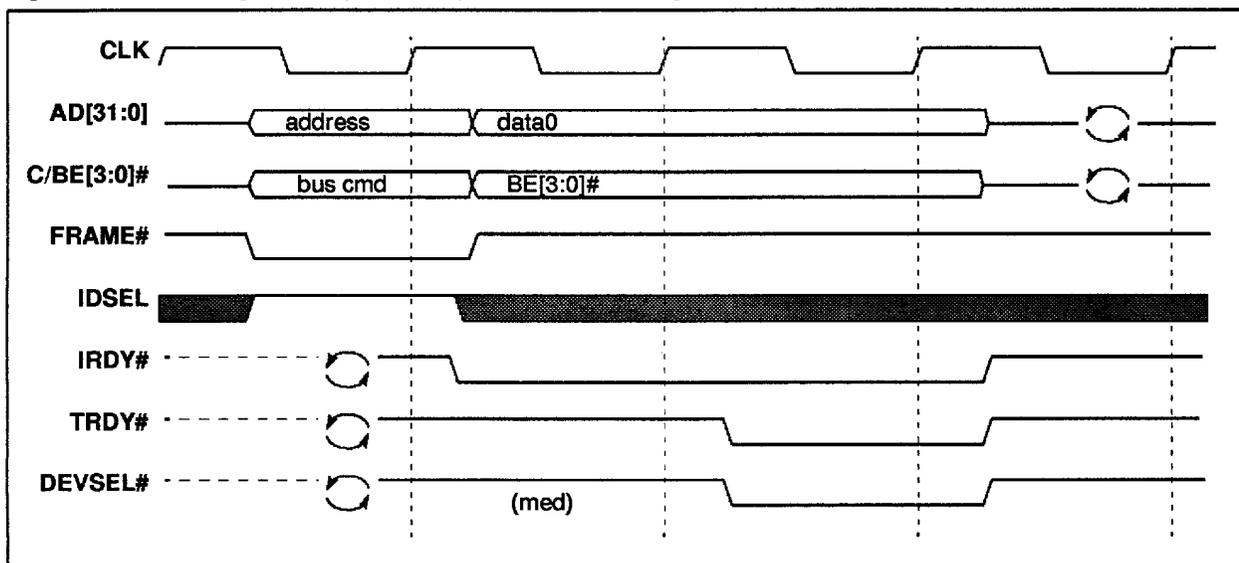
Figure 10. PCI Target configuration cycle - Slave Configuration Read
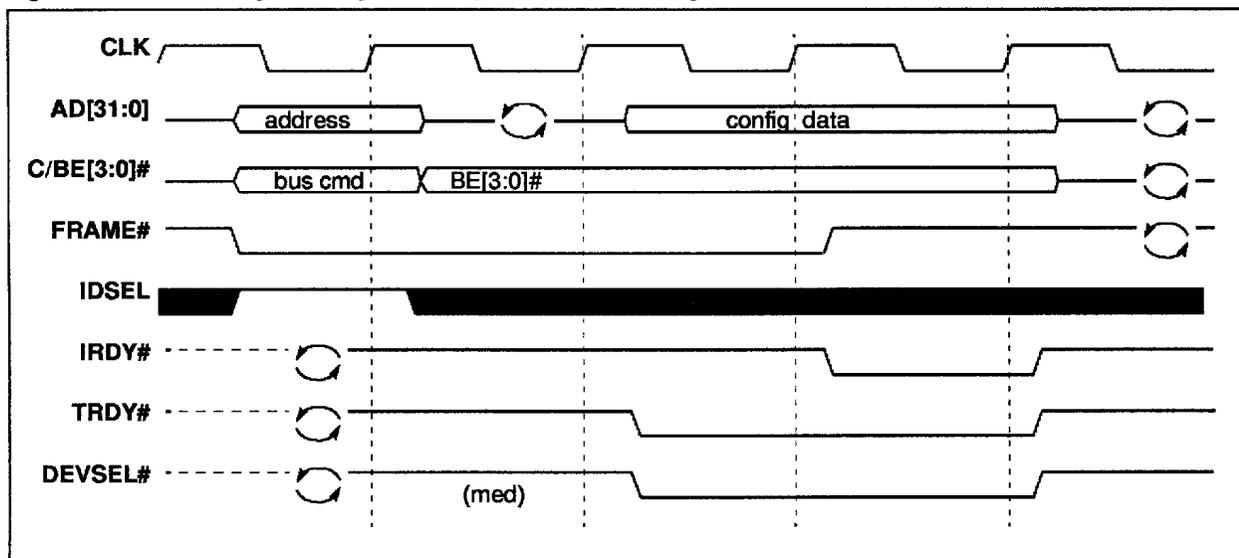
Figure 11. PCI basic arbitration cycle
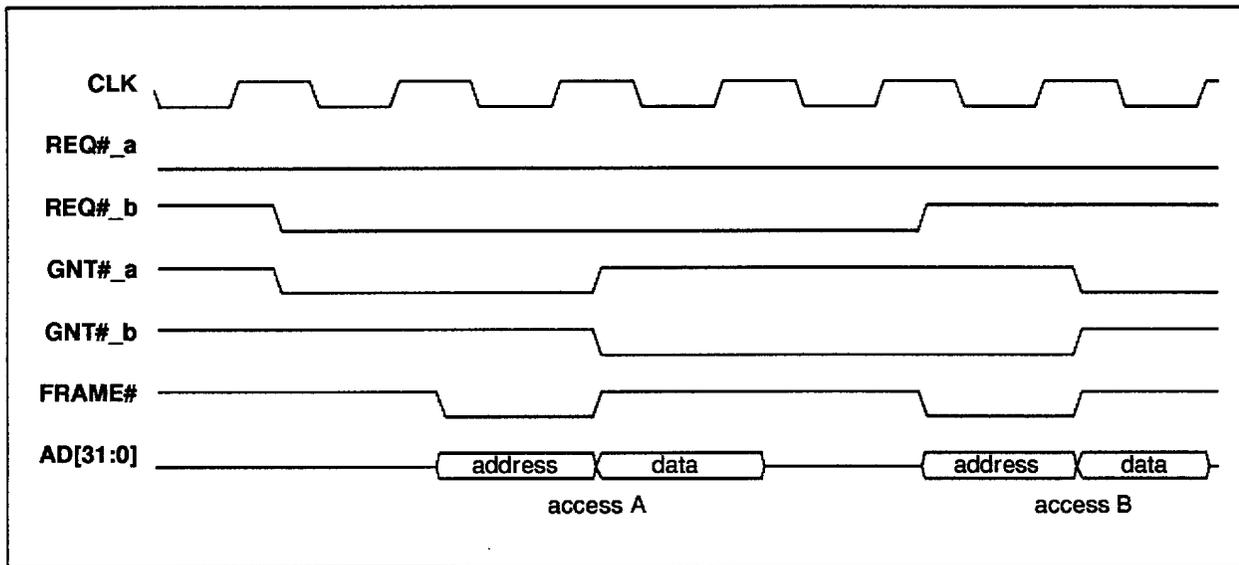
Figure 12. Target initiated termination

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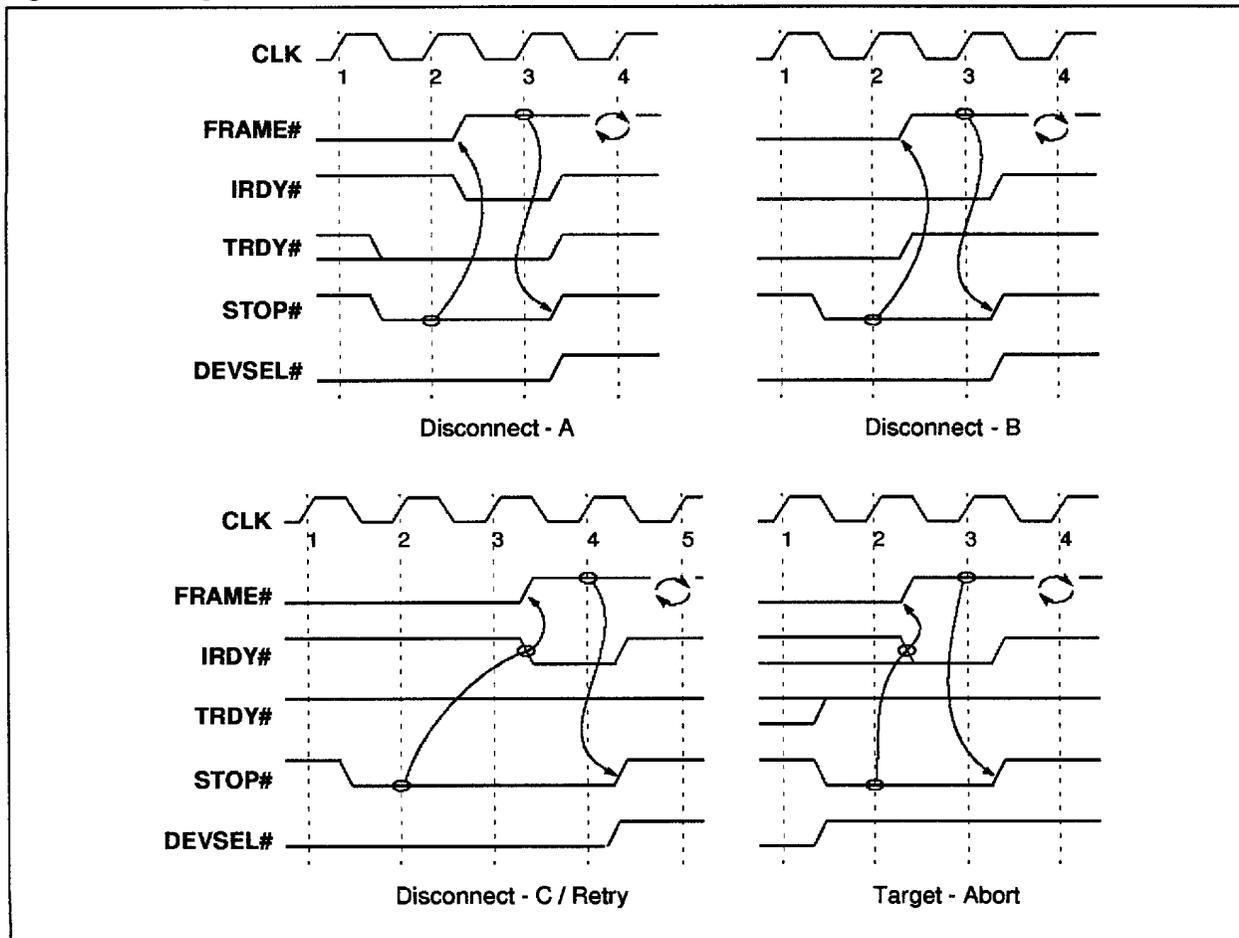
4.2 VL-BUS INTERFACE

VL-bus capability

Most of the Version 2.0 32-bit VL-Bus specification is supported by the STG2000. Unsupported functionality is related to memory coherency protocols intended for caches.

The STG2000 supports operation up to 50MHz, 4 interrupts, a capability for bursts of at least 32 bytes, and a full bus mastering capability handling 32-byte reads and 16-byte writes.

Figure 13. VL-Bus interface pin connections
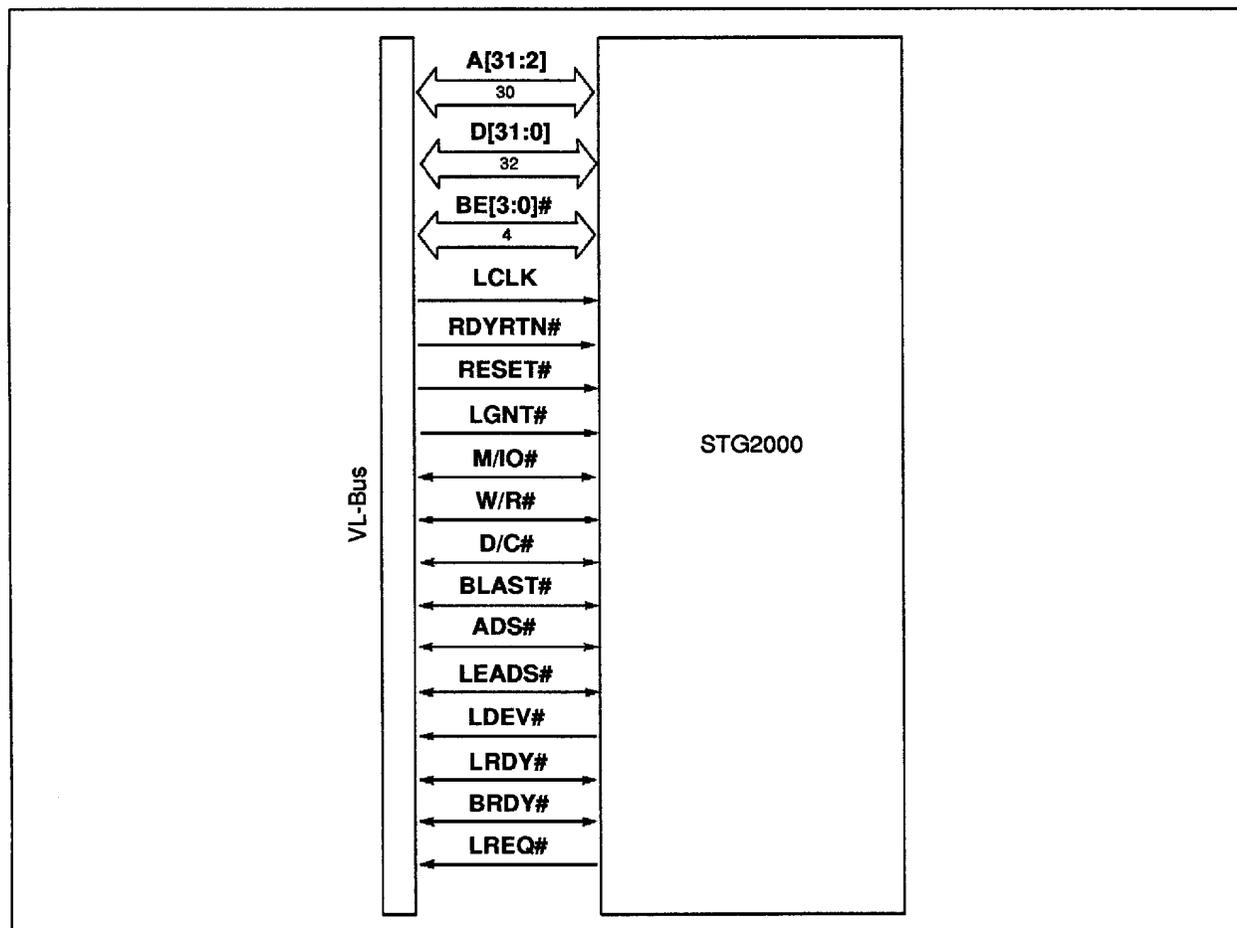
VL-Bus timing specification

Figure 14. VL-Bus clock specification
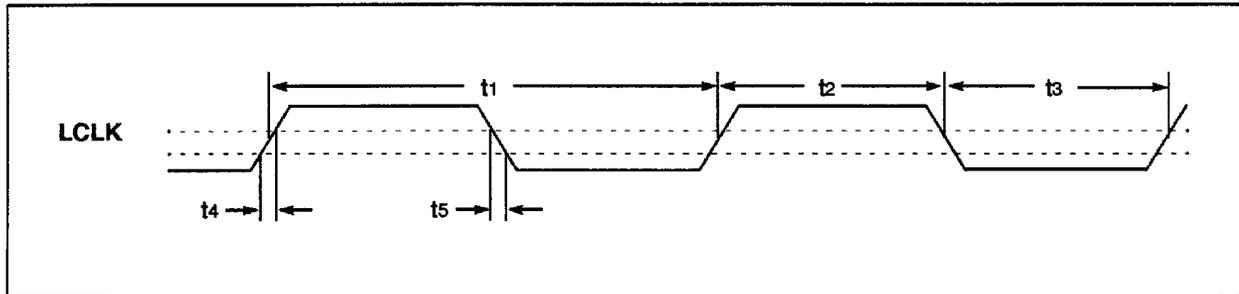
Table 3. VL-Bus clock specification

Symbol	Parameter	Min.	Max.	Unit	Notes
t1	**LCLK** period	20		ns	1
t2	**LCLK** high time	8		ns	
t3	**LCLK** low time	8		ns	
t4	**LCLK** rise time		2	ns	2
t5	**LCLK** fall time		2	ns	3

NOTES
    1 0.1% stability
    2 0.8V to 2.0V
    3 2.0V to 0.8V

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Figure 15. VL-bus Read/Write cycle timing diagram
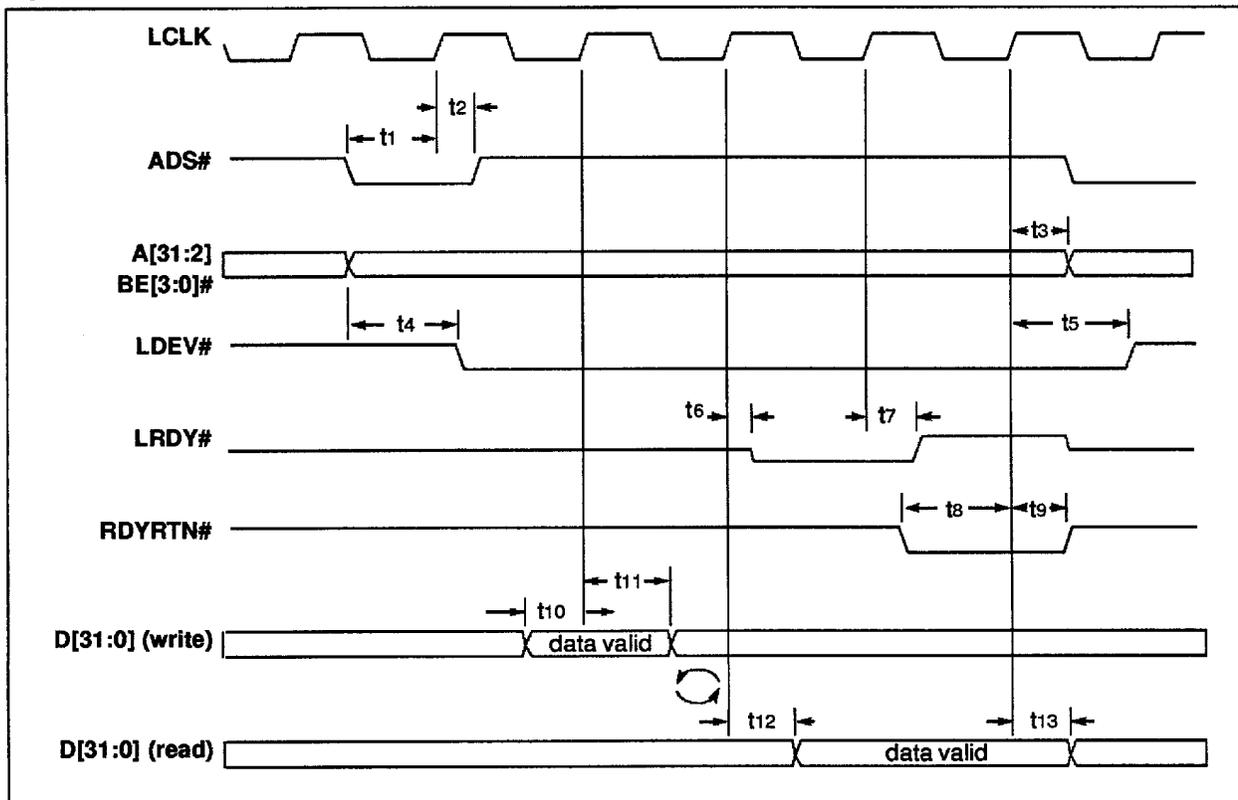
Table 4. VL-bus Read/Write cycle timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
t1	**ADS#** setup to **LCLK** rising			ns	1
t2	**ADS#** hold from **LCLK** rising			ns	1
t3	**A[31:2]** hold from **LCLK** rising			ns	1
t4	**LDEV#** low from **ADR[31:0]** valid			ns	1
t5	**LDEV#** high from **LCLK** rising			ns	1
t6	**LRDY#** low from **LCLK** rising			ns	1
t7	**LRDY#** high from **LCLK** rising			ns	1
t8	**RDYRTN#** low to **LCLK** rising			ns	1
t9	**RDYRTN#** high from **LCLK** rising			ns	1
t10	**D[31:0]** setup to **LCLK** rising (write)			ns	1
t11	**D[31:0]** hold from **LCLK** rising (write)			ns	1
t12	**D[31:0]** valid from **LCLK** rising (read)			ns	1
t13	**D[31:0]** hold from **LCLK** (read)			ns	1

NOTE
1 To be determined

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Figure 16. VL-Bus burst transfers
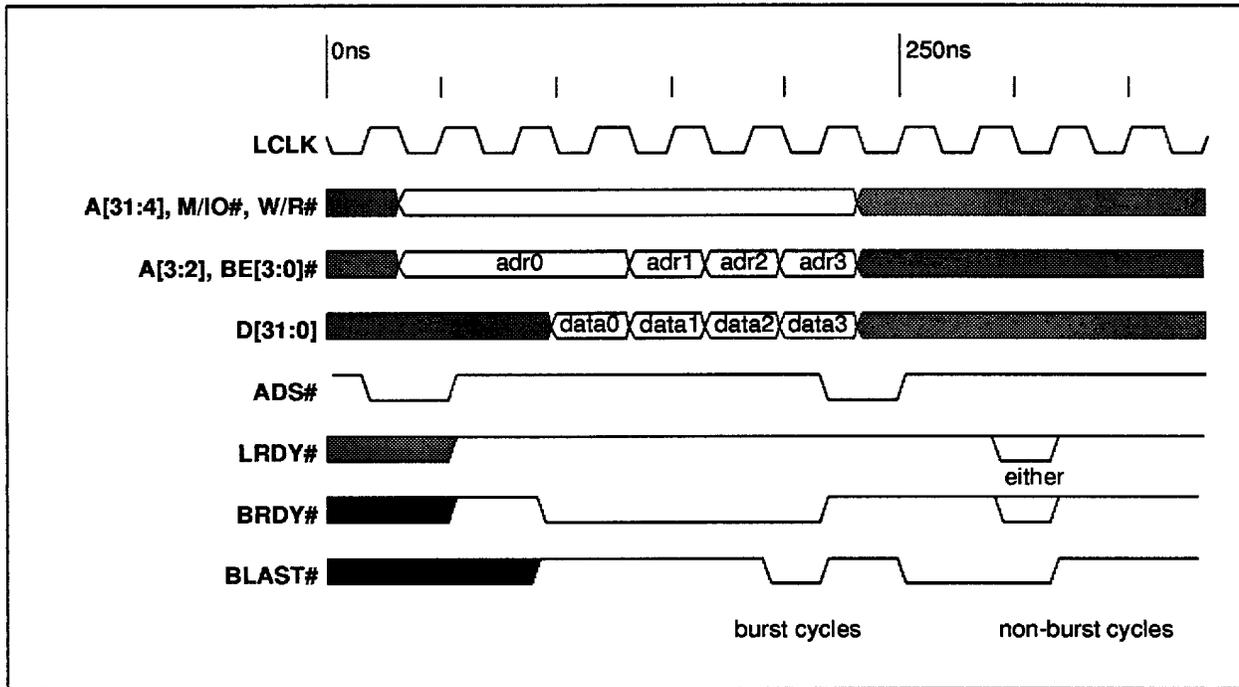
Figure 17. VL-Bus Local Bus Master arbitration timing diagram
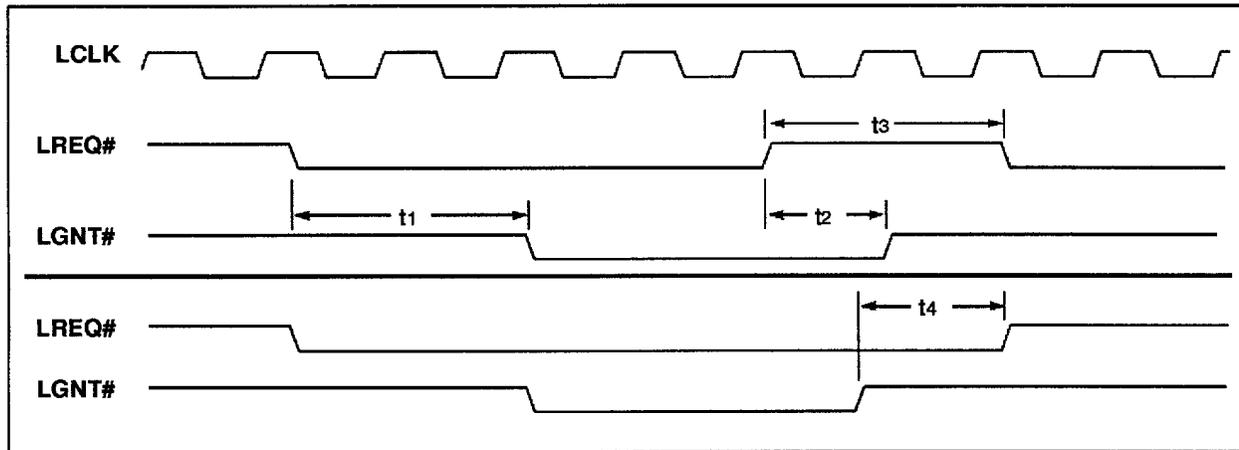
Table 5. VL-Bus Local Bus Master arbitration timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
t1	**LREQ#** falling to **LGNT#** falling	1		LCLK	
t2	**LREQ#** rising to **LGNT#** rising	1	2	LCLK	
t3	**LREQ#** rising to **LREQ#** falling	2		LCLK	
t4	**LGNT#** rising to **LREQ#** rising		5	μs	

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5 MEMORY AND PALETTE-DAC INTERFACE

5.1 DRAM MEMORY INTERFACE

The STG2000 DRAM memory interface is designed primarily for 4Mbit, symmetric address 256K×16, dual CAS# memory devices. The following DRAM memory cycles are supported by the STG2000:

- Random read (non-page mode access)
- Random read with extended data output
- Random write (non-page mode access)
- Fast page-mode read
- Hyper page-mode read with extended data output
- Page-mode write (late write)
- Page-mode write with non-persistent write-per-bit mask
- CAS-before-RAS refresh

The STG2000 can access pixels as 8-bit, 16-bit or 32-bit wide values. The DRAM allocated to the frame buffer is therefore configured to be addressed uniformly in either 8-bit, 16-bit or 32-bit quantities.

The STG2000 memory controller internally generates its own refresh timer. It will request a refresh cycle every 776 MCLK periods. At 50MHz, this represents a refresh request rate of 15.52μs. The refresh operation is exclusively performed by CAS-before-RAS DRAM refresh cycles.

DRAM memory configurations

The STG2000 memory is organized in banks. A memory system consists of one, two, or four banks of DRAM. Each bank consists of two 256K×16 DRAMs comprising 1MByte of storage organized as 256K×32. The STG2000 memory interface comprises a 32-bit DRAM data bus, two 9-bit DRAM address buses and the control signals required to manage up to 4 banks of memory with a 2-to-1 interleave. Figure 18 shows memory interface options for 1, 2 and 4MBytes of DRAM.

The STG2000 supports hyper page mode (extended data output) cycles in some configurations. They include 1MByte with either the STG 1732 or STG1764 DAC, and both 2MByte and 4MByte with the STG1764. The advantage is that very high data transfer rates can occur when using the EDO DRAMs. Bursts from a 64-bit wide EDO memory into the STG1764 occur at up to 400MByte/s. Bursts from a 32-bit 1MByte EDO memory into the STG1732 occur at 200MByte/s.

Standard DRAM is interleaved for improved performance in a 32-bit (STG1732) 2MByte design. This provides a 200MByte/s data transfer rate. Standard 4MByte DRAM designs are also interleaved into the STG1764 at a data transfer rate of 200MByte/s. A 1MByte standard DRAM memory can achieve a 100MByte/s data transfer rate.

Figure 18. 1, 2 and 4MByte DRAM memory configuration options

One bank, non interleaved,
1MByte, 32-bit DAC

Two banks, interleaved, 2MByte, 32-bit DAC

Two banks, interleaved,
2MByte, 64-bit DAC

Four banks, interleaved, 4MByte, 64-bit DAC

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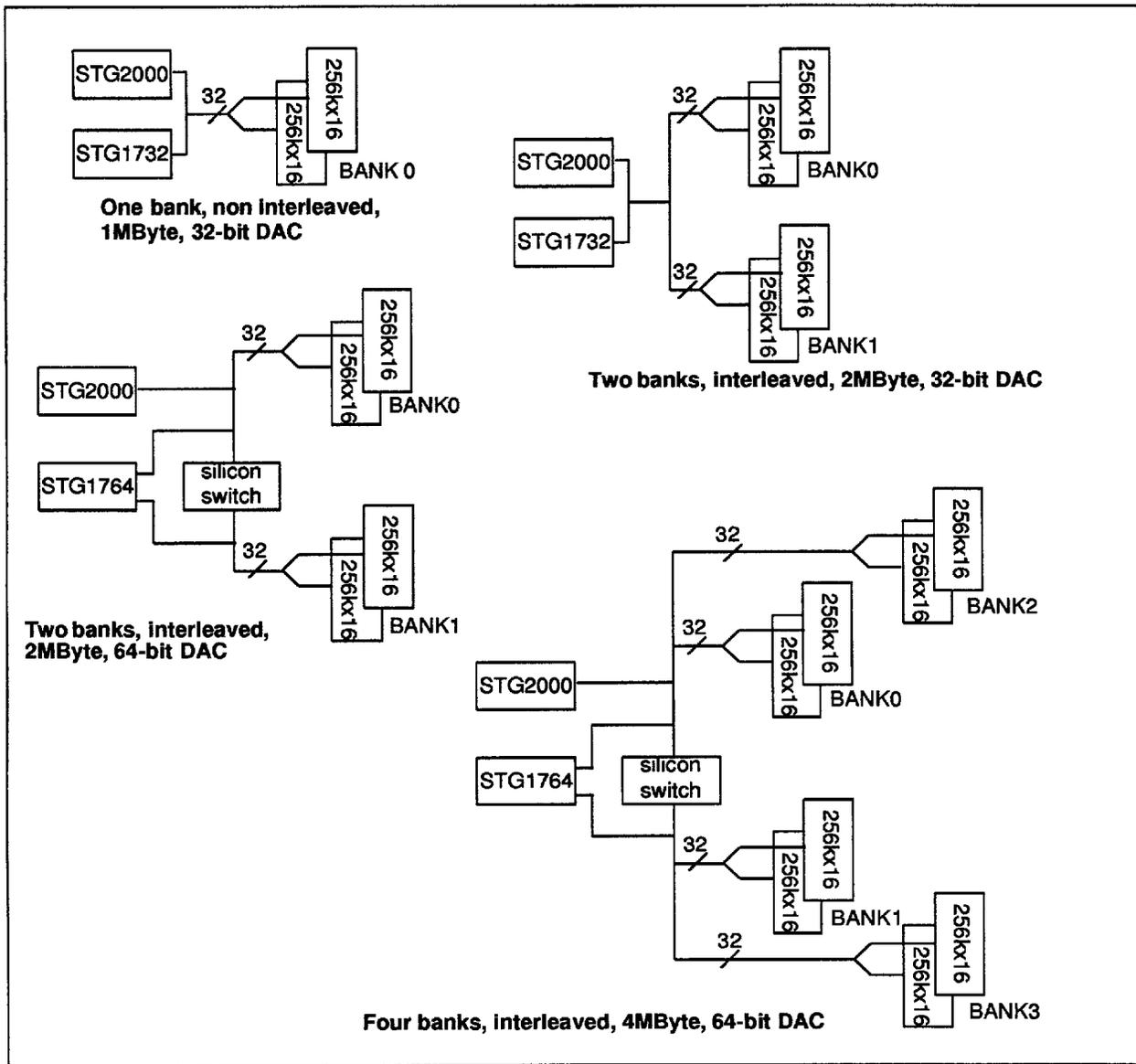
Figure 19. 1-2MByte DRAM configuration with the STG1732 Palette-DAC

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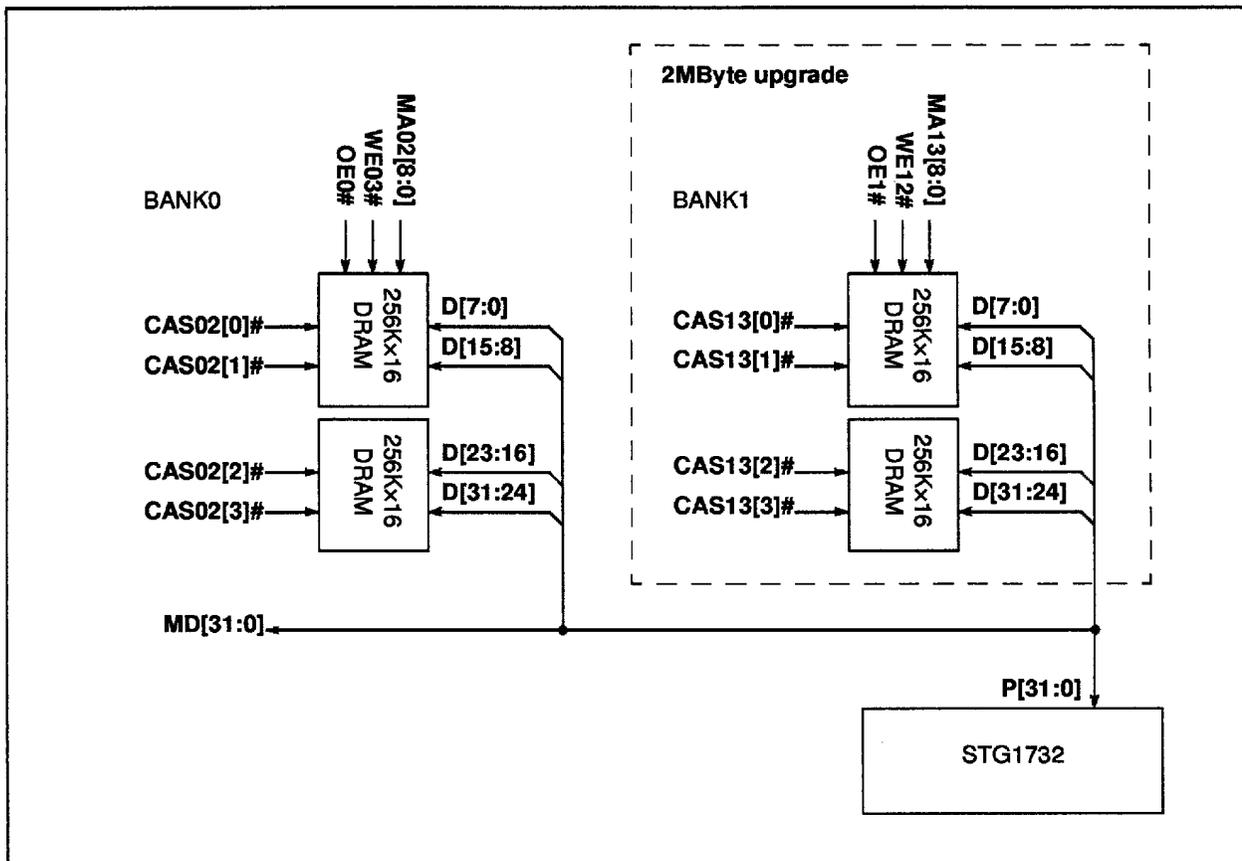
Figure 20. 1-4MByte DRAM configuration with the STG1764 Palette-DAC
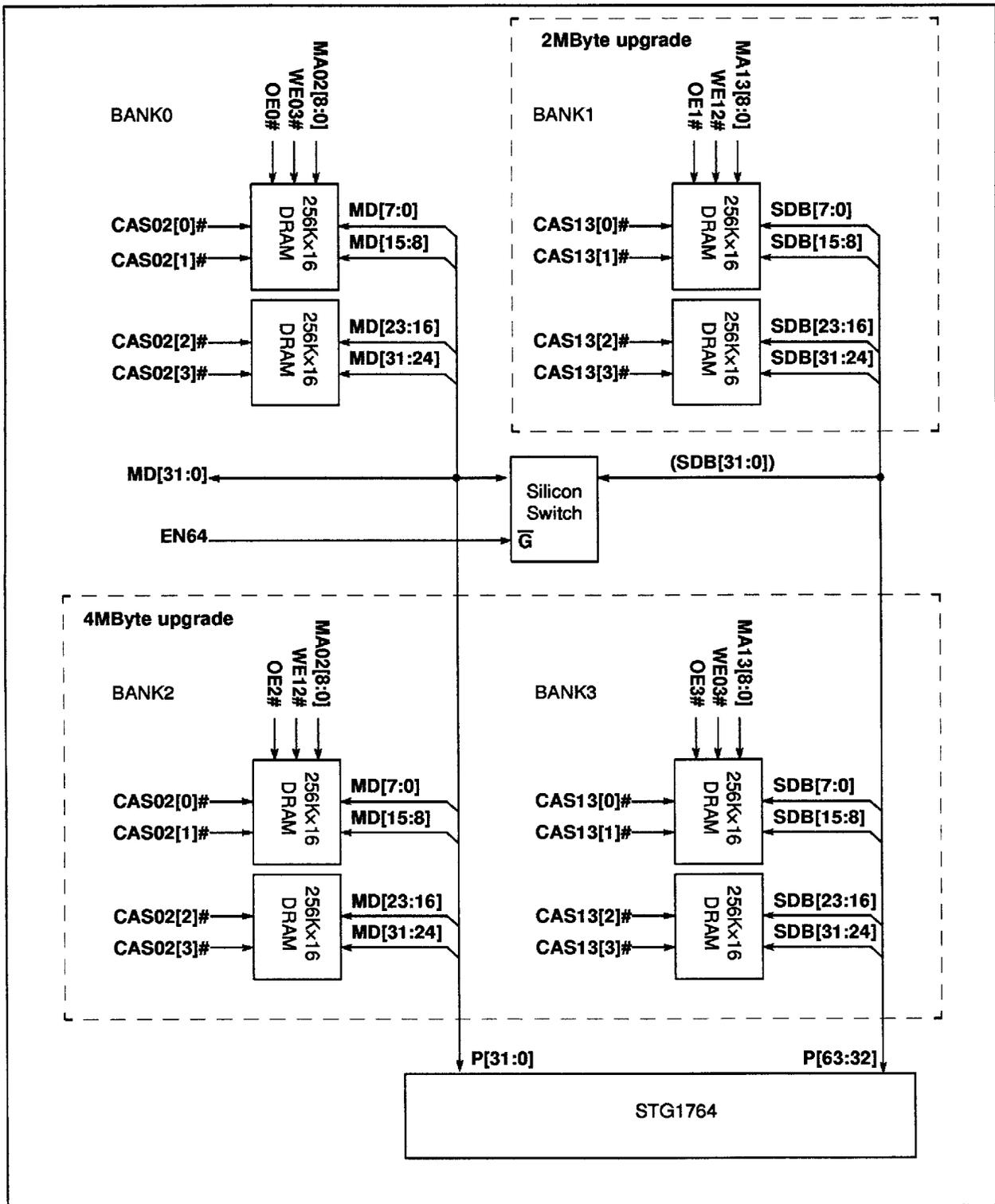
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DRAM interface timing specification

Figure 21. 4MByte DRAM read cycle timing diagram
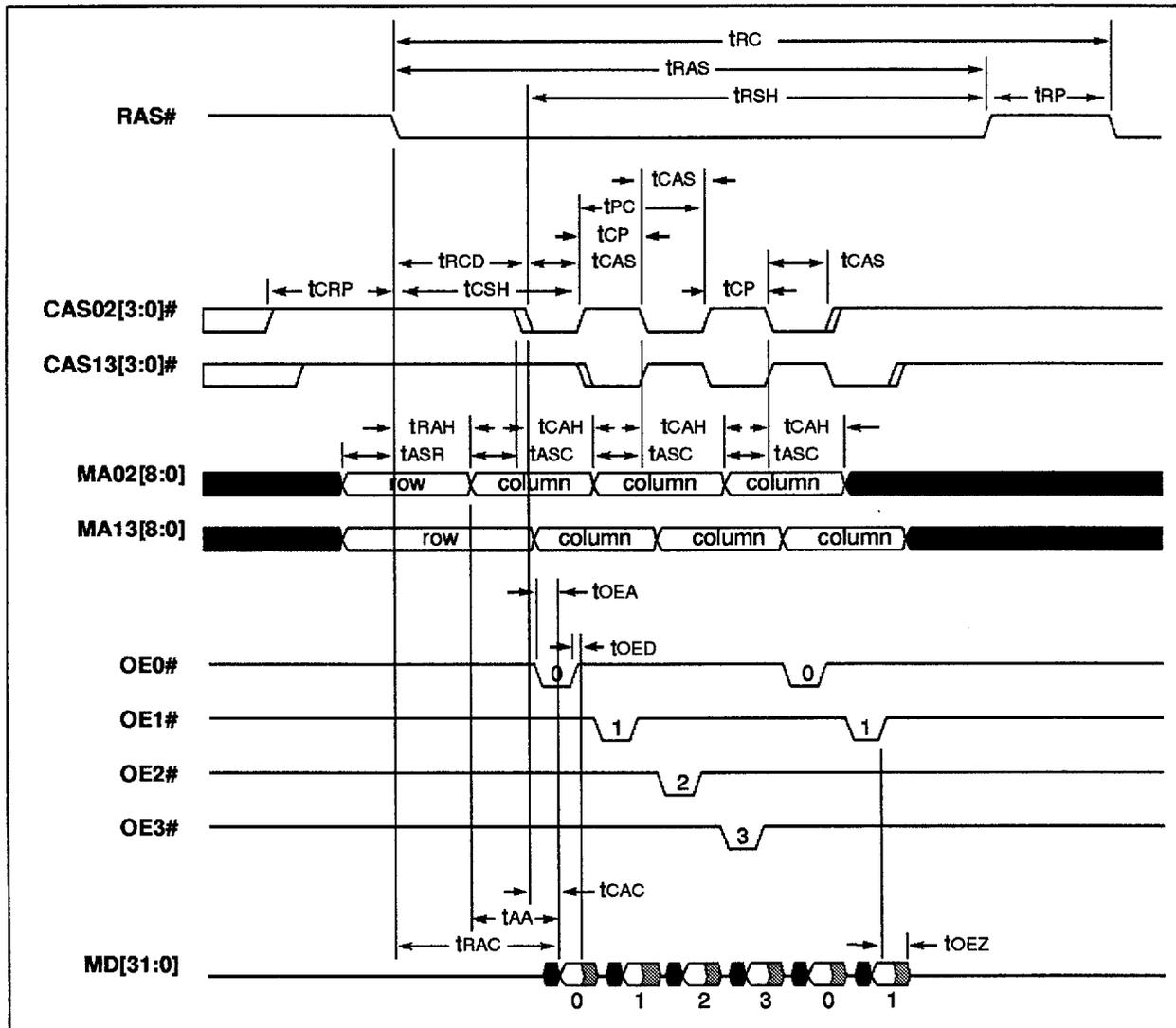
Table 6. 4MByte DRAM read cycle timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tRC	Read cycle time	6TMCLK-5		ns	
tRAS	RAS# pulse width	3.5TMCLK-2		ns	
tRP	RAS# precharge time	2.5TMCLK-2		ns	
tCRP	CASxx[3:0]# to RAS# precharge time	3TMCLK-10		ns	
tCSH	CASxx[3:0]# hold time	3TMCLK-5		ns	
tRCD	RAS# to CASxx[0:3]# delay time	2TMCLK-5		ns	
tRSH	RAS# hold time	1.5TMCLK-2		ns	
tCP	CASxx[3:0]# precharge time (page mode)	TMCLK-5		ns	
tCAS	CASxx[3:0]# pulse width	TMCLK-2		ns	
tASR	Row address setup time	TMCLK-5		ns	
tASC	Column address setup time	TMCLK-5		ns	
tRAH	Row address hold time	TMCLK-5		ns	
tCAH	Column address hold time	TMCLK-5		ns	
tCAC	Access time from CASxx[3:0]#	TMCLK		ns	
tAA	Access time from column address	2TMCLK-5		ns	
tRAC	Access time from RAS#	3TMCLK-2		ns	
tPC	Fast page mode cycle time	2TMCLK-2		ns	
tOEA	Output enable time	TMCLK-7		ns	
tOED	Output disable to data invalid	0		ns	
tOEZ	OEx# rising to MD[31:0] high-z		7	ns	

NOTE

1 TMCLK is the period of the internal memory clock.

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Figure 22. 1MByte DRAM hyper page mode read cycle timing diagram
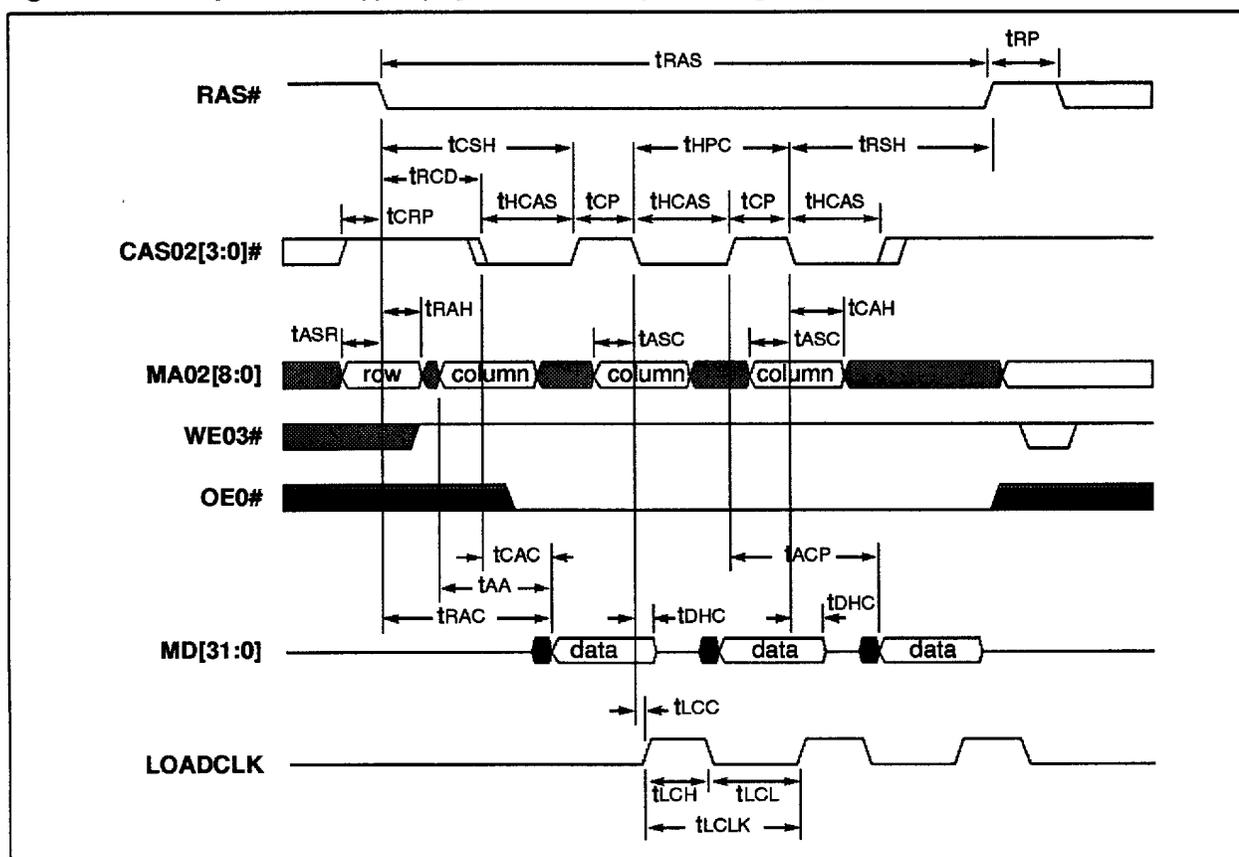
Table 7. 1, 2 and 4MByte DRAM hyper page mode read cycle timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tRC	Read cycle time	6TMCLK-5		ns	
tRAS	**RAS# pulse width**	3.5TMCLK-2		ns	
tRP	**RAS# precharge time**	2.5TMCLK-2		ns	
tCRP	**CASxx[3:0]# to RAS# precharge time**	3TMCLK-10		ns	
tCSH	**CASxx[3:0]# hold time**	3TMCLK-5		ns	
tRCD	**RAS# to CASxx[0:3]# delay time**	2TMCLK-5		ns	
tRSH	**RAS# hold time**	TMCLK-2		ns	
tCP	**CASxx[3:0]# precharge time (hyper page mode)**	0.5TMCLK-2		ns	
tHCAS	**CASxx[3:0]# pulse width (hyper page mode)**	0.5TMCLK-2		ns	
tASR	Row address setup time	TMCLK-5		ns	
tASC	Column address setup time	TMCLK-5		ns	
tRAH	Row address hold time	TMCLK-5		ns	
tCAH	Column address hold time	TMCLK-5		ns	
tCAC	Access time from **CASxx[3:0]#**	TMCLK		ns	
tAA	Access time from column address	TMCLK-2		ns	

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Symbol	Parameter	Min.	Max.	Unit	Notes
tRAC	Access time from **RAS#**	3TMCLK-2		ns	
tHPC	Hyper page mode read cycle time	TMCLK-2		ns	
tDHC	Data hold from **CASxx[3:0]#**	2		ns	
tACP	Access time from **CASxx[3:0]#** precharge	1.5TMCLK-5		ns	
tLCH	**LOADCLK** high pulse width	6		ns	
tLCL	**LOADCLK** low pulse width	6		ns	
tLCK	**LOADCLK** cycle time	18		ns	
tLCC	**LOADCLK** rising from **CASxx[3:0]#** active		0	ns	

NOTE

   1 TMCLK is the period of the internal memory clock.

Figure 23. 2MByte DRAM hyper page mode read cycle timing diagram into STG1764
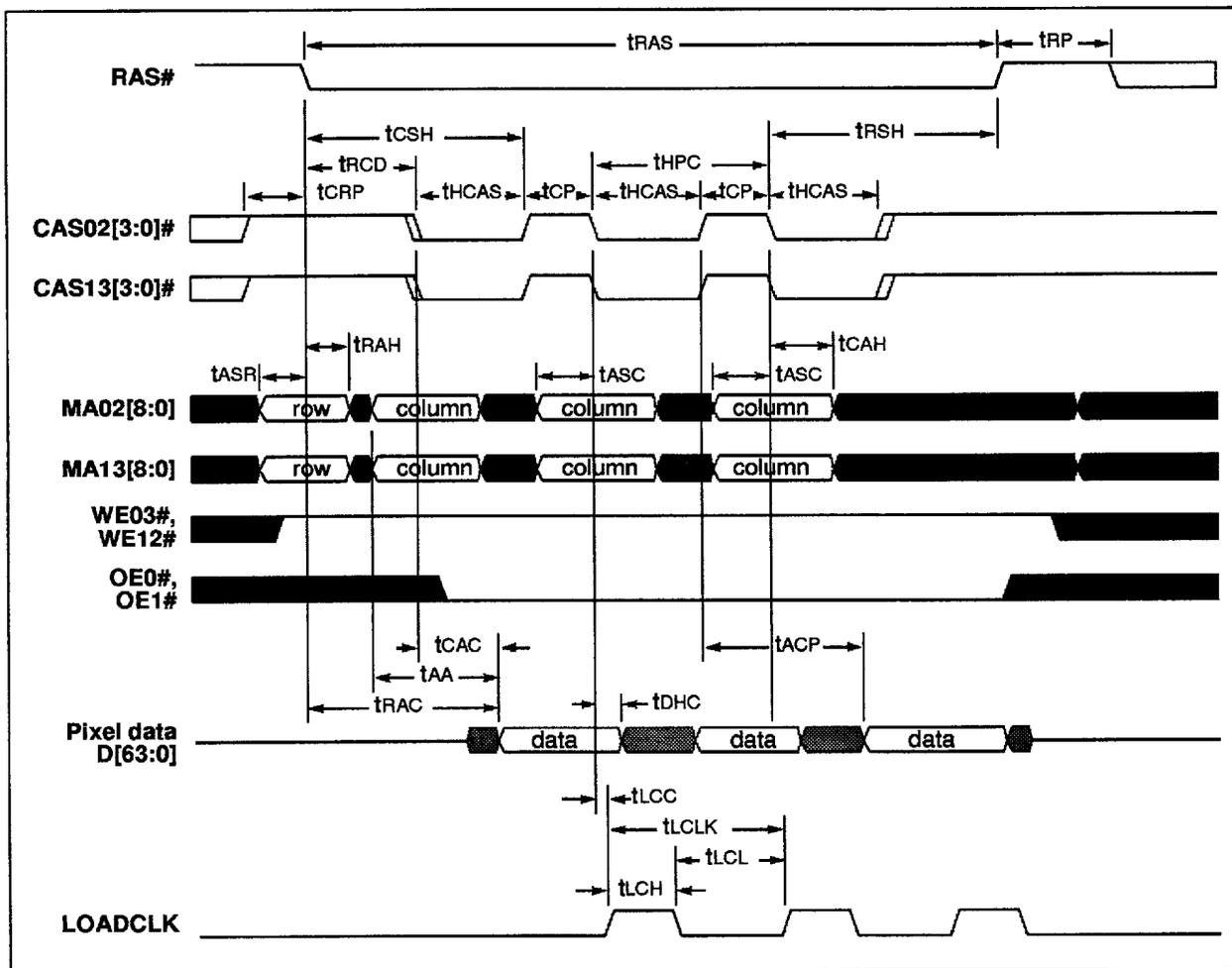
NOTE

   1 The timing parameters for the 2MByte DRAM hyper page mode read cycle are given in Table 7.

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Figure 24. 4MByte DRAM hyper page mode read cycle timing diagram into STG1764
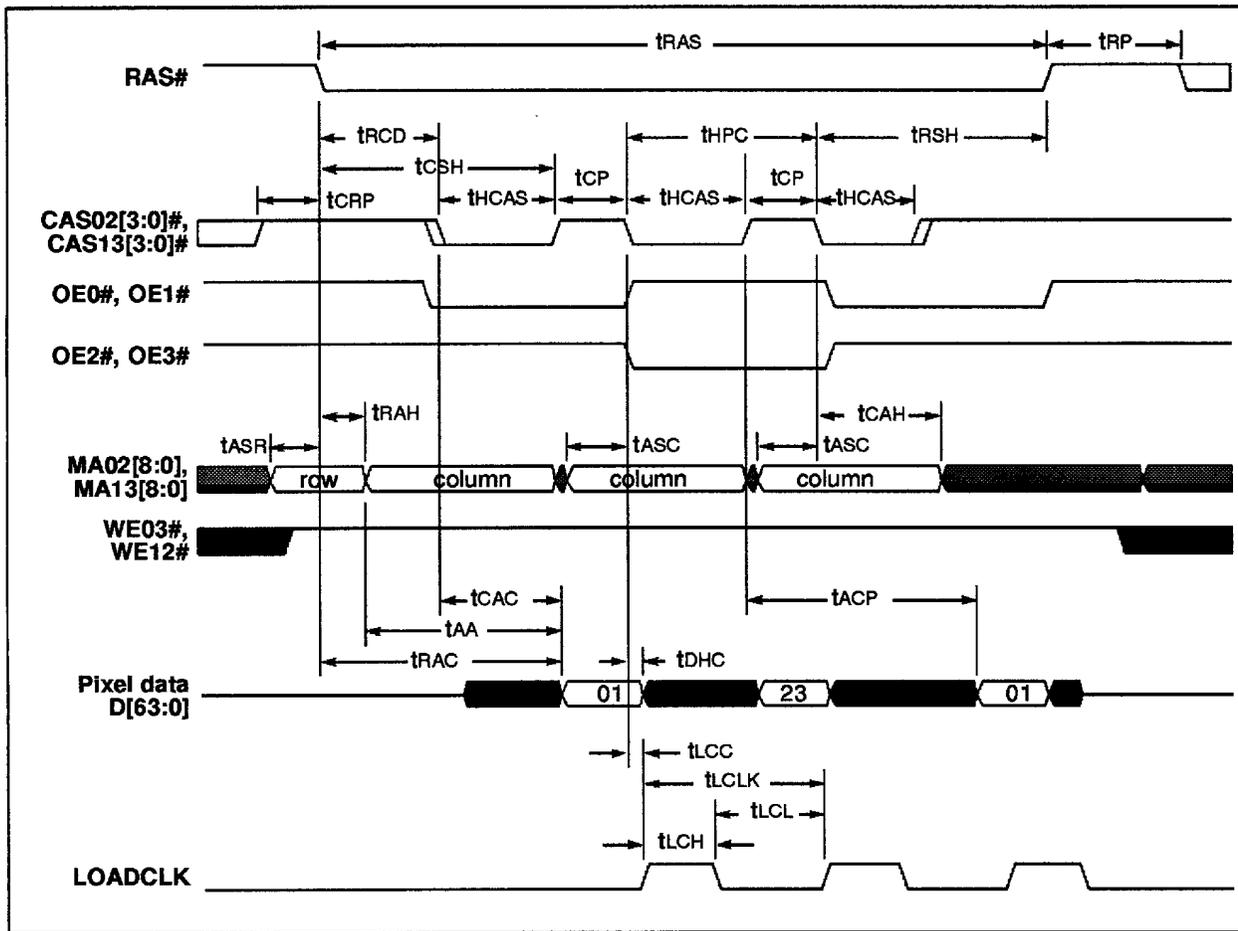
NOTE

1 The timing parameters for the 4MByte DRAM hyper page mode read cycle are given in Table 7.

Figure 25. 4MByte DRAM write cycle timing diagram (MA02[8:0] and MA13[8:0] interleaved)
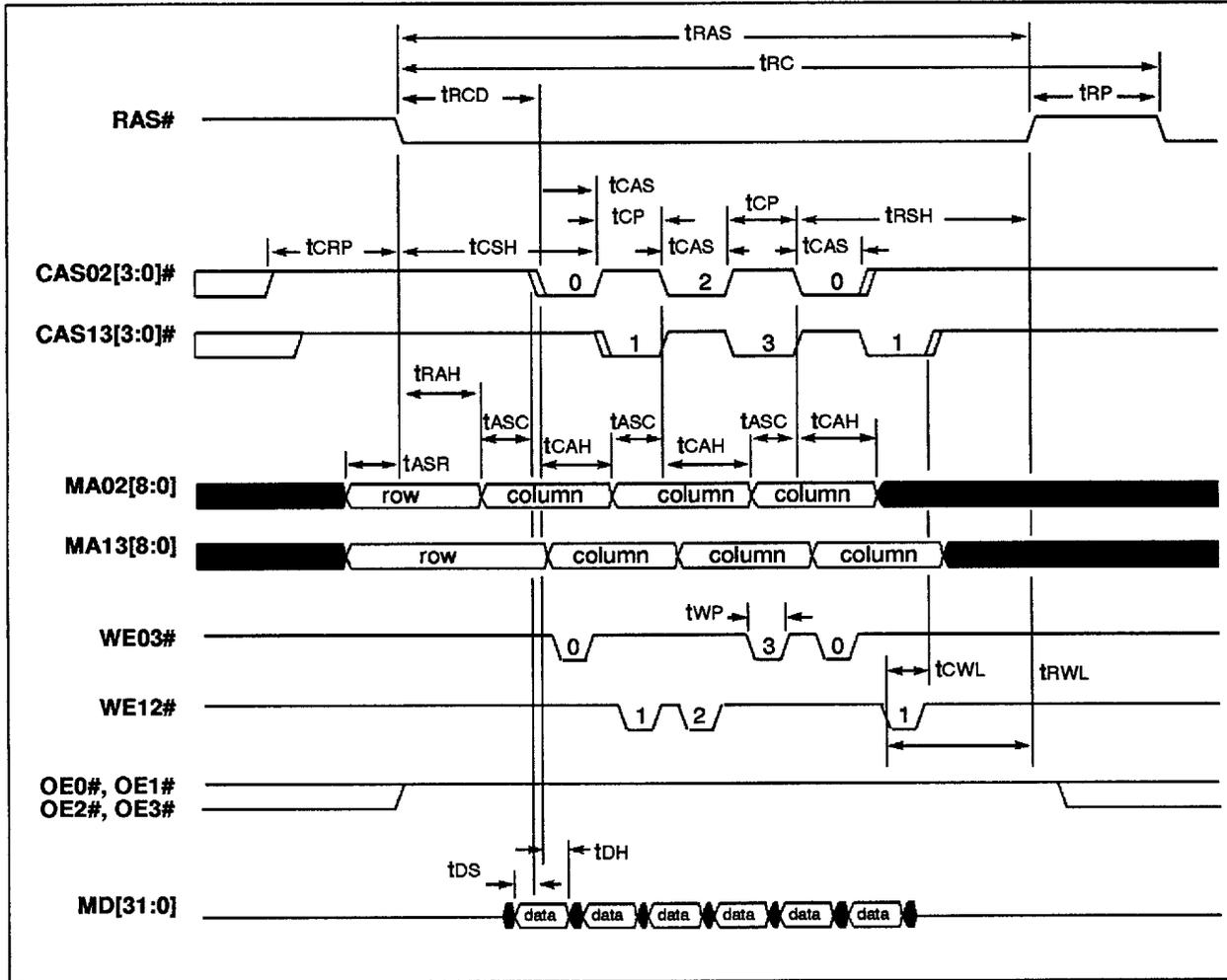
Table 8. 4MByte DRAM late write cycle timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tRC	**Write cycle time**	6TMCLK-5		ns	
tRAS	**RAS# pulse width**	3.5TMCLK-2		ns	
tRP	**RAS# precharge time**	2.5TMCLK-2		ns	
tCRP	**CASxx[3:0]# to RAS# precharge time**	3TMCLK-10		ns	
tCSH	**CASxx[3:0]# hold time**	3TMCLK-5		ns	
tRCD	**RAS# to CASxx[0:3]# delay time**	2TMCLK-5		ns	
tRSH	**RAS# hold time**	1.5TMCLK-2		ns	
tCP	**CASxx[3:0]# precharge time (page mode)**	TMCLK-5		ns	
tCAS	**CASxx[3:0]# pulse width (page mode)**	TMCLK-2		ns	
tASR	Row address setup time	TMCLK-5		ns	
tASC	Column address setup time	TMCLK-5		ns	
tRAH	Row address hold time	TMCLK-5		ns	

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Symbol	Parameter	Min.	Max.	Unit	Notes
tCAH	Column address hold time	TMCLK-5		ns	
tPC	Fast page mode cycle time	2TMCLK-2		ns	
tWP	Write command pulse width	0.5TMCLK		ns	
tCWL	Write command active to **CASxx[3:0]#** inactive	0.5TMCLK+2		ns	
tRWL	Write command active to **RAS#** inactive	0.5TMCLK+2			
tDS	Write data setup time	0.5TMCLK-2		ns	
tDH	Write data hold time	0.5TMCLK+2		ns	

NOTE
1 TMCLK is the period of the internal memory clock.

Figure 26. DRAM CAS# before RAS# refresh cycle timing diagram
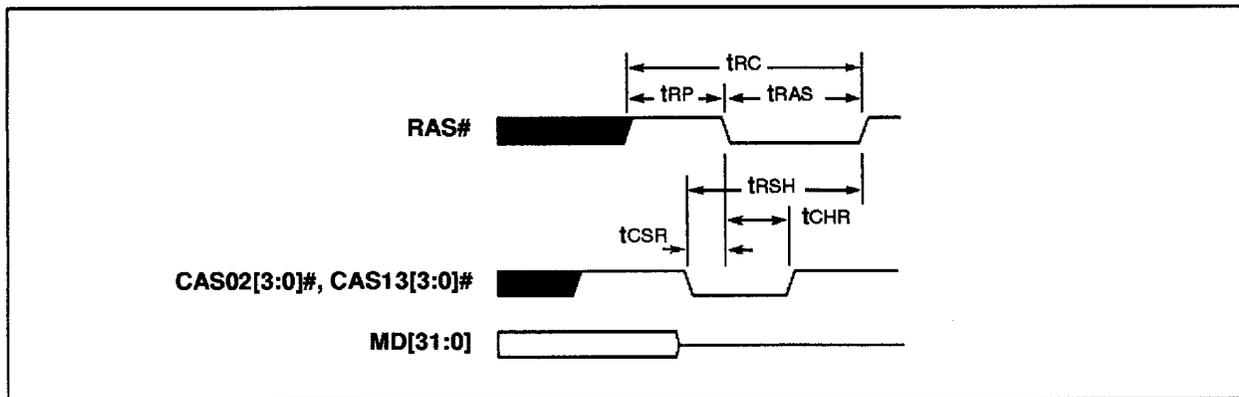
Table 9. DRAM CAS# before RAS# refresh cycle timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tRC	**CAS# before RAS# cycle time**	6TMCLK-5		ns	
tRAS	**RAS# pulse width**	3.5TMCLK-2		ns	
tRP	**RAS# precharge time**	2.5TMCLK-2		ns	
tRSH	**RAS# hold time**	4TMCLK-5		ns	
tCSR	**CASxx[3:0]# setup time**	TMCLK-5		ns	
tCHR	**CASxx[3:0]# hold time**	TMCLK-5		ns	

NOTE
1 TMCLK is the period of the internal memory clock.

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5.2   ROM INTERFACE

BIOS and initialization code for the STG2000 is accessed from a 32KByte ROM. The STG2000 memory bus interface signals **MDB[30:16]** and **MDB[7:0]** are used to address and read one of the 32KBytes of data respectively. The unique decode to the ROM device is provided by the **ROMCS#** chip select signal.

A R/W# function is also provided using **MD[31]** for implementations supporting Flash Memory. Note that either an EPROM or Flash ROM may be populated in the same DIP pinout; for more information see the RDK Design Guide [6].

Figure 27.   ROM and Flash ROM interfaces
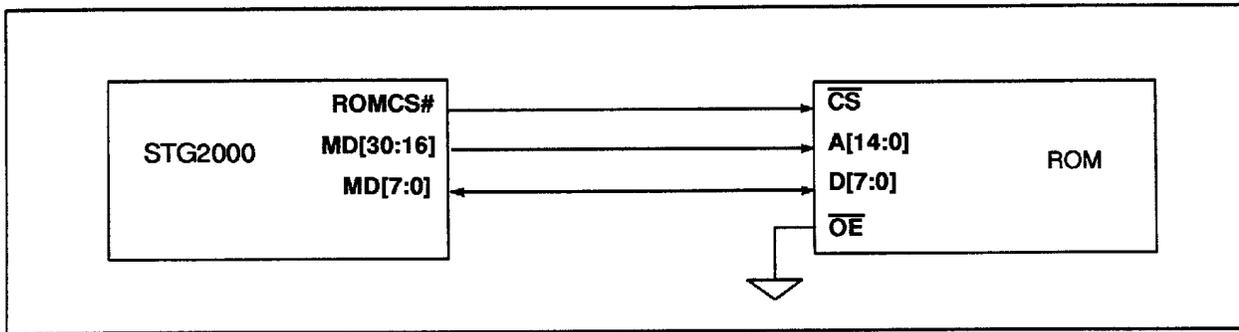
Figure 28.   FLASH ROM/EPROM interface

R1 and R3 are populated for EPROM
The 7400 and R2 are populated for FLASH ROM
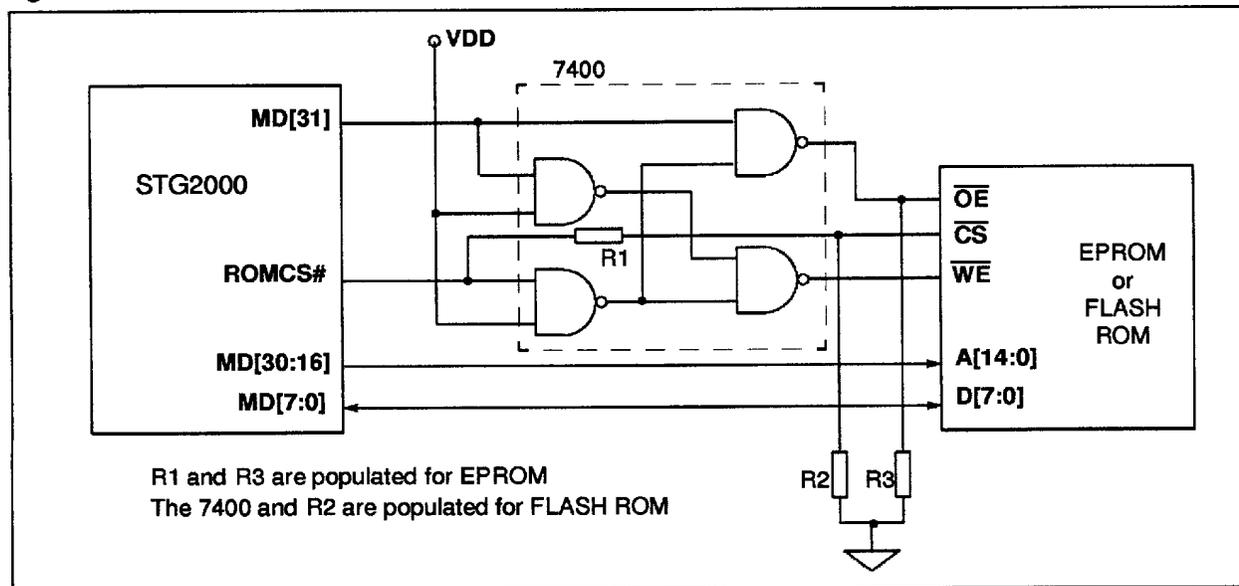
ROM Interface timing specification

Figure 29. ROM interface timing diagram
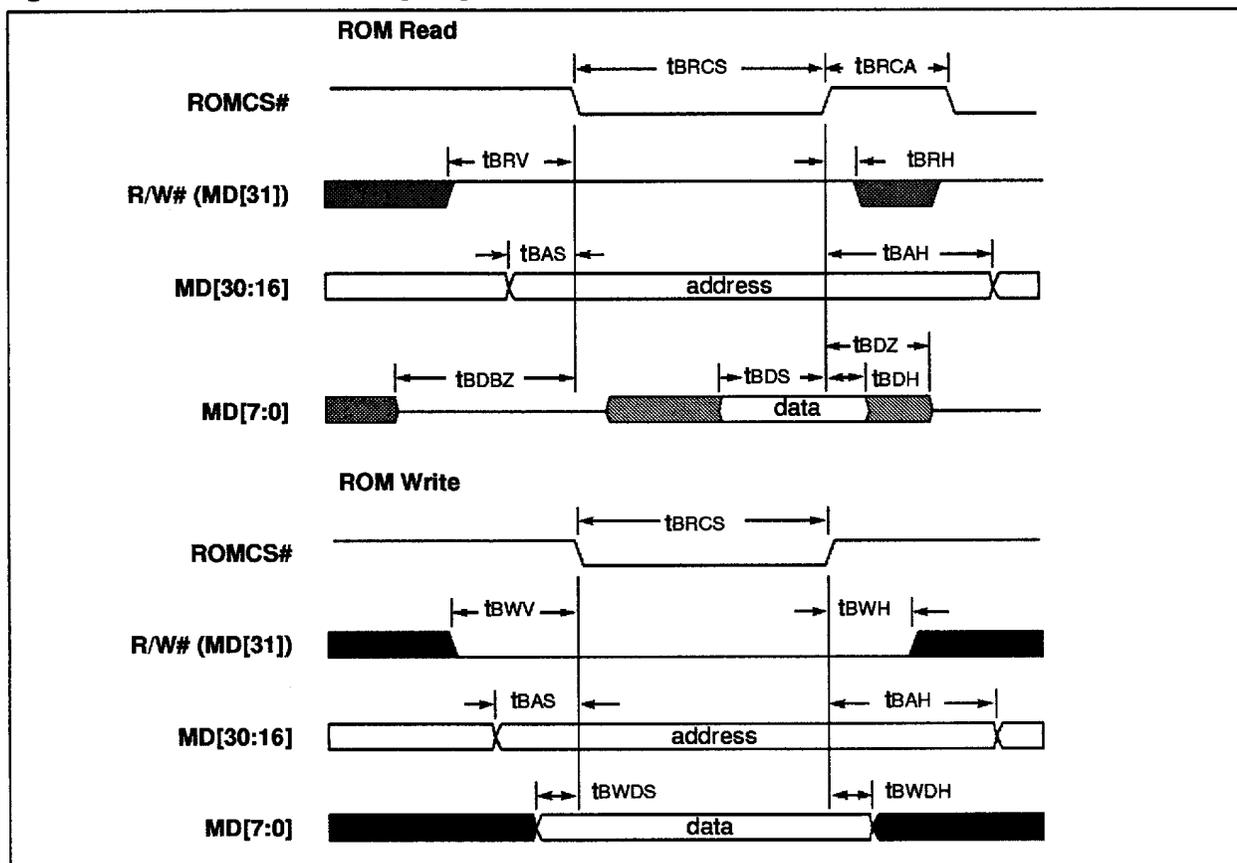
Table 10. ROM interface timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tBRCS	**ROMCS#** active pulse width	13T_{MCLK}-5		ns	
tBRCA	**ROMCS#** precharge time	T_{MCLK}-5		ns	
tBRV	Read valid to **ROMCS#** active	T_{MCLK}-5		ns	
tBRH	Read hold from **ROMCS#** inactive	T_{MCLK}-5		ns	
tBAS	Address setup to **ROMCS#** active	T_{MCLK}-5		ns	
tBAH	Address hold from **ROMCS#** inactive	T_{MCLK}-5		ns	
tBDBZ	Data bus high-z to **ROMCS#** active	T_{MCLK}-5		ns	
tBDS	Data setup to **ROMCS#** inactive	10		ns	
tBDH	Data hold from **ROMCS#** inactive	0		ns	
tBDZ	Data high-z from **ROMCS#** inactive		T_{MCLK}-5	ns	
tBWV	R/W# valid setup to **ROMCS#** active	T_{MCLK}-5		ns	
tBWH	R/W# hold from **ROMCS#** inactive	T_{MCLK}-5		ns	
tBWDH	Write data hold from **ROMCS#** inactive	T_{MCLK}-5		ns	
tBWDS	ROM write data setup to **ROMCS#** active	T_{MCLK}-5		ns	

NOTE

1 T_{MCLK} is the period of the internal memory clock.

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5.3 EEPROM INTERFACE

The STG2000 supports an external 1Kbit Electrically Erasable Programmable Memory (EEPROM) containing the initialization information required by the chip to power-up correctly. This includes the power-on settings required for correct system resource mapping and legacy mode configurations. Environment and other system related variables such as monitor timing adjustments are also contained in the EEPROM.

The STG2000 interface to the EEPROM is implemented via an industry standard Microwire bus. This 3-signal protocol uses a chip enable (**EECS**) to select the EEPROM. Data transfer is accomplished via a bidirectional serial data line (**EESD**) and clock (**EESCLK**).

The EEPROM is structured in a 128×8-bit word organization, such as the ST93C46A. This common format is available in a small outline (SO8) package which can easily be located in close proximity to the STG2000. The serial data transfer rate is low (<1MHz), hence signal routing is not critical. Details of the standard data format structure and software interface protocol for accessing the 1Kbit data are given in the SGS-THOMSON Datasheet for the ST93C46A [7]. Pre-programmed EEPROM devices for the STG2000 Multimedia Accelerator chipset are available from SGS-THOMSON with the part number NVCAATR.

The STG2000 automatically unlocks the EEPROM prior to sending a WRITE command. Following the write command it waits for the data line to be driven high, indicating completion of the write by the EEPROM. It then ends the user write request by sending an EWDS sequence to lock the EEPROM.

Figure 30. EEPROM power-on read sequence timing diagram
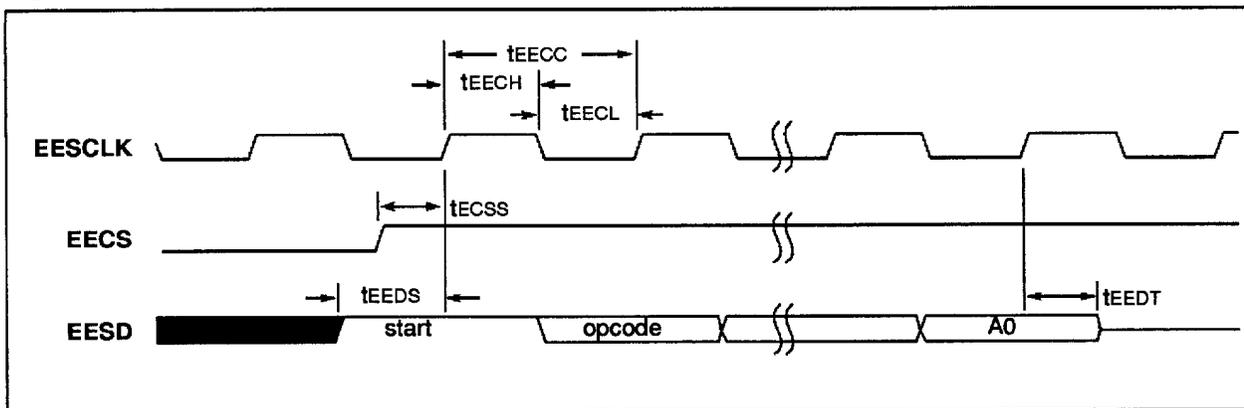
Table 11. EEPROM power-on read sequence timing parameters

Symbol	Parameter	Min.	Max.	Units	Notes
tEECC	**EESCLK** period	50		TMCLK	
tEECH	**EESCLK** high time	24		TMCLK	
tEECL	**EESCLK** low time	24		TMCLK	
tECSS	**EECS** high to **EESCLK** high	23		TMCLK	
tEEDS	**EESD** valid to **EESCLK** high	23		TMCLK	
tEEDT	**EESCLK** high to **EESD** inactive	23		TMCLK	

NOTE

1   TMCLK is the period of the internal memory clock.

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5.4 PALETTE-DAC INTERFACE

The STG1764 or STG1732 Palette-DAC interface comprises an 8-bit multiplexed address/data bus connecting to **MDB[15:8]** of the STG2000 memory bus. The unique decode to the Palette-DAC is provided by the **DACCS#** chip select signal. Each access is split into two phases; address and data. In the address phase the falling edge of **DACCS#** latches the 4-bit address into the Palette-DAC and latches **MDB[15]** (Palette-DAC signal **AD[7]**) to identify whether the current access is a read or write.

Figure 31. DAC interface
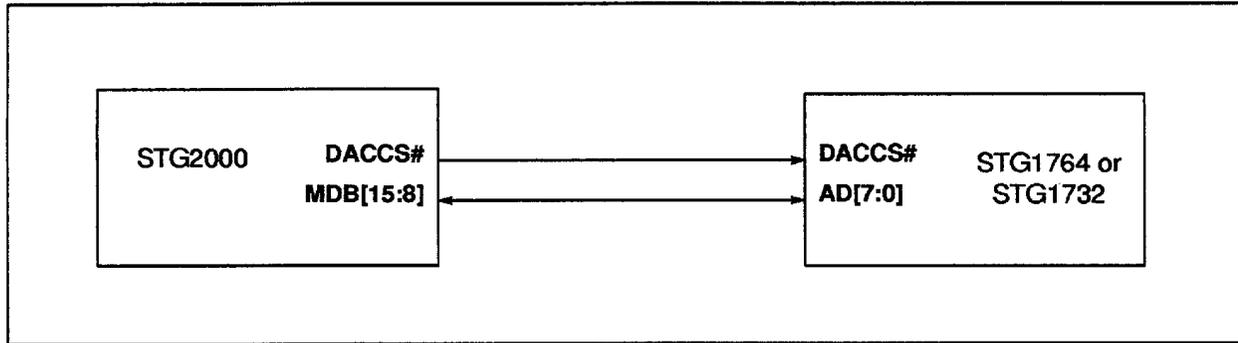
Palette-DAC interface timing specification

Figure 32. BLANK# timing diagram
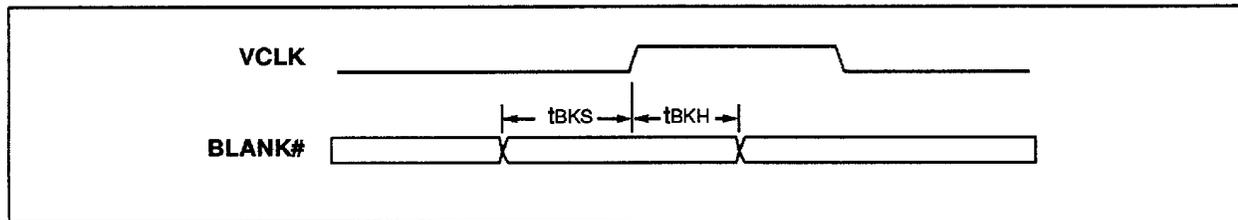
Table 12. BLANK# timing parameters

Symbol	Parameter	Min.	Max.	Units	Notes
tBKS	BLANK# set-up time	4.0		ns	
tBKH	BLANK# hold time	4.0		ns	

Figure 33. Palette-DAC interface read/write cycle timing diagram
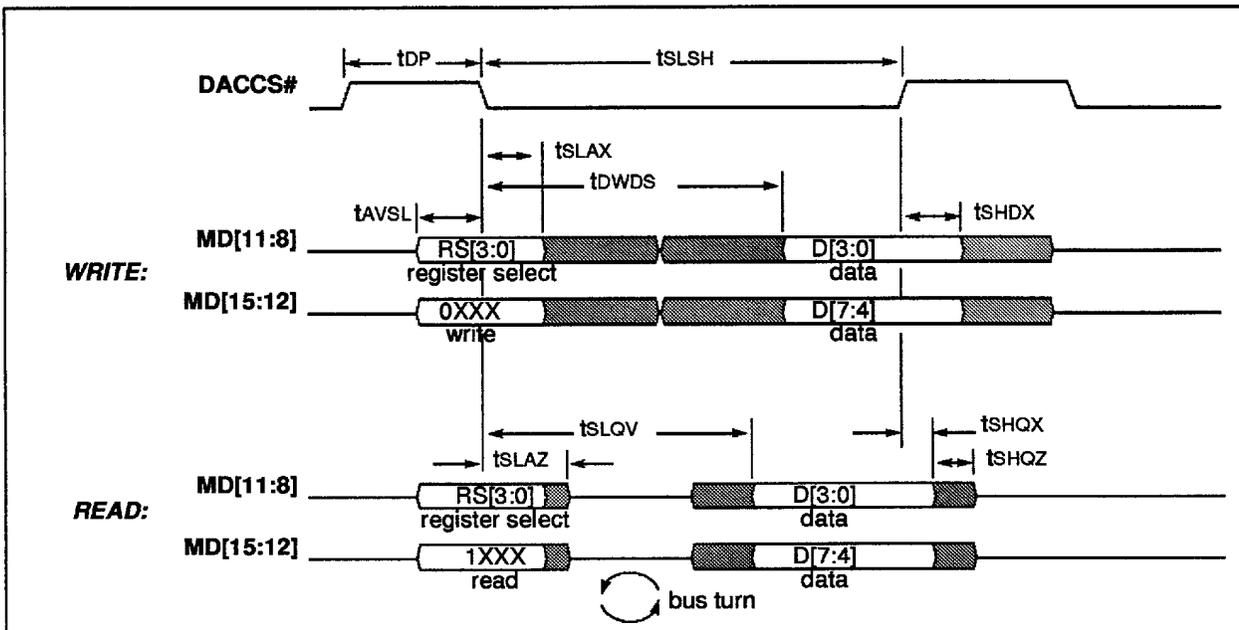
Table 13. Palette-DAC interface read/write cycle timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tDP	DAC interface precharge time	3TMCLK-5		ns	DAC write cycle
tSLSH	DACCS# pulse time	3TMCLK-5		ns	DAC read cycle
tAVSL	Address setup time	1.5TMCLK-5		ns	Game Port read/write cycle
tSLAX	Address hold time	0		ns	All accesses
tDWDS	Write data setup time		0.5TMCLK+10	ns	Write cycle
tSHDX	Write data hold time	0.5TMCLK-10		ns	Write cycle
tSLAZ	Address high-z time		10	ns	Read cycle
tSLQV	Read access time from **DACCS#** active	2TMCLK-10		ns	Read cycle
tSHQX	Read data hold time from **DACCS#** inactive	0		ns	Read cycle
tSHQZ	Output turn-off delay		TMCLK-5	ns	Read cycle

NOTE

1 TMCLK is the period of the internal memory clock.

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5.5 ALTCS# INTERFACE

The STG2000 can access 32KBytes of read/write memory. The STG2000 memory bus interface signals **MDB[30:16]** and **MDB[7:0]** are used to address and access one of the 32KBytes of data respectively. **MDB[31]** provides an indication of a read or write cycle. The unique decode to this 32KByte device is provided by the **ALTCS#** chip select signal.

Figure 34. ROM interfaces
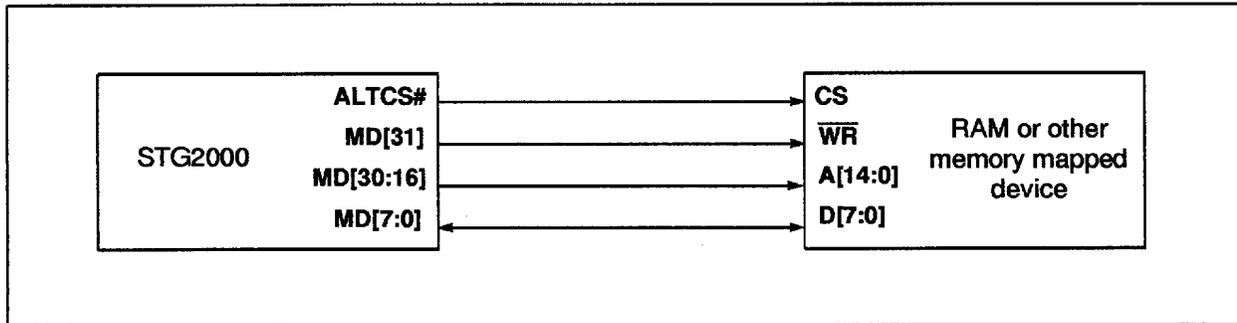
ALTCS# interface timing specification

Figure 35.   ALTCS# interface timing diagram
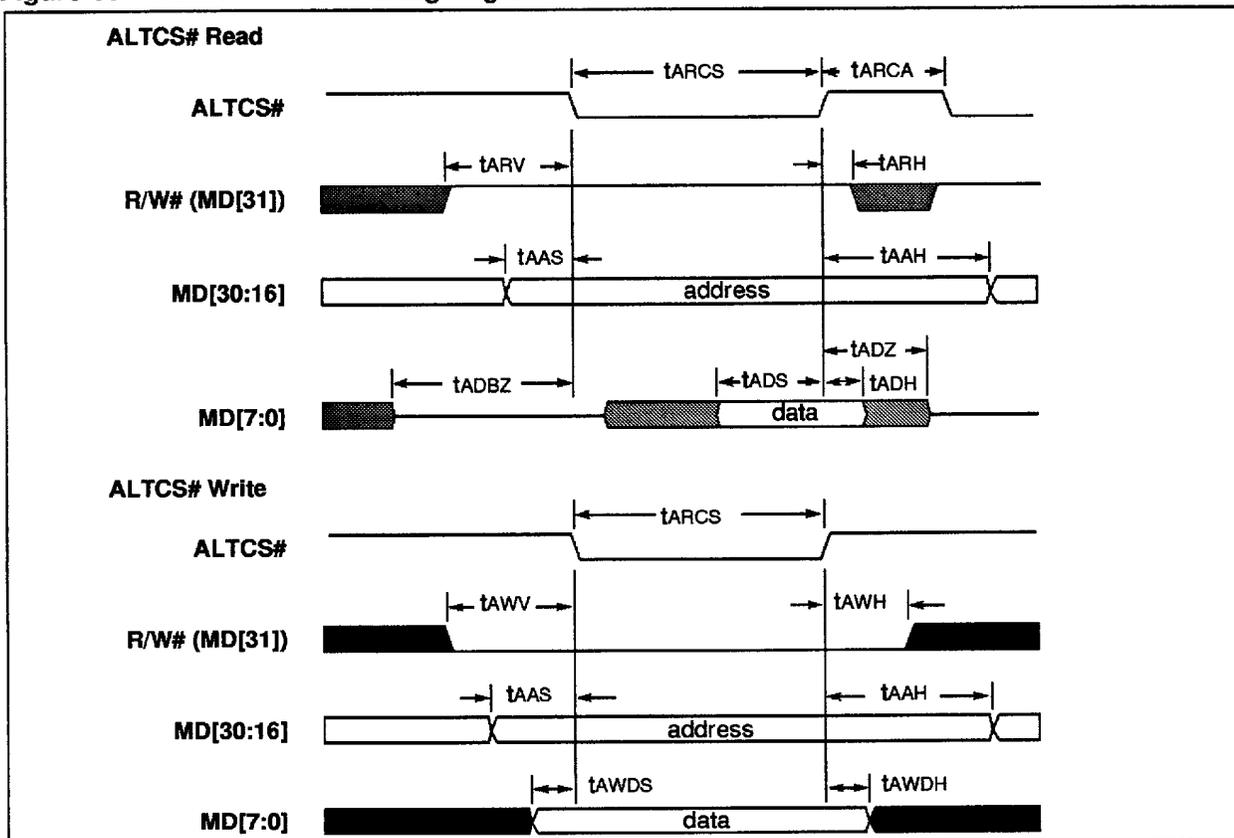
Table 14.   ALTCS# interface timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tARCS	**ALTCS#** pulse width	13TMCLK-5		ns	
tARCA	**ALTCS#** precharge time	TMCLK-5		ns	
tARV	Read valid to **ALTCS#** active	TMCLK-5		ns	
tARH	Read hold from **ALTCS#** inactive	TMCLK-5		ns	
tAAS	Address setup to **ALTCS#** active	TMCLK-5		ns	
tAAH	Address hold from **ALTCS#** inactive	TMCLK-5		ns	
tADBZ	Data bus high-z to **ALTCS#** active	TMCLK-5		ns	
tADS	Data setup to **ALTCS#** inactive	10		ns	
tADH	Data hold from **ALTCS#** inactive	0		ns	
tADZ	Data high-z from **ALTCS#** inactive		TMCLK-5	ns	
tAWV	R/W# valid setup to **ALTCS#** active	TMCLK-5		ns	
tAWH	R/W# hold from **ALTCS#** inactive	TMCLK-5		ns	
tAWDH	Write data hold from **ALTCS#** inactive	TMCLK-5		ns	
tAWDS	Write data setup **ALTCS#** active	TMCLK-5		ns	

NOTE

1   TMCLK is the period of the internal memory clock.

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6 AUDIO CODEC INTERFACE

The audio codec interface supports the Analog Devices AD1848 or equivalent. This is a mixed signal device that provides 16-bit stereo, multiple source audio capture and playback capability. The STG2000 audio codec interface, shown in Figure 36, does not use the interrupt or DMA features of the codec. The interface comprises an 8-bit data bus, two address bits and independent read and write strobes. The codec may be placed in a power-saving mode by asserting **AUPD#**.

Figure 36. Audio codec interface
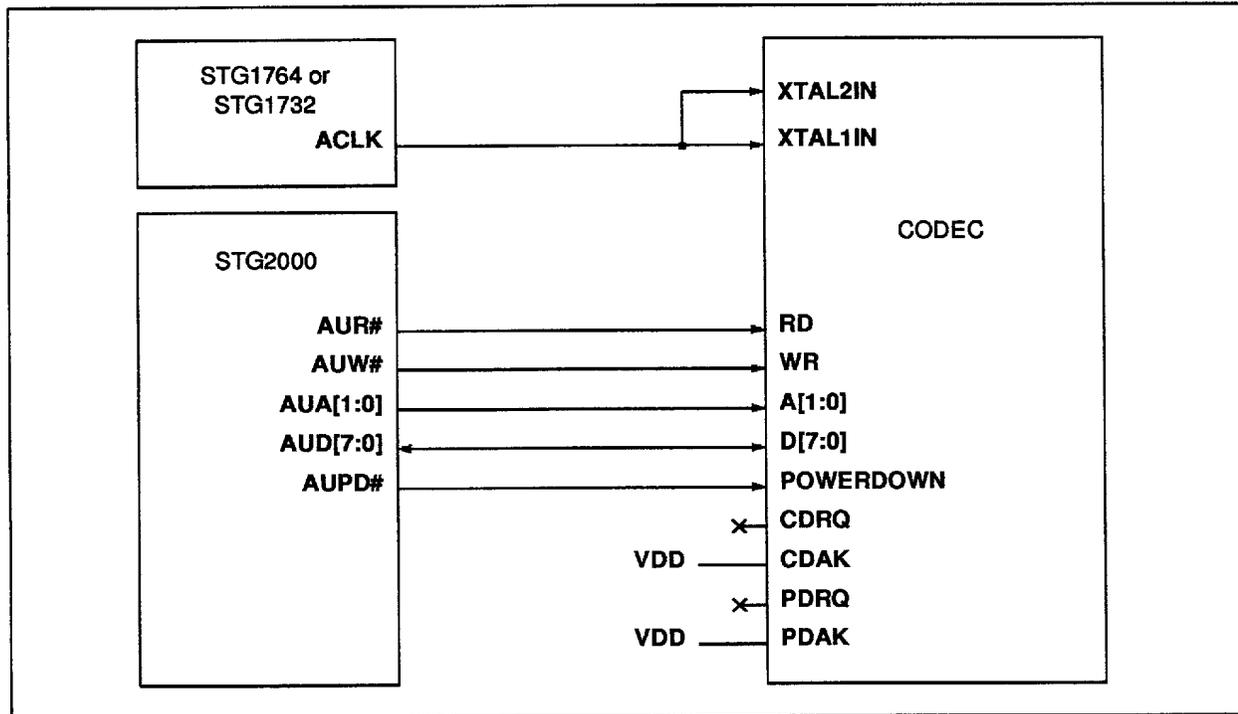
6.1 AUDIO CODEC INTERFACE TIMING SPECIFICATION

Figure 37. Audio codec interface write cycle timing diagram
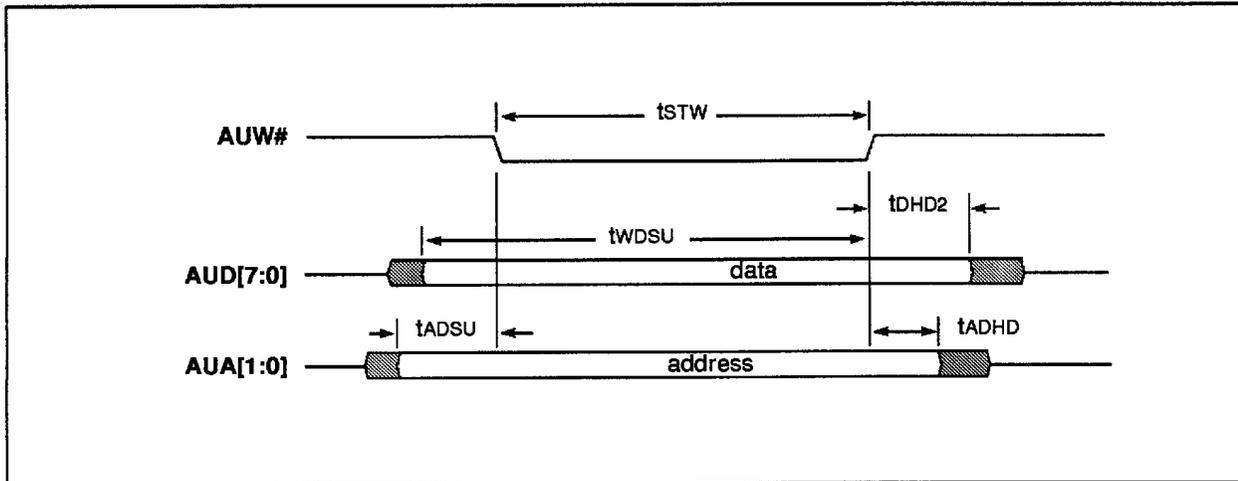
Table 15. Audio codec interface write cycle timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tSTW	**AUW#** strobe width	13T$_{MCLK}$-10		ns	1
tWDSU	**AUD[7:0]** setup to **AUW#** rising	17T$_{MCLK}$-20		ns	1
tADSU	**AUA[1:0]** setup to **AUW#** falling	4T$_{MCLK}$-20		ns	1
tADHD	**AUA[1:0]** hold from **AUW#** rising	3T$_{MCLK}$-20	t.b.d.	ns	1
tDHD2	**AUD[7:0]** hold from **AUW#** rising	7T$_{MCLK}$-20	t.b.d.	ns	1

NOTE

1   T$_{MCLK}$ = period of the internal memory clock

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Figure 38. Audio codec interface read cycle timing diagram
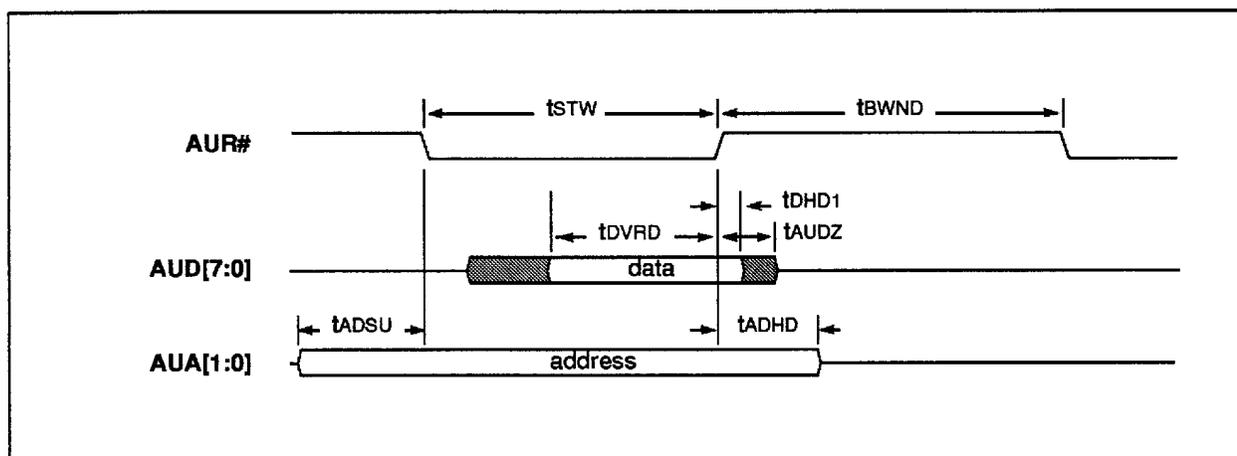
Table 16. Audio codec interface read cycle timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tSTW	AUR# strobe width	13TMCLK-10		ns	1
tBWND	AUR# rising to AUR# falling	15TMCLK-10		ns	1
tDVRD	AUD[7:0] valid to AUR# rising	20	t.b.d.	ns	
tADSU	AUA[1:0] setup to AUR# falling	4TMCLK-20		ns	1
tADHD	AUA[1:0] hold from AUR# rising	3TMCLK-20		ns	1
tDHD1	AUD[7:0] hold from AUR# rising	0		ns	
tAUDZ	AUR# rising to AUD[7:0] high-z		14TMCLK-20	ns	1

NOTE
1 TMCLK = period of the internal memory clock

7 POWER-ON RESET CONFIGURATION

The STG2000 latches its configuration on the trailing edge of **RST#/RESET#** and holds its system bus interface in a high impedance state until this time. Normally the configuration is read from the BIOS which is located on the memory data bus. The memory interface drives **RAS#** and **OE#** inactive during this period.

In motherboard designs the BIOS will typically be merged with that of the system, hence the configuration information must be transferred in another manner. To accomplish this, pull-up or pull-down resistors are connected to the **MD[7:0]** bus as appropriate. In the STG2000 only bits [4:0] are significant. Since there are no internal pull-up or pull-down resistors and the data bus should be floating during reset, a resistor value of 47KΩ should be sufficient.

Figure 39. Planar implementation of STG2000 on the PCI bus
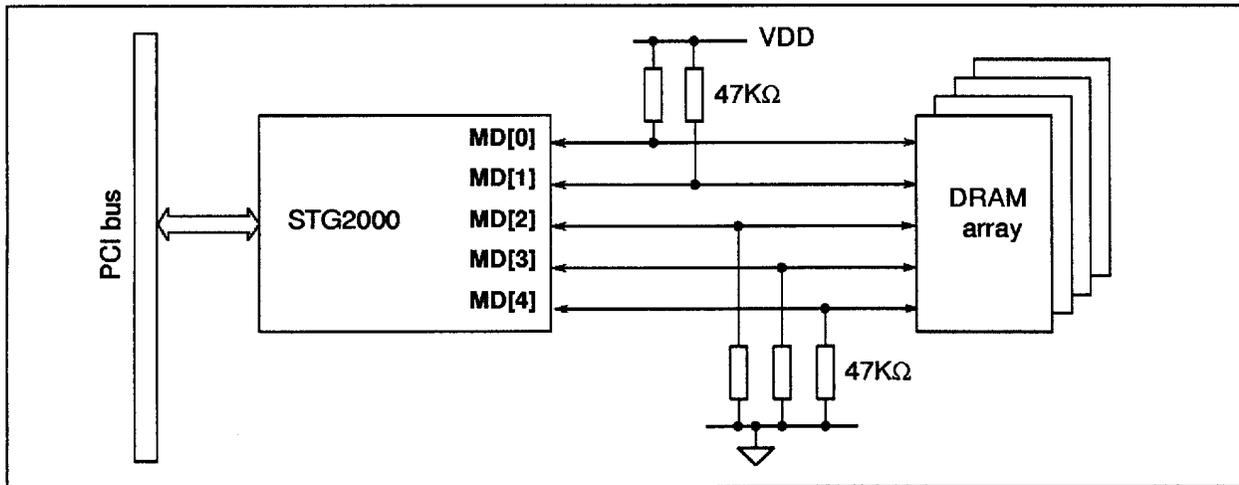
Power-on reset MD[7:0] bit assignments

7	6	5	4	3	2	1	0
Reserved			Bus Type	Board Type		Frame Buffer Type	

[7:5]   Reserved

[4]   Bus Type
   0 = PCI bus
   1 = VL-bus

[3:2]   Board Type
   00 = Motherboard
   01 = Adapter #1   Note: Normally add-on cards will use the Adapter #1 configuration.
   10 = Adapter #2
   11 = Adapter #3

[1:0]   Frame Buffer Type
   00 = VRAM
   01 = Illegal
   10 = Illegal
   11 = DRAM

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8   ELECTRICAL SPECIFICATIONS

8.1   ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Min.	Max.	Units	Notes
VDD	DC supply voltage		3.6	V	
	Voltage on input and output pins	GND-1.0	7.5	V	
TS	Storage temperature (ambient)	-55	125	°C	
TA	Temperature under bias	0	85	°C	

NOTE

1   Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8.2   DC SPECIFICATIONS

Table 17.   DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
VDD	Positive supply voltage	3.0	3.3	3.6	V	
IIN	Input current (signal pins)			±10	µA	1, 2
PDmax	Power dissipation			1.7	W	

NOTES

1   Includes high impedance output leakage for all bi-directional buffers with tri-state outputs
2   VDD = max, GND ≤ VIN ≤ VDD

Table 18.   Parameters applying to VL-bus interface pins

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
CIN	Input capacitance		10	12	pF	
COUT	Output load capacitance		10	175	pF	
VIH	Input logic 1 voltage	2.0		5.5	V	
VIL	Input logic 0 voltage	-0.5		0.8	V	
VOH	Output logic 1 level	2.4			V	
VOL	Output logic 0 level			0.5	V	
IOL	Output load current, logic 0 level			8	mA	

Table 19.   Parameters applying to PCI interface pins

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
CIN	Input capacitance	5		10	pF	
COUT	Output load capacitance	5		50	pF	
Parameters for 5V signaling environment only:						
VIH	Input logic 1 voltage	2.0		5.75	V	
VIL	Input logic 0 voltage	-0.5		0.8	V	
VOH	Output logic 1 level	2.4			V	
VOL	Output logic 0 level			0.55	V	
IOH	Output load current, logic 1 level			-2	mA	
IOL	Output load current, logic 0 level			3 or 6	mA	1

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
Parameters for 3.3V signaling environment only:						
VIH	Input logic 1 voltage	0.475VDD		VDD+0.5	V	
VIL	Input logic 0 voltage	-0.5		0.325VDD	V	
VOH	Output logic 1 level	0.9VDD			V	
VOL	Output logic 0 level			0.1VDD	V	
IOH	Output load current, logic 1 level			-0.5	mA	
IOL	Output load current, logic 0 level			1.5	mA	

NOTE

1 3mA for all signals except **FRAME#**, **TRDY#**, **IRDY#**, **DEVSEL#**, **STOP#** and **SERR#** which have IOL of 6mA.

Table 20. Parameters applying to all signal pins except VL-bus and PCI interfaces

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
CIN	Input capacitance		10	12	pF	
COUT	Output load capacitance		10	50	pF	
VIH	Input logic 1 voltage	2.0		5.75	V	
VIL	Input logic 0 voltage	-0.5		0.8	V	
VOH	Output logic 1 level	2.4			V	
VOL	Output logic 0 level			0.4	V	
IOH	Output load current, logic 1 level			-1	mA	
IOL	Output load current, logic 0 level			1	mA	

8.3 OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
TC	Ambient operating temperature	0	N/A	70	°C	

9 PACKAGE DIMENSION SPECIFICATION

9.1 208 PIN PLASTIC QUAD FLAT PACK

Table 21. STG2000 208 pin Plastic Quad Flat Pack dimensions

REF (see Figure 40).	CONTROL DIMENSIONS - mm			ALTERNATIVE DIMENSIONS - inches			NOTES
	MIN	NOM	MAX	MIN	NOM	MAX	
A			4.07			0.160	
A1	0.25			0.010			
A2	3.24		3.74	0.128		0.147	
b	0.16		0.30	0.006		0.012	
C	0.12		0.20	0.005		0.008	
D	27.80		28.20	1.095		1.110	
E	27.80		28.20	1.095		1.110	
e		0.50			0.020		BSC
HD	30.35		30.85	1.195		1.215	
HE	30.35		30.85	1.195		1.215	

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REF (see Figure 40).	CONTROL DIMENSIONS - mm			ALTERNATIVE DIMENSIONS - inches			NOTES
	MIN	NOM	MAX	MIN	NOM	MAX	
L	0.40		0.60	0.016		0.024	
L1		1.30			0.051		
ZD		1.25			0.049		
ZE		1.25			0.049		
θ	0		8	0		8	Degrees

Figure 40. STG2000 208 pin Plastic Quad Flat Pack dimension reference
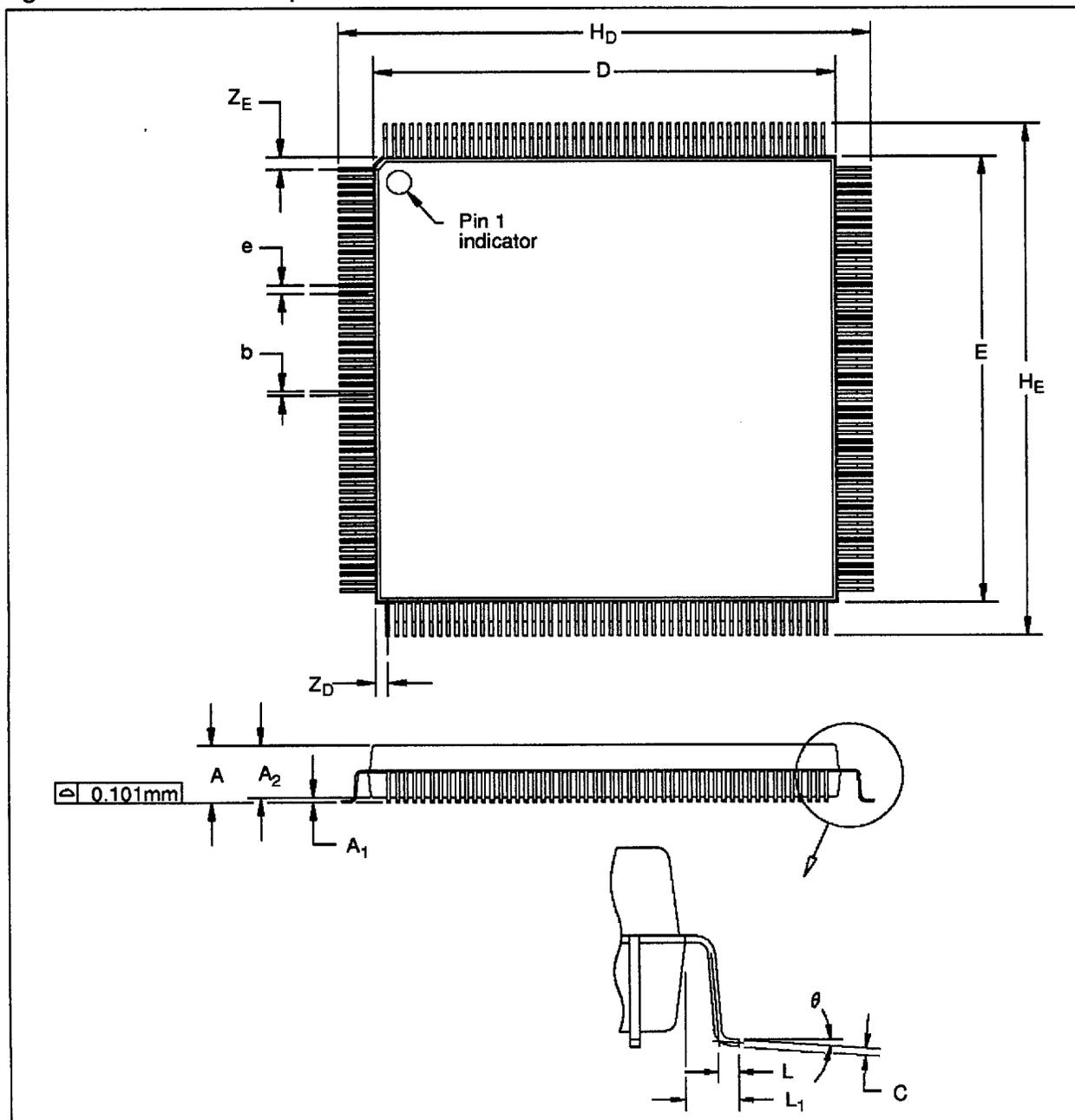
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10 REFERENCES

1 STG2000 *Multimedia Accelerator Datasheet*, SGS-THOMSON Microelectronics, June 1995, SGS-THOMSON Document Number: 42 1653 02 (this document)

2 STG1732/64 *Palette-DAC Datasheet*, SGS-THOMSON Microelectronics, June 1995, SGS-THOMSON Document Number: 42 1648 02

3 *NVidia Technical Reference*, NVidia Corporation, June 1995, NVidia Document Number: DOC-03-STN

4 *NV Architecture Overview*, NVidia Corporation, June 1995, NVidia Document Number: DOC-01-SUN

5 *Programming NV*, NVidia Corporation, June 1995, NVidia Document Number: DOC-03-SPN

6 *STG2000 Reference Design Kit (RDK), Design Guide*, SGS-THOMSON Microelectronics, June 1995, SGS-THOMSON Document Number: 72 OEK 290 00

7 ST93C46A, ST93C46C, ST93C46T *Serial access CMOS 1K bit EEPROM Datasheet*, SGS-THOMSON Microelectronics, August 1994

11 ORDERING INFORMATION

Device	Package	Part number
STG2000	208 pin PQFP	STG2000X

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APPENDICES

Descriptions of register contents include an indication if register fields are readable (R) or writable (W) and the initial power-on or reset value of the field (I). '-' indicates not readable / writable, X indicates an indeterminate value, hence I=X indicates register or field not reset.

A PCI CONFIGURATION REGISTERS

This section describes the 256 byte PCI configuration spaces as implemented by the STG2000. Two PCI functions, NV and VGA, are defined by the STG2000 which decodes and acknowledges the first 512 bytes of the configuration address space. The STG2000 does not respond (does not assert **DEVSEL#**) for functions 2 - 7.

A.1 REGISTER DESCRIPTIONS FOR FUNCTION 0 (VGA)

PCI Configuration Register 0x00
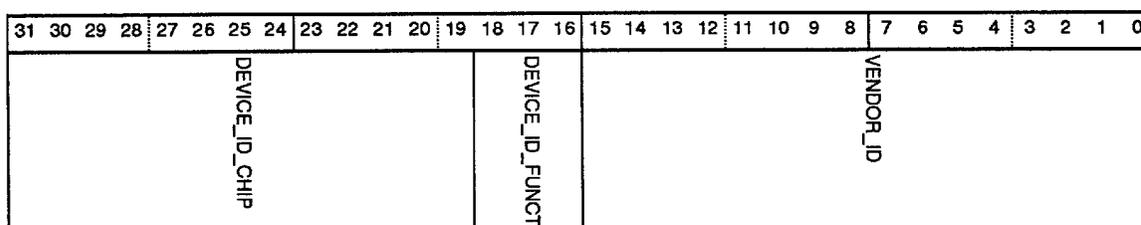
31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
	DEVICE_ID_CHIP		DEVICE_ID_FUNCT		VENDOR_ID		

Bits	Function	R W I
31:19	The DEVICE_ID_CHIP bits contain the chip number allocated by the manufacturer to identify the particular device. 1=STG2000	R - 1
18:16	The DEVICE_ID_FUNC bits contain the function number from the Configuration Address bits [10:8]. 0=VGA function	R - 1
15:0	VENDOR_ID bits allocated by the PCI Special Interest Group to uniquely identify the manufacturer of the device. 0x104A=SGS-THOMSON Microelectronics	R - X

PCI Configuration Register 0x04

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3	2	1	0
Reserved	DEVSEL_TIMING	Reserved		Reserved				PALETTE_SNOOP		Reserved		MEMORY_SPACE	IO_SPACE

Device Status Field (bits [31:16])

Bits	Function	R W I
31:27	Reserved	R - 0
26:25	The DEVSEL_TIMING bits indicate the timing of **DEVSEL#**. These bits indicate the slowest time that the STG2000 asserts **DEVSEL#** for any bus command except Configuration Read and Configuration Write. The STG2000 responds with medium **DEVSEL#** for the VGA device. 01=medium	R - 1
24:16	Reserved	R - 0

Device Control Command Field (bits[15:0])

Bits	Function	R W I
15:6	Reserved	R - 0
5	PALETTE_SNOOP indicates that VGA compatible devices should snoop their palette registers. 0=Palette accesses treated like all other accesses 1=Enables special palette snooping behavior	R W 0
4:2	Reserved	R - 0
1	MEMORY_SPACE indicates that the STG2000 will respond to memory space accesses. 0=Device response disabled 1=Enables response to Memory space accesses.	R W 0
0	IO_SPACE indicates that the device will respond to I/O space accesses. For the VGA function this bit enables I/O space accesses.	R W 0

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PCI Configuration Register 0x08

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
		CLASS_CODE					REVISION_ID

Bits	Function	R W I
31:8	The CLASS_CODE bits identify the generic function of the device and (in some cases) a specific register-level programming interface. The register is broken into three byte-size fields. The upper byte (at offset 0x0B) is a base class code which broadly classifies the type of function the device performs. The middle-byte (at offset 0x0A) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 0x09) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. The VGA function responds as a VGA compatible controller. 0x030000=VGA compatible controller	R - X
7:0	The REVISION_ID bits specify a device specific revision identifier. The value is chosen by the vendor. This field should be viewed as a vendor defined extension to the DEVICE_ID. 0x00=Rev A, 0x01=Rev B, 0x02=Rev C	R - X

PCI Configuration Register 0x0C

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
	Reserved		HEADER_TYPE			Reserved	

Bits	Function	R W I
31:24	Reserved	R - 0
23:16	HEADER_TYPE identifies the device as single or multi-function. STG2000 responds as a multi-function device. 0x80=Multiple function device	R - 0x80
16:00	Reserved	R - 0

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PCI Configuration Register 0x10   Base Memory Address Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															0x00000000																

Bits	Function	R W I
31:0	These bits are hardwired (read-only) to 0.	R - 0

PCI Configuration Registers 0x14 - 0x24   Base Address Registers

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															0x00000000																

Bits	Function	R W I
31:0	These bits are hardwired (read-only) to 0.	R - 0

PCI Configuration Register 0x30   Expansion ROM Base Address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROM_BASE_ADDRESS										ROM_BASE_RESERVED											Reserved										ROM_DECODE

Bits	Function	R W I
31:22	The ROM_BASE_ADDR bits contain the base address of the Expansion ROM. The bits correspond to the upper bits of the Expansion ROM base address. This decode permits the PCI boot manager to place the expansion ROM on a 4MByte boundary. STG2000 currently maps a 32KByte BIOS into the bottom of this 4MByte range. The writable bits are aliased between the NV and VGA devices.	R W X
21:11	ROM_BASE_RESERVED contain the lower bits of the base address of the Expansion ROM. These bits are hardwired to 0, forcing a 4MByte boundary.	R - 0
10:1	Reserved	R - 0
0	The ROM_DECODE bit indicates whether or not the STG2000 accepts accesses to its expansion ROM. When the bit is set, address decoding is enabled using the parameters in the other part of the base register. The MEMORY_SPACE bit (PCI Configuration Register 0x04, page 52) has precedence over the ROM_DECODE bit. STG2000 will respond to accesses to its expansion ROM only if both the MEMORY_SPACE bit and the ROM_DECODE bit are set to 1. 0=Expansion ROM address space is disabled 1=Expansion ROM address decoding is enabled	R W 0

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PCI Configuration Register 0x3C

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
	MAX_LAT		MIN_GNT		INTERRUPT_PIN		INTERRUPT_LINE

Bits	Function	R W I
31:24	The MAX_LAT bits contain the maximum time the STG2000 requires to gain access to the PCI bus. This read-only register is used to specify the STG2000's desired settings for Latency Timer values. The value specifies a period of time in units of 250ns. 0=No requirements (VGA function)	R - 0
23:16	The MIN_GNT bits contain the length of the burst period the STG2000 needs, assuming a clock rate of 33MHz. This read-only register is used to specify the STG2000's desired settings for Latency Timer values. The value specifies a period of time in units of 250ns. 0=No requirements (VGA function)	R - 0
15:8	The INTERRUPT_PIN bits contain the interrupt pin the device (or device function) uses. A value of 1 corresponds to **INTA#**. The NV, VGA, and real mode devices all use **INTA#**.	R - 1
7:0	The INTERRUPT_LINE bits contain the interrupt routing information. POST software will write the routing information into this register as it initializes and configures the system. The value in this field indicates which input of the system interrupt controller(s) the STG2000's interrupt pin is connected to. Device drivers and operating systems can use this information to determine priority and vector information. INTERRUPT_LINE is initialized to 0xFF (no connection) at reset. 0= Interrupt line IRQ0 1= Interrupt line IRQ1 0xF= Interrupt line IRQ15 0xFF=No interrupt line connection (reset value)	R W 0xFF

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A.2 REGISTER DESCRIPTIONS FOR FUNCTION 1 (NV)

PCI Configuration Register 0x00
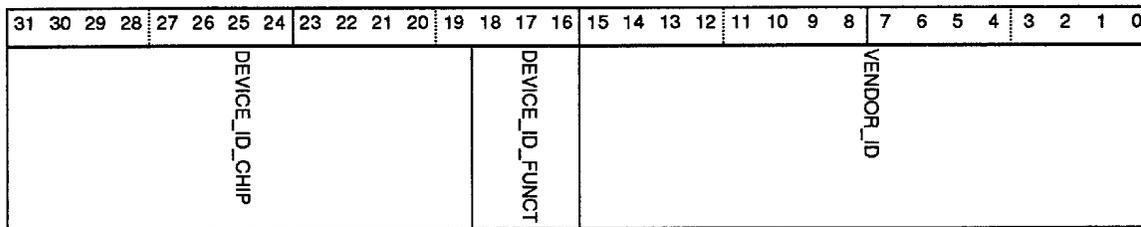
31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
	DEVICE_ID_CHIP		DEVICE_ID_FUNCT			VENDOR_ID	

Bits	Function	R W I
31:19	The DEVICE_ID_CHIP bits contain the chip number allocated by the manu-facturer to identify the particular device. 1=STG2000	R - 1
18:16	The DEVICE_ID_FUNC bits contain the function number from the Configura-tion Address bits [10:8]. 1=NV function	R - 0
15:0	VENDOR_ID bits allocated by the PCI Special Interest Group to uniquely identify the manufacturer of the device. 0x104A=SGS-THOMSON Microelectronics	R - X

PCI Configuration Register 0x04

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	SERR_SIGNALLED	RECEIVED_MASTER	RECEIVED_TARGET	Reserved	DEVSEL_TIMING			Reserved								Reserved							SERR_ENABLE	Reserved			WRITE_AND_INVAL	Reserved	BUS_MASTER	MEMORY_SPACE	IO_SPACE

Device Status Field (bits [31:16])

Bits	Function	R W I
31	Reserved	R - 0
30	SERR_SIGNALLED is set whenever the STG2000 asserts **SERR#**.	R W 0
29	RECEIVED_MASTER indicates that a master device's transaction (except for Special Cycle) was terminated with a master-abort. This bit is clearable (=1) in the NV device. 0=No abort 1=Master aborted	R W 0
28	RECEIVED_TARGET indicates that a master device's transaction was terminated with a target-abort. This bit is clearable (=1) in the NV device. 0=No abort 1=Master received target aborted	R W 0
27	Reserved	R - 0
26:25	The DEVSEL_TIMING bits indicate the timing of **DEVSEL#**. These bits indicate the slowest time that the STG2000 asserts **DEVSEL#** for any bus command except Configuration Read and Configuration Write. The STG2000 responds with fast **DEVSEL#** (0-cycle) except for retry accesses which respond with a medium **DEVSEL#**. 00=fast	R - 00
24:16	Reserved	R - X

Device Control Command Field (bits[15:0])

Bits	Function	R W I
15:9	Reserved	R - 0
8	SERR_ENABLE is an enable bit for the **SERR#** driver. 0=Disables the **SERR#** driver 1=Enables the **SERR#** driver	R W 0
7:5	Reserved	R W 0
4	WRITE_AND_INVAL is an enable bit for using the Memory Write and Invalidate command. 1=The STG2000 as bus master may generate the command 0=The Memory Write command must be used instead of Memory Write and Invalidate	R W 0
3	Reserved	R - 0

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Bits	Function	R W I
2	BUS_MASTER indicates that the device can act as a master on the PCI bus. 0=Disables the STG2000 from generating PCI accesses 1=Allows the STG2000 to behave as a bus master	R W 0
1	MEMORY_SPACE indicates that the STG2000 will respond to memory space accesses. 0=Device response disabled 1=Enables response to Memory space accesses.	R W 0
0	IO_SPACE indicates that the device will respond to I/O space accesses. Although this bit is read/writable for the NV function, it is for reference only since the NV device has no I/O space.	R W 0

PCI Configuration Register 0x08

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
		CLASS_CODE					REVISION_ID

Bits	Function	R W I
31:8	The CLASS_CODE bits identify the generic function of the device and (in some cases) a specific register-level programming interface. The register is broken into three byte-size fields. The upper byte (at offset 0x0B) is a base class code which broadly classifies the type of function the device performs. The middle-byte (at offset 0x0A) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 0x09) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. The NV function responds as 0x048000 = 'Multifunction Device'.	R - 0x048000
7:0	The REVISION_ID bits specify a device specific revision identifier. The value is chosen by the vendor. This field should be viewed as a vendor defined extension to the DEVICE_ID. 0x00=Rev A, 0x01=Rev B, 0x02=Rev C	R - X

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PCI Configuration Register 0x0C

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
	Reserved		HEADER_TYPE		LATENCY_TIMER		Reserved

Bits	Function	R W I
31:24	Reserved	R - 0
23:16	HEADER_TYPE identifies the device as single or multi-function. STG2000 responds as a multi-function device. 0x80=Multiple function device	R - 0x80
15:11	The LATENCY_TIMER bits contain, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. 0=0 clocks, 1=8 clocks, 30=240 clocks, 31=248 clocks	R W 0
10:0	Reserved	R - 0

PCI Configuration Register 0x10   Base Memory Address Register

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
BASE_ADDRESS		BASE_RESERVED					PREFETCHABLE	ADDRESS_TYPE		SPACE_TYPE

Bits	Function	R W I
31:25	The BASE_ADDRESS bits contain the most significant bits of the base address of the device. For the NV function this indicates that the STG2000 requires a 32MByte block of contiguous memory beginning on a 32MByte boundary.	R W 0
24:4	The BASE_RESERVED bits form the least significant bits of the base address and are hardwired to 0.	R - 0
3	The PREFETCHABLE bit indicates that there are no side effects on reads, that the device returns all bytes on reads regardless of the byte enables, and that host bridges can merge processor writes into this range without causing errors.	R - 1
2:1	The ADDRESS_TYPE bits contain the type (width) of the Base Address. 0=32-bit	R - 0
0	The SPACE_TYPE bit indicates whether the register maps into Memory or I/O space. 0=Memory space	R - 0

PCI Configuration Registers 0x14 - 0x24   Base Address Registers

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
0x00000000							

Bits	Function	R W I
31:0	These bits are hardwired (read-only) to 0.	R - 0

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PCI Configuration Register 0x30   Expansion ROM Base Address

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
	ROM_BASE_ADDRESS		ROM_BASE_RESERVED			Reserved	ROM_DECODE

Bits	Function	R W I
31:22	The ROM_BASE_ADDR bits contain the base address of the Expansion ROM. These bits correspond to the upper bits of the Expansion ROM base address. This decode permits the PCI boot manager to place the expansion ROM on a 4MByte boundary. STG2000 currently maps a 32KByte BIOS into the bottom of this 4MByte range. The writable bits are aliased between the NV and VGA devices.	R W X
21:11	ROM_BASE_RESERVED contain the lower bits of the base address of the Expansion ROM. These bits are hardwired to 0, forcing a 4MByte boundary.	R - 0
10:1	Reserved	R - 0
0	The ROM_DECODE bit indicates whether or not the STG2000 accepts accesses to its expansion ROM. When the bit is set, address decoding is enabled using the parameters in the other part of the base register. The MEMORY_SPACE bit (PCI Configuration Register 0x04, page 58) has precedence over the ROM_DECODE bit. STG2000 will respond to accesses to its expansion ROM only if both the MEMORY_SPACE bit and the ROM_DECODE bit are set to 1. 0=Expansion ROM address space is disabled 1=Expansion ROM address decoding is enabled	R W 0

PCI Configuration Register 0x3C

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
	MAX_LAT		MIN_GNT		INTERRUPT_PIN		INTERRUPT_LINE

Bits	Function	R W I
31:24	The MAX_LAT bits contain the maximum time the STG2000 requires to gain access to the PCI bus. This read-only register is used to specify the STG2000's desired settings for Latency Timer values. The value specifies a period of time in units of 250ns. 1=250ns (NV function)	R - 1
23:16	The MIN_GNT bits contain the length of the burst period the STG2000 needs, assuming a clock rate of 33MHz. This read-only register is used to specify the STG2000's desired settings for Latency Timer values. The value specifies a period of time in units of 250ns. 3=750ns (NV function)	R - 3
15:8	The INTERRUPT_PIN bits contain the interrupt pin the device (or device function) uses. A value of 1 corresponds to **INTA#**. The NV, VGA, and real mode devices all use **INTA#**.	R - 1
7:0	The INTERRUPT_LINE bits contain the interrupt routing information. POST software will write the routing information into this register as it initializes and configures the system. The value in this field indicates which input of the system interrupt controller(s) the STG2000's interrupt pin is connected to. Device drivers and operating systems can use this information to determine priority and vector information. INTERRUPT_LINE is initialized to 0xFF (no connection) at reset. 0=Interrupt line IRQ0 1=Interrupt line IRQ1 0xF=Interrupt line IRQ15 0xFF=No interrupt line connection (reset value)	R W 0xFF

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B   GAME PORT REGISTER

The STG2000 implements an IBM-compatible game port at I/O address 0x201. This supports four analog and four digital inputs for interfacing to joysticks and other devices used by games.

Game Port Register   0x201

7	6	5	4	3	2	1	0
DSD				ASD			

DSD   Digital Switch Data (bits [7:4], R/*/I=X)

DSD=0 Closed (trigger pressed)

DSD=1 Open (trigger not pressed)

ASD   Analog Switch Data (bits [3:0], R/*/I=X)

To determine the resistive value on an analog input, the time for the individual bits to flip from 1 to 0 must be measured. The analog bits [3:0] are set by a write to I/O location 0x201. The application must begin timing at this point and then poll until the bit corresponding to the required channel changes to a zero. The length of time for this to occur is proportional to the resistive value.

ASD=0 Timed out

ASD=1 Not timed out (waiting)

* Writing to this register will perform a reset as described above.

C   SOUND CARD EMULATION REGISTERS

C.1   STEREO MIXER REGISTERS

The stereo mixer functions, controlled through a series of indexed registers in the index space 0x00 - 0x2E, are accessed through the Stereo Mixer Index and Stereo Mixer Data registers. The stereo mixer controls the volume, output mixing and input source selection and also the stereo voice data output. The output mixing path combines signals from the Voice, MIDI, CD and Microphone sources. Input sources can be selected from CD, Line-in or Microphone; the default input source is Microphone.

C.1.1 STEREO MIXER I/O REGISTER DESCRIPTIONS

Stereo Mixer Index Register   Write - 0x224

7	6	5	4	3	2	1	0
			INDEX				

This register is written with the required index to select one of the Stereo Mixer Indexed registers.

Stereo Mixer Data Register   Write - 0x225

7	6	5	4	3	2	1	0
			DATA				

This register is written with the data of the register indexed through the Stereo Mixer Index Register.

C.1.2 STEREO MIXER INDEXED REGISTER DESCRIPTIONS

Reset Mixer Register   0x225 Index=0x00

7	6	5	4	3	2	1	0
			RM				

RM   Reset Mixer (bits [7:0], -/W/I=X)

The mixer will be reset by any 8-bit value written to this register. All Stereo Mixer registers will be restored to their default values.

Voice Volume Register   0x225 Index=0x04

7	6	5	4	3	2	1	0
	VVL		Reserved		VVR		Reserved

VVL   Voice Volume Left (bits [7:5], -/W/I=0x4)

This 3-bit value provides 8 levels of control of the left channel voice volume. Values 0 to 7 give a range of -46dB to 0dB in approximately 4dB steps. The default value of 4 corresponds to -11dB.

VVR   Voice Volume Right (bits [3:1], -/W/I=0x4)

This 3-bit value provides 8 levels of control of the right channel voice volume. Values 0 to 7 give a range of -46dB to 0dB in approximately 4dB steps. The default value of 4 corresponds to -11dB.

Mic Volume Register

7	6	5	4	3	2	1	0
Reserved					MV		Reserved

MV   Mic Mixing Volume (bits [2:1], -/W/I=0x0)

This 2-bit value provides 4 levels of control of the microphone mixing volume. Values 0 to 3 give a range of -46dB to 0dB in approximately 7dB steps. The default value of 0 corresponds to -46dB.

Input Source Register

7	6	5	4	3	2	1	0
Reserved					IS		

IS   Input Source (bits [2:1], -/W/I=0x0)

Selects the input source:

IS=0 or 2 Microphone source

IS=1 CD source

IS=3 Line-in source

Stereo Switch Register

7	6	5	4	3	2	1	0
Reserved						SS	Reserved

SS   Stereo Switch (bit 1, -/W/I=0x0)

Selects mono or stereo outputs:

SS=0 Mono

SS=1 Stereo

Master Volume Register

7	6	5	4	3	2	1	0
MVL			Reserved	MVR			Reserved

MVL   Master Volume Left (bits [7:5], -/W/I=0x4)

This 3-bit value provides 8 levels of control of the left channel master volume. Values 0 to 7 give a range of -46dB to 0dB in approximately 4dB steps. The default value of 4 corresponds to -11dB.

MVR   Master Volume Right (bits [3:1], -/W/I=0x4)

This 3-bit value provides 8 levels of control of the right channel master volume. Values 0 to 7 give a range of -46dB to 0dB in approximately 4dB steps. The default value of 4 corresponds to -11dB.

MIDI Volume Register
0x225 Index=0x26

7	6	5	4	3	2	1	0
	MIVL		Reserved		MIVR		Reserved

MIVL   MIDI Volume Left (bits [7:5], -/W/I=0x4)

This 3-bit value provides 8 levels of control of the left channel MIDI volume. Values 0 to 7 give a range of -46dB to 0dB in approximately 4dB steps. The default value of 4 corresponds to -11dB.

MIVR   MIDI Volume Right (bits [3:1], -/W/I=0x4)

This 3-bit value provides 8 levels of control of the right channel MIDI volume. Values 0 to 7 give a range of -46dB to 0dB in approximately 4dB steps. The default value of 4 corresponds to -11dB.

CD Volume Register
0x225 Index=0x28

7	6	5	4	3	2	1	0
	CDVL		Reserved		CDVR		Reserved

CDVL   CD Volume Left (bits [7:5], -/W/I=0x0)

This 3-bit value provides 8 levels of control of the left channel CD volume. Values 0 to 7 give a range of -46dB to 0dB in approximately 4dB steps. The default value of 0 corresponds to -46dB.

CDVR   CD Volume Right (bits [3:1], -/W/I=0x0)

This 3-bit value provides 8 levels of control of the right channel CD volume. Values 0 to 7 give a range of -46dB to 0dB in approximately 4dB steps. The default value of 0 corresponds to -46dB.

Line Volume Register
0x225 Index=0x2E

7	6	5	4	3	2	1	0
	LVL		Reserved		LVR		Reserved

LVL   Line Volume Left (bits [7:5], -/W/I=0x0)

This 3-bit value provides 8 levels of control of the left channel line-in volume. Values 0 to 7 give a range of -46dB to 0dB in approximately 4dB steps. The default value of 0 corresponds to -46dB.

LVR   Line Volume Right (bits [3:1], -/W/I=0x0)

This 3-bit value provides 8 levels of control of the right channel line-in volume. Values 0 to 7 give a range of -46dB to 0dB in approximately 4dB steps. The default value of 0 corresponds to -46dB.

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C.2 DSP REGISTERS

The DSP registers emulate the sound card Digital Sound Processor chip functions. These functions include:

- 8/16-bit mono/stereo digitized sound recording and playback

- Control of sampling rate

- DAC speaker control

- Control of DMA transfer

C.2.1 DSP REGISTER DESCRIPTIONS

DSP Reset Register   Write - 0x226

Resets the DSP emulation to its default state. To reset the DSP, write 0x01 to this register, pause for at least 3 microseconds, then write of 0x00. Following a reset, bit 7 of the DSP Data Available Status Register will be set and the DSP Read Data Port Register will have the value 0xAA.

DSP Read Data Port Register   Read - 0x22A

Provides access to incoming DSP data.

DSP Write Command/Data Register   Write - 0x22C

This register is used to send commands or data to the DSP. The DSP commands and functions available are shown in Table 22.

Table 22. DSP commands and functions

Function	Description
0x10	Direct mode 8-bit DAC (single-byte data transfer)
0x14	Direct mode 8-bit DAC via DMA
0x20	Direct mode 8-bit ADC (single-byte data transfer)
0x24	DMA mode 8-bit ADC
0x40	Set sampling rate
0x48	Set Block Transfer Size
0x80	Set Silence Mode Data length
0x91	High-Speed DMA mode 8-bit DAC
0x99	High-Speed DMA mode 8-bit ADC
0xD1	Turn on Speaker
0xD3	Turn off Speaker
0xD8	Get Speaker Status 0x00=off, 0xFF=on
0xD0	Halt DMA in progress
0xD4	Continue DMA
0xE1	Get DSP Version low-byte=Major high-byte=Minor

DSP Write Buffer Status Register   Read - 0x22C

7	6	5	4	3	2	1	0
CDBE	Reserved						

CDBE DSP Command/Data Buffer Empty (bit 7, R/-/X)

Indicates if the DSP command/data buffer is empty and ready to receive commands or data.

DSP Data Available Status   Read - 0x22E

7	6	5	4	3	2	1	0
DAS	Reserved						

DAS DSP Data Available Status (bit 7, R/-/X)

Indicates if there is incoming data available for reading.

C.3 FM SYNTHESIZER REGISTERS

C.3.1 REGISTER ACCESS

I/O Addresses

The FM synthesizer functions are controlled through a series of indexed registers in the index space 0x00 - 0xF5 which are accessed through the FM Music Address and FM Music Data registers described in Section C.3.2. These I/O registers are accessible at either locations 0x228/9 or 0x388/9, which are standard locations for the SoundBlaster 2.0 card and AdLib card respectively.

FM voices and operators

The FM synthesizer emulator supports nine FM voices (channels), each of which is assigned two operators (slots) through which voicing control is performed. In FM modulation mode the first operator corresponds to the modulating wave and the second to the carrier wave. These operators are controlled through four sets of registers in the index space 0x20-0x95. The mapping of channel and slot numbers to register indexes is shown in Table 23.

Table 23. Mapping of channel and slot numbers to register indexes

Channel number	1	2	3	1	2	3	4	5	6	4	5	6	7	8	9	7	8	9
Operator (slot) number for each channel	1			2			1			2			1			2		
Voicing Control Register index	20	21	22	23	24	25	28	29	2A	2B	2C	2D	30	31	32	33	34	35
KSL/Total Level Register index	40	41	42	43	44	45	48	49	4A	4B	4C	4D	50	51	52	53	54	55
Attack/Decay Rate Register index	60	61	62	63	64	65	68	69	6A	6B	6C	6D	70	71	72	73	74	75
Sustain Level/Release Rate Register index	80	81	82	83	84	85	88	89	8A	8B	8C	8D	90	91	92	93	94	95

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C.3.2 FM SYNTHESIZER I/O REGISTER DESCRIPTIONS

FM Music Address Register
Write - 0x228, 0x388

7	6	5	4	3	2	1	0
INDEX							

This register is written with the required index to select one of the indexed register described in Section C.3.3, page 71.

FM Music Status Register
Read - 0x228, 0x388

7	6	5	4	3	2	1	0
IRQ	T1F	T2F	Reserved				

IRQ Interrupt Request Status (bit 7, R/-/I=X)

IRQ=0 Indicates that both T1F and T2F are set to '0'.

IRQ=1 Indicates that either T1F or T2F is set to '1'.

T1F Timer 1 Flag (bit 6, R/-/I=X)

T1F=0 indicates that Timer 1 has not overflowed.

T1F=1 indicates that Timer 1 has overflowed.

T2F Timer 2 Flag (bit 5, R/-/I=X)

T2F=0 indicates that Timer 2 has not overflowed.

T2F=1 indicates that Timer 2 has overflowed.

FM Music Data Register
Write - 0x229, 0x389

7	6	5	4	3	2	1	0
DATA							

This register is written with the data of the register indexed through the FM Music Address Register.

C.3.3 FM SYNTHESIZER INDEXED REGISTER DESCRIPTIONS

LSI Test Register
0x229, 0x389 Index=0x01

7	6	5	4	3	2	1	0
Reserved		DS	Reserved				

DS Distortion Select (bit 5, -/W/I=X)

This bit enables the Wave Select function (see Wave Select Registers on page 80). For normal operation this bit is programmed to 0x00.

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Timer registers

There are two timer registers, Timer 1 with a resolution of 80μs and Timer 2 with a resolution of 320μs. Starting, stopping and flag control of both timers is possible. When a timer flag is set, a timer interrupt is generated.

Timer 1 Register

0x229, 0x389 Index=0x02

7	6	5	4	3	2	1	0
			T1				

T1   Timer 1 (bits[7:0], -/W/I=X)

Timer 1 is an 8-bit presettable counter with a resolution of 80μs. If an overflow occurs, the flag is set and the preset value is loaded. An overflow will occur at the rate of $T = (256-T1) \times 80\mu s$, where T1 = programmed value.

Timer 2 Register

0x229, 0x389 Index=0x03

7	6	5	4	3	2	1	0
			T2				

T2   Timer 2 (bits[7:0], -/W/I=X)

Timer 2 is an 8-bit presettable counter as described for Timer 1 but with a resolution of 320μs. An overflow will occur at the rate of $T = (256-T2) \times 320\mu s$, where T2 = programmed value

Timer Control Register

0x229, 0x389 Index=0x04

7	6	5	4	3	2	1	0
IRQR	MT1	MT2		Reserved		ST2	ST1

IRQR   IRQ reset (bit 7, -/W/I=X)

IRQR=1 resets the interrupt request flags for Timer 1 and 2 (the data on bits [6:0] is ignored and IRQR (bit 7) is reset to '0').

MT1   Mask T1 (bit 6, -/W/I=X)

MT1=1 masks the interrupt request flag for Timer 1 (the flag is set to '0' and has no effect on the operation of Timer 1).

MT2   Mask T2 (bit 5, -/W/I=X)

MT2=1 masks the interrupt request flag for Timer 2 (the flag is set to '0' and has no effect on the operation of Timer 2).

ST2   Start/Stop T2 (bit 1, -/W/I=X)

This bit controls the starting and stopping of Timer 2.

ST2=0 inhibits operation of Timer 2.

ST2=1 loads the preset value into Timer 2 and starts timing.

ST1   Start/Stop T1 (bit 0, -/W/I=X)

This bit controls the starting and stopping of Timer 1.

ST1=0 inhibits operation of Timer 1.

ST1=1 loads the preset value into Timer 1 and starts timing.

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Note Select Register

7	6	5	4	3	2	1	0
Reserved	NTS	Reserved					

NTS Note select (bit 6, -/W/I=X)

NTS=0 selects the keyboard split to be controlled from the second most significant bit of the F-number (see page 77) as shown in Table 24.

Table 24. Keyboard split for NTS=0

Block data/Octave	0		1		2		3		4		5		6		7	
F-Number (MSB)	X		X		X		X		X		X		X		X	
F-Number bit 8	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Keyboard split number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

NTS=1 selects the keyboard split to be controlled from the most significant bit of the F-number as shown in Table 25

Table 25. Keyboard split for NTS=1

Block data/Octave	0		1		2		3		4		5		6		7	
F-Number (MSB)	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
F-Number bit 8	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Keyboard split number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Voicing Control Registers

7	6	5	4	3	2	1	0
AM	VIB	EG-TYP	KSR	MUL			

AM (bit 7, -/W/I=X)

AM=0 switches AM modulation off.

AM=1 switches AM modulation on. The AM frequency is 3.7Hz; the modulation depth is determined by the AM-D bit of the Vibrato Depth/Rhythm Register at offset 0xBD.

VIB (bit 6, -/W/I=X)

VIB=1 switches on a vibrato effect. The vibrato frequency is 6.4Hz; the vibrato depth is determined by the VIBD bit of the Vibrato Depth/Rhythm Register (page 78).

EG-TYP(bit 5, -/W/I=X)

This bit switches between a connecting sound and a diminishing sound. These two voicing modes differ in the release rate of the envelope as shown in Figure 41.

EG-TYP=0 selects a diminishing sound

EG-TYP=1 selects a sustaining sound

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Figure 41. Connecting sound and diminishing sound envelopes

AR = Attack rate, DR = Decay rate, SL = Sustain level, RR = Release rate
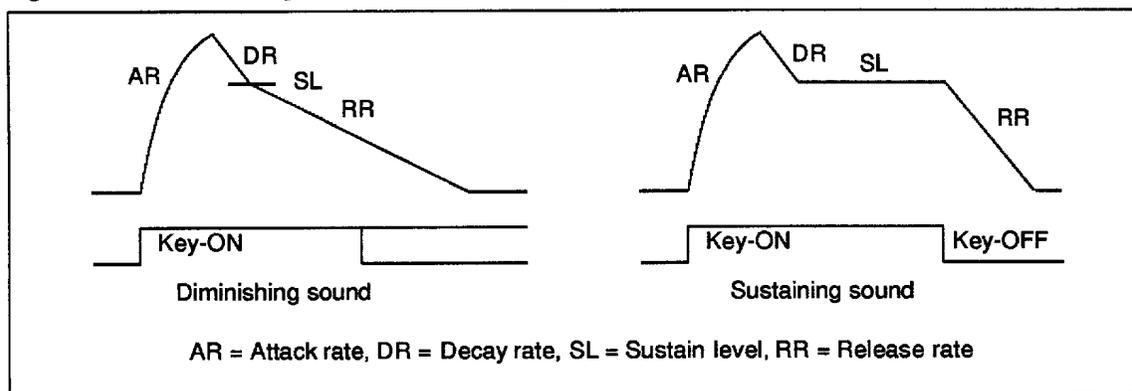
KSR Key Scaling Rate (bit 4, -/W/I=X)

This bit selects one of two key scaling offsets for the rate of DSR. The leading and trailing edges (attack and decay) of the sound of natural instruments tend to increase as the pitch becomes higher. This phenomenon is simulated by key scaling through which the rate of ADSR (Attack, Decay, Sustain and Release) is modified through the addition of an offset Rks. The general rate R for either AR, DR, SL or RR is determined by

$$R = 4 \times ADSR + Rks \text{ (as shown on page 76)}.$$

Rks = key scaling offset value

KSR=0 The key scaling offset value Rks for KSN (Key Split Number) = 0-15 are set to the values shown in Table 26.

Table 26. Key scaling offset value when KSR=0

Key Split Number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Rks	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3

KSR=1 The key scaling offset value Rks for KSN = 0-15 are set to the values shown in Table 26.

Table 27. Key scaling offset value when KSR=1

Key Split Number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Rks	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

MUL Frequency Multiple (bits [3:0], -/W/I=X)

The carrier and modulating waves frequencies are controlled by the multiples shown in Table 28.

Table 28. Frequency multiples

MUL	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Multiple	$^1/_2$	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

For example:

Frequency of F-number = ωF

Multiple for carrier wave = 2

Multiple for modulating wave = 6

F(t) = Esin (2ωft + Isin(6ωft))

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KSL/Total Level Registers

7	6	5	4	3	2	1	0
KSL		TL					

KSL Key Scaling Level (bits [7:6], -/W/I=X)

The key scaling mode simulates natural instruments' tendency for the output level to fall as the pitch increases. The degree of attenuation available in key scaling mode is set as shown in Table 29.

Table 29. Key scaling level

Bits 7 6	Degree of attenuation
0 0	0
0 1	1.5dB/Octave
1 0	3dB/Octave
1 1	6dB/Octave

TL Total Level (bits [5:0], -/W/I=X)

The total level is used to control the volume. The maximum attenuation is 47.25dB with a resolution of 0.75dB. Attenuation is controlled by setting bits[5:0] which control attenuation steps as shown in Table 30.

Table 30. Total level attenuation steps

Bit	5	4	3	2	1	0
Degree of attenuation (dB)	24	12	6	3	1.5	0.75

Attack/Decay Rate Registers

7	6	5	4	3	2	1	0
AR				DR			

AR Attack Rate (bits [7:4], -/W/I=X)

The attack rate sets the rising time for the sound envelope.

DR Decay Rate (bits [3:0], -/W/I=X)

The decay rate sets the falling time for the sound envelope.

Sustain Level/Release Rate Registers

<div align="right">0x229, 0x389 Indexes=0x80-0x85
0x88-0x8D
0x90-0x95</div>

7	6	5	4	3	2	1	0
SL				RR			

SL   Sustain Level (bits [7:4], -/W/I=X)

For sustaining sounds the sustain level specifies the point where the sound, attenuated during decay, changes to a constant level. For diminishing sounds, the sustain level gives the point where the decay rate changes to the release rate.

RR   Release Rate (bits [3:0], -/W/I=X)

The release rate determines the rate at which the sound disappears after Key-OFF. For diminishing sounds, the release rate indicates the attenuation after the sustain level is reached.

The general rate R for either AR, DR, SL or RR is determined as shown below:

$$R = (4 \times ADSR) + Rks$$

(where ADSR is the value of AR, DR, SL or RR and Rks is a function of KSR and KSN as shown on page 74).

Defining RM = $R[5:2]$ and RL = $R[1:0]$, the 0 - 96dB envelope AR, DR, SL and RR times in milliseconds can be calculated using;

$$Time\ (ms)\ = \alpha \times 2^{(1-RM)}$$

where α is a constant selected by RL. Note that for a value of RM = 0 there is no change in the envelope over time and for a value of RM = 15 the AR, DR, SL and RR times tend towards zero.

Table 31.   0-96dB attack and decay α's for RL = R[1:0]

RL=R[1:0]	0	1	2	3
Attack time α	2826.24	2252.80	1884.16	1579.44
Decay time α	39280.64	31416.32	26173.44	22446.08

F-Number Registers

7	6	5	4	3	2	1	0
			F-N				

F-N   F-Number (bits [7:0], -/W/I=X)

The F-Number is a 10-bit value which determines the frequency (note within a scale) of a particular voice. The eight least significant bits of the F-number are located in indexes 0xA0 to 0xA8 and the two most significant bits are located in bits [1:0] of indexes 0xB0 to 0xB8. The octave of the note selected by the F-Number is determined by the Block number located in bits [4:2] of indexes 0xB0 to 0xB8. The relationship between the desired frequency, F-Number and block is described by the following expression:

$$F\text{-number} = \frac{f \times 2^{19}/(fs)}{2^{Block-1}} = \frac{f \times 2^{20-Block}}{50000}$$

where f = desired frequency, fs = sampling frequency (fM/288 Hz)

Table 32 shows the required F-Numbers to achieve the tuning of an equal-tempered scale.

Table 32.   F-Numbers required for example scale

Note	Frequency (Hz)	F-Number	0xB0-0xB8 bits [1:0]	0xA0-0xA8 bits [7:0]
C	261.6	345	01	0101,1001
C#	277.2	365	01	0110,1101
D	293.7	387	01	1000,0011
D#	311.1	410	01	1001,1010
E	329.6	435	01	1011,0011
F	349.2	460	01	1100,1100
F#	370.0	488	01	1110,1000
G	392.0	517	10	0000,0101
G#	415.3	547	10	0010,0011
A	440.0	580	10	0100,0100
A#	466.2	615	10	0110,0111
B	493.9	651	10	1000,1011
C	523.3	690	10	1011,0010

Other tunings are possible, however when defining a tuning the largest F-Number possible should be used for the top note of the scale in order to minimize pitch error. When using F-Numbers in the range 345 - 690 it is recommended that the keyboard split point, NTS, be set to 1 (see Note Select Register, page 73).

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Block Registers
<div align="right">0x229, 0x389 Indexes=0xB0-0xB8</div>

7	6	5	4	3	2	1	0
Reserved		KON	BLOCK			F-N	

KON Key-ON (bit 5, -/W/I=X)

This bit controls on/off keying of the voice (see Figure 41).*

KON=1 The channel is on and voiced.

KON=0 The channel is keyed off.

BLOCK Block (Octave) select (bits [4:2])

Block specifies the octave applying to the programmed frequency (refer to the expression for deriving the F-Number, on page 77).

F-N F-Number (bits [1:0], -/W/I=X)

These are the two most significant bits of the F-Number as described above.

Vibrato Depth/Rhythm Register
<div align="right">0x229, 0x389 Index=0xBD</div>

7	6	5	4	3	2	1	0
AM-D	VIB-D	RHTM	BD	SD	TOM	TP-CY	HH

AM-D Amplitude Modulation Depth (bit 7, -/W/I=X)

Specifies the amplitude modulation depth for channels with amplitude modulation enabled (see Voicing Control Registers, page 73).

AM-D=0 Amplitude modulation depth = 1dB

AM-D=1 Amplitude modulation depth = 4.8dB

VIB-D Vibrato Depth (bit 6, -/W/I=X)

Specifies the vibrato depth for channels with vibrato enabled (see Voicing Control Registers, page 73).

VIB-D=0 Vibrato depth = 7 centitones

VIB-D=1 Vibrato depth = 14 centitones

RHTM Rhythm (bit 5, -/W/I=X)

Switches channels 7-9 to rhythm sound mode. Channels 1-6 remain in normal voice mode. Bits [4:0] of this register then provide on/off control of the rhythm instruments. In this mode the KON (Key-ON) bit of the F-Number registers at indexes 0xB6, 0xB7 and 0xB8 must be set to '0'. Table 33 shows the rhythm sounds assigned to each channel.

Table 33. Rhythm sounds assigned to each channel

Channel number	7	8	9	7	8	9
Slot number for each channel	1			2		
Instrument	BD	HH	TOM	BD	SD	TP-CY

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For the following bit definitions 1 = instrumentation on, 0 = instrumentation off.

BD   Bass Drum (bit 4, -/W/I=X)

SD   Snare Drum (bit 3, -/W/I=X)

TOM   Tom-tom (bit 2, -/W/I=X)

TP-CY   Top Cymbal (bit 1, -/W/I=X)

HH   Hi Hat (bit 0, -/W/I=X)

Feedback/Connection Registers   0x229, 0x389 Indexes=0xC0-0xC8

7	6	5	4	3	2	1	0
Reserved				FB			CON

FB   Feedback (bits [3:1], -/W/I=X)

These bits specify the modulation factor as shown in Table 34 for feedback FM modulation of slot 1 of the channel (see Figure 41).

Table 34. Modulation factor

FB	0	1	2	3	4	5	6	7
Modulation factor	0	$\pi/16$	$\pi/8$	$\pi/4$	$\pi/2$	π	2π	4π

CON   Connection (bit 0, -/W/I=X)

This bit controls the manner in which the two operators for the channel are connected.

CON=1 connects the two operators in parallel for sine wave output.

CON=0 connects the two operators in serial for FM modulation mode.

Figure 42. Operator connection options

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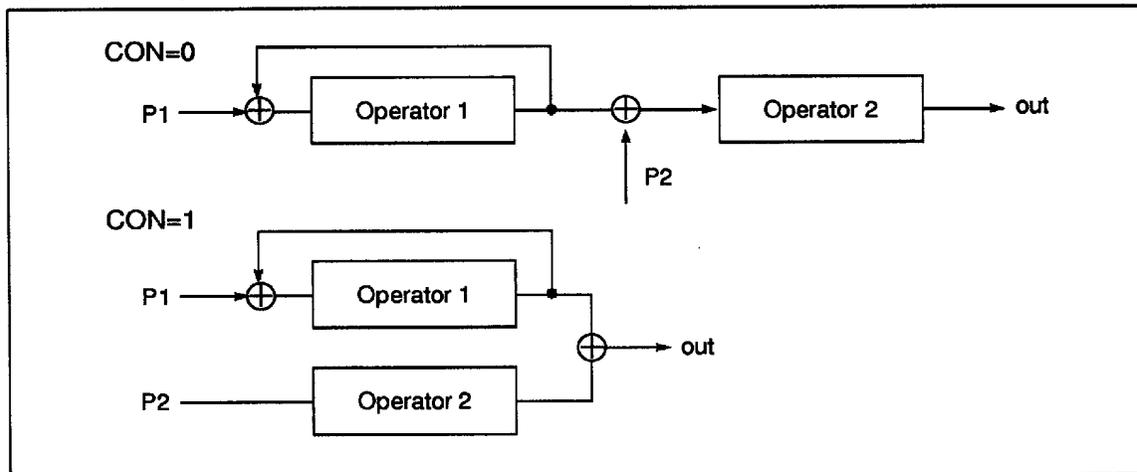
Wave Select Registers

0x229, 0x389 Indexes=0xE0-0xE5
0xE8-0xED
0xF0-0xF5

7	6	5	4	3	2	1	0
Reserved						WS	

WS Wave Select (bits [1:0], -/W/I=X)

If the DS bit of the LSI Test Register is set to '1' (see page 71), the channel output waveform will be as shown in Figure 43.

Figure 43. Waveform select options

Bits 1 0	Waveform
0 0	
0 1	
1 0	
1 1	

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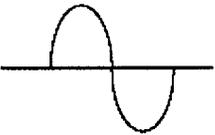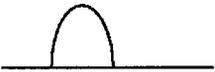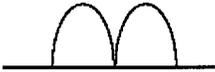
D   MPU-401 REGISTERS

The STG2000 implements an MPU-401 (MIDI Processing Unit) compatible interface. It supports simple UART mode only. UART mode is set to simple when the value 0x3F is written to the MPU Command Port Register. The MPU-401 is reset by writing 0xFF to the MPU Command Port Register. The STG2000 supports MPU-401 base addresses of 0x230, 0x300 and 0x330.

Command Port Register   0x231, 0x301 or 0x331

7	6	5	4	3	2	1	0
			MPU command				

MPU Command (bits [7:0], - W - =X)

> 0x3F=Set UART mode. Once UART mode is set, subsequent writes to this register are interpreted as data. The exception is 0xFF (reset) which must be written twice to ensure that the MPU-401 is in idle mode.

> 0xFF=Reset.

> Commands are acknowledged by the Data Port Register returning 0xFE. Note that when in UART mode the first reset command (0xFF) is not acknowledged.

Status Register   0x231, 0x301 or 0x331

7	6	5	4	3	2	1	0
SRD	SWR			Status data			

SRD   Read Status (bit 7, R - I=X)

   SRD=0 Able to read data

   SRD=1 Read buffer empty

SWR   Write status (bit 6, R - I=X)

   SWR=0 Able to write data

   SWR=1 Write buffer full. The write buffer can become full by either a write to the Data Port Register or the Command Port Register.

Data Port Register   0x230, 0x300 or 0x330

7	6	5	4	3	2	1	0
			DATA				

DATA   MPU data (bits [7:0], R/W/I=X)

E   VGA REGISTERS

E.1   GENERAL REGISTERS

Miscellaneous Output Register
<div align="right">Write - 0x3C2, Read - 0x3CC</div>

7	6	5	4	3	2	1	0
VSP	HSP	PB	Reserved	CS		ER	IOA

VSP   Vertical Sync Polarity (bit 7, R/W/I=X)

VSP=0 Positive sync polarity

VSP=1 Negative sync polarity, see Table 35

HSP   Horizontal Sync Polarity (bit 6, R/W/I=X)

HSP=0 Positive sync polarity

HSP=1 Negative sync polarity, see Table 35

Table 35.   Vertical size selection

Bits 7 6		Vertical size
0	0	Reserved
0	1	400 lines
1	0	350 lines
1	1	480 lines

PB   Page bit (bit 5, R/W/I=X)

Selects the 64K page of memory when the system is in one of the odd or even modes. (These modes are used in display modes 0, 1, 2, 3 and 7).

PB=0 selects the low 64K page of memory

PB=1 selects the high 64K page of memory

CS   Clock Select (bits [3:2] R/W/I=X)

Selects the Master Clock source according to Table 36.

Table 36.   Clock source selection

Bits 3 2		Function
0	0	Selects 25MHz clock
0	1	Selects 28MHz clock
1	0	Non-VGA standard clock selection
1	1	Non-VGA standard clock selection

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ER   Enable RAM (bit 1, R/W/I=X)

Enable access of CPU to video memory

ER=0 Disable access of the video memory from the CPU

ER=1 Enable access of the video memory from the CPU

IOA   Input/Output Address (bit 0, R/W/I=X)

Selects the CRT controller addresses to allow the monochrome adapter (MDA) to coreside with the color/graphics adapter (CGA). The write addresses to the Feature Control Register are affected in the same way.

IOA=0 sets the CRT controller addresses to 0x03Bx and the address for the Input Status Register 1 to 0x03BA.

IOA=1 sets CRT controller addresses to 0x03Dx and the Input Status Register 1 address to 0x03DA.

Feature Control Register

Write - 0x3BA (mono)/0x3DA (color), Read - 0x3CA

7	6	5	4	3	2	1	0
Reserved				VSS	Reserved		

VSS   Vertical Sync Select (bit 3, R/W/I=X)

VSS=0 Normal vertical sync output

VSS=1 Vertical sync output is the logical OR of the vertical sync and the vertical display enable

Input Status Register 0

Read - 0x3C2

7	6	5	4	3	2	1	0
VRI	Reserved (=00)		SS	Reserved			

VRI   Vertical Retrace Interrupt (bit 7, R/-/I=X)

Indicates the state of the Vertical Interrupt.

VRI=0 Vertical retrace is occurring (VBlank)

VRI=1 Vertical retrace not occurring (active display)

SS   Switch Sense (bit 4, R/-/I=X)

Indicates the sense switch status.

SS=0 Sense switch is off

SS=1 Sense switch is on

Input Status Register 1

Read - 0x3BA (mono), 0xDA (color)

7	6	5	4	3	2	1	0
Reserved				VR	Reserved		DE

VR   Vertical retrace (bit 3, R/-/I=X)

Indicates the status of vertical retrace.

VRI=0 Active display or horizontal blanking

VRI=1 Vertical retrace, video is blanked

DE   Display Enable NOT (bit 0, R/-/I=X)

Indicates the status of horizontal or vertical retrace.

DE=0 Active display

DE=1 Horizontal or vertical retrace, video is blanked

E.2 SEQUENCER REGISTERS

Sequencer Address Register

0x3C4

7	6	5	4	3	2	1	0
Reserved					INDEX		

INDEX Sequencer address (index) (bits[2:0], R/W/I=X)

These bits contain the index (0x00 to 0x04) of the currently active sequencer data register.

Reset register

0x3C5, Index=0x00

7	6	5	4	3	2	1	0
Reserved						SR	SR

SR   Synchronous Reset (bit 1, R/W/I=X)

Generates a synchronous reset. A synchronous reset preserves memory contents and must be used before changing the Clocking Mode Register in order to preserve memory contents.

SR=0 Generate and hold the system in a reset condition

SR=1 Release the reset if bit 0 is inactive

SR   Synchronous Reset (bit 0, R/W/I=X)

Identical in operation to bit 1.

Clocking mode register

0x3C5, Index=0x01

7	6	5	4	3	2	1	0
Reserved		SO	S4	DC	SL	Reserved	8/9

SO   Screen Off (bit 5, R/W/I=X)

SO=0 Screen is turned on

SO=1 Screen is turned off

S4   Shift Four (bit 4, R/W/I=X)

Controls how often the video serializers should be loaded

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S4=0 Load the serializers every character clock cycle

S4=1 Load the serializers every forth character clock cycle

DC   Dot clock (bit 3, R/W/I=X)

The dot clock is the basic VGA dot rate clock derived from the Master Clock (as selected by the CS bits of the Miscellaneous Output Register, page 82)

DC=0 Sets the dot clock to the same frequency as the Master Clock

DC=1 Selects the dot clock to run at the Master Clock frequency divided by 2

SL   Shift Load (bit 2, R/W/I=X)

This bit is significant only if bit 4 (S4) =0. These two bits combined allow the serializers to be loaded every cycle, every other cycle or every fourth cycle of the character clock.

SL=0 Load the serializers every character clock cycle

SL=1 Load the serializers every other character clock cycle

8/9   8/9 Dot clocks (bit 0, R/W/I=X)

Selects 8 or 9 dots per character modes. The 9 dot mode is used for alphanumeric modes 0+, 1+, 2+, 3+, 7 and 7+ only. All other modes must use 8 dots per character clock. Also see the ELG (Enable Line Graphic) bit of the Attribute Mode Control Register, page 100.

8/9=0 The character clock is generated 8 dots wide

8/9=1 The character clock is generated 9 dots wide

Map Mask Register   0x3C5, Index=0x02

7	6	5	4	3	2	1	0
Reserved				EM3	EM2	EM1	EM0

EM[3:0] Enable Map (bits[3:0], R/W/I=X)

When set to 1, the Enable Map bits enable system access to the corresponding map (VGA display plane).

Character Map Select Register   0x3C5, Index=0x03

7	6	5	4	3	2	1	0
Reserved		CMAH	CMBH	CMA		CMB	

In alphanumeric modes, bit 3 of the attribute byte normally defines the foreground intensity. This bit can be redefined as a switch between character sets, allowing 512 displayable characters. To enable this feature the Extended Memory (EM) bit in the Memory Mode Register (Index 0x04) should be set to 1 and different values for Character Map A and Character Map B should be selected.

CMAH   Character Map A Select (MSB) (bit 5, R/W/I=X)

This bit is the most significant bit of the CMA field (see below).

CMBH   Character Map B Select (MSB) (bit 4, R/W/I=X)

This bit is the most significant bit of the CMB field (see below).

CMA   Character Map A (bits[3:2], R/W/I=X)

In conjunction with bit 5 (CMAH) selects one of eight possible character sets when the character's attribute byte, bit 3=1.

CMB Character Map B (bits[1:0], R/W/I=X)

In conjunction with bit 4 (CMBH) selects one of eight possible character sets when the character's attribute byte, bit 3=0.

Memory Mode Register
0x3C5, Index=0x04

7	6	5	4	3	2	1	0
Reserved				C4	O/E	EM	Reserved

C4 Chain 4 (bit 3, R/W/I=X)

This bit controls whether the display planes are selected via the Read Map Select Register (0x3CF, Index 0x04) or if the display planes are selected by the low order A1 and A0 address bits.

C4=0 Display planes selected via the Read Map Select Register

C4=1 Display planes are selected by the low order A1 and A0 address bits.

O/E Odd/Even (bit 2, R/W/I=X)

Determines whether a display plane is addressed sequentially or whether odd addresses access display planes 1 and 3 and even addresses access display planes 0 and 2. The value of this bit should always complement that of the O/E field in the Mode Register (0x3CF, Index 0x05).

O/E=0 Enables the odd/even addressing mode

O/E=1 Sequential addressing mode

EM Extended Memory (bit 1, R/-/I=1)

This bit has a value of 1 and is read only.

EM=1 Extended memory is present. It indicates that VGA display memory is 256Kbytes.

E.3 CRT CONTROLLER REGISTERS

CRT Controller Address Register
0x3B4 (mono), 0x3D4 (color)

7	6	5	4	3	2	1	0
Reserved			INDEX				

INDEX CRT Controller Register Address (index) (bits[4:0], R/W/I=X)

These bits contain the index (0x00 to 0x18) of the currently active CRT controller data register (0x3B5/3D5).

Horizontal Total Register
0x3B5 (mono), 0x3D5 (color), Index=0x00

7	6	5	4	3	2	1	0
HT							

HT Horizontal Total (bits[7:0], R/W/I=X)

Programmed value = Total number of horizontal characters required -5.

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Horizontal Display End Register
0x3B5 (mono), 0x3D5 (color), Index=0x01

7	6	5	4	3	2	1	0
				HDE			

HDE Horizontal Display End (bits[7:0], R/W/I=X)

Programmed value = Number of displayed characters per line -1.

Start Horizontal Blanking Register
0x3B5 (mono), 0x3D5 (color), Index=0x02

7	6	5	4	3	2	1	0
				SHB			

SHB Start Horizontal Blanking (bits[7:0], R/W/I=X)

Programmed value = Character count which determines the point at which the Horizontal Blank signal goes active relative to the start of active display.

End Horizontal Blanking
0x3B5 (mono), 0x3D5 (color), Index=0x03

7	6	5	4	3	2	1	0
Reserved	DES			EHB			

Reserved (bit 7)

This bit =1 for normal operation.

DES Display Enable Skew (bits[6:5], R/W/I=X)

These bits control the amount of skew in character clocks that the display enable signal is delayed.

EHB End Horizontal Blanking (bits[4:0], R/W/I=X)

This field determines the end of the horizontal blanking period. The most significant bit is located in the EHB field of the End Horizontal Retrace Register.

Start Horizontal Retrace Register
0x3B5 (mono), 0x3D5 (color), Index=0x04

7	6	5	4	3	2	1	0
				SHR			

SHR Start Horizontal Retrace (bits[7:0], R/W/I=X)

These bits specify the character position where the horizontal retrace signal goes active.

End Horizontal Retrace Register
0x3B5 (mono), 0x3D5 (color), Index=0x05

7	6	5	4	3	2	1	0
EHB	HRD			EHR			

EHB End Horizontal Blanking (bit 7, R/W/I=X)

The most significant bit of the EHB field in the End Horizontal Blanking Register.

HRD Horizontal Retrace Delay (bits [6:5], R/W/I=X)

These bits control the skew of the horizontal retrace signal (from 0 to 3 character clock units).

EHR   End Horizontal Retrace (bits [4:0], R/W/I=X)

This field is compared with the Start Horizontal Retrace Register to give a horizontal character count at which the horizontal retrace signal goes inactive. When the low-order five bits of the Start Horizontal Retrace Register equal the five bits in the EHR field, the retrace time will end.

Vertical Total Register   0x3B5 (mono), 0x3D5 (color), Index=0x06

7	6	5	4	3	2	1	0
				VT			

VT   Vertical Total (bits [7:0], R/W/I=X)

This register contains the 8 low-order bits of a 10-bit vertical total. The vertical total value is the number of horizontal raster scans on the display, including vertical retrace, minus 2. This value determines the period of the vertical retrace signal.

The two high-order bits of this field are located in the Overflow Register (Index 0x07).

Overflow Register   0x3B5 (mono), 0x3D5 (color), Index=0x07

7	6	5	4	3	2	1	0
VRS9	VDE9	VT9	LC8	VBS8	VRS8	VDE8	VT8

VRS9   Vertical Retrace Start Bit 9 (bit 7, R/W/I=X)

Bit 9 of the Vertical Retrace Start value. The 8 low-order bits are located in the Vertical Retrace Start Register (Index 0x10). Bit 8 of this value is located in bit 2 of this register (VRS8).

VDE9   Vertical Display End Bit 9 (bit 6, R/W/I=X)

Bit 9 of the Vertical Display End value. The 8 low-order bits are located in the Vertical Display End Register (Index 0x12). Bit 8 of this value is located in bit 1 of this register (VDE8).

VT9   Vertical Total Bit 9 (bit 5, R/W/I=X)

Bit 9 of the Vertical Total value. The 8 low-order bits are located in the Vertical Total Register (Index 0x06). Bit 8 of this value is located in bit 0 of this register (VT8).

LC8   Line Compare Bit 8 (bit 4, R/W/I=X)

Bit 8 of the Line Compare value. The 8 low-order bits are located in the Line Compare Register (Index 0x17).

VBS8   Start Vertical Blanking Bit 8 (bit 3, R/W/I=X)

Bit 8 of the Start Vertical Blanking value. The 8 low-order bits are located in the Start Vertical Blanking Register (Index 0x15).

VRS8   Vertical Retrace Start Bit 8 (bit 2, R/W/I=X)

Bit 8 of the Vertical Retrace Start value, see bit 7 (VRS9) above.

VDE8   Vertical Display Enable End Bit 8 (bit 1, R/W/I=X)

Bit 8 of the Vertical Display Enable End value, see bit 6 (VDE9) above.

VT8   Vertical Total Bit 8 (bit 0, R/W/I=X)

Bit 8 of the Vertical Total value, see bit 5 (VT9) above.

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Preset Row Scan Register

0x3B5 (mono), 0x3D5 (color), Index=0x08

7	6	5	4	3	2	1	0
Reserved	BP		PRS				

BP Byte Panning (bits [6:5], R/W/I=X)

Specifies the number of bytes to pan during a multiple shift panning operation.

PRS Preset Row Scan (bits [4:0], R/W/I=X)

Specifies the row scan count for the top row of character on the screen. Normally the value in this field is 0 which displays the full vertical extent of the top row of characters.

Maximum Scan Line Register

0x3B5 (mono), 0x3D5 (color), Index=0x09

7	6	5	4	3	2	1	0
2T4	LC9	VBS9	MSL				

2T4 200 to 400 Line Conversion (bit 7, R/W/I=X)

Allows a 200-line mode to be displayed on 400 display lines.

2T4=0 Normal operation, 200-line mode displayed without conversion

2T4=1 Display 200 lines on 400-line display

LC9 Line Compare Bit 9 (bit 6, R/W/I=X)

Bit 9 of the Line Compare value. The 8 low-order bits are located in the Line Compare Register (Index 0x17). Bit 8 of this value is located in bit 4 of the Preset Row Scan Register (LC8).

VBS9 Start Vertical Blanking Bit 9 (bit 5, R/W/I=X)

Bit 9 of the Start Vertical Blanking value. The 8 low-order bits are located in the Start Vertical Blanking Register (Index 0x15). Bit 8 of this value is located in bit 3 of the Preset Row Scan Register (VBS8).

MSL Maximum Scan Line (bits [4:0], -/W/I=X)

Specifies the number of scan lines per character row. The value of this field is the maximum row scan number minus 1.

Cursor Start Register

0x3B5 (mono), 0x3D5 (color), Index=0x0A

7	6	5	4	3	2	1	0
Reserved		CD	Reserved	CS			

CD Cursor Disable (bit 5, R/W/I=X)

CD=0 Cursor on

CD=1 Cursor off

CS Cursor Start (bits [3:0], R/W/I=X)

Specifies the first scan line within a character box where the cursor begins.

Cursor End Register
0x3B5 (mono), 0x3D5 (color), Index=0x0B

7	6	5	4	3	2	1	0
Reserved	CSK		CE				

CSK   Cursor Skew (bits [6:5], R/W/I=X)

Specifies the number of character clocks the cursor is shifted to the right.

CE   Cursor end (bits [4:0], R/W/I=X)

Specifies the row within the character box where the cursor ends.

Start Address High Register
0x3B5 (mono), 0x3D5 (color), Index=0x0C

7	6	5	4	3	2	1	0
SAH							

SAH   Start Address High (bits [7:0], R/W/I=X)

The high order byte of the 16-bit starting address pointing to the first address after vertical retrace of the display buffer.

Start Address Low Register
0x3B5 (mono), 0x3D5 (color), Index=0x0D

7	6	5	4	3	2	1	0
SAL							

SAL   Start Address Low (bits [7:0], R/W/I=X)

The low order byte of the 16-bit starting address pointing to the first address after vertical retrace of the display buffer.

Cursor Location High Register
0x3B5 (mono), 0x3D5 (color), Index=0x0E

7	6	5	4	3	2	1	0
CLH							

CLH   Cursor Location High (bits [7:0], R/W/I=X)

The high order byte of the 16-bit display buffer address defining the cursor location.

Cursor Location Low Register
0x3B5 (mono), 0x3D5 (color), Index=0x0F

7	6	5	4	3	2	1	0
CLL							

CLL   Cursor Location Low (bits [7:0], R/W/I=X)

The low order byte of the 16-bit display buffer address defining the cursor location.

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Vertical Retrace Start Register   0x3B5 (mono), 0x3D5 (color), Index=0x10

7	6	5	4	3	2	1	0
				VRS			

VRS   Vertical Retrace Start (bits [7:0], R/W/I=X)

The eight low-order bits of the 9-bit start position of the vertical retrace signal, programmed in horizontal scan lines. Bit 8 is in the Overflow Register (Index 0x07).

Vertical Retrace End Register   0x3B5 (mono), 0x3D5 (color), Index=0x11

7	6	5	4	3	2	1	0
PR	BW	DVI	CVI		EVR		

PR   Protect Registers 0-7 (bit 7, R/W/I=X)

Protects CRT controller registers at indexes 0 - 7 from being modified.

PR=0 Enables write access to CRT controller registers

PR=1 Disables write access to CRT controller registers

BW   Bandwidth (bit 6, R/W/I=X)

Selects three or five DRAM refresh cycles per horizontal line. This Read/Write location does not have any controlling function and is supported for compatibility only.

DVI   Disable Vertical Interrupts (bit 5, R/W/I=X)

DVI=0 Enable vertical interrupts

DVI=1 Disable vertical interrupts

CVI   Disable Vertical Interrupts (bit 4, R/W/I=X)

CVI=0 Clear vertical interrupts

CVI=1 No effect

EVR   End Vertical Retrace (bits [3:0], R/W/I=X)

These four bits are compared with the value in the Vertical Retrace Start Register (Index 0x10) to determine when the vertical retrace period ends.

Vertical Display Enable End Register   0x3B5 (mono), 0x3D5 (color), Index=0x12

7	6	5	4	3	2	1	0
				VDE			

VDE   Vertical Display Enable End (bits [7:0]) R/W/I=X)

The eight low-order bits of a 10-bit value that determines the last horizontal scan line of the display. This value is equal to the total number of scan lines minus 1.

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Offset Register   0x3B5 (mono), 0x3D5 (color), Index=0x13

7	6	5	4	3	2	1	0
OFF							

OFF   Character Offset Pitch (bits [7:0], R/W/I=X)

This field determines the logical line width of the display. The offset value corresponds to the difference between the addresses of two vertically neighboring pixels.

Underline Location Register   0x3B5 (mono), 0x3D5 (color), Index=0x14

7	6	5	4	3	2	1	0
Reserved	DW	CB4	UL				

DW   Doubleword Mode (bit 6, R/W/I=X)

Selects normal addressing or doubleword addressing.

DW=0 Normal word addressing

DW=1 Doubleword addressing

CB4   Count by Four (bit 5, R/W/I=X)

If doubleword addressing is enabled, this field controls the clock to the memory address counter.

CB4=0 Normal clocking

CB4=1 Divide the clock to the memory address counter by 4

UL   Underline Location (bits [4:0], R/W/I=X)

The value in this field plus 1 determines the horizontal scan line within a character box on which the underline will occur.

Start Vertical Blank Register   0x3B5 (mono), 0x3D5 (color), Index=0x15

7	6	5	4	3	2	1	0
VBS							

VBS   Vertical Blank Start (bits [7:0], R/W/I=X)

The low order 8 bits of the 9-bit value that is compared to the horizontal scan line counter (bit 8 is in the Overflow Register (Index 0x07). When these two values are equal, the vertical blanking period begins.

End Vertical Blank Register   0x3B5 (mono), 0x3D5 (color), Index=0x16

7	6	5	4	3	2	1	0
Reserved	VBE						

VBE   Vertical Blank End (bits [6:0], R/W/I=X)

This 7-bit value is compared to the horizontal scan line counter. When these two values are equal, the vertical blanking period ends.

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Mode Control Register

0x3B5 (mono), 0x3D5 (color), Index=0x17

7	6	5	4	3	2	1	0
HW	W/B	AW	Reserved	CBT	HRS	SRS	CMS

HW   Hardware Reset (bit 7, R/W/I=X)

Enables or disables generation of the hardware horizontal and vertical retrace signals, display enable signals and blanking signals.

HW=0 Reset condition, timing signals disabled.

HW=1 Timing signals enabled.

W/B   Word/Byte Mode (bit 6, R/W/I=X)

Controls the way display memory is addressed.

W/B=0 Word mode is selected. This mode shifts the memory address counter bits down one bit; the most significant bit of the counter appears on the least significant bit of the memory address outputs.

W/B=1 Byte mode is selected; addresses are output to the display memory without being shifted.

AW   Address Wrap (bit 5, R/W/I=X)

Determines whether bit 13 or 15 should be output on the least significant address line to the display memory when the system is in word mode.

AW=0 Address bit 13 is selected as the least significant address bit to the display memory.

AW=1 Address bit 15 is selected as the least significant address bit to the display memory.

CBT   Count By Two (bit 3, R/W/I=X)

This bit is used to create either a byte or word refresh address for the display buffer.

CBT=0 Address counter uses the character clock (byte address).

CBT=1 Address counter uses the character clock divided by two (word address).

HRS   Horizontal Retrace Select (bit 2, R/W/I=X)

This bit selects the clock controlling the vertical timing counter to be either the horizontal retrace clock (HRS=0) or horizontal retrace clock divided by 2 (HRS=1).

Dividing the clock effectively doubles the vertical resolution of the CRT controller. The vertical counter has a maximum resolution of 1024 scan lines because the vertical total value is 10 bits wide. If the vertical counter is clocked with the horizontal retrace divided by 2, the vertical resolution is doubled to 2048 scan lines.

SRS   Select Row Scan Counter (bit 1, R/W/I=X)

This bit selects the source of bit 14 of the output multiplexer. When set to 0, bit 1 of the row scan counter is the source. When set to 1, bit 14 of the address counter is the source.

CMS   Compatibility Mode Support (bit 0, R/W/I=X)

The CMS bit selects the source of bit 13 of the output multiplexer. When set to 0, bit 0 of the row scan counter is the source. When set to 1, bit 13 of the address counter is the source.

Line Compare Register   0x3B5 (mono), 0x3D5 (color), Index=0x18

7	6	5	4	3	2	1	0
				LC			

LC   Line Compare (bits [7:0], R/W/I=X)

The 8 low order bits of the 10-bit Line Compare value. When the vertical counter reaches the Line Compare target value the internal address of the line counter is cleared. This creates a split screen where the lower screen is immune to scrolling. Bit 8 of this value is in the Overflow Register (page 88) and bit 9 in the Maximum Scan Line Register (page 89).

E.4 GRAPHICS CONTROLLER REGISTERS

Graphics Controller Address Register   0x3CE

7	6	5	4	3	2	1	0
	Reserved				INDEX		

INDEX   Graphics Controller Address (index) (bits[3:0], R/W/I=X)

This register is loaded with an index to the desired data register within the graphics controller. This index value is added to the graphics controller offset to access the data register.

Set/Reset Register   0x3CF, Index=0x00

7	6	5	4	3	2	1	0
	Reserved				S/R		

S/R   Set/Reset (bits [3:0], R/W/I=X)

These bits contain the value (0 or 1) written to the respective display plane when enabled by the Enable Set/Reset Register (Index 0x01).

Bit 0 = Value for display plane 0

Bit 1 = Value for display plane 1

Bit 2 = Value for display plane 2

Bit 3 = Value for display plane 3

Enable Set/Reset Register   0x3CF, Index=0x01

7	6	5	4	3	2	1	0
	Reserved				ESR		

ESR   Set/Reset (bits [3:0], R/W/I=X)

These bits enable the value contained in the Set/Reset Register (Index 0x00) to be written to the respective display plane. When a bit is set to 1, the respective display plane receives the value contained in the Set/Reset Register, when set to 0 that plane is written with data from the system (CPU).

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Color Compare Register

7	6	5	4	3	2	1	0
Reserved				CC			

CC   Color Compare (bits [3:0], R/W/I=X)

The value in this field represents a 4-bit color. This color value, contained in bits 3 to 0, is compared with display planes 3 to 0 respectively. A mask for the color compare operation is contained in the Color Don't Care Register (Index 0x07).

Data Rotate Register

7	6	5	4	3	2	1	0
Reserved			FS		DR		

FS   Function Select (bits [4:3], R/W/I=X)

Data written from the host to the display memory may be modified according to a logic function performed with data already present in display memory. The function selected is determined as shown in Table 37.

Table 37. Function select operations

Bits 4	3	Function
0	0	Data is written unmodified
0	1	Data ANDed with latched data
1	0	Data ORed with latched data
1	1	Data XORed with latched data

DR   Data Rotate (bits [2:0], R/W/I=X)

Data written from the host to display memory will be rotated to the right by the rotate count contained in this field. If a rotate operation is selected, it will be performed before the logical function selected in the FS field.

Read Map Select Register

7	6	5	4	3	2	1	0
Reserved						RMS	

RMS   Read Map Select (bits [1:0], R/W/I=X)

These bits select the display plane for system read operations.

Mode Register

0x3CF, Index=0x05

7	6	5	4	3	2	1	0
Reserved	SR		O/E	RM	Reserved	WM	

SR   Shift Register (bits [6:5], R/W/I=X)

This field controls the formatting of data output from the display planes. Formatting of data for straight VGA addressing, CGA compatibility or VGA mode 0x13 (265 color) are selected as shown in Table 38.

Table 38.   Formatting of data output

Bits 6 5	Function
0 0	Output the data with each display plane output on its associated serial output. This is the standard VGA format.
0 1	Output the data in a CGA compatible 320x200, four color graphics mode. This is used in display modes 0x04 and 0x05.
1 x	Output the data eight bits at a time from the four bit planes. This is the format for VGA mode 0x13.

O/E   Odd/Even (bit 4, R/W/I=X)

This bit is used to select between the VGA or CGA compatible mode of operation. It should always be the complement of the O/E bit in the Memory Mode Register (0x3C5, Index=0x04).

OE=0 Normal operating VGA mode. Display planes are addressed sequentially.

OE=1 CGA compatible mode. Even host addresses access even display planes (0 and 2) and odd host addresses access odd display planes (1 and 3).

RM   Read Mode (bit 3, R/W/I=X)

RM=0 Selects Read Mode 0. The system reads data from the display plane selected by the Read Map Select Register or selected by the two low order bits of the memory address (depending on the setting of the Chain 4 bit in the Memory Mode Register (0x3C5, Index=0x04)).

RM=1 Selects Read Mode 1. The system reads the results of the comparison of the four display planes and the Color Compare Register (Index 0x02).

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WM   Write Mode (bits [1:0], R/W/I=X)

This field selects Write Modes 0-3 as shown in Table 39.

Table 39.   Write Modes 0-3

Bits 1	0	Function
0	0	Write Mode 0. The default mode. Each display plane is written with system data (if enabled by the Map Mask Register, page 85). If a count is specified in the Data Rotate Register (Index 0x03) the data is rotated. If the set/reset function is enabled for a specific plane, that plane receives the 8-bit value contained in the Set/Reset register.
0	1	Write Mode 1. This mode allows eight neighboring horizontal pixels in all four planes to be moved from one display memory location to another.
1	0	Write Mode 2. This mode writes to eight neighboring pixels in all four display planes simultaneously. Display plane n (0 through 3) is filled with 8 bits of the value (0 or 1) of data bit n.
1	1	Write Mode 3. Each display plane is written with the 8-bit value contained in the Set/Reset Register (Index 0x00) for that plane (the Enable Set/Reset Register has no effect). Rotated system data is ANDed with the Bit Mask Register (Index 0x08) to form an 8-bit value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

Miscellaneous Register   0x3CF, Index=0x06

7	6	5	4	3	2	1	0
Reserved				MM		COE	G/A

MM   Memory Map (bits [3:2], R/W/I=X)

Display memory is mapped into the host processor's memory address space as shown in Table 40.

Table 40.   Mapping of display memory

Bits 3	2	Function
0	0	0xA0000 - 0xAFFFF (64KByte)
0	1	0xA0000 - 0xAFFFF (64KByte), VGA modes 8-13
1	0	0xB0000 - 0xB0FFF (4KByte), VGA mode 7
1	1	0xB8000 - 0xBFFFF (32KByte), VGA modes 0-6

COE   Chain Odd/Even (bit 1, R/W/I=X)

COE=0 Standard VGA addressing

COE=1 The host address bit 0 is replaced by a higher order address bit, causing even host addresses to access planes 0 and 2 and odd addresses to access planes 1 and 3. Used for MDA emulation.

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G/A Graphics/Alphanumerics Mode (bit 0, R/W/I=X)

GA=0 Selects the alphanumeric operating mode

GA=1 Selects the graphics operating mode

Color Don't Care Register

0x3CF, Index=0x07

7	6	5	4	3	2	1	0
Reserved				CDC			

CDC Color Don't Care (bits [3:0], R/W/I=X)

Bits 0-3 contain mask bits for the respective display planes in the color comparison operation described for the Color Compare Register (Index 0x02). This register is used in Read Mode 1 only (as determined by the RM field of the Mode Register, page 96).

0= Plane does not participate in comparison operation.

1= Compare normal

Bit Mask Register

0x3CF, Index=0x08

7	6	5	4	3	2	1	0
BM							

BM Bit mask (bits [7:0], R/W/I=X)

This register applies to all display planes simultaneously. The eight bits of the BM field correspond to eight horizontal neighboring pixels.

BM=0 When a bit is set to 0, the corresponding bit position in each display plane is masked to prevent change.

BM=1 When a bit is set to 1, the corresponding bit position in each plane can be changed.

E.5 ATTRIBUTE CONTROLLER REGISTERS

Attribute Address Register

Write - 0x3C0, Read - 0x3C1

7	6	5	4	3	2	1	0
Reserved		PAS	INDEX				

The Attribute Address Register shares a common address with the indexed attribute register. Access to these registers is controlled by the setting of an internal flip-flop. If the state of the flip-flop = 0 the Attribute Address Register will be accessed, if the state = 1, the indexed attribute register will be accessed. The flip-flop state is cleared by reading the Input Status Register 1 (Read - 0x3BA (mono), 0x3DA (color)) and toggled following each write to the Attribute Address Register.

PAS Palette Address Source (bit 5, R/W/I=X)

This bit is set to zero when loading the attribute registers and set to 1 for normal operation.

INDEX Attribute controller address (index) (bits[4:0], R/W/I=X)

These bits contain the index (0x00 to 0x14) of the Attribute Controller data register required to be accessed.

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Palette Registers 0 - F

Write - 0x3C1, Read - 0x3C1, Indexes=0x00 - 0x0F

7	6	5	4	3	2	1	0
Reserved		SR	SG	SB	R	G	B

The 6-bit Palette Registers allow dynamic mapping between the text attribute or graphic color input value and the display color on the CRT screen. The Palette registers should be modified only during vertical retrace to avoid unwanted effects on the displayed image.

SR Secondary Red (bit 5, R/W/I=X)

0=No secondary red, 1=secondary red present

SG Secondary Green (bit 4, R/W/I=X)

0=No secondary green, 1=secondary green present

SB Secondary Blue (bit 3, R/W/I=X)

0=No secondary blue, 1=secondary blue present

R Red (bit 2, R/W/I=X)

0=No red, 1= red present

G Green (bit 1, R/W/I=X)

0=No green, 1=green present

B Blue (bit 0, R/W/I=X)

0=No blue, 1=blue present

Attribute Mode Control Register

Write - 0x3C1, Read - 0x3C1, Index=0x10

7	6	5	4	3	2	1	0
IPS	PCS	PPC	Reserved	B/I	ELG	Reserved	

IPS Internal Palette Size (bit 7, R/W/I=X)

This bit selects the source of video bits [5:4] that act as inputs to the video DAC.

IPS=0 Video bits [5:4] are the outputs of the Palette Registers (Indexes 0x00 - 0x0F, see above).

IPS=1 Video bits [5:4] are bits [1:0] of the Color Select Register (Index 0x14)

PCS Pixel Clock Select (bit 6, R/W/I=X)

Allows selection of 256 colors in mode 0x13.

PCS=0 Normal operation

PCS=1 The video data is sampled so that 8 bits are available in the 256 color mode (0x13)

PPC Pixel Panning Compatibility (bit 5, R/W/I=X)

This bit allows a section of the screen to be panned independently during split screen operation.

PPC=0 Normal operation, line compare has no effect on the output of the Pixel Panning Register.

PPC=1 Top screen panning enabled in split screen mode. Line compare modifies output of the Pixel Panning Register.

B/I Enable Blink or Intensity (bit 3, -/W/I=X)

B/I=0 The most significant bit of the attribute byte selects the background intensity.

B/I=1 Enables blinking

ELG Enable Line Graphics Character Code (bit 2, -/R/I=0)

ELG=0 Set the ninth dot of the character to the background color, regardless of the character code.

ELG=1 Set the ninth dot of the character to the same value as the eighth dot for all graphics line characters (to support special line-character codes 0xC0 - 0x0F).

Overscan Color Register   Write - 0x3C0, Read - 0x3C1, Index=0x11

7	6	5	4	3	2	1	0
				OC			

OC Overscan Color (bits [7:0], R/W/I=X)

Selects the color of the border (overscan) region of the display. Bits [7:0] address the Palette-DAC look-up table to select an 8-bit indexed color (1 of 256 colors from the standard palette).

Color Plane Enable Register   Write - 0x3C0, Read - 0x3C1, Index=0x12

7	6	5	4	3	2	1	0
	Reserved				CPE		

CPE Color Planes Enable (bits [3:0], R/W/I=X)

The display planes may be selected or deselected depending on the values in this field. If a bit is set to 1, the respective plane is selected. Any combination of planes can be selected simultaneously.

Horizontal Pixel Panning Register   Write - 0x3C0, Read - 0x3C1, Index=0x13

7	6	5	4	3	2	1	0
	Reserved				HPP		

HPP Horizontal Pixel Pan (bits [3:0], R/W/I=X)

Specifies the number of pixels to shift the video data to the left as shown in Table 41. It is used in conjunction with the starting address for smooth panning operations.

Table 41. Horizontal pixel panning (number of pixels shifted to the left)

Register value (HPP)	Mode 13	Alphanumeric modes	All other modes
0	0	1	0
1	-	2	1
2	1	3	2
3	-	4	3
4	2	5	4
5	-	6	5
6	3	7	6
7	-	8	7
8	-	0	-

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Color Select Register   Write - 0x3C0, Read - 0x3C1, Index=0x14

7	6	5	4	3	2	1	0
Reserved				C67		C45	

C67   Color Register Address Bits 6 and 7 (bits [3:2], R/W/I=X)

Address bits 6 and 7 are combined with the six bits from the color palette to form the 8-bit address to the Palette-DAC.

C45   Color Register Address Bits 4 and 5 (bits [1:0]], R/W/I=X)

Address bits 4 and 5 are combined with the two bits in the C67 field and the four low order bits from the color palette to form the 8-bit address to the Palette-DAC. This field is only used if the IPS field of the Mode Control Register is set to 1.