Integrated 2D/3D graphics accelerator – Product Overview

FEATURES

- PowerVR™ Series 3 arcade performance 3D
  - DirectX7 Flexible Vertex Format support
  - 8 layer Multi-texturing
  - Twin high performance texturing pipelines
  - Full triangle setup (hidden surface removal, shading and texturing)
  - RGB gouraud shading and specular highlights
  - Bilinear, trilinear and anisotropic texture filtering
  - Color key and Alpha blended textures
  - Table and vertex fog
  - Texture compression
  - Full scene anti-aliasing
- 128-bit GUI accelerator
  - 3 operand ROPs
  - Hardware clipping
  - Color expansion
  - Transparent and stretch BitBLT
- AGP 2.0 bus master
  - DMA bus mastering for minimum CPU load
  - AGP 1x, 2x and 4x with SBA for host based textures
  - 3.3V PCI support
- Digital Video Output
  - 12-bit Multiplexed digital interface
  - Glueless connection to standard LCD interface devices and digital TV encoders
  - 24-bit LCD modes up to1280x1024 60Hz

- Video playback & MPEG2 decode acceleration
  - Motion compensation
  - 4:2:0 Overlay support
  - Sub picture blending
  - X, Y interpolated scaling
  - Color Keying
- SGRAM/SDRAM 128-bit interface
  - Single memory for frame buffer, video and texture memory
  - 2.0 GB/s bandwidth
  - 16 to 64 MBytes support
- Video port
  - Video port for video capture, TV Tuner, videoconferencing
  - VBI data capture for Intercast, Closed Caption and Teletext
- Integrated 270MHz palette DAC and clock synthesizer
  - 32x32 hardware cursor
  - 1920x1280 true color at 75Hz refresh
- PC'99 compliant

DESCRIPTION

KYRO is an integrated 2D/3D accelerator which extends the leadership of the PowerVR™ family of chips. It is designed to provide the highest Direct3D performance along with excellent 2D performance and video playback and decode acceleration.

KYRO integrates a 3D engine, 2D engine, 24-bpp palette RAMDAC, clock generators, a video input bus and digital interface into a 400-pin PBGA package.

SUPPORT

■ BIOS Support
- ● Fully IBM VGA compatible BIOS
- ● VBE v3.0 support
- ● DPMS and DDC2Bi
- ● OEM Configuration

■ Utilities
- ● Manufacturing test software
- ● Smart Tools
- ● Install

LOCALIZATION

● English	● Japanese
● French	● German
● Italian	● Spanish
● Traditional Chinese	● Simplified Chinese
● Korean	● Brazilian

ORDERING INFORMATION

To order sample trays or production quantities please contact your local ST Sales office.

Salestype

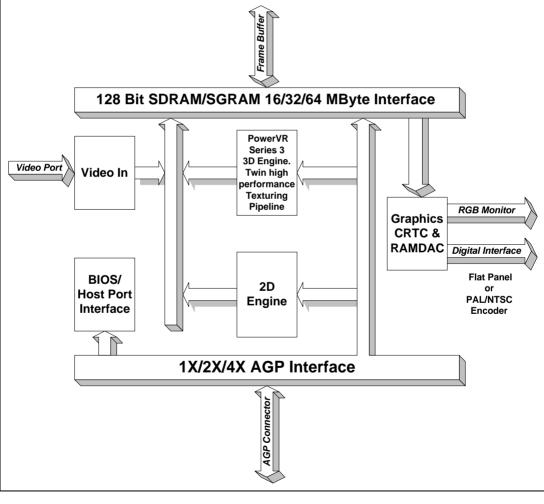|	
STG4000A1S/TR	Tape and Reels
STG4000A1S	Trays

SOFTWARE DRIVER SUPPORT

	Win 95/ DX7	Win 98/ DX7	NT4.0 (SP3)/ DX3	Win2000/ DX7	DOS
Display Driver	Y	Y	Y	Y	Y
DirectDraw HAL (inc. VPE)	Y (no VPE)	Y	Y	Y	
Direct3D HAL	Y	Y		Y	
OpenGL ICD	Y	Y	Y	Y	
Video Capture /WDM		Y		Y	
DVD Playback Support	Y	Y		Y	

1 Functional Description

1.1 General

KYRO is a single chip multimedia display device which integrates 2D and 3D accelerators with separate palette DAC and clock synthesizers for graphics output and includes a digital interface for connection to a TV Encoder or LCD interface device.

The KYRO includes glueless interfaces to AGP, SDRAM/SGRAM and video port.

1.2   Host Interface

The KYRO host interface is a glueless AGP v2.0 interface which acts as a bus master for 2D and 3D parameters as well as host based textures and video capture.

The AGP interface supports Memory Read, Memory Write, IORead, IOWrite, Memory Read Line and Memory Read Multiple PCI commands.

The AGP interface is a full 1x, 2x and 4x with side band addressing implementation supporting a peak bandwidth of 1GB/s. The read queue buffer supports 32 outstanding requests.

PCI power management device states of D0, D1, D2, $D3_{HOT}$ and $D3_{COLD}$ are supported allowing ACPI compliant system design.

Sub System Device and Vendor IDs are also supported in the PCI configuration space.

1.3   Memory Interface

KYRO is designed with a 128-bit SDRAM / SGRAM memory interface with a peak bandwidth of 2.0GB/s. On-chip caches and memory controller ensures that bandwidth is shared efficiently between the 2D, 3D and display functions.

The following memory configurations are supported:

Memory Type	Number of devices	Memory
16 Mbit SDRAM (x16)	8	16 MB
32 Mbit SGRAM (x32)	4	16 MB
32 Mbit SGRAM (x32)	8	32 MB
64 Mbit SDRAM (x32)	4	32 MB
64 Mbit SDRAM (x32)	8	64 MB
64 Mbit SDRAM (x16)	8	64 MB

1.4   2D Graphics Engine

KYRO incorporates a powerful 2D graphics accelerator which accelerates all three operand ROP BitBLTs and Transparent BLTs. The engine has been optimized to ensure there is no penalty for operating in 24bpp packed pixel modes. Other 2D operations supported in hardware include clipping, mono to color expansion, points and lines.

The engine bus masters both it's commands and parameters from either framebuffer or host which allows the CPU to do the minimum amount of work, increasing system throughput and supporting the use of Write Combining.

1.5   3D Graphics Engine

KYRO uses the PowerVR Series 3 3D core to provide the huge performance and advanced features required by tomorrow's 3D applications. The engine uses twin high performance texturing pipelines.

The 3D engine is a display list renderer which takes a whole scene of data to be rendered, partitions the data into screen tiles, performs hidden surface removal (without the need of an external Z-buffer) and performs deferred texturing on the resultant visible pixels.

Performance is ensured by the inclusion of complete hardware set-up of both triangle and texturing/shading parameters, the scene parameters being stored in host memory and bus mastered for maximum performance.

The chip supports Z-buffer-less hidden surface removal, RGB gouraud shading, perspective correct texture mapping, alpha blending and advanced texture filtering including bilinear, trilinear and anisotropic filtering as well as full scene anti-aliasing

1.6   Graphics Output

The graphics pixel pipeline incorporates color space conversion, overlay support, scaling and loadable LUT usable in all color depths to enable color management. DPMS and DDC2Bi are also supported.

1.7   Digital Port

Support for TV or LCD output in KYRO is provided by a 12-bit multiplexed RGB Port.   This can be connected to an external digital TV encoders including the Conexant Bt868/9 or Chrontel CH7003/4, or to a digital flat panel transmitter using the Silicon Image PanelLink Sil154. The port allows operation up to 1280x1024 60Hz, and supports both 18bpp and 24bpp modes.

The digital port can act in either master or slave mode. In master mode, the chip generates DAC clock, HSYNC, and VSYNC and in slave mode the production of pixels is synchronized to an externally generated DAC clock, HSYNC, and VSYNC.

Data is multiplexed onto the 12-bit port DVA_D[11:0] in the order shown below:

Pin	Normal Mode		Bt868/9 Modes	
	Rising Edge	Falling Edge	Rising Edge	Falling Edge
DVA_D11	G3	R7	G4	R7
DVA_D10	G2	R6	G3	R6
DVA_D9	G1	R5	G2	R5
DVA_D8	G0	R4	B7	R4
DVA_D7	B7	R3	B6	R3
DVA_D6	B6	R2	B5	G7
DVA_D5	B5	R1	B4	G6
DVA_D4	B4	R0	B3	G5
DVA_D3	B3	G7	G0	R2
DVA_D2	B2	G6	B2	R1
DVA_D1	B1	G5	B1	R0
DVA_D0	B0	G4	B0	G1

1.8   Video Port

The video interface allows capture of video data, including support for cropping, VBI capture, bus mastered data capture and image decimation.

1.9   BIOS

The BIOS interface is shared with the Frame Buffer Memory pins.

2 Mode Support

2.1 Supported Modes

The KYRO supports the following three display modes:

Display Modes	Connected Devices		
	CRT Monitor	**Digital Flat Panel**	**TV**
1	All Graphics Resolutions	Not Connected	Not Connected
2	Same as DFP	Maximum of 1280x1024 at 60Hz	Not Connected
3	Same as TV	Not Connected	PAL/NTSC Resolutions Only

2.2 Graphics Resolutions

KYRO supports a fully programmable PLL to allow a full range of resolutions and refresh rates to be supported:

Resolution	Colors	Refresh
1920x1440	up to 16.7 million	up to 60Hz
1920x1280	up to 16.7 million	up to 75Hz
1600x1200	up to 16.7 million	up to 85Hz
1280x1024	up to 16.7 million	up to 120Hz
1152x864	up to 16.7 million	up to 120Hz
1024x768	up to 16.7 million	up to 120Hz
800x600	up to 16.7 million	up to 120Hz
640x480	up to 16.7 million	up to 120Hz
VGA Modes 0,1,2,3,4,5,6,7,0Dh, 0Eh, 0Fh, 10h, 11h, 12h, 13h		

2.3   Digital Flat Panel Mode

The digital port may be programmed at refresh rates to match the requirements of the attached LCD device to a maximum of 1280x1024 at 60Hz (normal blanking). Lower resolutions will be centered in the screen.

2.4   TV Mode

All PAL/NTSC TV formats are supported. When connected to TV, the Digital Flat Panel cannot be used. However the CRT Monitor can simultaneously display the same resolution (mirror) as the TV Mode.

3 Mechanical/Package Specifications

3.1 Thermal Specification

- Thermal resistance: ΘJ/A = 15°C/W

3.2 Material Data

Standard BOM for BGA27 sq malta.

BT resin	IBIDEN
Glue	ablebond 8390
Resin	Nitto HC100HF
Balls	Sn/Pb, 30 mils
Wire	gold, 1.2 mils

3.2.1 Package Dimensions

Dimensions						
	Drawing (mm)			**Drawing (inch)**		
REF	TYP	MIN	MAX	TYP	MIN	MAX
A		2.13	2.6		0.08	0.1
A1		0.5	0.7		0.02	0.03
A2		1.63	1.9		0.06	0.07
b		0.6	0.9		0.02	0.04
D	27	26.82	27.18	1.06	1.06	1.07
D1	24.13 BASIC			0.951 BASIC		
D2		23.9	24.1		0.94	0.95
e	1.27 BASIC			0.050 BASIC		
E	27	26.82	27.18	1.063	1.06	1.07
E1	24.13 BASIC			0.951 BASIC		
E2		23.9	24.1		0.94	0.95

Controlling Dimension: Millimeters, Drawing BGA27x27 finished 14090202-004.
Reference Document: JEDEC M0151.

400 Pin Plastic Ball Grid Array Package dimension reference.

POA FOR PBGA 400 27X27X2.6 / F20 1.27

400 F20

The ST logo is a registered trademark of STMicroelectronics

KYRO is a trademark of STMicroelectronics

PowerVR is a trademark of Imagination Technologies Group plc

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

http://www.st.com