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- First preliminary release

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- Remove absolute rating of OVDD in chapter 6.1
- Modify Absolute Maximum Ratings in page 58

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- Add Theta Jc in chapter 6.1
- Modify page 25

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- Update Table 6.5-2 DDR SDRAM Timing Table in page 62

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1 Volari™ Z9M Series GPU

1.1 Introduction

Volari™ Z9M GPU is the extreme programmable GPU of the XGI™ 2D GPU family that comes in a 297-ball, 23mmx23mm BGA package (lead-free). The Volari™ Z9M integrates a PCI 2.2 controller and a 64-bit 2D graphics engine. It integrates a 16-bit DDR memory. The Z9M also incorporates a configurable 3.3V/2.5V DVO digital interface to support a third party LVDS/TMDS transmitter. It can achieve high 2D performance with a memory interface supporting a bandwidth of up to 0.33 GB/s (DDR @166MHz).

1.2 Volari™ Z9M GPU Features

PCI Bus Interface

- Supports 32-bit PCI bus standard Revision 2.2 compliant
- Supports 33Mhz PCI operation
- Built-in write-once subsystem and subsystem-vendor ID configuration register for on board VGA or power on auto subsystem and subsystem-vendor ID fetching from BIOS for add-on VGA card
- Built-in PCI power management configuration register for D0, D1, D2 and D3 modes
- Supports 66 MHz zero wait-state memory mapped I/O burst write
- Built-in 66 MHz zero wait-state PCI post-write buffer with byte merge to enhance frame buffer write performance
- Built-in read cache to enhance frame buffer read performance
- Supports one-wait burst read cycle when buffer hits
- Supports automatic disconnect or retry after waiting for 16 PCI clocks when read cache misses or post write buffer is full
- Supports 4-wait signal I/O read/write cycle
- Supports full 32-bit memory frame buffer address decoding for 128MB size
- Supports full 32-bit re-locatable VGA I/O address decoding for 128 I/O ports
- Supports full 32-bit memory mapped I/O address decoding for 128KB size
- Supports full 32-bit ROM address decoding for 32KB and 64KB size
- Supports SPI interface for VGA BIOS
- Supports medium DEVSEL decoding timing
- Supports RAMDAC snoop
- Supports IMAC compatible PCI data format

High Performance 2D Accelerator

- Built-in hardware command queue
- Built-in Direct Draw Accelerator
- Built-in GDI 2000 Accelerator
- Built-in an 1T pipelined 64-bit BITBLT graphics engine with the following functions:
  - 256 raster operations
  - Rectangle fill
  - Color expansion
  - Enhanced color expansion
  - Line-drawing with styled pattern
  - Built-in bytes pattern registers
  - Built-in 8x8 mask registers
  - Rectangle clipping
  - Transparent BitBlt with source and destination keys
  - Source data in command queue Bitblt
- Supports memory-mapped, zero wait-state, burst engine write
- Built-in 64x64x2 bit-mapped mono hardware cursor
- Maximum 256MB frame buffer with linear addressing
- Built-in source read-buffer to minimize engine wait-state
- Built-in destination read-buffer to minimize engine wait-state

High Efficient BroadBahn™ Memory Architecture

- Integrate DDR SDRAM memory
- Integrate 8MB memory configurations
- Supports internal 64-bit display memory path

High Performance Flat Panel Display Interface

- Supports graphics mode up to 1600x1200@60NI 16M colors
- Built-in power sequencing control outputs
- Supports 12-bit, 18-bit, and dual 12-bit digital interface
- Digital interface to an external LVDS/TMDS transmitter
- Digital interface (DVO) to KVM for remote panel interface
- Configurable 3.3V, 2.5V Digital Interface for Single 12bit / Dual 12bit
- Configurable 3.3V Digital Interface for Single 18bit

High Integration

- Built-in CRT FIFO to support ultra high resolution graphics modes and reduce CPU wait-state
- Built-in programmable 24-bit true-color RAMDAC with 230 MHz pixel clock
  - Built-in reference voltage generator and monitor sensing circuit
  - Supports downloadable 24 bits RAMDAC for gamma correction in high color and true color modes
  - Supports programmable 4 levels DAC current ratio
  - Supports programmable pedestal level
- Two built-in clock generators
  - Integrates PLL loop filter for CRT and DRAM
- Built-in 14.318 MHz reference clock oscillator circuit
- Built-in SPI flash ROM programming interface

Resolution, Color & Frame Rate

- Supports 230 MHz pixel clock
- Supports VESA standard super high resolution graphics modes
- Supports virtual screen up to 4096x4096

Power Management

- Supports power management for VGA monitor
- Supports direct I/O command to force graphics controller into standby/suspend/off state
- Power down internal SRAM in direct color mode
- Supports PCI power management configuration registers for supporting ACPI power down controller
- Power down all internal macro cells such as SRAM, DAC, clock generator, DLL in power savings mode
- Supports auto clock throttling for 2D engine

Multimedia Application

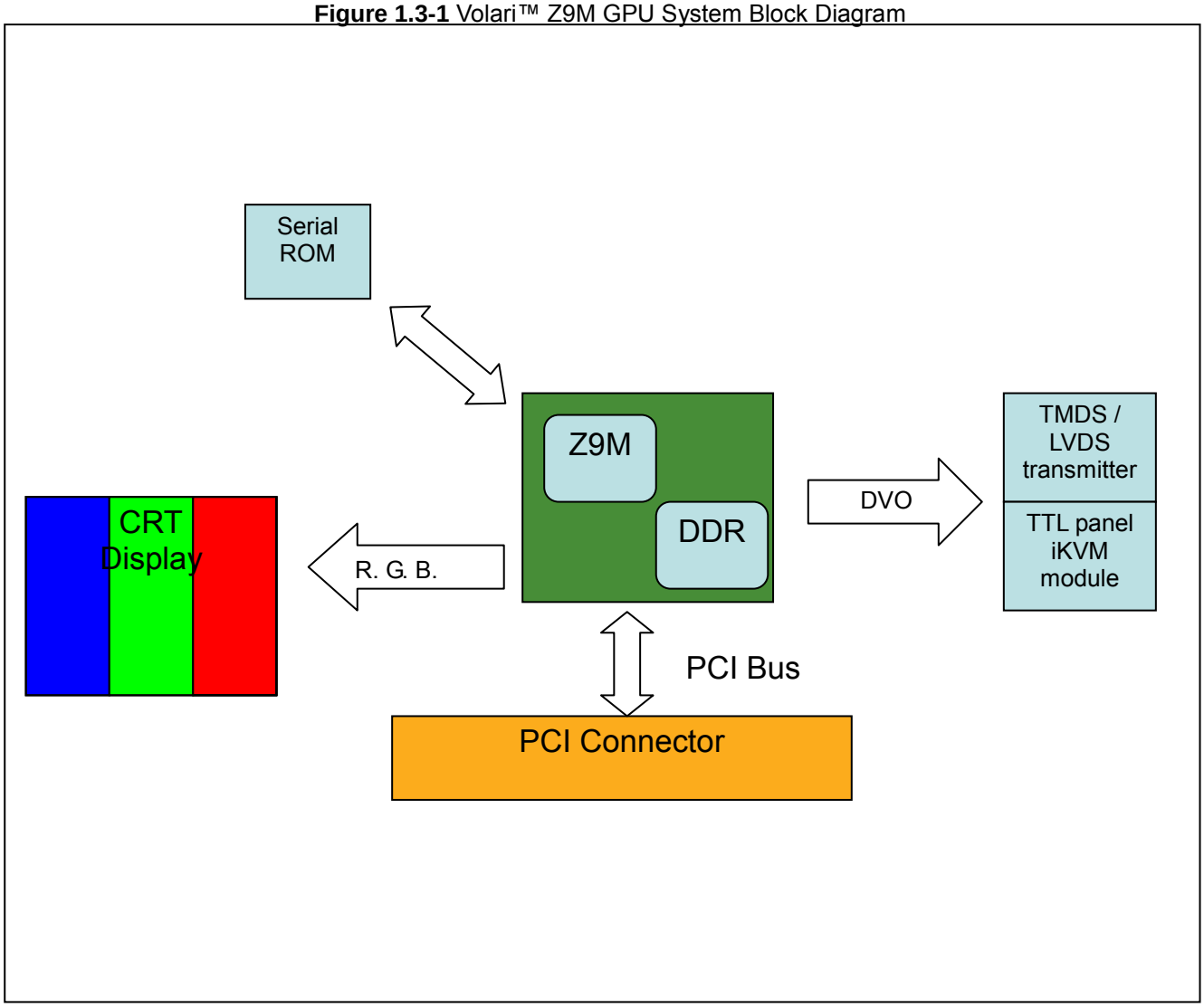
- Supports DDC1, DDC2B and DDC 3.0 specifications
- Supports RAMDAC snoop for multimedia applications

Miscellaneous

- Supports 32K/64K Bytes ROM decoding
- Supports 20MHz SPI ROM interface
- Supports Signature Analysis for automatic testing
- Supports full scan testing
- Supports BIST for internal memory testing
- 297-balls, 23mm x 23mm BGA package, ball pitch 0.8mm
- Halogen-free package

1.3 Single Volari™ Z9M GPU Block Diagram

Figure 1.3-1 Volari™ Z9M GPU System Block Diagram



2 Volari™ Z9M GPU Description

2.1 2D Graphics Engine

The Volari™ Z9M graphics controller incorporates a powerful 64-bit graphics engine to enhance the performance of 2D operations. The capabilities of the graphics engine include, but are not limited to BitBlt, Color Expansion, Enhanced Color Expansion, Line Drawing, Transparent BitBlt, and Rectangle Fill.

For all enhanced 256 color (8 bpp), 32k & 64k hi-color (16 bpp), and 16M true color (32 bpp) graphics modes. The 2D engine supports the following functions:

- 256 raster operations
- Rectangle fill
- Color expansion
- Enhanced Color expansion
- Line drawing with styled pattern
- Built-in bytes pattern registers
- Built-in 8x8 mask registers
- Rectangle Clipping
- Transparent BitBlt with source and destination keys
- Source data in command queue Bitblt

The engine also support new GDI 2000 functions

2.2 PCI Bus Interface

The Volari™ Z9M GPU is a native PCI device which connects directly to the PCI bus onboard the motherboard of via an add-in card. The Z9M decodes 32-bit addresses and configures the device based on the applicable control lines between the target and initiator. The GPU can execute both I/O and memory access instructions as a 32-bit device.

2.3 BroadBahn™ Memory Architecture

The internal memory controller of the Z9M generates the timing parameters for display memory. It supports the DDR SDRAM timing specifications

The Z9M integrates the 4Mx16 of DDR SDRAM memory.

The frequency of the Volari™ Z9M memory controller interface is synchronous with the 2D engine at 166MHz with the I/O interface at 166MHz. It can support up to a 0.33GB/s bandwidth, with a 16-bit DDR SDRAM integrated. The DRAM capacity is 8MB. The DRAM controller has a pipeline design to increase the feed-through of data to and from the frame buffer. The Z9M also has an optimized DRAM arbiter to perform ping-pong bank operation to reduce DRAM pre-charge time for achieving the maximum utilization rate of the memory.

2.4 Other Function Blocks

CRT Controller

The CRT controller generates the HSYNC and VSYNC synchronization signals required for the correct monitor interface, as well as blanking signals required by the attribute controller.

CRT FIFO

The CRT FIFO allows the display memory controller to access the display memory (frame buffer) for screen refreshes at the memory controller speed, rather than at the slower screen refresh rate. At the higher memory controller speed, the data in the CRT FIFO exceeds the amount of data needed at the screen refresh rate, thus giving the user a more visually appealing interface as more data is available for each frame. The Z9M also provides hardware auto threshold detection to calculate and ensure optimal memory utilization rate takes place. When these thresholds are auto detected, the engine wait-time is reduced which improves overall performance.

DDC Controller

The DDC controller provides two channels to communicate with a DDC monitor. The first channel is the DDC clock which is a bi-directional clock signal that provides the DDC clock interface. The second channel is the bi-directional DDC data signal which transfers data from / to the monitor. With DDC support, the VGA BIOS can determine the capability of the connected monitor (ex. Maximum resolution and refresh rate) and configure the Z9M parameters to support the correct monitor specifications for the best viewing

The DDC levels of support in the Z9M are level 1, level 2B, and level 3.0.

Graphics Controller

The graphics controller will perform text manipulation, block transfers, data rotation, color mapping, and other 2D operations.

Video RAMDAC

The RAMDAC contains the color palette and 24-bit true color DAC. The maximum frequency of the RGB DAC is 230 MHz. The maximum resolution the DAC supports is 1600x1200@60NI video mode (true color with a 32-bit DRAM interface or high color with 16 bit-DRAM interface).

The color palette, with 256 24-bit entries, converts a color code that specifies the color of a pixel into three 8-bit values, one each for red, green and blue.

The 24-bit true color DAC is designed for direct color graphics mode. It converts each digital color value to three analog voltages for red, green, and blue.

Digital Output Interface

The Z9M also incorporates a configurable 3.3V/2.5V (DVO) digital interface to support a third party LVDS/TMDS transmitter. The data formats supported are 12-bit (3.3V/2.5V), 18-bit (RGB 666; 3.3V), and dual 12-bit (RGB 888; 3.3V/2.5V). This option allows more display flexibility to allow the following options:

- CRT
- CRT + DVO (TTL)
- CRT + External TMDS/LVDS
- DVO (TTL)

Read-ahead Cache

The incorporation of a read-ahead cache will enable the display memory read time to be reduced, which will enhance the performance of the graphics accelerator. The read-ahead feature will allow more read transaction data (larger blocks) to be sent to the graphics processor as a method of decreasing the read latency. The larger block size increases the chance that another request can utilize the existing data present in the cache that was transferred during a preceding read request.

Post Write Buffer

The post write buffer contains a buffer of CPU write accesses to display memory that have not been executed due to memory arbitration. With the addition of the post-write buffer, the Volari™ Z9M will release the CPU as soon as it records the address and data of the write requests. When the display memory is available for the CPU write requests stored in the buffer, the data will then be written into display memory without CPU intervention. This frees up CPU time and system performance increases.

Internal Double-Clock Synthesizer

The Volari™ Z9M has three built-in clock synthesizers to generate the memory clock (MCLK), engine clock (ECLK), and data clock (DCLK). These clock synthesizers can generate several variable frequencies allowing the flexibility for selecting the range of working frequencies that the Z9M can operate under.

The three clocks (MCLK, ECLK and DCLK) are synthesized from a single external 14.318 MHz reference source. Based on the characteristic equation of the clock synthesizer, the MCLK can be set at the maximum frequency that the display memory is set to, to take advantage of the peak memory bandwidth to improve graphics performance. The ECLK frequency can be dynamically reduced (ECLK frequency scaling) during idle states to help reduce chip power consumption.

The following block diagram is for the Z9M clock synthesizer.

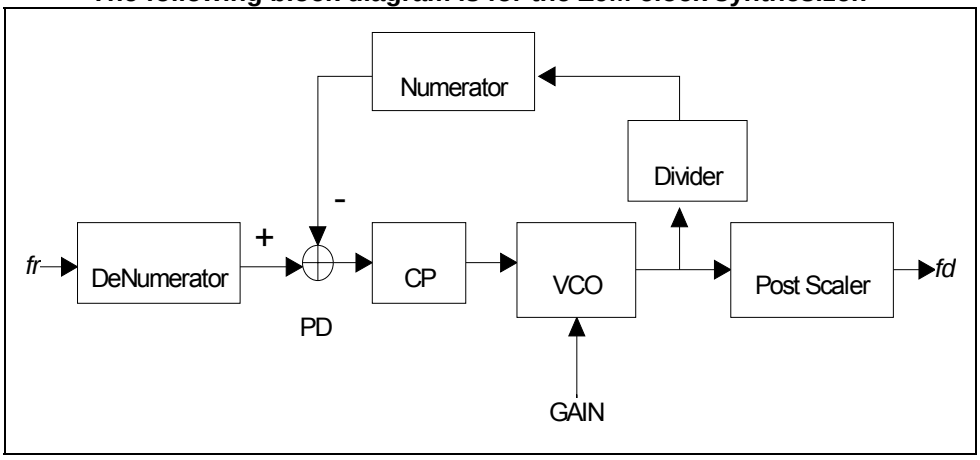


Figure 2.4 -1 Block Diagram of Clock Synthesizer

In the diagram above, we have the following items:

- PD is the phase detection
- CP is the charge pump
- VCO is the voltage-controlled oscillator
- fr is the reference input frequency
- fd is the output frequency

The operation of the clock synthesizer based on the stable output frequency is as follows:

fd=fr x ((Numerator+1))/(DeNumerator+1)) x (Divider/Post Scalar)

With this formula, we can select ideal values for the numerator, denumerator, divider, and post scalar to obtain the desired output frequency.

VGA Compatibility

The Volari™ Z9M is fully compatible with all standard IBM VGA modes and EGA, CGA, MDA and Hercules modes.

Process and Supply Voltages

Volari™ Z9M is manufactured by a low-power 0.18um CMOS process. The Z9M is a 5V tolerant part that does not require a 5 volts VDD power pin. The supply voltages for the various interfaces are as follows:

- Internal logic: 1.8V ± 5%
- DRAM I/O: 2.5V ± 5%
- PCI I/O: 3.3V ± 5%, 5V ± 5%
- Digital Out: 2.5V ± 5%, or 3.3V ± 5%

Software Support

In order to fully utilize and support the Volari™ Z9M GPU hardware features, XGI™ Technology has developed a high-performance VESA™ extension compliant BIOS.

Extended graphics and text modes are supported by software application drivers which are developed in-house. In addition, most of the operating systems (OS) are currently supported such like Windows Server, Linux, Unix…etc. XGI could provide the basic OS support list and support more by customer request.

3 Mode Tables

3.1 Standard VGA Modes (CRT, DVO)

MODE	TYPE	DISPLAY SIZE	COLORS SHADES	ALPHA FORMAT	BUFFER START	BOX SIZE	MAX. PAGES	CRT/DVO/ Mirror
0	A/N	320x200	16	40x25	B800	8x8	8	CRT/DVO/ Mirror
0*	A/N	320x350	16	40x25	B800	8x14	8	CRT/DVO/ Mirror
0+	A/N	360x400	16	40x25	B800	9x16	8	CRT/DVO/ Mirror
1	A/N	320x200	16	40x25	B800	8x8	8	CRT/DVO/ Mirror
1*	A/N	320x350	16	40x25	B800	8x14	8	CRT/DVO/ Mirror
1+	A/N	360x400	16	40x25	B800	9x16	8	CRT/DVO/ Mirror
2	A/N	640x200	16	80x25	B800	8x8	8	CRT/DVO/ Mirror
2*	A/N	640x350	16	80x25	B800	8x14	8	CRT/DVO/ Mirror
2+	A/N	720x400	16	80x25	B800	9x16	8	CRT/DVO/ Mirror
3	A/N	640x200	16	80x25	B800	8x8	8	CRT/DVO/ Mirror
3*	A/N	640x350	16	80x25	B800	8x14	8	CRT/DVO/ Mirror
3+	A/N	720x400	16	80x25	B800	9x16	8	CRT/DVO/ Mirror
4	APA	320x200	4	40x25	B800	8x8	1	CRT/DVO/ Mirror
5	APA	320x200	4	40x25	B800	8x8	1	CRT/DVO/ Mirror
6	APA	640x200	2	80x25	B800	8x8	1	CRT/DVO/ Mirror
7	A/N	720x350	4	80x25	*B000*	9x14	8	CRT/DVO/ Mirror
7+	A/N	720x400	4	80x25	*B000*	9x16	8	CRT/DVO/ Mirror
0D	APA	320x200	16	40x25	A000	8x8	8	CRT/DVO/ Mirror
0E	APA	640x200	16	80x25	A000	8x8	4	CRT/DVO/ Mirror
0F	APA	640x350	2	80x25	*B000*	8x14	2	CRT/DVO/ Mirror
10	APA	640x350	16	80x25	A000	8x14	2	CRT/DVO/ Mirror
11	APA	640x480	2	80x30	A000	8x16	1	CRT/DVO/ Mirror
12	APA	640x480	16	80x30	A000	8x16	1	CRT/DVO/ Mirror
13	APA	320x200	256	40x25	A000	8x8	1	CRT/DVO/ Mirror

Note:1. A/N: Alpha/Numeric

2. APA: All Point Addressable (Graphics)

MODE	DISPLAY SIZE	COLORS SHADES	FRAME RATE.	H-SYNC.	VIDEO FREQ.	CRT/DVO/ Mirror
0	320x200	16	70	31.5 K	25.1 M	CRT/DVO/Mirror
0*	320x350	16	70	31.5 K	25.1 M	CRT/DVO/Mirror
0+	360x400	16	70	31.5 K	28.3 M	CRT/DVO/Mirror
1	320x200	16	70	31.5 K	25.1 M	CRT/DVO/Mirror
1*	320x350	16	70	31.5 K	25.1 M	CRT/DVO/Mirror
1+	360x400	16	70	31.5 K	28.3 M	CRT/DVO/Mirror
2	640x200	16	70	31.5 K	25.1 M	CRT/DVO/Mirror
2*	640x350	16	70	31.5 K	25.1 M	CRT/DVO/Mirror
2+	720x400	16	70	31.5 K	28.3 M	CRT/DVO/Mirror
3	640x200	16	70	31.5 K	25.1 M	CRT/DVO/Mirror
3*	640x350	16	70	31.5 K	25.1 M	CRT/DVO/Mirror
3+	720x400	16	70	31.5 K	28.3 M	CRT/DVO/Mirror
4	320x200	4	70	31.5 K	25.1 M	CRT/DVO/Mirror
5	320x200	4	70	31.5 K	25.1 M	CRT/DVO/Mirror
6	640x200	2	70	31.5 K	25.1 M	CRT/DVO/Mirror
7*	720x350	4	70	31.5 K	28.3 M	CRT/DVO/Mirror
7+	720x400	4	70	31.5 K	28.3 M	CRT/DVO/Mirror
0D	320x200	16	70	31.5 K	25.1 M	CRT/DVO/Mirror
0E	640x200	16	70	31.5 K	25.1 M	CRT/DVO/Mirror
0F	640x350	2	70	31.5 K	25.1 M	CRT/DVO/Mirror
10	640x350	16	70	31.5 K	25.1 M	CRT/DVO/Mirror
11	640x480	2	60	31.5 K	25.1 M	CRT/DVO/Mirror
12	640x480	16	60	31.5 K	25.1 M	CRT/DVO/Mirror
13	320x200	256	70	31.5 K	25.1 M	CRT/DVO/Mirror

Note:i – interlaced mode

n – Non-interlaced mode

3.2 Low Resolution Modes (CRT, DVO)

MODE	TYPE	DISPLAY SIZE	COLORS SHADES	ALPHA FORMAT	BUFFER START	BOX SIZE	MAX. PAGES	CRT/DVO/ Mirror
50	APA	320x240	256	40x30	A000	8x8	1	CRT/DVO/Mirror
53	APA	320x240	32K	40x30	A000	8x8	1	CRT/DVO/Mirror
56	APA	320x240	64K	40x30	A000	8x8	1	CRT/DVO/Mirror
51	APA	400x300	256	50x38	A000	8x8	1	CRT/DVO/Mirror
54	APA	400x300	32K	50x38	A000	8x8	1	CRT/DVO/Mirror
57	APA	400x300	64K	50x38	A000	8x8	1	CRT/DVO/Mirror
52	APA	512x384	256	64x48	A000	8x8	1	CRT/DVO/Mirror
55	APA	512x384	32K	64x48	A000	8x8	1	CRT/DVO/Mirror
58	APA	512x384	64K	64x48	A000	8x8	1	CRT/DVO/Mirror

Note:1. A/N: Alpha/Numeric

2. APA: All Point Addressable (Graphics)

3.3 Supported Enhanced CRT/DVO Mode and Memory Configuration Table (MCLK=166MHz)

MODE	DCLK (HZ)	PAGE SIZE (BYTE)	BAND WIDTH (BYTE/S)	DRAM REQUIREMENT (BYTE)	DDRII BUS WIDTH REQUIRED	CRT/DVO/ MIRROR
640x480x8@60NI	25.1M	330K	25M	4M	4 bit	CRT/DVO/ Mirror
640x480x16@60NI	25.1M	600K	50M	4M	4 bit	CRT/DVO/ Mirror
640x480x32@60NI	25.1M	1.2M	100M	4M	4 bit	CRT/DVO/ Mirror
640x480x8@72NI	31.5M	330K	31.5M	4M	4 bit	CRT/DVO/ Mirror
640x480x16@72NI	31.5M	600K	63M	4M	4 bit	CRT/DVO/ Mirror
640x480x32@72NI	31.5M	1.2M	126M	4M	4 bit	CRT/DVO/ Mirror
640x480x8@75NI	31.5M	330K	31.5M	4M	4 bit	CRT/DVO/ Mirror
640x480x16@75NI	31.5M	600K	63M	4M	4 bit	CRT/DVO/ Mirror
640x480x32@75NI	31.5M	1.2M	126M	4M	4 bit	CRT/DVO/ Mirror
640x480x8@85NI	36M	330K	36M	4M	4 bit	CRT/DVO/ Mirror
640x480x16@85NI	36M	600K	72M	4M	4 bit	CRT/DVO/ Mirror
640x480x32@85NI	36M	1.2M	144M	4M	4 bit	CRT/DVO/ Mirror
800x600x8@60NI	40M	468K	40M	4M	4 bit	CRT/DVO/ Mirror
800x600x16@60NI	40M	938K	80M	4M	4 bit	CRT/DVO/ Mirror
800x600x32@60NI	40M	1.857M	160M	4M	4 bit	CRT/DVO/ Mirror
800x600x8@72NI	50M	468K	50M	4M	4 bit	CRT/DVO/ Mirror
800x600x16@72NI	50M	938K	100M	4M	4 bit	CRT/DVO/ Mirror
800x600x32@72NI	50M	1.857M	200M	4M	4 bit	CRT/DVO/ Mirror
800x600x8@75NI	50M	468K	50M	4M	4 bit	CRT/DVO/ Mirror
800x600x16@75NI	50M	938K	100M	4M	4 bit	CRT/DVO/ Mirror
800x600x32@75NI	50M	1.857M	200M	4M	4 bit	CRT/DVO/ Mirror
800x600x8@85NI	56.3M	468K	56.3M	4M	4 bit	CRT/DVO/ Mirror
800x600x16@85NI	56.3M	938K	112.6M	4M	4 bit	CRT/DVO/ Mirror
800x600x32@85NI	56.3M	1.857M	225.2M	4M	4 bit	CRT/DVO/ Mirror
1024x768x8@60NI	65M	0.768M	65M	4M	4 bit	CRT/DVO/ Mirror
1024x768x16@60NI	65M	1.536M	130M	4M	4 bit	CRT/DVO/ Mirror
1024x768x32@60NI	65M	3.072M	260M	4M	4 bit	CRT/DVO/ Mirror
1024x768x8@75NI	78.75M	0.768M	78.75M	4M	4 bit	CRT/DVO/ Mirror
1024x768x16@75NI	78.75M	1.536M	157.5M	4M	4 bit	CRT/DVO/ Mirror
1024x768x32@75NI	78.75M	3.072M	330M	4M	8 bit	CRT/DVO/ Mirror
1024x768x8@85NI	94.5M	0.768M	94.5M	4M	4 bit	CRT/DVO/ Mirror

1024x768x16@85NI	94.5M	1.536M	189M	4M	4 bit	CRT/DVO/ Mirror
1024x768x32@85NI	94.5M	3.072M	398M	4M	8 bit	CRT/DVO/ Mirror
1280x1024x8@60NI	108M	1.28M	110M	4M	4 bit	CRT/DVO/ Mirror
1280x1024x16@60NI	108M	2.56M	220M	4M	4 bit	CRT/DVO/ Mirror
1280x1024x32@60NI	108M	5.12M	440M	8M	8 bit	CRT/DVO/ Mirror
1280x1024x8@75NI	135M	1.28M	135M	4M	4 bit	CRT/DVO/ Mirror
1280x1024x16@75NI	135M	2.56M	270M	4M	8 bit	CRT/DVO/ Mirror
1280x1024x32@75NI	135M	5.12M	540M	8M	16 bit	CRT/DVO/ Mirror
1280x1024x8@85NI	157.5M	1.28M	157.5M	4M	4 bit	CRT/DVO/ Mirror
1280x1024x16@85NI	157.5M	2.56M	330M	4M	8 bit	CRT/DVO/ Mirror
1280x1024x32@85NI	157.5M	5.12M	630M	8M	16 bit	CRT/DVO/ Mirror
1600x1200x8@60NI	162M	1.875M	162M	4M	4 bit	CRT/DVO/ Mirror
1600x1200x16@60NI	162M	3.75M	324M	4M	8 bit	CRT/DVO/ Mirror

The table could be extended.

4 Volari™ Z9M Ball Distribution and Definition

PCI Interface:

Ball location	Signal name	Output Current Drive (IoL)	Output Current Drive (IoH)	Input Leakage (IiL)	Input Leakage (IiH)	Package Cap.	Type	Description
B2	RSTN	N/A	N/A	-10nA	20nA	6.83pF	I	PCI Reset is used to bring PCI-specific registers, sequencer, and signals to a consistent state. This pin has 5V tolerance.
A1	CLK	N/A	N/A	-4nA	11nA	N/A	I	PCI Bus Clock provides timing for all transactions on PCI bus. This pin has 5V tolerance. The signal should be away from other sensitive signals to avoid crosstalk.
A2	INTAN	75mA	-61mA	N/A	N/A	6.83pF	O	PCI Interrupt indicates the interrupt signal generated by XG21 GPU. This pin has 5V tolerance.
C1, B1, C2, D4, D2, E4, D1, F4, E1, G4, F2, F1, G2, H4, G1, H1, L1, M2, M4, M1, N4, N1, N2, P1, P2, R4, R2, R1, T2, T1, U1, V1	AD[31:0]	61mA	-69mA	-4nA	0.1uA	8.11pF	I/O	PCI Address/Data Bus is multiplexed on the same pins. The address phase is the clock cycle in which FRAMEN is asserted and the data phase is immediately after the address phase.
P4, L2, J2, E2	CBE0N CBE1N CBE2N CBE3N	61mA	-69mA	-4nA	0.1uA	8.11pF	I/O	PCI Command/Byte Enable Bus is multiplexed on the same pins. During the address phase of a transaction, C/BE define the bus command, and during the data phase C/BE are used as Byte Enable.
L4	PAR	61mA	-69mA	N/A	N/A	8.11pF	I/O	PCI Parity Bit is even parity across AD[31..0] and CBE[3..0]N.
J4	FRAMEN	61mA	-69mA	-4nA	0.1uA	8.11pF	I/O	PCI Frame Cycle is driven by the current master to indicate the beginning and duration of an access.
K4	TRDYN	61mA	-69mA	-4nA	0.1uA	8.11pF	I/O	PCI Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
J1	IRDYN	61mA	-69mA	-4nA	0.1uA	8.11pF	I/O	PCI Initiator ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
K1	STOPN	61mA	-69mA	-4nA	0.1uA	8.11pF	I/O	PCI Stop indicates the current target is requesting the master to stop the current transaction.
K2	DEVSELN	61mA	-69mA	-4nA	0.1uA	8.11pF	I/O	PCI Device Select indicates whether any device on the bus has been selected.
H2	IDSEL	N/A	N/A	-4nA	0.1uA	8.11pF	I	PCI Initial Device Select is used during configuration transactions.

Memory Interface:

Ball location	Signal name	Output Current Drive (IoL)	Output Current Drive (IoH)	Input Leakage (IiL)	Input Leakage (IiH)	Package Cap.	Type	Description
AA16, AA15	SCLKA, SCLKAN	43mA	-44mA	N/A	N/A	4.67pF	O	Test mode output clock. Normal use, keep pin floating.
AA8	CSA	43mA	-44mA	N/A	N/A	4.67pF	O	Test mode output chip select. Normal use, keep pin floating.
Y2	WEA	43mA	-44mA	N/A	N/A	4.67pF	O	Test mode output write enable. Normal use, keep pin floating.
AA3	RASA	43mA	-44mA	N/A	N/A	4.67pF	O	Test mode output row address. Normal use, keep pin floating.
AA2	CASA	43mA	-44mA	N/A	N/A	4.67pF	O	Test mode output column address. Normal use, keep pin floating.
AA20	CKEA	43mA	-44mA	N/A	N/A	4.67pF	O	Clock Enable; Pull low with 4.7K resistor.
V19, Y1	DQMA[1:0]	43mA	-41mA	N/A	N/A	4.67pF	O	Test mode output data mask. Normal use, Keep pin floating
Y6, AA7, W17, AA19, Y20, AA21, Y21, Y8, W21, V21, V20, W20, AA17, Y18, AA18, W15	MAA[15:0]	43mA	-44mA	N/A	N/A	4.67pF	O	Test mode output memory address. Normal use, MAA[2:0] keep pin floating, MAA [13:3] pins are used for the hardware trapping setting. The hardware trapping settings need to be pulled high or low, and cannot be floating.
Y15, AA14, V6, V15, W16, V5, V16, Y14, AA4, AA5, Y7, AA6, Y5, Y3, W6, Y4	DQA[15:0]	43mA	-44mA	-6nA	0	4.67pF	I/O	Test mode in/out memory data bus. Normal use, Keep pin floating
G20, P20, Y19, V18, W7, AA1	DDRASTB [3:0], DDRASTB [1:0]N	44mA	-43mA	-8nA	2nA	4.67pF	I/O	Test mode output Data Strobe. Normal use, Keep pin floating
V9	MVREF	N/A	N/A	N/A	N/A	N/A	AI	Reference voltage of DDR I/O. Connect to 1/2 OVDDM
W19	DVREF	N/A	N/A	N/A	N/A	N/A	AI	Reference voltage of DDR I/O. Connect to 1/2 OVDDM
T21	MNRSET	N/A	N/A	-6nA	0	N/A	AI	DDR NMOS calibration reference resistor. Pull-up with a 120Ω resistor to OVDDM.
T20	MPRSET	N/A	N/A	-6nA	0	N/A	AI	DDR PMOS calibration reference resistor. Pull-down with a 120Ω resistor to ground.
N18	DDR3RSTN	43mA	-44mA	N/A	N/A	4.67pF	O	DDR3 reset. Keep pin floating.

Serial ROM (SPI) Interface:

Ball location	Signal name	Output Current Drive (IoL)	Output Current Drive (IoH)	Input Leakage (IiL)	Input Leakage (IiH)	Package Cap.	Type	Description
B13	SPICS	75mA	-61mA	N/A	N/A	6.83pF	O	SPI chip select.
A14	SPISI	75mA	-61mA	N/A	N/A	6.83pF	O	SPI data in.
A13	SPICK	75mA	-61mA	N/A	N/A	6.83pF	O	SPI clock.
B14	SPISO	N/A	N/A	-14nA		6.83pF	I	SPI data out.

VGA DAC Interface:

Ball location	Signal name	Output Current Drive (IoL)	Output Current Drive (IoH)	Input Leakage (IiL)	Input Leakage (IiH)	Package Cap.	Type	Description
A4	R	0uA (input code = 00h)	19191uA (input code = FFh)	N/A	N/A	N/A	A	Red video signal output.
A5	G	0uA (input code = 00h)	18895uA (input code = FFh)	N/A	N/A	N/A	A	Green video signal output.
A6	B	0uA (input code = 00h)	18724uA (input code = FFh)	N/A	N/A	N/A	A	Blue video signal output.
C11	RSET	N/A	N/A	N/A	N/A	N/A	A	Bias for DAC current source. Pull-down with a 120Ω resistor to GND.
D12	COMP	N/A	N/A	N/A	N/A	N/A	A	DAC compensation pin.
D11	VBWN	N/A	N/A	N/A	N/A	N/A	A	Voltage reference.
A16	HSYNC	147mA	-175mA	N/A	N/A	6.83pF	O	Horizontal sync. Place a 22Ω resistor in series.
A15	VSYNC	130mA	-148mA	N/A	N/A	6.83pF	O	Vertical sync. Place a 22Ω resistor in series.
C13	DDCDAT	76mA	-76mA		195nA	6.83pF	I/O	Display Data Channel Data line. Place a 100Ω resistor in series and pull-up to 5V.
D13	DDCCLK	76mA	-76mA		327nA	6.83pF	I/O	Display Data Channel clock line. Place a 100Ω resistor in series and pull-up to 5V.

Miscellaneous Signals:

Ball location	Signal name	Output Current Drive (IoL)	Output Current Drive (IoH)	Input Leakage (IiL)	Input Leakage (IiH)	Package Cap.	Type	Description
A20	REFOSCI	N/A	N/A	0	0	N/A	I	Reference clock 14.31818 MHz input. Place close to Z9M.
A21	REFOSCO	14mA	-9mA	N/A	N/A	N/A	O	Reference clock 14.31818 MHz output. Place close to Z9M.
A17	SPIN	N/A	N/A	-1nA	72nA	6.83pF	I	Spread spectrum reference clock 14.31818 MHz input. If not used, tie to GND.
A18	VBRCLK	44mA	-43mA	N/A	N/A	N/A	O	Provide reference clock 14.31818 MHz. Float the pin.
D15	PWRSTN	N/A	N/A	0	0	6.83pF	I	Power on reset of clock generator. Pull-up with a 100KΩ resistor to 3.3V.
C12	ENTEST	N/A	N/A	-381nA		6.83pF	I	Test enable. Tie to GND with a 1KΩ resistor.
D14	GPIOA	75mA	-61mA	-5nA	59nA	6.83pF	I/O	SCL for Digital RGB Interface. See Ch. 13 for details.
C14	GPIOB	75mA	-61mA	-5nA	59nA	6.83pF	I/O	SDA for Digital RGB interface. See Ch. 13 for details.
B21	GPIOC	75mA	-61mA	-5nA	59nA	6.83pF	I/O	General purpose in/out pin.
C21	GPIOD	75mA	-61mA	-5nA	59nA	6.83pF	I/O	General purpose in/out pin.
D20	GPIOE	75mA	-61mA	-5nA	59nA	6.83pF	I/O	General purpose in/out pin.
D21	GPIOF	75mA	-61mA	-5nA	59nA	6.83pF	I/O	General purpose in/out pin.
C15	GPIOG	75mA	-61mA	-5nA	59nA	6.83pF	I/O	General purpose in/out pin.
B20	GPIOH	147mA	-175mA	-5nA	59nA	6.83pF	I/O	General purpose in/out pin.
C20	GPIOI	130mA	-148mA	-5nA	59nA	6.83pF	I/O	General purpose in/out pin.

Digital RGB Interface:

Ball location	Pin Name	18-bit Interface	Dual edge 12-bit		CRT+Sil 1162 (Dual 12 bit DVI)	DVO only	CRT+DVO	CRT only	CRT+THC63LVD823A(18bit LVDS)	CRT+TTL
			Low	High						
E20	DQA31	R0	G3	R7	D11				R12	R0
G21	DQA30	R1	G2	R6	D10				R13	R1
F20	DQA29	R2	G1	R5	D9				R14	R2
F21	DQA28	R3	G0	R4	D8				R15	R3
E21	DQMA3	G5	B5	R1	D5				G17	G5
H18	DQA27	R4	B7	R3	D7				R16	R4
H20	DQA26	R5	B6	R2	D6				R17	R5
J21	DQA25	G0	CLK+	CLK+	IDCK+				G12	G0
K21	DQA24	G1	CLK-	CLK-	IDCK-				G13	G1
M21	DQA23	G2	B4	R0	D4				G14	G2
L20	DQA22	G3	B3	G7	D3				G15	G3
P21	DQA21	G4	B2	G6	D2				G16	G4
N20	DQA20	B0	B1	G5	D1				B12	B0
M20	DQMA2	B5							B17	B5
N21	DQA19	B1	B0	G4	D0				B13	B1
R20	DQA18	B2	DE	DE	DE				B14	B2
R21	DQA17	B3	HSYNC	HSYNC	HSYNC				B15	B3
P18	DQA16	B4	VSYNC	VSYNC	VSYNC				B16	B4
D13	DDCCLK				CRT I2C SCL pull H	Pull L	CRT I2C SCL pull H	CRT I2C SCL pull H	CRT I2C SCL Pull H	CRT I2C SCL Pull H
C13	DDCDAT				CRT I2C SDA pull H	Pull L	CRT I2C SDA pull H	CRT I2C SDA pull H	CRT I2C SDA Pull H	CRT I2C SDA Pull H
D14	GPIOA				DVI I2C SCL pull H	Pull H	Pull H	Pull L	LCD VDD Pull L	LCD VDD Pull L
C14	GPIOB				DVI I2C SDA pull H	Pull H	Pull H	Pull L	LCD backlight Pull L	LCD backlight Pull L
B21	GPIOC	CLK			Enable DVI plug intA				CLK IN	CLK IN
C21	GPIOD	DE			Enable DVI nonPlug intA				DE	DE
D20	GPIOE				DVI hot Plug Sense	L: dual 12bit H: 18bit	L: dual 12bit H: 18bit		default H: 18bit	default H: 18bit
D21	GPIOF				PD# pull L	Pull H	Pull H		/PDWN Pull L	/PDWN Pull L
C15	GPIOG				Pull L	Pull L	Pull L	Pull L	Pull L	Pull L
B20	GPIOH	HSYNC			DDR2 Strap	DDR2 Strap	DDR2 Strap	DDR2 Strap	HSYNC (DDR2 Strap)	HSYNC (DDR2 Strap)
C20	GPIOI	VSYNC							VSYNC	VSYNC

Note: -If digital RGB output is utilized, the memory interface can only support the lower16-bits (DQ[15:0], DQM[1:0]) on the memory bus. The upper 16-bits (DQ[31:16], DQM[3:2]) of the memory bus are reserved for the digital RGB output interface. The upper 16-bits cannot simultaneously support both memory and digital RGB.

-For output current drive (IoL and IoH) and input leakage current (IiL and IiH), please see tables above.

Power Balls :

Ball location	Signal name	Type	Description
C17	AVDDDCLK	P	3.3V Analog power (DCLK generator).
C18	AVSSDCLK	P	Analog ground (DCLK generator).
D16	AVDDMCLK	P	3.3V Analog power (MCLK generator).
C16	AVSSMCLK	P	Analog ground (MCLK generator).
A10	AVDDDLL	P	3.3V Analog power (CLK DLL).
A9	AVSSDLL	P	Analog ground (CLK DLL).
D8	AVDDDAC1	P	1.8V Analog power (DAC).
D9	AVDDDAC2	P	1.8V Analog power (DAC).
C9	AVSSDAC1	P	Analog ground (DAC).
D10	AVSSDAC2	P	Analog ground (DAC).
V17	AVDDMDLL	P	3.3V Analog power (DDR DLL).
W18	AVSSMDLL	P	Analog ground (DDR DLL).
D18	OVDD3	P	3.3V power for Misc. and SPI.
D17	OVDD25	P	3.3V power for DVO control signal
C4, C5, C6, U4, V3	OVDDQ	P	3.3V power for PCI interface.
V10, V11, V12, W10, W11, W12, Y10, Y11, Y12, AA10, AA11	OVDDM	P	2.5V power for DRAM I/O interface.
V13, W13, Y13, AA12, AA13	VDDM	P	2.5V power for DRAM core power
J18, K18, L18	VDDO	P	3.3V power DVO interface
D5, D6, V4, V14, W4, W5, W14, U18, T18, R18, F18, E18	PVDD	P	3.3V power for I/O pre-driving.
A8, B8, C8, C7, D7, J12, J11, J10, K11, L11, M11, N12, N11, N10	IVDD	P	1.8V power for GPU digital core power.
A3, A7, A11, A12, A19, B3, B4, B5, B6, B7, B9, B10, B11, B12, B15, B16, B17, B18, B19, C3, C10, C19, G18, M18, H21, L21, U21, J20, K20, U20, D19, E19, F19, G19, H19, J19, K19, L19, M19, N19, P19, R19, T19, U19, Y17, Y16, W9, Y9, AA9, V8, W8, V7, T4, U2, V2, W2, W1, D3, E3, F3, G3, H3, J3, K3, L3, M3, N3, P3, R3, T3, U3, W3, J9, K9, L9, M9, N9, K10, L10, M10, K12, L12, M12, J13, K13, L13, M13, N13	GND	P	Digital ground.

Note:
P = Power pin
I = Input pin
O = Output pin
I/O = Input / Output pin
A = Analog pin

5 Volari™ Z9M Registers

5.1 General Registers

Miscellaneous Output Registers

Register Type: Read/Write
Read Port: 3CC
Write Port: 3C2
Default: 00h

D7 Vertical Sync Polarity
- 0: Select 'positive vertical sync'
- 1: Select 'negative vertical sync'

D6 Horizontal Sync Polarity
- 0: Select 'positive horizontal sync'
- 1: Select 'negative horizontal sync'

TABLE 5.1-1 SYNC POLARITY VS. VERTICAL SCREEN RESOLUTION

	D6	EGA	VGA
0	0	200 Lines	Invalid
0	1	350 Lines	400 Lines
1	0	Invalid	350 Lines
1	1	Invalid	480 Lines

D5 Odd/Even Page
- 0: Select low page of memory
- 1: Select high page of memory

D4 Reserved

D[3:2] Clock Select

TABLE 5.1-2 TABLE FOR VIDEO CLOCK SELECTION

D3	D2	DCLK
0	0	25.175 MHz
0	1	28.322 MHz
1	0	Don't Care
1	1	For internal clock generator.

D1 Display RAM Enable
- 0: Disable processor access to video RAM
- 1: Enable processor access to video RAM

D0 I/O Address Select
- 0: Sets addresses for monochrome emulation
- 1: Sets addresses for color graphics emulation

Feature Control Register

Register Type: Read/Write
Read Port: 3CA
Write Port: 3BA/3DA
Default: 00h
D[7:4] Reserved (0)
D3 Vertical Sync Select
0: Normal Vertical Sync output to monitor
1: [Vertical Sync OR Vertical Display Enable] output to monitor
D[2:0] Reserved (0)

Input Status Register 0

Register Type: Read only
Read Port: 3C2
Default: 00h
D7 Vertical Retrace Interrupt Pending
0: Cleared
1: Pending
D[6:5] Reserved
D4 Switch Sense
D[3:0] Reserved

Input Status Register 1

Register Type: Read only
Read Port: 3BA/3DA
Default: 00h
D[7:6] Reserved
D[5:4] Diagnostic

TABLE 5.1-3 TABLE FOR VIDEO READ-BACK THROUGH DIAGNOSTIC BIT (I)

Color Plane Enable Register		Input Status Register 1	
D5	**D4**	**D5**	**D4**
0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Unused	Unused

TABLE 5.1-4 TABLE FOR VIDEO READ-BACK THROUGH DIAGNOSTIC BIT (II)

Color Plane Enable register		Input Status Register 1	
D5	**D4**	**D5**	**D4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

D3 Vertical Trace
0: Inactive
1: Active
D[2:1] Reserved
D0 Display Enable Not
0: Display period
1: Retrace period

VGA Enable Register

Register Type: Read/Write
Read/Write Port: 3C3
Default: 00h
D0 VGA Enable
0: Disable
1: Enable

Segment Selection Register 0

Register Type: Read/Write
Read/Write Port: 3CD
Default: 00h
D[7:0] Segment Selection Write Bit[7:0]

Segment Selection Register 1

Register Type: Read/Write
Read/Write Port: 3CB
Default: 00h
D[7:0] Segment Selection Read Bit[7:0]

5.2 CRT Controller Registers

CRT Controller Index Register

Register Type: Read/Write
Read/Write Port: 3B4/3D4
Default: 00h
D[7:0] CRT Controller Index
- 00h ~ 18h for standard VGA
- 19h ~ 26h for XGI™ Technology extended CRT registers

TABLE 5.2.-1 TABLE OF CRT CONTROLLER REGISTERS

Index (3B4/3D4)	CRT Controller Registers (3B5/3D5)
00h	Horizontal Total
01h	Horizontal Display Enable End
02h	Horizontal Blank Start
03h	Horizontal Blank End
04h	Horizontal Retrace Start
05h	Horizontal Retrace End
06h	Vertical Total
07h	Overflow Register
08h	Preset Row Scan
09h	Max Scan Line/Text Character Height
0Ah	Text Cursor Start
0Bh	Text Cursor End
0Ch	Screen Start Address High
0Dh	Screen Start Address Low
0Eh	Text Cursor Location High
0Fh	Text Cursor Location Low
10h	Vertical Retrace Start
11h	Vertical Retrace End
12h	Vertical Display Enable End
13h	Screen Offset
14h	Underline Location
15h	Vertical Blank Start
16h	Vertical Blank End
17h	Mode Control
18h	Line Compare
1Bh	CRT horizontal counter read-back
1Ch	CRT vertical counter read back

1Dh	CRT overflow counter read back
22h	Graphics Data Latch Read-back Register
24h	Attribute Controller Toggle Read-back Register
26h	Attribute Controller Index Read-back Register

CR0: Horizontal Total

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 00h
Default: 00h
D[7:0] Horizontal Total Bit[7:0]

CR1: Horizontal Display Enable End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 01h
Default: 00h
D[7:0] Horizontal Display Enable End Bit[7:0]

CR2: Horizontal Blank Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 02h
Default: 00h
D[7:0] Horizontal Blank Start Bit[7:0]

CR3: Horizontal Blank End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 03h
Default: 00h
D7 Reserved
D[6:5] Display Skew Control Bit[1:0]
00: No skew
01: Skew 1 character
10: Skew 2 characters
11: Skew 3 characters
D[4:0] Horizontal Blank End Bit[4:0]

CR4: Horizontal Retrace Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 04h
Default: 00h
D[7:0] Horizontal Retrace Start Bit[7:0]

CR5: Horizontal Retrace End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 05h
Default: 00h
D7 Horizontal Blank End Bit[5]
D[6:5] Horizontal Retrace Delay Bit[1:0]
00: Skew 0 character clock
01: Skew 1 character clock
10: Skew 2 character clocks
11: Skew 3 character clocks
D[4:0] Horizontal Retrace End Bit[4:0]

CR6: Vertical Total

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 06h
Default: 00h
D[7:0] Vertical Total Bit[7:0]

CR7: Overflow Register

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 07h
Default: 00h
D7 Vertical Retrace Start Bit[9]
D6 Vertical Display Enable End Bit[9]
D5 Vertical Total Bit[9]
D4 Line Compare Bit[8]
D3 Vertical Blank Start Bit[8]
D2 Vertical Retrace Start Bit[8]
D1 Vertical Display Enable End Bit[8]
D0 Vertical Total Bit[8]

CR8: Preset Row Scan

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 08h
Default: 00h
D7 Reserved
D[6:5] Byte Panning Control Bit[1:0]
D[4:0] Preset Row Scan Bit[4:0]

CR9: Maximum Scan Line/Text Character Height

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 09h
Default: 00h
D7 Double Scan
0: Disable
1: Enable 400 lines display
D6 Line Compare Bit[9]
D5 Vertical Blank Start Bit[9]
D[4:0] Character Cell Height Bit[4:0]

CRA: Text Cursor Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Ah
Default: 00h
D[7:6] Reserved
D5 Text Cursor Off
0: Text Cursor On
1: Text Cursor Off
D[4:0] Text Cursor Start Bit[4:0]

CRB: Text Cursor End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Bh
Default: 00h
D7 Reserved
D[6:5] Text Cursor Skew
00: No skew
01: Skew one character clock
10: Skew two character clocks
11: Skew three character clocks
D[4:0] Text Cursor End Bit[4:0]

CRC: Screen Start Address High

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Ch
Default: 00h
D[7:0] Screen Start Address Bit[15:8]

CRD: Screen Start Address Low

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Dh
Default: 00h
D[7:0] Screen Start Address Bit[7:0]

CRE: Text Cursor Location High

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Eh
Default: 00h
D[7:0] Text Cursor Location Bit[15:8]

CRF: Text Cursor Location Low

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Fh
Default: 00h
D[7:0] Text Cursor Location Bit[7:0]

CR10: Vertical Retrace Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 10h
Default: 00h
D[7:0] Vertical Retrace Start Bit[7:0]

CR11: Vertical Retrace End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 11h
Default: 00h

D7 Write Protect for CR0 to CR7
- 0: Disable Write Protect
- 1: Enable Write Protect

D6 Alternate Refresh Rate
- 0: Selects three refresh cycles per scan line
- 1: Selects five refresh cycles per scan line

D5 Vertical Interrupt Enable
- 0: Enable
- 1: Disable

D4 Vertical Interrupt Clear
- 0: Clear
- 1: Not Clear

D[3:0] Vertical Retrace End Bit[3:0]

CR12: Vertical Display Enable End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 12h
Default: 00h

D[7:0] Vertical Display Enable End Bit[7:0]

CR13: Screen Offset

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 13h
Default: 00h

D[7:0] Screen Offset Bit[7:0]

CR14: Underline Location Register

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 14h
Default: 00h

D7 Reserved

D6 Double-word Mode Enable
- 0: Disable
- 1: Enable

D5 Count by 4
- 0: Disable
- 1: Enable

D[4:0] Underline Location Bit[4:0]

CR15: Vertical Blank Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 15h
Default: 00h

D[7:0] Vertical Blank Start Bit[7:0]

CR16: Vertical Blank End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 16h
Default: 00h
D[7:0] Vertical Blank End Bit[7:0]

CR17: Mode Control Register

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 17h
Default:00h
D7 Hardware Reset
0: Disable horizontal and vertical retraces outputs
1: Enable horizontal and vertical retrace outputs
D6 Word/Byte Address Mode
0: Set the memory address mode to word
1: Set the memory address mode to byte

D5 Address Wrap
0: Disable the full 256K of memory
1: Enable the full 256K of memory
D4 Reserved
D3 Count by Two
0: Byte refresh
1: Word refresh
D2 Horizontal Retrace Select
0 : Normal
1 : Double Scan
D1 RA1 replaces MA14
0 : Enable
1 : Disable
D0 RA0 replaces MA13
0: Enable
1: Disable

CR18: Line Compare Register

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 18h
Default: 00h
D[7:0] Line Compare Bit[7:0]

CR1B: CRT Horizontal Counter Read Back

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Bh
Default: xxh
D[7:0] CRT horizontal counter bit[7:0]

CR1C: CRT Vertical Counter Read Back

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Ch
Default: xxh
D[7:0] CRT vertical counter bit[7:0]

CR1D: CRT Overflow Counter Read Back

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Dh
Default: xxh
D[7:5] Reserved
D4 CRT horizontal counter bit 8
D3 Reserved
D[2:0] CRT vertical counter bit[10:8]

Note: The horizontal and vertical counter value will be latched when read register CR20. So the three registers value should be read after read CR20.

CR1E: Extended Signature Read-Back Register 2

Register Type: Read Only
Read/Write Port:3B5/3D5, Index 1Eh
Default: xxh
D[7:0] Signature read-back bit[23:16]

CR20: CRT Counter Trigger Port

Register Type:Read Only
Read/Write Port:3B5/3D5, Index 20h
Default: xxh
D[7:0] Reserved

CR24: Attribute Controller Toggle Read-back Register

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 24h
Default: xxh
D7 Attribute Controller Toggle
D[6:0] Reserved

CR26: Attribute Controller Index Read-back Register

Register Type: Read Only
Read/Write Port:3B5/3D5, Index 26h
Default: xxh
D[7:6] Reserved
D5 Video Enable
D[4:0] Attribute Controller Index bit[8:4]

5.3 Sequencer Registers

Sequencer Index Register

Register Type: Read/Write

Read/Write Port: 3C4
Default: 00h
D[7:6] Reserved
D[5:0] Sequencer Index Bit[5:0]

TABLE 5.3.-1 TABLE OF SEQUENCER REGISTERS

Index (3C4)	Sequencer Register (3C5)
00	Reset Register
01	Clock Mode
02	Color Plane Write Enable
03	Character Generator Select
04	Memory Mode

SR0: Reset Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 00h
Default: 00h
D[7:2] Reserved
D1 Synchronous reset
0: Reset
1: Normal
D0 Asynchronous reset
0: Reset
1: Normal

SR1: Clock Mode Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 01h
Default: 00h
D[7:6] Reserved
D5 Screen Off
0: Display On
1: Display Off
D4 Shifter Load 32 enables
0: Disable
1: Data shifter loaded every 4th Character Clock
D3 Dot Clock Divide by 2 enables
0: Disable
1: Video Clock is divided by 2 to generate Dot Clock
D2 Shifter Load 16 (while D4=0)
0: Disable
1: Data shifter loaded every 2nd Character Clock
D1 Reserved
D0 8/9 Dot Clock
0: Dot Clock is divided by 9 to generate Character Clock
1: Dot Clock is divided by 8 to generate Character Clock

SR2: Color Plane Write Enable Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 02h
Default: 00h
D[7:4] Reserved
D3 Plane 3 write enable
0: Disable
1: Enable
D2 Plane 2 write enable
0: Disable
1: Enable
D1 Plane 1 write enable
0: Disable
1: Enable
D0 Plane 0 write enable
0: Disable
1: Enable

SR3: Character Generator Select Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 03h
Default: 00h
D[7:6] Reserved
D5 Character generator table B selects Bit[2]
D4 Character generator table A select Bit[2]
D[3:2] Character generator table B selects Bit[1:0]
D[1:0] Character generator table A select Bit[1:0]

TABLE 5.3.-2 TABLE OF SELECTING ACTIVE CHARACTER GENERATOR

D5	**D3**	**D2**	**Used when text attribute bit 3 is 1**
D4	**D1**	**D0**	**Used when text attribute bit 3 is 0**
0	0	0	Character Table 1
0	0	1	Character Table 2
0	1	0	Character Table 3
0	1	1	Character Table 4
1	0	0	Character Table 5 (VGA only)
1	0	1	Character Table 6 (VGA only)
1	1	0	Character Table 7 (VGA only)
1	1	1	Character Table 8 (VGA only)

SR4: Memory Mode Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 04h
Default: 00h

D[7:4] Reserved

D3 Chain-4 Mode enables
- 0: Disable
- 1: Enable

D2 Odd/Even Mode enables
- 0: Enable
- 1: Disable

D1 Extended Memory
- 0: Select 64K
- 1: Select 256K

D0 Reserved

5.4 Graphics Controller Registers

Graphics Controller Index Register

Register Type: Read/Write
Read/Write Port: 3CE
Default: 00h
D[7:4] Reserved
D[3:0] Graphics Controller Index Bit[3:0]

TABLE 5.4.-1 TABLE OF GRAPHICS CONTROLLER REGISTERS

Index (3CE)	Graphics Controller Register (3CF)
00	Set/Reset Register
01	Set/Reset Enable Register
02	Color Compare Register
03	Data Rotate & Function Select
04	Read Plane Select Register
05	Mode Register
06	Miscellaneous Register
07	Color Don't Care Register
08	Bit Mask Register

GR0: Set/Reset Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 00h
Default: 00h
D[7:4] Reserved
D3 Set/Reset Map for plane 3
D2 Set/Reset Map for plane 2
D1 Set/Reset Map for plane 1
D0 Set/Reset Map for plane 0

GR1: Set/Reset Enable Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 01h
Default: 00h
D[7:4] Reserved
D3 Enable Set/Reset for plane 3
0: Disable
1: Enable
D2 Enable Set/Reset for plane 2
0: Disable
1: Enable
D1 Enable Set/Reset for plane 1
0: Disable
1: Enable
D0 Enable Set/Reset for plane 0
0: Disable
1: Enable

GR2: Color Compare Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 02h
Default: 00h
D[7:4] Reserved
D3 Color Compare Map for plane 3
D2 Color Compare Map for plane 2
D1 Color Compare Map for plane 1
D0 Color Compare Map for plane 0

GR3: Data Rotate/Function Select Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 03h
Default: 00h
D[7:5] Reserved
D[4:3] Function Select

TABLE 5.4.-2 TABLE OF FUNCTION SELECT

D4	D3	Function
0	0	write data unmodified
0	1	write data AND processor latches
1	0	write data OR processor latches
1	1	write data XOR processor latches

D[2:0] Rotate Count

TABLE 5.4-3 TABLE OF ROTATE COUNT

D2	D1	D0	Right Rotation
0	0	0	none
0	0	1	1 bits
0	1	0	2 bits
0	1	1	3 bits
1	0	0	4 bits
1	0	1	5 bits
1	1	0	6 bits
1	1	1	7 bits

GR4: Read Plane Select Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 04h
Default: 00h
D[7:2] Reserved
D[1:0] Read Plane Select bit 1, 0
00: Plane 0
01: Plane 1
10: Plane 2
11: Plane 3

GR5: Mode Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 05h
Default: 00h
D7 Reserved
D6 256-color Mode
0: Disable
1: Enable

D5 Shift Register Mode
0: Configure shift register to be EGA compatible
1: Configure shift register to be CGA compatible
D4 Odd/Even Addressing Mode enables
0: Disable
1: Enable
D3 Read Mode
0: Map Select Read
1: Color Compare Read
D2 Reserved
D[1:0] Write mode

TABLE 5.4-4 TABLE FOR WRITE MODE

D1	D0	Mode Selected
0	0	Write Mode 0: Direct processor write (Data Rotate, Set/Reset may apply).
0	1	Write Mode 1: Use content of latches as write data.
1	0	Write Mode 2: Color Plane n(0-3) is filled with the value of bit m in the processor write data.
1	1	Write Mode 3: Color Plane n(0-3) is filled with 8 bits of the color value contained in the Set/Reset Register for that plane. The Enable Set/Reset Register is not effective. Processor data will be AND with Bit Mask Register content to form new bit mask pattern. (data rotate may apply).

GR6: Miscellaneous Register

Register Type:Read/Write
Read/Write Port:3CF, Index 06h
Default: 00h
D[7:4] Reserved
D[3:2] Memory Address Select

TABLE 5.4-5 TABLE OF MEMORY ADDRESS SELECT

D3	D2	Address range
0	0	A0000 to BFFFF
0	1	A0000 to AFFFF
1	0	B0000 to B7FFF
1	1	B8000 to BFFFF

D1 Chain Odd And Even Maps
0 : Disable
1 : Enable
D0 Graphics Mode Enable
0: Select alphanumeric mode
1: Select graphics mode

GR7: Color Don't Care Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 07h
Default: 00h
D[7:4] Reserved
D3 Plane 3 Don't Care
0: Disable color comparison
1: Enable color comparison
D2 Plane 2 Don't Care
0: Disable color comparison
1: Enable color comparison
D1 Plane 1 Don't Care
0: Disable color comparison
1: Enable color comparison
D0 Plane 0 Don't Care
0: Disable color comparison
1: Enable color comparison

GR8: Bit Mask Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 08h
Default: 00h
D[7:0] Bit Mask Enable Bit[7:0]

5.5 Attribute Controller and Video DAC Registers

Attribute Controller Index Register

Register Type: Read/Write
Read Port: 3C0
Write Port: 3C0
Default: 00h
D[7:6] Reserved
D5 Palette Address Source
0: From CPU
1: From CRT
D[4:0] Attribute Controller Index Bit[4:0] (00h-14h)

TABLE 5.5-1 TABLE OF ATTRIBUTE CONTROLLER REGISTERS

Index (3C0)	Attribute Controller Register (3C0)
00h	Color Palette Register 0
01h	Color Palette Register 1
02h	Color Palette Register 2
03h	Color Palette Register 3
04h	Color Palette Register 4
05h	Color Palette Register 5
06h	Color Palette Register 6
07h	Color Palette Register 7
08h	Color Palette Register 8
09h	Color Palette Register 9
0Ah	Color Palette Register 10
0Bh	Color Palette Register 11
0Ch	Color Palette Register 12
0Dh	Color Palette Register 13
0Eh	Color Palette Register 14
0Fh	Color Palette Register 15
10h	Mode Control Register
11h	Screen Border Color
12h	Color Plane Enable Register
13h	Pixel Panning Register
14h	Color Select Register (VGA)

AR0~ARF: Palette Registers

Register Type: Read/Write
Read Port: 3C1, Index 00h ~ 0Fh
Write Port: 3C0, Index 00h ~ 0Fh
Default: 00h
D[7:6] Reserved
D[5:0] Palette Entries

AR10: Mode Control Register

Register Type: Read/Write
Read Port: 3C1, Index 10h
Write Port: 3C0, Index 10h
Default: 00h
D7 P4, P5 Source Select
0: AR0-F Bit[5:4] is used as the source for the Lookup Table Address Bit[5:4]
1: AR14 Bit[1:0] are used as the source for the Lookup Table Address Bit[5:4]
D6 Pixel Double Clock Select
0: The pixels are clocked at every clock cycle
1: The pixels are clocked at every other clock cycle
D5 PEL Panning Compatibility with Line Compare
0: Disable
1: Enable
D4 Reserved
D3 Background Intensity or Blink enable (while the Character Attribute D7=1)
0: Background Intensity attribute enable
1: Background Blink attribute enable
D2 Line Graphics enable
0: The ninth bit of nine-bit-wide character cell will be the same as the background.
1: The ninth bit of nine-bit-wide character cell will be made be the same as the eighth bit for character codes in the range C0h through DFh.
D1 Display Type
0: The contents of the Attribute byte are treated as color attribute.
1: The contents of the Attribute byte are treated as MDA-compatible attribute.
D0 Graphics/Text Mode
0: The Attribute Controller will function in text mode.
1: The Attribute Controller will function in graphics mode.

AR11: Screen Border Color

Register Type: Read/Write
Read Port: 3C1, Index 11h
Write Port: 3C0, Index 11h
Default: 00h
D[7:6] Reserved
D[5:0] Palette Entry

AR12: Color Plane Enable Register

Register Type: Read/Write
Read Port: 3C1, Index 12h

Write Port: 3C0, Index 12h
Default: 00h
D[7:6] Reserved
D[5:4] Display Status MUX Bit[1:0]
These bits select two of the eight bits color outputs to be available in the status register. The output color combinations available on the status bits are as follows:

TABLE 5.5-2 TABLE FOR VIDEO READ-BACK THROUGH DIAGNOSTIC BIT (I)

Color Plane Enable Register		**Input Status Register 1 (Refer to 7.1.4)**	
D5	D4	D5	D4
0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Unused	Unused

TABLE 5.5-3 TABLE FOR VIDEO READ-BACK THROUGH DIAGNOSTIC BIT (II)

Color Plane Enable Register		**Input Status Register 1 (Refer to 7.1.4)**	
D5	D4	D5	D4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

D[3:0] Enable Color Plane Bit[3:0]

AR13: Pixel Panning Register

Register Type: Read/Write
Read Port: 3C1, Index 13h
Write Port: 3C0, Index 13h
Default: 00h
D[7:4] Reserved
D[3:0] Pixel Pan Bit[3:0]
This field specifies the number of pixels the display data will be shifted to the left. This field is interpreted as indicated in the following table:

TABLE 5.5-4 TABLE OF PIXEL PANNING

D3	D2	D1	D0	Monochrome Text	VGA Mode 13	All others
0	0	0	0	8	0	0
0	0	0	1	0	Invalid	1
0	0	1	0	1	1	2
0	0	1	1	2	Invalid	3
0	1	0	0	3	2	4
0	1	0	1	4	Invalid	5
0	1	1	0	5	3	6
0	1	1	1	6	Invalid	7
1	0	0	0	7	Invalid	Invalid
1	0	0	1	Invalid	Invalid	Invalid
1	0	1	0	Invalid	Invalid	Invalid
1	0	1	1	Invalid	Invalid	Invalid
1	1	0	0	Invalid	Invalid	Invalid
1	1	0	1	Invalid	Invalid	Invalid
1	1	1	0	Invalid	Invalid	Invalid
1	1	1	1	Invalid	Invalid	Invalid

AR14: Color Select Register

Register Type: Read/Write
Read Port: 3C1, Index 14h
Write Port: 3C0, Index 14h
Default: 00h
D[7:4] Reserved
D[3:2] Color Bit[7:6]
These two bits are concatenated with the six bits from the Palette Register to form the address into the LUT and to drive P[7:6].
D[1:0] Color Bit[5:4]
If AR10 D7 is programmed to a '1', these two bits replace the corresponding two bits from the Palette Register to form the address into the LUT and to drive P[5:4]. If AR10 D7 is programmed to a '0', these two bits are ignored.

5.6 Color Registers

DAC Status Register

Register Type: Read Only
Read Port: 3C7
Default: 00h
D[7:2] Reserved
D[1:0] DAC State Bit[1:0]
00: Write Operation in progress
11: Read Operation in progress

DAC Index Register (Read Mode)

Register Type: Write Only
Write Port:C7
Default: 00h
D[7:0] DAC Index Bit[7:0]

DAC Index Register (Write Mode)

Register Type: Read/Write
Read/Write Port: 3C8
Default: 00h
D[7:0] DAC Index Bit[7:0]

DAC Data Register

Register Type: Read/Write
Read/Write Port: 3C9
Default: 00h
When SR7 D2 = 1
D[7:6] Reserved
D[5:0] DAC Data [5:0]
Before writing to this register, 3C8h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue values for the DAC entry are written. After the third value is written, the values are transferred to the LUT and the DAC index is incremented in case new values for the next DAC index are to be written.
Before reading from this register, 3C7h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue value for the DAC entry may be read from this DAC index. After the third value is read, the DAC index is incremented in case the value for the next DAC indexes to be read.When SR7 D2 = 0 D[7:0] DAC Data [7:0]When SR7 D2 = 0, the 24-bit LUT is enabled. This LUT could translate the R, G, B values into new R, G, B values independently. This LUT could be used for performing GAMMA correction function. The programming procedure is same as standard LUT when SR7 D2 = 1.

PEL Mask Register

Register Type: Read/Write
Read/Write Port: 3C6
Default: 00h
D[7:0] Pixel Mask Bit[7:0]
This field is the Pixel Mask for the palette DAC. If a bit in this field is programmed to '0', the corresponding bit in the pixel data will be ignored in looking up an entry in the LUT.

5.7 Extended Registers

Register Type: Read/Write
Read/Write Port: 3C4
Default: 00h
D[7:6] Reserved
D[5:0] Extended Register Index Bit[5:0] (05h ~ 3Fh)

TABLE 5.7-1 TABLE OF EXTENDED REGISTERS

Index (3C4)	Extended Enhanced Register (3C5)
05h	Extended Password/Identification Register
06h	Extended graphics mode register
07h	RAMDAC control register
08h	CRT threshold register I
09h	CRT threshold register II
0Ah	Extended vertical overflow register
0Bh	Extended horizontal overflow register I
0Ch	Extended horizontal overflow register II
0Dh	Extended CRT starting address register
0Eh	Extended CRT pitch register
0Fh	CRT misc. control register
10h	Display line width register
11h	DDC register
12h	Feature connector control register
13h	DRAM configuration setting register
14h	DRAM sizing register
15h	DRAM state machine control register
16h	DRAM refresh queue setting
17h	DRAM I/O pads setting register I
18h	DRAM timing setting register I
19h	DRAM timing setting register II
1Ah	DRAM feedback SCLK delay compensation register I
1Bh	DRAM feedback SCLK delay compensation register II
1Ch	DRAM I/O pads setting register II
1Dh	Segment Selection Overflow Register
1Eh	Module enable register
1Fh	Power management register
20h	PCI address decoder setting register
21h	PCI state machine setting register

22h	PCI controller timing register
23h	PCI timer register I
24h	PCI timer register II
25h	Reserved
26h	Turbo Queue base address register
27h	Turbo Queue control register
28h	Extended MCLK clock generator register I
29h	Extended MCLK clock generator register II
2Ah	Extended MCLK clock generator register III
2Bh	Extended DCLK clock generator register I
2Ch	Extended DCLK clock generator register II
2Dh	Extended DCLK clock generator register III
2Eh	Reserved
2Fh	Reserved
30h	Reserved
31h	Extended clock generator misc. register
32h	Extended clock source selection register
33h	Reserved
34h	Interrupt status register
35h	Interrupt enable register
36h	Interrupt reset register
37h	Reserved
38h	Power on trapping register I
39h	Power on trapping register II
3Ah	Power on trapping register III
3Bh	Bounding option read back
3Ch	Synchronous reset register
3Dh	Testing enabling register
3Eh	CRT1 S/W Flipping register I
3Fh	Reserved

5.8 PCI Configuration Registers

CNFG00: Configuration Register 00h

Register Type: Read
Read Port: 0000h
Default: 002018CA
D[31:16] :Device ID (read only)
XGI™ Technology Volari™ Z9M Device ID is 0020h or 0021h set by MAA13
D[15:0] : Vendor ID (read only)
XGI™ Technology Vendor ID is 18Cah

CNFG04: Configuration Register 04h

Register Type: Read/Write
Read Port: 0004h
Default: 02300000h
D[31:30] reserved
D29 Received master abort
0: normal
1: Volari™ Z9M GPU transaction is terminated by master abort
D28 Received target abort
0: normal
1: Volari™ Z9M GPU transaction is terminated by target abort
D27 Signaled target abort
0: normal
1: Volari™ Z9M GPU terminates transaction with target abort
D[26:25] DEVSEL* timing (read only)
00: fast
01: medium (fixed at this value)
10: slow
11: reserved
D24 reserved
D23 Fast back-to-back capable (read only)
0: not capable (fixed at this value)
1: capable
D22 reserved
D21 66 MHz capable (read only)
0: Support 33MHz
1: Support 66 MHz (fixed at this value)

D20 Capabilities List (read only)
0: does not implement a list of capabilities
1: implements a list of capabilities (fixed at this value)
D[19:10] reserved
D9 Fast back-to-back enable (read only)
0: disable (fixed at this value)
1: enable
D[8:6] reserved
D5 VGA Palette Snoop (read/write)
0: Disable
1: Enable
D4 Memory writes and invalidate enable (read only)
0: Disable (fixed at this value)
1: Enable
D3 Special cycles (read only)
0: Disable (fixed at this value)
1: Enable

D2 Bus Master (read only)
0: Device is not a bus master (fixed at this value)
1: Device is a bus master
D1 Memory Space (read/write)
0: Disable
1: Enable
D0 I/O Space (read/write)
0: Disable
1: Enable

CNFG08: Configuration Register 08h

Register Type: Read
Read Port: 0008h
Default: 030000XXh
D[31:8] Class Code (= 031000h)
D[7:0] Revision ID (= xxh)
The revision ID is depend on the chip version

CNFG0C: Configuration Register 0Ch

Register Type: Read
Read Port: 000Ch
Default: 80000700h
D31 BIST capable (read only)
0: not capable
1: capable (default)
D30 Start BIST (read/write)
0: BIST stop / BIST completed
1: invoke BIST (for internal test only)
D[29:28] reserved
D[27:24] Completion Code (read only)
0000: BIST test passed
others: test failure code (for internal test only)
D23 Reserved

D[22:16] reserved
D[15:11] Latency timer[7:3] (read/write)
PCI master maximum latency time = Latency timer[7:3]*8 clock cycles of AGP bus
D[10:8] Latency timer[2:0] (read only)
111: default value
D[7:0] reserved

CNFG10: Configuration Register 10h

Register Type: Read/Write
Read Port: 0010h
Default: 00000008h

If I/O pins MAA[10:8] are trapped high, then

D[31:28] Linear Memory Base address[31:28] (read/write)
32-bit memory base register for 256MB linear frame buffer

D[27:4] Linear Memory Base address[27:4] (read only)
00000000000000000000: default value

D3 Prefetchable (read only)
1: enable (default)

D[2:1] Addressing type (read only)
00: 32-bit address space (default)

D0 Memory space indicator (read only)
0: memory space (default)

If I/O pins MAA[10:8] are trapped low, then default = 0

D[31:21] Linear Memory Base address[31:21] (read/write)
32-bit memory base register for 2MB linear frame buffer

D[20:4] Linear Memory Base address[20:4] (read only)

Table of Function Select Table of Function Select 00000000000000000000: default value

D3 Prefetchable (read only)
1: enable (default)

D[2:1] Addressing type (read only)
00: 32-bit address space (default)

D0 Memory space indicator (read only)
0: memory space (default)

If I/O pin ROMMA10 is trapped low, then default = 0

CNFG14: Configuration Register 14h

Register Type: Read/Write
Read Port: 0014h
Default: 00000000h

D[31:18] MMIO Base address[31:18] (read/write)
32-bit memory base register for 128KB linear frame buffer

D[17:4] MMIO Base address[17:4] (read only)
0000000000000: default value

D3 Prefetchable (read only)
0: disable (default)

D[2:1] Addressing type (read only)
00: 32-bit address space (default)

D0 Memory space indicator (read only)
0: memory space (default)

CNFG18: Configuration Register 18h

Register Type: Read/Write
Read Port: 0018h
Default: 00000001h

D[31:7] Relocated I/O Base address[31:7] (read/write)
32-bit I/O base register for 128 I/O register

D[6:1] Relocated I/O Base address[6:1] (read only)
000000: default value

D0 Memory space indicator (read only)
1: I/O space (default)

CNFG2C: Configuration Register 2Ch

Register Type: Read/Write Once Only
Read Port: 002Ch
Default: 00000000h
D[31:16] Subsystem ID
D[15:0] Subsystem Vendor ID

CNFG30: Configuration Register 30h

Register Type: Read/Write
Read Port: 0030h
Default: 00000000h
D[31:15] Expansion ROM Base Address[31:15] (read/write)
D[15:11] Expansion ROM Base Address[15:11] (read only)
D[10:1] reserved
D0 ROM Enable Bit
0: Disable
1: Enable

CNFG34: Configuration Register 34h

Register Type: Read Only
Read Port: 0034h
Default: 00000040h
D[31:8] reserved
D[7:0] Capabilities list offset pointer

CNFG3C: Configuration Register 3Ch

Register Type: Read/Write
Read Port: 003Ch
Default: 00000000h
D[31:16] reserved
D[15:8] Interrupt Pin (Read Only)
If I/O pin ROMMA3 is trapped high, then = 01h
If I/O pin ROMMA3 is trapped low, then = 00h
D[7:0] Interrupt Line (read/write)

5.9 Power management Registers

CNFG40: Configuration Register 40h

Register Type: Read
Read Port: 0040h
Default: 00005001h
D[31:27] PME support
xxxx1: PME# could be asserted from D0
xxx1x: PME# could be asserted from D1
xx1xx: PME# could be asserted from D2
x1xxx: PME# could be asserted from D3hot
1xxxx: PME# could be asserted from D3cold
D26 D2 support
0: this device does not supports D2
1: this device supports D2
D25 D1 support
0: this device does not supports D1
1: this device supports D1
D[15:8] Pointer to next ID (read only)
= 50h (point to AGP configuration registers)
D[7:0] Capability ID (read only)
= 01h (PCI power management ID)

CNFG44: Configuration Register 44h

Register Type: Read
Read Port: 0044h
Default: 00000000h
D[31:2] reserved
D[1:0] PCI power state
00: D0
01: D1
10: D2
11: D3

5.10 Hardware Trapping

The hardware trapping sets the initial state of the GPU during power-on.

Table 5.15-1 Hardware trapping options

Pin Name	Value	Register	Description
MAA[3] BhwTrap[0]	0 1	SR38[0] (BromDev)	Enable SPI (Firmware Trapping) Disable SPI (PCI Write)
MAA[4] BhwTrap[1]	0 1	SR38[1] (BromSize)	32KB ROM decoding 64KB ROM decoding
MAA[5] BhwTrap[2]	0 1	SR38[2] (BADBusRev)	Disable PCI AD Bus Reverse Enable PCI AD Bus Reverse
MAA[6] BhwTrap[3]	0 1	SR3A[0] (BAFSubsysID)	Sub-system ID auto-fetch Sub-system ID programmable
MAA[7] BhwTrap[4]	0 1	SR3A[1] (BenPciSusN)	D2 state enable D2 state disable
MAA[10:8] BhwTrap[7:5]	000 111	SR3A[4:2] (BLFBSizeSel)	Local Frame Buffer size selection 2MB to 256MB
MAA[11] BhwTrap[8]	0 1	SR3A[5] (BPciIODrv)	PCI I/O interface driving control
MAA[12] BhwTrap[9]	0 1	SR3A[6] (BextClkgen)	select internal clock generators select external clock generators
MAA[13] BhwTrap[10]	0 1 (default)	SR3A[7] (HWTraping[10])	Device ID decide by SR1E[1]; SR1E[1] =1 => Device ID =0021; SR1E[1] =0 => Device ID =0020 Device ID = 0021 (default)

When MAA5 is high, the AD signals of the PCI bus are reversed. The relationship of the signals is shown below:
MAA5=0, the AD bus default values are shown on the left side
MAA5=1, the AD bus default values are shown on the right side

AD0 → AD24	AD1→ AD31	AD2→ AD30	AD3→ AD28	AD4→ AD29	AD5 →AD27
AD6 → AD25	AD7→ AD26	AD8→ AD23	AD9→ AD19	AD10→AD22	AD11→AD17
AD12→AD20	AD13→AD21	AD14→AD16	AD15→AD18	AD16→AD14	AD17→AD15
AD18→AD13	AD19→AD9	AD20→AD11	AD21→AD10	AD22→AD12	AD23→AD8
AD24→AD6	AD25→AD5	AD26→AD7	AD27→AD3	AD28→AD2	AD29→AD0
AD30→AD1	AD31→AD4				

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

TABLE 6.1-1 TABLE OF ABSOLUTE MAXIMUM RATINGS

Parameter	Min.	Max.	Unit
Operation temperature	-20 (Ta)	85 (Ta) / 110 (Tc)	℃
Storage temperature	-40	125	℃

Note:

When Ta=25℃, Tc=56℃
Theta Jc = 1.1 ℃/W

6.2 DC Characteristics

OVDD3 = 3.3 V ± 5 %, IVDD = 1.8 V ± 5 % ,GND = 0 V

TABLE 6.2-1 TABLE OF DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
V_{IL}	Input low voltage of 3.3V signals	-0.5	0.8	V	
V_{IH}	Input high voltage of 3.3V signals	2.2	OVDD3+ 10%	V	
V_{OL}	Output low voltage of 3.3V signals	-	0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output high voltage of 3.3V signals	2.4	-	V	I_{OH} = -1.0 mA
I_{IL}	Input leakage current	-	± 10	uA	
I_{OZ}	Tristate leakage current	-	± 20	uA	$0.45 < V_{OUT} < V_{DD}$

6.3 DC Characteristics for DAC (Analog Output Characteristics)

TABLE 6.3-1 TABLE OF DC CHARACTERISTICS FOR DAC

Description	Min	Typical	Max	Unit
Black Level	-	0	-	V
White Level	-	700	770	mV
ILE	-1.0	-	+1.0	LSB
DLE	-0.5	-	+0.5	LSB
1 LSB	-	2.734	-	mV
Iref	-	8.40	-	mA

6.4 AC Characteristics for DAC (Analog Output Characteristics)

TABLE 6.4-1 TABLE OF AC CHARACTERISTICS FOR DAC

Description	Parameter	Condition	Typical	Max.	Unit
Settling Time	Tsett	R=37.5 ohm C1=30 pF	-	6	ns

6.5 AC Characteristics

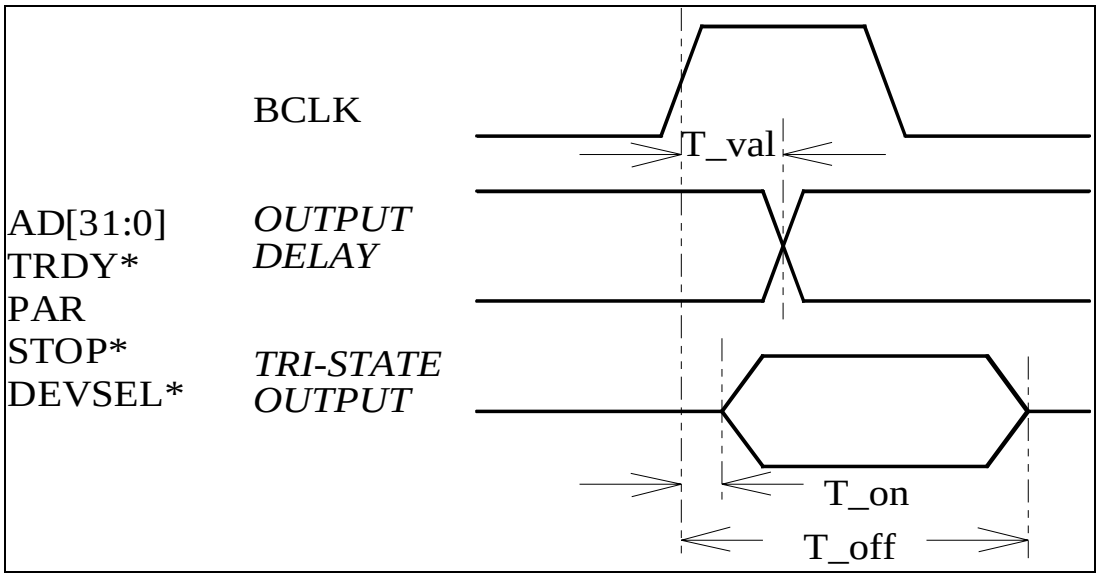


Figure 6.5-1 PCI Output and Tri-state Timing

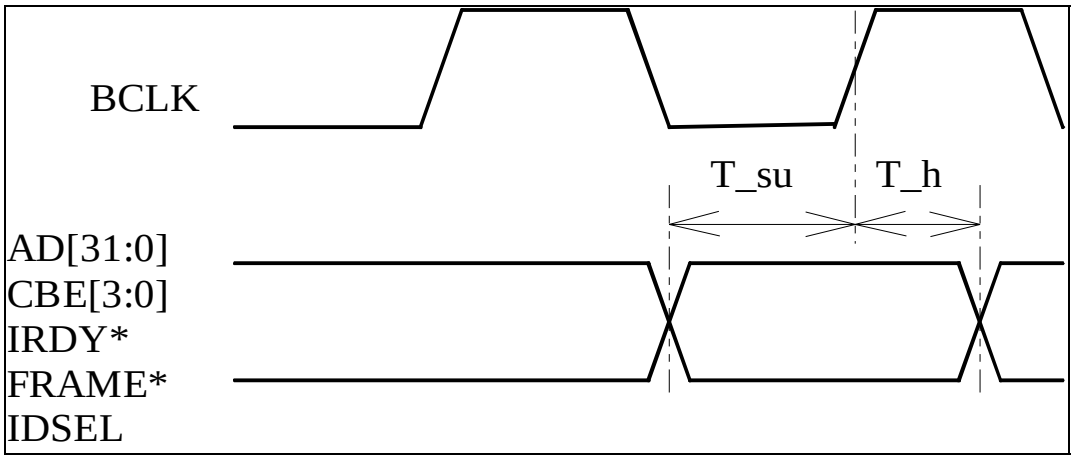


Figure 6.5-2 PCI Input Timing

Symbol	Parameter	66MHz		33MHz		Units
		MIN	MAX	MIN	MAX	
Tval	BCLK to Signal Valid Delay	2	6	2	11	ns
Ton	Float to Active Delay	2	-	2	-	ns
Toff	Active to Float Delay	-	14	-	28	ns
Tsu	Input Setup Time to BCLK	3	-	7	-	ns
Th	Input Hold Time from BCLK	0	-	0	-	ns

Table 6.5-1 PCI Timing Table

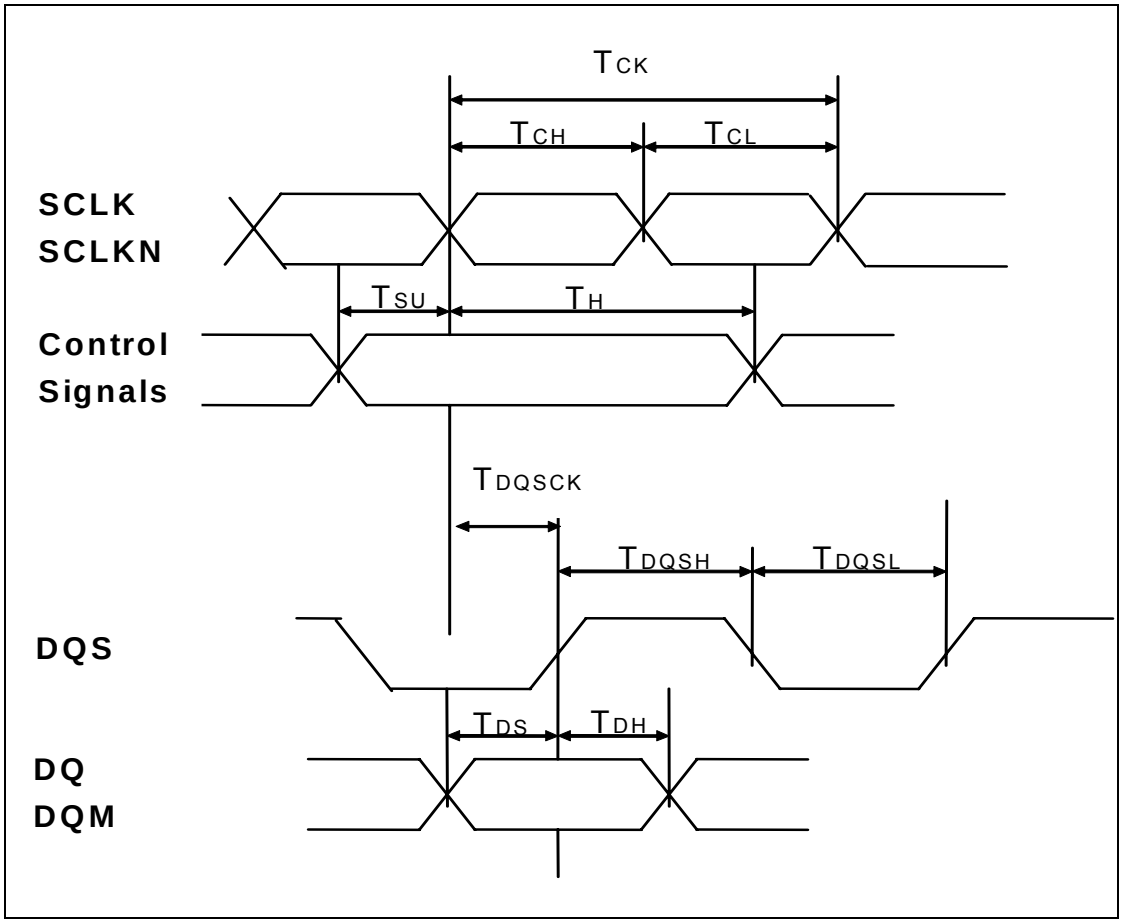


Figure 6.5-3 DDR SDRAM Write Timing

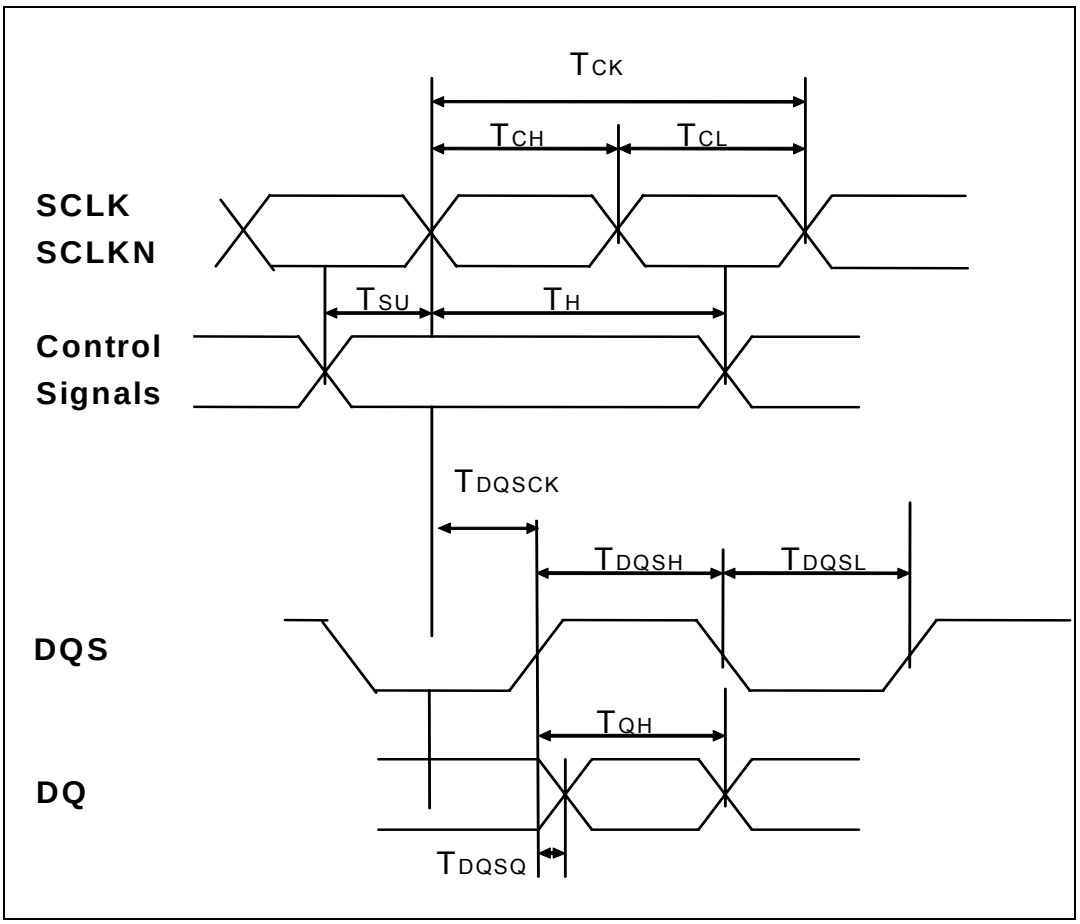


Figure 6.5-4 DDR SDRAM Read Timing

Symbol	Parameter	Min	Max.	Units
T_{CK}	Clock Cycle Time	6		ns
T_{CH}	CLK high level width	0.45	0.55	T_{CK}
T_{CL}	CLK low level width	0.45	0.55	T_{CK}
T_{IS}	Control Setup Timing	0.75	-	ns
T_{IH}	Control Hold Timing	0.75	-	ns
T_{DS}	DQ/DM Setup Timing	0.45	-	ns
T_{DH}	DQ/DM Hold Timing	0.45	-	ns
T_{DQSCK}	DQS to CLK Timing	-0.6	0.6	ns
T_{DQSH}	DQS High Pulse Width	0.35	-	T_{CK}
T_{DQSL}	DQS Low Pulse Width	0.35	-	T_{CK}
T_{QH}	DQ Output Hold Time	1.1	-	ns
T_{DQSQ}	DQS to DQ Time	-	0.45	ns

Table 6.5-2 DDR SDRAM Timing Table

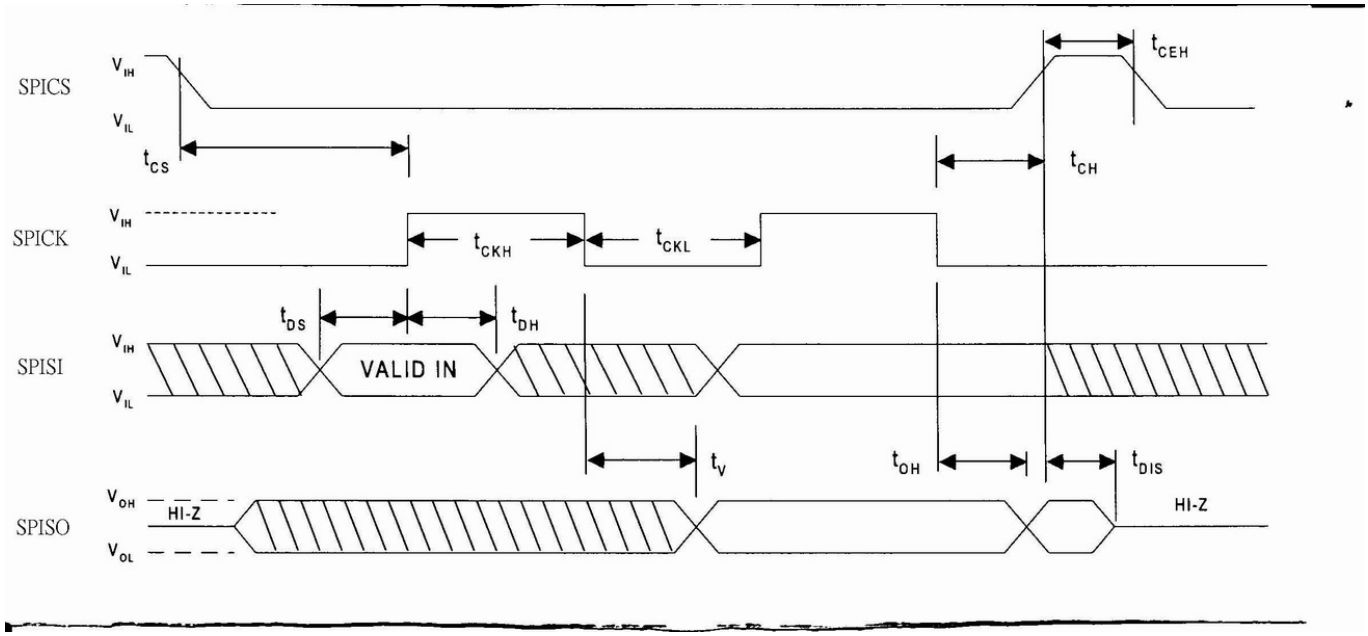


Figure 6.5-5 SPI Timing

		min	max	Unit
tCSS	CS to CK setup time	30	-	ns
tCSH	CK to CS hold time	20	-	ns
tCS	CS high time	50	-	ns
tWH	CK high time	20	-	ns
tWL	CK low time	20	-	ns
tSU	Data write setup time	20	-	ns
tH	Data write hold time	20	-	ns
tV	Data read setup time	5	-	ns
tHO	Data read hold time	5	-	ns
tDIS	Data disable time	10	-	ns

(Units: ns)

Table 6.5-3 SPI Timing Table

7 Volari™ Z9M Ballout

7.1 Volari™ Z9M Ball Distribution

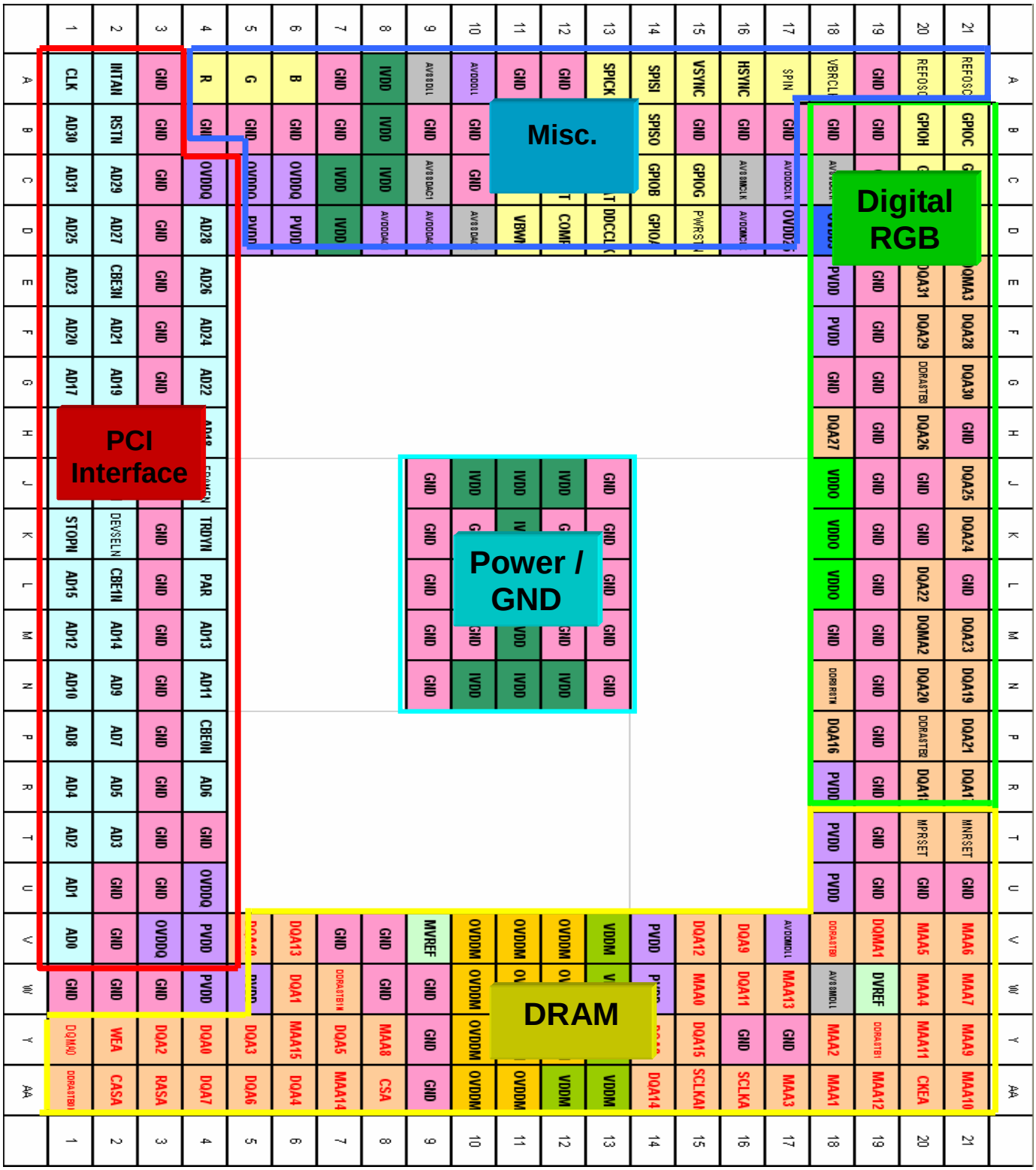


Figure 7.1-1 Volari™ Z9M Interface

7.2 Volari™ Z9M Pin Assignment

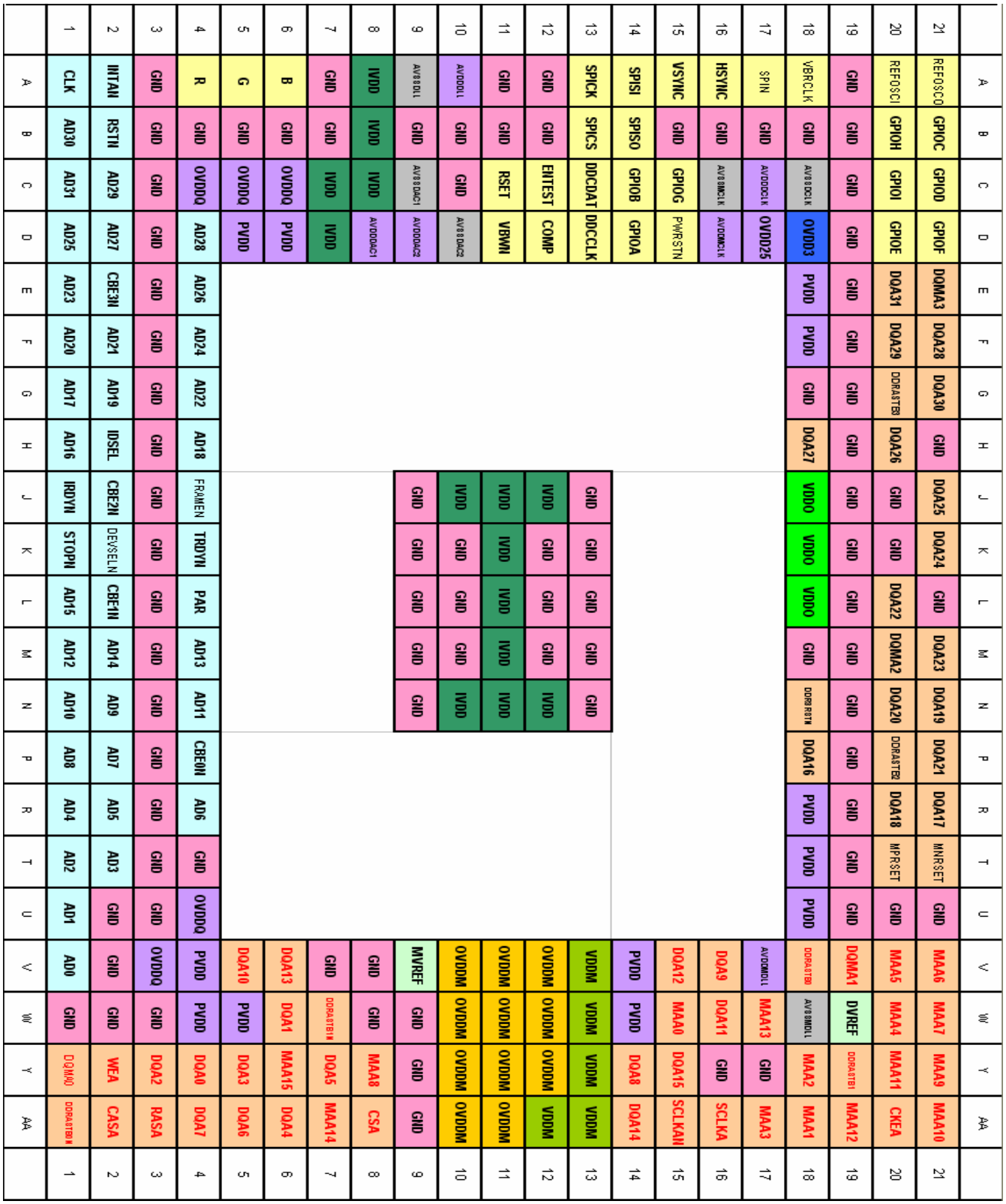


Figure 7.2-1 Volari™ Z9M Ball Assignment

8 Volari™ Z9M SMT Thermal Profile (lead free)

<TBD>

Figure 8.1-1 Volari™ Z9M GPU SMT Top-Side Thermal Profile (Lead free)

9 Volari™ Z9M Hardware Trapping

Pin Name	Value	Description	Default
MAA 3	0 1	Enable SPI Disable SPI	0
MAA4	0 1	32KB ROM decoding 64KB ROM decoding	0
MAA5	0 1	Disable PCI AD Bus Reverse Enable PCI AD Bus Reverse	0
MAA6	0 1	Sub-system ID auto-fetch Sub-system ID programmable	0
MAA7	0 1	D2 state Enable D2 state Disable	0
MAA8	0 1	Local Frame Buffer Size -- MAA[10:8] 0 0 0: 2MB 1 0 1: 64MB 0 0 1: 4MB 1 1 0: 128MB 0 1 0: 8MB 1 1 1: 256MB 0 1 1: 16MB 1 0 0: 32MB	0
MAA9	0 1		0
MAA10	0 1		1
MAA11	0 1	PCI I/O interface driving control 0: Weak 1: Strong	0
MAA12	0 1	Select internal clock generator Select external clock generator	0
MAA13	0 1	Device ID decide by SR1E[1]; SR1E[1] =1 => Device ID =0021; SR1E[1] =0 => Device ID =0020 Device ID = 0021 (default)	1

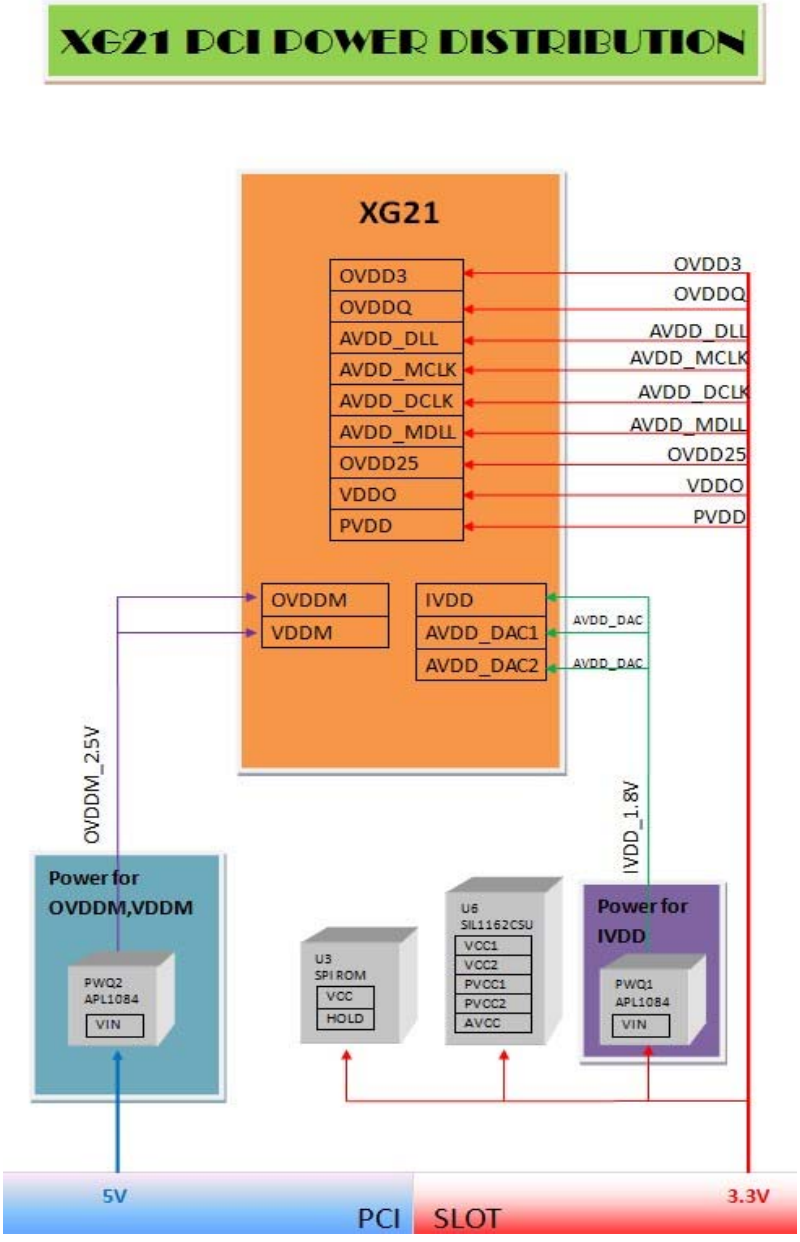
Note: 1. If the serial ROM is not used (integrated system BIOS), then MAA3 and MAA6 both need to be high.

2. The hardware trapping signal needs to be set high or low, depending on the system configuration. These pins cannot be left floating or open.

10 Volari™ Z9M Power Consumption

Test Environment:

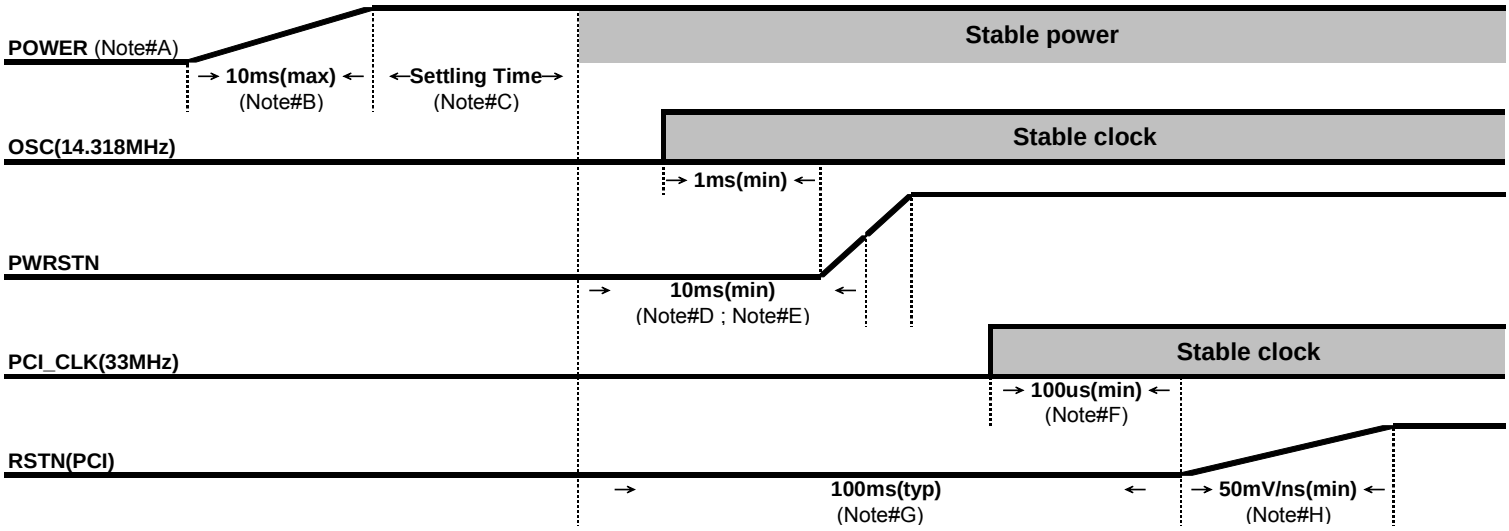
Plat form configurations:		Graphics card information:	
OS	**Windows XP**	Board type	**21M1SDA0F**
Main board	**Asus_P4S800**	Board NO.	**A01**
CPU type	**P4 3.0GHz**	GPU type	**Z9M**
System DRAM	**DDR_4Mx16bit**	Ring0	**19.23**
Chipset	**SiS_648**	Driver version	**V1.09.05**
Dram Part Number	**integrated**	BIOS version	**V1.09.05**
Resolution Setting	**1600*1200_32bit_60Hz**		



The maximum power requirement of each power rail is:

Item	Pin Name	Net Name	Voltage		Current	Power(W)
			ideal	measured(V)	I(mA)	
Power branch for Z9M	IVDD	IVDD	1.80	1.81	332	0.601
	AVDD_DAC1	AVDD_DAC	1.80	1.81	86	0.156
	AVDD_DAC2					
	AVDD_DLL	AVDD_DLL	3.30	3.34	4	0.013
	AVDD_DCLK	AVDD_DCLK	3.30	3.34	10	0.033
	AVDD_MCLK	AVDD_MCLK	3.30	3.34	6	0.020
	AVDD_MDLL	AVDD_MDLL	3.30	3.34	20	0.067
	VDDO	VDDO	3.30	3.34	38	0.127
	OVDD3	OVDD3	3.30	3.34	2	0.007
	OVDD25	OVDD25	3.30	3.34	6	0.020
	OVDDQ + PVDD	OVDDQ + PVDD	3.30	3.34	49	0.164
	VDDM	OVDDM	2.50	2.51	182	0.457
	OVDDM					
					Total	**1.664**

11 Volari™ Z9M Power-On Sequence



Note#A: The nominal power is included several power rails listed as below:

1.8V => IVDD
1.8V => VDDM / OVDDM (apply to DDRII DRAM)
2.5V => VDDM / OVDDM (apply to DDR DRAM)
3.3V => OVDDQ / PVDD / AVDDDLL / AVDDDCLK / AVDDMCLK / AVDDMDLL

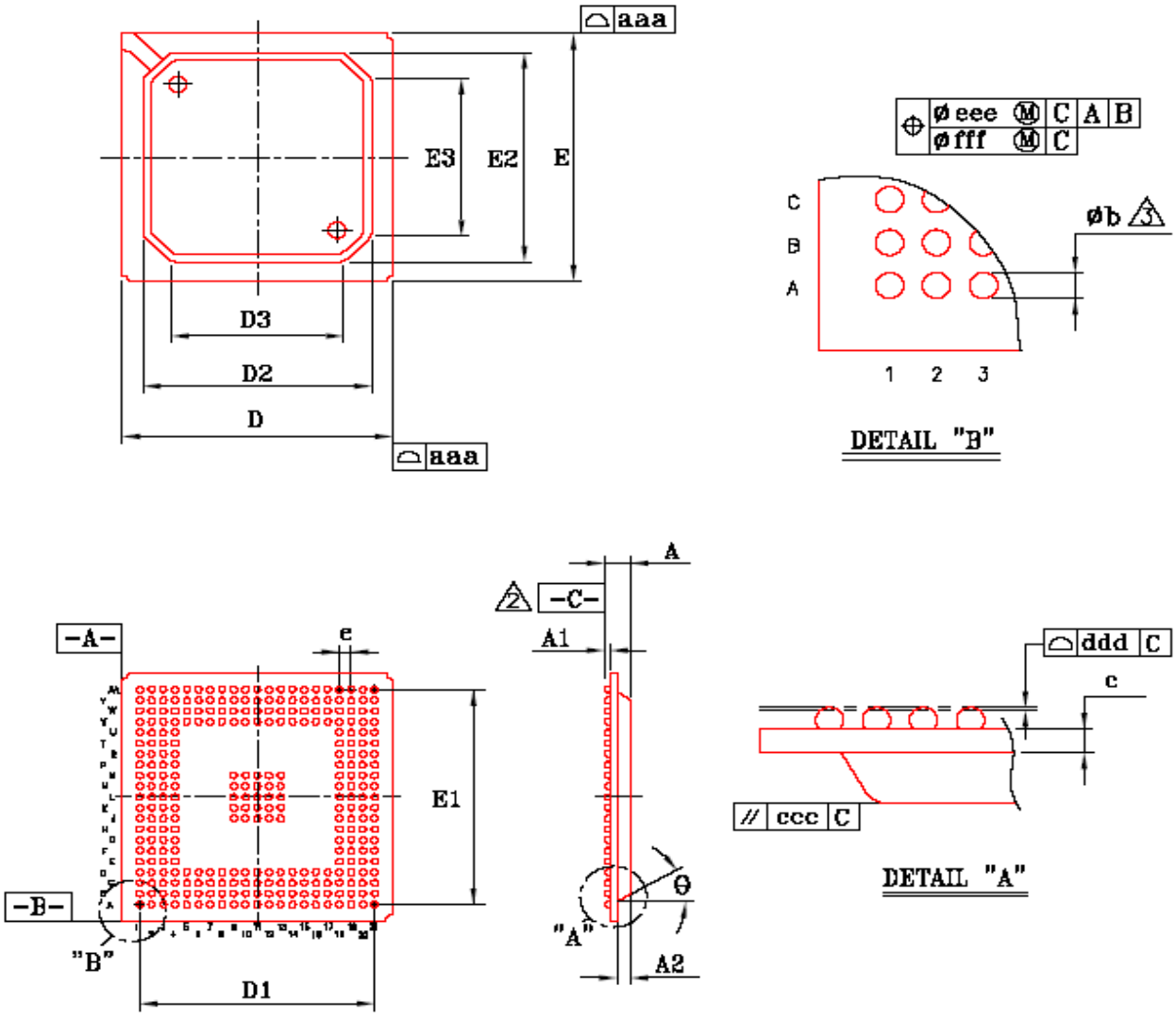
Note#B: It is recommended the all above powers can be rised up within a period, as short as possible.
Note#C: Settling time is defined for above powers meeting the spec.
Note #D: Three points of PWRSTN trigger potential are 10%, 50%, and 90%
Note #E: It doesn't defined PWRSTN slew rate due to the delay time controlled by RC constant.
Note #F: PCI Bus standard, reset active time after CLK stable, please refer to the Table 4-6 (P.134) in the PCI Spec. Rev. 2
Note #G: PCI Bus recommended value , please refer to the Figure 4-12 (P.140) in the PCI Spec. Rev. 2.1
Note #H: PCI Bus standard, RSTN slew rate, please refer to the Table 4-5 (P.133) in the PCI Spec. Rev. 2.1

12 AC Timing Parameters for Digital RGB

Symbol	Parameter	Min	Typ	Max	Units
Tcip	CLK Period	6		40	ns
Fcip	CLK Frequency	25		165	MHz
Tcih	CLK High Time	2.6			ns
Tcil	CLK Low Time	2.9			ns
Tijit	Worst Case CLK Jitter			1	ns
Tshs	Data, DE, VS, HS Setup Time to CLK+ Falling/Rising Edge	0.5			ns
Thhs	Data, DE, VS, HS Hold Time to CLK+ Falling/Rising Edge	0.6			ns
Thde	Data Enable (DE) High Time			8191	Tcip
Tlde	Data Enable (DE) Low Time	128			Tcip
Tddf	VS/HS Delay from DE Falling Edge		1		Tcip
Tddr	VS/HS Delay to DE Rising Edge		1		Tcip

TABLE 12.1-2 AC TIMING PARAMETERS FOR DIGITAL RGB

13 Volari™ Z9M 23 X 23mm Mechanical Dimension



Symbol	dimension in mm			dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	——	2.23	2.43	——	0.088	0.096
A1	0.40	0.50	0.60	0.016	0.020	0.024
A2	1.12	1.17	1.22	0.044	0.046	0.048
b	0.50	0.60	0.70	0.020	0.024	0.028
c	0.51	0.56	0.61	0.020	0.022	0.024
D	22.80	23.00	23.20	0.898	0.906	0.913
D1	——	20.00	——	——	0.787	——
D2	19.30	19.50	19.70	0.760	0.768	0.776
D3	——	14.70	——	——	0.579	——
E	22.80	23.00	23.20	0.898	0.906	0.913
E1	——	20.00	——	——	0.787	——
E2	19.30	19.50	19.70	0.760	0.768	0.776
E3	——	14.70	——	——	0.579	——
e	——	1.00	——	——	0.039	——
aaa	0.20			0.008		
ccc	0.25			0.010		
ddd	0.15			0.006		
eee	0.25			0.010		
fff	0.10			0.004		
θ	30° TYP			30° TYP		

Package Outline

- 23mmx23mm MCMBGA
- Ball Count: 297 balls
- Ball Pitch :1.0 mm