TABLE OF CONTENTS

1. Revision Notes

Being first release, this document describes the SiS6326 Rev. Ax/Bx detailed technical information. All the information contained in this document can only be applied to SiS6326 Rev. Ax/Bx chips.

2. SiS6326 Overview

1 Introduction

Targeting the emerging PC market, SiS6326 is the first member of the new SiS63x6 family, which consists of high integration, super performance, and feature-rich 3D/2D graphics & video accelerators.

Being a 208-pin PQFP package, SiS6326 integrates AGP/PCI VGA controller, 3D/2D graphics accelerator, NTSC/PAL TV-OUT solution, MPEG-2/1 video decoder, and video accelerator. The target of SiS6326 is to meet all the emerging PC requirements which includes 3D acceleration, output to TV, DVD/VCD player, and video acceleration in one chip and in a market acceptable price.

As the first member of 63x6 family, totally new pin-outs and application circuits are developed. However the definition of the registers are designed as backward compatible with previous SiS62x5 as possible as to shorten the product-to-market time.

2 Features

PCI Bus Interface

- **Supports 32-bit PCI local bus standard Revision 2.1 compliant**
- **Supports 66MHz PCI operation**
- **Supports PCI bus master for 3D texture fetch**
- **Built-in write-once subsystem vendor ID configuration register**
- **Supports zero wait-state memory mapped I/O burst write**
- **Built-in 8 stages PCI post-write buffer to enhance frame buffer write performance**
- **Built-in 128 bits read cache to enhance frame buffer read performance**
- **Supports full 16-bit re-locatable VGA I/O address decoding**
- **Supports PCI multimedia design guide Rev. 1.0**

AGP Interface

- **Supports AGP 1.0 compliant configuration setting**
- **Supports AGP 133MHz**

High Performance & High Quality 3D Accelerator

- **Built-in a high performance 3D engine**
  - Built-in 32-bit floating point format VLIW triangle setup engine
  - Built-in texture cache with LRU replacement strategy
  - Supports PCI master and AGP 133 MHz for texture fetch
  - Peak polygon rate: 800K polygon/sec @ 50 pixel/polygon with Gouraud shaded, point-sampled, linear and bilinear texture mapping
  - Peak fill rate: 40M pixel/sec
- **Built-in a high quality 3D engine**
  - Supports solid, flat, and Gouraud shading
  - Supports high quality dithering
  - Supports Z-test, Alpha-test, and scissors clipping test
  - Supports stipple patterns, stipple alpha, line pattern, and ROP
  - Supports Z-buffer and alpha buffer
  - Supports per-pixel texture perspective correction
  - Supports point-sampled, linear, bi-linear, and tri-linear texture filtering
  - Supports MIP structure texture
  - Supports rectangle structure texture
  - Supports 1/2/4 BPP palletize texture
  - Supports 1/2/4/8 BPP luminance texture
  - Supports 4/8 BPP mix mode texture format
  - Supports 8/16/24/32 BPP RGB/ARGB texture format
  - Supports video texture in all supported texture formats. The supported video formats are RGB555, RGB565, and YUV422 formats
  - Supports texture transparency, blending, wrapping, mirror, and clamping
  - Supports fogging, alpha blending, and primitive transparency

High Performance 2D Accelerator

- **Built-in 42 double-words hardware command queue**
- **Supports Turbo Queue (Software Command Queue in off-screen memory) architec-**

ture to achieve extra-high performance (patent pending)

- **Built-in Direct Draw Accelerator**
- **Built-in an 1T 64-bit BITBLT graphics engine with the following functions:**
  - 256 raster operations
  - Rectangle fill
  - Color/Font expansion
  - Enhanced Color expansion
  - Enhanced Font expansion
  - Line-drawing with styled pattern
  - Built-in 8x16 pattern registers
  - Built-in 8x8 mask registers
  - Rectangle Clipping
  - Transparent BitBlt
  - Direct Draw
- **Supports memory-mapped, zero wait-state, burst engine write**
- **Supports burst frame buffer read/write for SDRAM/SGRAM**
- **Built-in 64x64x2 bit-mapped hardware cursor**
- **Maximum 4M Bytes frame buffer with linear addressing**
- **Built-in 4 stages engine write-buffer and 9x64 bits read-buffer to minimize engine wait-state**
- **Built-in 64x32 CRT FIFOs to support super high resolution graphics modes and reduce CPU wait-state**

Complete TV-OUT Solution

- **Built-in complete NTSC/PAL video encoder**
  - Built-in 3-Channel 10-bit DAC with power down mode
  - Built-in 3-line anti-flicker filter
  - Built-in TV sense circuits for auto detect TV connection
  - Supports RCA-style composite video and S-Video outputs
  - Supports loadable RAMDAC for gamma correction in high color and true color modes
  - No external TTL or DAC required
- **Supports NTSC/PAL interlaced display in**
  - 640x480x60Hz and 640x400x60Hz modes for NTSC
  - 640x480x50Hz and 800x600x50Hz modes for PAL
  - low resolution modes for both NTSC and PAL (hidden)
- **Supports non-interlaced scan, output either even or odd lines**
- **Supports 4 types of filtering mode: mild, medium, strong, and adaptive**
- **Supports VGA and TV simultaneous output**
- **Supports TV image positioning by hardware**
- **Supports under-scan and over-scan scaling**

MPEG-2/1 Video Decoder

- **MPEG-2 ISO/IEC 13818-2 MP@ML and MPEG-1 ISO/IEC 11172-2 standards compliant**
- **Low cost design based on MPEG macro-block layer decoding architecture**
  - Built-in run length and zig-zag decoder
  - Built-in IDCT logic

- Built-in motion compensation logic

- **14 bits resolution in IDCT transformation**
- **Half pixel resolution in motion compensation**
- **Built-in two 196x64 video line buffers for MPEG video playback**

Video Accelerator

- **Supports single frame buffer architecture**
- **Supports YUV-to-RGB color space conversion**
- **Supports bi-linear video interpolation with integer increments of 1/64**
- **Supports graphics and video overlay function**
  - Independent graphics and video formats
  - 16 color-key and/or chroma-key operation
  - 3-bit graphics and video blending
  - Rectangular video window modes
- **Supports current scan line of refresh read-back**
- **Supports tearing free double buffer swapping**
- **Built-in video decoder interface**
  - Philips SAA7110/SAA7111
  - Brooktree BT815/817/819A (8-bit SPI mode 1,2)
- **Supports VMI to connect VMI devices**
  - Shares VMI control and data bus with MD bus
- **Supports Vertical Blank Interrupt**
- **Supports RGB555, RGB565, YUV422, and YUV420 video format**
- **Built-in 64x16 video capture FIFOs to support video capture**
- **Built-in two 196x64 video playback line buffers**
- **Supports DCI Drivers**
- **Supports Direct Draw Drivers**

Display Memory Interface

- **Supports FP, EDO, one-cycle EDO, SDRAM, and SGRAM timing**
- **Supports 1MB, 2MB, and 4MB memory configurations**
- **Supports 256Kx4, 256Kx8, and 256Kx16 FP and EDO DRAM types**
- **Supports 2-CAS/1-WE DRAM and EDO DRAM types**
- **Supports 256Kx32 SDRAM and SGRAM types up to 83.3 MHz**
- **Supports 32/64-bit display memory path**
- **Supports auto memory size detecting**

High Integration

- **Built-in programmable 24-bit true-color RAMDAC up to 175MHz pixel clock**
  - Built-in reference voltage generator and monitor sense circuit
  - Supports loadable RAMDAC for gamma correction in high color and true color modes
- **Built-in dual-clock generator**
  - Integrates PLL loop filter
- **Built-in 14.318 MHz oscillator circuits**
- **Built-in two 196x64 video line buffers for MPEG video playback**
- **Built-in standard feature connector logic support**

- **Built-in PCI multimedia interface**

Resolution, Color & Frame Rate

- **Supports 175 MHz pixel clock**
- **Supports super high resolution graphics modes**
  - 640x480 256/32K/64K/16M colors 85Hz NI
  - 800x600 16/256/32K/64K/16M colors 85Hz NI
  - 1024x768 16/256/32K/64K/16M colors 85Hz NI
  - 1280x1024 16/256/32K/64K colors 75 Hz NI
  - 1600x1200 16/256 colors 65Hz NI
  - low resolution modes (hidden)
- **Supports virtual screen up to 2048x2048**
- **Supports 80/132 columns text modes**

Power Management

- **Supports VESA Display Power Management Signaling (DPMS) compliant VGA monitor for power management**
- **Built-in 30 min. standby and suspend timers with keyboard, hardware cursor, and/or video memory read/write as activation source**
- **Supports direct I/O command to force graphics controller into standby/suspend/off state**
- **Power down internal SRAM in direct color mode**
- **Built-in a low power signal pin for supporting external power down controller**

Multimedia Application

- **Supports DDC1 and DDC2B specifications**
- **Supports RAMDAC snoop for multimedia applications**

Miscellaneous

- **Only 3 ICs (including DRAMs) required to implement a PCI true-color graphics adapter without any TTLs**
- **Supports 64K Bytes ROM decoding**
- **Supports Signature Analysis for automatic test**
- **Implemented by 3.3V CMOS technology with 5.0V tolerance I/O buffers**
- **208-pin PQFP package**

3 Block Diagram

.1 SiS6326 System Block Diagram

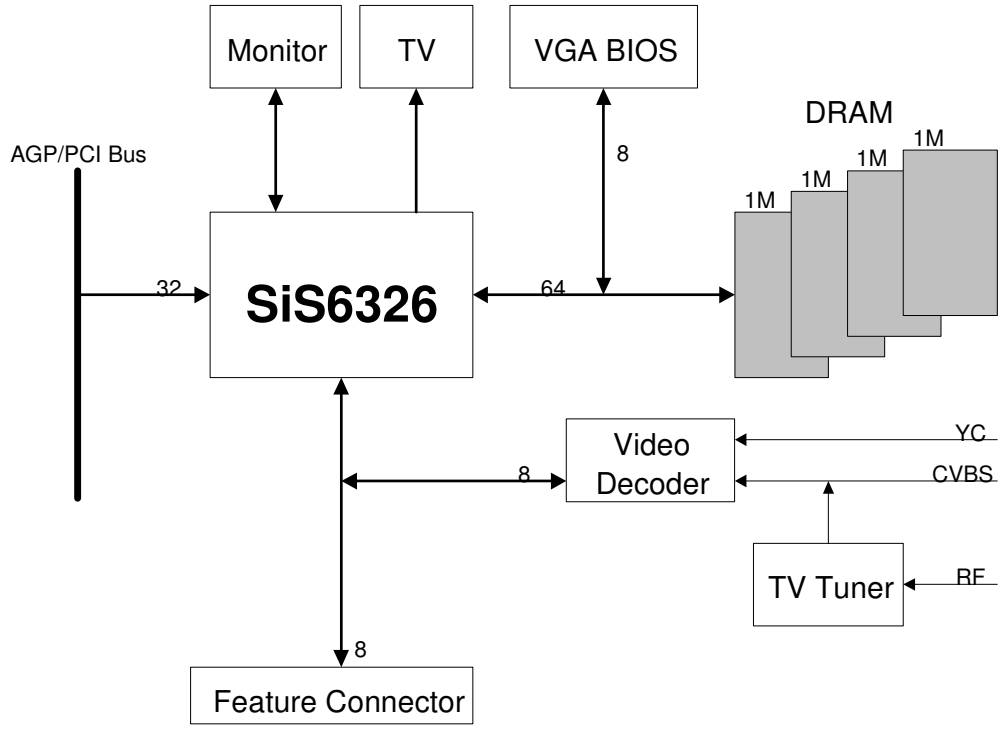


Figure 2.1

.2 SiS6326 Block Diagram

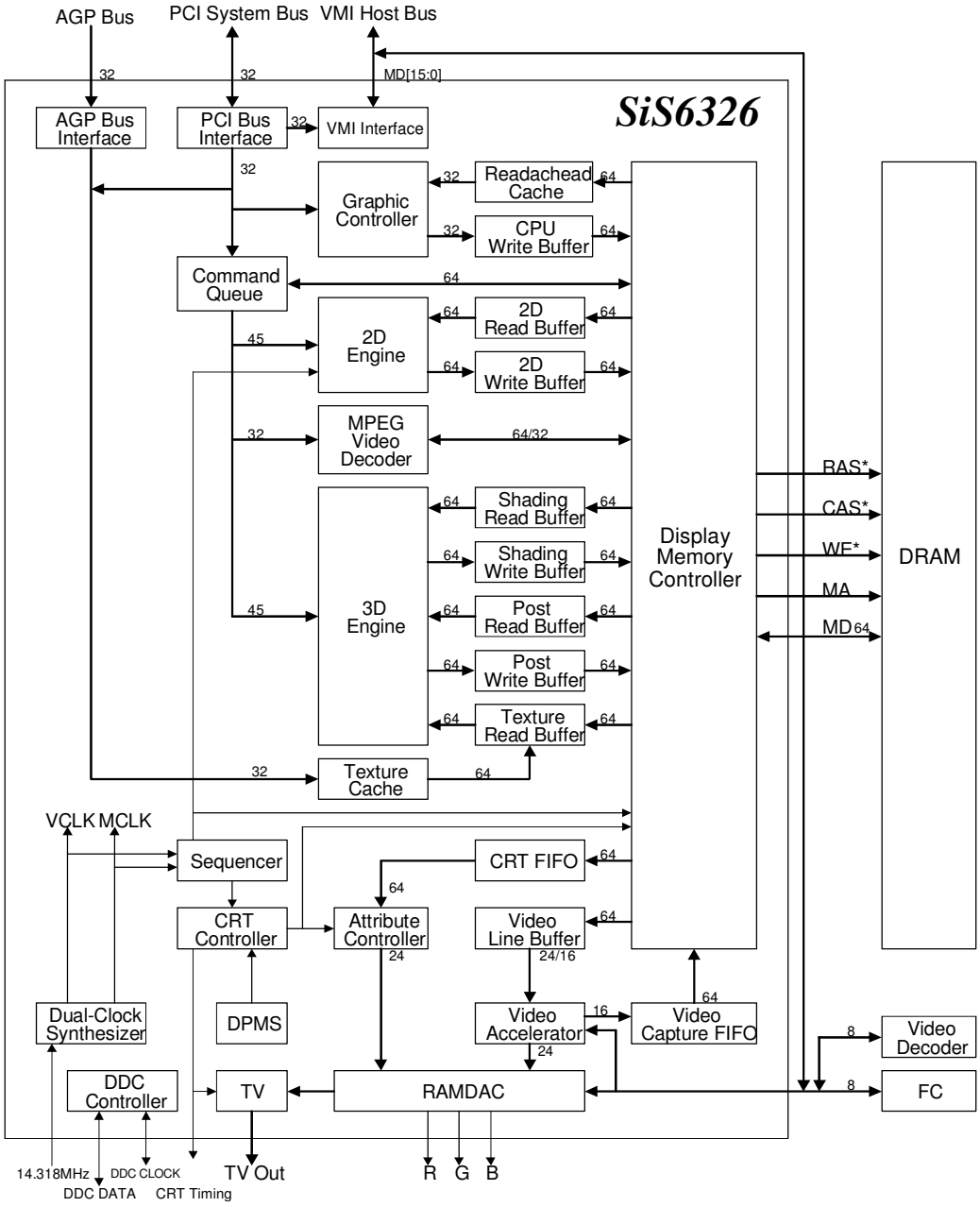


Figure 2.2

.3 SiS6326 3D Engine Block Diagram

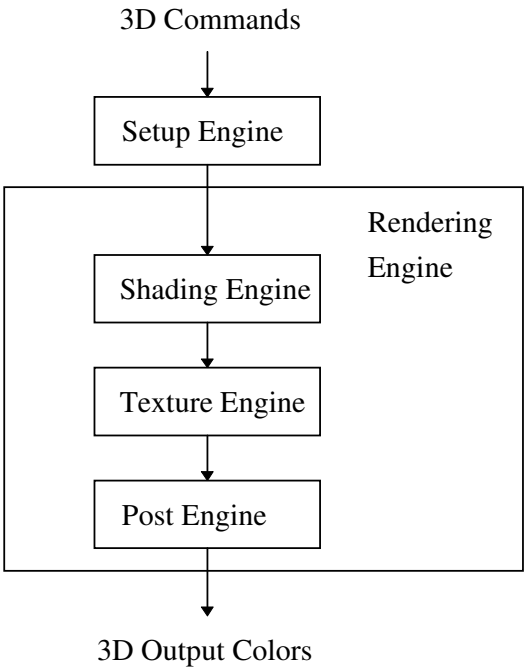


Figure 2.3

.4 6326 MPEG Video Decoder Block Diagram

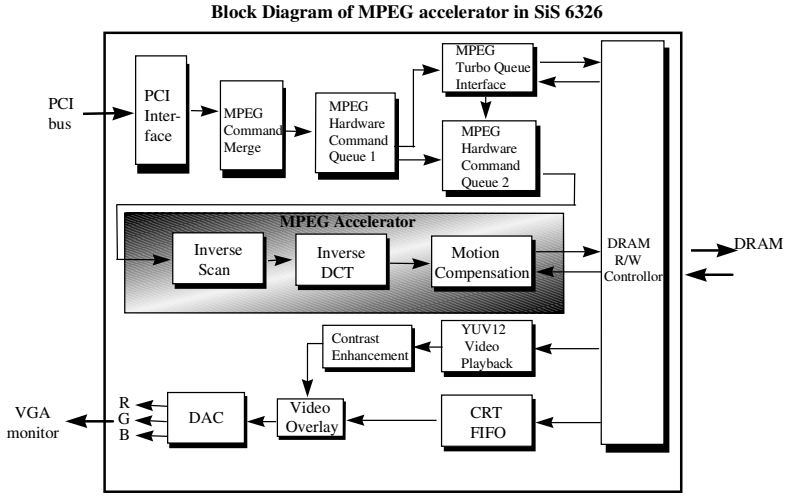


Figure 2.4

.5 6326 TV-OUT Block Diagram

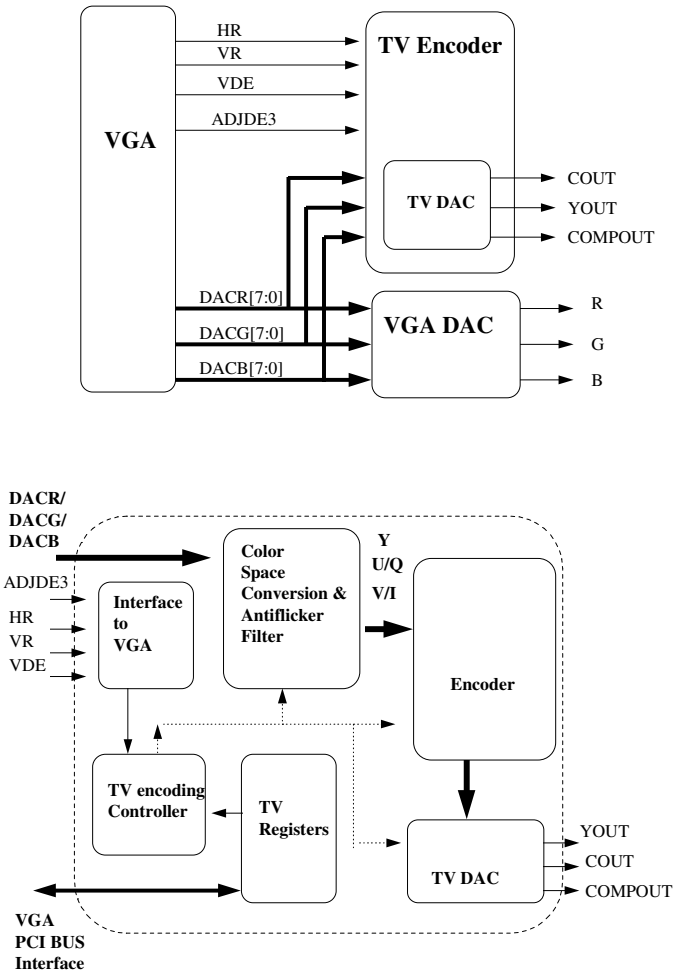


Figure 2.5

3. Function Description

1 Highlight Function Blocks

.1 2D Graphics Engine

Basically the 2D graphics engine of SiS6326 is a 64-bit BitBlt graphics engine. However SiS6326 makes a tremendous performance improvement in the 2D engine design than its previous generation in SiS62x5 series.

The most critical design improvement is the engine throughput enhancement. Basically, the 2D engines of SiS62x5 series are classified as 2T architecture. This means it needs two memory clocks to generate one pair of address and data for video memory update. This design architecture could maintain a balanced throughput in fast page and two-cycle EDO DRAM configuration. But for one-cycle EDO and SGRAM configuration, 2T engine is an unbalanced design and 1T engine is the only reasonable architecture migration path. SiS6326 does integrate a new developed 1T graphics engine. So it could outperform its previous generation in SGRAM and one-cycle EDO configuration. For fast page and two-cycle EDO DRAM configurations, significant performance jump could also be expected.

Furthermore SiS6326 improves much timing efficiency in Turbo Queue design. The source FIFO capacity is also double. This could improve performance in screen-to-screen related graphics operations. In the mean time, the PCI engine command burst write is also improved from 3T to 1T.

For enhanced 256-color graphics mode, the engine supports the following functions:

- 256 raster operations
- Rectangle fill
- Color/Font expansion
- Enhanced Color expansion
- Line-drawing with styled pattern
- Built-in 8x16 pattern registers
- Built-in 8x8 mask registers
- Rectangle Clipping
- Transparent BitBlt
- Direct Draw

For 32K or 64K high-color graphics mode, the engine supports the following functions:

- 256 raster operations
- Rectangle fill
- Color/Font expansion
- Enhanced Color expansion
- Line-drawing with styled pattern
- Built-in 8x16 pattern registers
- Built-in 8x8 mask registers
- Rectangle Clipping
- Transparent BitBlt
- Direct Draw

For 16M-color graphics mode, due to different graphics process methods, the engine supports the following functions:

- Source/Destination BitBlt
- Pattern/Destination BitBlt
- Color/Font Expansion

For detail descriptions of the graphics engine functions, please refer to "1 2D Graphics Engine" on Page 15.

.2 3D Accelerator

Targeting on Direct3D acceleration, SiS6326 achieves extremely high fill and polygon rate in high quality with a highly balanced pipeline 3D architecture. The major key technologies that guarantee a high 3D performance are the integrated Turbo Queue, Setup Engine, Texture Cache, and Pipeline Render Engine.

For more detail description about the 3D engine, please refer to “2 3D Acceleration” on Page 20.

.3 TV-OUT Video Encoder

SiS6326 integrates a complete and high quality NTSC/PAL video encoder with the capability of simultaneously display on both TV and VGA monitor. SiS6326 video encoder supports NTSC and PAL standards and integrates video DACs, anti-flicker circuits, and composite and S video sense circuits.

SiS6326 supports the following resolutions in TV outputs. For NTSC system, they are 640x400 @ 60 Hz and 640x480 @ 60 Hz for NTSC system. For PAL system, they are 640x480 @ 50Hz and 800x600 @ 50Hz are supported. Furthermore for all low resolution modes, SiS6326 supports TV output function for both NTSC and PAL. All these resolutions meet the Microsoft OS requirements. Under-scan, over-scan, and TV centering functions are available by registers programming.

For detail description about the TV-OUT video encoder, please refer to “12 TV-OUT Technology” on Page 34.

.1 TV-OUT DAC

The TV-OUT block built-in a 3-channel 10-bit DAC. User can connect the encoder output DAC to the composite and S-Video decoder (e.g. TV or VCR) at the same time.

To save power consumption, power-down mode is automatically set when TV encoder senses no device is attached to the TV DAC output. The electrical characteristics of TV DAC will be described latter.

.4 MPEG-2/1 Video Decoder

SiS6326 integrates an MPEG video decoder that supports both MPEG-2 and MPEG-1 video standards. Basically, this MPEG video decoder is a macro-layer decoder that takes about 80% MPEG video decoding computing power and let the left 20% done by CPU. Therefore the scheme used in SiS6326 is the most economic and efficient design approach and maintains much design flexibility. DVD video standard is under the coverage of this silicon de-

sign. It costs not much silicon area but significantly reduces CPU loading than that in pure software MPEG video decoder. What CPU has to do in video decoding are syntax parsing, variable-length decoding, and inverse quantization. All the other video tasks will be done by SiS6326.

For MPEG or AC3 audio decoding, it would count on CPU computing power or an external MPEG or AC3 audio decoder option.

In the process of MPEG video decoding, SiS6326 would allocate four image buffers in off-screen area. These four image buffers are for I-picture, P-picture, B-picture (under rendering), and one additional B-picture (under displaying). For MPEG-1 decoding, it takes about 490K bytes. For MPEG-2 decoding, It takes at least 1980K bytes off-screen memory.

In order to support MPEG-2 video overlay, SiS6326 doubles its video line buffer length with total capacity up to 720x16x2 bits.

For detail description about the MPEG video decoder, please refer to "11 MPEG Decoder" on Page 32.

.5 Video Accelerator

SiS6326 video accelerator could work in four different modes: standard FC (feature connector) mode, direct video mode, VMI interface mode, and PCI multimedia mode.

In standard FC mode, SiS6326 supports standard FC operation.

In direct video mode, SiS6326 could work with the Philips SAA7110 / SAA7111 and Brooktree Bt815/817/819A (8-bit SPI mode 1, 2) to provide the PC-Video solution. After receiving the video data, SiS6326 would perform scaling and store these video data to display memory. Furthermore SiS6326 would perform color-space conversion, interpolation, and scaling on the stored video data before overlaying with graphics data for final display.

In VMI interface mode, SiS6326 could connect to some VMI devices.

In PCI multimedia mode, SiS6326 supports PCI multimedia design specification to meet future potential trend.

For detail description about the video accelerator, please refer to "10 Video Accelerator" on Page 27.

.6 AGP/PCI Bus Interface

SiS6326 connects directly to the PCI or AGP bus with no glue logic, and it decodes the 32-bit address and responds to the applicable control lines. It could execute both I/O and memory access as an 8-, 16-, 32-bit device.

For detail description about the AGP/PCI bus interface, please refer to "3 AGP/PCI Bus Interface" on Page 21.

.7 Display Memory Controller

The Display Memory Controller generates timing for display memory. It can support the following DRAM timing:

- Fast Page (FP) DRAM

- Normal (2-cycle) EDO DRAM
- One cycle EDO DRAM
- SDRAM
- SGRAM

For both fast page DRAM and EDO DRAM (1-cycle or 2-cycle), it can support 256Kx4, 256Kx8, and 2-CAS/1-WE 256Kx16 types.

For detail description about the display memory controller, please refer to "6 Display Memory Architecture" on Page 23.

.8 VMI

SiS6326 built-in VMI (Video Module Interface) Specification version 1.4 compliant interface. Since VMI interface signals are multiplexed with MD bus in SiS6326, therefore there would be two TTLs added when implementing VMI interface on the board.

SiS6326 can be programmed to supports both mode A and mode B for host port interface. It contains a 128-bit FIFO post-write buffer and 32-bit read-cache.

For detail description about the VMI spec, please refer to the "VMI Specification Version 1.4".

For how to implement VMI interface in SiS6326 board, please refer to related application circuits released by SiS.

2 Other Function Blocks

.1 Attribute Controller

The Attribute Controller formats the display for the screen. Display color selection, text blinking, alternate font selection, and underlining are performed by the Attribute Controller.

.2 CRT Controller

The CRT Controller generates the HSYNC and VSYNC signals required for the monitor, as well as BLANK* signals required by the Attribute Controller.

.3 CRT FIFO

The 64x64 CRT FIFO allows the Display Memory Controller to access the display memory for screen refresh at maximum memory speed rather than at the screen refresh rate. It provides 3 programmable thresholds - CRT/CPU Threshold Low, CRT/CPU Threshold High, and CRT/Engine Threshold High. With adequate programming these three thresholds, the CPU wait-time would be reduced to improve the graphics performance.

.4 DDC Controller

The DDC Controller provides two different channels to communicate with the monitor which supports DDC level 1 or DDC level 2B. One is DDC CLK channel which is bi-directional and provides the clock for DDC. The other is DDC DATA channel which is bi-directional and could query some information from monitor.

With the advantage of DDC, VGA BIOS could realize the capability of the connected monitor and take adequate action (such as to program the parameters for higher frame rate, ..., etc.) to make end users feel more comfortable.

.5 DPMS

It provides some registers to control the CRT timing to be compatible with the VESA DPMS specification. (For detail description, please refer to "8 Power Management" on Page 26.)

.6 Dual-Clock Synthesizer

The Dual-Clock Synthesizer generates MCLK and VCLK with single external reference clock. With this character, we could set the MCLK at the maximum speed which the display memory could work normally, thus it takes the advantage of the real peak memory bandwidth and improves the graphics performance. (For detail description, please refer to "7 Internal Dual-Clock Synthesizer" on Page 25.)

.7 Graphics Controller

It performs text manipulation, data rotation, color mapping, and miscellaneous operations.

.8 Graphics & Video RAMDAC

The RAMDAC contains the color palette and 24-bit true color DAC.

The color palette, with 256 18-bit entries, converts a color code that specifies the color of a pixel into three 6-bit values, one each for red, green, and blue.

The 24-bit true color DAC is designed for direct color graphics mode. It converts each digital color value to three analog voltages for red, green, and blue.

.9 Read-ahead Cache

It is a 128-bit cache. With this cache, the times of the operation of display memory read would be reduced, thus increase the performance.

.10 Write FIFO

The Write FIFO contains a queue of CPU write accesses to display memory that have not been executed because of memory arbitration. With this queue, the SiS6326 will release CPU as soon as it records the address and data, and then write into display memory when the display memory is available. Thus CPU performance is increased.

4. Technical Description

1 2D Graphics Engine

It is an enhanced 1T 64-bit BitBlt Graphics Engine.

For enhanced 256-color graphics mode, the engine supports the following functions:

- 256 raster operations
- Rectangle fill

- Color/Font expansion
- Enhanced Color expansion
- Line-drawing with styled pattern
- Built-in 8x16 pattern registers
- Built-in 8x8 mask registers
- Rectangle Clipping
- Transparent BitBlt
- Direct Draw

For 32K or 64K high-color graphics mode, the engine supports the following functions:

- 256 raster operations
- Rectangle fill
- Color/Font expansion
- Enhanced Color expansion
- Line-drawing with styled pattern
- Built-in 8x16 pattern registers
- Built-in 8x8 mask registers
- Rectangle Clipping
- Transparent BitBlt
- Direct Draw

For 16M-color graphics mode, due to different graphics process methods, the engine supports the following functions:

- Source/Destination BitBlt
- Pattern/Destination BitBlt
- Color/Font Expansion

Descriptions of the graphics engine functions are summarized as follows:

Bit Block Transfer (BitBlt)

BitBlt moves a block of data from one location (source) to another location (destination). It is a ternary operation. The operands could be the source data, the destination data, and the brush pattern. There are three different kinds of BitBlt: from the host memory to the display memory, from the display memory to the host memory, and from one location of the display memory to another location of the display memory.

In the first two cases, the operation simply uses the "move string instruction" (REP MOVS) to move the source data to the destination to accomplish the BitBlt operation. It is called "CPU-driven BitBlt".

In the case of moving from the display memory to the display memory, integrated Graphics Controller could gain the advantage of its advanced engine design to solve the problems of memory overlapping during the block transfers. The only effort is to program the adequate parameters.

BitBlt with Mask

When the BitBlt operation deals with the hatched brush pattern, the programmer just needs to set the monochrome mask into Mask Registers and program an adequate BG ROP and Background Color, then the engine would handle the complicated process.

Color/Font Expansion

The color/font expansion is used to expand a monochrome data (one bit per pixel) into a second color format which is n-bit per pixel during a moving operation.

The foreground color and background color is addressed respectively from I/O address 8290h to 8292h and from I/O address 8294h to 8296h. The font patterns are stored in the pattern registers (I/O address 82ACh to 82EBh) or in the off-screen memory which is called Enhanced Color/Font Expansion. These pattern registers store the monochrome bitmap. The BitBlt engine can expand 512 pixels at a time. Thus the font-drawing and monochrome bitmap expansion can be easily accomplished.

Enhanced Color Expansion

If the size of a monochrome bitmap is larger than 512 pixels, there is not enough space in pattern registers to store this bitmap. In this case, the bitmap should be stored in the off-screen display memory instead of the pattern registers. The operation is called Enhanced Color Expansion or Enhanced Font Expansion depended on the data format.

The format written into the off-screen memory of the Enhanced Color Expansion operation is m x n.

When the Command 1 Register D[5] (Enhanced Color Expansion Enable Bit, I/O address 82ABh) is set to 1, the Enhanced Color Expansion mode is enable. The SRC Start Linear Address (I/O address 8280h to 8282h) is used to specify the starting address of the off-screen memory. Integrated Graphics Controller stores the monochrome bitmap into the assigned off-screen memory. Therefore the BitBlt engine could expand more pixels using the Enhanced Color Expansion.

Font Expansion

The Font Expansion is very similar to the Enhanced Color Expansion. The major difference is the format stored in the off-screen memory. The format written into the off-screen memory of the Enhanced Font Expansion operation is 8 x n.

When the Command 1 Register D[4] (Font Expansion Enable Bit, I/O address 82ABh) is set to 1, the Font Expansion mode is enable. The SRC Start Linear Address (I/O address 8280h to 8282h) is used to specify the start address of the off-screen memory. Integrated Graphics Controller stores the monochrome bitmap into off-screen memory byte by byte successively. Therefore the BitBlt engine would expand these pixels using the Font Expansion.

Line Drawing

The Bresenham's Line Algorithm is a well popular algorithm in graphics, which is used to draw a line. The drawing line could be either a solid line or a dashed line. To draw a solid line, we must use one solid foreground color. To draw a dashed line, we'll use two colors specified by the foreground and background color registers. There are several registers involved to control the starting location, pixel count, error term, and line style, etc.

Rectangle Fill

A rectangle area fill is a function to fill a specified rectangle area by using either a solid color (rectangle fill) or a pattern (pattern fill).

Rectangle Fill is simply to fill the destination rectangle with a solid color. The solid color is specified into the foreground color register.

Pattern Fill repeats a source pattern into a destination rectangle. Therefore the pattern registers (I/O address 82ACh to 82EBh) must be specified. The pattern often consists of a background and foreground color because the color expansion would be used in conjunction with the pattern fill.

Raster Operations (Raster Ops or ROPs)

Raster Ops would perform some logical or arithmetic operations on the graphics data. There are 256 raster ops defined by Microsoft. Each raster op code is a Boolean operation with three operands: the source, the selected pattern, and the destination.

Direct Draw

The Windows 95 Game SDK enables the creation of world class computer games. Direct Draw is a component of that SDK that allows direct manipulation of video display memory. In order to enhance the performance of games, SiS6326 provides some Direct Draw functions.

Since the former engine functions can just support part of Direct Draw capabilities, three new functions are added into the graphics accelerator in order to meet the other Direct Draw functions. They are color key range comparison, alpha blending, and Direct Draw raster operation.

The register format for Direct Draw is different from those of the engine's functions listed above.

To enable Direct Draw, the Direct Draw enable bits (refer to ".3 Register Format for Direct Draw: Command Register 0 D[3:2]" on page 115) must be set to "11". Once Direct Draw is enabled, all of the engine operations are under the "Read-Modify-Write" mode. That is, the destination data have to be read from memory for processing before being written back.

After receiving the destination data, the source and destination data are sent to the color key range comparators to determine whether they are between the high and low color key values. If they are in the color key range, the Direct Draw raster operation (D_Rop) will determine whether the data after alpha blending or the original destination will be written back to memory.

There are two control bits for alpha blending. They are the S_Alpha bit (refer to "Alpha Blending Control Bit for Source Color" on page 113.) and D_alpha Bit (refer to "Alpha Blending Control Bit for Destination Color" on page 113.). The table below shows the relationship between these two control bits and the data after alpha blending.

S_Alpha	D_Alpha	Data after Alpha Blending
0	0	Source
0	1	Destination
1	0	Source
1	1	(Source + Destination)/2

.1 Turbo Queue in 2D Graphics Engine

In SiS6326, the graphics engine performs the acceleration functions as stated in the previous section via the acceleration commands stored in the command queue. The command queue is a FIFO (First In First Out) and ring structure. i.e. If an acceleration command is filled in the

last stage of the command queue, then the following acceleration command would be filled in the first stage of the command queue.

Once this command queue is congested, the CPU's request will be pending until the command queue has free space to accept more acceleration commands. This would downgrade the graphics system performance severely. Thus the length of command queue will dominate the performance of the graphics engine.

To lengthen the command queue as long as required, SiS6326 provides two different kinds of command queue. The first one is built in SiS6326, which is called *Hardware Command Queue*. The other one is built in the off-screen display memory, which is called *Turbo Queue* and is patent owned by SiS. The architecture diagram of SiS6326 command queue is as follows.

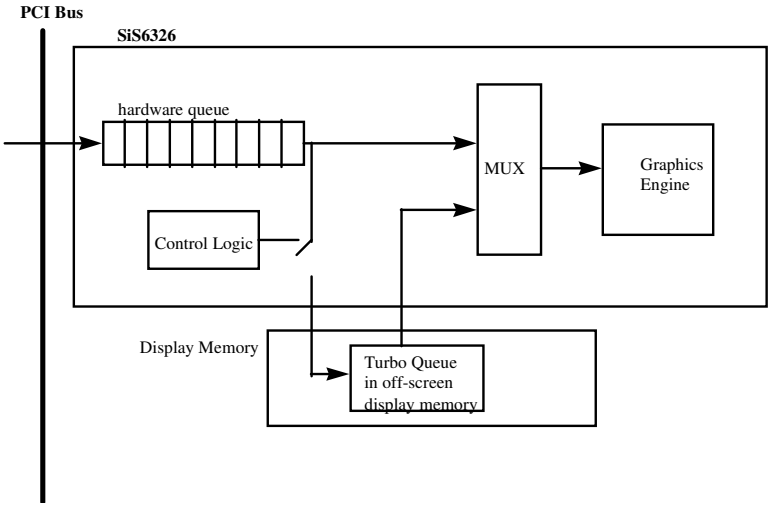


Figure 4.1

The Hardware Command Queue is a 42 double-words queue. And there are 30K Bytes off-screen memory space reserved for the Turbo Queue. Since the average length of an engine command is 8 double-words (which is called 1 stage), therefore the SiS6326 command queue could be regarded as infinity stages with Turbo Queue and could get rid of the CPU waiting issue to get extra high performance.

When the hardware command queue is going to be full, the head commands would be moved to the Turbo Queue and left hardware queue space for new PCI commands. The command queue architecture makes the transmission of SiS6326 PCI commands most efficient.

The Turbo Queue is also a FIFO and ring structure as stated before. The Turbo Queue base address is generally set to the last 32K Bytes segment on off-screen. To program the extended register SR2C (Turbo Queue Base Address Register) could allocate the Turbo Queue into the off-screen region of the display memory automatically.

2 3D Acceleration

The major technologies for the high performance and high quality 3D rendering in SiS6326 are:

- Turbo Queue
- Setup Engine
- Texture Cache
- Pipeline Rendering Engine

.1 Turbo Queue in 3D Accelerator

Using the Turbo Queue architecture (*SiS patent pending*) will speedup the rendering for 3D engine. The Turbo Queue length is virtually infinite, therefore 3D driver can issue commands without waiting. To save the high cost for building a long enough hardware command queue, 6326 allocates a portion of the off screen memory as the command queue buffer. Once 6326 detects the status of the internal hardware command queue nearly full, some of the commands in the hardware queue will be temporally swapped to the off-screen area. When 2D or 3D engine finishes previous command, these off-screen commands will be read back first as the next command for execution.

In 6326 architecture, 2D and 3D engines share the same hardware queue and off-screen command queue but only one engine is active at a time. In this way, we can guarantee a correct execution sequence.

.2 Setup Engine

Setup Engine is one of the most critical parts in the new generation 3D design. It calculates and prepares all of the parameters for primitive drawing. All these computations need more than hundreds of addition, subtraction, multiplication, and division. If we do this setup calculation by host CPU, the sequential coding and processing forms a bottleneck for 3D rendering.

To off-load this computation time from host CPU and to do it in parallel, SiS6326 integrates a VLIW-like 32-bit floating point Setup Engine. It can finish all of the setup computations for a triangle within 60 memory clocks. This should be 10 times faster than the computing power from Pentium-200 CPU. Moreover, Setup Engine also supports line and point setup calculations with much less memory clocks than triangle setup required. This Setup Engine, specially designed to fit all the data formats in Microsoft Direct3D API, can accept vertex values directly in floating point format.

Once Setup Engine finishes the setup computations for a triangle, it transfers all these parameters to Render Engine within one memory clock. While Rendering Engine is busying drawing a triangle, Setup Engine can calculate the parameters needed for the next one.

.3 Rendering Engine

Rendering Engine is a pipeline structure engine in SiS6326. This engine is formed by Shading Engine, Texture Engine, and Post Engine.

The output of Shading Engine is a series of pixel color which represents the shade of a primitive. Texture Engine is responsible for attaching the texture color on a pixel. Then, Post Engine will do some operations such as fogging, alpha blending, dithering, and ROP for this pixel.

In order to support high quality texture mapping, SiS6326 supports point-sampled, linear, bilinear, and tri-linear texture filtering. With an integrated high-capacity texture cache, SiS6326

can render texture pixels in the same fill rate no matter point-sampled, linear, or bi-linear texture filtering method is in used. For tri-linear texture mapping, half fill rate is achieved. But better video quality is expected rendering in tri-linear texture mapping mode.

.4 Texture Cache

Texture Cache is one of the critical part of high performance 3D design. Most of the 3D chips have not built-in texture cache and need to fetch each texture pixel again and again during the rendering process. If the texture is in used for several times, there is no reason to fetch texture from memory again and again. Built-in texture cache could significantly improve texture mapping performance.

With built-in texture cache, each time when a texture miss happens, a segment of texture will be read from texture buffer and stored in a internal texture cache line. Replacement policy is based on LRU (Least Recently Used) algorithm to optimize the texture cache hit rate. Under Direct3D benchmark, more than 90% hit rate has been measured. The texture buffer can locate in off screen area or system memory. If you need very large texture buffer size, the location in system memory is suggested.

.5 Conclusion

The introduction of SiS6326 means the beginning of the new generation of 3D accelerator and the end of low-end, unbalanced 3D solutions. To achieve a high performance in 3D rendering, several strategies have to be used. Turbo Queue, Setup Engine, Rendering Engine, and Texture Cache will become the uncompromising choice in high performance 3D architecture.

3 AGP/PCI Bus Interface

In 3D application (especially in 3D games), the memory space (size) storing texture data is unexpected since it's up to how many textures and how delicate texture the application programs want to create. And as the market request more and more delicate image, we may expect the texture buffer (texture memory) would be increased very fast. i.e. The 3D board's cost would rise and rise due to install more and more memory on the board.

To limit the 3D board's cost and save user's money and without down-grading the performance, SiS6326 supports AGP architecture and allows locating texture buffer in system memory. This memory sharing is based on a dynamic scheme (i.e. You may free the memory space if you won't need them.) and will not impact system performance when 3D applications are not active. Even when 3D application is active, it would only be little impact. Especially in SiS6326, with built-in texture cache, it would be almost no impact. Why?

For texture buffer operation, it is a read-only operation for 3D engine (write is performed by CPU) and read is faster than write and read / write mix operation in PC environment. Therefore we may expect fetching texture from AGP read would only be little impact of performance. Furthermore with SiS6326 built-in texture cache, it may be regarded as one time read event in most cases. Therefore it almost won't affect performance.

Basically, SiS6326 only supports texture buffer sharing with system memory. Back buffer and z-buffer sharing with system memory are not supported since they are not good candidates. Why? For both back buffer and z-buffer operations, they both read and write quite frequently. That means they would compete with CPU access system memory very often and

therefore pull-down quite lot system performance.

Due to the limited pin counts in a 208 pins PQFP package, SiS6326 could not support sideband signals in AGP bus design. However with SiS6326 texture cache, sideband signaling is not important.

With SiS6326 internal texture cache, the texture fetch from AGP bus may be regarded as one time read event in most cases since the cache hit would be normal case. Therefore it may release most AGP bus loading and would not impact AGP performance even lack of sideband signaling. Only texture miss conditions would require extra AGP transactions and it's expect to be seldom.

SiS6326 can support AGP 2X transfer mode, i.e. 133MHz texture read bus speed. All the AGP pinouts sequence is designed to fit AGP connector design to reduce trace length and improve signal quality. An external reference voltage should be generated by low source impedance voltage divider and by 0.4 Vddq, which is required for differential input buffers of AD and AD_STB pins.

In addition to AGP Bus, SiS6326 supports 32-bit PCI local bus standard Revision 2.1. Ahead of previous generation chips, SiS6326 supports PCI master operation, 66MHz PCI, and PCI burst write to take advantage of PCI bus advanced feature to further improve performance. But PCI burst read is not supported since it has very little impact on performance in graphics application.

4 BIOS ROM

SiS6326 follows the one-load-per-slot specification of PCI standard Revision 2.1. The address bus of BIOS ROM are multiplexed with MD[15:0] and the data bus are multiplexed with MD[23:16]. Note that this solution is without glue logic.

SiS6326 could decode 40K/48K/56K/64K Bytes ROM space. It would be very flexible for customers to design their own display BIOS and also save memory space in the whole system.

5 Configuration Pins Definition

The MD[16:32] pins are designed to be power-on configuration pins and should be used very carefully as not to make any troubles.

The following table describes the definition of these configuration pins.

	Function	**0 (default, without pull-up)**	**1 (with pull-up resistor)**
MD16	I/O Address Select	3C3h	46E8h
MD17	VGA Enable/Disable	Controlled by system BIOS	Forced to disable
MD18	Select NTSC/PAL	NTSC	PAL
MD19	Reserved for BIOS	0	1
MD20	AGP Bus	Disable	Enable
MD21	AGP 2X Transfer Mode	Disable	Enable
MD22	Clock Generator Select	Internal	External

MD23	64K ROM Decoding	Disable	Enable
MD24	DRAM Types Select 0	0	1
MD25	DRAM Types Select 1	0	1
MD26	BIOS ROM Decoder	Enable	Disable
MD27	INTA#	Disable	Enable
MD28	VMI	Enable	Disable
MD29	DRAM Speed Set 0	0	1
MD30	DRAM Speed Set 1	0	1
MD31	DRAM Speed Set 2	0	1

Note:

1. MD[25:24]: DRAM Types Select
   00: SGRAM/SDRAM
   01: 2-cycle EDO DRAM
   10: 1-cycle EDO DRAM
   11: Fast Page DRAM

2. MD[31:29]: DRAM Speed Setting

	SGRAM	**2-cycle EDO**	**1-cycle EDO**	**Fast Page**
000	66	65	50	55
001	75	70	55	60
010	83	75	60	65
011	90	80	65	70
100	100	85	70	75
101	115	90	75	80
110	134	55	80	45
111	50	60	45	50

6 Display Memory Architecture

SiS6326 supports 1M Byte, 2M Bytes, and 4M Bytes DRAM configuration.

SiS6326 supports the following DRAM types:

- Fast Page (FP) DRAM
- Normal (2-cycle) EDO DRAM
- One cycle EDO DRAM
  This is for accessing some fast EDO DRAM. In this mode, it would get double bandwidth than normal EDO DRAM timing with the same MCLK frequency.
- 256Kx32 SDRAM
- 256Kx32 SGRAM

The FP DRAM and EDO DRAM types that SiS6326 supports are: 256Kx4, 256Kx8 and 2-CAS/1-WE 256Kx16.

SiS6326 also supports auto memory size detecting to provide more flexibility in mass production.

.1 Memory Configuration Pins

For FP and EDO DRAM,

In 1-bank configuration,
- RAS0* would be active.
- Only CAS[0:3]* would be active.
- WE* would be active.
- Only MD[0:31] would be active.
- MA[0:8] would be connected to all bank.

In 2-bank configuration,
- RAS0* would be active.
- CAS[0:7]* would be active.
- WE* would be active.
- MD[0:63] would be active.
- MA[0:8] would be connected to all bank.

In 4-bank configuration,
- RAS0* and RAS1* would be active.
- CAS[0:7]* would be active.
- WE* would be active.
- MD[0:63] would be active.
- MA[0:8] would be connected to all bank.

For SGRAM & SDRAM,

In 1-bank configuration,
- SCLK[0:1] would be active.
- CS0* would be active.
- Only DQM[0:3] would be active.
- WE* would be active.
- SRAS* and SCAS* would be active.
- Only MD[0:31] would be active.
- MA[0:9] would be connected to all bank.

In 2-bank configuration,
- SCLK[0:1] would be active.
- CS0* would be active.
- DQM[0:7] would be active.
- WE* would be active.
- SRAS* and SCAS* would be active.
- MD[0:63] would be active.
- MA[0:9] would be connected to all bank.

In 4-bank configuration,
- SCLK[0:1] would be active.
- CS0*, CS1* would be active.
- DQM[0:7] would be active.

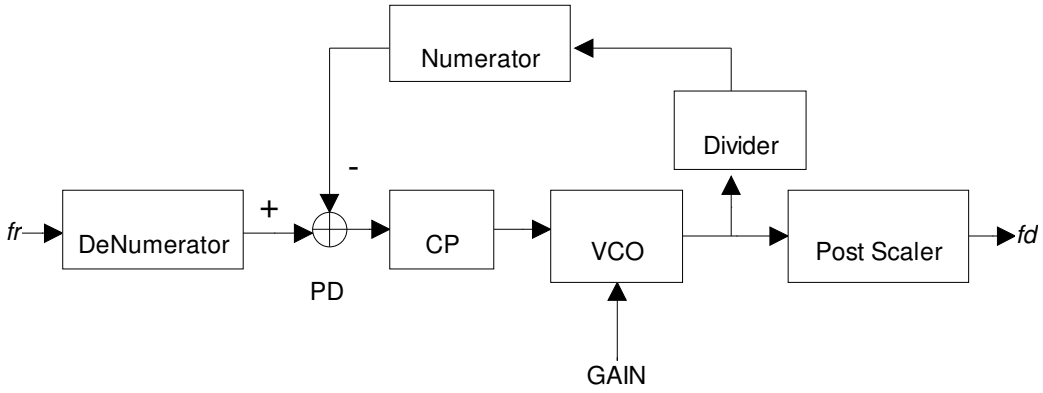
- WE* would be active.
- SRAS* and SCAS* would be active.
- MD[0:63] would be active.
- MA[0:9] would be connected to all bank.

For recommended memory configuration layout, please refer to "10 Appendix A. Recommended Memory Configuration" on page 221.

7 Internal Dual-Clock Synthesizer

SiS6326 has built-in a dual-clock synthesizer to generate the MCLK and VCLK. This clock synthesizer could generate several variable frequencies, thus it could provide the flexibility for selecting the working frequency.

The following block diagram is for clock synthesizer.



where PD is phase detection,
CP is charge pump,
VCO is voltage controlled oscillator,
fr is reference frequency, and
fd is desired frequency.

The operation of clock synthesizer is described as follow:

When the synthesizer outputs the steady frequency, it means that
fr/DeNumerator = *fd**Post Scalar /(Divider*Numerator)
i.e.
fd=*fr**(Numerator/DeNumerator)*(Divider/Post Scalar)

With this formula, we could select adequate values for Numerator, DeNumerator, Divider, and Post Scalar to obtain the desired frequency.

The planned Video Clocks (VCLK) are as follow: (units: MHz)

25.175	28.322	40.000	50.000	77.000
36.000	44.889	135.000	120.000	80.000
31.500	110.000	65.000	75.000	94.500

162.00	175.500			

Other video clocks would be added to the scheme after verified OK.
The planned Memory Clocks (MCLK) are from 40 MHz to 90 MHz with resolution 2 MHz.

8 Power Management

To satisfy the power saving for Green PC, SiS6326 supports the control protocol of DPMS (Display Power Management Signaling) proposed by VESA Monitor Committee. This protocol can reduce the VGA Monitors' power consumption.

SiS6326 has built-in two timers for stand-by and suspend modes that can be programmed from 2 minutes to 30 minutes (2 min./increase) with the extended registers.

SiS6326 also supports forcing the video subsystem into stand-by, suspend, or off modes with the extended registers.

Power saving is done by blocking HSYNC and/or VSYNC signals to the VGA monitor. The sources of activation are from the monitoring of keyboard, hardware cursor, and/or video memory read/write. The overview of the signal blocking requirements are as follows:

POWER MANAGEMENT STATE	HORIZONTAL SYNC	VERTICAL SYNC	VIDEO DISPLAY
ON	Pulses	Pulses	Yes
Stand-By	No Pulses	Pulses	No
Suspend	Pulses	No Pulses	No
OFF	No Pulses	No Pulses	No

9 Resolutions Supported

Resolution	1M Byte DRAM	2M Byte DRAM	4M Byte DRAM
640x480x8	√	√	√
640x480x16	√	√	√
640x480x24	√	√	√
800x600x4	√	√	√
800x600x8	√	√	√
800x600x16	√	√	√
800x600x24	X	√	√
1024x768x4	√	√	√
1024x768x8	√	√	√
1024x768x16	X	√	√
1024x768x24	X	X	√
1280x1024x4	√	√	√
1280x1024x8	X	√	√
1280x1024x16	X	X	√
1600x1200x4	√	√	√

1600x1200x8	X	√	√

Except these real resolution modes, SiS6326 is also built-in virtual screen mode which could support up to 2048x2048 resolution.

10 Video Accelerator

.1 Video Password/Identification Register

A video registers protection is implemented in the index 80h of CRT index register 3D4. To disable the protection, the software must first match the protection key value of 86h. If not match, read/write to any of the video associated registers are denied.

.2 Video Play Back

SiS6326 video accelerator could work in four different modes: standard FC (feature connector) mode, direct video mode, VMI interface mode, and PCI multimedia mode.

In standard FC mode, SiS6326 supports the industry standard FC spec to provide a standard video link to the third-parties' video adapters.

In direct video mode, SiS6326 could work with the Philips SAA7110 / SAA7111 and Brooktree Bt815/817/819A (8-bit SPI mode 1, 2), to provide the PC-Video solution and provide the very flexible overlaying ability mentioned below.

SiS6326 allows on-screen video and graphics overlaying on a pixel-by-pixel basis and supports both interlaced or non-interlaced video format. Overlaying occurs within programmable video extents based on a flexible color key and chroma key mechanism. By using the programmable filter, scalar, and DDA interpolation to the video data, SiS6326 allows the video data to blend and overlay with the graphics data at the same rate.

In VMI interface mode, SiS6326 supports VMI interface to connect VMI devices from 3rd parties.

Furthermore in PCI multimedia mode, SiS6326 supports PCI multimedia design guide Rev. 1.0 spec to meet future potential trend.

.3 Video Capture Window

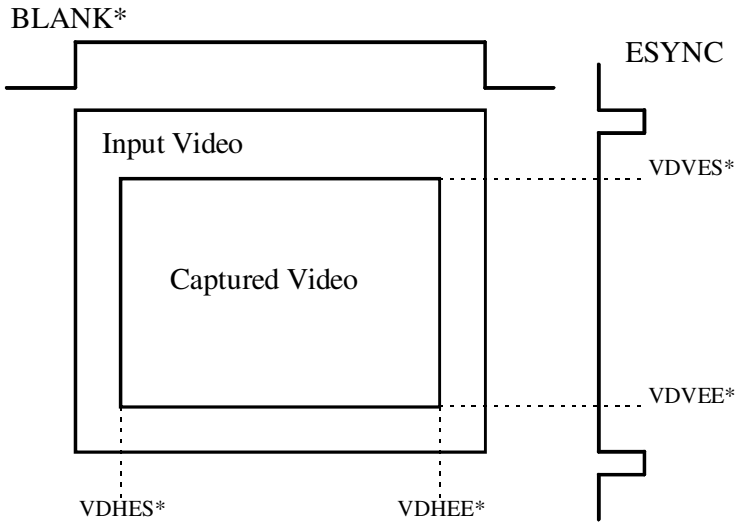


Figure 4.2

SiS6326 provides video capture windowing to select a part of input video to be captured into video frame buffer. This capture window is defined by four parameter: video data horizontal start (VDHES), video data horizontal end (VDHEE), video data vertical start (VDVES), and video data vertical end (VDVEE).

There are the video data horizontal counter and the video data vertical counter inside SiS6326. The video data horizontal counter is reset at the positive edge of signal BLANK* and counted up by PCLK or LLC1. The video data vertical counter is reset at the positive edge of ESYNC and counted up by positive of BLANK*. When the value of the video data horizontal counter is equal to or greater than VDHES and the video data vertical counter is equal to or greater than VDVES, the video data capture starts or continues. After the value of the video data horizontal counter is equal to or greater than VDHEE or the video data vertical counter is equal to or greater than VDVEE, the video capture ends.

.4 Video Captured Down Scaling

SiS6326 provides independent X-Y down scaling of the captured video image in integer increments of 1/64. Images may be scaled down to n/64 (n = 1 ~ 64) of the original image size to support video icons for graphics user interfaces, or to reduce the memory bandwidth. The scaling factor is controlled by HDSF and VDSF, which ranging from 0 to 63, and the scaling factors are (64-HDSF)/64 in horizontal and (64-VHSF)/64 in vertical.

.5 Video Capture FIFO

The scaled-down video data would be fed into the video capture FIFO before being stored to display memory. The 64x16 video capture FIFOs serve as buffers between the video capture mechanisms and the display memory, are provided to fit the bandwidth limitation of the display memory during video image capture operation.

.6 Multi-format Video Frame Buffer

The video frame buffer of SiS6326 is shared with graphics frame buffer and is a multi-format frame buffer. It could accept 16-bpp YUV422, RGB555, and RGB565 color format and 12-bpp YUV420 (plane mode).

The decompression CODEC, hardware or software, could fill the valid decompressed video frame data into the off-screen video frame buffer through the PCI local bus.

The other PCI motion video card or CPU can transfer the video data through PCI local bus directly into video frame buffer.

Then SiS6326 would overlay the video on the screen.

.7 YUV420 Plane Mode

SiS6326 supports YUV420 plane mode. The data rate of YUV420 is 12-bpp which is smaller than 16-bpp of YUV422. So that the data bandwidth can be reduced and improve the video playback performance. The YUV420 mode need three start address for Y, U and V plane, and two offset for Y and U,V plane.

.8 Video Playback Line Buffers

When CRT refresh the screen, the video data must be overlaid with graphics data. Therefore the video data would first be read out from off-screen video frame buffer into the video playback line buffers for further handling.

The video playback line buffers serve as buffers between display memory and the playback mechanisms, are provided to fit the limitation of the display memory during video playback operation.

.9 Color Space Conversion & Color Format Conversion

If the data read from the video frame buffer is in YUV422, the real time YUV-to-RGB converter will be turn on. The video data would be converted to RGB888 format for successive processing. The YUV422 are converted following the CCIR601-2 standard.

If the data read from the video frame buffer is in RGB format, the YUV-to-RGB converter would be bypassed. All the RGB565 and RGB555 format are supported and then would be converted to RGB888 format.

.10 Horizontal Interpolation DDA

The DDA (Digital Differential Accumulator) using the following mathematical calculation with 2-tap, N-phase and scaling up factor UFACT (from J points scaling up to J * UFACT points):

Destination[i] = (1 - Weight") * Source[j] + Weight" * Source[j+1]
j = TRUNC(i / UFACT)
Weight" = TRUNC(i / UFACT) - j

However since the Weight" is not an integer, the multiplication is hard to implement and therefore the following Weight is used for calculation.

Weight = TRUNC(Weight" * N) / N

The SiS6326 built-in an X-interpolation DDA mechanism to get better video stretching qual-

ity. The interpolation accuracy of DDA mechanism is 2-tap and 8-phase.

.11 Vertical Interpolation DDA

The SiS6326 built-in a Y-interpolation DDA mechanism and two line buffers mechanism to get better video stretching quality. The interpolation accuracy of DDA mechanism is 2-tap and 8-phase.

.12 Video Playback Horizontal Zooming

The playback video data can be horizontal zoom-in in 64/n factor (n = 1 ~ 64) and zoom-out in about m/16 factor (m = 1 ~ 16). The zooming factor (HPFACT) is controlled by 4-bit integer part and 6-bit fraction part. The horizontal video size will be zoomed to 1/HPFACT. If HPFACT<1, it will performing horizontal up scaling. If HPFACT>1, it will performing horizontal down scaling.

.13 Video Playback Vertical Zooming

The playback video data can be vertical zoom-in in 64/n factor (n = 1 ~ 64) and zoom-out in arbitrary factor. The zooming factor (VPFACT) is controlled by 6-bit fraction part. The video size will be zoomed to 1/VPFACT. Since the VPFACT is always less than 1, therefore you can only perform vertical up scaling by this factor. The vertical down scaling can be done by multiplying the Video Frame Buffer Offset with an integer I. Then the vertical video size will be zoomed to 1/(I*VPFACT).

.14 Video Data Blending

The pixels of graphics data can be blended by graphics data alpha value, then add with the blended video data to generate blended data. The accuracy of the blending is 4 bits, the 4 MSBs of this register.

The pixels of video data can be blended by video data alpha value, then add with the blended graphics data to generate blended data. The accuracy of the blending is 4 bits, the 4 MSBs of this register.

.15 Color Keying

A control signal is generated by comparing the 24 bits graphics data to the 24 bits color key low value and 24 bits color key high value. The bit number is dependent on color depth used. If the graphics data value is between the two color key values (all of three RGB parts), the color key is detected. This comparison mechanism can be disable by setting the video window size to zero, i.e. X-start=0, X-end=0, Y-start=0, and Y-end=0.

.16 Chroma Keying

A control signal is generated by comparing the 24 bits video data to the 24 bits chroma key low value and 24-bit chroma key high value. The chroma key can be YUV or RGB format. If the video data value is between two chroma key values (all of three RGB or YUV parts), the chroma key is detected.

.17 Graphics & Video Overlay

The overlay of the graphics data and the video data is performed by color keying and chroma keying method. The overlay operation is set by Key Overlay Operation Mode Register. The operation is defined below:

Operation Mode	Operation
0000	always select graphics data
0001	select blended data when color key and chroma key, otherwise select graphics data
0010	select blended data when color key and not chroma key, otherwise select graphics data
0011	select blended data when color key, otherwise select graphics data
0100	select blended data when not color key and chroma key, otherwise select graphics data
0101	select blended data when chroma key, otherwise select graphics data
0110	select blended data when color key xor chroma key, otherwise select graphics data
0111	select blended data when color key or chroma key, otherwise select graphics data
1000	select blended data when not color key and not chroma key, otherwise select graphics data
1001	select blended data when color key xnor chroma key, otherwise select graphics data
1010	select blended data when not chroma key, otherwise select graphics data
1011	select blended data when color key or not chroma key, otherwise select graphics data
1100	select blended data when not chroma key, otherwise select graphics data
1101	select blended data when not color key or chroma key, otherwise select graphics data
1110	select blended data when not color key or not chroma key, otherwise select graphics data
1111	always select blended data

.18 Video Window Control Registers

The video window area is defined by six registers that specify a rectangular region by X-start, X-end, Y-start, and Y-end (X: Horizontal, Y: Vertical). Please refer to ".2 to .7" on Page 118 to 119.

The location of the video window is referenced to the VGA sync signals.

The size of the video window is defined in VGA pixels and lines.

.19 Video Panning

The displayed video image could be panned around the captured video image by setting the video display starting address. i.e. You may selectively display any part of the captured video image. The video display starting address is equal to the video frame buffer starting address adds the panning offset. Please refer to ".11, .12, and .14" on Page 120 to 121.

.20 Overlay Memory Data

The display memory is configured to two areas: one is the graphics area (which is the actual screen display area) storing graphics pixel data, and the other is the video area (which is also called off-screen area) storing the video pixel data.

In the graphics area, the corresponding video window area is reserved with the color key value. During the CRT scan period, a comparison of graphics data with color key data is performed. Once a match meet, the CRT output path would be switched from graphics path to video path to display the video data.

.21 Video Playback Contrast Enhancement and Brightness Control

To achieve higher video quality, the SiS6326 built-in the Contrast Enhancement and Brightness Control mechanism.

For Contrast Enhancement, first, the mean value is calculated by some pixels and some frames. The number of sampled pixels and frames is programmable by registers. Contrast Enhancement mechanism then increases the difference between the video data and mean value. The increasing rate is programmed by gain. The value of gain is frame 1.0 to 1.4375.

The Brightness of video data can be controlled. The Brightness is a 2's complement value from -128 to 127. This value is then added with the video data to increase or decrease the brightness of video.

.22 Video CPU Write Data Decimation

The DRAM bandwidth is not enough under some high resolution and high color depth graphics modes, so the video overlay cannot perform under these modes. The Video CPU Write Data Decimation mechanism can decimate two continuous pixels of video to one pixel to reduce the video bandwidth. The video performance can be improved but video quality will be downgraded slightly.

11 MPEG Decoder

SiS6326 provides ISO/IEC 11172-1 MPEG-1 and ISO/IEC 13818-2 MPEG-2 MP@ML video decoding functions. It receives commands and decodes them from SiS6326 command queue FIFO. The command queue space is constituted of one 32-stage, one 10-stage hardware queue, and one 3840-stage software queue which uses off-screen memory. The command queue FIFO can provide high speed and high efficient command transmission between PCI bus and MPEG decoder module. Some of the MPEG commands can be compressed before entering the command queue FIFO to reduce software queue DRAM bandwidth.

SiS6326 high speed MPEG video decoding accelerator can provide IDCT and motion compensation capabilities for supporting DVD and VCD titles playback. It accelerates the MPEG video playback by macro-block layer decoding. The system layer bit-stream parsing, video

bit-stream parsing, and inverse quantization are left to CPU. Each 32-bits MPEG command is transferred via PCI bus burst write cycle in one cycle (33Mhz bus clock) or two cycles (66 MHz bus clock) to get fast command reception.

At the same time, the video playback module reads the data in the decoder buffer. The data is arranged in YUV (YCbCr) 420 format. After YUV to RGB conversion and overlay composition, the RAMDAC outputs the real time video to VGA output port.

Figure 4.3 is SiS6326 MPEG video decompression flow. The VLD (Variable Length Decoding) and Iquant (Inverse Quantization) are done by software.

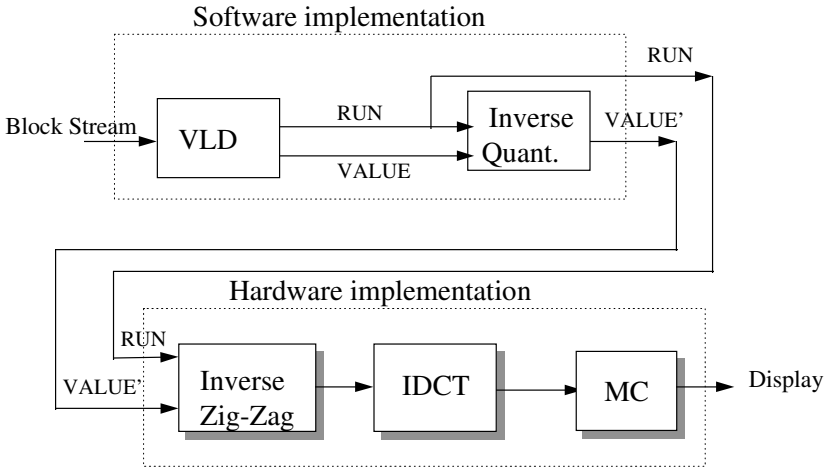


Figure 4.3

.1 Turbo Queue in MPEG

The Command Queues Architecture also apply to MPEG video decoder and operate in the same way as described previously (".1 Turbo Queue in 2D Graphics Engine" on page 18). The following paragraph is a re-description of SiS6326 Turbo Queue operation in terms of MPEG to re-emphasize the importance of Turbo Queue.

In SiS6326, there are two command queues between PCI bus interface and the MPEG accelerator. One is hardware queue and the other one is Turbo Queue. The architecture diagram of SiS6326 command queue is as follows.

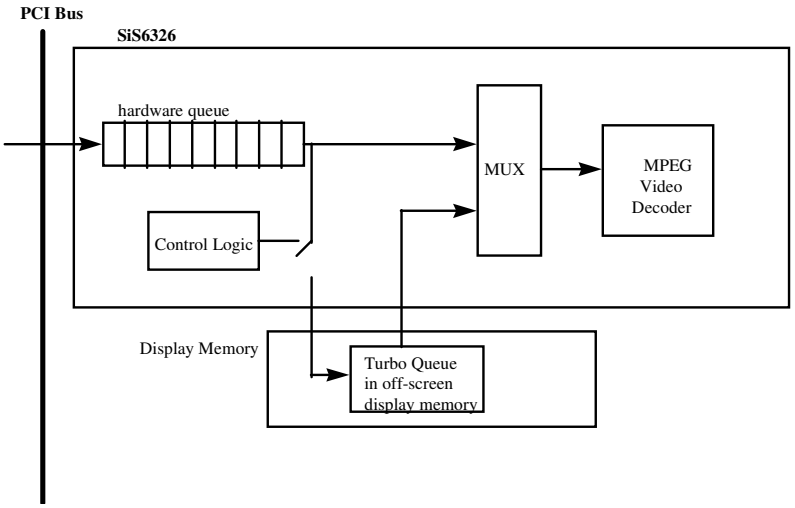


Figure 4.4

The Hardware Command Queue is a 42 double-words queue. And there are 30K Bytes off-screen memory space reserved for the Turbo Queue. Since the average length of an MPEG command is 8 double-words (which is called 1 stage), therefore the SiS6326 command queue could be regarded as infinity stages with Turbo Queue and could get rid of the CPU waiting issue to get extra high performance.

When the hardware command queue is going to be full, the head commands would be moved to the Turbo Queue and left hardware queue space for new PCI commands. The command queue architecture makes the transmission of SiS6326 PCI commands most efficient.

The Turbo Queue base address is generally set to the last 32K Bytes segment on off-screen. To program the extended register SR2C (Turbo Queue Base Address Register) could allocate the Turbo Queue into the off-screen region of the display memory automatically.

12 TV-OUT Technology

In SiS6326, three TV DACs and anti-flicker line buffers are integrated to create high quality and non-flicker NTSC/PAL video outputs. All these three TV DACs are 10-bit resolution and share reference voltage with the built-in VGA DAC reference voltage generator. An external resistor is designed to adjust TV DAC full swing voltage. In the normal conditions, composite and S-video full swings are about 1.2V and 1.0V respectively. Current consumption is about 30 mA for each TV DAC when active and less than 1 mA when disabled.

AS requested by the TV standard, the TV clock source should be very precise to generate the correct color. For NTSC system, 27.000 MHz is required. For PAL system, 36.000 MHz is required.

To save the precision oscillator cost, SiS6326 integrates the video clock generator to generate the required high precision TV clock. The SiS6326 high precision sub-carrier frequency generator is based on a high resolution sine/cosine ROM table and phase accumulator. The sub-

carrier frequency is programmed by software and could be fine tuned through an user friendly utility to fit different TV sets. This is very important in practice since there are so many different TV sets in the world.

The SiS6326 TV encoder accepts digital R/G/B signal generated by VGA directly as to be free from A/D distortion. The TV encoder would generates its own synchronization signal by referencing the VGA synchronization signals, such as horizontal retrace and vertical retrace. This encoder run at the same pixel clock as the VGA does. Both TV and PC monitor can display simultaneously.

The data path and control signals between TV encoder, VGA core, and DAC are shown in Figure 2.5. First, the color space conversion block converses R/G/B signals into Y,U,V for PAL and Y,I,Q for NTSC. Then, these signals are written into TV line buffer for latter anti-flicker process.

SiS6326 supports four types of anti-flicker modes: mild, medium, strong, and adaptive modes. Basically, anti-flicker is similar to image filtering that can reduce flicker phenomenon. But to some extent, anti-flicker also degrades video quality. Therefore SiS6326 innovates an "adaptive" anti-flicker mode to fix flicker issue without down-grade video quality. In adaptive mode, SiS6326 can adaptively select different anti-flicker filter strength pixel by pixel, depending on the flicker probability detected by the internal logic. Based on this scheme, SiS6326 can offer non-flicker video quality with minimum video quality degradation.

SiS6326 integrates three TV sense analog comparator to detect the status of the composite or S-video connectivity. Based on the read-back value, BIOS and software utility can intelligently set the video encoder configuration. For example, for composite video only connection, software utility can automatically select the composite video settings, turn on the composite video DACs, and disable the Y/C video DACs for power saving. For S-video only connection, software utility can automatically disable luminance and chrominance filter, which is required in composite video output, to enhance S-video sharpness.

SiS6326 offers an power-on configuration pin for power-on selection between PAL and NTSC in TV boot-up systems. For monitor boot-up system, the PAL and NTSC could be selected by either hardware configuration or software setting.

13 Signature Analysis

The signature analysis is provided to automatically test the graphics data which is the input of the DAC. This technique is based on the concept of cyclic redundancy checking (CRC) and is realized in hardware using linear feedback shift registers (LFSRs). It is composed of a 16-bit signature generator register which is called multiple-input signature register (*MISR,* shown in the following figure) and is used to ensure a unique signature of different patterns.

For a given test image, the signature analysis could get a right unique signature number. If an error occurs in the controller or the data manipulation, it would result in a different wrong signature number as compared to the pre-calculated signature value. Thus a test technician could sort the good or bad chips more quickly and accurately and requires no visual inspection of the screen for errors in the mass product environment. This could save significant testing time. If the display screen includes blinking attributes or a blinking cursor, then the signature will be different when blink-off and blink-on for those frames. Assume all error patterns

are equally likely, then the probability of failing to detect an error by the *MISR* is approximately 0.000015.

To match the inputs of *MISR*, the 24-bit graphics data (i.e. the input of the DAC of the RAMDAC) would be first converted into 16-bit data. The corresponding transfer function of the *MISR* of the following figure is

$$p(x) = 1 + c_1 \cdot x + c_2 \cdot x^2 + c_3 \cdot x^3 + ... + c_{16} \cdot x^{16}$$

where $c_1, c_2, c_3, ..., c_{16}$ can be either 0 or 1. SiS6326 sets the parameters of the signature register as

$$p(x) = 1 + x + x^7 + x^{10} + x^{16}$$

Once the software enables the signature analysis function, SiS6326 could test itself intelligently and automatically. This function could also be disabled by the extended control register for power saving purposes.

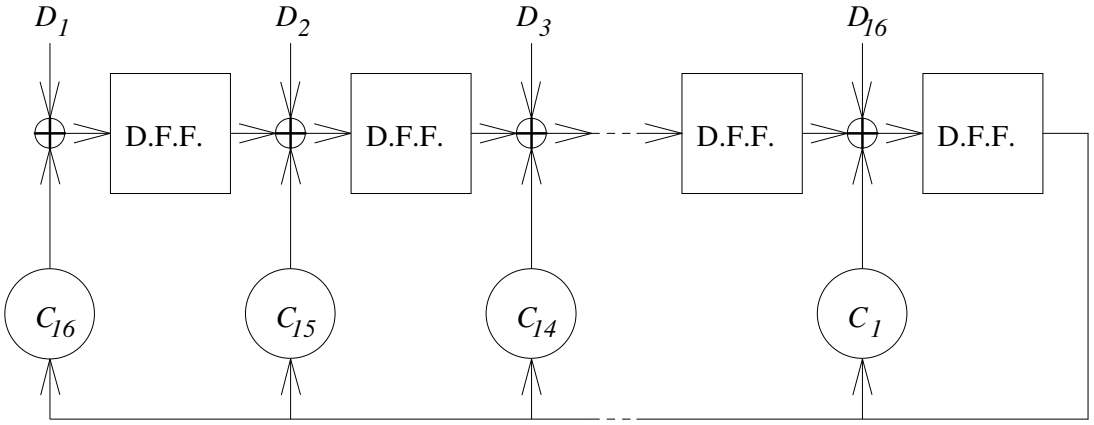


Figure 4.5 Multi-Input Signature Register (MISR)

14 Compatibility

The SiS6326 is fully compatible with all standard IBM VGA modes and EGA, CGA, MDA, and Hercules modes.

15 Process and Supply Voltages

SiS6326 is manufactured by 3.3 volts CMOS process. All the I/O buffers are 5V tolerant. Only one 5 volts VDD pin is required for the reference of voltage tolerance. All other supply voltages must be within 3.3 volts ± 5%.

In non-AGP configuration, all the AGP pins must be tight to ground.

16 Software Support

To fully utilize and support the SiS6326 hardware features, SiS has developed a high-performance VESA extension compliant BIOS.

Extended graphics and text modes are supported by software application drivers developed by SiS. The following applications are currently supported:

- 3D Studio Version 3.0
- AutoCAD/386 Release 11, 12, 13
- Auto Shade/386 Version 2.0
- Microsoft Windows 3.1 & 3.11
- Microsoft Windows 95
- Microsoft Windows NT Version 3.1, 3.5, 3.51, and 4.0
- OS/2 Presentation Manager 2.1, 3.0, and 4.0

Video operation are supported by software application drivers developed by SiS. The following applications are currently supported:

- Microsoft Video For Windows
- DCI driver
- Direct Draw driver

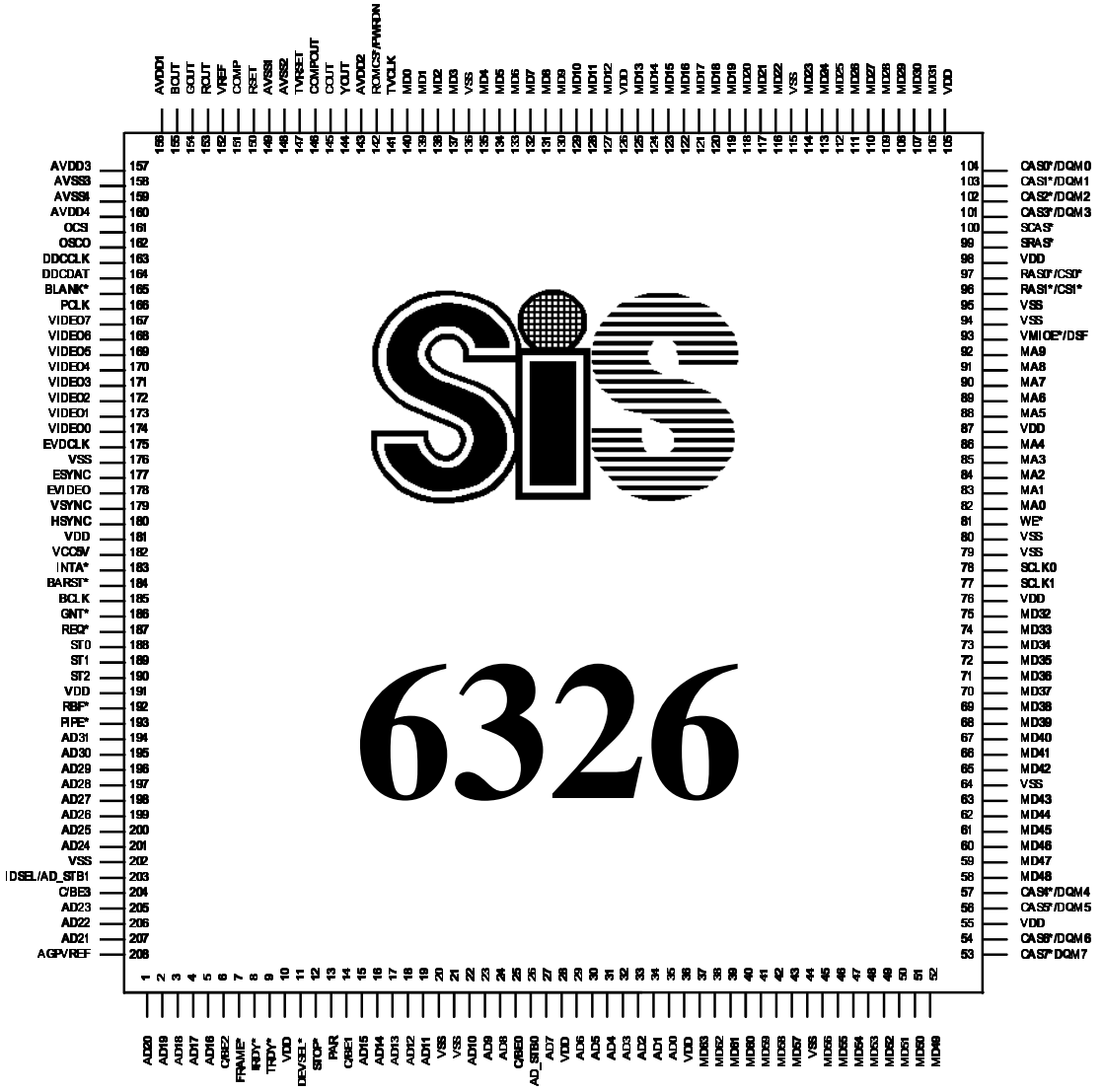
3D operation are supported by software application drivers developed by SiS. The following applications are currently supported:

- Microsoft Direct3D
- OpenGL in Windows NT
- Renderware for Windows 95

5. Pin Description

1 Pin Assignment

.1 Pin Outline



.2 Pin List

Pin No.	Pin Name	Type	Driving Type
1	AD20	I/O	4
2	AD19	I/O	4
3	AD18	I/O	4
4	AD17	I/O	4
5	AD16	I/O	4
6	C/BE2	I/O	4
7	FRAME*	I/O	4
8	IRDY*	I/O	4
9	TRDY*	I/O	4
10	VDD		
11	DEVSEL*	I/O	4
12	STOP*	I/O	4
13	PAR	I/O	4
14	C/BE1	I/O	4
15	AD15	I/O	4
16	AD14	I/O	4
17	AD13	I/O	4
18	AD12	I/O	4
19	AD11	I/O	4
20	VSS		
21	VSS		
22	AD10	I/O	4
23	AD9	I/O	4
24	AD8	I/O	4
25	C/BE0	I/O	4
26	AD_STB0	I	

Pin No.	Pin Name	Type	Driving Type
27	AD7	I/O	4
28	VDD		
29	AD6	I/O	4
30	AD5	I/O	4
31	AD4	I/O	4
32	AD3	I/O	4
33	AD2	I/O	4
34	AD1	I/O	4
35	AD0	I/O	4
36	VDD		
37	MD63	I/O	4/2D
38	MD62	I/O	4/2D
39	MD61	I/O	4/2D
40	MD60	I/O	4/2D
41	MD59	I/O	4/2D
42	MD58	I/O	4/2D
43	MD57	I/O	4/2D
44	VSS		
45	MD56	I/O	4/2D
46	MD55	I/O	4/2D
47	MD54	I/O	4/2D
48	MD53	I/O	4/2D
49	MD52	I/O	4/2D
50	MD51	I/O	4/2D
51	MD50	I/O	4/2D
52	MD49	I/O	4/2D

NOTE: Driving Type
8R: 8mA, 1 driven factor
4 : 4mA, 1 driven factor
4R: 4mA, 0.5 driven factor
8: 8mA, 2 driven factor
12: 12mA, 2 driven factor

A. I: Analog Input
A. O: Analog Output
D: Internal Pull-Down

Pin No.	Pin Name	Type	Driving Type
53	CAS7*/DQM7	O	4/2
54	CAS6*/DQM6	O	4/2
55	VDD		
56	CAS5*/DQM5	O	4/2
57	CAS4*/DQM4	O	4/2
58	MD48	I/O	4/2D
59	MD47	I/O	4/2D
60	MD46	I/O	4/2D
61	MD45	I/O	4/2D
62	MD44	I/O	4/2D
63	MD43	I/O	4/2D
64	VSS		
65	MD42	I/O	4/2D
66	MD41	I/O	4/2D
67	MD40	I/O	4/2D
68	MD39	I/O	4/2D
69	MD38	I/O	4/2D
70	MD37	I/O	4/2D
71	MD36	I/O	4/2D
72	MD35	I/O	4/2D
73	MD34	I/O	4/2D
74	MD33	I/O	4/2D
75	MD32	I/O	4/2D
76	VDD		
77	SCLK1	O	8/12
78	SCLK0	O	8/12

Pin No.	Pin Name	Type	Driving Type
79	VSS		
80	VSS		
81	WE*	O	4/2
82	MA0	O	4/2
83	MA1	O	4/2
84	MA2	O	4/2
85	MA3	O	4/2
86	MA4	O	4/2
87	VDD		
88	MA5	O	4/2
89	MA6	O	4/2
90	MA7	O	4/2
91	MA8	O	4/2
92	MA9	O	4/2
93	VMIOE*/DSF	O	4R
94	VSS		
95	VSS		
96	RAS1*/CS1*	O	4/2
97	RAS0*/CS0*	O	4/2
98	VDD		
99	SRAS*	O	4/2
100	SCAS*	O	4/2
101	CAS3*/DQM3	O	4/2
102	CAS2*/DQM2	O	4/2
103	CAS1*/DQM1	O	4/2
104	CAS0*/DQM0	O	4/2

NOTE: Driving Type

8R: 8mA, 1 driven factor
4 : 4mA, 1 driven factor
4R: 4mA, 0.5 driven factor
8: 8mA, 2 driven factor
12: 12mA, 2 driven factor

A. I: Analog Input
A. O: Analog Output
D: Internal Pull-Down

Pin No.	Pin Name	Type	Driving Type
105	VDD		
106	MD31	I/O	4/2D
107	MD30	I/O	4/2D
108	MD29	I/O	4/2D
109	MD28	I/O	4/2D
110	MD27	I/O	4/2D
111	MD26	I/O	4/2D
112	MD25	I/O	4/2D
113	MD24	I/O	4/2D
114	MD23	I/O	4/2D
115	VSS		
116	MD22	I/O	4/2D
117	MD21	I/O	4/2D
118	MD20	I/O	4/2D
119	MD19	I/O	4/2D
120	MD18	I/O	4/2D
121	MD17	I/O	4/2D
122	MD16	I/O	4/2D
123	MD15	I/O	4/2D
124	MD14	I/O	4/2D
125	MD13	I/O	4/2D
126	VDD		
127	MD12	I/O	4/2D
128	MD11	I/O	4/2D
129	MD10	I/O	4/2D
130	MD9	I/O	4/2D

Pin No.	Pin Name	Type	Driving Type
131	MD8	I/O	4/2D
132	MD7	I/O	4/2D
133	MD6	I/O	4/2D
134	MD5	I/O	4/2D
135	MD4	I/O	4/2D
136	VSS		
137	MD3	I/O	4/2D
138	MD2	I/O	4/2D
139	MD1	I/O	4/2D
140	MD0	I/O	4/2D
141	TVCLK	I	
142	ROMCS*/ PWRDN	I/O	8R
143	AVDD2		
144	YOUT	O	
145	COUT	O	
146	COMPOUT	O	
147	TVRSET	A.I	
148	AVSS2		
149	AVSS1		
150	RSET	A.I	
151	COMP	A.I	
152	VREF	A.I	
153	ROUT	A.O	
154	GOUT	A.O	
155	BOUT	A.O	
156	AVDD1		

NOTE: Driving Type

8R: 8mA, 1 driven factor
4 : 4mA, 1 driven factor
4R: 4mA, 0.5 driven factor
8: 8mA, 2 driven factor
12: 12mA, 2 driven factor

A. I: Analog Input
A. O: Analog Output
D: Internal Pull-Down

Pin No.	Pin Name	Type	Driving Type
157	AVDD3		
158	AVSS3		
159	AVSS4		
160	AVDD4		
161	OSCI	I	
162	OSCO	O	
163	DDCCLK	I/O	4R
164	DDCDAT	I/O	4R
165	BLANK*	I/O	8R
166	PCLK	I/O	8R
167	VIDEO7	I/O	8R
168	VIDEO6	I/O	8R
169	VIDEO5	I/O	8R
170	VIDEO4	I/O	8R
171	VIDEO3	I/O	8R
172	VIDEO2	I/O	8R
173	VIDEO1	I/O	8R
174	VIDEO0	I/O	8R
175	EVDCLK	I	
176	VSS		
177	ESYNC	I	
178	EVIDEO	I	
179	VSYNC	I/O	8R
180	HSYNC	I/O	8R
181	VDD		
182	VCC5V		

Pin No.	Pin Name	Type	Driving Type
183	INTA*	O	4R
184	BARST*	I	
185	BCLK	I	
186	GNT*	I	
187	REQ*	O	4
188	ST0	I	
189	ST1	I	
190	ST2	I	
191	VDD		
192	RBF*	O	4
193	PIPE*	O	4
194	AD31	I/O	4
195	AD30	I/O	4
196	AD29	I/O	4
197	AD28	I/O	4
198	AD27	I/O	4
199	AD26	I/O	4
200	AD25	I/O	4
201	AD24	I/O	4
202	VSS		
203	IDSEL/ AD_STB1	I	
204	C/BE3	I/O	4
205	AD23	I/O	4
206	AD22	I/O	4
207	AD21	I/O	4
208	AGPVREF		

NOTE: Driving Type

8R: 8mA, 1 driven factor
4 : 4mA, 1 driven factor
4R: 4mA, 0.5 driven factor
8: 8mA, 2 driven factor
12: 12mA, 2 driven factor

A. I: Analog Input
A. O: Analog Output
D: Internal Pull-Down

2 Pin Definition

.1 PCI Bus Interface

Pin No.	Symbol	Type	Name and Function
184	BARST*	I	*PCI Reset* is used to bring PCI-specific registers, sequencer, and signals to a consistent state.
185	BCLK	I	*PCI Bus Clock* provides timing for all transactions on PCI bus.
29~35, 27, 22~24, 15~19, 1~5, 205~207, 194~201	AD[6:0], AD7, AD[10:8], AD[15:11], AD[20:16], AD[23:21], AD[24:31]	I/O	*PCI Address/Data Bus* are multiplexed on the same pins. The Address phase is the clock cycle in which FRAME* is asserted and the data phase is immediately after the address phase.
25, 14, 6, 204	C/BE0, C/BE1, C/BE2, C/BE3	I/O	*PCI Command/Byte Enable Bus* are multiplexed on the same pins. During the address phase of a transaction, C/BE define the bus command, and during the data phase C/BE are used as Byte Enables.
13	PAR	O	*PCI Parity Bit* is even parity across AD[31:0] and C/BE[3:0].
7	FRAME*	I/O	*PCI Frame Cycle* is driven by the current master to indicate the beginning and duration of an access.
9	TRDY*	I/O	*PCI Target Ready* indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
8	IRDY*	I/O	*PCI Initiator Ready* indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction
12	STOP*	I/O	*PCI Stop* indicates the current target is requesting the master to stop the current transaction.
203	IDSEL	I	*PCI Initialization Device Select* is used as a chip select during configuration read and write transactions.
11	DEVSEL*	I/O	*PCI Device Select* indicates whether any device on the bus has been selected.
183	INTA*	O	*PCI Interrupt* indicates the interrupt signal generated by SiS6326.
186	GNT*	I	*PCI Master Request* indicates to the arbiter that this agent desires use of the bus.
187	REQ*	O	*PCI Master Grant* indicates to the agent that access to the bus has been granted.

.2 AGP Interface

Pin No.	Symbol	Type	Name and Function
184	BARST*	I	*Same as PCI*
185	BCLK	I	*AGP Clock* provides timing for AGP and PCI control signals.
	AD[31:0]	I/O	*Same as PCI*
	C/BE[3:0]	I	*AGP Command information.*
193	PIPE*	O	*AGP Pipelined* request is asserted by the current master to indicate a full width request is to be enqueued by the target.
188~190	ST[0:2]	I	*AGP Status* bus provides information from the arbiter to a Master on what it may do.
192	RBF*	I	*AGP Read Buffer Full* indicates if the master is ready to accept previously requested low priority read data or not.
26	AD_STB0	I	*AGP AD Bus Strobe 0* provides timing for 2x data transfer mode on the AD[15:0]
203	AD_STB1	I	*AGP AD Bus Strobe 1* provides timing for 2x data transfer mode on the AD[31:16]. Mux with IDSEL
8	IRDY*	O	*AGP Master Ready* indicates the AGP compliant master is ready to provide all write data for the current transaction.
9	TRDY*	I	*AGP Target Ready* indicates the AGP compliant target is ready to provide read for the entire transaction.
186	GNT*	I	*Same as PCI.*
187	REQ*	O	*Same as PCI.*
183	INTA*	O	*Same as PCI.*
208	AGPVREF		*Reference Voltage* for AGP AD[31:0] and AD_STB[1:0] I/O pads.

.3 Display Memory Interface

For FP, EDO DRAM,

Pin No.	Symbol	Type	Name and Function
96~97	RAS*[1:0]	O	*Row Address Strobe*
53~54, 56~57, 101~104	CAS*[7:6], CAS*[5:4], CAS*[3:0]	O	*Column Address Strobe bus*
81	WE*	O	*Write Enable*
82~86, 88~91	MA[0:4], MA[5:8]	O	*Memory Address bus*
37~43, 45~52,	MD[63:57], MD[56:49],	I/O	*Memory Data Bus*

58~63, 65~75, 106~114, 116~125, 127~135, 137~140	MD[48:43], MD[42:32], MD[31:23], MD[22:13], MD[12:4], MD[3:0]		

For SDRAM/SGRAM DRAM,

Pin No.	Symbol	Type	Name and Function
77~78	SCLK[1:0]	O	*Clock Output*
96~97	CS*[1:0]	O	*Chip Select*
53~54, 56~57, 101~104	DQM[7:6], DQM[5:4], DQM[3:0]		*Byte Input/Output Mask*
81	WE*	O	*Write Enable*
99	SRAS*	O	*Row Address Asserted Bank Enable*
100	SCAS*	O	*Column Address Asserted*
93	DSF	O	*Special Functional Input Flag* Mux with VMIOE*
82~86, 88~92	MA[0:4], MA[5:9],	O	*Memory Address bus*
37~43, 45~52, 58~63, 65~75, 106~114, 116~125, 127~135, 137~140	MD[63:57], MD[56:49], MD[48:43], MD[42:32], MD[31:23], MD[22:13], MD[12:4], MD[3:0]	I/O	*Memory Data Bus*

.4 Clock Signals

Pin No.	Symbol	Type	Name and Function
161	OSCI	I	*Reference Clock 14.318 MHz Input*
162	OSCO	O	*Reference Clock 14.318 MHz Output*

NOTE: A. I: Analog Input; A. O: Analog Output

.5 Video/Video DAC Interface (In Standard FC mode)

Pin No.	Symbol	Type	Name and Function
180	HSYNC	I/O	*Horizontal Sync*
179	VSYNC	I/O	*Vertical Sync*
166	PCLK	I/O	*Pixel Clock*
167~174	VIDEO[7:0]	I/O	*Video Data Bus*
165	BLANK*	I/O	*Blank Video signal*

153	ROUT	A. O	*Red Video Signal Output*
154	GOUT	A. O	*Green Video Signal Output*
155	BOUT	A. O	*Blue Video Signal Output*
151	COMP	A. I	*Compensation Pin* Bypass this pin with an external 0.1 uF capacitor to AVDD.
150	RSET	A. I	*Reference Resistor* An external resistor is connected between the RSET pin and AGND to control the magnitude of the full-scale current.
152	VREF	A. I	*Voltage Reference* If an external voltage is used, it must supply this input with a 1.235V reference.
177	ESYNC	I	*Enable Sync Input, active low*
175	EVDCLK	I	*Enable Video Clock Input, active low*
178	EVIDEO	I	*Enable Video Data Input, active low*

NOTE: A. I: Analog Input; A. O: Analog Output

.6 Video Input Interface (In Direct Video Mode)

Pin No.	Symbol	Type	Name and Function
167~174	VIDEO[7:0]	I/O	*Video Data Bus*
177	VDVSYNC	I	*Video Data Vertical Sync Signal,* *Mux with EVSYNC*
175	VDFIELD	I	*Video Data Field Signal,* *Mux with EVDCLK*
178	EVIDEO	I	*Enable Video Data Input, active low*
165	VDDE	I/O	*Video Data Valid,* Mux with Blank*

.7 BIOS Interface

Pin No.	Symbol	Type	Name and Function
142	ROMCS*	O	*ROM Chip Select*
	ROMADR[15:0]	I/O	*ROM Address* Mux with MD[15:0]
	ROMDAT[7:0]	I/O	*ROM Data Bus* Mux with MD[23:16]

.8 DDC Interface

Pin No.	Symbol	Type	Name and Function
164	DDCDAT	I/O	*Display Data Channel Data Line*
163	DDCCLK	I/O	*Display Data Channel Clock Line*

.9 TV-OUT Interface

Pin No.	Symbol	Type	Name and Function
144	YOUT	A.O	*S-Video Luminance Output*

145	COUT	A.O	*S-Video Chrominance Output*
146	COMPOUT	A.O	*Composite Output*
147	TVRSET	A.I	*Reference Resistor* An external resistor is connected between the TVRSET pin and AGND to control the magnitude of the full-scale current.
141	TVCLK	I	*TV Clock Input*

.10 VMI Interface

Pin No.	Symbol	Type	Name and Function
93	VMIOE*	O	*VMI device chip select, active low* Mux with DSF
	VMIHD[7:0]	I/O	*VMI Data Bus* Mux with MD[7:0]
	VMIHA[3:0]	O	*VMI Address Bus* Mux with MD[11:8]
127	CS*	O	*Chip Select for Both Mode A and Mode B* Mux with MD12
125	DS*	O	*Data Strobe for Mode A* Mux with MD13
124	R/W*	O	*Read/Write# for Mode A* Mux with MD14
123	DTACK	I	*Data Acknowledge for Mode A* Mux with MD15
125	RD*	O	*Read for Mode B* Mux with MD13
124	WR*	O	*Write for Mode B* Mux with MD14
123	READY	I	*Data Ready for Mode B* Mux with MD15

.11 Misc.

Pin No.	Symbol	Type	Name and Function
142	PWDN*	I	*External Power Down Pin* Mux with ROMCS*

.12 Power and Ground

Pin No.	Symbol	Type	Name and Function
143,156, 157,160	AVDD		*Analog Power*
148,149 158,159	AVSS		*Analog Ground*
10,28,36, 55,76,87,	VDD		*Digital Power*

98,105,126, 181,191			
20,21,44, 64,79,80, 94,95,115, 136,176, 202	VSS		*Digital Ground*
182	VCC5V		*5V Reference Voltage*

6. Mode Tables

1 Standard VGA Modes

MODE	TYPE	DISPLAY SIZE	COLORS SHADES	ALPHA FORMAT	BUFFER START	BOX SIZE	MAX. PAGES
0	A/N	320x200	16	40x25	B800	8x8	8
0*	A/N	320x350	16	40x25	B800	8x14	8
0+	A/N	360x400	16	40x25	B800	9x16	8
1	A/N	320x200	16	40x25	B800	8x8	8
1*	A/N	320x350	16	40x25	B800	8x14	8
1+	A/N	360x400	16	40x25	B800	9x16	8
2	A/N	640x200	16	80x25	B800	8x8	8
2*	A/N	640x350	16	80x25	B800	8x14	8
2+	A/N	720x400	16	80x25	B800	9x16	8
3	A/N	640x200	16	80x25	B800	8x8	8
3*	A/N	640x350	16	80x25	B800	8x14	8
3+	A/N	720x400	16	80x25	B800	9x16	8
4	APA	320x200	4	40x25	B800	8x8	1
5	APA	320x200	4	40x25	B800	8x8	1
6	APA	640x200	2	80x25	B800	8x8	1
7	A/N	720x350	4	80x25	***B000***	9x14	8
7+	A/N	720x400	4	80x25	***B000***	9x16	8
0D	APA	320x200	16	40x25	A000	8x8	8
0E	APA	640x200	16	80x25	A000	8x8	4
0F	APA	640x350	2	80x25	***B000***	8x14	2
10	APA	640x350	16	80x25	A000	8x14	2
11	APA	640x480	2	80x30	A000	8x16	1
12	APA	640x480	16	80x30	A000	8x16	1
13	APA	320x200	256	40x25	A000	8x8	1

NOTE: 1. A/N: Alpha/Numeric
2. APA: All Point Addressable (Graphics)

MODE	DISPLAY SIZE	COLORS SHADES	FRAME RATE.	H-SYNC.	VIDEO FREQ.
0	320x200	16	70	31.5 K	25.1 M
0*	320x350	16	70	31.5 K	25.1 M
0+	360x400	16	70	31.5 K	28.3 M
1	320x200	16	70	31.5 K	25.1 M
1*	320x350	16	70	31.5 K	25.1 M
1+	360x400	16	70	31.5 K	28.3 M
2	640x200	16	70	31.5 K	25.1 M
2*	640x350	16	70	31.5 K	25.1 M
2+	720x400	16	70	31.5 K	28.3 M
3	640x200	16	70	31.5 K	25.1 M
3*	640x350	16	70	31.5 K	25.1 M
3+	720x400	16	70	31.5 K	28.3 M
4	320x200	4	70	31.5 K	25.1 M
5	320x200	4	70	31.5 K	25.1 M
6	640x200	2	70	31.5 K	25.1 M
7*	720x350	4	70	31.5 K	28.3 M
7+	720x400	4	70	31.5 K	28.3 M
0D	320x200	16	70	31.5 K	25.1 M
0E	640x200	16	70	31.5 K	25.1 M
0F	640x350	2	70	31.5 K	25.1 M
10	640x350	16	70	31.5 K	25.1 M
11	640x480	2	60	31.5 K	25.1 M
12	640x480	16	60	31.5 K	25.1 M
13	320x200	256	70	31.5 K	25.1 M

NOTE: i - interlaced mode
n - noninterlaced mode

2 Enhanced Video Modes

MODE	TYPE	DISPLAY SIZE	COLORS SHADES	ALPHA FORMAT	BUFFER START	BOX SIZE	MAX. PAGES
22	A/N	1056x352	16	132x44	B800	8x8	2
23	A/N	1056x350	16	132x25	B800	8x14	4
24	A/N	1056x364	16	132x28	B800	8x13	4
25	APA	640x480	16	80x60	A000	8x8	1
26	A/N	720x480	16	80x60	B800	9x8	3
29	APA	800x600	16	100x37	A000	8x16	1
2A	A/N	800x600	16	100x40	B800	8x15	4
2D	APA	640x350	256	80x25	A000	8x14	1
2E	APA	640x480	256	80x30	A000	8x16	1
2F	APA	640x400	256	80x25	A000	8x16	1
30	APA	800x600	256	100x37	A000	8x16	1
37	APA	1024x768	16	128x48	A000	8x16	1
38	APA	1024x768	256	128x48	A000	8x16	1
39	APA	1280x1024	16	160x64	A000	8x16	1
3A	APA	1280x1024	256	160x64	A000	8x16	1
3B	APA	1600x1200	16	200x75	A000	8x16	1
3C	APA	1600x1200	256	200x75	A000	8x16	1
40	APA	320x200	32K	40x25	A000	8x8	1
41	APA	320x200	64K	40x25	A000	8x8	1
42	APA	320x200	16.8M	40x25	A000	8x8	1
43	APA	640x480	32K	80x30	A000	8x16	1
44	APA	640x480	64K	80x30	A000	8x16	1
45	APA	640x480	16.8M	80x30	A000	8x16	1
46	APA	800x600	32K	100x37	A000	8x16	1
47	APA	800x600	64K	100x37	A000	8x16	1
48	APA	800x600	16.8M	100x37	A000	8x16	1
49	APA	1024x768	32K	128x48	A000	8x16	1
4A	APA	1024x768	64K	128x48	A000	8x16	1
4B	APA	1024x768	16.8M	128x48	A000	8x16	1
4C	APA	1280x1024	32K	160x64	A000	8x16	1
4D	APA	1280x1024	64K	160x64	A000	8x16	1

NOTE: 1. A/N: Alpha/Numeric
2. APA: All Point Addressable (Graphics)

MODE	DISPLAY SIZE	COLORS SHADES	FRAME RATE.	H-SYNC.	VIDEO FREQ.
22	1056x352	16	70	30.5 K	40.0 M
23	1056x350	16	70	30.5 K	40.0 M
24	1056x364	16	70	30.5 K	40.0 M
25	640x480	16	60	31.5 K	25.1 M
26	720x480	16	60	31.5 K	25.1 M
29	800x600	16	56	35.1 K	30.0 M
29*	800x600	16	60	37.9 K	40.0 M
29+	800x600	16	72	48.0 K	50.0 M
29#	800x600	16	75	46.8 K	50.0 M
29##	800x600	16	85	53.7 K	56.3 M
2A	800x600	16	56	35.1 K	36.0 M
2D	640x350	256	70	31.5 K	25.1 M
2E	640x480	256	60	31.5 K	25.1 M
2E*	640x480	256	72	37.9 K	31.5 M
2E+	640x480	256	75	37.5 K	31.5 M
2E++	640x480	256	85	43.4 K	36.0 M
2F	640x400	256	70	31.5 K	25.1 M
30	800x600	256	56	35.1 K	36.0 M
30*	800x600	256	60	37.9 K	40.0 M
30+	800x600	256	72	48.0 K	50.0 M
30#	800x600	256	75	46.8 K	50.0 M
30##	800x600	256	85	53.7 K	56.3 M
37i	1024x768	16	87	35.5 K	44.9 M
37n	1024x768	16	60	48.4 K	65.0 M
37n+	1024x768	16	70	56.5 K	75.0 M
37n#	1024x768	16	75	60.2 K	80.0 M
37n##	1024x768	16	85	68.7 K	94.5 M
38i	1024x768	256	87	35.5 K	44.9 M
38n	1024x768	256	60	48.4 K	65.0 M
38n+	1024x768	256	70	56.5 K	75.0 M
38n#	1024x768	256	75	60.2 K	80.0 M
38n##	1024x768	256	85	68.7 K	94.5 M
39I	1280x1024	16	87	48.8 K	80.0 M
39n	1280x1024	16	60	65.0 K	110.0 M
39n+	1280x1024	16	75	80.0 K	135.0 M
3Ai	1280x1024	256	87	48.8 K	80.0 M
3An	1280x1024	256	60	65.0 K	110.0 M
3An+	1280x1024	256	75	80.0 K	135.0 M

3Bi	1600x1200	16	87	75.6 K	135.0 M
3B	1600x1200	16	60	75.6 K	162.0 M
3B*	1600x1200	16	65	75.6 K	175.5 M
3Ci	1600x1200	256	87	75.6 K	135.0 M
3C	1600x1200	256	60	75.6 K	162.0 M
3C*	1600x1200	256	65	75.6 K	175.5 M
40	320x200	32K	70	31.5 K	25.1 M
41	320x200	64K	70	31.5 K	25.1 M
42	320x200	16.8M	70	31.5 K	25.1 M
43	640x480	32K	60	31.5 K	25.1 M
43*	640x480	32K	72	37.9 K	31.5 M
43+	640x480	32K	75	37.5 K	31.5 M
43++	640x480	32K	85	43.4 K	36.0 M
44	640x480	64K	60	31.5 K	25.1 M
44*	640x480	64K	72	37.9 K	31.5 M
44+	640x480	64K	75	37.5 K	31.5 M
44++	640x480	64K	85	43.4 K	36.0 M
45	640x480	16.8M	60	31.5 K	25.1 M
45*	640x480	16.8M	72	37.9 K	31.5 M
45+	640x480	16.8M	75	37.5 K	31.5 M
45++	640x480	16.8M	85	43.4 K	36.0 M
46	800x600	32K	56	35.1 K	36.0 M
46*	800x600	32K	60	37.9 K	40.0 M
46+	800x600	32K	72	48.0 K	50.0 M
46#	800x600	32K	75	46.8 K	50.0 M
46##	800x600	32K	85	53.7 K	56.3 M
47	800x600	64K	56	35.1 K	36.0 M
47*	800x600	64K	60	37.9 K	40.0 M
47+	800x600	64K	72	48.0 K	50.0 M
47#	800x600	64K	75	46.8 K	50.0 M
47##	800x600	64K	85	53.7 K	56.3 M
48	800x600	16.8M	56	35.1 K	36.0 M
48*	800x600	16.8M	60	37.9 K	40.0 M
48+	800x600	16.8M	72	48.0 K	50.0 M
48#	800x600	16.8M	75	46.8 K	50.0 M
48##	800x600	16.8M	85	53.7 K	56.3 M
49i	1024x768	32K	87	35.5 K	44.9 M
49n	1024x768	32K	60	48.4 K	65.0 M
49n+	1024x768	32K	70	56.5 K	75.0 M
49n#	1024x768	32K	75	60.2 K	80.0 M
49n##	1024x768	32K	85	68.7 K	94.5 M

4Ai	1024x768	64K	87	35.5 K	44.9 M
4An	1024x768	64K	60	48.4 K	65.0 M
4An+	1024x768	64K	70	56.5 K	75.0 M
4An#	1024x768	64K	75	60.2 K	80.0 M
4An##	1024x768	64K	85	68.7 K	94.5 M
4Bi	1024x768	16.8M	87	35.5 K	44.9 M
4Bn	1024x768	16.8M	60	48.4 K	65.0 M
4Bn+	1024x768	16.8M	70	56.5 K	75.0 M
4Bn#	1024x768	16.8M	75	60.2 K	80.0 M
4Bn##	1024x768	16.8M	85	68.7 K	94.5 M
4Ci	1280x1024	32K	89	48.8 K	80.0 M
4Di	1280x1024	64K	89	48.8 K	80.0 M

NOTE: i - interlaced mode
n - noninterlaced mode

- For the limitation of memory bandwidth in 1MB DRAM configuration, the following video modes is not supported in 1MB configuration: modes 45*, 45+, 46+, 46#, 47+, and 47#.

3 Low Resolution Modes

MODE	TYPE	DISPLAY SIZE	COLORS SHADES	ALPHA FORMAT	BUFFER START	BOX SIZE	MAX. PAGES
50	APA	320x240	256	40x30	A000	8x8	1
53	APA	320x240	32K	40x30	A000	8x8	1
56	APA	320x240	64K	40x30	A000	8x8	1
51	APA	400x300	256	50x38	A000	8x8	1
54	APA	400x300	32K	50x38	A000	8x8	1
57	APA	400x300	64K	50x38	A000	8x8	1
52	APA	512x384	256	64x48	A000	8x8	1
55	APA	512x384	32K	64x48	A000	8x8	1
58	APA	512x384	64K	64x48	A000	8x8	1

NOTE: 1. A/N: Alpha/Numeric
2. APA: All Point Addressable (Graphics)

7. Registers Description

- 7.1 to 7.6 are IBM VGA standard registers.
- 7 is SiS6326 Extended Registers, starting from page 81.
- 8 is SiS6326 2D Graphics Engine Registers, starting from page 102.
- 9 is Video Accelerator Registers, starting from page 117.
- 10 is PCI Configuration Registers, starting from page 138.
- 11 is AGP Configuration Registers, starting from page 141.
- 12 is SiS6326 MPEG Video Decoder Registers, starting from page 143.
- 13 is SiS6326 TV OUT Registers, starting from page 150.
- 14 is SiS6326 3D Programming Registers, starting from 165.

1 General Registers

.1 Miscellaneous Output Register

Register Type: Read/Write
Read Port: 3CC
Write Port: 3C2
Default: 00h

D7 Vertical Sync Polarity
0: Select 'positive vertical sync'
1: Select 'negative vertical sync'

D6 Horizontal Sync Polarity
0: Select 'positive horizontal sync'
1: Select 'negative horizontal sync'

Sync Polarity vs. Vertical Screen Resolution

D7	D6	EGA	VGA
0	0	200 Lines	Invalid
0	1	350 Lines	400 Lines
1	0	Invalid	350 Lines
1	1	Invalid	480 Lines

D5 Odd/Even Page
0: Select low page of memory
1: Select high page of memory

D4 Reserved

D[3:2] Clock Select

Table for Video Clock Selection

D3	D2	DCLK
0	0	25.175 MHz
0	1	28.322 MHz

1	0	Don't Care
1	1	For internal clock generator.

D1 Display RAM Enable
0: Disable processor access to video RAM
1: Enable processor access to video RAM
D0 I/O Address Select
0: Sets addresses for monochrome emulation
1: Sets addresses for color graphics emulation

.2 Feature Control Register

Register Type: Read/Write
Read Port: 3CA
Write Port: 3BA/3DA
Default: 00h

D[7:4] Reserved (0)
D3 Vertical Sync Select
0: Normal Vertical Sync output to monitor
1: [Vertical Sync OR Vertical Display Enable] output to monitor
D[2:0] Reserved (0)

.3 Input Status Register 0

Register Type: Read only
Read Port: 3C2
Default: 00h

D7 Vertical Retrace Interrupt Pending
0: Cleared
1: Pending
D[6:5] Reserved
D4 Switch Sense
D[3:0] Reserved

.4 Input Status Register 1

Register Type: Read only
Read Port: 3BA/3DA
Default: 00h

D[7:6] Reserved
D[5:4] Diagnostic

Table for Video Read-back Through Diagnostic Bit (I)

Color Plane Enable Register		**Input Status Register 1**	
D5	**D4**	**D5**	**D4**
0	0	Red	Blue
0	1	Secondary Red	Secondary Green

1	0	Secondary Blue	Green
1	1	Unused	Unused

Table for Video Read-back Through Diagnostic Bit (II)

Color Plane Enable Register		**Input Status Register 1**	
D5	**D4**	**D5**	**D4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

D3 Vertical Trace
0: Inactive
1: Active
D[2:1] Reserved
D0 Display Enable Not
0: Display period
1: Retrace period

.5 VGA Enable Register

Register Type: Read/Write
Read/Write Port: 3C3 or 46E8
Default: 00h

D0 VGA Enable (for 3C3 only)
0: Disable
1: Enable
D3 VGA Enable (for 46E8 only)
0: Disable
1: Enable

.6 Segment Selection Register 0

Register Type: Read/Write
Read/Write Port: 3CD
Default: 00h

If D3 of SRB (Dual Segment Mode Enable bit) sets to 1, then
D[7:6] Reserved
D[5:0] Segment Selection Write Bit[5:0]

If D3 of SRB (Dual Segment Mode Enable bit) sets to 0, then
D[7:4] Segment Selection Write Bit[3:0]
D[3:0] Segment Selection Read Bit[3:0]

.7 Segment Selection Register 1

Register Type: Read/Write
Read/Write Port: 3CB

Default: 00h

If D3 of SRB (Dual Segment Mode Enable bit) sets to 1, then
D[7:6] Reserved
D[5:0] Segment Selection Read Bit[5:0]

If D3 of SRB (Dual Segment Mode Enable bit) sets to 0, then
D[7:0] Reserved

2 CRT Controller Registers

.1 CRT Controller Index Register

Register Type: Read/Write
Read/Write Port: 3B4/3D4
Default: 00h

D[7:0] CRT Controller Index
- 00h ~ 18h for standard VGA
- 19h ~ 26h for SiS extended CRT registers
- 80h ~ BFh for SiS extended video registers

Index (3B4/3D4)	CRT Controller Registers (3B5/3D5)
00h	Horizontal Total
01h	Horizontal Display Enable End
02h	Horizontal Blank Start
03h	Horizontal Blank End
04h	Horizontal Retrace Start
05h	Horizontal Retrace End
06h	Vertical Total
07h	Overflow Register
08h	Preset Row Scan
09h	Max Scan Line/Text Character Height
0Ah	Text Cursor Start
0Bh	Text Cursor End
0Ch	Screen Start Address High
0Dh	Screen Start Address Low
0Eh	Text Cursor Location High
0Fh	Text Cursor Location Low
10h	Vertical Retrace Start
11h	Vertical Retrace End
12h	Vertical Display Enable End
13h	Screen Offset
14h	Underline Location
15h	Vertical Blank Start
16h	Vertical Blank End
17h	Mode Control
18h	Line Compare
19h	Extended Signature Read-Back Register 0
1Ah	Extended Signature Read-Back Register 1
1Bh	CRT horizontal counter read-back
1Ch	CRT vertical counter read back
1Dh	CRT overflow counter read back
1Eh	Extended Signature Read-Back Register 2
22h	Graphics Data Latch Read-back Register

24h	Attribute Controller Toggle Read-back Register
26h	Attribute Controller Index Read-back Register

.2 CR0: Horizontal Total

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 00h
Default: 00h

D[7:0] Horizontal Total Bit[7:0]

.3 CR1: Horizontal Display Enable End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 01h
Default: 00h

D[7:0] Horizontal Display Enable End Bit[7:0]

.4 CR2: Horizontal Blank Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 02h
Default: 00h

D[7:0] Horizontal Blank Start Bit[7:0]

.5 CR3: Horizontal Blank End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 03h
Default: 00h

D7 Reserved
D[6:5] Display Skew Control Bit[1:0]
00: No skew
01: Skew 1 character
10: Skew 2 characters
11: Skew 3 characters
D[4:0] Horizontal Blank End Bit[4:0]

.6 CR4: Horizontal Retrace Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 04h
Default: 00h

D[7:0] Horizontal Retrace Start Bit[7:0]

.7 CR5: Horizontal Retrace End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 05h
Default: 00h

D7 Horizontal Blank End Bit[5]

D[6:5]	Horizontal Retrace Delay Bit[1:0] 00: Skew 0 character clock 01: Skew 1 character clock 10: Skew 2 character clocks 11: Skew 3 character clocks
D[4:0]	Horizontal Retrace End Bit[4:0]

.8 CR6: Vertical Total

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 06h
Default: 00h

D[7:0]	Vertical Total Bit[7:0]

.9 CR7: Overflow Register

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 07h
Default: 00h

D7	Vertical Retrace Start Bit[9]
D6	Vertical Display Enable End Bit[9]
D5	Vertical Total Bit[9]
D4	Line Compare Bit[8]
D3	Vertical Blank Start Bit[8]
D2	Vertical Retrace Start Bit[8]
D1	Vertical Display Enable End Bit[8]
D0	Vertical Total Bit[8]

.10 CR8: Preset Row Scan

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 08h
Default: 00h

D7	Reserved
D[6:5]	Byte Panning Control Bit[1:0]
D[4:0]	Preset Row Scan Bit[4:0]

.11 CR9: Maximum Scan Line/Text Character Height

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 09h
Default: 00h

D7	Double Scan 0: Disable 1: Enable 400 lines display
D6	Line Compare Bit[9]
D5	Vertical Blank Start Bit[9]
D[4:0]	Character Cell Height Bit[4:0]

.12 CRA: Text Cursor Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Ah
Default: 00h

D[7:6]	Reserved
D5	Text Cursor Off 0: Text Cursor On 1: Text Cursor Off
D[4:0]	Text Cursor Start Bit[4:0]

.13 CRB: Text Cursor End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Bh
Default: 00h

D7	Reserved
D[6:5]	Text Cursor Skew 00: No skew 01: Skew one character clock 10: Skew two character clocks 11: Skew three character clocks
D[4:0]	Text Cursor End Bit[4:0]

.14 CRC: Screen Start Address High

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Ch
Default: 00h

D[7:0]	Screen Start Address Bit[15:8]

.15 CRD: Screen Start Address Low

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Dh
Default: 00h

D[7:0]	Screen Start Address Bit[7:0]

.16 CRE: Text Cursor Location High

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Eh
Default: 00h

D[7:0]	Text Cursor Location Bit[15:8]

.17 CRF: Text Cursor Location Low

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Fh
Default: 00h

D[7:0]	Text Cursor Location Bit[7:0]

.18 CR10: Vertical Retrace Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 10h
Default: 00h

D[7:0]	Vertical Retrace Start Bit[7:0]

.19 CR11: Vertical Retrace End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 11h
Default: 00h

D7	Write Protect for CR0 to CR7 0: Disable Write Protect 1: Enable Write Protect
D6	Alternate Refresh Rate 0: Selects three refresh cycles per scanline 1: Selects five refresh cycles per scanline
D5	Vertical Interrupt Enable 0: Enable 1: Disable
D4	Vertical Interrupt Clear 0: Clear 1: Not Clear
D[3:0]	Vertical Retrace End Bit[3:0]

.20 CR12: Vertical Display Enable End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 12h
Default: 00h

D[7:0]	Vertical Display Enable End Bit[7:0]

.21 CR13: Screen Offset

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 13h
Default: 00h

D[7:0]	Screen Offset Bit[7:0]

.22 CR14: Underline Location Register

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 14h
Default: 00h

D7	Reserved
D6	Double-word Mode Enable 0: Disable 1: Enable
D5	Count by 4

0: Disable
1: Enable

D[4:0] Underline Location Bit[4:0]

.23 CR15: Vertical Blank Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 15h
Default: 00h

D[7:0] Vertical Blank Start Bit[7:0]

.24 CR16: Vertical Blank End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 16h
Default: 00h

D[7:0] Vertical Blank End Bit[7:0]

.25 CR17: Mode Control Register

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 17h
Default: 00h

D7 Hardware Reset
0: Disable horizontal and vertical retrace outputs
1: Enable horizontal and vertical retrace outputs

D6 Word/Byte Address Mode
0: Set the memory address mode to word
1: Set the memory address mode to byte

D5 Address Wrap
0: Disable the full 256K of memory
1: Enable the full 256K of memory

D4 Reserved

D3 Count by Two
0: Byte refresh
1: Word refresh

D2 Horizontal Retrace Select
0: Normal
1: Double Scan

D1 RA1 replace MA14
0: Enable
1: Disable

D0 RA0 replace MA13
0: Enable
1: Disable

.26 CR18: Line Compare Register

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 18h

Default: 00h

D[7:0] Line Compare Bit[7:0]

.27 CR19: Extended Signature Read-back Register 0

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 19h
Default: xxh

D[7:0] Signature read-back bit[7:0]

.28 CR1A: Extended Signature Read-back Register 1

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Ah
Default: xxh

D[7:0] Signature read-back bit[15:8]

.29 CR1B: CRT Horizontal Counter Read Back

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Bh
Default: xxh

D[7:0] CRT horizontal counter bit[7:0]

.30 CR1C: CRT Vertical Counter Read Back

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Ch
Default: xxh

D[7:0] CRT vertical counter bit[7:0]

.31 CR1D: CRT Overflow Counter Read Back

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Dh
Default: xxh

D[7:5] Reserved
D4 CRT horizontal counter bit 8
D3 Reserved
D[2:0] CRT vertical counter bit[10:8]

Note: The horizontal and vertical counter value will be latched when read register CR20. So the three registers value should be read after read CR20.

.32 CR1E: Extended Signature Read-Back Register 2

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Eh
Default: xxh

D[7:0] Signature read-back bit[23:16]

.33 CR20: CRT Counter Trigger Port

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 20h
Default: xxh

D[7:0]	Reserved

.34 CR22: Graphics Data Latch Read-back Register

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 22h
Default: xxh

D[7:0]	Graphics Data Latch bit[7:0]

.35 CR24: Attribute Controller Toggle Read-back Register

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 24h
Default: xxh

D7	Attribute Controller Toggle
D[6:0]	Reserved

.36 CR26: Attribute Controller Index Read-back Register

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 26h
Default: xxh

D[7:6]	Reserved
D5	Video Enable
D[4:0]	Attribute Controller Index bit[8:4]

3 Sequencer Registers

.1 Sequencer Index Register

Register Type: Read/Write
Read/Write Port: 3C4
Default: 00h

D[7:6]	Reserved
D[5:0]	Sequencer Index Bit[5:0]

Table of Sequencer Registers

Index (3C4)	Sequencer Register (3C5)
00	Reset Register
01	Clock Mode
02	Color Plane Write Enable
03	Character Generator Select
04	Memory Mode

.2 SR0: Reset Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 00h
Default: 00h

D[7:2]	Reserved
D1	Synchronous reset 0: Reset 1: Normal
D0	Asynchronous reset 0: Reset 1: Normal

.3 SR1: Clock Mode Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 01h
Default: 00h

D[7:6]	Reserved
D5	Screen Off 0: Display On 1: Display Off
D4	Shifter Load 32 enable 0: Disable 1: Data shifter loaded every 4th Character Clock
D3	Dot Clock Divide by 2 enable 0: Disable 1: Video Clock is divided by 2 to generate Dot Clock
D2	Shifter Load 16 (while D4=0)

0: Disable
1: Data shifter loaded every 2nd Character Clock

D1 Reserved

D0 8/9 Dot Clock
0: Dot Clock is divided by 9 to generate Character Clock
1: Dot Clock is divided by 8 to generate Character Clock

.4 SR2: Color Plane Write Enable Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 02h
Default: 00h

D[7:4] Reserved

D3 Plane 3 write enable
0: Disable
1: Enable

D2 Plane 2 write enable
0: Disable
1: Enable

D1 Plane 1 write enable
0: Disable
1: Enable

D0 Plane 0 write enable
0: Disable
1: Enable

.5 SR3: Character Generator Select Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 03h
Default: 00h

D[7:6] Reserved

D5 Character generator table B select Bit[2]

D4 Character generator table A select Bit[2]

D[3:2] Character generator table B select Bit[1:0]

D[1:0] Character generator table A select Bit[1:0]

Table of Selecting Active Character Generator

D5	**D3**	**D2**	**Used when text attribute bit 3 is 1**
D4	**D1**	**D0**	**Used when text attribute bit 3 is 0**
0	0	0	Character Table 1
0	0	1	Character Table 2
0	1	0	Character Table 3
0	1	1	Character Table 4
1	0	0	Character Table 5 (VGA only)
1	0	1	Character Table 6 (VGA only)
1	1	0	Character Table 7 (VGA only)

1	1	1	Character Table 8 (VGA only)

.6 SR4: Memory Mode Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 04h
Default: 00h

D[7:4]	Reserved
D3	Chain-4 Mode enable 0: Disable 1: Enable
D2	Odd/Even Mode enable 0: Enable 1: Disable
D1	Extended Memory 0: Select 64K 1: Select 256K
D0	Reserved

4 Graphics Controller Registers

.1 Graphics Controller Index Register

Register Type: Read/Write
Read/Write Port: 3CE
Default: 00h

D[7:4] Reserved
D[3:0] Graphics Controller Index Bit[3:0]

Index (3CE)	Graphics Controller Register (3CF)
00	Set/Reset Register
01	Set/Reset Enable Register
02	Color Compare Register
03	Data Rotate & Function Select
04	Read Plane Select Register
05	Mode Register
06	Miscellaneous Register
07	Color Don't Care Register
08	Bit Mask Register

.2 GR0: Set/Reset Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 00h
Default: 00h

D[7:4] Reserved
D3 Set/Reset Map for plane 3
D2 Set/Reset Map for plane 2
D1 Set/Reset Map for plane 1
D0 Set/Reset Map for plane 0

.3 GR1: Set/Reset Enable Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 01h
Default: 00h

D[7:4] Reserved
D3 Enable Set/Reset for plane 3
0: Disable
1: Enable
D2 Enable Set/Reset for plane 2
0: Disable
1: Enable
D1 Enable Set/Reset for plane 1
0: Disable
1: Enable

D0 Enable Set/Reset for plane 0
0: Disable
1: Enable

.4 GR2: Color Compare Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 02h
Default: 00h

D[7:4] Reserved
D3 Color Compare Map for plane 3
D2 Color Compare Map for plane 2
D1 Color Compare Map for plane 1
D0 Color Compare Map for plane 0

.5 GR3: Data Rotate/Function Select Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 03h
Default: 00h

D[7:5] Reserved
D[4:3] Function Select

Table of Function Select

D4	D3	Function
0	0	write data unmodified
0	1	write data AND processor latches
1	0	write data OR processor latches
1	1	write data XOR processor latches

D[2:0] Rotate Count

Table of Rotate Count

D2	D1	D0	Right Rotation
0	0	0	none
0	0	1	1 bits
0	1	0	2 bits
0	1	1	3 bits
1	0	0	4 bits
1	0	1	5 bits
1	1	0	6 bits
1	1	1	7 bits

.6 GR4: Read Plane Select Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 04h
Default: 00h

D[7:2] Reserved
D[1:0] Read Plane Select bit 1, 0
00: Plane 0
01: Plane 1
10: Plane 2
11: Plane 3

.7 GR5: Mode Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 05h
Default: 00h

D7 Reserved
D6 256-color Mode
0: Disable
1: Enable
D5 Shift Register Mode
0: Configure shift register to be EGA compatible
1: Configure shift register to be CGA compatible
D4 Odd/Even Addressing Mode enable
0: Disable
1: Enable
D3 Read Mode
0: Map Select Read
1: Color Compare Read
D2 Reserved
D[1:0] Write mode

Table for Write Mode

D1	D0	Mode Selected
0	0	*Write Mode 0:* Direct processor write (Data Rotate, Set/Reset may apply).
0	1	*Write Mode 1:* Use content of latches as write data.
1	0	*Write Mode 2:* Color Plane n(0-3) is filled with the value of bit m in the processor write data.
1	1	*Write Mode 3:* Color Plane n(0-3) is filled with 8 bits of the color value contained in the Set/Reset Register for that plane. The Enable Set/Reset Register is not effective. Processor data will be AND with Bit Mask Register content to form new bit mask pattern. (data rotate may apply)

.8 GR6: Miscellaneous Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 06h
Default: 00h

D[7:4] Reserved

D[3:2] Memory Address Select

Table of Memory Address Select

D3	D2	Address range
0	0	A0000 to BFFFF
0	1	A0000 to AFFFF
1	0	B0000 to B7FFF
1	1	B8000 to BFFFF

D1 Chain Odd And Even Maps
0: Disable
1: Enable

D0 Graphics Mode Enable
0: Select alphanumeric mode
1: Select graphics mode

.9 GR7: Color Don't Care Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 07h
Default: 00h

D[7:4] Reserved

D3 Plane 3 Don't Care
0: Disable color comparison
1: Enable color comparison

D2 Plane 2 Don't Care
0: Disable color comparison
1: Enable color comparison

D1 Plane 1 Don't Care
0: Disable color comparison
1: Enable color comparison

D0 Plane 0 Don't Care
0: Disable color comparison
1: Enable color comparison

.10 GR8: Bit Mask Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 08h
Default: 00h

D[7:0] Bit Mask Enable Bit[7:0]

5 Attribute Controller and Video DAC Registers

.1 Attribute Controller Index Register

Register Type: Read/Write
Read Port: 3C0
Write Port: 3C0
Default: 00h

D[7:6] Reserved
D5 Palette Address Source
0: From CPU
1: From CRT
D[4:0] Attribute Controller Index Bit[4:0] (00h-14h)

Index (3C0)	Attribute Controller Register (3C0)
00h	Color Palette Register 0
01h	Color Palette Register 1
02h	Color Palette Register 2
03h	Color Palette Register 3
04h	Color Palette Register 4
05h	Color Palette Register 5
06h	Color Palette Register 6
07h	Color Palette Register 7
08h	Color Palette Register 8
09h	Color Palette Register 9
0Ah	Color Palette Register 10
0Bh	Color Palette Register 11
0Ch	Color Palette Register 12
0Dh	Color Palette Register 13
0Eh	Color Palette Register 14
0Fh	Color Palette Register 15
10h	Mode Control Register
11h	Screen Border Color
12h	Color Plane Enable Register
13h	Pixel Panning Register
14h	Color Select Register (VGA)

.2 AR0~ARF: Palette Registers

Register Type: Read/Write
Read Port: 3C1, Index 00h ~ 0Fh
Write Port: 3C0, Index 00h ~ 0Fh
Default: 00h

D[7:6] Reserved
D[5:0] Palette Entries

.3 AR10: Mode Control Register

Register Type: Read/Write
Read Port: 3C1, Index 10h
Write Port: 3C0, Index 10h
Default: 00h

D7 P4, P5 Source Select
0: AR0-F Bit[5:4] are used as the source for the Lookup Table Address Bit[5:4]
1: AR14 Bit[1:0] are used as the source for the Lookup Table Address Bit[5:4]

D6 Pixel Double Clock Select
0: The pixels are clocked at every clock cycle
1: The pixels are clocked at every other clock cycle

D5 PEL Panning Compatibility with Line Compare
0: Disable
1: Enable

D4 Reserved

D3 Background Intensity or Blink enable (while the Character Attribute D7=1)
0: Background Intensity attribute enable
1: Background Blink attribute enable

D2 Line Graphics enable
0: The ninth bit of nine-bit-wide character cell will be the same as the background.
1: The ninth bit of nine-bit-wide character cell will be made be the same as the eighth bit for character codes in the range C0h through DFh.

D1 Display Type
0: The contents of the Attribute byte are treated as color attribute.
1: The contents of the Attribute byte are treated as MDA-compatible attribute.

D0 Graphics/Text Mode
0: The Attribute Controller will function in text mode.
1: The Attribute Controller will function in graphics mode.

.4 AR11: Screen Border Color

Register Type: Read/Write
Read Port: 3C1, Index 11h
Write Port: 3C0, Index 11h
Default: 00h

D[7:6] Reserved
D[5:0] Palette Entry

.5 AR12: Color Plane Enable Register

Register Type: Read/Write
Read Port: 3C1, Index 12h
Write Port: 3C0, Index 12h
Default: 00h

D[7:6] Reserved

D[5:4] Display Status MUX Bit[1:0]
These bits select two of the eight bits color outputs to be available in the status register. The output color combinations available on the status bits are as follows:

Table for Video Read-back Through Diagnostic Bit (I)

Color Plane Enable Register		Input Status Register 1 (Refer to .4 on page 57)	
D5	**D4**	**D5**	**D4**
0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Unused	Unused

Table for Video Read-back Through Diagnostic Bit (II)

Color Plane Enable Register		Input Status Register 1 (Refer to .4 on page 57)	
D5	**D4**	**D5**	**D4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

D[3:0] Enable Color Plane Bit[3:0]

.6 AR13: Pixel Panning Register

Register Type: Read/Write
Read Port: 3C1, Index 13h
Write Port: 3C0, Index 13h
Default: 00h

D[7:4] Reserved

D[3:0] Pixel Pan Bit[3:0]
This field specifies the number of pixels the display data will be shifted to the left. This field is interpreted as indicated in the following table:

D3	D2	D1	D0	Monochrome Text	VGA Mode 13	All others
0	0	0	0	8	0	0
0	0	0	1	0	Invalid	1
0	0	1	0	1	1	2
0	0	1	1	2	Invalid	3
0	1	0	0	3	2	4
0	1	0	1	4	Invalid	5
0	1	1	0	5	3	6
0	1	1	1	6	Invalid	7
1	0	0	0	7	Invalid	Invalid
1	0	0	1	Invalid	Invalid	Invalid

1	0	1	0	Invalid	Invalid	Invalid
1	0	1	1	Invalid	Invalid	Invalid
1	1	0	0	Invalid	Invalid	Invalid
1	1	0	1	Invalid	Invalid	Invalid
1	1	1	0	Invalid	Invalid	Invalid
1	1	1	1	Invalid	Invalid	Invalid

.7 AR14: Color Select Register

Register Type: Read/Write
Read Port: 3C1, Index 14h
Write Port: 3C0, Index 14h
Default: 00h

D[7:4] Reserved

D[3:2] Color Bit[7:6]
These two bits are concatenated with the six bits from the Palette Register to form the address into the LUT and to drive P[7:6].

D[1:0] Color Bit[5:4]
If AR10 D7 is programmed to a '1', these two bits replace the corresponding two bits from the Palette Register to form the address into the LUT and to drive P[5:4]. If AR10 D7 is programmed to a '0', these two bits are ignored.

6 Color Registers

.1 DAC Status Register

Register Type: Read Only
Read Port: 3C7
Default: 00h

D[7:2] Reserved
D[1:0] DAC State Bit[1:0]
00: Write Operation in progress
11: Read Operation in progress

.2 DAC Index Register (Read Mode)

Register Type: Write Only
Write Port: 3C7
Default: 00h

D[7:0] DAC Index Bit[7:0]

.3 DAC Index Register (Write Mode)

Register Type: Read/Write
Read/Write Port: 3C8
Default: 00h

D[7:0] DAC Index Bit[7:0]

.4 DAC Data Register

Register Type: Read/Write
Read/Write Port: 3C9
Default: 00h

When SR7 D2 = 1 (refer to ".4" on page 83),

D[7:6] Reserved
D[5:0] DAC Data [5:0]
Before writing to this register, 3C8h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue values for the DAC entry are written. After the third value is written, the values are transferred to the LUT and the DAC index is incremented in case new values for the next DAC index are to be written.
Before reading from this register, 3C7h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue value for the DAC entry may be read from this DAC index. After the third value is read, the DAC index is incremented in case the value for the next DAC index to be read.

When SR7 D2 = 0 (refer to ".4" on page 83),

D[7:0] DAC Data [7:0]
When SR7 D2 = 0, the 24-bit LUT is enabled. This LUT can translate the R, G, B values into new R, G, B values independently. This LUT can be used for performing GAMMA correction function. The programming

procedure is same as standard LUT when SR7 D2 = 1.

.5 PEL Mask Register

Register Type: Read/Write
Read/Write Port: 3C6
Default: 00h

D[7:0] Pixel Mask Bit[7:0]
This field is the Pixel Mask for the palette DAC. If a bit in this field is programmed to a '0', the corresponding bit in the pixel data will be ignored in looking up an entry in the LUT.

7 SiS6326 Extended Registers

.1 Extended Index Register

Register Type: Read/Write
Read/Write Port: 3C4
Default: 00h

D[7:6] Reserved
D[5:0] Extended Register Index Bit[5:0] (05h ~ 37h)

Index (3C4)	Extended Enhanced Register (3C5)
05h	Extended Password/Identification Register
06h	Extended Graphics Mode Control Register
07h	Extended Misc. Control Register 0
08h	Extended CRT/CPU Threshold Control Register 0
09h	Extended CRT/CPU Threshold Control Register 1
0Ah	Extended CRT Overflow Register
0Bh	Extended Misc. Control Register 1
0Ch	Extended Misc. Control Register 2
0Dh	Extended Configuration Status 0
0Eh	Extended Configuration Status 1
0Fh	Extended Scratch Register 0
10h	Extended Scratch Register 1
11h	Extended DDC and Power Control Register
12h	Extended Horizontal Overflow Register
13h	Extended Clock Generator Register
13h	Extended 25Mhz Video Clock Register 2
13h	Extended 28Mhz Video Clock Register 2
14h	Extended Hardware Cursor Color 0 Red Register
15h	Extended Hardware Cursor Color 0 Green Register
16h	Extended Hardware Cursor Color 0 Blue Register
17h	Extended Hardware Cursor Color 1 Red Register
18h	Extended Hardware Cursor Color 1 Green Register
19h	Extended Hardware Cursor Color 1 Blue Register
1Ah	Extended Hardware Cursor Horizontal Start Register 0
1Bh	Extended Hardware Cursor Horizontal Start Register 1
1Ch	Extended Hardware Cursor Horizontal Preset Register
1Dh	Extended Hardware Cursor Vertical Start Register 0
1Eh	Extended Hardware Cursor Vertical Start Register 1
1Fh	Extended Hardware Cursor Vertical Preset Register
20h	Extended Linear Addressing Base Address Register 0
21h	Extended Linear Addressing Base Address Register 1
22h	Extended Standby/Suspend Timer Register
23h	Extended Misc. Control Register 3
24h	Extended Reserved Register

25h	Extended Scratch Register 2
26h	Extended Graphics Engine Register 0
27h	Extended Graphics Engine Register 1
28h	Extended Internal Memory Clock Register 0
29h	Extended Internal Memory Clock Register 1
2Ah	Extended Internal Video Clock Register 0
2Ah	Extended 25Mhz Video Clock Register 0
2Ah	Extended 28Mhz Video Clock Register 0
2Bh	Extended Internal Video Clock Register 1
2Bh	Extended 25Mhz Video Clock Register 1
2Bh	Extended 28Mhz Video Clock Register 1
2Ch	Extended Turbo Queue Base Address
2Dh	Extended Memory Start Control Register
2Eh	Extended Reserved Register
2Fh	Extended DRAM Frame Buffer Size Register
30h	Extended Fast Page Flip Starting Address Low Register
31h	Extended Fast Page Flip Starting Address Middle Register
32h	Extended Fast Page Flip Starting Address High Register
33h	Extended Misc. Control Register 4
34h	Extended Misc. Control Register 5
35h	Extended Misc. Control Register 6
36h	Extended Scratch Register 3
37h	Extended Scratch Register 4
38h	Extended Misc. Control Register 7
39h	Extended Misc. Control Register 8
3Ah	Extended MPEG Turbo Queue Base Address
3Bh	Extended Clock Generator Control Register
3Ch	Extended Misc. Control Register 9

.2 SR5: Extended Password/Identification Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 05h
Default: 00h

D[7:0] Password/Identification Bit[7:0]
If 86h is written into this register, then A1h will be read from this register, and unlock all the extension registers.
If the value other than 86h is written into this register, then 21h will be read from this register, and lock all the extension registers.

.3 SR6: Extended Graphics Mode Control Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 06h
Default: 00h

D7 Graphics mode linear addressing enable
0: Disable
1: Enable

D6 Graphics mode hardware cursor display enable
0: Disable
1: Enable

D5 Graphics mode interlaced enable
0: Disable
1: Enable

D4 True-Color graphics mode enable
0: Disable
1: Enable

D3 64K-Color graphics mode enable
0: Disable
1: Enable

D2 32K-Color graphics mode enable
0: Disable
1: Enable

D1 Enhanced graphics mode enable
0: Disable
1: Enable

D0 Enhanced text mode enable
0: Disable
1: Enable

.4 SR7: Extended Misc. Control Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 07h
Default: 00h

D7 Merge video line buffer into CRT FIFO
0: Disable
1: Enable
The size of CRT FIFO can be set to 256x64 bit when merged with video line buffer only when video playback is disabled.

D6 Enable feature connector (VIDEO 0-7, PCLK) output
0: Disable
1: Enable

D5 Internal RAMDAC power saving mode
0: Power saving mode
1: High power mode

D4 Extended video clock frequency divided by 2
0: Disable
1: Enable

D3 Enable multi-line pre-fetch
0: Enable
1: Disable

D2	24-bit color palette enable for direct color mode 0: Enable 1: Disable
D1	High Speed DAC operation 0: Low speed 1: High Speed This bit should be set when DCLK frequency is greater than 135MHz
D0	External DAC reference voltage input 0: Internal DAC reference voltage 1: External DAC reference voltage To achieve more accurate reference voltage. The reference voltage of DAC can be input from external.

.5 SR8: Extended CRT/CPU Threshold Control Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 08h
Default: 00h

D[7:4]	CRT/CPU Arbitration Threshold Low Bit[3:0]
D[3:0]	CRT/Engine Threshold High Bit[3:0]

.6 SR9: Extended CRT/CPU Threshold Control Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 09h
Default: 00h

D[7:4]	ASCII/Attribute Threshold Bit[3:0]
D[3:0]	CRT/CPU Threshold High Bit[3:0]

.7 SRA: Extended CRT Overflow Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 0Ah
Default: 00h

D[7:4]	Extended Screen Offset Bit[11:8]
D3	Extended Vertical Retrace Start Bit[10]
D2	Extended Vertical Blank Start Bit[10]
D1	Extended Vertical Display Enable End Bit[10]
D0	Extended Vertical Total Bit[10]

.8 SRB: Extended Misc. Control Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 0Bh
Default: 00h

D7	True-Color Graphics mode RGB Sequence Selection 0: Red, Green, and Blue in byte order 1: Blue, Green, and Red in byte order
D[6:5]	Memory-mapped I/O Space Selection Bit[1:0]

00: Disable
01: Select Axxxxh as Memory-mapped I/O Space
10: Select Bxxxxh as Memory-mapped I/O Space
11: Select PCI config register 14H as Memory-mapped I/O space

D4 True-Color frame rate modulation enable
0: Disable
1: Enable

D3 Dual segment register mode enable
0: Disable
1: Enable

D2 I/O gating enable while write-buffer is not empty
0: Disable
1: Enable

D1 16-color packed pixel enable
0: Disable
1: Enable

D0 CPU-driven BITBLT operation enable
0: Disable
1: Enable

.9 SRC: Extended Misc. Control Register 2

Register Type: Read/Write
Read/Write Port: 3C5, Index 0Ch
Default: 00h

D7 Graphics mode 32-bit memory access enable
0: Disable
1: Enable

D6 Text mode 16-bit memory access enable
0: Disable
1: Enable

D5 Read-ahead cache operation enable
0: Disable
1: Enable

D4 Reserved

D3 Test mode enable
0: Disable
1: Enable

D[2:1] Memory Configuration Bit[1:0]
00: 1MByte/1 bank
01: 2MByte/2 banks
10: 4MByte/2 banks or 4 banks
11: 1MByte/2 banks

D0 Synchronous reset timing generator enable
0: Disable
1: Enable

.10 SRD: Extended Configuration Status 0

Register Type: Read Only
Read Port: 3C5, Index 0Dh
Default: 00h

D7 Enable 64K ROM decoding
0: Disable
1: Enable when MD23 is pulled up with resistor.

D6 Clock Generator Selection
0: Select internal clock generator
1: Select external clock generator (used for SiS internal test only) when MD22 is pulled up with resistor

D5 AGP 2X Transfer Mode enable
0: Disable
1: Enable AGP 2X Transfer Mode when MD21 is pulled up with resistor.

D4 AGP bus enable
0: Disable
1: Enable AGP bus when MD20 is pulled up with resistor.

D3 Reserved (i.e. MD19 is reserved.)

D2 NTSC/PAL select
0: NTSC
1: PAL when MD18 is pulled up with resistor

D1 Video subsystem enable/disable at power-on is
0: Controlled by System BIOS
1: Forced to disable when MD17 is pulled up with resistor.

D0 Select I/O address 3C3h or 46E8h as video subsystem port
0: Select 3C3h
1: Select 46E8h when MD16 is pulled up with resistor.

.11 SRE: Extended Configuration Status 1

Register Type: Read Only
Read Port: 3C5, Index 0Eh
Default: 00h

D[7:5] DRAM speed setting bit[2:0]
0: MD[31:29] not pulled-up with resistors
1: MD[31:29] pulled-up with resistors

	SGRAM	2-cycle EDO	1-cycle EDO	Fast Page
000	66	65	50	55
001	75	70	55	60
010	83	75	60	65
011	90	80	65	70
100	100	85	70	75
101	115	90	75	80
110	134	55	80	45
111	50	60	45	50

D4	Enable VMI Interface 0: Enable 1: Disable when MD28 is pulled up with resistor.
D3	INTA# Selection 0: Disable 1: Enable when MD27 is pulled up with resistor
D2	BIOS ROM decoding logic 0: Enable 1: Disable when MD26 is pulled up with resistor.
D[1:0]	Reserved (i.e. MD[25:24] are reserved.)

.12 SRF: Extended Scratch Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 0Fh
Default: 00h

D[7:0]	Reserved for video BIOS

.13 SR10: Extended Scratch Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 10h
Default: 00h

D[7:0]	Reserved for video BIOS

.14 SR11: Extended DDC and Power Control Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 11h
Default: 00h

D7	Force VGA into suspend mode 0: Disable 1: Enable
D6	Force VGA into standby mode 0: Disable 1: Enable
D5	Enable video memory access as activation source 0: Disable 1: Enable
D4	Enable keyboard and hardware cursor as system activation source 0: Disable 1: Enable
D[3:2]	Reserved
D1	DDC DATA Programming While writing this bit, 0: Output '0' logic into DDC Data Signal. 1: Output '1' logic into DDC Data Signal. While reading this bit, 0: Get '0' logic from DDC Data Signal .

1: Get '1' logic from DDC Data Signal .

D0 DDC CLK Programming
While writing this bit,
0: Output '0' logic into DDC Clock Signal.
1: Output '1' logic into DDC Clock Signal.
While reading this bit,
0: Get '0' logic from DDC Clock Signal .
1: Get '1' logic from DDC Clock Signal .

.15 SR12: Extended Horizontal Overflow Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 12h
Default: 00h

D[7:5] Horizontal Retrace Skew
000 : no delay
001 : delay 1 DCLK
010 : delay 2 DCLK
011 : delay 3 DCLK
100 : delay 4 DCLK
101 : delay 5 DCLK
110 : delay 6 DCLK
111 : delay 7 DCLK

D4 Extended Horizontal Blank End Bit[6]
D3 Extended Horizontal Retrace Start Bit[8]
D2 Extended Horizontal Blank Start Bit[8]
D1 Extended Horizontal Display Enable End Bit[8]
D0 Extended Horizontal Total Bit[8]

.16 SR13: Extended Clock Generator Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 13h
Default: 00h

D7 MCLK Post-scale Bit[2]
D6 Internal VCLK Post-Scale Bit[2]
D[5:0] Reserved

.17 SR13-1: Extended 25Mhz Video Clock Register 2

Register Type: Read/Write
Read/Write Port: 3C5, Index 13h
Default: 00h

D7 Reserved
D6 25Mhz VCLK Post-Scale Bit[2]
D[5:0] Reserved

.18 SR13-2: Extended 28Mhz Video Clock Register 2

Register Type: Read/Write

Read/Write Port: 3C5, Index 13h
Default: 00h

D7	Reserved
D6	28Mhz VCLK Post-Scale Bit[2]
D[5:0]	Reserved

.19 SR14: Extended Hardware Cursor Color 0 Red Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 14h
Default: 00h

D[7:6]	Reserved
D[5:0]	Hardware Cursor Color 0 Red Bit[5:0]

.20 SR15: Extended Hardware Cursor Color 0 Green Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 15h
Default: 00h

D[7:6]	Reserved
D[5:0]	Hardware Cursor Color 0 Green Bit[5:0]

.21 SR16: Extended Hardware Cursor Color 0 Blue Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 16h
Default: 00h

D[7:6]	Reserved
D[5:0]	Hardware Cursor Color 0 Blue Bit[5:0]

.22 SR17: Extended Hardware Cursor Color 1 Red Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 17h
Default: 00h

D[7:6]	Reserved
D[5:0]	Hardware Cursor Color 1 Red Bit[5:0]

.23 SR18: Extended Hardware Cursor Color 1 Green Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 18h
Default: 00h

D[7:6]	Reserved
D[5:0]	Hardware Cursor Color 1 Green Bit[5:0]

.24 SR19: Extended Hardware Cursor Color 1 Blue Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 19h
Default: 00h

D[7:6] Reserved
D[5:0] Hardware Cursor Color 1 Blue Bit[5:0]

.25 SR1A: Extended Hardware Cursor Horizontal Start Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Ah
Default: 00h

D[7:0] Hardware Cursor Horizontal Start Bit[7:0]

.26 SR1B: Extended Hardware Cursor Horizontal Start Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Bh
Default: 00h

D[7:3] Reserved
D[2:0] Hardware Cursor Horizontal Start Bit[10:8]

.27 SR1C: Extended Hardware Cursor Horizontal Preset Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Ch
Default: 00h

D[7:6] Reserved
D[5:0] Hardware Cursor Horizontal Preset Bit[5:0]

.28 SR1D: Extended Hardware Cursor Vertical Start Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Dh
Default: 00h

D[7:0] Hardware Cursor Vertical Start Bit[7:0]

.29 SR1E: Extended Hardware Cursor Vertical Start Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Eh
Default: 00h

D[7:4] Hardware Cursor Pattern Select Bit[3:0]
D3 Hardware Cursor Side Pattern Enable
0: Disable
1: Enable
D[2:0] Hardware Cursor Vertical Start Bit[10:8]

.30 SR1F: Extended Hardware Cursor Vertical Preset Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Fh
Default: 00h

D[7:6] Reserved
D[5:0] Hardware Cursor Vertical Preset Bit[5:0]

.31 SR20: Extended Linear Addressing Base Address Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 20h
Default: 00h

D[7:0]	Linear Addressing Base Address Bit[26:19]

.32 SR21: Extended Linear Addressing Base Address Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 21h
Default: 00h

D7	Reserved
D[6:5]	Linear Addressing Space Aperture Bit[1:0] 00: 512 Kbyte 01: 1 Mbyte 10: 2 Mbyte 11: 4 MByte
D[4:0]	Linear Addressing Base Address Bit[31:27]

.33 SR22: Extended Standby/Suspend Timer Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 22h
Default: 00h

D[7:4]	Suspend Timer Bit[3:0] The resolution for Suspend Timer is 2 minutes.
D[3:0]	Standby Timer Bit[3:0] The resolution for Standby Timer is 2 minutes.

.34 SR23: Extended Misc. Control Register 3

Register Type: Read/Write
Read/Write Port: 3C5, Index 23h
Default: 00h

D7	Reserved
D6	CRC Generator Enable 0: Disable 1: Enable
D5	EDO DRAM Enable Bit 0: Disable 1: Enable
D4	Bypass SRAM 0: Disable 1: Enable
D3	Video Compatible Hardware Cursor Visibility Enable 0: Disable 1: Enable
D[2:0]	DRAM Control Signal Delay Compensation Bit[1:0]

000: Delay 4 ns
001: Delay 5 ns
010: Delay 6 ns
011: Delay 7 ns
100: Delay 8 ns
101: Delay 9 ns
110: Delay 10 ns
111: Delay 11 ns

.35 SR24: Extended Reserved Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 24h
Default: 00h

D[7:0]	Reserved

.36 SR25: Extended Scratch Register 2

Register Type: Read/Write
Read/Write Port: 3C5, Index 25h
Default: 00h

D[7:0]	Reserved for VGA BIOS

.37 SR26: Extended Graphics Engine Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 26h
Default: 00h

D7	Reserved
D6	Power-down Internal RAMDAC 0: Disable 1: Enable
D5	PCI Burst-Write Mode enable 0: Disable 1: Enable
D4	Continuous Memory Data Access Enable Bit 0: Disable 1: Enable
D3	Reserved
D2	Slow DRAM RAS pre-charge time 0: Disable (3 MCLK/DRAM cycle) 1: Enable (4 MCLK/DRAM cycle)
D1	Slow FP/EDO DRAM RAS* to CAS* Timing enable 0: Disable (7 MCLK/DRAM cycle) 1: Enable (8 MCLK/DRAM cycle)
D0	Reserved

.38 SR27: Extended Graphics Engine Register 1

Register Type: Read/Write

Read/Write Port: 3C5, Index 27h
Default: 00h

D7	Turbo Queue Engine enable 0: Disable 1: Enable
D6	Graphics Engine Register Programming enable 0: Disable 1: Enable
D[5:4]	Logical Screen Width and Byte-Per-Pixel Select Bit[1:0] 00 1024, 256 colors or 512, 32k/64k colors 01 2048, 256 colors or 1024, 32k/64k colors 10 4096, 256 colors or 2048, 32k/64k colors 11 invalid
D[3:0]	Extended Screen Start Address Bit[19:16]

.39 SR28: Extended Internal Memory Clock Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 28h
Default: 00h

D[7]	MCLK Divider 0: Do not divide 1: Divide by 2
D[6:0]	MCLK Numerator Bit[6:0] [0000000:1111111] = [1:128]

NOTE: For the operation of internal memory clock generation, please refer to "7 Internal Dual-Clock Synthesizer" on Page 25.

.40 SR29: Extended Internal Memory Clock Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 29h
Default: 00h

D7	MCLK VCO Gain 0: Gain for low frequency operation 1: Gain for high frequency operation
D[6:5]	MCLK Post-Scale Bit[1:0] When SR13 D6=0 (refer to ".16" on page 88), 00: Do not scale 01: Scaled by 2 10: Scaled by 3 11: Scaled by 4 When SR13 D6=1 (refer to ".16" on page 88), 00: Reserved 01: Reserved 10: Scaled by 6 11: Scaled by 8

D[4:0] MCLK DeNumerator Bit[4:0]
[00000:11111] = [1:32]

NOTE: For the operation of internal memory clock generation, please refer to "7 Internal Dual-Clock Synthesizer" on Page 25.

.41 SR2A: Extended Internal Video Clock Register 0

Register Type: Read/Write
Read/Write Port: 3C5h,Index 2Ah
Default: 00h

D[7] Internal VCLK Divider
0: Do not divide
1: Divide by 2
D[6:0] Internal VCLK Numerator Bit[6:0]
[0000000:1111111] = [1:128]

NOTE: For the operation of internal video clock generation, please refer to "7 Internal Dual-Clock Synthesizer" on Page 25.

.42 SR2A-1: Extended 25MHz Video Clock Register 0

Register Type: Read/Write
Read/Write Port: 3C5h,Index 2Ah
Default: 00h

D[7] 25Mhz VCLK Divider
0: Do not divide
1: Divide by 2
D[6:0] 25Mhz VCLK Numerator Bit[6:0]
[0000000:1111111] = [1:128]

.43 SR2A-2: Extended 28MHz Video Clock Register 0

Register Type: Read/Write
Read/Write Port: 3C5h,Index 2Ah
Default: 00h

D[7] 28Mhz VCLK Divider
0: Do not divide
1: Divide by 2
D[6:0] 28Mhz VCLK Numerator Bit[6:0]
[0000000:1111111] = [1:128]

.44 SR2B: Extended Internal Video Clock Register 1

Register Type: Read/Write
Read/Write Port: 3C5h, Index 2Bh
Default: 00h

D7 Internal VCLK VCO Gain
0: Gain for low frequency operation
1: Gain for high frequency operation
D[6:5] Internal VCLK Post-Scale Bit[1:0]

When SR13 D7 = 0 (refer to ".16" on page 88),
00: Do not scale
01: Scaled by 2
10: Scaled by 3
11: Scaled by 4
When SR13 D7 = 1 (refer to ".16" on page 88),
00: Reserved
01: Reserved
10: Scaled by 6
11: Scaled by 8

D[4:0] Internal VCLK DeNumerator Bit[4:0]
[00000:11111] = [1:32]

NOTE: For the operation of internal video clock generation, please refer to "7 Internal Dual-Clock Synthesizer" on Page 25.

.45 SR2B-1: Extended 25MHz Video Clock Register 1

Register Type: Read/Write
Read/Write Port: 3C5h, Index 2Bh
Default: 00h

D7 25MHz VCLK VCO Gain
0: Gain for low frequency operation
1: Gain for high frequency operation

D[6:5] 25MHz VCLK Post-Scale Bit[1:0]
When SR13-1 D7 = 0 (refer to ".17" on page 88),
00: Do not scale
01: Scaled by 2
10: Scaled by 3
11: Scaled by 4
When SR13-1 D7 = 1 (refer to ".17" on page 88),
00: Reserved
01: Reserved
10: Scaled by 6
11: Scaled by 8

D[4:0] 25MHz VCLK DeNumerator Bit[4:0]
[00000:11111] = [1:32]

.46 SR2B-2: Extended 28MHz Video Clock Register 1

Register Type: Read/Write
Read/Write Port: 3C5h, Index 2Bh
Default: 00h

D7 28MHz VCLK VCO Gain
0: Gain for low frequency operation
1: Gain for high frequency operation

D[6:5] 28MHz VCLK Post-Scale Bit[1:0]
When SR13-2 D7 = 0 (refer to ".18" on page 88),
00: Do not scale

01: Scaled by 2
10: Scaled by 3
11: Scaled by 4
When SR13B D7 = 1 (refer to ".18" on page 88),
00: Reserved
01: Reserved
10: Scaled by 6
11: Scaled by 8

D[4:0] 28MHz VCLK DeNumerator Bit[4:0]
[00000:11111] = [1:32]

.47 SR2C: Extended Turbo Queue Base Address

Register Type: Read/Write
Read/Write Port: 3C5h, Index 2Ch
Default: 00h

D7 Reserved
D[6:0] Turbo Queue Base Address Bit[6:0]

.48 SR2D: Extended Memory Start Control Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 2Dh
Default: 00h

D[7:4] Reserved
D[3:0] Page Size Select
0000: 2 KB at 32-bit mode, 4 KB at 64-bit mode
0001: 4 KB at 32-bit mode, 8 KB at 64-bit mode
0010: 8 KB at 32-bit mode, 16 KB at 64-bit mode
0011: 16 KB at 32-bit mode, 32 KB at 64-bit mode
0100: 1 KB at 32-bit mode, 2 KB at 64-bit mode
Others: Reserved

.49 SR2E: Extended Reserved Register

Register Type: Read/Write
Read/Write Port: 3C5h, Index 2Eh
Default: 00h

D[7:0] Reserved

.50 SR2F: Extended DRAM Frame Buffer Size Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 2Fh
Default: 00h

D[7:6] Reserved
D5 Enable Fast Change Mode Timing
0: Disable
1: Enable

D4	Enable Fast Page Flip 0: Disable 1: Enable
D[3:0]	Reserved

.51 SR30: Extended Fast Page Flip Starting Address Low Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 30h
Default: 00h

D[7:0]	Fast page flip starting address bit[7:0]

.52 SR31: Extend Fast Page Flip Starting Address Middle Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 31h
Default: 00h

D[7:0]	Fast page flip start address bit[15:8]

.53 SR32: Extended Fast Page Flip Starting Address High Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 32h
Default: 00h

D[7:4]	Reserved
D[3:0]	Fast page flip start address bit[19:16]

Note: The fast page flip starting address is latched when SR32 is written. So the registers, SR30 and SR31, should be programmed before SR32. These registers are enabled by setting SR2F D4 (refer to ".50" on page 96).

.54 SR33: Extended Misc. Control Register 4

Register Type: Read/Write
Read/Write Port: 3C5, Index 33h
Default: 00h

D7	Reserved
D6	Select external TVCLK as MCLK enable 0: Disable 1: Enable
D5	Relocated VGA I/O port addresses decoding disable 0: Disable 1: Enable The standard VGA register I/O port address can be relocated to address defined by PCI Config Register 18H. This bit disable the relocated address decoding.
D4	Standard VGA I/O port addresses decoding enable 0: Enable 1: Disable The standard VGA register I/O port address decoding can be disabled by

this bit.

D3	Enable one cycle EDO DRAM timing 0: Disable 1: Enable
D2	Select SGRAM Latency 0: Latency = 3 1: Latency = 2
D1	Enable SGRAM Mode Write timing 0: Disable 1: Enable This bit must be set before accessing SGRAM. It must clear to 0 before setting to 1 to generate a new Mode Write cycle.
D0	Enable SGRAM timing 0: Disable 1: Enable

.55 SR34: Extended Misc. control Register 5

Register Type: Read/Write
Read/Write Port: 3C5, Index 34h
Default: 00h

D7	DRAM controller one cycle write enable 0: Disable 1: Enable
D6	DRAM controller one cycle read enable 0: Enable 1: Disable
D[5:3]	Reserved
D2	Enable DRAM output PAD low power consumption 0: Disable 1: Enable
D1	Reserved
D0	Enable Hardware Command Queue threshold low 0: Disable 1: Enable

.56 SR35: Extended Misc. Control Register 6

Register Type: Read/Write
Read/Write Port: 3C5, Index 35h
Default: 00h

D7	Enable Hardware MPEG 0: Disable 1: Enable
D6	MA delay compensation 0: Add 0ns 1: Add 2ns
D5	SGRAM burst timing enable

0: Enable
1: Disable

D4 Enable PCI burst write zero-wait
0: Disable
1: Enable

D[3:2] DRAM CAS LOW period width compensation bit[1:0]
00: Add 0ns
01: Add 2ns
10: Add 4ns
11: Add 6ns

D1 Enable PCI Bus Write Cycle Retry
0: Disable
1: Enable

D0 Enable PCI Bus Read Cycle Retry
0: Disable
1: Enable

.57 SR36: Extended Scratch Register 3

Register Type: Read/Write
Read/Write Port: 3C5, Index 36h
Default: 00h

D[7:0] Reserved for VGA BIOS

.58 SR37: Extended Scratch Register 4

Register Type: Read/Write
Read/Write Port: 3C5, Index 37h
Default: 00h

D[7:0] Reserved for VGA BIOS

.59 SR38: Extended Misc. Control Register 7

Register Type: Read/Write
Read/Write Port: 3C5, Index 38h
Default: 00h

D[7:4] Hardware Cursor Location
Hardware Cursor Starting Address Bit[21:18]

D3 Reserved

D2 Disable Line compare
0: Enable
1: Disable

D[1:0] Video Clock Register Selection Bit[1:0]
00 : Select Internal Video Clock Registers
SR13, SR2A, SR2B
01 : Select 25MHz Video Clock Registers
SR13, SR2A-1, SR2B-1
10 : Select 28MHz Video Clock Registers
SR13, SR2A-2, SR2B-2

11 : Reserved
There are three video clock registers Internal Video Clock Registers, 25Mhz Video Clock Registers, 28Mhz Video Clock Registers. All three registers use the same index of 3C5, index 13, 2A and 2B. The selection is programmed by Video Clock Register Selection Bit[1:0]. The VCLK frequency is generated from Internal Video Clock Registers when Miscellaneous Output Register (port 3C2) Bit[3:0]=11. The VCLK frequency is generated from 25Mhz Video Clock Registers when Miscellaneous Output Register (port 3C2) bit[3:0]=00. The VCLK frequency is generated from 28Mhz Video Clock Registers when Miscellaneous Output Register (port 3C2) bit[3:0]=01.

.60 SR39: Extended Misc. Control Register 8

Register Type: Read/Write
Read/Write Port: 3C5, Index 39h
Default: 00h

D[7:5]	Reserved
D4	Select external TVCLK as internal TVCLK enable 0: Disable 1: Enable
D3	Select external REFCLK as internal TVCLK enable 0: Disable 1: Enable
D2	Enable 3D Accelerator 0: Disable 1: Enable
D1	MPEG IDCT command software compression mode 0: Disable 1: Enable
D0	Enable MPEG II video decoding mode 0: Disable 1: Enable

.61 SR3A: Extended MPEG Turbo Queue Base Address

Register Type: Read/Write
Read/Write Port: 3C5h, Index 3Ah
Default: 00h

D7	Reserved
D[6:0]	MPEG Turbo Queue Base Address Bit[6:0]

.62 SR3B: Extended Clock Generator Control Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 3Bh
Default: 00h

D[7:4]	Video clock generator control bit[3:0]
D[3:0]	Memory clock generator control bit[3:0]

.63 SR3C: Extended Misc. Control Register 9

Register Type: Read/Write
Read/Write Port: 3C5, Index 3Ch
Default: 00h

D7	Reserved
D6	SCLK output enable 0: Enable 1: Disable
D5	AGP request high priority enable 0: Select low priority 1: Select high priority
D4	Enable Oscillator I/O PAD Power Down 0: Enable 1: Disable
D3	Enable AGP Dynamic Power Saving 0: Disable 1: Enable
D2	PCI-66 MHz timing enable 0: Disable 1: Enable
D[1:0]	Turbo Queue length 2D/3D configuration bit[1:0] 00: 2D = 32KB, 3D = 0KB. 01: 2D = 16KB, 3D = 16KB. 10: 2D = 8KB, 3D = 24KB. 11: 2D = 4KB, 3D = 28KB.

8 2D Graphics Engine Registers

SiS6326 integrated graphics controller supports a powerful graphics engine to enhance the performance. The functions of the graphics engine in SiS6326 include BitBlt, BitBlt with mask, Color/Font Expansion, Enhanced Color/Font Expansion, Line Drawing, and Direct Draw.

Since the register formats for the line drawing and Direct Draw are different from those of the other general engine functions, we would like to describe these three register formats separately in the following paragraphs:

.1 Register Format for General Engine Functions
.2 Register Format for Line Drawing (starts from page 108)
.3 Register Format for Direct Draw (starts from page 112)

.1 Register Format for General Engine Functions

The following table shows the register format for the general Graphics Engine functions.

D[31:24]	D[23:16]	D[15:08]	D[07:00]	I/O Address
Reserved	SRC Start Linear Address [21:0]			8280h
Selection bits	DST Start Linear Address [21:0]			8284h
DST Pitch		SRC Pitch		8288h
Rectangular Height		Rectangular Width		828Ch
FG ROP	FG (Foreground) Color			8290h
BG ROP	BG (Background) Color			8294h
Mask3	Mask2	Mask1	Mask0	8298h
Mask7	Mask6	Mask5	Mask4	829Ch
Top Clipping		Left Clipping		82A0h
Bottom Clipping		Right Clipping		82A4h
Command 1	Command 0	Command Queue Status		82A8h
Pattern 3	Pattern 2	Pattern 1	Pattern 0	82ACh
Pattern 7	Pattern 6	Pattern 5	Pattern 4	82B0h
Pattern 11	Pattern 10	Pattern 9	Pattern 8	82B4h
Pattern 15	Pattern 14	Pattern 13	Pattern 12	82B8h
Pattern 19	Pattern 18	Pattern 17	Pattern 16	82BCh
Pattern 23	Pattern 22	Pattern 21	Pattern 20	82C0h
Pattern 27	Pattern 26	Pattern 25	Pattern 24	82C4h
Pattern 31	Pattern 30	Pattern 29	Pattern 28	82C8h
Pattern 35	Pattern 34	Pattern 33	Pattern 32	82CCh
Pattern 39	Pattern 38	Pattern 37	Pattern 36	82D0h
Pattern 43	Pattern 42	Pattern 41	Pattern 40	82D4h
Pattern 47	Pattern 46	Pattern 45	Pattern 44	82D8h
Pattern 51	Pattern 50	Pattern 49	Pattern 48	82DCh
Pattern 55	Pattern 54	Pattern 53	Pattern 52	82E0h
Pattern 59	Pattern 58	Pattern 57	Pattern 56	82E4h
Pattern 63	Pattern 62	Pattern 61	Pattern 60	82E8h

Pattern 67	Pattern 66	Pattern 65	Pattern 64	82ECh
Pattern 71	Pattern 70	Pattern 69	Pattern 68	82F0h
Pattern 75	Pattern 74	Pattern 73	Pattern 72	82F4h
Pattern 79	Pattern 78	Pattern 77	Pattern 76	82F8h
Pattern 83	Pattern 82	Pattern 81	Pattern 80	82FCh
Pattern 87	Pattern 86	Pattern 85	Pattern 84	8300h
Pattern 91	Pattern 90	Pattern 89	Pattern 88	8304h
Pattern 95	Pattern 94	Pattern 93	Pattern 92	8308h
Pattern 99	Pattern 98	Pattern 97	Pattern 96	830Ch
Pattern 103	Pattern 102	Pattern 101	Pattern 100	8310h
Pattern 107	Pattern 106	Pattern 105	Pattern 104	8314h
Pattern 111	Pattern 110	Pattern 109	Pattern 108	8318h
Pattern 115	Pattern 114	Pattern 113	Pattern 112	831Ch
Pattern 119	Pattern 118	Pattern 117	Pattern 116	8320h
Pattern 123	Pattern 122	Pattern 121	Pattern 120	8324h
Pattern 127	Pattern 126	Pattern 125	Pattern 124	8328h

Source Start Linear Address

Register Type: Read/Write
Read/Write Port: 8280h~8283h
Default: 00h

D[31:22] Reserved
D[21:0] Source Start Linear Address Bit[21:0]

Destination Start Linear Address

Register Type: Read/Write
Read/Write Port: 8284h~8287h
Default: 00h

D31 Enhanced Color Expansion Busy Bit
0: Idle
1: Busy
This bit is read only
D[30:27] Reserved
D26 Enable No.64~127 pattern registers for color-expansion function.
0: Disable
1: Enable
D25 Enable No.64~127 pattern registers for pattern-copy function in high color mode.
0: Disable
1: Enable
D24 Select pattern registers for pattern-copy function in 256 color mode.
0: Select No.0~63 pattern registers
1: Select No.64~127 pattern registers
D[21:0] Destination Start Linear Address Bit[21:0]

Source Pitch

Register Type: Read/Write
Read/Write Port: 8288h~8289h
Default: 00h

D[15:12] Reserved
D[11:0] Source Pitch Bit[11:0]

Destination Pitch

Register Type: Read/Write
Read/Write Port: 828Ah~828Bh
Default: 00h

D[15:12] Reserved
D[11:0] Destination Pitch Bit[11:0]

Rectangular Width

Register Type: Read/Write
Read/Write Port: 828Ch~828Dh
Default: 00h

D[15:12] Reserved
D[11:0] Destination Rectangular Width Bit[11:0]

Rectangular Height

Register Type: Read/Write
Read/Write Port: 828Eh~828Fh
Default: 00h

D[15:12] Reserved
D[11:0] Destination Rectangular Height Bit[11:0]

Foreground Color

Register Type: Read/Write
Read/Write Port: 8290h~8292h
Default: 00h

D[23:0] Foreground Color Bit[23:0]

FG Rop

Register Type: Read/Write
Read/Write Port: 8293h
Default: 00h

D[7:0] Foreground Raster Operation Bit[7:0]

Background Color

Register Type: Read/Write
Read/Write Port: 8294h~8296h
Default: 00h

D[23:0] Background Color Bit[23:0]

BG Rop

Register Type: Read/Write

Read/Write Port: 8297h
Default: 00h

D[7:0] Background Raster Operation Bit[7:0]

Mono Mask Register

Register Type: Read/Write
Read/Write Port: 8298h~829Fh
Default: 00h

D[63:0] Mono Mask Bit[63:0]

Left Clipping

Register Type: Read/Write
Read/Write Port: 82A0h~82A1h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Left Bit[11:0]

Top Clipping

Register Type: Read/Write
Read/Write Port: 82A2h~82A3h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Top Bit[11:0]

Right Clipping

Register Type: Read/Write
Read/Write Port: 82A4h~82A5h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Right Bit[11:0]

Bottom Clipping

Register Type: Read/Write
Read/Write Port: 82A6h~82A7h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Bottom Bit[11:0]

Command Queue Status

Register Type: Read
Read/Write Port: 82A8h~82A9h
Default: 00h

If Hardware Command Queue is enable, then
D[15:5] reserved
D[4:0] Available Command Queue Length Bit[4:0]

If Turbo Queue is enable, then

D[15:0] Head/Tail Index Bit[15:0]
The Head Index is written into this register, and the Tail Index is read from this registers.

Command Register 0

Register Type: Read/Write
Read/Write Port: 82AAh
Default: 00h

D7 Rectangular clipping mode
0: Clipping internal region
1: Clipping external region

D6 Rectangular Clipping Control
0: Disable rectangular clipping logic
1: Enable rectangular clipping logic

D5 Y direction control
0: Y counter decrease
1: Y counter increase

D4 X direction control
0: X counter decrease
1: X counter increase

D[3:2] Pattern select bit 1-0
00: From background color registers
01: From foreground color registers
10: From pattern registers
11: Reserved

D[1:0] Source select bit 1-0
00: From background color registers
01: From foreground color registers
10: From video memory
11: From CPU-driven BitBlt source data

Command Register 1

Register Type: Read/Write
Read/Write Port: 82ABh
Default: 00h

D7 Hardware Command Queue status
0: Hardware Command queue is not empty
1: Hardware Command queue is empty

D6 Graphics engine status
0: Graphics engine is idle and Hardware command queue is empty
1: Graphics engine is busy or Hardware command queue is not empty

D5 Enhanced Color Expansion
0: Disable enhanced color expansion
1: Enable enhanced color expansion

D4 Enhanced Font Expansion
0: Disable enhanced font expansion
1: Enable enhanced font expansion

D3	Line drawing last pixel control 0: Last pixel will be drawn 1: Last pixel will not be drawn
D2	Line drawing major axial selection 0: Y-axial is major 1: X-axial is major
D[1:0]	Command type select Bit[1:0] 00: BitBlt 01: BitBlt with mask 10: Color/Font expansion 11: Line drawing

NOTE: Word-Writing to Command 1 and Command 0, it will automatically initiate graphics engine to execute the specified command.

Pattern Register n

Register Type:	Read/Write
Read/Write Port:	82ACh-82EBh
Default:	00h

D[7:0]	For 256 color mode with BitBlt engine, these registers store the 8x8 color bitmap. For Color-Expansion, these registers store the monochrome bitmap, thus it can expand 512 pixels at a time.

.2 Register Format for Line Drawing

The register format for Line-Drawing is shown in following table.

D[31:24]	D[23:16]	D[15:08]	D[07:00]	IO Address
Reserved		X Start		8280h
Reserved		Y Start		8284h
Reserved		Reserved		8288h
Reserved		Major Axial Pixel Count		828Ch
FG ROP	FG (Foreground) Color			8290h
BG ROP	BG (Background) Color			8294h
K2 Term		K1 Term		8298h
Line Style		Error Term		829Ch
Top Clipping		Left Clipping		82A0h
Bottom Clipping		Right Clipping		82A4h
Command/Status		Reserved	Status 0	82A8h

X Start

Register Type: Read/Write
Read/Write Port: 8280h~8281h
Default: 00h

D[15:12] Reserved
D[11:0] X Start Bit[11:0]

Y Start

Register Type: Read/Write
Read/Write Port: 8284h~8285h
Default: 00h

D[15:12] Reserved
D[11:0] Y Start Bit[11:0]

Major Axial Pixel Count

Register Type: Read/Write
Read/Write Port: 828Ch~828Dh
Default: 00h

D[15:12] Reserved
D[11:0] Major Axial Pixel Count Bit[11:0]

Foreground Color

Register Type: Read/Write
Read/Write Port: 8290h~8292h
Default: 00h

D[23:0] Foreground Color Bit[23:0]

FG ROP

Register Type: Read/Write

Read/Write Port: 8293h
Default: 00h

D[7:0] Foreground Raster Operation Bit[7:0]

Background Color

Register Type: Read/Write
Read/Write Port: 8294h~8296h
Default: 00h

D[23:0] Background Color Bit[23:0]

BG ROP

Register Type: Read/Write
Read/Write Port: 8297h
Default: 00h

D[7:0] Background Raster Operation Bit[7:0]

K1 Term

Register Type: Read/Write
Read/Write Port: 8298h~8299h
Default: 00h

D[15:14] Reserved
D[13:0] K1 Term Bit[13:0]

K2 Term

Register Type: Read/Write
Read/Write Port: 829Ah~829Bh
Default: 00h

D15:14] Reserved
D[13:0] K2 Term Bit[13:0]

Error Term

Register Type: Read/Write
Read/Write Port: 829Ch~829Dh
Default: 00h

D[15:14] Reserved
D[13:0] Error Term Bit[13:0]

Line Style

Register Type: Read/Write
Read/Write Port: 829Eh~829Fh
Default: 00h

D[15:0] Style Pattern Bit[15:0]

Left Clipping

Register Type: Read/Write
Read/Write Port: 82A0h~82A1h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Left Bit[11:0]

Top Clipping

Register Type: Read/Write
Read/Write Port: 82A2h~82A3h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Top Bit[11:0]

Right Clipping

Register Type: Read/Write
Read/Write Port: 82A4h~82A5h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Right Bit[11:0]

Bottom Clipping

Register Type: Read/Write
Read/Write Port: 82A6h~82A7h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Bottom Bit[11:0]

Command Queue Status

Register Type: Read/Write
Read/Write Port: 82A8h~82A9h
Default: 00h

If Hardware Command Queue is enable, then
D[15:5] reserved
D[4:0] Available Command Queue Length Bit[4:0]

If Turbo Queue is enable, then
D[15:0] Head/Tail Index Bit[15:0]
The Head Index is written into this register and the Tail Index is read from this registers.

Command Register 0

Register Type: Read/Write
Read/Write Port: 82AAh
Default: 00h

D7 Rectangular Clipping Mode
0: Clipping internal region
1: Clipping external region
D6 Rectangular Clipping Control
0: Disable rectangular clipping logic
1: Enable rectangular clipping logic
D5 Y direction control

0: Y counter decrease
1: Y counter increase

D4 X direction control
0: X counter decrease
1: X counter increase

D[3:2] Pattern select bit[1:0]
00: From background color registers
01: From foreground color registers
10: From pattern registers
11: Reserved

D[1:0] Source select bit[1:0]
00: From background color registers
01: From foreground color registers
10: From video memory
11: From CPU-driven BitBlt source data

Command Register 1

Register Type: Read/Write
Read/Write Port: 82ABh
Default: 00h

D7 Hardware Command Queue status
0: Hardware Command queue is not empty
1: Hardware Command queue is empty

D6 Graphics engine status
0: Graphics engine is idle and Hardware command queue is empty
1: Graphics engine is busy or Hardware command queue is not empty

D5 Enhanced Color Expansion
0: Disable enhanced color expansion
1: Enable enhanced color expansion

D4 Enhanced Font Expansion
0: Disable enhanced font expansion
1: Enable enhanced font expansion

D3 Line drawing last pixel control
0: Last pixel will be drawn
1: Last pixel will not be drawn

D2 Line drawing major axial selection
0: Y-axial is major
1: X-axial is major

D[1:0] Command type select bit[1:0]
00: Bitblt
01: BitBlt with mask
10: Color/Font expansion
11: Line drawing

NOTE: Word-writing to Command 1 and Command 0, it will automatically initiate graphics engine to execute the specified command.

.3 Register Format for Direct Draw

The register format for Direct Draw is shown in following table.

D[31:24]	D[23:16]	D[15:08]	D[07:00]	IO Address
Reserved	Source Start Linear Address			8280h
Reserved	Destination Start Linear Address			8284h
Destination Pitch		Source Pitch		8288h
Rectangular Height		Rectangular Width		828Ch
S_Alpha Bit	High Value of Source Color Key			8290h
D_Alpha Bit	High value of Destination Color Key			8294h
D_Rop	Low Value of Source Color Key			8298h
Reserved	Low Value of Destination Color Key			829Ch
Top Clipping		Left Clipping		82A0h
Bottom Clipping		Right Clipping		82A4h
Command/Status		Command Queue Status		82A8h

Source Start Linear Address

Register Type: Read/Write
Read/Write Port: 8280h~8283h
Default: 00h

D[31:22] Reserved
D[21:0] Source Start Linear Address Bit[21:0]

Destination Start Linear Address

Register Type: Read/Write
Read/Write Port: 8284h~8287h
Default: 00h

D[31:22] Reserved
D[21:0] Destination Start Linear Address Bit[21:0]

Source Pitch

Register Type: Read/Write
Read/Write Port: 8288h~8289h
Default: 00h

D[15:12] Reserved
D[11:0] Source Pitch Bit[11:0]

Destination Pitch

Register Type: Read/Write
Read/Write Port: 828Ah~828Bh
Default: 00h

D[15:12] Reserved
D[11:0] Destination Pitch Bit[11:0]

Rectangular Width

Register Type: Read/Write
Read/Write Port: 828Ch~828Dh
Default: 00h

D[15:12]	Reserved
D[11:0]	Destination Rectangular Width Bit[11:0]

Rectangular Height

Register Type: Read/Write
Read/Write Port: 828Eh~828Fh
Default: 00h

D[15:12]	Reserved
D[11:0]	Destination Rectangular Height Bit[11:0]

High value of Source Color Key

Register Type: Read/Write
Read/Write Port: 8290h~8292h
Default: 00h

D[23:0]	High Value of Source Color Key Bit[23:0]

Alpha Blending Control Bit for Source Color (S_Alpha Bit)

Register Type: Read/Write
Read/Write Port: 8293h
Default: 00h

D[7:1]	Reserved
D0	Control Bit for Source Color Alpha Blending

High Value of Destination Color Key (D_Alpha Bit)

Register Type: Read/Write
Read/Write Port: 8294h~8296h
Default: 00h

D[23:0]	High Value of Destination Color Key Bit[23:0]

Alpha Blending Control Bit for Destination Color (D_Alpha Bit)

Register Type: Read/Write
Read/Write Port: 8297h
Default: 00h

D[7:1]	Reserved
D0	Control Bit for Destination Color Alpha Blending

Low Value of Source Color Key

Register Type: Read/Write
Read/Write Port: 8298h~829Ah
Default: 00h

D[23:0]	Low Value of Source Color Key Bit[23:0]

Direct Draw Rop (D_Rop)

Register Type: Read/Write

Read/Write Port: 829Bh
Default: 00h

D[7:4] Reserved
D[3:0] Direct Draw Raster Operation Bit[3:0]

Low Value of Destination Color Key

Register Type: Read/Write
Read/Write Port: 829Ch~829Fh
Default: 00h

D[23:0] Low Value of Destination Color Key Bit[23:0]

Left Clipping

Register Type: Read/Write
Read/Write Port: 82A0h~82A1h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Left Bit[11:0]

Top Clipping

Register Type: Read/Write
Read/Write Port: 82A2h~82A3h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Top Bit[11:0]

Right Clipping

Register Type: Read/Write
Read/Write Port: 82A4h~82A5h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Right Bit[11:0]

Bottom Clipping

Register Type: Read/Write
Read/Write Port: 82A6h~82A7h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Bottom Bit[11:0]

Command Queue Status

Register Type: Read/Write
Read/Write Port: 82A8h~82A9h
Default: 00h

If Hardware Command Queue is enable, then
D[15:5] reserved
D[4:0] Available Command Queue Length Bit[4:0]

If Turbo Queue is enable, then

D[15:0] Head/Tail Index Bit[15:0]
The Head Index is written into this register and the Tail Index is read from this registers.

Command Register 0

Register Type: Read/Write
Read/Write Port: 82AAh
Default: 00h

D7 Rectangular Clipping Mode
0: Clipping internal region
1: Clipping external region

D6 Rectangular Clipping Control
0: Disable rectangular clipping logic
1: Enable rectangular clipping logic

D5 Y direction control
0: Y counter decrease
1: Y counter increase

D4 X direction control
0: X counter decrease
1: X counter increase

D[3:2] Direct Draw Enable
00: Reserved
01: Reserved
10: Reserved
11: Enable Direct Draw
The two bits (D[3:2]) must be set to "11" then the Direct Draw function can be enabled.

D[1:0] Source select bit[1:0]
00: From background color registers
01: From foreground color registers
10: From video memory
11: From CPU-driven BitBlt Source Data

Command Register 1

Register Type: Read/Write
Read/Write Port: 82ABh
Default: 00h

D7 Hardware Command Queue status
0: Hardware Command queue is not empty
1: Hardware Command queue is empty

D6 Graphics engine status
0: Graphics engine is idle and Hardware command queue is empty
1: Graphics engine is busy or Hardware command queue is not empty

D5 Enhanced Color Expansion
0: Disable enhanced color expansion
1: Enable enhanced color expansion

D4	Enhanced Font Expansion 0: Disable enhanced font expansion 1: Enable enhanced font expansion
D3	Line drawing last pixel control 0: Last pixel will be drawn 1: Last pixel will not be drawn
D2	Line drawing major axial selection 0: Y-axial is major 1: X-axial is major
D[1:0]	Command type select bit[1:0] 00: Bitblt 01: BitBlt with mask 10: Color/Font expansion 11: Line drawing

NOTE: Word-writing to Command 1 and Command 0, it will automatically initiate graphics engine to execute the specified command.

9 Video Accelerator Registers

Index(3D4)	Video Accelerator Register (3D5)
80h	Password/Identification Register
81h	Video Window Horizontal Display Start Low Register
82h	Video Window Horizontal Display End Low Register
83h	Video Window Horizontal Display Overflow Register
84h	Video Window Vertical Display Start Low Register
85h	Video Window Vertical Display End Low Register
86h	Video Window Vertical Display Overflow Register
87h	Video Capture Frame Buffer Starting Address Low Register
88h	Video Capture Frame Buffer Starting Address Middle Register
89h	Video Frame Buffer Overflow Register
8Ah	Video Display Frame Buffer Starting Address Low Register
8Bh	Video Display Frame Buffer Starting Address Middle Register
8Ch	Video Frame Buffer Offset Low Register
8Dh	Video Display Frame Buffer End Address Low Register
8Eh	Video Frame Buffer Offset Address High Register
8Fh	Video Capture Threshold Value Register
90h	Video Capture Horizontal Down Scaling Factor Register
91h	Video Capture Vertical Down Scaling Register
92h	Horizontal Up Scaling Factor and Horizontal Interpolation Accuracy Factor Register
93h	Vertical Up Scaling Factor Register
94h	Horizontal Scaling Factor Integer Register
95h	Video Overlay Color Key Blue Low Value Register
96h	Video Overlay Color Key Green Low Value Register
97h	Video Overlay Color Key Red Low Value Register
98h	Video Control Misc. Register 0
99h	Video Control Misc. Register 1
9Ah	Video Chroma Key B/Y Low Value Register
9Bh	Video Chroma Key G/U Low Value Register
9Ch	Video Chroma Key R/V Low Value Register
9Dh	Video Control Misc. Register 3
9Eh	Video Playback Threshold Low Value Register
9Fh	Video Playback Threshold High Value Register
A0h	Line Buffer Size Register
A1h	Video Overlay Color Key Blue High Value Register
A2h	Video Overlay Color Key Green High Value Register
A3h	Video Overlay Color Key Red High Value Register
A4h	Video Chroma Key B/Y High Value Register
A5h	Video Chroma Key G/U High Value Register
A6h	Video Chroma Key R/V High Value Register
A7h	Graphics Data Alpha Value Register

A8h	Video Data Alpha Value Register
A9h	Key Overlay Operation Mode Register
AAh	Video Capture Horizontal Start Register
ABh	Video Capture Horizontal End Register
ACh	Video Capture Vertical Start Register
ADh	Video Capture Vertical End Register
AEh	Video Capture Horizontal Overflow Register
AFh	Video Capture Vertical Overflow Register
B0h	System Memory Video Frame Buffer Setting Register 1
B1h	System Memory Video Frame Buffer Setting Register 2
B2h	System Memory Video Frame Buffer Setting Register 3 and Video Control Register
B3h	Contrast Enhancement Mean Value Sampling Rate Factor Register
B4h	Brightness Register
B5h	Contrast Enhancement Control Register
B6h	Video Misc. Control Register
B7h	Video U Plane Starting Address Low Register
B8h	Video U Plane Starting Address Middle Register
B9h	Video UV Plane Starting Address High Register
BAh	Video V Plane Starting Address Low Register
BBh	Video V Plane Starting Address Middle Register
BCh	Video UV Plane Offset Register
BDh	Video UV Plane Offset High Register
E0h	Index Register of TV OUT Registers
E1h	Data Register of TV OUT Registers

.1 Password/Identification Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 80h
Default: 00h

D[7:0] Password/identification Bit[7:0]

Description:
If 86h is written to this register, A1h will be read from this register and all the video extension registers would be unlocked to allow desired change.
If any value other than 86h is written to this register, 21h will be read from this register and all the video extension registers would be locked to prevent unauthorized change.

.2 Video Window Horizontal Display Start Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 81h
Default: 00h

D[7:0] Video window horizontal display start Bit[7:0]

Description:

The Video Window Horizontal Display Start Bit[10:0] form the left boundary of the video window. The Bit[10:8] is located in the Video Window Horizontal Display Overflow Register (Index 83h, ".4" on page 119). The boundary is in unit of pixel.

.3 Video Window Horizontal Display End Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 82h
Default: 00h

D[7:0]	Video window horizontal display end Bit[7:0]

Description:
The Video Window Horizontal Display End Bit[10:0] form the right boundary of the video window. The Bits[10:8] is located in the Video Window Horizontal Display Overflow Register (Index 83h, ".4" on page 119). The boundary is in unit of pixel.

.4 Video Window Horizontal Display Overflow Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 83h
Default: 00h

D[2:0]	Video window horizontal display start Bit[10:8]
D3	Reserved
D[6:4]	Video window horizontal display end Bit[10:8]
D7	Reserved

.5 Video Window Vertical Display Start Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 84h
Default: 00h

D[7:0]	Video window vertical display start Bit[7:0]

Description:
The Video Window Vertical Display Start Bit[10:0] form the top boundary of the video window. The Bit[10:8] is located in the Video Window Vertical Display Overflow Register (Index 86h, ".7" on page 119). The boundary is in unit of line.

.6 Video Window Vertical Display End Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 85h
Default: 00h

D[7:0]	Video window vertical display end Bit[7:0]

Description:
The Video Window Vertical Display End Bit[10:0] form the bottom boundary of the video window. The Bit[10:8] is located in the Video Window Vertical Display Overflow Register (Index 86h, ".7" on page 119). The boundary is in unit of line.

.7 Video Window Vertical Display Overflow Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 86h
Default: 00h

D[2:0]	Video window horizontal display start Bit[10:8]
D3	Reserved
D[6:4]	Video window horizontal display end Bit[10:8]
D7	Reserved

.8 Video Capture Frame Buffer Starting Address Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 87h
Default: 00h

D[7:0]	Video capture frame buffer starting address Bit[7:0]

Description:
The Video Capture Frame Buffer Starting Address Bit[19:0] form the video frame buffer starting address in unit of double-word. The Bit[15:8] are located in the Video Capture Frame Buffer Starting Address Middle Register (Index 88h, ".9" on page 120). The Bit[19:16] are located in the Video Frame Buffer Overflow Register (Index 89h, ".10" on page 120).

.9 Video Capture Frame Buffer Starting Address Middle Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 88h
Default: 00h

D[7:0]	Video capture frame buffer starting address Bit[15:8]

.10 Video Frame Buffer Overflow Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 89h
Default: 00h

D[3:0]	Video capture frame buffer starting address Bit[19:16]
D[7:4]	Video display frame buffer starting address Bit[19:16]

.11 Video Display Frame Buffer Starting Address Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 8Ah
Default: 00h

D[7:0]	Video display frame buffer starting address Bit[7:0]

Description:
The Video Display Frame Buffer Starting Address Bit[19:0] form the video display starting address in unit of double-word. The Bit[15:8] are located in the Video Display Frame Buffer Starting Address Middle Register (Index 8Bh, ".12" on page 121). The Bits[19:16] are located in the Video Frame Buffer Overflow Register (Index 89h, ".10" on page 120).
This address could be different from the video capture frame buffer starting address to perform the video display panning function.

.12 Video Display Frame Buffer Starting Address Middle Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 8Bh
Default: 00h

D[7:0]	Video display frame buffer starting address Bit[15:8]

.13 Video Frame Buffer Offset Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 8Ch
Default: 00h

D[7:0]	Video frame buffer offset Bit[7:0]

Description:
The Video Frame Buffer Offset Bit[11:0] form the offset of the video frame buffer. The Bit[11:8] are located in the Video Frame Buffer Offset High Register (Index 8Eh, ".15" 121). The offset defines the size of the scan line of the video data captured in the video frame buffer in unit of double word. It should slightly larger than the actual size of captured video image to avoid the data over stored to next scan line buffer.

.14 Video Display Frame Buffer End Address Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 8Dh
Default: 00h

D[7:0]	Video display frame buffer end address Bit[7:0]

Description:
The Video Capture Frame Buffer End Address Bit[7:0] form the end address of the video frame buffer. The address is in unit of 16k bytes. This address defines the end address of the capture frame buffer. It can prevent the captured data to destroy the other data outside the capture frame buffer when the video data input is unstable.

.15 Video Frame Buffer Offset Address High Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 8Eh
Default: 00h

D[3:0]	Video frame buffer offset Bit[11:8]
D[7:4]	Reserved

.16 Video Capture Threshold Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 8Fh
Default: 00h

D[2:0]	Video capture threshold low Bit[2:0]
D3	Reserved
D[6:4]	Video capture threshold high Bit[2:0]
D7	Reserved

Description:
This register contains the video capture FIFO threshold low and the video capture FIFO threshold high.
The threshold low defines the FIFO lower boundary which indicates the FIFO is full enough and the data in the FIFO can be written into the DRAM. But if the priority of the threshold low is lower than others, it can wait until it is able to write the data of FIFO into the DRAM.
The threshold high defines the FIFO upper boundary which indicates the FIFO is about to be overflow and the data of the FIFO must be written into the DRAM as soon as possible.
These two thresholds should be modified to catch the maximum performance by compromising with the CRT threshold, video display threshold, and DRAM refresh rate, etc.

.17 Video Capture Horizontal Down Scaling Factor Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 90h
Default: 00h

D[5:0]	Video capture horizontal down scaling factor Bit[5:0]
D[7:6]	Reserved

Description:
This register contains the video capture horizontal down scaling factor (HDSF). The horizontal size of the captured video frame will be scaled to (64-HDSF)/64. Since the scaled-down video frame maybe will not fit into the video display window, the margins outside the video display window will be cut off. This factor is not only used to fit the window size but also is used to reduce the bandwidth required for the video capture and video display.

.18 Video Capture Vertical Down Scaling Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 91h
Default: 00h

D[5:0]	Vertical down scaling factor Bit[5:0]
D[7:6]	Reserved

Description:
This register contains the video capture vertical down scaling factor (VDSF). The vertical size of the captured video frame will be scaled to (64-VDSF)/64. Since the scaled-down video frame maybe will not fit into the video display window, the margins outside the video display window will be cut off. This factor is not only used to fit the window size but also is used to reduce the bandwidth required for the video capture and video display.

.19 Horizontal Up Scaling Factor and Horizontal Interpolation Accuracy Factor Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 92h
Default: 00h

D[5:0]	Horizontal up scaling factor Bit[5:0]
D[7:6]	Horizontal up-scaling interpolation accuracy factor 00: replication 01: 2-phase

10: 4-phase
11: 8-phase

Description:
This field contains the video playback horizontal up scaling factor fraction (HSFF). It is combined with the horizontal scaling factor integer (HSFI) register (Index 94h, ".21" on page 123) to form horizontal scaling. The horizontal size will be scaled to 1/(HSFI+(HSFF/64)). The HSFI should be zero for up-scaling. The HSFI should not be zero for down-scaling.
The Up-scaling interpolation accuracy factor can modify the up-scaling interpolation DDA accuracy phases.

.20 Vertical Up Scaling Factor Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 93h
Default: 00h

D[5:0] Vertical up scaling factor Bit[5:0]
D[7:6] Video frame buffer data format selection Bit[1:0]

for YUV format,
00: UYVY 4:2:2
01: VYUY 4:2:2
10: YUYV 4:2:2
11: YVYU 4:2:2

for RGB format,
00: RGB 5:5:5
01: RGB 5:6:5

Description:
This field contains the video playback vertical up scaling factor (VUSF). The vertical size will be scaled to 64/VUSF. If VUSF=0, the vertical size will not be scaled.

.21 Horizontal Scaling Factor Integer Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 94h
Default: 00h

D[3:0] Horizontal Scaling Factor Integer Bit[3:0]
D[7:4] Reserved

.22 Video Overlay Color Key Blue Low Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 95h
Default: 00h

D[7:0] Blue Key Bit[7:0]

Description:
This register contains the blue video overlay color key low value.
In 8-bit color mode, it is used as the color key low value.
In 16-bit color mode, it is used as the low byte of color key low value.

In 24-bit color mode, it is used as the blue byte of the color key low value.
If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

.23 Video Overlay Color Green Low Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 96h
Default: 00h

D[7:0]	Green Key Bit[7:0]

Description:
This register contains the green video overlay color key low value.
In 8-bit color mode, it is invalid.
In 16-bit color mode, it is used as the high byte of color key low value.
In 24-bit color mode, it is used as the green byte of the color key low value.
If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

.24 Video Overlay Color Red Low Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 97h
Default: 00h

D[7:0]	Red Key Bit[7:0]

Description:
This register contains the red video overlay color key low value.
In 8-bit color mode, it is invalid.
In 16-bit color mode, it is invalid.
In 24-bit color mode, it is used as the red byte of the color key low value.
If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

.25 Video Control Misc. Register 0

Register Type: Read/Write
Read/Write Port: 3D5, Index 98h
Default: 00h

D0	Enable video capture 0: Disable video capture 1: Enable video capture This bit could enable the video capture. If the video data is input through feature connector (FC), this bit should be set. The video pause function can be performed by disable this bit but enable the video playback bit.
D1	Enable video playback 0: Disable video playback

1: Enable video playback
This bit could enable the video playback. When the data of the video frame buffer are fetched by the system, the bandwidth of DRAM maybe not enough. The video playback can be disabled to gain the bandwidth but the video will not be played back.

D2 Reserved

D3 Reserved

D4 Video only display mode
0: Disable video only display mode
1: Enable video only display mode
The graphics display can be disable by setting this bit. This can reduce the DRAM bandwidth especially on the full screen video playback mode.

D5 Video capture interlace control
0: Disable video capture interlace control
1: Enable video capture interlace control
The video data input through feature connector could be interlaced. If the input video data are interlaced this bit should be set.

D6 Video format selection
0: Select RGB format
1: Select YUV format
This bit is used with the video frame buffer data format selection field of register CR92 to select the correct video data format.

D7 Field Polarity Selection
0: Select Odd/*Even
1: Select *Odd/Even
This bit can select the polarity of Field signal.

.26 Video Control Misc. Register 1

Register Type: Read/Write
Read/Write Port: 3D5, Index 99h
Default: 00h

D0 Enable YUV data capture
0: Capture RGB format video data
1: Capture YUV format video data
The video capture can be RGB and YUV format.

D1 Enable dithering
0: Disable dithering
1: Enable dithering
The captured video data can be dithered for better video quality.

D2 Capture format select
0: Format RGB 565
1: Format RGB 555
The capture video data may be RGB 555 or RGB565 format.

D[5:3] Horizontal filter select
000: 1
001: $(1/8(1+3z^{-1}+3z^{-2}+z^{-3}))$

010: $(1/4(1+2z^{-1}+z^{-2}))$
011: $(1/2(1+z^{-1}))$
100: $(1/8(1+2z^{-1}+2z^{-2}+2z^{-3}+z^{-4}))$
others: Reserved

D6 Enable vertical sync. interrupt
0: Disable
1: Enable
The video input vertical sync. signal could cause interrupt when this bit is enabled.

D7 Clear vertical sync. interrupt
0: Disable
1: Enable
After the vertical sync. caused an interrupt, this bit should be set for clear the interrupt request.

.27 Video Chroma Key B/Y Low Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 9Ah
Default: 00h

D[7:0] Video Chroma B/Y Key Low Bit[7:0]

Description:
This register contains the blue or Y video overlay chroma key low value.
In RGB chroma key mode, it is used as the blue byte of the chroma key low value.
In YUV chroma key mode, it is used as the Y of the chroma key low value.
If the value of the video data is greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced graphics data in the way defined by key operation mode.

.28 Video Chroma Key G/U Low Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 9Bh
Default: 00h

D[7:0] Video Chroma G/U Key Low Bit[7:0]

Description:
This register contains the green or U video overlay chroma key low value.
In RGB chroma key mode, it is used as the green byte of the chroma key low value.
In YUV chroma key mode, it is used as the U of the chroma key low value.
If the value of the video data is greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced graphics data in the way defined by key operation mode.

.29 Video Chroma Key R/V Low Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 9Ch
Default: 00h

D[7:0] Video Chroma R/V Key Low Value Bit[7:0]

Description:
This register contains the red or V video overlay chroma key low value.
In RGB chroma key mode, it is used as the red byte of the chroma key low value.
In YUV chroma key mode, it is used as the V of the chroma key low value.
If the value of the video data is greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced graphics data in the way defined by key operation mode.

.30 Video Control Misc. Register 3

Register Type: Read/Write
Read/Write Port: 3D5, Index 9Dh
Default: 00h

D7 Enable system memory video frame buffer
0: Disable
1: Enable
The captured frame buffer can be placed on system memory.
But this mode can only be enabled under shared-memory architecture.

D6 Support for Brooktree Bt819A video decoder SPI mode 1
0: Disable
1: Enable

D5 Enable VMI interrupt
0: Disable
1: Enable
The VMI device could cause interrupt when this bit is enabled.

D4 Enable VMI interface
0: Disable
1: Enable

D3 Enable VMI device access
0: Disable
1: Enable

D2 Chroma Key Format selection
0: RGB format
1: YUV format

D1 UV format select for video playback
0: CCIR 601 format
1: 2's complement format

D0 UV format select for video capture
0: CCIR 601 format
1: 2's complement format

.31 Video Playback Threshold Low Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 9Eh
Default: 00h

D7 Reserved

D[6:0] Video playback threshold low Bit[6:0]

Description:
This register contains the video line buffer threshold low.
The threshold low defines the video line buffer lower boundary which indicates the line buffer is not enough and the video data should be read from the DRAM.

.32 Video Playback Threshold High Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 9Fh
Default: 00h

D7 Reserved
D[6:0] Video playback threshold high Bit[6:0]

Description:
This register contains the video line buffer threshold high.
The threshold high defines the video line buffer upper boundary which indicates the data in the video line buffer is enough.
These two thresholds (video playback threshold low and threshold high) should be modified to get the maximum performance by compromising with the CRT threshold, video capture threshold, and DRAM refresh rate, etc.

.33 Line Buffer Size Register

Register Type: Read/Write
Read/Write Port: 3D5, Index A0h
Default: 00h

D[7:0] Line Buffer Size Bit[7:0]

Description:
This register should be set to the line buffer size used by playback. The size is in unit of quad-word.

.34 Video Overlay Color Key Blue High Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index A1h
Default: 00h

D[7:0] Blue Key High Value Bit[7:0]

Description:
This register contains the blue video overlay color key high value.
In 8-bit color mode, it is used as the color key high value.
In 16-bit color mode, it is used as the low byte of color key high value.
In 24-bit color mode, it is used as the blue byte of the color key high value.
If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

.35 Video Overlay Color Key Green High Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index A2h
Default: 00h

D[7:0] Green Key High Value Bit[7:0]

Description:
This register contains the green video overlay color key high value.
In 8-bit color mode, it is invalid.
In 16-bit color mode, it is used as the high byte of color key high value.
In 24-bit color mode, it is used as the green byte of the color key high value.
If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

.36 Video Overlay Color Key Red High Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index A3h
Default: 00h

D[7:0] Red Key High Value Bit[7:0]

Description:
This register contains the red video overlay color key high value.
In 8-bit color mode, it is invalid.
In 16-bit color mode, it is invalid.
In 24-bit color mode, it is used as the red byte of the color key high value.
If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

.37 Video Chroma Key B/Y High Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index A4h
Default: 00h

D[7:0] Video Chroma B/Y Key High Value Bit[7:0]

Description:
This register contains the blue or Y video overlay chroma key high value.
In RGB chroma key mode, it is used as the blue byte of the chroma key high value.
In YUV chroma key mode, it is used as the Y of the chroma key high value.
If the value of the video data is the greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced by graphics data in the way defined by key operation mode.

.38 Video Chroma Key G/U High Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index A5h
Default: 00h

D[7:0] Video Chroma G/U Key High Value Bit[7:0]

Description:
This register contains the green or U video overlay chroma key high value.
In RGB chroma key mode, it is used as the green byte of the chroma key high value.
In YUV chroma key mode, it is used as the U of the chroma key high value.
If the value of the video data is the greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced by graphics data in the way defined by key operation mode.

.39 Video Chroma Key R/V High Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index A6h
Default: 00h

D[7:0] Video Chroma R/V Key High Value Bit[7:0]

Description:
This register contains the red or V video overlay chroma key high value.
In RGB chroma key mode, it is used as the red byte of the chroma key high value.
In YUV chroma key mode, it is used as the V of the chroma key high value.
If the value of the video data is the greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced graphics data in the way defined by key operation mode.

.40 Graphics Data Alpha Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index A7h
Default: 00h

D[7:0] Graphics Data Alpha Value Bit[7:0]

Description:
The pixels of graphics data can be blended by graphics data alpha value, then added with the blended video data to generates blended data. The accuracy of the blending is 4 bits, the 4 MSBs of this register.

.41 Video Data Alpha Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index A8h
Default: 00h

D[7:0] Video Data Alpha Value Bit[7:0]

Description:
The pixels of video data can be blended by video data alpha value, then added with the blended graphics data to generates blended data. The accuracy of the blending is 4 bits, the 4 MSBs of this register.

.42 Key Overlay Operation Mode Register

Register Type: Read/Write

Read/Write Port: 3D5, Index A9h
Default: 00h

D[7:4] Reserved
D[3:0] Key Overlay Operation Mode Bit[3:0]

Description:
There are two keys for graphics data and video data overlay, which are color key and chroma key. The key overlay operation mode indicates the way the overlay would be performed.

Operation Mode	**Operation**
0000	always select graphics data
0001	select blended data when color key and chroma key, otherwise select graphics data
0010	select blended data when color key and not chroma key, otherwise select graphics data
0011	select blended data when color key, otherwise select graphics data
0100	select blended data when not color key and chroma key, otherwise select graphics data
0101	select blended data when chroma key, otherwise select graphics data
0110	select blended data when color key xor chroma key, otherwise select graphics data
0111	select blended data when color key or chroma key, otherwise select graphics data
1000	select blended data when not color key and not chroma key, otherwise select graphics data
1001	select blended data when color key xnor chroma key, otherwise select graphics data
1010	select blended data when not chroma key, otherwise select graphics data
1011	select blended data when color key or not chroma key, otherwise select graphics data
1100	select blended data when not chroma key, otherwise select graphics data
1101	select blended data when not color key or chroma key, otherwise select graphics data
1110	select blended data when not color key or not chroma key, otherwise select graphics data
1111	always select blended data

.43 Video Capture Horizontal Start Register

Register Type: Read/Write
Read/Write Port: 3D5, Index AAh

Default: 00h

D[7:0] Video Capture Horizontal Start Bit[7:0]

Description:
The Video Capture Horizontal Start Bit[10:0] indicate the left boundary of the captured video data. The Bit[10:8] is located in the Video Capture Horizontal Overflow Register (Index AEh, ".47" on page 133). The boundary is counted by the input video data clock. When the signal BLANK* is valid, the video data horizontal counter starts to count.
The video data capture would be started or continued when the video data horizontal counter is equal to or greater than the Video Capture Horizontal Start and the video data vertical counter is equal to or greater than the Video Capture Vertical Start.
The video data capture would be ended when the video data horizontal counter is equal to or greater than the Video Capture Horizontal End or the video data vertical counter is equal to or greater than the Video Capture Vertical End.

Note: This register should be set to zero at Brooktree BT819A video decoder SPI mode 2.

.44 Video Capture Horizontal End Register

Register Type: Read/Write
Read/Write Port: 3D5, Index ABh
Default: 00h

D[7:0] Video Capture Horizontal End Bit[7:0]

Description:
The Video Capture Horizontal End Bit[10:0] indicate the right boundary of the captured video data. The Bit[10:8] is located in the Video Capture Horizontal Overflow Register (Index AEh, ".47" on page 133). The boundary is counted by the input video data clock. When the signal BLANK* is valid, the video data horizontal counter starts to count.
The video data capture would be started or continued when the video data horizontal counter is equal to or greater than the Video Capture Horizontal Start and the video data vertical counter is equal to or greater than the Video Capture Vertical Start.
The video data capture would be ended when the video data horizontal counter is equal to or greater than the Video Capture Horizontal End or the video data vertical counter is equal to or greater than the Video Capture Vertical End.

.45 Video Capture Vertical Start Register

Register Type: Read/Write
Read/Write Port: 3D5, Index ACh
Default: 00h

D[7:0] Video Capture Vertical Start Bit[7:0]

Description:
The Video Capture Vertical Start Bit[9:0] indicate the upper boundary of the captured video data. The Bit[9:8] is located in the Video Capture Vertical Overflow Register (Index AFh, ".48" on page 133). The boundary is counted by the input video data clock. In the positive edge of the signal VDVSYNC, the video data vertical counter would be reset and then starts to count.

The video data capture would be started or continued when the video data horizontal counter is equal to or greater than the Video Capture Horizontal Start and the video data vertical counter is equal to or greater than the Video Capture Vertical Start.
The video data capture would be ended when the video data horizontal counter is equal to or greater than the Video Capture Horizontal End or the video data vertical counter is equal to or greater than the Video Capture Vertical End.

.46 Video Capture Vertical End Register

Register Type: Read/Write
Read/Write Port: 3D5, Index ADh
Default: 00h

D[7:0]	Video Capture Vertical End Bit[7:0]

Description:
The Video Capture Vertical End Bit[9:0] indicate the upper boundary of the captured video data. The Bit[9:8] is located in the Video Capture Vertical Overflow Register (Index Afh, ".48" on page 133). The boundary is counted by the input video data clock. In the positive edge of the signal VDVSYNC, the video data vertical counter would be reset and then starts to count.
The video data capture would be started or continued when the video data horizontal counter is equal to or greater than the Video Capture Horizontal Start and the video data vertical counter is equal to or greater than the Video Capture Vertical Start.
The video data capture would be ended when the video data horizontal counter is equal to or greater than the Video Capture Horizontal End or the video data vertical counter is equal to or greater than the Video Capture Vertical End.

.47 Video Capture Horizontal Overflow Register

Register Type: Read/Write
Read/Write Port: 3D5, Index AEh
Default: 00h

D7	Reserved
D[6:4]	Video Capture Horizontal End Bit[10:8]
D3	Reserved
D[2:0]	Video Capture Horizontal Start Bit[10:8]

.48 Video Capture Vertical Overflow Register

Register Type: Read/Write
Read/Write Port: 3D5, Index AFh
Default: 00h

D7	Reserved
D[6:4]	Video Data Input Delay Compensation Bit[2:0] 000: no delay 001: 2ns 010: 4ns 011: 6ns 100: inversed

101: 2ns, inversed
110: 4ns, inversed
111: 6ns, inversed
This field is programmed for input video data clock and input video data delay compensation.

D[3:2] Video Capture Vertical End Bit[9:8]
D[1:0] Video Capture Vertical Start Bit[9:8]

.49 System Memory Video Frame Buffer Setting Register 1

Register Type: Read/Write
Read/Write Port: 3D5, Index B0h
Default: 00h

D[7:0] Reserved

.50 System Memory Video Frame Buffer Setting Register 2

Register Type: Read/Write
Read/Write Port: 3D5, Index B1h
Default: 00h

D[7:0] Reserved

.51 System Memory Video Frame Buffer Setting Reg. 3 and Video Control Reg.

Register Type: Read/Write
Read/Write Port: 3D5, Index B2h
Default: 00h

D7 Enable Video Decimation
0: Disable
1: Enable
D[6:5] Reserved
D4 Support for Brooktree BT819A video decoder SPI mode 2
0: Disable
1: Enable
D[3:0] Reserved

.52 Contrast Enhancement Mean Value Sampling Rate Factor Register

Register Type: Read/Write
Read/Write Port: 3D5, Index B3h
Default: 00h

D[7:0] Contrast Enhancement Mean Value Sampling Rate Factor Bits[7:0]

Description:
The contrast enhancement needs mean value for each frame. This mean value is calculated by sampling some pixels from one video frame. The sampling rate = Contrast Enhancement Mean Value Sampling Rate Factor / 1024.

.53 Brightness

Register Type: Read/Write

Read/Write Port: 3D5, Index B4h
Default: 00h

D[7:0] Brightness Bit[7:0]

Description:
The Brightness is an 8-bit 2's complement number from -128 to +127. This value is added with the video data to control the brightness.

.54 Contrast Enhancement Control Register

Register Type: Read/Write
Read/Write Port: 3D5, Index B5h
Default: 00h

D[2:0] Contrast Gain Bit[2:0]
000: 1.0
001: 1.0625
010: 1.125
011: 1.1875
100: 1.25
101: 1.3125
110: 1.375
111: 1.4375

D[5:3] Contrast Mean Frame Samples Bit[2:0]
000: 2 frames
001: 4 frames
010: Reserved
011: 8 frames
100: Reserved
101: Reserved
110: Reserved
111: 16 frames

D[7:6] Contrast Mean Pixel Samples Bit[1:0]
00: 2048 pixels
01: 4096 pixels
10: 8192 pixels
11: 16384 pixels

.55 Video Control Misc. Register 4

Register Type: Read/Write
Read/Write Port: 3D5, Index B6h
Default: 00h

D[1:0] CPU Writing Video Data Type
00: RGB 555
01: YUV 422
10: RGB 565
11: Reserved

D2 Enable YUV 420 mode

0: Disable
1: Enable

D[7:3] Reserved

.56 Video U Plane Starting Address Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index B7h
Default: 00h

D[7:0] Video U Plane Starting Address Low Bit[7:0]

.57 Video U Plane Starting Address Middle Register

Register Type: Read/Write
Read/Write Port: 3D5, Index B8h
Default: 00h

D[7:0] Video U Plane Starting Address Middle Bit[15:8]

.58 Video UV Plane Starting Address High Register

Register Type: Read/Write
Read/Write Port: 3D5, Index B9h
Default: 00h

D[7:4] Video V Plane Starting Address High Bit[19:16]
D[3:0] Video U Plane Starting Address High Bit[19:16]

.59 Video V Plane Starting Address Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index BAh
Default: 00h

D[7:0] Video V Plane Starting Address Low Bit[7:0]

.60 Video V Plane Starting Address Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index BBh
Default: 00h

D[7:0] Video V Plane Starting Address Middle Bit[15:8]

.61 Video UV Plane Offset Register

Register Type: Read/Write
Read/Write Port: 3D5, Index BCh
Default: 00h

D[7:0] Video UV Plane Offset Bit[7:0]

.62 Video UV Plane Offset High Register

Register Type: Read/Write
Read/Write Port: 3D5, Index BDh
Default: 00h

D[7:4] Reserved
D[3:0] Video UV Plane Offset Bit[11:8]

.63 Index Register of TV-OUT Registers

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h
Default: 00h

D[7:0] TV-OUT Register Index

Note: For detail TV-OUT Registers description, please refer to "13 TV OUT Registers" on page 150.

.64 Data Register of TV-OUT Registers

Register Type: Read/Write
Read/Write Port: 3D5, Index E1h
Default: 00h

D[7:0] TV-OUT Register Data

Note: For detail TV-OUT Registers description, please refer to "13 TV OUT Registers" on page 150.

10 PCI Configuration Registers

.1 Configuration Register 00h

Register Type: Read
Read Port: 0000h
Default: 63261039h

D[31:16] Device ID
SiS6326 Device ID is 6326h
D[15:0] Vendor ID
Integrated Vendor ID is 1039h

.2 Configuration Register 04h

Register Type: Read/Write
Read Port: 0004h
Default: 02200004h

D[26:25] DEVSEL* timing (= 01, Read Only)
00: fast
01: medium (fixed at this value)
10: slow
D21 66 MHz Capable
0: Support 33MHz
1: Support 66 MHz (fixed at this value)
D12 Capabilities List
0: does not implement a list of capabilities
1: implements a list of capabilities
D5 VGA Palette Snoop
0: Disable
1: Enable
D3 Bus Master
0: Device is not a bus master
1: Device is a bus master (fixed at this value)
D1 Memory Space
0: Disable
1: Enable
D0 I/O Space
0: Disable
1: Enable

.3 Configuration Register 08h

Register Type: Read
Read Port: 0008h
Default: 030000AXh

D[31:8] Class Code (= 030000h)
D[7:0] Revision ID (= Axh, for Rev. Ax)

.4 Configuration Register 10h

Register Type: Read/Write
Read Port: 0010h
Default: 00000008h

D[31:0] 32-bit memory base register for 4MB linear frame buffer

.5 Configuration Register 14h

Register Type: Read/Write
Read Port: 0014h
Default: 00000000h

D[31:0] 32-bit memory base register for 64KB memory mapped I/O

.6 Configuration Register 18h

Register Type: Read/Write
Read Port: 0018h
Default: 00000001h

D[31:0] 32-bit I/O base register for 16 I/O space which is reserved for VMI interface

.7 Configuration Register 2Ch

Register Type: Read/Write Once Only
Read Port: 002Ch
Default: 00000000h

D[31:16] Subsystem ID
D[15:0] Subsystem Vendor ID

.8 Configuration Register 30h

Register Type: Read/Write
Read Port: 0030h
Default: 000C0000h

D[31:11] Expansion ROM Base Address
D0 ROM Enable Bit
0: Disable
1: Enable

.9 Configuration Register 3Ch

Register Type: Read/Write
Read Port: 003Ch
Default: 00000100h

If D3 of SRE (".11" on page 86) is 1, then
D[15:8] Interrupt Pin (= 01h, Read Only)
D[7:0] Interrupt Line (= 00h)

If D3 of SRE (".11" on page 86) is 0, then
D[15:8] Interrupt Pin (= 00h, Read Only)
D[7:0] Interrupt Line (= 00h)

11 AGP Configuration Registers

Note: All the registers described in this section can be accessed only when AGP is enable.

.1 Configuration Register 34h

Register Type: Read Only
Read Port: 0034h
Default: 00000050h

D[7:0]	Capabilities list offset pointer (Read Only)

.2 Configuration Register 50h

Register Type: Read Only
Read Port: 0050h
Default: 00105c02h

D[23:20]	Major revision number
D[19:16]	Minor revision number
D[15:8]	Pointer to next item
D[7:0]	Cap_ID: value 02h identifies the list item as pertaining to AGP register

.3 Configuration Register 54h

Register Type: Read Only
Read Port: 0054h
Default: 01000003h

D[31:24]	Maximum number of AGP command requests
D9	Side band addressing support 0: Not support 1: Support
D1	2X mode support 0: Not support 1: Support
D0	1X mode support 0: Not support 1: Support

.4 Configuration Register 58h

Register Type: Read/Write
Read Port: 0058h
Default: 00000000h

D[31:24]	Maximum number of AGP requests can be enqueued
D9	1: side band address mode enable 0: sideband address mode disable
D8	1: AGP enable 0: AGP disable
D1	1: 2X mode enable 0: 2X mode disable

D0	1: 1X mode enable 0: 1X mode disable

.5 Configuration Register 5Ch

Register Type:	Read
Read Port:	005Ch
Default:	00000000h

D[15:8]	NULL: 00h indicates final item in the capability list

12 MPEG Video Decoder Registers

.1 IDCT Coefficient Register

Register Type: Read/Write
Read/Write Port: 8600h~86FFh
Default: all 0

All Memory Mapped I/O 86XX are decoded into this IDCT coefficient register. The definitions of the bit fields in this register depend on the value of MCMDMODE (3C4h, Index 39h, "7.7.60" on page 138). If it is set to 0, the definitions of the bit fields are:

D[11:0]	12-bit Dequantized IDCT Coefficient
D[15:12]	Reserved
D[21:16]	6-bit IDCT Run Length Coefficient
D[31:22]	Reserved

If MCMDMODE is set to 1, then there are three command types which are identified by D31 (rvmode[1]) and D15 (rvmode[0]).

Type 1. rvmode[1:0] = 00 (for two run-value pairs, whose values are between -256 and 255)

D[8:0]	9-bit Dequantized IDCT Coefficient0
D[14:9]	6-bit IDCT Run Length Coefficient0
D[24:16]	9-bit Dequantized IDCT Coefficient1
D[30:25]	6-bit IDCT Run Length Coefficient1

Type 2. rvmode[1:0] = 01 (for one run-value pair, whose value is between 256 and 2047 or between -2048 and -257)

D[8:0]	Reserved
D[14:9]	6-bit IDCT Run Length Coefficient
D[27:16]	12-bit Dequantized IDCT Coefficient
D[30:28]	Reserved

Type 3. rvmode[1:0] = 10 (for one run-value pair, whose value is between -256 and 255)

D[8:0]	9-bit Dequantized IDCT Coefficient
D[14:9]	6-bit IDCT Run Length Coefficient
D[30:16]	Reserved

.2 Macro-Block Type Register

Register Type: Read/Write
Read/Write Port: 8700h~8703h
Default: all 0

D[31:28]	Sub-Pixel Compensation Flag of the Fourth Motion Vector: filflgd[3:0] Bit definitions are the same as filflga[3:0].
D[27:24]	Sub-Pixel Compensation Flag of the Third Motion Vector: filflgc[3:0] Bit definitions are the same as filflga[3:0].
D[23:20]	Sub-Pixel Compensation Flag of the Second Motion Vector: filflgb[3:0] Bit definitions are the same as filflga[3:0].
D[19:16]	Sub-Pixel Compensation Flag of the First Motion Vector: filflga[3:0] filflga3: for chrominance block in vertical direction 1: enable sub-pixel compensation

	0: disable filflga2: for chrominance block in horizontal direction 1: enable sub-pixel compensation 0: disable filflga1: for luminance block in vertical direction 1: enable sub-pixel compensation 0: disable filflga0: for luminance block in horizontal direction 1: enable sub-pixel compensation 0: disable
D15	Field Type 1: Bottom Field 0: Top Field or Frame Picture In MPEG-1, always set to 0.
D14	DCT Encoding Type 1: Field Based DCT for Frame Picture 0: Frame Based DCT for Frame Picture If picture type is field picture, always set to 1. In MPEG-1, it is always setto 0.
D[13:12]	Motion Compensation Mode Bit[1:0] If picture type is frame picture, 00: Intra Macro-Block 01: Field Mode Compensation 10: Frame Mode Compensation 11: Dual Prime Mode Compensation If picture type is field picture, 00: Intra Macro-Block 01: Field Mode Compensation 10: 16*8 Mode Compensation 11: Dual Prime Mode Compensation In MPEG-1, only frame mode compensation is used.
D11	Picture Type Flag 1: Field Picture 0: Frame Picture In MPEG-1, only frame picture is used.
D10	Backward Compensation Flag 1: Required 0: Not Required
D9	Forward Compensation Flag 1: Required 0: Not Required
D8	Macro-Block Intra Flag 1: Current Macro-Block is Intra Macro-Block. 0: Current Macro-Block is not Intra Macro-Block
D7	Flag of Wait for Page Flip End 1: Wait for Flipping End Signal 0: Do not Wait for Flipping End Signal

D6	Flag of Last Macro-Block of Each Picture 1: Last Macro-Block of a Picture 0: Not the Last Macro-Block of a Picture
D[5:0]	Coded Block Pattern: cbp[5:0] cbp[5] =1, if Y0 block IDCT data exists in the stream cbp[4] =1, if Y1 block IDCT data exists in the stream cbp[3] =1, if Y2 block IDCT data exists in the stream cbp[2] =1, if Y3 block IDCT data exists in the stream cbp[1] =1, if Cb block IDCT data exists in the stream cbp[0] =1, if Cr block IDCT data exists in the stream

.3 Macro-Block Address Register

Register Type: Read/Write
Read/Write Port: 8704h~8707h
Default: all 0

D[5:0]	X Coordinate of Current Macro-Block Bit[5:0]
D[9:6]	Reserved
D[11:10]	Current Buffer Select Bit[1:0] 00: Use Buffer0 01: Use Buffer1 10: Use Buffer2 11: Use Buffer3
D[15:12]	Reserved
D[21:16]	Y Coordinate of Current Macro-Block Bit[5:0]
D[31:22]	Reserved

Description:
The X and Y coordinate of current macro-block present the position in a frame or field picture in macro-block unit.

.4 The First Motion Vector Register

Register Type: Read/Write
Read/Write Port: 8708h~870Bh
Default: all 0

D[9:0]	X Direction Vector Relative to Buffer Origin Bit[9:0] in Pixel Unit
D[11:10]	Buffer Select Bit[1:0] 00: Reference Buffer0 01: Reference Buffer1 10: Reference Buffer2 11: Reference Buffer3
D[14:12]	Reserved
D15	X Direction Chrominance Vector Add One Flag 1: Add one 0: not
D[25:16]	Y Direction Vector Relative to Buffer Origin Bit[9:0] in Pixel Unit
D[30:26]	Reserved
D31	Y Direction Chrominance Vector Add One Flag

1: Add one
0: not

Description:
The X and Y Direction Chrominance Vector Add One Flags are set to 1 when the PMV values of x and y direction equal to -(4m+1), where m= 0, 1, 2, 3, ...

.5 The Second Motion Vector Register

Register Type: Read/Write
Read/Write Port: 870Ch~870Fh
Default: all 0

The definitions of the bit fields are the same as those of the First Motion Vector Register.

.6 The Third Motion Vector Register

Register Type: Read/Write
Read/Write Port: 8710h~8713h
Default: all 0

The definitions of the bit fields are the same as those of the First Motion Vector Register.

.7 The Fourth Motion Vector Register

Register Type: Read/Write
Read/Write Port: 8714h~8717h
Default: all 0

The definitions of the bit fields are the same as those of the First Motion Vector Register.

.8 Dummy Register 1

Register Type: Write
Write Port: 8718h
Default: all 0

Description:
This register is written at the end of the Motion Compensation Parameter series to indicate the end of the Motion Compensation Parameters. The content written into this register is ignored because there is no physical device for the content storage.

.9 Dummy Register 2

Register Type: Write
Write Port: 871Ch
Default: all 0

Description:
This register is written at the end of every block of IDCT coefficients to indicated the end of one 8x8 IDCT block. The content written into this register is ignored because there is no physical device for the content storage.

.10 MPEG Page Flip Buffer Register

Register Type: Read/Write
Read/Write Port: 8720h~8723h

Default: all 0

D[1:0]	Buffer Select for Video Playback Page Flip 00: Use Buffer0 01: Use Buffer1 10: Use Buffer2 11: Use Buffer3
D2	Even/Odd Field Select 1: Even Field 0: Odd Field or Frame Picture
D[31:3]	Reserved

.11 Line Offset Register

Register Type: Read/Write
Read/Write Port: 8724h~8727h
Default: all 0

D[7:0]	Luminance Line Offset in Double Word Unit
D[15:8]	Reserved
D[23:16]	Chrominance Line Offset in double Word Unit
D[30:24]	Reserved
D31	Scan Type of the Current DCT-Encoded Block 1: Alternate Scan 0: Zig-Zag Scan

.12 Y Section Start Address of MPEG Buffer0 Register

Register Type: Read/Write
Read/Write Port: 8728h~872Bh
Default: all 0

D[31:20]	Reserved
D[19:0]	Y Section Start Address of MPEG Buffer0 in Double Word Unit

.13 Cb Section Start Address of MPEG Buffer0 Register

Register Type: Read/Write
Read/Write Port: 872Ch~872Fh
Default: all 0

D[31:20]	Reserved
D[19:0]	Cb Section Start Address of MPEG Buffer0 in Double Word Unit

.14 Cr Section Start Address of MPEG Buffer0 Register

Register Type: Read/Write
Read/Write Port: 8730h~8733h
Default: all 0

D[31:20]	Reserved
D[19:0]	Cr Section Start Address of MPEG Buffer0 in Double Word Unit

.15 Y Section Start Address of MPEG Buffer1 Register

Register Type: Read/Write
Read/Write Port: 8734h~8737h
Default: all 0

D[31:20] Reserved
D[19:0] Y Section Start Address of MPEG Buffer1 in Double Word Unit

.16 Cb Section Start Address of MPEG Buffer1 Register

Register Type: Read/Write
Read/Write Port: 8738h~873Bh
Default: all 0

D[31:20] Reserved
D[19:0] Cb Section Start Address of MPEG Buffer1 in Double Word Unit

.17 Cr Section Start Address of MPEG Buffer1 Register

Register Type: Read/Write
Read/Write Port: 873Ch~873fh
Default: all 0

D[31:20] Reserved
D[19:0] Cr Section Start Address of MPEG Buffer1 in Double Word Unit

.18 Y Section Start Address of MPEG Buffer2 Register

Register Type: Read/Write
Read/Write Port: 8740h~8743h
Default: all 0

D[31:20] Reserved
D[19:0] Y Section Start Address of MPEG Buffer2 in Double Word Unit

.19 Cb Section Start Address of MPEG Buffer2 Register

Register Type: Read/Write
Read/Write Port: 8744h~8747h
Default: all 0

D[31:20] Reserved
D[19:0] Cb Section Start Address of MPEG Buffer2 in Double Word Unit

.20 Cr Section Start Address of MPEG Buffer2 Register

Register Type: Read/Write
Read/Write Port: 8748h~874Bh
Default: all 0

D[31:20] Reserved
D[19:0] Cb Section Start Address of MPEG Buffer2 in Double Word Unit

.21 Y Section Start Address of MPEG Buffer3 Register

Register Type: Read/Write
Read/Write Port: 874Ch~874Fh
Default: all 0

D[31:20]	Reserved
D[19:0]	Y Section Start Address of MPEG Buffer3 in Double Word Unit

.22 Cb Section Start Address of MPEG Buffer2 Register

Register Type: Read/Write
Read/Write Port: 8750h~8753h
Default: all 0

D[31:20]	Reserved
D[19:0]	Cb Section Start Address of MPEG Buffer3 in Double Word Unit

.23 Cr Section Start Address of MPEG Buffer2 Register

Register Type: Read/Write
Read/Write Port: 8754h~8757h
Default: all 0

D[31:20]	Reserved
D[19:0]	Cb Section Start Address of MPEG Buffer3 in Double Word Unit

.24 MPEG Status Register

Register Type: Read
Read Port: 8758h~875Bh
Default: xxh

D[31:19]	Reserved
D18	Motion Compensation Status 1: Motion Compensation Busy 0: Motion Compensation Free
D17	IDCT Status 1: IDCT Busy 0: IDCT Free
D16	MPEG decoder Idle Status 1: MPEG decoder Idle 0: MPEG decoder Busy
D[15:0]	Available Command Queue Length

13 TV OUT Registers

Index Register of TV-OUT Registers

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h
Default: 00h

D[7:0] TV-OUT Register Index

Data Register of TV-OUT Registers

Register Type: Read/Write
Read/Write Port: 3D5, Index E1h
Default: 00h

D[7:0] TV-OUT Register Data

.1 VR0: Basic TV Function Control Register

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 00h
3D5, Index E1h
Default: 00h

D[7:5] FSEL, TV antiflicker mode selection
000: No filtering
001: Light filtering
010: Median filtering
011: Strong filtering
1xx: Adaptive filtering

D4 COMPN, Composite signal out
0: Enable Composite TV siganl out
1: Disable Composite TV signal out

D3 SVIDEON, S-Video signal out
0: Enable S-Video signal out
1: Disable S-Video signal out

D2 ENTV, Enable TV mode
0: Disable
1: Enable

D1 SHRINK, Shrink VGA vertical display to fit into TV mode
0: Normal, no shrinking
1: Shrink

D0 REGODD, Set interlace scan mode
0: Set non-interlace scan mode, odd lines are always displayed.
1: Set interlace scan mode

.2 VR1: Vertical Shrink Scale

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 01h
3D5, Index E1h

Default: 00h

D[7:0] TVSCALE[7:0]

.3 VR2: Phase Increment for Sub-carrier Frequency Generation 1

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 02h
3D5, Index E1h
Default: 00h

D7 NTSC/PAL mode select
0: Select NTST mode TV output
1: Select PAL mode TV output
D[6:0] FSC[22:16]

.4 VR3: Phase Increment for Sub-carrier Frequency Generation 2

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 03h
3D5, Index E1h
Default: 00h

D[7:0] FSC[15:8]

.5 VR4: Phase Increment for Sub-carrier Frequency Generation 3

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 04h
3D5, Index E1h
Default: 00h

D[7:0] FSC[7:0]

.6 VR5: TV Vertical Active Start: Odd Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 05h
3D5, Index E1h
Default: 00h

D[7:0] RTVACTSO[7:0]

Note: RTVACTSO[9:8] are located in VR9 D[1:0].

.7 VR6: TV Vertical Active Start: Even Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 06h
3D5, Index E1h
Default: 00h

D[7:0] RTVACTSE[7:0]

Note: RTVACTSE[9:8] are located in VR9 D[3:2].

.8 VR7: TV Vertical Active End: Odd Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 07h
3D5, Index E1h
Default: 00h

D[7:0] RTVACTEO[7:0]

Note: RTVACTEO[9:8] are located in VR9 D[5:4].

.9 VR8: TV Vertical Active End: Even Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 08h
3D5, Index E1h
Default: 00h

D[7:0] RTVACTEE[7:0]

Note: RTVACTEE[9:8] are located in VR9 D[7:6].

.10 VR9: Overflow Register 1

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 09h
3D5, Index E1h
Default: 00h

D[1:0] RTVACTSO[9:8]
D[3:2] RTVACTSE[9:8]
D[5:4] RTVACTEO[9:8]
D[7:6] RTVACTEE[9:8]

.11 VR0A: TV Vertical SYNC End: Odd Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 0Ah
3D5, Index E1h
Default: 00h

D[7:0] RVSYNCEO[7:0]

Note: RVSYNCEO[9:8] are located in VR0E D[1:0].

.12 VR0B: TV Vertical Equalizer1 End: Odd Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 0Bh
3D5, Index E1h
Default: 00h

D[7:0] RVEQ1EO[7:0]

Note: RVEQ1EO[9:8] are located in VR0E D[3:2].

.13 VR0C: TV Vertical Equalizer2 End: Odd Field

Register Type: Read/Write

Read/Write Port: 3D5, Index E0h, Index 0Ch
3D5, Index E1h
Default: 00h

D[7:0] RVEQ2EO[7:0]

Note: RVEQ2EO[9:8] are located in VR0E D[5:4].

.14 VR0D: TV Vertical SYNC End: Even Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 0Dh
3D5, Index E1h
Default: 00h

D[7:0] RVSYNCEE[7:0]

Note: RVSYNCEE[9:8] are located in VR0E D[7:6].

.15 VR0E: Overflow Register 2

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 0Eh
3D5, Index E1h
Default: 00h

D[1:0] RVSYNCEO[9:8]
D[3:2] RVEQ1EO[9:8]
D[5:4] RVEQ2EO[9:8]
D[7:6] RVEQ1EE[9:8]

.16 VR0F: TV Vertical Equalizer1 End: Even Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 0Fh
3D5, Index E1h
Default: 00h

D[7:0] RVEQ1EE[7:0]

Note: RVEQ1EE[9:8] are located in VR13 D[1:0].

.17 VR10: TV Vertical Equalizer2 End: Even Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 10h
3D5, Index E1h
Default: 00h

D[7:0] RVEQ2EE[7:0]

Note: RVEQ2EE[9:8] are located in VR13 D[3:2].

.18 VR11: TV Vertical Counter Initial Value

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 11h

3D5, Index E1h
Default: 00h

D[7:0] RTVVCINI[7:0]

Note: RTVVCINI[9:8] are located in VR13 D[5:4].

.19 VR12: Line Buffer Read Address Initial Value

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 12h
3D5, Index E1h
Default: 00h

D[7:0] RAINI[7:0]

Note: RAINI[9:8] are located in VR13 D[7:6].

.20 VR13: Overflow Register 3

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 13h
3D5, Index E1h
Default: 00h
Register Type: Read/Write

D[1:0] RVEQ1EE[9:8]
D[3:2] RVEQ2EE[9:8]
D[5:4] RTVVCINI[9:8]
D[7:6] RAINI[9:8]

.21 VR14: Frame 1 Burst Start: Odd Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 14h
3D5, Index E1h
Default: 00h

D[7:0] RF1BRSTSO[7:0]

Note: RF1BRSTSO[9:8] are located in VR18 D[1:0].

.22 VR15: Frame 1 Burst Start: Even Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 15h
3D5, Index E1h
Default: 00h

D[7:0] RF1BRSTSE[7:0]

Note: RF1BRSTSE[9:8] are located in VR18 D[3:2].

.23 VR16: Frame 1 Burst End: Odd Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 16h

3D5, Index E1h
Default: 00h

D[7:0] RF1BRSTEO[7:0]

Note: RF1BRSTEO[9:8] are located in VR18 D[5:4].

.24 VR17: Frame 1 Burst End: Even Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 17h
3D5, Index E1h
Default: 00h

D[7:0] RF1BRSTEE[7:0]

Note: RF1BRSTEE[9:8] are located in VR18 D[7:6].

.25 VR18: Overflow Register 4

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 18h
3D5, Index E1h
Default: 00h

D[1:0] RF1BRSTSO[9:8]
D[3:2] RF1BRSTSE[9:8]
D[5:4] RF1BRSTEO[9:8]
D[7:6] RF1BRSTEE[9:8]

.26 VR19: Frame 2 Burst Start: Odd Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 19h
3D5, Index E1h
Default: 00h

D[7:0] RF2BRSTSO[7:0]

Note: RF2BRSTSO[9:8] are located in VR1D D[1:0].

.27 VR1A: Frame 2 Burst Start: Even Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 1Ah
3D5, Index E1h
Default: 00h

D[7:0] RF2BRSTSE[7:0]

Note: RF2BRSTSE[9:8] are located in VR1D D[3:2].

.28 VR1B: Frame 2 Burst End: Odd Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 1Bh
3D5, Index E1h

Default: 00h

D[7:0] RF2BRSTEO[7:0]

Note: RF2BRSTEO[9:8] are located in VR1D D[5:4].

.29 VR1C: Frame 2 Burst End: Even Field

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 1Ch
3D5, Index E1h
Default: 00h

D[7:0] RF2BRSTEE[7:0]

Note: RF2BRSTEE[9:8] are located in VR1D D[7:6].

.30 VR1D: Overflow Register 5

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 1Dh
3D5, Index E1h
Default: 00h

D[1:0] RF2BRSTSO[9:8]
D[3:2] RF2BRSTSE[9:8]
D[5:4] RF2BRSTEO[9:8]
D[7:6] RF2BRSTEE[9:8]

.31 VR1E: Half Line Definition for Vertical SYNC/Equal./Display

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 1Eh
3D5, Index E1h
Default: 00h

D7 RTVACTSOh
0: Odd field TV Active Video start at the half of TV scan line
1: Odd field TV Active Video start at the beginning of TV scan line
D6 RTVACTSEh
0: Even field TV Active Video start at the half of TV scan line
1: Even field TV Active Video start at the beginning of TV scan line
D5 RTVACTEOh
0: Odd field TV Active Video end at the half of TV scan line
1: Odd field TV Active Video end at the end of TV scan line
D4 RTVACTEEh
0: Even field TV Active Video end start at the half of TV scan line
1: Even field TV Active Video end at the end of TV scan line
D3 RVSYNCEOh
0: Odd field TV Vertical SYNC end at the half of TV scan line
1: Odd field TV Vertical SYNC end at the end of TV scan line
D2 RVEQ1EOh
0: Odd field TV First Equalizer end at the half of TV scan line

1: Odd field TV First Equalizer end at the end of TV scan line

D1 RVEQ2EOh
0: Odd field TV Second Equalizer end at the half of TV scan line
1: Odd field TV Second Equalizer end at the end of TV scan line

D0 RVSYNCEEh
0: Even field TV Vertical SYNC end at the half of TV scan line
1: Even field TV Vertical SYNC end at the end of TV scan line

.32 VR1F: SYNC Slop/Level

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 1Fh
3D5, Index E1h
Default: 00h

D7 RVEQ1EEh
0: Even field TV First Equalizer end at the half of TV scan line
1: Even field TV First Equalizer end at the end of TV scan line

D6 RVEQ2EEh
0: Even field TV Second Equalizer end at the half of TV scan line
1: Even field TV Second Equalizer end at the end of TV scan line

D[5:1] RSYSLOP[4:0]
TV horizontal SYNC expansion slop

D0 RSYNCLV[8]
TV horizontal SYNC level Bit[8]
Bit[7:0] are located in VR20 D[7:0]

.33 VR20: TV Horizontal SYNC Level

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 20h
3D5, Index E1h
Default: 00h

D[7:0] RSYNCLV[7:0]

.34 VR21: Vertical State Initial Value

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 21h
3D5, Index E1h
Default: 00h

D[7:5] Reserved
D[4:0] RVSTINI[4:0]

.35 VR22: TV Horizontal Cycle Count

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 22h
3D5, Index E1h
Default: 00h

D[7:0] HTVCOUNT[7:0]

Note: HTVCOUNT[11:8] are located in VR24 D[3:0].

.36 VR23: TV Horizontal Burst Start

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 23h
3D5, Index E1h
Default: 00h

D[7:0] RHBURSTS[7:0]

Note: RHBURSTS[11:8] are located in VR24 D[7:4].

.37 VR24: Overflow Register 6

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 24h
3D5, Index E1h
Default: 00h

D[7:4] RHBURSTS[11:8]
D[3:0] HTVCOUNT[11:8]

.38 VR25: TV Horizontal Burst End

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 25h
3D5, Index E1h
Default: 00h

D[7:0] RHBURSTE[7:0]

Note: RHBURSTE[11:8] are located in VR24 D[3:0].

.39 VR26: TV Horizontal Blank End

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 26h
3D5, Index E1h
Default: 00h

D[7:0] RHBLKE[7:0]

Note: RHBLKE[11:8] are located in VR27 D[7:4].

.40 VR27: Overflow Register 7

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 27h
3D5, Index E1h
Default: 00h

D[7:4] RHBLKE[11:8]
D[3:0] RHBURSTE[11:8]

.41 VR28: TV Horizontal SYNC Start

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 28h
3D5, Index E1h
Default: 00h

D[7:0] RHSYS[7:0]

Note: RHSYS[11:8] are located in VR2A D[3:0].

.42 VR29: TV Horizontal SYNC Start: Half Line

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 29h
3D5, Index E1h
Default: 00h

D[7:0] RHFSYS[7:0]

Note: RHFSYS[11:8] are located in VR2A D[7:4].

.43 VR2A: Overflow Register 8

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 2Ah
3D5, Index E1h
Default: 00h

D[7:4] RHFSYS[11:8]
D[3:0] RHSYS[11:8]

.44 VR2B: TV Horizontal SYNC Expansion2 Start

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 2Bh
3D5, Index E1h
Default: 00h

D[7:0] RHSYEXP2S[7:0]

Note: RHSYEXP2S[11:8] are located in VR2D D[3:0].

.45 VR2C: TV Horizontal SYNC Expansion2 End

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 2Ch
3D5, Index E1h
Default: 00h

D[7:0] RHSYEXP2E[7:0]

Note: RHSYEXP2E[11:8] are located in VR2D D[7:4].

.46 VR2D: Overflow Register 9

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 2Dh
3D5, Index E1h

Default: 00h

D[7:4] RHSYEXP2E[11:8]
D[3:0] RHSYEXP2S[11:8]

.47 VR2E: TV Equalizer Pulse End

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 2Eh
3D5, Index E1h
Default: 00h

D[7:0] RHEQPLE[7:0]

Note: RHEQPLE[11:8] are located in VR30 D[3:0].

.48 VR2F: TV Equalizer Pulse End: Half Line

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 2Fh
3D5, Index E1h
Default: 00h

D[7:0] RHFEQPLE[7:0]

Note: RHFEQPLE[11:8] are located in VR30 D[7:4].

.49 VR30: Overflow Register 10

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 30h
3D5, Index E1h
Default: 00h

D[7:4] RHFEQPLE[11:8]
D[3:0] RHEQPLE[11:8]

.50 VR31: TV SYNC Pulse End

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 31h
3D5, Index E1h
Default: 00h

D[7:0] RHSYPLE[7:0]

Note: RHSYPLE[11:8] are located in VR33 D[3:0].

.51 VR32: TV SYNC Pulse End: Half Line

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 32h
3D5, Index E1h
Default: 00h

D[7:0] RHFSYPLE[7:0]

Note: RHFSYPLE[11:8] are located in VR33 D[7:4].

.52 VR33: Overflow Register 11

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 33h
3D5, Index E1h
Default: 00h

D[7:4]	RHFSYPLE[11:8]
D[3:0]	RHSYPLE[11:8]

.53 VR34: TV Equalizer SYNC Expansion2 End

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 34h
3D5, Index E1h
Default: 00h

D[7:0]	RHEQSYE[7:0]

Note: RHEQSYE[11:8] are located in VR36 D[3:0].

.54 VR35: TV Equalizer SYNC Expansion2 End: Half Line

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 35h
3D5, Index E1h
Default: 00h

D[7:0]	RHFEQSYE[7:0]

Note: RHFEQSYE[11:8] are located in VR36 D[7:4].

.55 VR36: Overflow Register 12

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 36h
3D5, Index E1h
Default: 00h

D[7:4]	RHFEQSYE[11:8]
D[3:0]	RHEQSYE[11:8]

.56 VR37: TV SYNC SYNC-Expansion2 End

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 37h
3D5, Index E1h
Default: 00h

D[7:0]	RHSYSYE[7:0]

Note: RHSYSYE[11:8] are located in VR39 D[3:0].

.57 VR38: TV SYNC SYNC-Expansion2 End: Half Line

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 38h

3D5, Index E1h
Default: 00h

D[7:0] RHFSYSYE[7:0]

Note: RHFSYSYE[11:8] are located in VR39 D[7:4].

.58 VR39: Overflow Register 13

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 39h
3D5, Index E1h
Default: 00h

D[7:4] RHFSYSYE[11:8]
D[3:0] RHSYSYE[11:8]

.59 VR3A: TV Horizontal Active Start

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 3Ah
3D5, Index E1h
Default: 00h

D[7:0] RHACTS[7:0]

Note: RHACTS[11:8] are located in VR3C D[3:0].

.60 VR3B: TV Horizontal Blank-Expansion2 End

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 3Bh
3D5, Index E1h
Default: 00h

D[7:0] RHBK2XPE[7:0]

Note: RHBK2XPE[11:8] are located in VR3C D[7:4].

.61 VR3C: Overflow Register 14

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 3Ch
3D5, Index E1h
Default: 00h

D[7:4] RHBK2XPE[11:8]
D[3:0] RHACTS[11:8]

.62 VR3D: TV Horizontal Blank-Expansion2 End: Half Line

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 3Dh
3D5, Index E1h
Default: 00h

D[7:0] RHFBK2XPE[7:0]

Note: RHFBK2XPE[11:8] are located in VR3F D[3:0].

.63 VR3E: TV Horizontal Active End

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 3Eh
3D5, Index E1h
Default: 00h

D[7:0]	RHACTE[7:0]

Note: RHACTE[11:8] are located in VR3F D[7:4].

.64 VR3F: Overflow Register 15

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 3Fh
3D5, Index E1h
Default: 00h

D[7:4]	RHACTE[11:8]
D[3:0]	RHFBK2XPE[11:8]

.65 VR40: TV Horizontal Active End: Half Line

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 40h
3D5, Index E1h
Default: 00h

D[7:0]	RHFACTE[7:0]

Note: RHFACTE[11:8] are located in VR41 D[3:0].

.66 VR41: TV Horizontal Active End: Half Line

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 41h
3D5, Index E1h
Default: 00h

D[7:4]	Reserved
D[3:0]	RHFACTE[11:8]

.67 VR42: TV DAC Sense Input Register 1

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 42h
3D5, Index E1h
Default: 00h

D[7:0]	PYCIN[7:0]

Note: PYCIN[9:8] are located in VR43 D[1:0].

.68 VR43: TV DAC Sense Input Register 2/Encoder Filter Enable Bits

Register Type: Read/Write

Read/Write Port: 3D5, Index E0h, Index 43h
3D5, Index E1h
Default: 00h

D[7:5]	Reserved
D4	ENYF 0: Bypass Y filter 1: Enable Y filter
D3	ENCF 0: Bypass chrominance filter 1: Enable chrominance filter
D2	TVSENSE 0: Disable TVSENSE 1: Enable TVSENSE
D[1:0]	PYCIN[9:8]

.69 VR44: TV DAC Sense Read-back Register

Register Type: Read/Write
Read/Write Port: 3D5, Index E0h, Index 44h
3D5, Index E1h
Default: 00h

D[7:3]	Reserved
D2	RSENY Y signal read-back
D1	RSENC Cb & Cr signal read-back
D0	RSENCO Composite signal read-back

14 3D Programming Registers

.1 Legend of 3D Registers

Notation	Definition
(number)	The number of bits
(f)	Floating point representation
(i)	Integer representation
(s12)	Sign Magnitude Representation with 12 integer bits
A	Alpha component
A8	Alpha component, 8 bits integer representation
$Addr_{number}$	Address buss
Apix	Alpha component of a pixel
Atex	Alpha component of a texel
B	Blue color component
Cout	Output color
Cpix	Pixel color
Cr	Color stored in the color register CR
F	Fog factor
G	Green color component
Ltex	Luminance of a texel
M	Mix mode factor
R	Red color component
SB	Specular blue color component
SG	Specular green color component
SR	Specular red color component
TSARGBa	The register which stores the color component ARGB of vertex a
TSARGBb	The register which stores the color component ARGB of vertex b
TSARGBc	The register which stores the color component ARGB of vertex c
TSFSa	The register which stores the fog factor and specular color components of vertex a
TSFSb	The register which stores the fog factor and specular color components of vertex b
TSFSc	The register which stores the fog factor and specular color components of vertex c
TSUa	The register which stores the U coordinate of vertex a
TSUb	The register which stores the U coordinate of vertex b
TSUc	The register which stores the U coordinate of vertex c
TSVa	The register which stores the V coordinate of vertex a
TSVb	The register which stores the V coordinate of vertex b
TSVc	The register which stores the V coordinate of vertex c
TSWa	The register which stores the W perspective correction factor of vertex a
TSWb	The register which stores the W perspective correction factor of

	vertex b
TSWc	The register which stores the W perspective correction factor of vertex c
TSXa	The register which stores the X coordinate of vertex a
TSXb	The register which stores the X coordinate of vertex b
TSXc	The register which stores the X coordinate of vertex c
TSYa	The register which stores the Y coordinate of vertex a
TSYb	The register which stores the Y coordinate of vertex b
TSYc	The register which stores the Y coordinate of vertex c
TSZa	The register which stores the Z coordinate of vertex a
TSZb	The register which stores the Z coordinate of vertex b
TSZc	The register which stores the Z coordinate of vertex c
U	The X coordinate in a Texture
V	The Y coordinate in a Texture
W	Perspective correction factor
X	X coordinate
Y	Y coordinate
Z	Z coordinate
Z8	Z value, 8 bits representation
Z16	Z value, 16 bits representation

.2 3D Registers Summary

Vertex Parameter Registers

	Name	I/O Address	Triangle Drawing	Line Drawing	Point Drawing
1	TSFSa	8803h-8800h	√	√	√
2	TSZa	8807h-8804h	√	√	√
3	TSXa	880Bh-8808h	√	√	√
4	TSYa	880Fh-880Ch	√	√	√
5	TSARGBa	8813h-8810h	√	√	√
6	TSUa	8817h-8814h	√	√	√
7	TSVa	881Bh-8818h	√	√	√
8	TSWa	881Fh-881Ch	√	√	
9	TSFSb	8823h-8820h	√	√	
10	TSZb	8827h-8824h	√	√	
11	TSXb	882Bh-8828h	√	√	
12	TSYb	882Fh-882Ch	√	√	
13	TSARGBb	8833h-8830h	√	√	
14	TSUb	8837h-8834h	√	√	
15	TSVb	883Bh-8838h	√	√	
16	TSWb	883Fh-883Ch	√	√	
17	TSFSc	8843h-8840h	√		
18	TSZc	8847h-8844h	√		

19	TSXc	884Bh-8848h	√		
20	TSYc	884Fh-884Ch	√		
21	TSARGBc	8853h-8850h	√		
22	TSUc	8857h-8854h	√		
23	TSVc	885Bh-8858h	√		
24	TSWc	885Fh-885Ch	√		
25	Reserved	89F7h-8860h	√		

Primitive Setting Register

89FBh ~ 89F8h	D[31:24]	Reserved	
	D[23:21]	Reserved	
	D[20:18]	TSHMD	Shading Mode
	D[17:16]	TTFROM	Point, Start, or Top Vertex Come From
	D[15:14]	TMFROM	Middle Vertex Come From
	D[13:12]	TBFROM	End or Bottom Vertex Come From
	D[11:8]	TSETFIRE	Set 3D Engine Fire Position
	D[7]	TDRAWDIR	Drawing Direction
	D[6:3]	Reserved	
	D[2:0]	TDRAW	Drawing Primitive Command

Engine Fire & Status Register

89FFh ~ 89FCh	D[31:0]	TFIRE	Write for 3D Engine Fire
	D[31:0]	TSTATUS	Read for 3D Engine Status

Enable Setting Register

8A03h ~ 8A00h	D[31:24]	Reserved	
	D[23:22]	Reserved	
	D[21]	TenZW	Z Write Enable
	D[20]	TenZT	Z Test Enable
	D[19]	Reserved	
	D[18]	TenAW	Alpha Write Enable
	D[17]	TenAT	Alpha Test Enable
	D[16]	TenABUF	Alpha Buffer Enable
	D[15]	Reserved	
	D[14]	TenSTIP	Stipple Enable
	D[13]	TenSTIPA	Stipple Alpha Enable
	D[12]	TenLPT	Line Pattern Enable
	D[11]	TenPRSET	Primitive Setup Enable
	D[10]	TenTXMP	Texture Mapping Enable
	D[9]	TenTXPP	Texture Perspective Enable
	D[8]	TenTXTR	Texture Transparency Enable
	D[7]	TenCACHE	Enable Texture Cache

	D[6]	Reserved	
	D[5]	TenLCH	Enable Large Cache Size
	D[4]	TenSPEC	Specular Enable
	D[3]	TenFOG	Fog Enable
	D[2]	TenBLEND	Blending Enable
	D[1]	TenTRSP	Transparency Enable
	D[0]	TenDITH	Dither Enable

Z Setting Registers

8A07h ~ 8A04h	D[31:24]	Reserved	
	D[23:22]	Reserved	
	D[21:20]	TZBUFFM	Z-Buffer Data Format
	D[19]	Reserved	
	D[18:16]	TZTMD	Z-Test Mode
	D[15:14]	Reserved	
	D[13:0]	TZPIT	Z-Buffer Pitch
8A0Bh ~ 8A08h	D[31:0]	TZBAS	Z-Buffer Base Address

Alpha Setting Registers

8A0Fh ~ 8A0Ch	D[31:30]	Reserved	
	D[29:28]	TABUFFM	Alpha Buffer Data Format
	D[27]	Reserved	
	D[26:24]	TATMD	Alpha Test Mode
	D[23:16]	TAREF	Alpha Reference Value
	D[15:12]	Reserved	
	D[11:0]	TAPIT	Alpha Buffer Pitch
8A13h ~ 8A10h	D[31:0]	TABAS	Alpha Buffer Base Address

Destination Setting Registers

8A17h ~ 8A14h	D[31:28]	Reserved	
	D[27:24]	TROP	Raster Operation
	D[23]	Reserved	
	D[22:16]	TDSTCFM	Destination Color Format
	D[15:14]	Reserved	
	D[13:0]	TDSTPIT	Destination Color Surface Pitch
8A1Bh ~ 8A18h	D[31:0]	TDSTBAS	Destination Color Surface Base Address

Line Setting Register

8A1Fh ~ 8A1Ch	D[31:0]	TLPT	Line Pattern and Repeat Factor

Fog Setting Register

8A23h ~ 8A20h	D[31:25]	Reserved	
	D[24]	TFOGMD	Fog Mode
	D[23:0]	TFOGC	Fog Color Register

Miscellaneous Setting Registers

8A27h ~ 8A24h	D[31:24]	Reserved	
	D[23:0]	TTRSL	Transparency Color Range Low Value
8A2Bh ~ 8A28h	D[31:28]	TBLDST	Destination Blending Mode
	D[27:24]	TBLSRC	Source Blending Mode
	D[23:0]	TTRSH	Transparency Color Range High Value
8A2Fh ~ 8A2C	D[31:0]	Reserved	
8A33h ~ 8A30h	D[31:26]	Reserved	
	D[25:0]	TCLTB	Clipping Value for Top & Bottom
8A37h ~ 8A34h	D[31:26]	Reserved	
	D[25:0]	TCLLR	Clipping Value for Left & Right

Texture Setting Registers

8A3Bh ~ 8A38h	D[31:24]	TTXFM	Texel Format
	D[23:16]	TTXMPMD	Texture Mapping Mode
	D[15]	UVPOLAR	Set Sign or Un-sign Format of U,V
	D[14:12]	TTXBLMKB	Texture Blending Mask Bit Setting
	D[11:8]	TTXLV	Texture Level
	D[7:6]	Reserved	
	D[5]	TTXINSY	Texture Memory Located in System Memory
	D[4]	TTXCHCL	Clear Texture Cache
	D[3]	TTXFLMAX	Texture Magnified Filter Mode
	D[2:0]	TTXFLMIN	Texture Restrictional Filter Mode
8A3Fh ~ 8A3Ch	D[31:26]	TTXBLCMD	Texture Blending Color Mode Setting
	D[25:24]	TTXBLAMD	Texture Blending Alpha Mode Setting
	D[23:0]	TTXTRSL	Texture Transparency Color Range Low Value
8A43h ~ 8A40h	D[31:24]	Reserved	
	D[23:0]	TTXTRSH	Texture Transparency Color Range High Value
8A47h ~ 8A44h	D[31:0]	TTX0BAS	Texture Level 0 Base Address
8A4Bh ~ 8A48h	D[31:0]	TTX1BAS	Texture Level 1 Base Address
8A4Fh ~	D[31:0]	TTX2BAS	Texture Level 2 Base Address

8A4Ch			
8A53h ~ 8A50h	D[31:0]	TTX3BAS	Texture Level 3 Base Address
8A57h ~ 8A54h	D[31:0]	TTX4BAS	Texture Level 4 Base Address
8A5Bh ~ 8A58h	D[31:0]	TTX5BAS	Texture Level 5 Base Address
8A5Fh ~ 8A5Ch	D[31:0]	TTX6BAS	Texture Level 6 Base Address
8A63h ~ 8A60h	D[31:0]	TTX7BAS	Texture Level 7 Base Address
8A67h ~ 8A64h	D[31:0]	TTX8BAS	Texture Level 8 Base Address
8A6Bh ~ 8A68h	D[31:0]	TTX9BAS	Texture Level 9 Base Address
8A6Fh ~ 8A6Ch	D[31:27]	Reserved	
	D[26:16]	TTX0PCTL	Texture Level 0 Pitch
	D[15:11]	Reserved	
	D[10:0]	TTX1PCTL	Texture Level 1 Pitch
8A73h ~ 8A70h	D[31:27]	Reserved	
	D[26:16]	TTX2PCTL	Texture Level 2 Pitch
	D[15:11]	Reserved	
	D[10:0]	TTX3PCTL	Texture Level 3 Pitch
8A77h ~ 8A74h	D[31:27]	Reserved	
	D[26:16]	TTX4PCTL	Texture Level 4 Pitch
	D[15:11]	Reserved	
	D[10:0]	TTX5PCTL	Texture Level 5 Pitch
8A7Bh ~ 8A78h	D[31:27]	Reserved	
	D[26:16]	TTX6PCTL	Texture Level 6 Pitch
	D[15:11]	Reserved	
	D[10:0]	TTX7PCTL	Texture Level 7 Pitch
8A7Fh ~ 8A7Ch	D[31:27]	Reserved	
	D[26:16]	TTX8PCTL	Texture Level 8 Pitch
	D[15:11]	Reserved	
	D[10:0]	TTX9PCTL	Texture Level 9 Pitch
8A83h ~ 8A80h	D[31:28]	TTXW	Width of Texture Level 0
	D[27:24]	TTXH	Height of Texture Level 0
	D[23:0]	TTXCB	Texture Color Base Register for Mix Mode
8A87h ~ 8A84h	D[31:24]	Reserved	
	D[23:0]	TTXC0	Texture Color Register 0 for Mix Mode
8A8Bh ~ 8A88h	D[31:24]	Reserved	
	D[23:0]	TTXC1	Texture Color Register 1 for Mix Mode
8A8Fh ~ 8A8Ch	D[31:0]	Reserved	
	D[23:0]	TTXCR	Texture Color Register for Luminance

8A93h ~ 8A90h	D[31:0]	TTXCTB	Texture Border Color Register
8AD3h ~ 8A94h	D[31:0] x 16	TTXIDX15 ~ TTXIDX0	Texture Index Palette Register 0 ~ Texture Index Palette Register 15

Index Format
Index4: Use TTXIDX15 - TTXIDX0
Index2: Use TTXIDX3 - TTXIDX0
Index1: Use TTXIDX1 - TTXIDX0

Reserved Registers

8AFEh ~ 8AD4h		Reserved	

End of Primitive Setting Register

8AFFh	D[7:0]	TEND	End of Primitive List

Stipple Setting Registers

8B7Fh ~ 8B00h	D[31:0] x 32	T0STIP ~ T31STIP	Stipple Pattern 0 ~ Stipple Pattern 31

.3 Vertex Parameter Registers

Fog & Specular Color Components of Vertex a

Register Type: Read/Write
Read/Write Port: 8803h ~ 8800h
Default: xx xx xx xxh

D[31:24] TSFSa (i) ➡➡ fog factor of vertex a
D[23:16] TSSRa (i) ➡➡ specular red color of vertex a
D[15:8] TSSGa (i) ➡➡ specular green color of vertex a
D[7:0] TSSBa (i) ➡➡ specular blue color of vertex a

Z Coordinate of Vertex a

Register Type: Read/Write
Read/Write Port: 8807h ~ 8804h
Default: xx xx xx xxh

D[31:0] TSZa (f) ➡➡ Z of vertex a

X Coordinate of Vertex a

Register Type: Read/Write
Read/Write Port: 880Bh ~ 8808h
Default: xx xx xx xxh

D[31:0] TSXa (f) ➡➡ X of vertex a

Y Coordinate of Vertex a

Register Type: Read/Write
Read/Write Port: 880Fh ~ 880Ch
Default: xx xx xx xxh

D[31:0] TSYa (f) ➡➡ Y of vertex a

Color Component ARGB of Vertex a

Register Type: Read/Write
Read/Write Port: 8813h ~ 8810h
Default: xx xx xx xxh

D[31:24] TSAa (i) ➡➡ A of vertex a
D[23:16] TSRa (i) ➡➡ R of vertex a
D[15:8] TSGa (i) ➡➡ G of vertex a
D[7:0] TSBa (i) ➡➡ B of vertex a

X Coordinate in a Texture of Vertex a

Register Type: Read/Write
Read/Write Port: 8817h ~ 8814h
Default: xx xx xx xxh

D[31:0] TSUa (f) ➡➡ U of vertex a

Y Coordinate in a Texture of Vertex a

Register Type: Read/Write
Read/Write Port: 881Bh ~ 8818h
Default: xx xx xx xxh

D[31:0] TSVa (f) ➡➡ V of vertex a

Perspective Correction Factor in a Texture of Vertex a

Register Type: Read/Write
Read/Write Port: 881Fh ~ 881Ch
Default: xx xx xx xxh

D[31:0] TSWa (f) ➡➡ W of vertex a

Fog & Specular Color Components of Vertex b

Register Type: Read/Write
Read/Write Port: 8823h ~ 8820h
Default: xx xx xx xxh

D[31:24] TSFSb (i) ➡➡ fog factor of vertex b
D[23:16] TSSRb (i) ➡➡ specular red color of vertex b
D[15:8] TSSGb (i) ➡➡ specular green color of vertex b
D[7:0] TSSBb (i) ➡➡ specular blue color of vertex b

Z Coordinate of Vertex b

Register Type: Read/Write
Read/Write Port: 8827h ~ 8824h
Default: xx xx xx xxh

D[31:0] TSZb (f) ➡➡ Z of vertex b

X Coordinate of Vertex b

Register Type: Read/Write
Read/Write Port: 882Bh ~ 8828h
Default: xx xx xx xxh

D[31:0] TSXb (f) ➡➡ X of vertex b

Y Coordinate of Vertex b

Register Type: Read/Write
Read/Write Port: 882Fh ~ 882Ch
Default: xx xx xx xxh

D[31:0] TSYb (f) ➡➡ Y of vertex b

Color Component ARGB of Vertex b

Register Type: Read/Write
Read/Write Port: 8833h ~ 8830h
Default: xx xx xx xxh

D[31:24] TSAb (i) ➡➡ A of vertex b
D[23:16] TSRb (i) ➡➡ R of vertex b
D[15:8] TSGb (i) ➡➡ G of vertex b
D[7:0] TSBb (i) ➡➡ B of vertex b

X Coordinate in a Texture of Vertex b

Register Type: Read/Write
Read/Write Port: 8837h ~ 8834h
Default: xx xx xx xxh

D[31:0] TSUb (f) ➡➡ U of vertex b

Y Coordinate in a Texture of Vertex c

Register Type: Read/Write
Read/Write Port: 883Bh ~ 8838h
Default: xx xx xx xxh

D[31:0] TSVb (f) ➡➡ V of vertex b

Perspective Correction Factor in a Texture of Vertex b

Register Type: Read/Write
Read/Write Port: 883Fh ~ 883Ch
Default: xx xx xx xxh

D[31:0] TSWb (f) ➡➡ W of vertex b

Fog & Specular Color Components of Vertex c

Register Type: Read/Write
Read/Write Port: 8843h ~ 8840h
Default: xx xx xx xxh

D[31:24] TSFSc (i) ➡➡ fog factor of vertex c
D[23:16] TSSRc (i) ➡➡ specular red color of vertex c
D[15:8] TSSGc (i) ➡➡ specular green color of vertex c

D[7:0] TSSBc (i) ➡➡ specular blue color of vertex c

Z Coordinate of Vertex c

Register Type: Read/Write
Read/Write Port: 8847h ~ 8844h
Default: xx xx xx xxh

D[31:0] TSZc (f) ➡➡ Z of vertex c

X Coordinate of Vertex c

Register Type: Read/Write
Read/Write Port: 884Bh ~ 8848h
Default: xx xx xx xxh

D[31:0] TSXc (f) ➡➡ X of vertex c

Y Coordinate of Vertex c

Register Type: Read/Write
Read/Write Port: 884Fh ~ 884Ch
Default: xx xx xx xxh

D[31:0] TSYc (f) ➡➡ Y of vertex c

Color Component ARGB of Vertex c

Register Type: Read/Write
Read/Write Port: 8853h ~ 8850h
Default: xx xx xx xxh

D[31:24] TSAc (i) ➡➡ A of vertex c
D[23:16] TSRc (i) ➡➡ R of vertex c
D[15:8] TSGc (i) ➡➡ G of vertex c
D[7:0] TSBc (i) ➡➡ B of vertex c

X Coordinate in a Texture of Vertex c

Register Type: Read/Write
Read/Write Port: 8857h ~ 8854h
Default: xx xx xx xxh

D[31:0] TSUc (f) ➡➡ U of vertex c

Y Coordinate in a Texture of Vertex c

Register Type: Read/Write
Read/Write Port: 885Bh ~ 8858h
Default: xx xx xx xxh

D[31:0] TSVc (f) ➡➡ V of vertex c

Perspective Correction Factor in a Texture of Vertex c

Register Type: Read/Write
Read/Write Port: 885Fh ~ 885Ch
Default: xx xx xx xxh

D[31:0] TSWc (f) ➡➡ W of vertex c

Reserved Registers

Register Type: Read/Write
Read/Write Port: 89F7h ~ 8860h
Default: xx xx xx xxh

D[31:0] Reserved

.4 Primitive Setting Registers

Register Type: Read/Write
Read/Write Port: 89FBh ~ 89F8h
Default: xx xx xx xxh

D[31:24] Reserved
D[23:21] Reserved

D[20:18] TSHMD ➡➡ Shading Mode
For triangle shading,
000: Reserved
001: FLAT_SHADING via top vertex
010: FLAT_SHADING via middle vertex
011: FLAT_SHADING via bottom vertex
100: SMOOTH_SHADING via GOURAUD_SHADING
111 ~ 101: Reserved
For line shading,
000: Reserved
001: FLAT_SHADING via start vertex
010: Reserved
011: FLAT_SHADING via end vertex
100: SMOOTH_SHADING via GOURAUD_SHADING
111 ~ 101: Reserved

D[17:16] TTFROM ➡➡ top vertex come from
For triangle,
00: top vertex come from vertex a
01: top vertex come from vertex b
10: top vertex come from vertex c
11: reserved
For line,
00: start vertex come from vertex a
01: start vertex come from vertex b
10: start vertex come from vertex c
11: reserved
For point,
00: vertex come from vertex a
01: vertex come from vertex b
10: vertex come from vertex c
11: reserved

D[15:14] TMFROM ➡➡ middle vertex come from
For triangle,

00: middle vertex come from vertex a
01: middle vertex come from vertex b
10: middle vertex come from vertex c
11: reserved

D[13:12] TBFROM ➡➡ bottom vertex come from
For triangle,
00: bottom vertex come from vertex a
01: bottom vertex come from vertex b
10: bottom vertex come from vertex c
11: reserved
For line,
00: end vertex come from vertex a
01: end vertex come from vertex b
10: end vertex come from vertex c
11: reserved

D[11:8] TSETFIRE ➡➡ Set 3D Engine Fire Position
0000: 3D Engine fired right after the write of TFIRE
0001: 3D Engine fired right after the write of TSARGBa
0010: 3D Engine fired right after the write of TSWa
0011: 3D Engine fired right after the write of TSARGBb
0100: 3D Engine fired right after the write of TSWb
0101: 3D Engine fired right after the write of TSARGBc
0110: 3D Engine fired right after the writE of TSWc
0111: 3D Engine fired right after the write of TSVc
1000-1111: Reserved

D7 TDRAWDIR ➡➡ Drawing Direction
For triangle drawing,
0: left to right
1: right to left
For line drawing,
0: horizontal
1: vertical

D[6:3] Reserved

D[2:0] TDRAW ➡➡ Drawing Primitive Command
000: Draw a Point
001: Draw a Line
010: Draw a Triangle
011-111: Reserved

.5 Engine Fire & Status Register

Register Type: Read/Write
Read/Write Port: 89FFh ~ 89FCh
Default: xx xx xx xxh

For write operation,

D[31:0]	TFIRE ➡➡ Write to Fire 3D Engine

For read operation,

D[31:0]	TSTATUS ➡➡ Read for 3D Engine Status as follow:
D[27:16]	Available 3D Queue Length 3D Queue Length = D[27:16] * 8 Bytes
D[15:2]	Reserved
D1	T3IDLEQE ➡➡ 3D Engine Idle & 3D Queue Empty 0: 3D Engine Busy or 3D Queue not Empty 1: 3D Engine Idle and 3D Queue Empty
D0	T3IDLE ➡➡ 3D Engine Idle 0: 3D Engine Busy 1: 3D Engine Idle

.6 Enable Setting Register

Register Type: Read/Write
Read/Write Port: 8A03h ~ 8A00h
Default: all 00h

D[31:22]	Reserved
D21	TenZW ➡➡ Z Write Enable 0: Z Write Disable 1: Z Write Enable
D20	TenZT ➡➡ Z Test Enable 0: Z Test Disable 1: Z Test Enable
D19	Reserved
D18	TenAW ➡➡ Alpha Write Enable 0: Alpha Write Disable 1: Alpha Write Enable
D17	TenAT ➡➡ Alpha Test Enable 0: Alpha Test Disable 1: Alpha Test Enable
D16	TenABUF ➡➡ Alpha Buffer Enable 0: Alpha Buffer Disable 1: Alpha Buffer Enable
D15	Reserved
D[14:13]	TenSTIP, TenSTIPA ➡➡ Stipple Enable, Stipple Alpha Enable 0x: Stipple Disable 10: Stipple Enable, Stipple Alpha Disable 11: Stipple Enable, Stipple Alpha Enable
D12	TenLPT ➡➡ Line Pattern Enable 0: Line Pattern Disable 1: Line Pattern Enable
D11	TenPRSET ➡➡ Primitive Setup Enable

0: Primitive Setup Disable
1: Primitive Setup Enable

D10 TenTXMP ➡➡ Texture Mapping Enable
0: Texture Mapping Disable
1: Texture Mapping Enable

D9 TenTXPP ➡➡ Texture Perspective Correction Enable
0: Texture Perspective Correction Disable
1: Texture Perspective Correction Enable

D8 TenTXTR ➡➡ Texture Transparency Enable
0: Texture Transparency Disable
1: Texture Transparency Enable

D7 TenCACHE ➡➡ Enable Texture Cache
0: Texture Cache Disable
1: Texture Cache Enable

D6 Reserved

D5 TenLCH ➡➡ Enable Large Cache Size
0: Small Cache Size
1: Large Cache Size

D4 TenSPEC ➡➡ Specular Enable
0: Specular Disable
1: Specular Enable

D3 TenFOG ➡➡ Fog Enable
0: Fog Disable
1: Fog Enable

D2 TenBLEND ➡➡ Blending Enable
0: Blending Disable
1: Blending Enable

D1 TenTRSP ➡➡ Transparency Enable
0: Transparency Disable
1: Transparency Enable

D0 TenDITH ➡➡ Dither Enable
0: Dither Disable
1: Dither Enable

.7 Z Setting Registers

Z Setting Register 1

Register Type: Read/Write
Read/Write Port: 8A07h ~ 8A04h
Default: xx xx xx xxh

D[31:24] Reserved
D[23:22] Reserved
D[21:20] TZBUFFM ➡➡ Z Buffer Format
00: Z8
01: Z16
1x: Reserved

D19 Reserved
D[18:16] TZTMD ➡➡ Z Test Mode
000: Z test never pass
001: Pass if Znew < Zdst
010: Pass if Znew = Zdst
011: Pass if Znew ≤ Zdst
100: Pass if Znew > Zdst
101: Pass if Znew ≠ Zdst
110: Pass if Znew ≥ Zdst
111: Z test always pass
D[15:14] Reserved
D[13:0] TZPIT ➡➡ Z Buffer Pitch
Addr13 ~ Addr0

Z Setting Register 2

Register Type: Read/Write
Read/Write Port: 8A0Bh ~ 8A08h
Default: xx xx xx xxh

D[31:0] TZBAS ➡➡ Z Buffer Base Address

If Z Buffer is located in system memory,
D[31:0] Addr31 ~ Addr0

If Z Buffer is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

.8 Alpha Setting Registers

Alpha Setting Register 1

Register Type: Read/Write
Read/Write Port: 8A0Fh ~ 8A0Ch
Default: xx xx xx xxh

D[31:30] Reserved
D[29:28] TABUFFM ➡➡ Alpha Buffer Color Format
00 ~ 10: Reserved
11: A8 (alpha component, 8-bit integer representation)
D27 Reserved
D[26:24] TATMD ➡➡ Alpha Test Mode
000: Alpha test never pass
001: Pass if Anew < Aref
010: Pass if Anew = Aref
011: Pass if Anew ≤ Aref
100: Pass if Anew > Aref
101: Pass if Anew ≠ Aref
110: Pass if Anew ≥ Aref
111: Alpha test always pass

D[23:16] TAREF ➡➡ Alpha Reference Value
A8 format (alpha component, 8-bit integer representation)
D[15:12] Reserved
D[11:0] TAPIT ➡➡ Alpha Buffer Pitch
Addr11 ~ Addr0

Alpha Setting Register 2

Register Type: Read/Write
Read/Write Port: 8A13h ~ 8A10h
Default: xx xx xx xxh

D[31:0] TABAS ➡➡ Alpha Buffer Base Address

If Alpha Buffer is located in system memory,
D[31:0] Addr31 ~ Addr0

If Alpha Buffer is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

.9 Destination Setting Registers

Destination Setting Register 1

Register Type: Read/Write
Read/Write Port: 8A17h ~ 8A14h
Default: xx xx xx xxh

D[31:28] Reserved

D[27:24] TROP ➡➡ Raster Operation

0000:	BLACK	0
0001:	NOT_MERGE_PEN	DPon
0010:	MASK_NOT_PEN	DPna
0011:	NOT_COPY_PEN	Pn
0100:	MASK_PEN_NOT	PDna
0101:	NOT	Dn
0110:	XOR_PEN	DPx
0111:	NOT_MASK_PEN	DPan
1000:	MASK_PEN	DPa
1001:	NOT_XOR_PEN	DPxn
1010:	NOP	D
1011:	MERGE_NOT_PEN	DPno
1100:	COPY_PEN	P
1101:	MERGE_PEN_NOT	PDno
1110:	MERGE_PEN	DPo
1111:	WHITE	1

D23 Reserved

D[22:16] TDSTCFM ➡➡ Destination Color Format
D22 0: RGB ordering in RGB format

1: BGR ordering in RGB format

D[21:20] 00: Index format or RGB_8bpp format
01: RGB_16bpp format
10: RGB_24bpp format
11: RGB_32bpp format

For D[22] = 0,

D[19:16] For D[21:20] = 01 (RGB_16bpp format),

0000: RGB555, xRRR RRGG GGGB BBBB
0001: RGB565, RRRR RGGG GGGB BBBB
0010: ARGB1555, ARRR RRGG GGGB BBBB
0011: ARGB4444, AAAA RRRR GGGG BBBB

For D[21:20] = 11 (RGB_32bpp format),

0000: ARGB1888 Axxx xxxx RRRR RRRR GGGG GGGG BBBB BBBB
0001: ARGB2888 AAxx xxxx RRRR RRRR GGGG GGGG BBBB BBBB
0010: ARGB4888 AAAA xxxx RRRR RRRR GGGG GGGG BBBB BBBB
0011: ARGB8888 AAAA AAAA RRRR RRRR GGGG GGGG BBBB BBBB
0100: RGB0888 xxxx xxxx RRRR RRRR GGGG GGGG BBBB BBBB

Others: Reserved

For D[22] = 1,

D[19:16] For D[21:20] = 01 (RGB_16bpp format)

0000: BGR555 xBBB BBGG GGGR RRRR
0001: BGR565 BBBB BGGG GGGR RRRR
0010: ABGR1555 ABBB BBGG GGGR RRRR
0011: ABGR4444 AAAA BBBB GGGG RRRR

For D[21:20] = 11 (RGB_32bpp format),

0000: ABGR1888 Axxx xxxx BBBB BBBB GGGG GGGG RRRR RRRR
0001: ABGR2888 AAxx xxxx BBBB BBBB GGGG GGGG RRRR RRRR
0010: ABGR4888 AAAA xxxx BBBB BBBB GGGG GGGG RRRR RRRR
0011: ABGR8888 AAAA AAAA BBBB BBBB GGGG GGGG RRRR RRRR
0100: BGR0888 xxxx xxxx BBBB BBBB GGGG GGGG RRRR RRRR

Others: Reserved

D[15:14] Reserved

D[13:0] TDSTPIT ➡➡ Destination Pitch
Addr13 ~ Addr0

Destination Setting Register 2

Register Type: Read/Write
Read/Write Port: 8A1Bh ~ 8A18h
Default: xx xx xx xxh

D[31:0] TDSTBAS ➡➡ Destination Base Address

If Destination Surface is located in system memory,
D[31:0] Addr31 ~ Addr0

If Destination Surface is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

.10 Line Setting Register

Register Type: Read/Write
Read/Write Port: 8A1Fh ~ 8A1Ch
Default: xx xx xx xxh

D[31:16] TLPT ➡➡ Line pattern
D[15:0] TLPTNRP (i) ➡➡ Repeat factor of Line Pattern

.11 Fog Setting Register

Register Type: Read/Write
Read/Write Port: 8A23h ~ 8A20h
Default: xx xx xx xxh

D[31:25] Reserved
D24 TFOGMD ➡➡ Fog Mode
0: Constant Fog Mode
1: Normal Fog Mode
D[23:0] TFOGC ➡➡ Color Register of Fog
D[23:16] = TGFR (i) ➡➡ Fog Color R
D[15:8] = TGFG (i) ➡➡ Fog Color G
D[7:0] = TGFB (i) ➡➡ Fog Color B

.12 Miscellaneous Setting Registers

Miscellaneous Setting Register 1

Register Type: Read/Write
Read/Write Port: 8A27h ~ 8A24h
Default: xx xx xx xxh

D[31:27] Reserved
D[23:16] TTRSLR (i) ➡➡ R of Transparency Color Low Range
D[15:8] TTRSLG (i) ➡➡ G of Transparency Color Low Range
D[7:0] TTRSLB (i) ➡➡ B of Transparency Color Low Range

Miscellaneous Setting Register 2

Register Type: Read/Write

Read/Write Port: 8A2Bh ~ 8A28h
Default: xx xx xx xxh

D[31:28] TBLDST ➡➡ Destination Blending Mode
0000: BLEND_ZERO
Blend factor is (0, 0, 0, 0) for (A,R,G,B)
0001: BLEND_ONE
Blend factor is (1, 1, 1, 1) for (A,R,G,B)
0010: BLEND_SRC_COLOR
Blend factor is [R(s),G(s),B(s),A(s)]
0011: BLEND_INV_SRC_COLOR
Blend factor is [1-R(s),1-G(s),1-B(s),1-A(s)]
0100: BLEND_SRC_ALPHA
Blend factor is [A(s),A(s),A(s),A(s)]
0101: BLEND_INV_SRC_ALPHA
Blend factor is [1-A(s),1-A(s),1-A(s), 1-A(s)]
0110: BLEND_DST_ALPHA
Blend factor is [A(d),A(d),A(d),A(d)]
0111: BLEND_INV_DST_ALPHA
Blend factor is [1-A(d),1-A(d),1-A(d)]
1111 ~ 1000: Reserved

D[27:24] TBLSRC ➡➡ Source Blending Mode
0000: BLEND_ZERO
Blend factor is (0, 0, 0, 0)
0001: BLEND_ONE
Blend factor is (1, 1, 1, 1)
0010-0011: Reserved
0100: BLEND_SRC_ALPHA
Blend factor is [A(s), A(s), A(s), A(s)]
0101: BLEND_INV_SRC_ALPHA
Blend factor is [1-A(s), 1-A(s), 1-A(s), 1-A(s)]
0110: BLEND_DST_ALPHA
Blend factor is [A(d), A(d), A(d), A(d)]
0111: BLEND_INV_DST_ALPHA
Blend factor is [1-A(d), 1-A(d), 1-A(d)]
1000: BLEND_DST_COLOR
Blend factor is [R(d), G(d), B(d), A(d)]
1001: BLEND_INV_DST_COLOR
Blend factor is [1-R(d), 1-G(d), 1-B(d), 1-A(d)]
1010: BLEND_SRC_ALPHA_SAT
Blend factor is (f, f, f, 1); f = min[A(s), 1-A(d)]
1011: BLEND_BOTH_SRC_ALPHA
Source blend factor is [A(s), A(s), A(s), A(s)]
Destination blend factor is [1-A(s), 1-A(s), 1-A(s), 1-A(s)]
1100: BLEND_BOTH_INV_SRC_ALPHA
Source blend factor is [1-A(s), 1-A(s), 1-A(s), 1-A(s)]
Destination blend factor is [A(s), A(s), A(s), A(s)]

1111-1101: Reserved

D[23:16] TTRSHR (i) ➡➡ R of Transparency Color High Range
D[15:8] TTRSHG (i) ➡➡ G of Transparency Color High Range
D[7:0] TTRSHB (i) ➡➡ B of Transparency Color High Range

Miscellaneous Setting Register 3

Register Type: Read/Write
Read/Write Port: 8A2Fh ~ 8A2Ch
Default: xx xx xx xxh

D[31:0] Reserved

Miscellaneous Setting Register 4

Register Type: Read/Write
Read/Write Port: 8A33h ~ 8A30h
Default: xx xx xx xxh

D[31:26] Reserved
D[25:13] TCLTOP (s12) ➡➡ Top Clipping Value
D[12:0] TCLBOT (s12) ➡➡ Bottom Clipping Value

Miscellaneous Setting Register 5

Register Type: Read/Write
Read/Write Port: 8A37h ~ 8A34h
Default: xx xx xx xxh

D[31:26] Reserved
D[25:13] TCLLEFT (s12) ➡➡ Left Clipping Value
D[12:0] TCLRGT (s12) ➡➡ Right Clipping Value

.13 Texture Setting Registers

Texture Setting Register 1

Register Type: Read/Write
Read/Write Port: 8A3Bh ~ 8A38h
Default: xxh, xxh, x0000000b, 00h

D[31:24] TTXFM ➡➡ Texel Format
D31 RGB ordering
0: RGB ordering in RGB format
1: BGR ordering in RGB format
D[30:28] format
000: Palette Index format
001: Mix format
010: YUV format
011: Luminance format
100: RGB_8bpp or BGR_8bpp format
101: RGB_16bpp or BGR_8bpp format
110: RGB_24bpp or BGR_24bpp format
111: RGB_32bpp or BGR_32bpp format

(Color ordering is shown from MSB to LSB)

For D[31:28] = 0000 (RGB ordering & palette index format),

D[27:24]
- 0000: Index1
  Use TTXIDX0, 1
- 0001: Index2
  Use TTXIDX0, 1, 2, 3
- 0010: Index4
  Use TTXIDX0-15

For D[31:28] = 0001 (RGB ordering & mix format),

D[27:24]
- 0000: M4
  MMMM
- 0110: AM44
  AAAA MMMM

For D[31:28] = 0010 (RGB ordering & YUV format),

D[27:24]
- 0000: YUV422
  $Y_1Y_1Y_1Y_1$ $Y_1Y_1Y_1Y_1$ CuCuCuCu CuCuCuCu $Y_0Y_0Y_0Y_0$ $Y_0Y_0Y_0Y_0$
  CvCvCvCv CvCvCvCv
- 0001: YVU422
  $Y_1Y_1Y_1Y_1$ $Y_1Y_1Y_1Y_1$ CvCvCvCv CvCvCvCv $Y_0Y_0Y_0Y_0$ $Y_0Y_0Y_0Y_0$
  CuCuCuCu CuCuCuCu
- 0010: UVY422
  CuCuCuCu CuCuCuCu $Y_1Y_1Y_1Y_1$ $Y_1Y_1Y_1Y_1$
  CvCvCvCvCvCvCvCv $Y_0Y_0Y_0Y_0Y_0$ $Y_0Y_0Y_0$
- 0011: VUY422
  CvCvCvCv CvCvCvCv $Y_1Y_1Y_1Y_1$ $Y_1Y_1Y_1Y_1$
  CuCuCuCuCuCuCuCu $Y_0Y_0Y_0Y_0Y_0Y_0Y_0Y_0$

For D[31:28] = 0011 (RGB ordering & luminance format),

D[27:24]
- 0000: L1
  L
- 0001: L2
  LL
- 0010: L4
  LLLL
- 0011: L8
  LLLL LLLL
- 0101: AL22
  AALL
- 1000: AL44
  AAAA LLLL
- 1100: AL88
  AAAA AAAA LLLL LLLL

For D[31:28] = 0100 (ARGB 8bpp format),

D[27:24]
- 0000: RGB332
  RRRG GGBB
- 0001: RGB233
  RRGG GBBB
- 0010: RGB232

xRRG GGBB
0011: ARGB1232
ARRG GGBB

For D[31:28] = 0101 (ARGB 16bpp format),

D[27:24]
0000: RGB555
xRRR RRGG GGGB BBBB
0001: RGB565
RRRR RGGG GGGB BBBB
0010: ARGB1555
ARRR RRGG GGGB BBBB
0011: ARGB4444
AAAA RRRR GGGG BBBB
0111: ARGB8332
AAAA AAAA RRRG GGBB
1011: ARGB8233
AAAA AAAA RRGG GBBB
1111: ARGB8232
AAAA AAAA xRRG GGBB

For D[31:28] = 0110 (ARGB 24bpp format),

D[27:24]
0011: ARGB8565
AAAA AAAA RRRR RGGG GGGB BBBB
0111: ARGB8555
AAAA AAAA xRRR RRGG GGGB BBBB
1000: RGB888
RRRR RRRR GGGG GGGG BBBB BBBB

For D[31:28] = 0111 (ARGB 32bpp format),

D[27:24]
0011: ARGB8888
AAAA AAAA RRRR RRRR GGGG GGGG BBBB BBBB
0100: ARGB0888
xxxx xxxx RRRR RRRR GGGG GGGG BBBB BBBB

For D[31:28] = 1100 (ABGR 8bpp format),

D[27:24]
0000: BGR332
BBBG GGRR
0001: BGR233
BBGG GRRR
0010: BGR232
xBBG GGRR
0011: ABGR1232
ABBG GGRR

For D[31:28] = 1101 (ABGR 16bpp format),

D[27:24]
0000: BGR555
xBBB BBGG GGGR RRRR
0001: BGR565
BBBB BGGG GGGR RRRR
0010: ABGR1555
ABBB BBGG GGGR RRRR
0011: ABGR4444

AAAA BBBB GGGG RRRR
0111: ABGR8332
AAAA AAAA BBBG GGRR
1011: ABGR8233
AAAA AAAA BBGG GRRR
1111: ABGR8232
AAAA AAAA xBBG GGRR

For D[31:28] = 1110 (ABGR 24bpp format),

D[27:24] 0011: ABGR8565
AAAA AAAA BBBB BGGG GGGR RRRR
0111: ABGR8555
AAAA AAAA xRRR RRGG GGGB RRRR
1000: BGR888
BBBB BBBB GGGG GGGG RRRR RRRR

For D[31:28] = 1111 (ABGR 32bpp format),

D[27:24] 0011: ABGR8888
AAAA AAAA BBBB BBBB GGGG GGGG RRRR RRRR
0100: ABGR0888
xxxx xxxx BBBB BBBB GGGG GGGG RRRR RRRR
Others: Reserved

D[23:16] TTXMPMD ➡➡ Texture Mapping Mode
(Priority: wrap > mirror > clamp)
xx xxxx00: Wrap Disable
xx xx00xx: Mirror Disable
xx 00xxxx: Clamp Disable
xx xxxxx1: Wrap along U axis
xx xxxx1x: Wrap along V axis
xx xxx1x0: Mirror along U axis
xx xx1x0x: Mirror along V axis
xx x1x0x0: Clamp along U axis
xx 1x0x0x: Clamp along V axis
x0 xxxxxx: Do not use Border Color (CTB) for smoothing
x1 xxxxxx: Use CTB for smoothing
0x xxxxxx: Do not use CTB if out of texture area
1x xxxxxx: Use CTB if out of texture area

D15 UVPOLAR ➡➡ Set Sign or Un-sign Format of Cu, Cv
0: Cu and Cv are un-sign representation
1: Cu and Cv are Sign magnitude representation

D[14:2] TTXBLMKB ➡➡ Texture Blending Mask Bit Setting
000: Bit n = Bit 0 of Atex
001: Bit n = Bit 1 of Atex
010: Bit n = Bit 2 of Atex
011: Bit n = Bit 3 of Atex
100: Bit n = Bit 4 of Atex
101: Bit n = Bit 5 of Atex
110: Bit n = Bit 6 of Atex

111: Bit n = Bit 7 of Atex

D[11:8] TTXLV ➡➡ Texture Level
0000: Single Texture Structure
1001 ~ 0001: MIP structure
This number must small than or equal to
max {TTXW, TTXH}.
1111 ~ 1010: Reserved

D[7:6] Reserved

D5 TTXINSY ➡➡ Texture Memory Located in System Memory
0: Texture Memory is located in local frame buffer
1: Texture Memory is located in system memory

D4 TTXCHCL ➡➡ Clear Texture Cache
0: Let Texture Cache Work Normally
1: Clear Data in Texture Cache

D3 TTXFLMAX ➡➡ Texture filter mode when a texture is magnified
0: Nearest
1: Linear

D[2:0] TTXFLMIN ➡➡ Texture filter mode when a texture is restricted
000: NEAREST
001: LINEAR
010: NEAREST_MIP_NEAREST
011: NEAREST_MIP_LINEAR
100: LINEAR_MIP_NEAREST
101: LINEAR_MIP_LINEAR
11x: Reserved

Texture Setting Register 2

Register Type: Read/Write
Read/Write Port: 8A3Fh ~ 8A3Ch
Default: xx xx xx xxh

D[31:26] TTXBLCMD ➡➡ Texture Blending Color Mode Setting
For ARGB format,
00 0000: Cout = Ctex
00 0001: Cout = Cpix
00 0010: Cout = Cpix Ctex
00 0011: Cout = Cpix Ctex
00 0100: Cout = (1 - Atex) Cpix + Atex Ctex
00 0101: Reserved
00 0110: Cout = (1 - Apix) Ctex + Apix Cpix
00 0111: Cout = (1 - Apix) Ctex + Apix Cpix
00 1000: Cout = Ctex, if Bit n of Atex = 1,
Cout = Cpix, if Bit n of Atex = 0
00 1001: Cout = Ctex , if Bit n of Atex = 1,
Cout = Cpix, if Bit n of Atex = 0
00 101x: Reserved
00 1100: Cout = Cpix Ctex, if Bit n of Atex = 1,
Cout = Cpix , if Bit n of Atex = 0

00 1101: Cout = Cpix Ctex, if Bit n of Atex = 1,
Cout = Cpix, if Bit n of Atex = 0
00 1110: Cout = Cpix Ctex, if Bit n of Atex = 1,
Cout = Cpix, if Bit n of Atex = 0
0 1111: Reserved
01 xxxx: Reserved
1x xxxx: Reserved

For RGB format,
00 0000: Cout = Ctex
00 0001: Cout = Cpix
00 0010: Cout = Cpix Ctex
00 0011: Cout = Cpix Ctex
00 0100: Cout = Ctex
00 0101: Reserved
00 0110: Cout = Cpix
00 0111: Cout = Cpix
00 1000: Cout = Ctex
00 1001: Cout = Cpix
00 101x: Reserved
00 1100: Cout = Cpix Ctex
00 1101: Cout = Cpix
00 1110: Cout = Cpix Ctex
00 1111: Reserved
01 xxxx: Reserved
1x xxxx: Reserved

For AL format,
00 0000: Cout = Ltex Cr
00 0001: Cout = Cpix
00 0010: Cout = Ltex Cpix
00 0011: Cout = Ltex Cr Cpix
00 0100: Cout = (1 - Ltex) Cpix + Ltex Cr
00 0101: Reserved
00 0110: Cout = (1- Apix) Cr + Apix Cpix
00 0111: Cout = (1- Apix) Ltex Cr + Apix Cpix
00 1000: Cout = Ltex Cr, if Bit n of Atex = 1
Cout = Cpix, if Bit n of Atex = 0
00 1001: Cout = Ltex Cr, if Bit n of Atex = 1
Cout = Cpix, if Bit n of Atex = 0
00 101x: Reserved
00 1100: Cout = Ltex Cpix, if Bit n of Atex = 1
Cout = Cpix, if Bit n of Atex = 0
00 1101: Cout = Ltex Cpix, if Bit n of Atex = 1
Cout = Cpix, if Bit n of Atex = 0
00 1110: Cout = Ltex Cr Cpix, if Bit n of Atex = 1
Cout = Cpix, if Bit n of Atex = 0
00 1111: Reserved

01 xxxx: Reserved
1x xxxx: Reserved

For L format,
00 0000: Cout = Ltex Cr
00 0001: Cout = Cpix
00 0010: Cout = Ltex Cpix
00 0011: Cout = Ltex Cr Cpix
00 0100: Cout = Ltex Cr
00 0101: Reserved
00 0110: Cout = Cpix
00 0111: Cout = Cpix
00 1000: Cout = Ltex Cr
00 1001: Cout = Cpix
00 101x: Reserved
00 1100: Cout = Ltex Cpix
00 1101: Cout = Cpix
00 1110: Cout = Ltex Cr Cpix
00 1111: Reserved
01 xxxx: Reserved
1x xxxx: Reserved

D[25:24] TTXBLAMD ➡➡ Texture Blending Alpha Mode Setting
00: Aout = Atex, for ARGB, AL texture format
Aout = Apix, for RGB, L texture format
01: Aout = Apix
10: Aout = Apix Atex, for ARGB, AL texture format
Aout = Apix, for RGB, L texture format
11: Reserved

D[23:16] TTXTRSLR (i) ➡➡ R of Texture Transparency Color Low Range
D[15:8] TTXTRSLG (i) ➡➡ G of Texture Transparency Color Low Range
D[7:0] TTXTRSLB (i) ➡➡ B of Texture Transparency Color Low Range

Texture Setting Register 3

Register Type: Read/Write
Read/Write Port: 8A43h ~ 8A40h
Default: xx xx xx xxh

D[31:24] Reserved
D[23:16] TTXTRSHR (i) ➡➡ R of Texture Transparency Color High Range
D[15:8] TTXTRSHG (i) ➡➡ G of Texture Transparency Color High Range
D[7:0] TTXTRSHB (i) ➡➡ B of Texture Transparency Color High Range

Texture Level 0 Base Address

Register Type: Read/Write
Read/Write Port: 8A47h ~ 8A44h
Default: xx xx xx xxh

D[31:0] TTX0BAS ➡➡ Texture Level 0 Base Address

If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 1 Base Address

Register Type: Read/Write
Read/Write Port: 8A4Bh ~ 8A48h
Default: xx xx xx xxh

D[31:0] TTX1BAS ➡➡ Texture Level 1 Base Address

If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 2 Base Address

Register Type: Read/Write
Read/Write Port: 8A4Fh ~ 8A4Ch
Default: xx xx xx xxh

D[31:0] TTX2BAS ➡➡ Texture Level 2 Base Address

If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 3 Base Address

Register Type: Read/Write
Read/Write Port: 8A53h ~ 8A50h
Default: xx xx xx xxh

D[31:0] TTX3BAS ➡➡ Texture Level 3 Base Address

If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 4 Base Address

Register Type: Read/Write
Read/Write Port: 8A57h ~ 8A54h
Default: xx xx xx xxh

D[31:0] TTX4BAS ➡➡ Texture Level 4 Base Address

If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 5 Base Address

Register Type: Read/Write
Read/Write Port: 8A5Bh ~ 8A58h
Default: xx xx xx xxh

D[31:0] TTX5BAS ➡➡ Texture Level 5 Base Address

If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 6 Base Address

Register Type: Read/Write
Read/Write Port: 8A5Fh ~ 8A5Ch
Default: xx xx xx xxh

D[31:0] TTX6BAS ➡➡ Texture Level 6 Base Address

If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 7 Base Address

Register Type: Read/Write
Read/Write Port: 8A63h ~ 8A60h
Default: xx xx xx xxh

D[31:0] TTX7BAS ➡➡ Texture Level 7 Base Address

If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 8 Base Address

Register Type: Read/Write
Read/Write Port: 8A67h ~ 8A64h
Default: xx xx xx xxh

D[31:0] TTX8BAS ➡➡ Texture Level 8 Base Address

If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 9 Base Address

Register Type: Read/Write
Read/Write Port: 8A6Bh ~ 8A68h
Default: xx xx xx xxh

D[31:0] TTX9BAS ➡➡ Texture Level 9 Base Address

If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0

If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 0 & 1 Pitch Control

Register Type: Read/Write
Read/Write Port: 8A6Fh ~ 8A6Ch
Default: xx xx xx xxh

D[31:27] Reserved
D[26:16] TTX0PCTL ➡➡ Texture Level 0 Pitch Control
Addr10 ~ Addr0
D[15:11] Reserved
D[10:0] TTX1PCTL ➡➡ Texture Level 1 Pitch Control
Addr10 ~ Addr0

Texture Level 2 & 3 Pitch Control

Register Type: Read/Write
Read/Write Port: 8A73h ~ 8A70h
Default: xx xx xx xxh

D[31:27] Reserved
D[26:16] TTX2PCTL ➡➡ Texture Level 2 Pitch Control
Addr10 ~ Addr0
D[15:11] Reserved
D[10:0] TTX3PCTL ➡➡ Texture Level 3 Pitch Control
Addr10 ~ Addr0

Texture Level 4 & 5 Pitch Control

Register Type: Read/Write
Read/Write Port: 8A77h ~ 8A74h
Default: xx xx xx xxh

D[31:27] Reserved

D[26:16] TTX4PCTL ➡➡ Texture Level 4 Pitch Control
Addr10 ~ Addr0
D[15:11] Reserved
D[10:0] TTX5PCTL ➡➡ Texture Level 5 Pitch Control
Addr10 ~ Addr0

Texture Level 2 & 3 Pitch Control

Register Type: Read/Write
Read/Write Port: 8A7Bh ~ 8A78h
Default: xx xx xx xxh

D[31:27] Reserved
D[26:16] TTX6PCTL ➡➡ Texture Level 6 Pitch Control
Addr10 ~ Addr0
D[15:11] Reserved
D[10:0] TTX7PCTL ➡➡ Texture Level 7 Pitch Control
Addr10 ~ Addr0

Texture Level 8 & 9 Pitch Control

Register Type: Read/Write
Read/Write Port: 8A7Fh ~ 8A7Ch
Default: xx xx xx xxh

D[31:27] Reserved
D[26:16] TTX8PCTL ➡➡ Texture Level 8 Pitch Control
Addr10 ~ Addr0
D[15:11] Reserved
D[10:0] TTX9PCTL ➡➡ Texture Level 9 Pitch Control
Addr10 ~ Addr0

Texture Setting Register 4

Register Type: Read/Write
Read/Write Port: 8A83h ~ 8A80h
Default: xx xx xx xxh

D[31:28] TTXW ➡➡ Texture Width
0000: Texture Width = 2^0 = 1
0001: Texture Width = 2^1 = 2
0010: Texture Width = 2^2 = 4
0011: Texture Width = 2^3 = 8
0100: Texture Width = 2^4 = 16
0101: Texture Width = 2^5 = 32
0110: Texture Width = 2^6 = 64
0111: Texture Width = 2^7 = 128
1000: Texture Width = 2^8 = 256
1001: Texture Width = 2^9 = 512
1010 ~ 1111: Reserved
D[27:24] TTXH ➡➡ Texture Height
0000: Texture Height = 2^0 = 1
0001: Texture Height = 2^1 = 2

0010: Texture Height = 2^2 = 4
0011: Texture Height = 2^3 = 8
0100: Texture Height = 2^4 = 16
0101: Texture Height = 2^5 = 32
0110: Texture Height = 2^6 = 64
0111: Texture Height = 2^7 = 128
1000: Texture Height = 2^8 = 256
1001: Texture Height = 2^9 = 512
1010-1111: Reserved

D[23:16]	TXCBR (i) ➡➡ R of Texture Color Base Register for Mix Mode
D[15:8]	TXCBG (i) ➡➡ G of Texture Color Base Register for Mix Mode
D[7:0]	TXCBB (i) ➡➡ B of Texture Color Base Register for Mix Mode

Texture Color Register 0 for Mix Mode

Register Type: Read/Write
Read/Write Port: 8A87h ~ 8A84h
Default: xx xx xx xxh

D[31:24]	Reserved
D[23:16]	TTXC0R (i) ➡➡ R of Texture Color Register 0
D[15:8]	TTXC0G (i) ➡➡ G of Texture Color Register 0
D[7:0]	TTXC0B (i) ➡➡ B of Texture Color Register 0

Texture Color Register 1 for Mix Mode

Register Type: Read/Write
Read/Write Port: 8A8Bh ~ 8A88h
Default: xx xx xx xxh

D[31:24]	Reserved
D[23:16]	TTXC1R (i) ➡➡ R of Texture Color Register 1
D[15:8]	TTXC1G (i) ➡➡ G of Texture Color Register 1
D[7:0]	TTXC1B (i) ➡➡ B of Texture Color Register 1

Texture Color Register for Luminance

Register Type: Read/Write
Read/Write Port: 8A8Fh ~ 8A8Ch
Default: xx xx xx xxh

D[31:24]	Reserved
D[23:16]	TTXCRR (i) ➡➡ R of Luminance
D[15:8]	TTXCRG (i) ➡➡ G of Luminance
D[7:0]	TTXCRB (i) ➡➡ B of Luminance

Texture Border Color Register

Register Type: Read/Write
Read/Write Port: 8A93h ~ 8A90h
Default: xx xx xx xxh

D[31:24]	TXCTBA (i) ➡➡ A of Texture Border
D[23:16]	TXCTBR (i) ➡➡ R of Texture Border
D[15:8]	TXCTBG (i) ➡➡ G of Texture Border

D[7:0] TXCTBB (i) ➡➡ B of Texture Border

Texture Index Palette Register 0

Register Type: Read/Write
Read/Write Port: 8A97h ~ 8A94h
Default: xx xx xx xxh

D[31:24] Reserved
D[23:16] TTXIDX0B (i) ➡➡ B of Index 0
D[15:8] TTXIDX0G (i) ➡➡ G of Index 0
D[7:0] TTXIDX0R (i) ➡➡ R of Index 0

Texture Index Palette Register 1

Register Type: Read/Write
Read/Write Port: 8A9Bh ~ 8A98h
Default: xx xx xx xxh

D[31:24] Reserved
D[23:16] TTXIDX1B (i) ➡➡ B of Index 1
D[15:8] TTXIDX1G (i) ➡➡ G of Index 1
D[7:0] TTXIDX1R (i) ➡➡ R of Index 1

Texture Index Palette Register 2

Register Type: Read/Write
Read/Write Port: 8A9Fh ~ 8A9Ch
Default: xx xx xx xxh

D[31:24] Reserved
D[23:16] TTXIDX2B (i) ➡➡ B of Index 2
D[15:8] TTXIDX2G (i) ➡➡ G of Index 2
D[7:0] TTXIDX2R (i) ➡➡ R of Index 2

Texture Index Palette Register 3

Register Type: Read/Write
Read/Write Port: 8AA3h ~ 8AA0h
Default: xx xx xx xxh

D[31:24] Reserved
D[23:16] TTXIDX3B (i) ➡➡ B of Index 3
D[15:8] TTXIDX3G (i) ➡➡ G of Index 3
D[7:0] TTXIDX3R (i) ➡➡ R of Index 3

Texture Index Palette Register 4

Register Type: Read/Write
Read/Write Port: 8AA7h ~ 8AA4h
Default: xx xx xx xxh

D[31:24] Reserved
D[23:16] TTXIDX4B (i) ➡➡ B of Index 4
D[15:8] TTXIDX4G (i) ➡➡ G of Index 4
D[7:0] TTXIDX4R (i) ➡➡ R of Index 4

Texture Index Palette Register 5

Register Type: Read/Write
Read/Write Port: 8AABh ~ 8AA8h
Default: xx xx xx xxh

D[31:24]	Reserved
D[23:16]	TTXIDX5B (i) ➡➡ B of Index 5
D[15:8]	TTXIDX5G (i) ➡➡ G of Index 5
D[7:0]	TTXIDX5R (i) ➡➡ R of Index 5

Texture Index Palette Register 6

Register Type: Read/Write
Read/Write Port: 8AAFh ~ 8AACh
Default: xx xx xx xxh

D[31:24]	Reserved
D[23:16]	TTXIDX6B (i) ➡➡ B of Index 6
D[15:8]	TTXIDX6G (i) ➡➡ G of Index 6
D[7:0]	TTXIDX6R (i) ➡➡ R of Index 6

Texture Index Palette Register 7

Register Type: Read/Write
Read/Write Port: 8AB3h ~ 8AB0h
Default: xx xx xx xxh

D[31:24]	Reserved
D[23:16]	TTXIDX7B (i) ➡➡ B of Index 7
D[15:8]	TTXIDX7G (i) ➡➡ G of Index 7
D[7:0]	TTXIDX7R (i) ➡➡ R of Index 7

Texture Index Palette Register 8

Register Type: Read/Write
Read/Write Port: 8AB7h ~ 8AB4h
Default: xx xx xx xxh

D[31:24]	Reserved
D[23:16]	TTXIDX8B (i) ➡➡ B of Index 8
D[15:8]	TTXIDX8G (i) ➡➡ G of Index 8
D[7:0]	TTXIDX8R (i) ➡➡ R of Index 8

Texture Index Palette Register 9

Register Type: Read/Write
Read/Write Port: 8ABBh ~ 8AB8h
Default: xx xx xx xxh

D[31:24]	Reserved
D[23:16]	TTXIDX9B (i) ➡➡ B of Index 9
D[15:8]	TTXIDX9G (i) ➡➡ G of Index 9
D[7:0]	TTXIDX9R (i) ➡➡ R of Index 9

Texture Index Palette Register 10

Register Type: Read/Write
Read/Write Port: 8ABFh ~ 8ABCh

Default: xx xx xx xxh

D[31:24] Reserved
D[23:16] TTXIDX10B (i) ➡➡ B of Index 10
D[15:8] TTXIDX10G (i) ➡➡ G of Index 10
D[7:0] TTXIDX10R (i) ➡➡ R of Index 10

Texture Index Palette Register 11

Register Type: Read/Write
Read/Write Port: 8AC3h ~ 8AC0h
Default: xx xx xx xxh

D[31:24] Reserved
D[23:16] TTXIDX11B (i) ➡➡ B of Index 11
D[15:8] TTXIDX11G (i) ➡➡ G of Index 11
D[7:0] TTXIDX11R (i) ➡➡ R of Index 11

Texture Index Palette Register 12

Register Type: Read/Write
Read/Write Port: 8AC7h ~ 8AC4h
Default: xx xx xx xxh

D[31:24] Reserved
D[23:16] TTXIDX12B (i) ➡➡ B of Index 12
D[15:8] TTXIDX12G (i) ➡➡ G of Index 12
D[7:0] TTXIDX12R (i) ➡➡ R of Index 12

Texture Index Palette Register 13

Register Type: Read/Write
Read/Write Port: 8ACBh ~ 8AC8h
Default: xx xx xx xxh

D[31:24] Reserved
D[23:16] TTXIDX13B (i) ➡➡ B of Index 13
D[15:8] TTXIDX13G (i) ➡➡ G of Index 13
D[7:0] TTXIDX13R (i) ➡➡ R of Index 13

Texture Index Palette Register 14

Register Type: Read/Write
Read/Write Port: 8ACFh ~ 8ACCh
Default: xx xx xx xxh

D[31:24] Reserved
D[23:16] TTXIDX14B (i) ➡➡ B of Index 14
D[15:8] TTXIDX14G (i) ➡➡ G of Index 14
D[7:0] TTXIDX14R (i) ➡➡ R of Index 14

Texture Index Palette Register 15

Register Type: Read/Write
Read/Write Port: 8AD3h ~ 8AD0h
Default: xx xx xx xxh

D[31:24] Reserved

D[23:16] TTXIDX15B (i) ➡➡ B of Index 15
D[15:8] TTXIDX15G (i) ➡➡ G of Index 15
D[7:0] TTXIDX15R (i) ➡➡ R of Index 15

Reserved Registers

Register Type: Read/Write
Read/Write Port: 8AFEh ~ 8AD4h
Default: xx xx xx xxh

D[31:0] Reserved

.14 End of Primitive Setting Register

Register Type: Read/Write
Read/Write Port: 8AFFh
Default: xxh

D[7:0] TEND ➡➡ End of Primitive List
This is a dummy register. The data stored in this register is no meaning.

.15 Stipple Pattern Registers

Stipple Pattern 0 Register

Register Type: Read/Write
Read/Write Port: 8B03h ~ 8B00h
Default: xx xx xx xxh

D[31:0] T0STIP ➡➡ Stipple Pattern 0
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 1 Register

Register Type: Read/Write
Read/Write Port: 8B07h ~ 8B04h
Default: xx xx xx xxh

D[31:0] T1STIP ➡➡ Stipple Pattern 1
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 2 Register

Register Type: Read/Write
Read/Write Port: 8B0Bh ~ 8B08h
Default: xx xx xx xxh

D[31:0] T2STIP ➡➡ Stipple Pattern 2
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 3 Register

Register Type: Read/Write
Read/Write Port: 8B0Fh ~ 8B0Ch
Default: xx xx xx xxh

D[31:0] T3STIP ➡➡ Stipple Pattern 3
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 4 Register

Register Type: Read/Write
Read/Write Port: 8B13h ~ 8B10h
Default: xx xx xx xxh

D[31:0] T4STIP ➡➡ Stipple Pattern 4
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 5 Register

Register Type: Read/Write
Read/Write Port: 8B17h ~ 8B14h
Default: xx xx xx xxh

D[31:0] T5STIP ➡➡ Stipple Pattern 5
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 6 Register

Register Type: Read/Write
Read/Write Port: 8B1Bh ~ 8B18h
Default: xx xx xx xxh

D[31:0] T6STIP ➡➡ Stipple Pattern 6
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 7 Register

Register Type: Read/Write
Read/Write Port: 8B1Fh ~ 8B1Ch
Default: xx xx xx xxh

D[31:0] T7STIP ➡➡ Stipple Pattern 7
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 8 Register

Register Type: Read/Write
Read/Write Port: 8B23h ~ 8B20h
Default: xx xx xx xxh

D[31:0] T8STIP ➡➡ Stipple Pattern 8
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 9 Register

Register Type: Read/Write
Read/Write Port: 8B27h ~ 8B24h

Default: xx xx xx xxh

D[31:0] T9STIP ➡➡ Stipple Pattern 2
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 10 Register

Register Type: Read/Write
Read/Write Port: 8B2Bh ~ 8B28h
Default: xx xx xx xxh

D[31:0] T10STIP ➡➡ Stipple Pattern 10
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 11 Register

Register Type: Read/Write
Read/Write Port: 8B2Fh ~ 8B2Ch
Default: xx xx xx xxh

D[31:0] T11STIP ➡➡ Stipple Pattern 11
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 12 Register

Register Type: Read/Write
Read/Write Port: 8B33h ~ 8B30h
Default: xx xx xx xxh

D[31:0] T12STIP ➡➡ Stipple Pattern 12
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 13 Register

Register Type: Read/Write
Read/Write Port: 8B37h ~ 8B34h
Default: xx xx xx xxh

D[31:0] T13STIP ➡➡ Stipple Pattern 13
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 14 Register

Register Type: Read/Write
Read/Write Port: 8B3Bh ~ 8B38h
Default: xx xx xx xxh

D[31:0] T14STIP ➡➡ Stipple Pattern 14
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 15 Register

Register Type: Read/Write

Read/Write Port: 8B3Fh ~ 8B3Ch
Default: xx xx xx xxh

D[31:0] T15STIP ➡➡ Stipple Pattern 15
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 16 Register

Register Type: Read/Write
Read/Write Port: 8B43h ~ 8B40h
Default: xx xx xx xxh

D[31:0] T16STIP ➡➡ Stipple Pattern 16
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 17 Register

Register Type: Read/Write
Read/Write Port: 8B47h ~ 8B44h
Default: xx xx xx xxh

D[31:0] T17STIP ➡➡ Stipple Pattern 17
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 18 Register

Register Type: Read/Write
Read/Write Port: 8B4Bh ~ 8B48h
Default: xx xx xx xxh

D[31:0] T18STIP ➡➡ Stipple Pattern 18
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 19 Register

Register Type: Read/Write
Read/Write Port: 8B4Fh ~ 8B4Ch
Default: xx xx xx xxh

D[31:0] T19STIP ➡➡ Stipple Pattern 19
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 20 Register

Register Type: Read/Write
Read/Write Port: 8B53h ~ 8B50h
Default: xx xx xx xxh

D[31:0] T20STIP ➡➡ Stipple Pattern 20
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 21 Register

Register Type: Read/Write
Read/Write Port: 8B57h ~ 8B54h
Default: xx xx xx xxh

D[31:0] T21STIP ➡➡ Stipple Pattern 21
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 22 Register

Register Type: Read/Write
Read/Write Port: 8B5Bh ~ 8B58h
Default: xx xx xx xxh

D[31:0] T22STIP ➡➡ Stipple Pattern 22
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 23 Register

Register Type: Read/Write
Read/Write Port: 8B5Fh ~ 8B5Ch
Default: xx xx xx xxh

D[31:0] T23STIP ➡➡ Stipple Pattern 23
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 24 Register

Register Type: Read/Write
Read/Write Port: 8B63h ~ 8B60h
Default: xx xx xx xxh

D[31:0] T24STIP ➡➡ Stipple Pattern 24
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 25 Register

Register Type: Read/Write
Read/Write Port: 8B67h ~ 8B64h
Default: xx xx xx xxh

D[31:0] T25STIP ➡➡ Stipple Pattern 25
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 26 Register

Register Type: Read/Write
Read/Write Port: 8B6Bh ~ 8B68h
Default: xx xx xx xxh

D[31:0] T26STIP ➡➡ Stipple Pattern 26
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 27 Register

Register Type: Read/Write
Read/Write Port: 8B6Fh ~ 8B6Ch
Default: xx xx xx xxh

D[31:0] T27STIP ➡➡ Stipple Pattern 27
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 28 Register

Register Type: Read/Write
Read/Write Port: 8B73h ~ 8B70h
Default: xx xx xx xxh

D[31:0] T28STIP ➡➡ Stipple Pattern28
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 29 Register

Register Type: Read/Write
Read/Write Port: 8B77h ~ 8B74h
Default: xx xx xx xxh

D[31:0] T29STIP ➡➡ Stipple Pattern 29
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 30 Register

Register Type: Read/Write
Read/Write Port: 8B7Bh ~ 8B78h
Default: xx xx xx xxh

D[31:0] T30STIP ➡➡ Stipple Pattern 30
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 31 Register

Register Type: Read/Write
Read/Write Port: 8B7Fh ~ 8B7Ch
Default: xx xx xx xxh

D[31:0] T31STIP ➡➡ Stipple Pattern 31
0: The pixel should not be written.
1: The pixel should be written.

8. Electrical Characteristics

1 Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Ambient operation temperature	0	70	^{0}C
Storage temperature	-40	125	^{0}C
Input voltage	-0.3	5.5	V
Output voltage	-0.5	3.6	V

NOTE:
Stress above these listed may cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

2 DC Characteristics

T_A = 0 - 70 ^{0}C, V_{DD} = 3.3 V ± 5 %, V_{DD} 5= 5 V ± 5 %,GND = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-0.5	0.8	V	
V_{IH}	Input high voltage	2.2	5.5	V	
V_{OL}	Output low voltage	-	0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH} = -1.0 mA
I_{IL}	Input leakage current	-	± 10	uA	
I_{OZ}	tristate leakage current	-	± 20	uA	0.45 < V_{OUT} < V_{DD}

3 DC Characteristics for DAC (Analog Output Characteristics)

Description	Min	Typical	Max	Unit
Black Level	-	0	-	V
White Level	-	660	-	mV
ILE	-1.0	-	+1.0	LSB
DLE	-0.5	-	+0.5	LSB
1 LSB	-	2.625	-	mV
Iref	-	8.40	-	mA

4 AC Characteristics for DAC (Analog Output Characteristics)

Description	Parameter	Condition	Typical	Max.	Unit
Settling Time	Tsett	R=37.5 ohm C1=30 pF	-	6	ns

5 AC Characteristics

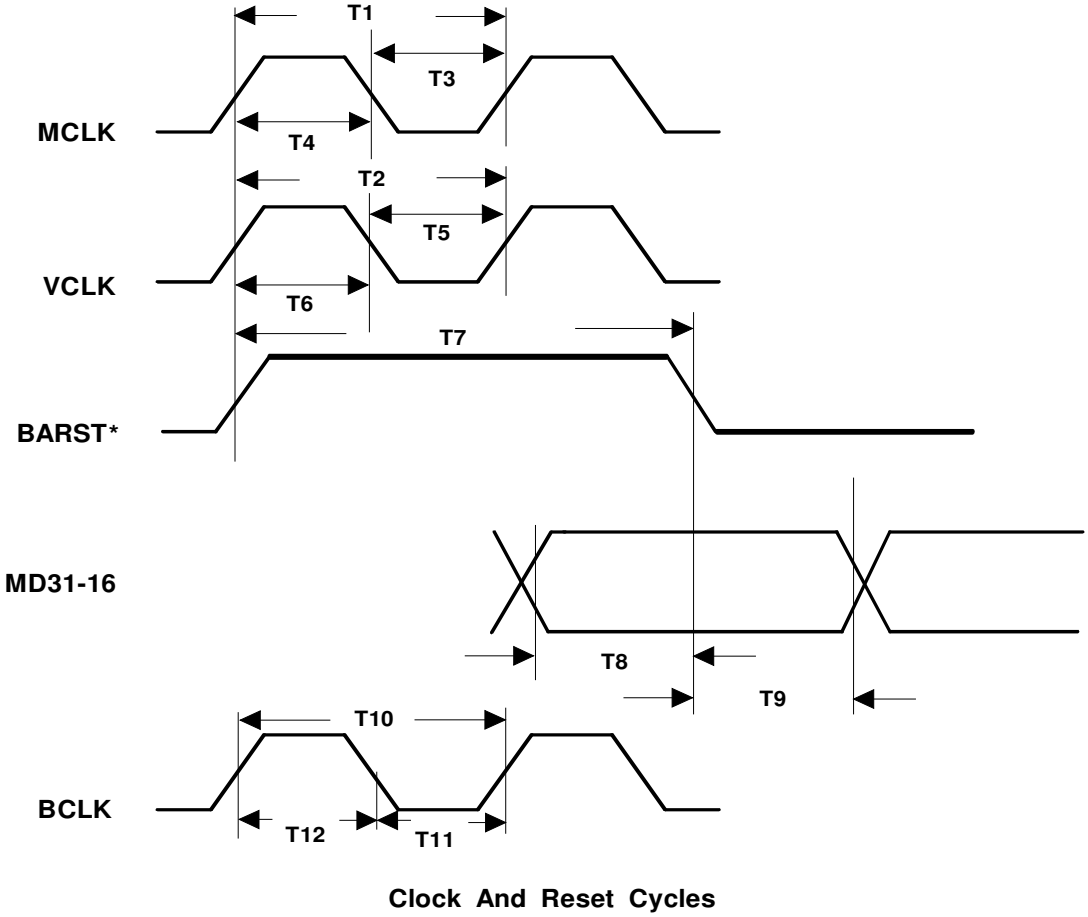


Figure 8.1 Clock and Reset Cycles

Clock and Reset Timing Table

Symbol	Parameter	Min	Max
T_1	MCLK Period	10	
T_2	VCLK Period	5.5	
T_3	MCLK Low Time	4	
T_4	MCLK High Time	4	
T_5	VCLK Low Time	2.2	
T_6	VCLK High Time	2.2	
T_7	Reset High Time	400	
T_8	System Configuration Data Setup Time	20	
T_9	System Configuration Data Hold Time	20	
T_{10}	BCLK Period (33MHz / 66MHz)	30 /15	∞ / 30
T_{11}	BCLK High Time (33MHz /66MHz)	11 / 6	
T_{12}	BCLK Low Time (33MHz /66MHz)	11 / 6	

(Units: ns)

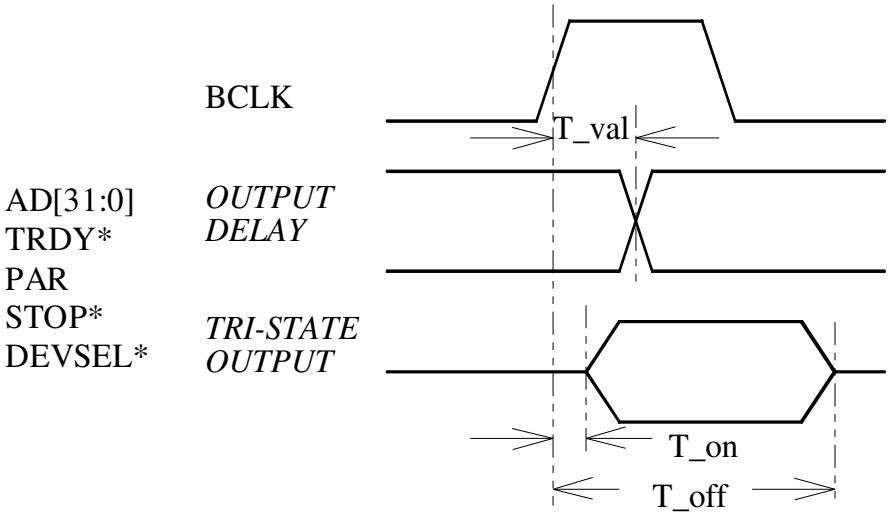


Figure 8.2 PCI/AGP Output and Tri-state Timing

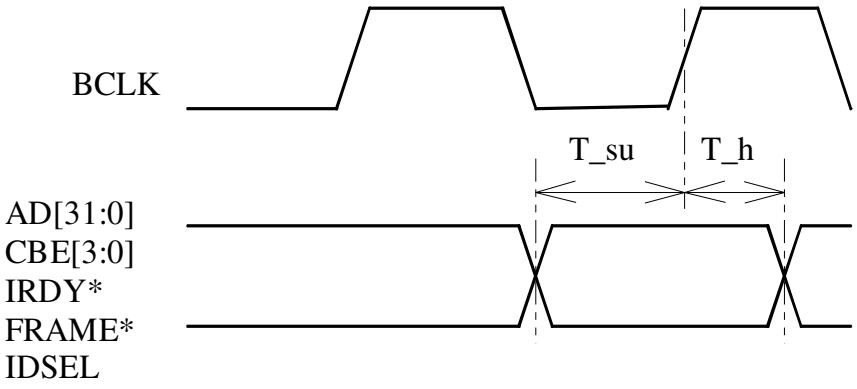


Figure 8.3 PCI/AGP Input Timing

PCI Timing Table

Symbol	Parameter	66MHz		33MHz		Units
		Min	Max	Min	Max	
T_{val}	BCLK to Signal Valid Delay	2	6	2	11	ns
T_{on}	Float to Active Delay	2	-	2	-	ns
T_{off}	Active to Float Delay	-	14	-	28	ns
T_{su}	Input Setup Time to BCLK	3	-	7	-	ns
T_h	Input Hold Time from BCLK	0	-	0	-	ns

AGP 1X Timing Table

Symbol	Parameter	Min	Max	Units
T_{cyc}	BCLK Cycle Time	15	30	ns
T_{val}	BCLK to Signal Valid Delay	1.5	6	ns
T_{on}	Float to Active Delay	1.5	6	ns
T_{off}	Active to Float Delay	1	14	ns
T_{su}	Input Setup Time to BCLK	5	-	ns
T_{h}	Input Hold Time from BCLK	0.5	-	ns

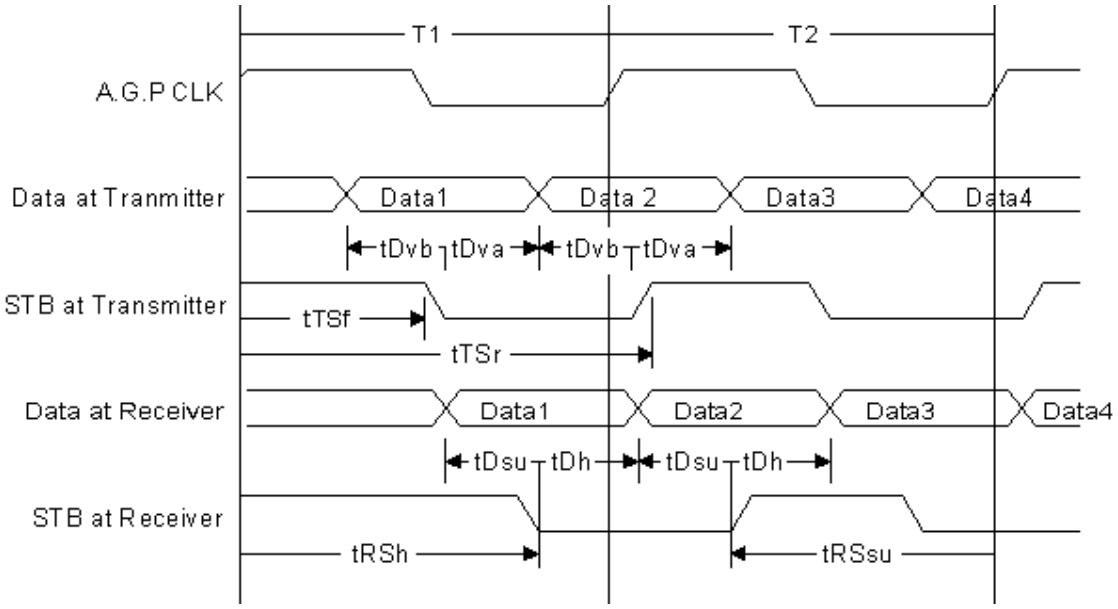


Figure 8.4 AGP 133 Timing Diagram

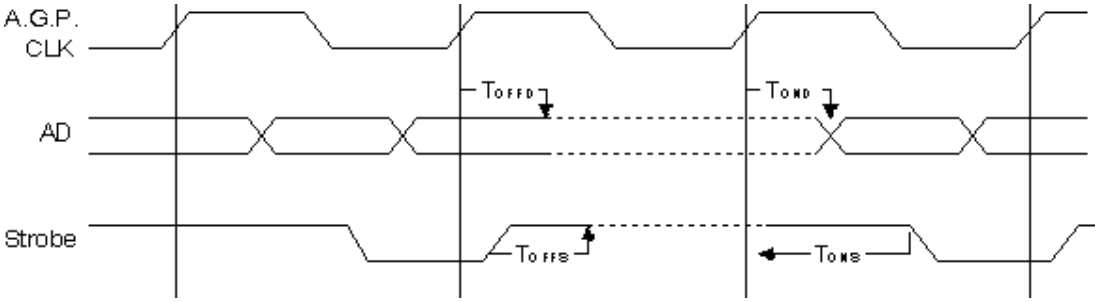


Figure 8.5 Strobe/Data Turnaround Timings

AGP 2X Timing Table

Symbol	Parameter	Min	Max	Units	Notes
Transmitter Output Signals:					
tTSf	CLK to transmit strobe falling	2	12	ns	
tTSr	CLK to transmit strobe rising		20	ns	

tDvb	Data valid before strobe	1.7		ns	
tDva	Data valid after strobe	1.7		ns	
tONd	Float to Active Delay	-1	9	ns	
tOFFd	Active to Float Delay	1	12	ns	
tONS	Strobe active to strobe falling edge setup	6	10	ns	
tOFFS	Strobe rising edge to strobe float delay	6	10	ns	
Receiver Input Signals:					
tRSsu	Receive strobe setup time to CLK	6		ns	
tRSh	Receive strobe hold time hold time from CLK	1		ns	
tDsu	Data to strobe setup time	1		ns	
tDh	Strobe to data hold time	1		ns	

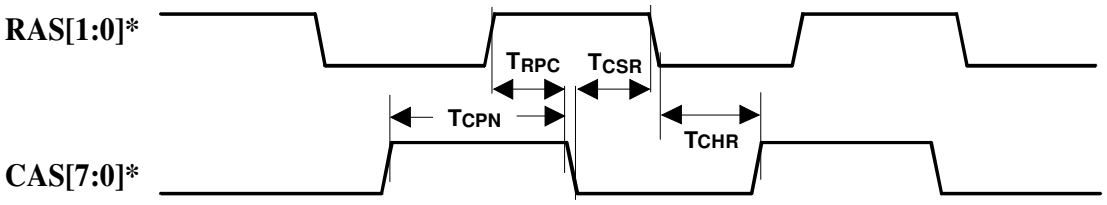


Figure 8.6 CAS Before RAS Refresh Cycle

CAS Before RAS Refresh Cycle Timing Table

Sym.	Parameter	T-Value		MCLK 50 MHz		MCLK 60 MHz	
		Min	Max	Min	Max	Min	Max
T_{CPN}	CAS* Precharge Time	1	-	20	-	16.7	-
T_{RPC}	RAS* High to CAS* Low Precharge Time	2	-	40	-	33.4	-
T_{CSR}	CAS* Before RAS* Setup Time	1	-	20	-	16.7	-
T_{CHR}	CAS* Before RAS* Hold Time	3	-	60	-	50.1	-

(Units: ns)

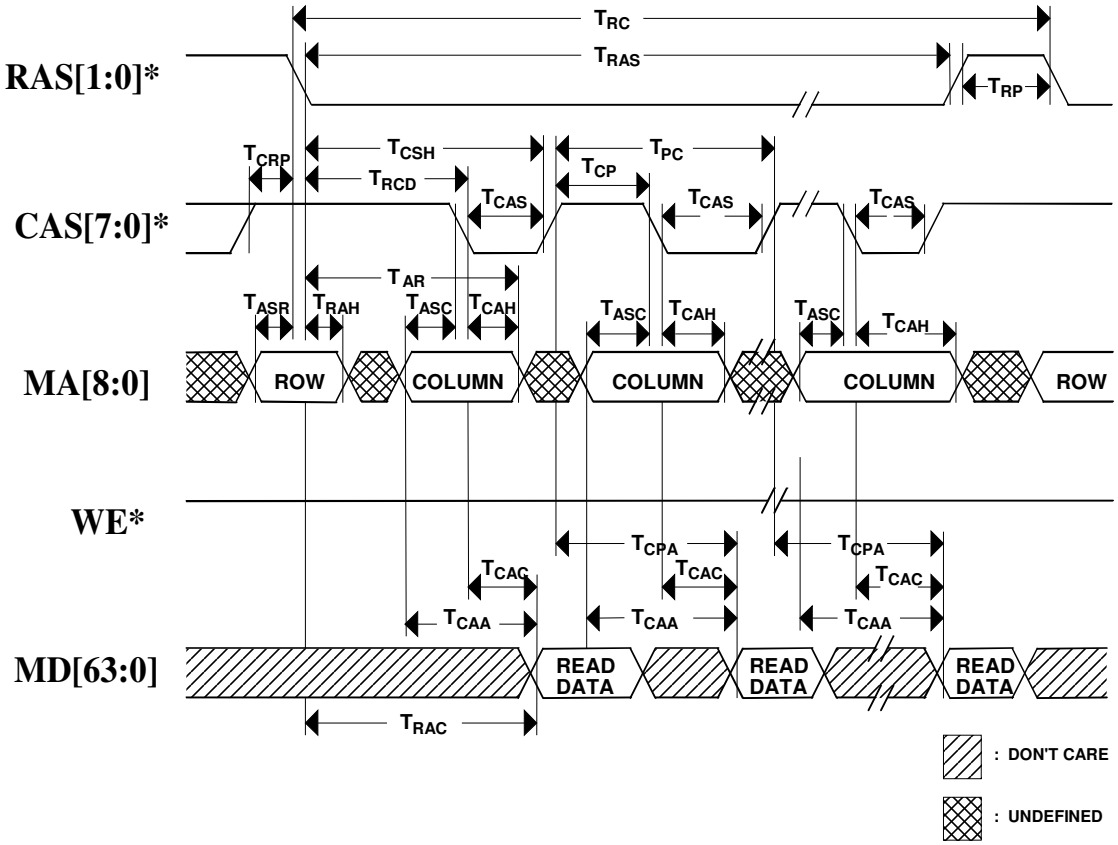


Figure 8.7 Video Memory Fast Page Mode Read Cycle

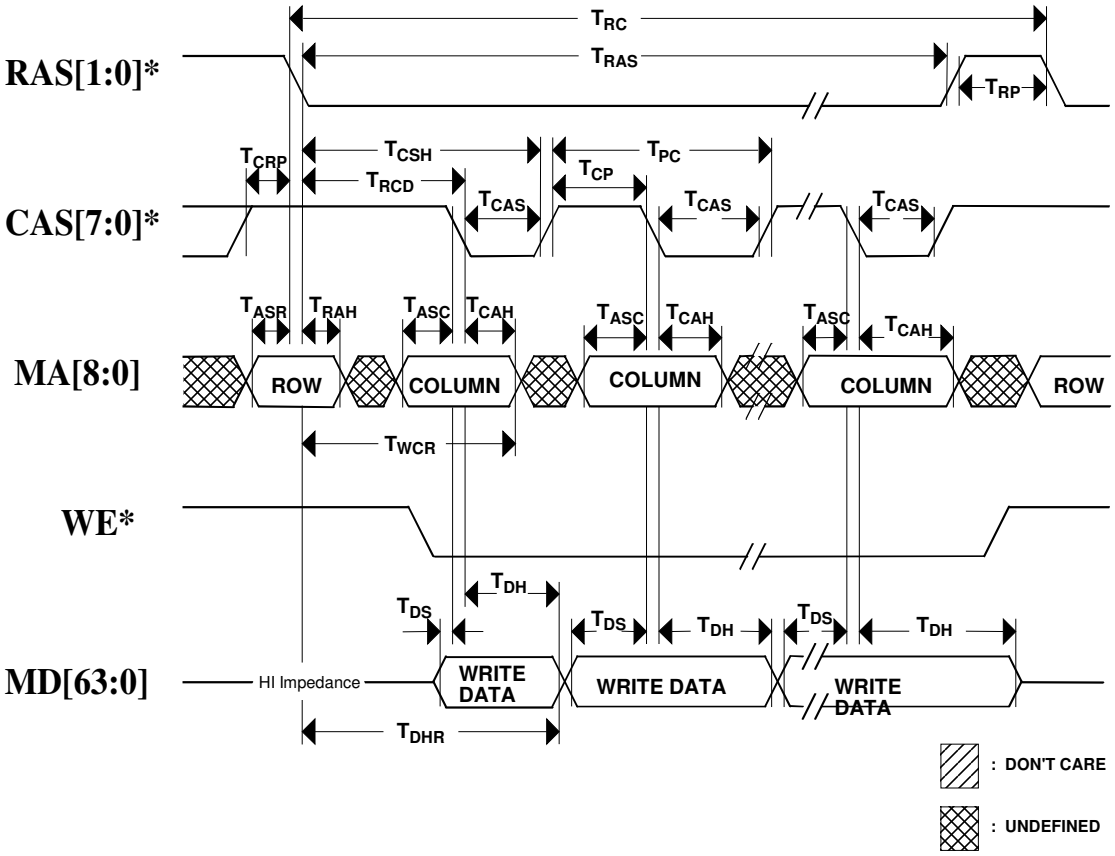


Figure 8.8 Video Memory Fast Page Mode Write Cycle

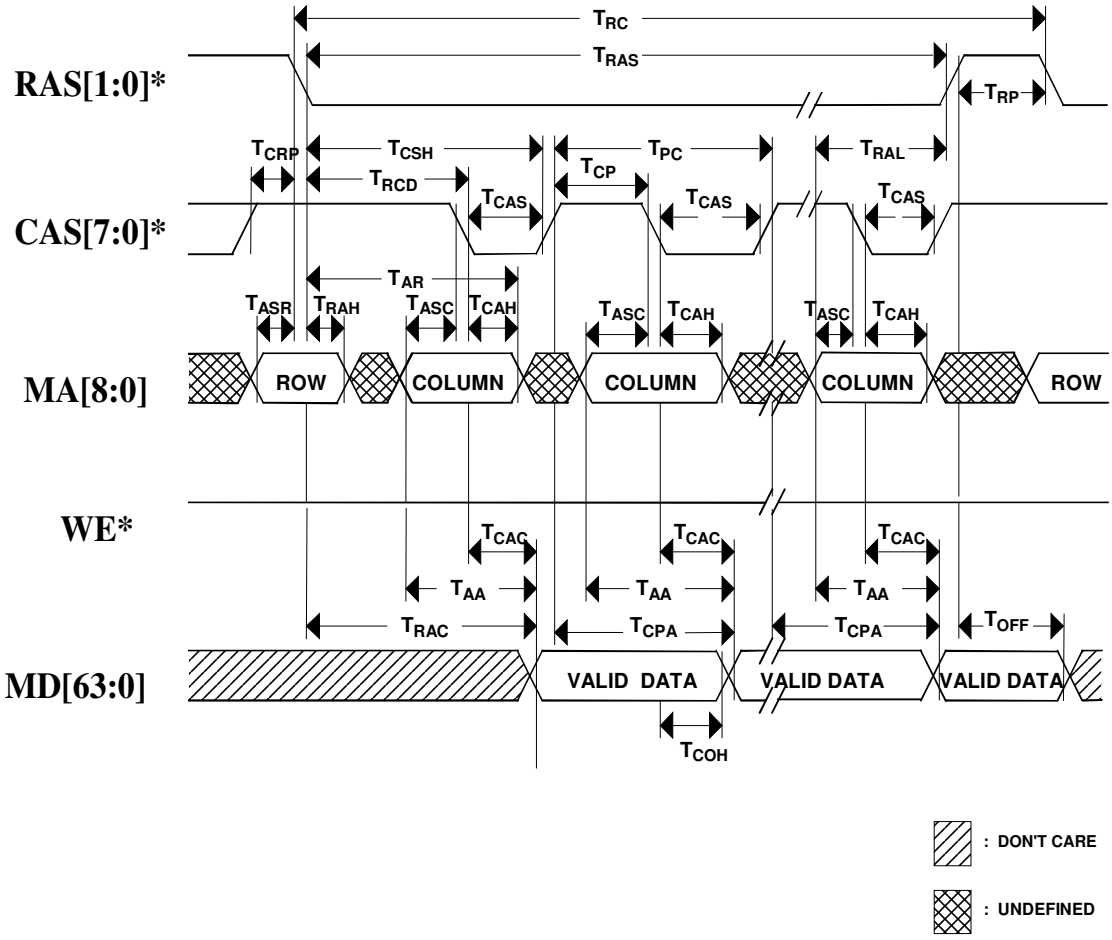


Figure 8.9 Video Memory Fast Page Mode Read Cycle with Extended Data

Video Memory Fast Page Mode Read/Write Cycle Timing Table

Guaranteed Timings

Sym.	Parameter	T-Value		MCLK 50 MHz		MCLK 60 MHz	
		Min.	Max.	Min.	Max.	Min.	Max.
T_{CAS}	CAS* Pulse Width	1	-	20	-	16.7	-
T_{CRP}	CAS* to RAS* Precharge Time	2	-	40	-	33.4	-
T_{CSH}	CAS* Hold Time	4	-	80	-	66.8	-
T_{PC}	CAS* Cycle Time	2	-	40	-	33.4	-
T_{CP}	CAS* Precharge Time	1	-	20	-	16.7	-
T_{RP}	RAS* Precharge Time	3	-	60	-	50.1	-
T_{RC}	RAS* Cycle Time	7	-	140	-	116.9	-
T_{RAS}	RAS* Pulse Width	4	-	80	-	66.8	-
T_{RCD}	RAS* to CAS* Delay Time	3	-	60	-	50.1	-
T_{RAH}	Row Address Hold Time	2	-	40	-	33.4	-
T_{AR}	Column Address Hold From RAS*	4	-	80	-	66.8	-
T_{ASC}	Column Address Setup Time	1	-	20	-	16.7	-
T_{CAH}	Column Address Hold Time	1	-	20	-	16.7	-
T_{WCR}	Write Command Hold Referenced to RAS*	3.5	-	70	-	58.5	-
T_{DS}	Data-in Setup Time	0.5	-	10	-	8.4	-
T_{DH}	Data-in Hold Time	1	-	20	-	16.7	-
T_{DHR}	Data Hold Referenced to RAS*	4	-	80	-	66.8	-
T_{ASR}	Row-Address Setup Time	0	-	0	-	0	-
T_{COH}	Data Output Hold after CAS* LOW (Only for EDO-DRAM)	-	-	5	-	5	-

(Units: ns)

Required Timing Table

Sym.	Parameter	T-Value		MCLK 50MHz		MCLK 60MHz	
		Min.	Max.	Min.	Max.	Min.	Max.
T_{CPA}	Data Access Time from CAS* Precharge	-	2	-	40	-	33.3
T_{RAC}	Data Access Time from RAS*	-	4	-	80	-	66.6
T_{CAC}	Data Access Time from CAS*	-	1	-	20	-	33.3
T_{CAA}	Data Access Time form Column Address	-	2	-	40	-	66.6

(Units: ns)

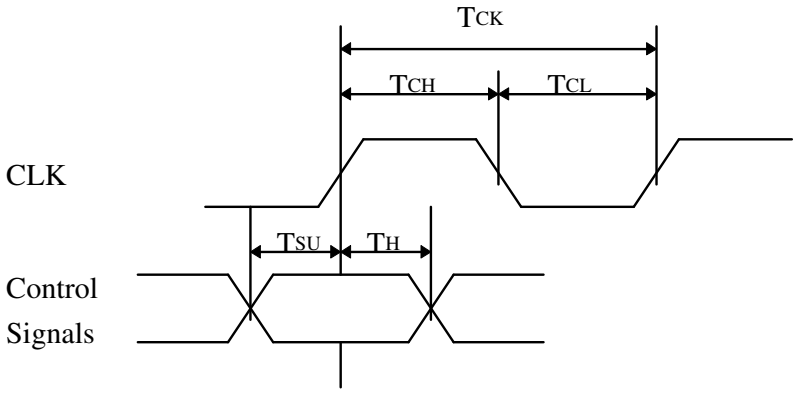


Figure 8.10 SDRAM/SGRAM input/output Timing

SDRAM/SGRAM Timing Table

Symbol	Parameter		Min	Max.	Units
T_{CK}	Clock Cycle Time	latency=3	12 (83.3 MHz)		ns
		latency=2	18 (55 MHz)		ns
T_{CH}	CLK high level width		4		ns
T_{CL}	CLK low level width		4		ns
T_{SU}	Setup Timing		3.5		ns
T_{H}	Hold Timing		1.5		ns

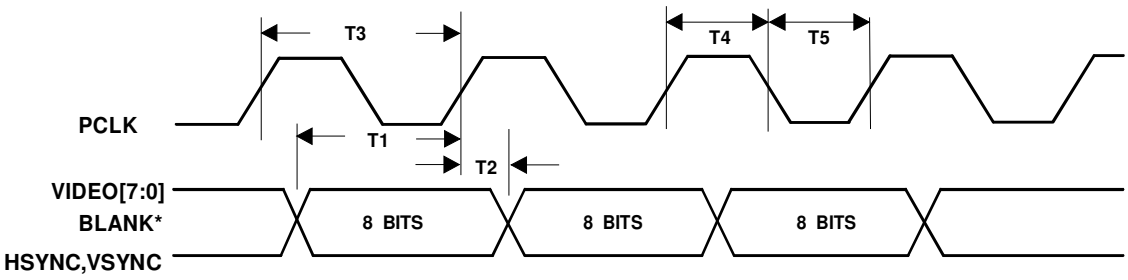


Figure 8.11 Video Timing 4, 8, and 16 Bits/Pixel Modes

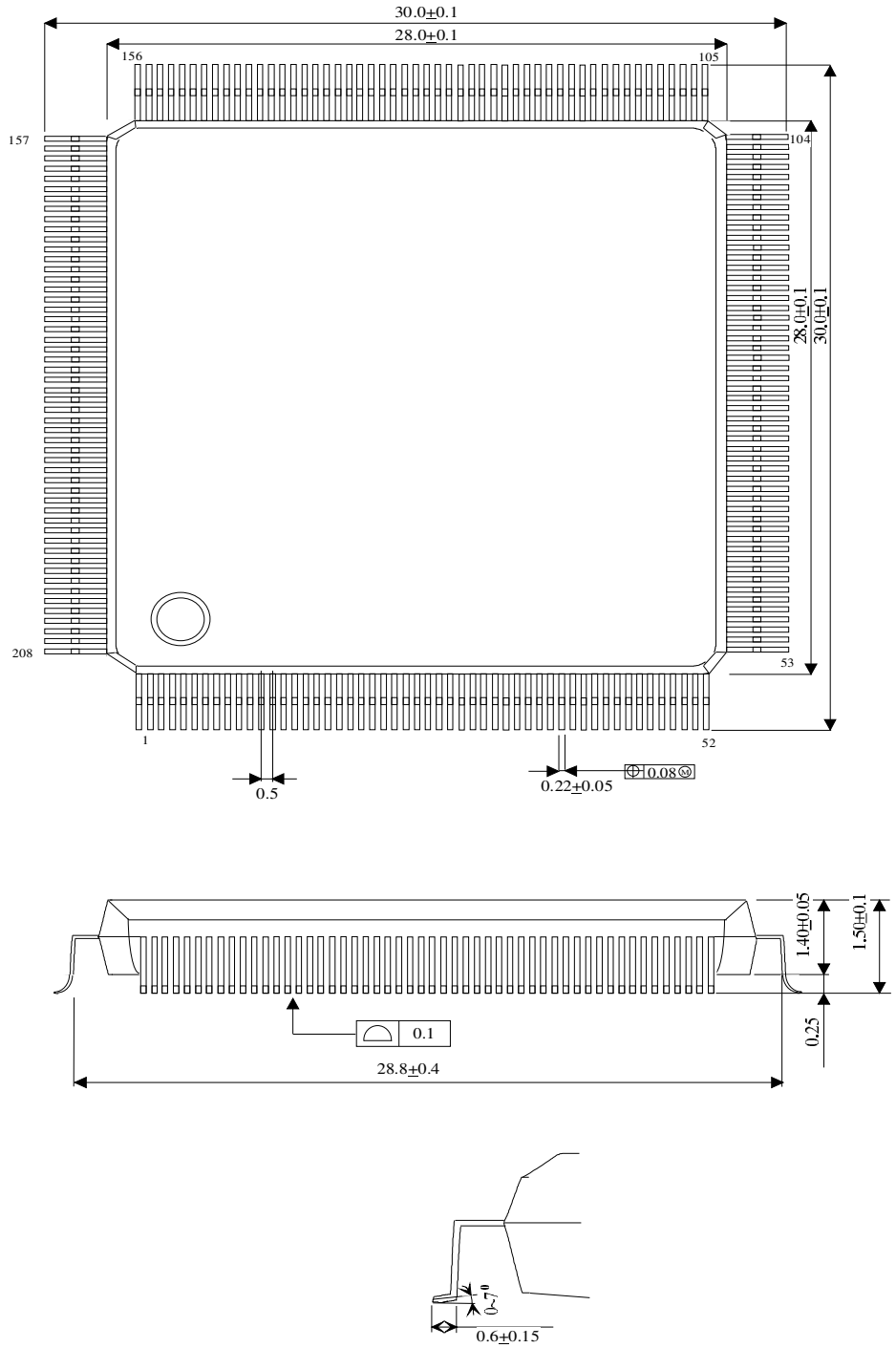
4, 8, and 16 BPP Video AC Timing Table

Symbol	Parameter	Min.	Max.	Notes
T_1	VIDEO[7:0], BLANK*, SYNC Setup Time	10	-	
T_2	VIDEO[7:0], BLANK*, SYNC Hold Time	2	-	
T_3	PCLK Period	20	-	
T_4	PCLK High Time	7	-	
T_5	PCLK Low Time	7	-	

(Units: ns)

9. Mechanical Dimension

QFP208-P (208-Pin Plastic Flat Package) Unit: mm



10. Appendix A. Recommended Memory Configuration

1M Byte Display Memory Using 256Kx4 DRAM

	U1	U2	U3	U4
RAS*	RAS0*	RAS0*	RAS0*	RAS0*
CAS*	CAS0*	CAS0*	CAS1*	CAS1*
WE*	WE*	WE*	WE*	WE*
ADDR	MA[0:8]	MA[0:8]	MA[0:8]	MA[0:8]
DATA	MD[0:3]	MD[4:7]	MD[8:11]	MD[12:15]
PLANE	0	0	1	1
Bank	0	0	0	0

	U5	U6	U7	U8
RAS*	RAS0*	RAS0*	RAS0*	RAS0*
CAS*	CAS2*	CAS2*	CAS3*	CAS3*
WE*	WE*	WE*	WE*	WE*
ADDR	MA[0:8]	MA[0:8]	MA[0:8]	MA[0:8]
DATA	MD[16:19]	MD[20:23]	MD[24:27]	MD[28:31]
PLANE	2	2	3	3
Bank	0	0	0	0

1M Byte Display Memory Using 2-CAS 256Kx16 DRAM

	U1	U2
RAS*	RAS0*	RAS0*
CASU*	CAS0*	CAS2*
CASL*	CAS1*	CAS3*
WE*	WE*	WE*
ADDR	MA[0:8]	MA[0:8]
DATA	MD[0:15]	MD[16:31]
PLANE	0,1	2,3
Bank	0	0

1M Byte Display Memory Using 128Kx32x2-bank SGRAM

	U1
CLK	SCLK0
CS*	CS0*
RAS*	SRAS*
CAS*	SCAS*
WE*	WE*
DQM	DQM[0:3]
ADDR	MA[0:9]
DATA	MD[0:31]
CKE	VDD
DSF	DSF
PLANE	0,1,2,3
Bank	0

2M Byte Display Memory Using 2-CAS 256Kx16 DRAM

	U1	U2	U3	U4
RAS*	RAS0*	RAS0*	RAS0*	RAS0*
CASU*	CAS0*	CAS2*	CAS4*	CAS6*
CASL*	CAS1*	CAS3*	CAS5*	CAS7*
WE*	WE*	WE*	WE*	WE*
ADDR	MA[0:8]	MA[0:8]	MA[0:8]	MA[0:8]
DATA	MD[0:15]	MD[16:31]	MD[32:47]	MD[48:63]
PLANE	0,1	2,3	0,1	2,3
Bank	0	0	1	1

2M Byte Display Memory Using 128Kx32x2-bank SGRAM

	U1	U2
CLK	SCLK0	SCLK1
CS*	CS0*	CS0*
RAS*	SRAS*	SRAS*
CAS*	SCAS*	SCAS*
WE*	WE*	WE*
DQM	DQM[0:3]	DQM[4:7]
ADDR	MA[0:9]	MA[0:9]
DATA	MD[0:31]	MD[32:63]
CKE	VDD	VDD
DSF	DSF	DSF
PLANE	0,1,2,3	0,1,2,3
Bank	0	1

4M Byte Display Memory Using 2-CAS 256Kx16 DRAM

	U1	U2	U3	U4
RAS*	RAS0*	RAS0*	RAS0*	RAS0*
CASU*	CAS0*	CAS2*	CAS4*	CAS6*
CASL*	CAS1*	CAS3*	CAS5*	CAS7*
WE*	WE*	WE*	WE*	WE*
ADDR	MA[0:8]	MA[0:8]	MA[0:8]	MA[0:8]
DATA	MD[0:15]	MD[16:31]	MD[32:47]	MD[48:63]
PLANE	0,1	2,3	0,1	2,3
Bank	0	0	1	1

	U5	U6	U7	U8
RAS*	RAS1*	RAS1*	RAS1*	RAS1*
CASU*	CAS0*	CAS2*	CAS4*	CAS6*
CASL*	CAS1*	CAS3*	CAS5*	CAS7*
WE*	WE*	WE*	WE*	WE*
ADDR	MA[1:8]	MA[1:8]	MA[1:8]	MA[1:8]
DATA	MD[0:15]	MD[16:31]	MD[32:47]	MD[48:63]
PLANE	0,1	2,3	0,1	2,3
Bank	2	2	3	3

4M Byte Display Memory Using 128Kx32x2-bank SGRAM

	U1	U2	U3	U4
CLK	SCLK0	SCLK1	SCLK0	SCLK1
CS*	CS0*	CS0*	CS1*	CS1*
RAS*	SRAS*	SRAS*	SRAS*	SRAS*
CAS*	SCAS*	SCAS*	SCAS*	SCAS*
WE*	WE*	WE*	WE*	WE*
DQM	DQM[0:3]	DQM[4:7]	DQM[0:3]	DQM[4:7]
ADDR	MA[0:9]	MA[0:9]	MA[0:9]	MA[0:9]
DATA	MD[0:31]	MD[32:63]	MD[0:31]	MD[32:63]
CKE	VDD	VDD	VDD	VDD
DSF	DSF	DSF	DSF	DSF
PLANE	0,1,2,3	0,1,2,3	0,1,2,3	0,1,2,3
Bank	0	1	2	3

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