Intel, Digital Attempt Settlement

According to a *Wall Street Journal* report, Intel and Digital executives are negotiating a settlement to the companies' legal actions (see MPR 6/2/97, p. 26) that could result in Intel paying Digital up to $1.5 billion. In exchange, the proposed settlement would give Intel Digital's Alpha technology as well as its Hudson fab, currently outfitted for 0.35-micron production. If accepted, the deal is likely to accelerate Digital's transition to IA-64.

The story appears to have been leaked by a Digital executive participating in the negotiations, probably to weaken Alpha and accelerate the settlement, which is reportedly opposed by Digital CEO Robert Palmer. Intentional or not, the widespread press coverage has weakened public perception of Alpha and is likely to create a chill in Digital's sales until the issue is resolved. Wall Street responded positively to the news that Digital might phase out Alpha, pushing up the company's stock price.

Although the *Journal* reported Intel would acquire the Alpha line, such an arrangement seems unlikely to pass muster with the Federal Trade Commission (FTC). Instead, it seems likely Intel would simply license the Alpha technology, settling the patent-infringement claims that Digital has brought in its lawsuit. Intel has no need to add another product line to its portfolio, but some aspects of the Alpha technology might improve the performance of Merced and future IA-64 chips. Since the Merced design is nearly complete, however, any changes to that chip would be small and would not provide much value to Intel.

Digital has been seeking for some time to sell capacity in its fab, which is underutilized due to the low volumes of Alpha chips. Intel's fab capacity has been tight recently (see MPR 4/21/97, p. 3), but converting the Hudson fab to a state-of-the-art 0.25-micron process would take months, by which time we expect Intel's capacity crunch will have eased. Intel may have plans that require more capacity, however, and the Hudson fab is a valuable asset.

If Digital sells its fab to Intel, it would need assurances that Intel would build Alpha chips at Hudson in a foundry arrangement, unless existing Alpha licensees Mitsubishi and Samsung could satisfy Digital's needs. Presumably, Digital would continue developing new Alpha designs, including the nearly complete 21264 and follow-on products. This arrangement could allow Alpha to persist for some time.

Intel, however, probably isn't interested in providing unbounded foundry services for a processor that will be Merced's chief competitor on the performance front. We doubt the company will accept such an arrangement unless Digital commits to an orderly transition from Alpha to IA-64. To help encourage this transition, the proposed deal reportedly includes significant discounts on Digital's future purchases of IA-64 processors.

A transition to IA-64 could be difficult for Digital's customers, many of whom only recently have converted from VAX (or MIPS) to Alpha. Digital could ease the blow with a binary translator from Alpha to IA-64 (sort of a reverse FX!32), and Intel might even add some Alpha compatibility features in IA-64, although probably not until Merced II appears in 2001. Even so, Digital is likely to lose customers in the transition, just as it lost customers in the VAX-to-Alpha transition. The question for the system maker is whether it would do any better by staying with Alpha. —*L.G.*

BOPS Raises Curtain on ManArray DSP

The design team behind the IBM Mfast, a single-chip DSP array (see MPR 12/4/95, p. 1), is back again as an independent company, along with new management and engineering staff. At the recent Microprocessor Forum, Gerald Pechanek, now the chief technical officer of BOPS (*www.bops.com*), described the startup's ManArray signal processor core, which is based on new processing elements and a unique on-chip interconnect topology.

In contrast with Mfast, ManArray uses clusters of processing elements (PEs) with a separate sequence processor (SP) and communications switch in each cluster, as well as an optimized cluster interconnect scheme that minimizes the quantity and length of on-chip wiring. Each processing element has a small amount of local memory. The most common transfers between PEs require only one clock cycle, permitting high throughput on typical signal-processing tasks.

The new processing elements use VLIW techniques to achieve unusually high performance. ManArray will provide floating-point support, eliminating one of the limitations of Mfast. BOPS says a single four-PE cluster can calculate the product of a four-element vector and a 4×4 matrix in just two cycles, sufficient to transform 50 million 3D vectors per second at an expected clock frequency of 100 MHz.

Instead of selling chips, BOPS plans to license ManArray cores to customers in the 3D, video-encoding, and communications markets. BOPS will produce synthesizable cores with various numbers of processing elements, a plan that should offer enough scalability to meet a wide range of customer needs. These cores can be combined with other elements, such as an AGP or PCI bus interface, a Rambus memory controller, and other custom peripherals.

The first BOPS product is Kitty Hawk, a synthesizable core planned for 1H98 with a single four-PE cluster, an SP, and a bus interface. The Kitty Hawk cluster is expected to require 181,000 gates of logic plus 16K of SRAM, or just 27 mm^2 in a 0.35-micron process. Average power consumption for the cluster is estimated at 1.3 W; peak performance at 100 MHz is 12.8 BOPS on 8-bit data. BOPS says the Kitty Hawk design will scale readily to a four-cluster design with 16 PEs capable of 51.2 BOPS. —*P.N.G.*

S3 Integrates DRAM With Notebook 3D

Combining the company's mature Virge/MX mobile 3D chip with 2M of 128-bit 85-MHz SDRAM, S3's Virge/MXi, announced at the recent Microprocessor Forum, joins a growing list of notebook graphics chips with integrated memory. The new chip is the first to combine integrated DRAM and 3D hardware acceleration, however, which sets it apart from its competition.

There have been earlier parts with integrated frame buffers, such as Trident's Cyber9388 and NeoMagic's MagicGraph 128XD (see MPR 6/23/97, p. 5), and other notebook graphic controllers offer 3D acceleration, but being first to market with both features in a single chip should give S3 a valuable edge in this competitive market. Without an on-chip setup engine, the Virge/MXi's 3D performance will be far below that of modern desktop 3D chips, but notebook customers care more about battery life than rendering speed, and the Virge/MXi has a decisive edge in that respect. S3 estimates the new chip's power consumption at less than 1.2 W with 3D acceleration enabled, or well under 1 W in typical 2D applications.

S3 has priced the Virge/MXi at $54 in 10,000-unit quantities, and it expects the part to be available in 1H98. At the Forum, S3's Ronda Collier said the company's embedded DRAM technology will support 128-bit arrays operating at speeds in excess of 200 MHz, though the Virge/MXi runs its DRAM at just 85 MHz. The new array also lacks the write-per-bit and block-write features found in external SGRAMs, slightly reducing performance compared with a discrete solution. The Virge/MXi also lacks support for additional off-chip memory, putting it at a disadvantage for high-end notebooks, but the new chip should be a popular choice for midrange machines. —*P.N.G.*

Corollary Acquisition Boosts Intel Server Plans

With an eye on high-end servers, Intel has agreed to acquire multiprocessor pioneer Corollary *(www.corollary.com)*, providing a standard solution for eight-way Pentium II system designs. Corollary has been the leading supplier of PC-based multiprocessor technology; it currently licenses its C-bus II (see MPR 8/21/91, p. 1) design for eight-way Pentium systems to companies including Data General, Hitachi, Fujitsu, IBM, NEC, and, in a recent announcement, Compaq. The privately held company, which has 80 employees, was acquired for an undisclosed sum.

Corollary is developing a new design, called Profusion (see MPR 9/16/96, p. 9), that connects two four-processor Pentium II buses with two 630-pin ASICs that bridge the two buses together, provide a shared memory controller, and drive a third P6 bus for I/O devices.

The initial Profusion design, intended for Pentium Pro, is not yet complete and is unlikely to become a product. A faster version for Pentium II is planned for 1998. Intel presumably will offer eight-way Deschutes-based motherboards based on this design. Following Corollary's business model, Intel also will offer the board design for license to companies that want to make their own modifications. The ASICs themselves will not be offered as separate products.

The acquisition supports Intel's strategy of moving its processors into progressively larger systems. Intel has so far focused on four-way systems with its own technology and has left it to OEMs and third parties to provide technology for larger systems; Corollary's chip set will allow Intel to produce its own eight-way boards and make it easier for others to do so. Intel is also, no doubt, looking forward to Merced; Corollary already had a Merced version of Profusion in its product plans. Separately, Intel is investigating high-speed serial-bus approaches for creating larger multiprocessor clusters. —*M.S.*

LPC Offers Low-Cost ISA Replacement

Intel's new Low Pin Count (LPC) interface is designed to replace ISA/X-bus connections between core-logic chip sets and legacy I/O devices, saving at least 30 pins on these devices and reducing overall system cost. LPC is indeed a low-pin-count interface, requiring only a 4-bit, 33-MHz bidirectional bus and one new framing signal. LPC also uses the existing PCI clock and reset signals, along with up to six optional signals for peripherals with bus mastering, DMA, or power-management features.

The new LPC 1.0 specification *(developer.intel.com/design/pcisets/lpc/index.htm)* is intended for use only with super-I/O, audio, BIOS memory, and system-management devices. Since LPC is intended to be an interim step to the elimination of all legacy buses in favor of PCI, USB, and 1394 solutions, Intel doesn't want chip vendors using it for new types of devices. The new bus is also meant for motherboard components only, so there will be no LPC cards or cables.

National Semiconductor has already announced an LPC-compatible super-I/O device, the PC87360, expected to sample by the end of this year. Without offering specific pin count or pricing information, National promises the PC87360 will reduce cost, power consumption, and board space compared with existing super-I/O products.

Intel's other goals for LPC were to match or improve on the latency and transfer rate of the existing ISA/X-bus interface, support the same types of transactions over a much larger address space (4G instead of 16M), and ensure software transparency. LPC devices may be accessed by software exactly as if they were legacy ISA/X-bus devices, providing compatibility with existing BIOS and operating-system code.

Achieving these goals with as few as five new signal pins is quite an accomplishment. Although LPC is likely to have a limited life in the PC market—just a few years, until BIOS, OS, and application software no longer require ISA-compatible peripherals, or these functions are integrated directly into core logic—its extreme low cost and excellent flexibility may give it a life of its own in other markets. —*P.N.G.* M