VRAM

256K x 4 DRAM WITH 512 x 4 SAM

FEATURES

- Industry standard pinout, timing and functions
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$, and HIDDEN
- 512-cycle refresh within 8ms
- Optional FAST PAGE MODE access cycles
- Dual port organization: 256K x 4 DRAM port
  512 x 4 SAM port
- No refresh required for Serial Access Memory
- Low power: 15mW standby; 275mW active, typical
- Fast access times – 80ns random, 25ns serial

SPECIAL FUNCTIONS

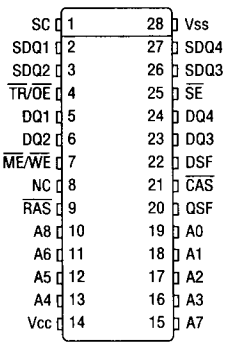
- JEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER

OPTIONS / MARKING

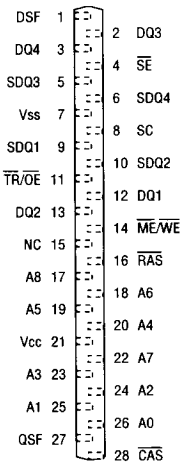
• Timing (DRAM, SAM)	
80ns, 25ns	- 8
100ns, 30ns	-10
120ns, 35ns	-12
• Packages	
Plastic SOJ	DJ
Plastic ZIP	Z

PIN ASSIGNMENT (Top View)

28-Pin SOJ
(E-9)



28-Pin ZIP
(C-5)



GENERAL DESCRIPTION

The MT42C4255 is a high speed, dual port CMOS dynamic random access memory or video RAM (VRAM) containing 1,048,576 bits. These bits may be accessed either by a 4-bit wide DRAM port or by a 512 x 4-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4-bit DRAM). Four 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 4-bit random access I/O port, the four internal 512 bit wide paths between the DRAM and the SAM, and the 4-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{\text{RAS}}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C4255 is compatible with (and can be identical to) the operation of the MT42C4064 (64K x 4 VRAM). However, the MT42C4255 offers several additional functions that may be used to increase system performance or ease critical timing requirements. These "special functions" are described in detail in the following section.

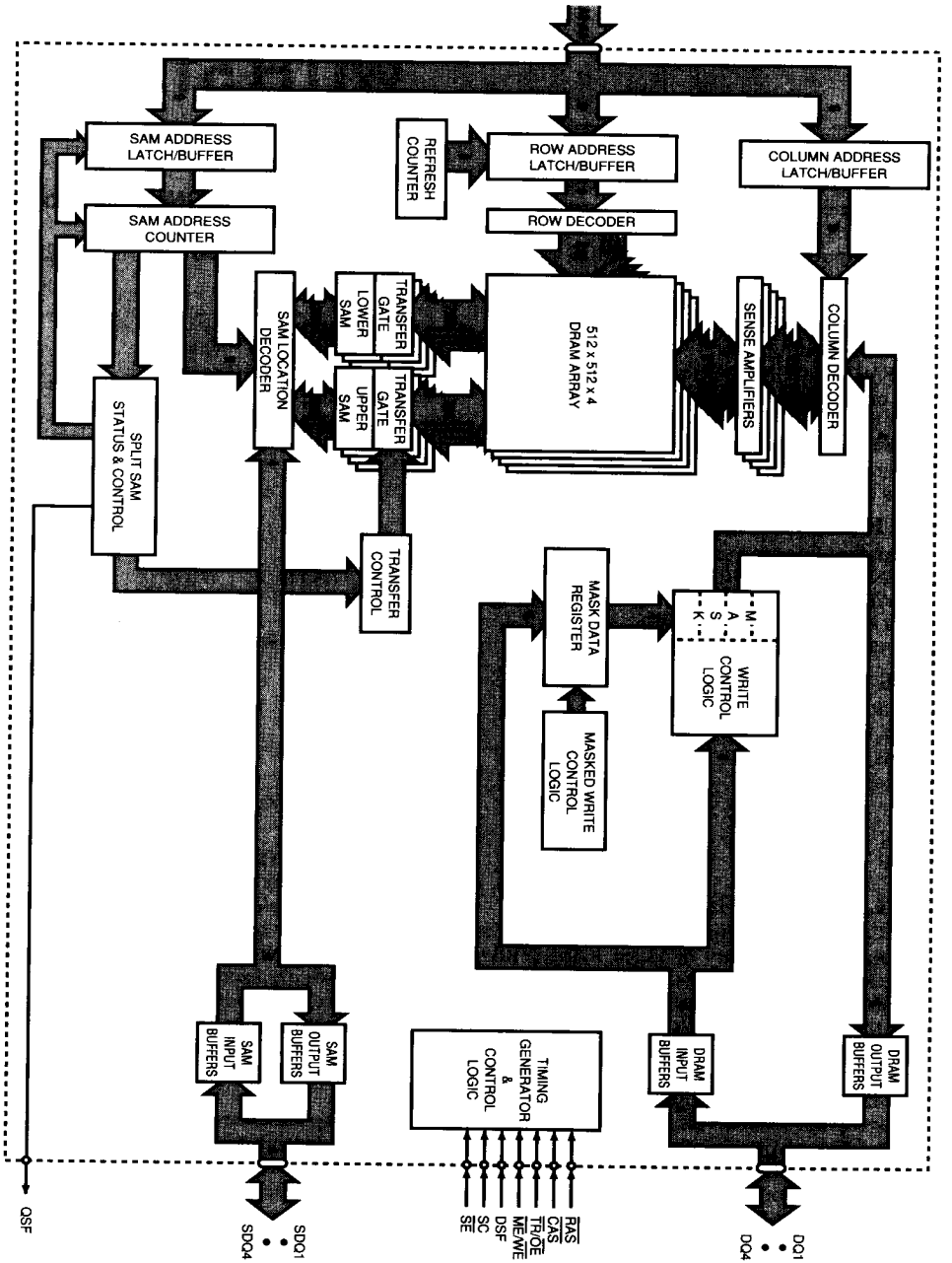


Figure 1
MT42C4255 BLOCK DIAGRAM

PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	8	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
4	11	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in the High-Z state.
7	14	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$ a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
25	4	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in the High-Z state. $\overline{SE}$ is also used during a WRITE TRANSFER operation to indicate whether a WRITE TRANSFER or a PSEUDO WRITE TRANSFER cycle is performed.
22	1	DSF	Input	Special Function Select: DSF is used to indicate which special functions (MASKED WRITE vs. PERSISTENT MASKED WRITE, etc.) are used on a particular access cycle.
9	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 9 row-address bits and as a strobe for the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, and DQ inputs.
21	28	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 9 column-address bits and enable the DRAM output buffers (DQs) (along with $\overline{TR/OE}$).
19, 18, 17, 16, 13, 12, 11, 15, 10	26, 25, 24, 23, 20, 19, 18, 22, 17	A0 to A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select 4 bits out of the 262,144 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and the SAM start address (when $\overline{CAS}$ goes LOW). A8 = "don't care" for the start address when doing SPLIT TRANSFERS.
5, 6, 23, 24	12, 13, 2, 3	DQ1 - DQ4	Input/ Output	DRAM Data I/O: Data Input/Output for DRAM cycles; inputs for the LOAD MASK REGISTER cycles.
2, 3, 26, 27	9, 10, 5, 6	SDQ1 - SDQ4	Input/ Output	Serial Data I/O: Input/Output for SAM access cycles or High-Z, when $\overline{SE}$ = HIGH.
20	27	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address 0 to 255, HIGH if address 256 to 511.
8	15	NC	–	No Connect: This pin should be left either unconnected or tied to ground.
14	21	Vcc	Supply	Power Supply: +5V ±10%
28	7	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C4255 may be divided into three functional blocks (see Figure 1): the DRAM, the transfer circuitry, and the serial access memory (SAM). All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing transfer operations the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM based memory, the MT42C4255 VRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 8ms. The MT42C4255 supports $\overline{CAS}$-BEFORE-$\overline{RAS}$, $\overline{RAS}$-ONLY and HIDDEN types of refresh cycles.

For the $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and simply must perform 512 $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles within the 8ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for $\overline{RAS}$-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the $\overline{RAS}$-ONLY and $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles.

HIDDEN REFRESH cycles are performed by toggling $\overline{RAS}$ (and keeping $\overline{CAS}$ LOW) after a READ or WRITE cycle. This performs $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM portion of the MT42C4255 is fully static and does not require any refreshing.

DRAM READ AND WRITE CYCLES

The DRAM portion of the VRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has several special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select a 4-bit word from the 262,144 available are latched into the chip using the A0-A8, $\overline{RAS}$ and $\overline{CAS}$ inputs. First, the 9 row-address bits are set-up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH to LOW. Next, the 9 column-address bits are set-up on the address inputs and clocked-in when $\overline{CAS}$ goes from HIGH to LOW.

For single port DRAMS, the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. However, for the VRAM, when $\overline{RAS}$ goes LOW, $(\overline{TR})/\overline{OE}$ selects between DRAM access or TRANSFER cycles. $(\overline{TR})/\overline{OE}$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition for all DRAM operations (except $\overline{CAS}$-BEFORE-$\overline{RAS}$).

If $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ4 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH to LOW sometime after $\overline{RAS}$ falls to enable the DRAM output port.

For single port normal DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the VRAM, $\overline{ME}/(\overline{WE})$ is used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If $\overline{ME}/(\overline{WE})$ is LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any DRAM access cycle (READ or WRITE), $\overline{ME}/(\overline{WE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition. If $(\overline{ME})/\overline{WE}$ is LOW before $\overline{CAS}$ goes LOW, a DRAM EARLY-WRITE operation is performed and the data present on the DQ1-DQ4 data port will be written into the selected memory cells. If $(\overline{ME})/\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW, a DRAM LATE-WRITE operation is performed. Refer to the AC timing diagrams.

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

NONPERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only specific bits within a 4-bit word. The MT42C4255 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}$/($\overline{WE}$) and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a NONPERSISTENT MASKED WRITE is performed and the data (mask data) present on the DQ1-DQ4 inputs will be written into the mask data register. The mask data acts as an individual WRITE ENABLE for each of the four DQ1-DQ4 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ4 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The MASKED WRITE is non-persistent (must be re-entered at every $\overline{RAS}$ cycle) if DSF is LOW when $\overline{RAS}$ goes LOW. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE. FAST PAGE MODE can be used with NONPERSISTENT MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle. An example NONPERSISTENT MASKED WRITE cycle is shown in Figure 2.

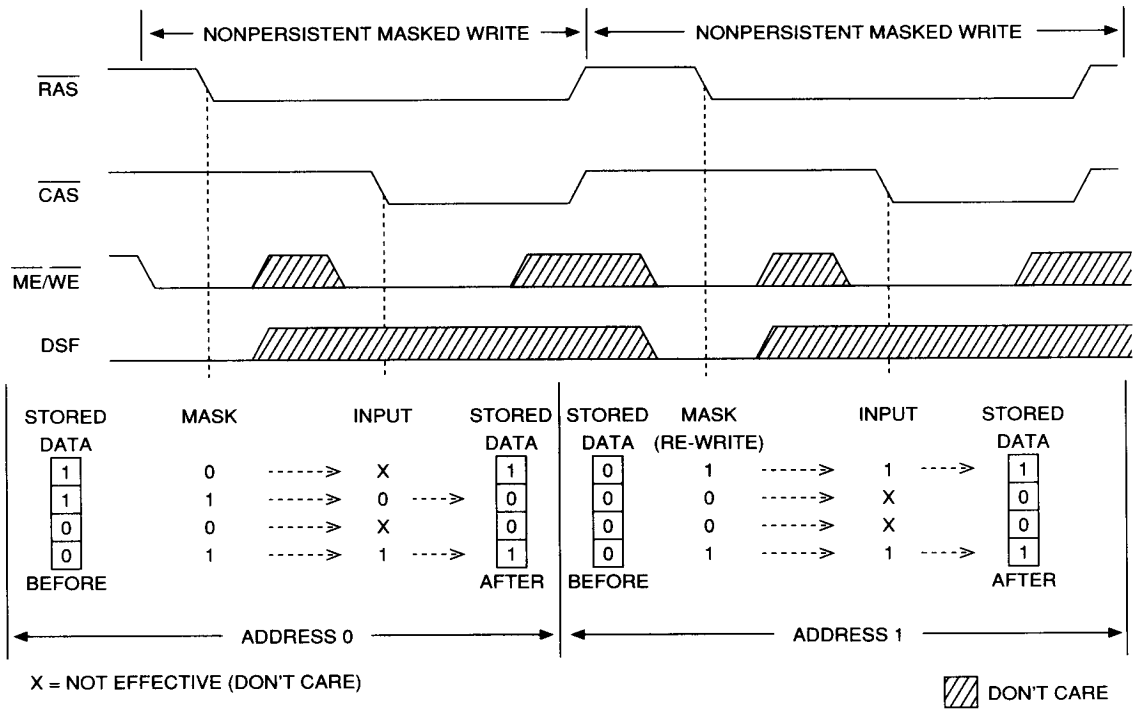


Figure 2
NONPERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF HIGH when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW. Mask data may also be loaded into the mask register by performing a NONPERSISTENT MASKED WRITE before the PERSISTENT MASKED WRITE.

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ LOW and DSF HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE, the data present on the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls, and the mask data register will not be cleared at the end of the cycle. Any number of PERSISTENT MASKED WRITE cycles, to any address, may be performed without having to reload the mask data register. Figure 3 shows the LOAD MASK REGISTER and two PERSISTENT MASKED WRITE cycles in operation. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow controllers that cannot provide mask data to the DQ pins at $\overline{RAS}$ time to perform MASKED WRITE operations. PERSISTENT MASKED WRITE operations can be performed during FAST PAGE MODE and the same mask will apply to all addressed columns in the addressed row.

LOAD MASK DATA REGISTER

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a REGISTER load cycle. DSF is used when $\overline{CAS}$ goes LOW to select the register to be loaded and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: *For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless NONPERSISTENT MASKED WRITE or LOAD MASK REGISTER cycles are performed.*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE cycles to selectively enable writes to the four DQ planes.

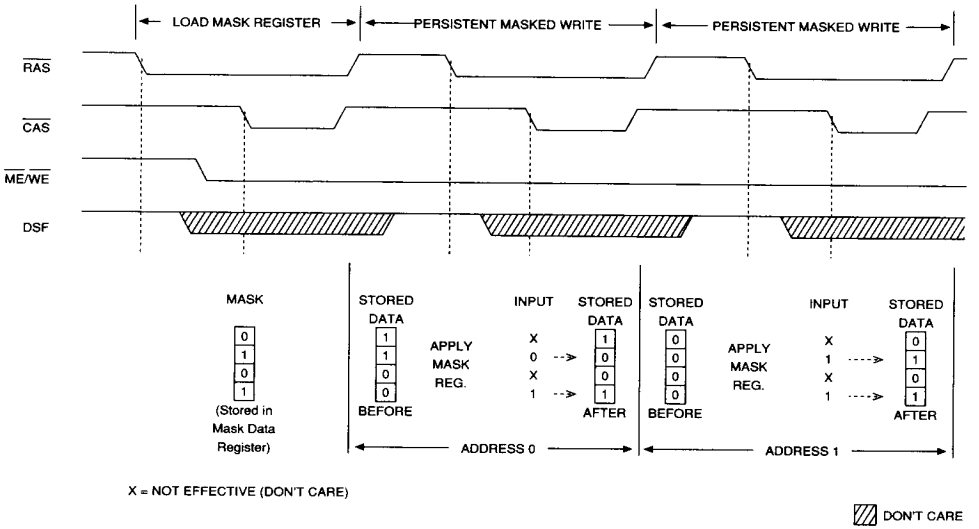


Figure 3
PERSISTENT MASKED WRITE EXAMPLE

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW then $\overline{RAS}$ goes LOW. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER, SPLIT READ TRANSFER, and ALTERNATE WRITE TRANSFER cycles. Each of the TRANSFER cycles available is described below.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate the four 512-bit DRAM row planes that are to be transferred to the four SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished two ways. If the transfer is to be synchronized with SC (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW (refer to the AC Timing Diagrams). The 2048 bits of DRAM data are written into the SAM data registers and the serial shift start address is stored in an internal 9-bit register. QSF will be LOW if access is from the lower half (addresses 0 through 255), and HIGH if access is from the upper half (256 through 511). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

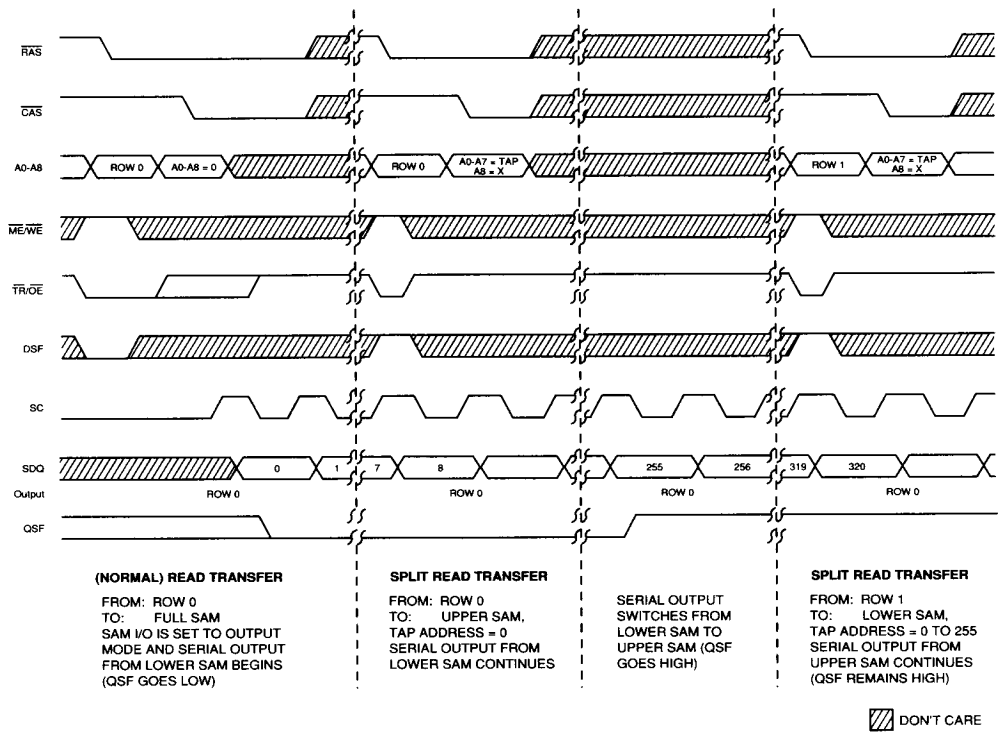


Figure 5
TYPICAL SPLIT READ TRANSFER INITIATION SEQUENCE

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the REAL-TIME READ TRANSFER cycle has to occur immediately after the last bit of "old data" was clocked out of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data can be transferred to the other half. The transfer can occur at any time while the other half is sending data and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of $\overline{RAS}$ or $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles.

A normal, non-split READ TRANSFER cycle must precede any sequence of SPLIT READ TRANSFER cycles to provide a reference to which half of the SAM the access will begin. Then SPLIT READ TRANSFERS may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in non-split transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH to LOW transition of $\overline{CAS}$. It is internally generated so that the SPLIT TRANSFER will be to the SAM half not currently being accessed.

Figure 5 shows a typical SPLIT READ TRANSFER initiation sequence. The normal READ TRANSFER is first performed, followed by a SPLIT READ TRANSFER of the same row to the upper half of the SAM. The purpose of the SPLIT TRANSFER of the same data is to initiate the split SAM operating mode and load the Tap address. Serial access continues, and when the SAM address counter reaches 255 ("A8"=0, A0-A7=1) the new Tap address is loaded for the next half ("A8"=1, A0-A7=Tap) and the QSF output goes HIGH. Once the serial access has switched to the upper SAM, new data may be transferred to the lower SAM. The controller must wait for the state of QSF to change and then the new data may be transferred to the SAM half not being accessed. For example, the next step in Figure 5 would be to wait until QSF went LOW (indicating that row-1 data is shifting out the lower SAM) and then transfer the upper half of row 1 to the upper SAM.

WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously, except $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A WRITE TRANSFER changes the direction of the SAM I/O buffers to the input mode. QFS is LOW if access is to the lower half of the SAM, and HIGH if access is to the upper half.

PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)

The PSEUDO WRITE TRANSFER cycle is used to change the direction of SAM port from output to input without performing a WRITE TRANSFER cycle. A PSEUDO WRITE TRANSFER is a WRITE TRANSFER with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the ALTERNATE WRITE TRANSFER is identical to the WRITE TRANSFER except that the DSF pin is HIGH and $(\overline{ME})/\overline{WE}$ is LOW when $\overline{RAS}$ goes LOW, allowing $\overline{SE}$ to be a "don't care." This allows the outputs to be disabled using $\overline{SE}$ during a WRITE TRANSFER cycle.

POWER UP AND INITIALIZATION

When Vcc is initially supplied or when refresh is interrupted for more than 8ms, the MT42C4255 must be initialized.

After Vcc is at specified operating conditions, for 100µs minimum, 8 $\overline{RAS}$ cycles and 1 SC cycle must be executed to initialize the memory array. When the device is initialized, the DRAM I/O pins (DQs) are in a High-Z state, regardless of the state of $(\overline{TR})/\overline{OE}$. The DRAM array will contain random data.

The SAM portion of the MT42C4255 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the serial input mode (WRITE TRANSFER) and the I/O pins (SDQ's) will be High- Z, regardless of the state of $\overline{SE}$a,b. The mask register will contain random data after power-up.

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE					A0 - A8[1]		DQ1 - DQ4[2]		MASK REGISTER
		CAS	TR/OE	ME/WE	DSF	SE	RAS	CAS A8=X	RAS	CAS[3]	
	DRAM OPERATIONS										
CBR	CAS-BEFORE-RAS REFRESH	0	X	X	X	X	—	X	—	X	X
ROR	RAS-ONLY REFRESH	1	1	X	X	X	ROW	—	X	—	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	X	ROW	COLUMN	X	VALID DATA	X
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	X	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	X	ROW	COLUMN	X	VALID DATA	USE
	REGISTER OPERATIONS										
LMR	LOAD MASK REGISTER	1	1	1	1	X	ROW[4]	X	X	WRITE MASK	LOAD
	TRANSFER OPERATIONS										
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	ROW	TAP[5]	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	ROW	TAP[5]	X	X	X
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	ROW	TAP[5]	X	X	X
PWT	PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)	1	0	0	0	1	ROW[4]	TAP[5]	X	X	X
AWT	ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	1	X	ROW	TAP[5]	X	X	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ4 inputs when RAS falls and when CAS falls.
3. On WRITE cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is latched at the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
5. This is the first SAM address location that the first SC cycle will access. For Split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for lower half, 511 for upper half).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Operating Temperature, Ta(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0V)	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, SC, $\overline{SE}$, DSF	C_{I2}		8	pF	2
Input/Output Capacitance: DQ, SDQ	$C_{I/O}$		9	pF	2
Output Capacitance: QSF	C_O		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-8**	**-10**	**-12**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC1}	90	80	70	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC2}	70	60	50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH} after 8 $\overline{RAS}$ cycles min)	I_{CC3}	10	10	10	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH})	I_{CC4}	90	80	70	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling)	I_{CC5}	80	70	60	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC6}	95	85	75	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-8**	**-10**	**-12**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC7}	130	120	110	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC8}	110	100	90	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH} after 8 $\overline{RAS}$ cycles min)	I_{CC9}	50	45	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH})	I_{CC10}	130	120	110	mA	3, 4
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling)	I_{CC11}	120	110	100	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC12}	135	125	115	mA	3, 4

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		180		210		ns	
READ-MODIFY-WRITE cycle time	^tRWC	205		235		280		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	45		55		65		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	tPRWC	100		110		140		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		25		30		35	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	^tOE		20		25		30	ns	
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55		65	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		30		35		ns	
$\overline{RAS}$ precharge time	^tRP	60		70		80		ns	
$\overline{CAS}$ pulse width	^tCAS	25	10,000	30	10,000	35	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	55	20	70	25	85	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	12		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	17	40	20	50	20	60	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	20		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		85		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	30	ns	20, 23
Output Disable	^tOD	0	20	0	20	0	30	ns	23
Output Disable hold time from start of write	^tOEH		15		15		20	ns	27
Output Enable to $\overline{RAS}$ delay	^tORD		0		0		0	ns	

DRAM TIMING PARAMETERS (Continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		70		85		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	20		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		70		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	110		130		160		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	70		80		100		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	55		60		65		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	30		30		30		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	12		15		15		ns	
Mask Data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	
Mask Data to $\overline{RAS}$ hold time	^tMH	12		15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
TRANSFER command to $\overline{RAS}$ setup time	^tTLS	0		0		0		ns	25
TRANSFER command to $\overline{RAS}$ hold time	^tTLH	12	10,000	15	10,000	15	10,000	ns	25
TRANSFER command to $\overline{RAS}$ hold time (REAL-TIME READ TRANSFER only)	^tRTH	70	10,000	80	10,000	90	10,000	ns	25
TRANSFER command to $\overline{CAS}$ hold time (REAL-TIME READ TRANSFER only)	^tCTH	20		25		30		ns	25
TRANSFER command to column address hold time (for REAL TIME READ TRANSFER only)	^tATH	25		30		35		ns	25
TRANSFER command to SC lead time	^tTSL	5		5		5		ns	25
TRANSFER command to $\overline{RAS}$ lead time	^tTRL	0		0		0		ns	25
TRANSFER command to $\overline{RAS}$ delay time	^tTRD	15		15		15		ns	25
TRANSFER command to $\overline{CAS}$ time	^tTCL	0		0		0		ns	25
TRANSFER command to $\overline{CAS}$ delay time	^tTCD	15		15		15		ns	25
First SC edge to TRANSFER command delay time	^tTSD	10		10		10		ns	25
Serial output buffer turn-off delay from $\overline{RAS}$	^tSDZ	10	35	10	40	10	50	ns	
SC to $\overline{RAS}$ setup time	^tSRS	30		30		40		ns	
$\overline{RAS}$ to SC delay time	^tSRD	20		25		30		ns	
Serial data input to $\overline{SE}$ delay time	^tSZE	0		0		0		ns	
$\overline{RAS}$ to SD buffer turn-on time	^tSRO	10		15		15		ns	
Serial data input delay from $\overline{RAS}$	^tSDD	45		50		55		ns	
Serial data input to $\overline{RAS}$ delay time	^tSZS	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	^tESR	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	^tREH	12		15		15		ns	
NONTRANSFER command to $\overline{RAS}$ setup time	^tYS	0		0		0		ns	26
NONTRANSFER command to $\overline{RAS}$ hold time	^tYH	12		15		15		ns	26
DSF to $\overline{RAS}$ setup time	^tFSR	0		0		0		ns	
DSF to $\overline{RAS}$ hold time	^tRFH	12		15		15		ns	
SC to QSF delay time	^tSQD		25		30		35	ns	
SPLIT TRANSFER setup time	^tSTS	30		35		40		ns	
SPLIT TRANSFER hold time	^tSTH	30		35		40		ns	
$\overline{RAS}$ to QSF delay time	^tRQD		65		85		105	ns	
$\overline{TR/OE}$ to QSF delay time	^tTQD		25		30		35	ns	
$\overline{CAS}$ to QSF delay time	^tCQD		35		40		45	ns	
$\overline{RAS}$ to first SC delay	^tRSD	80		95		105		ns	
$\overline{CAS}$ to first SC delay	^tCSD	20		25		35		ns	
Column address valid to first SC delay	^tASD	45		55		65		ns	

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

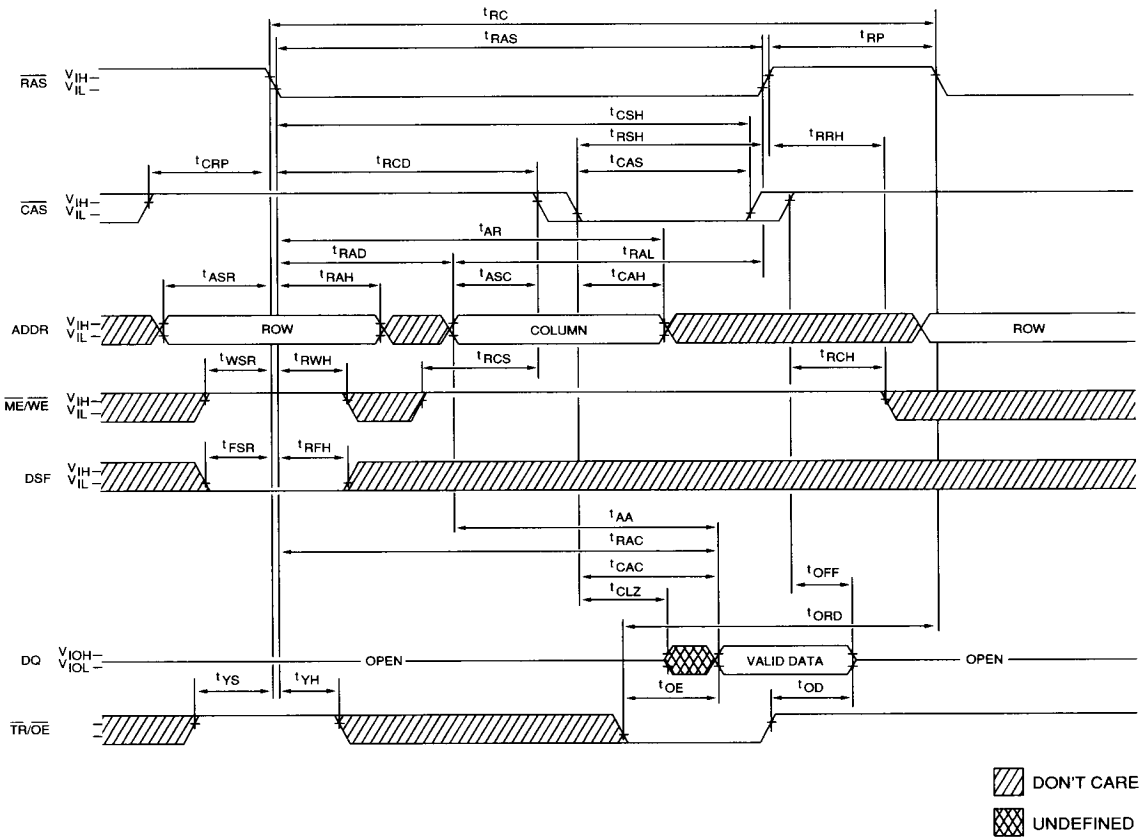
(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	25		30		35		ns	
Access time from SC	^tSAC		25		30		35	ns	24
SC precharge time (SC LOW time)	^tSP	10		10		12		ns	
SC pulse width (SC HIGH time)	^tSAS	10		10		12		ns	
Access time from $\overline{SE}$	^tSEA		15		20		30	ns	24
$\overline{SE}$ precharge time	^tSEP	10		15		15		ns	
$\overline{SE}$ pulse width	^tSE	10		15		15		ns	
Serial data-out hold time after SC high	^tSOH	5		5		5		ns	24
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	0	12	0	15	0	25	ns	24
Serial data-in setup time	^tSDS	0		0		0		ns	24
Serial data-in hold time	^tSDH	10		15		20		ns	24
SERIAL INPUT (Write) Enable setup time	^tSWS	0		0		0		ns	
SERIAL INPUT (Write) Enable hold time	^tSWH	10		15		20		ns	
SERIAL INPUT (Write) Disable setup time	^tSWIS	0		0		0		ns	
SERIAL INPUT (Write) Disable hold time	^tSWIH	10		15		20		ns	

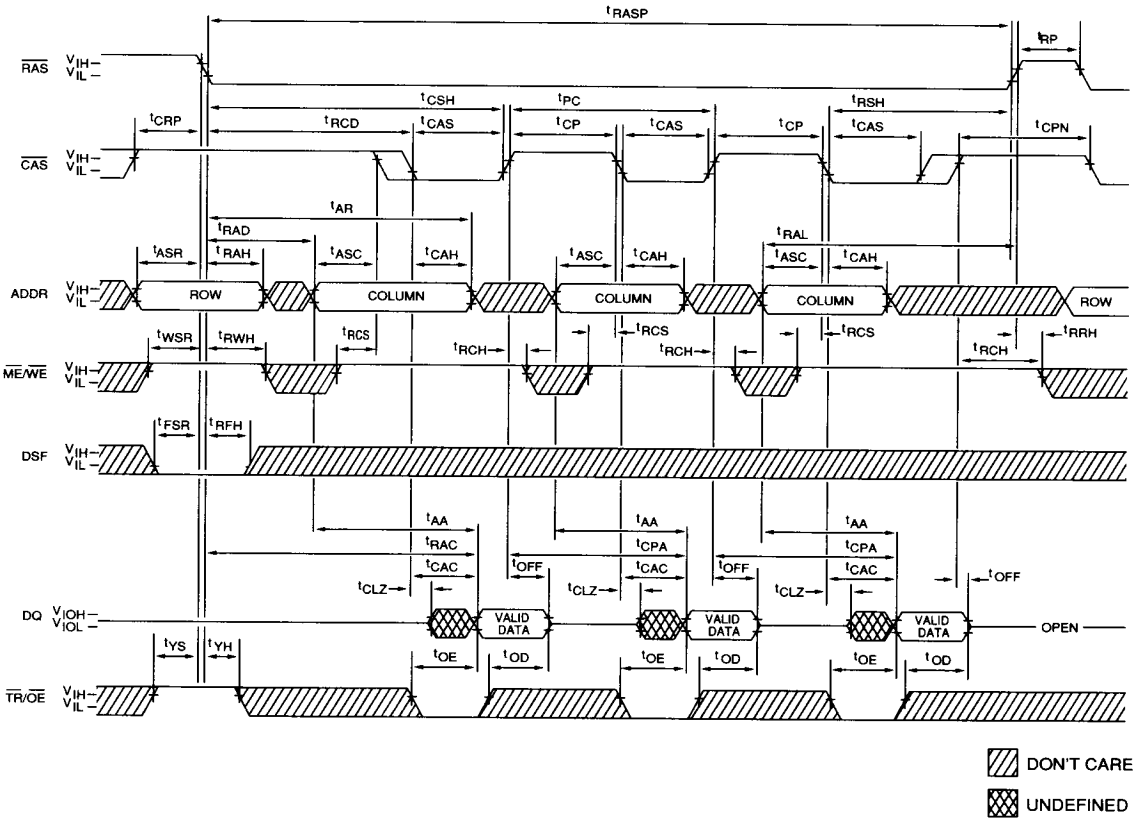
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles and 1 SC cycle before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, DRAM data output (DQ1-DQ4) is high impedance.
12. If $\overline{CAS} = V_{IL}$, DRAM data output (DQ1-DQ4) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 2 TTL gates and 100pF. Output reference levels: $V_{OH} = 2.4V$; $V_{OL} = 0.4V$.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^tWCS \le ^tWCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the write to avoid data contention. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 2 TTL gate and 50pF. Output reference levels: $V_{OH} = 2.0V$; $V_{OL} = 0.8V$.
25. TRANSFER command means that $\overline{TR}/\overline{OE}$ is LOW when $\overline{RAS}$ goes LOW.
26. NONTRANSFER command means that $\overline{TR}/\overline{OE}$ is HIGH when $\overline{RAS}$ goes LOW.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.

DRAM READ CYCLE



DRAM FAST-PAGE-MODE READ CYCLE



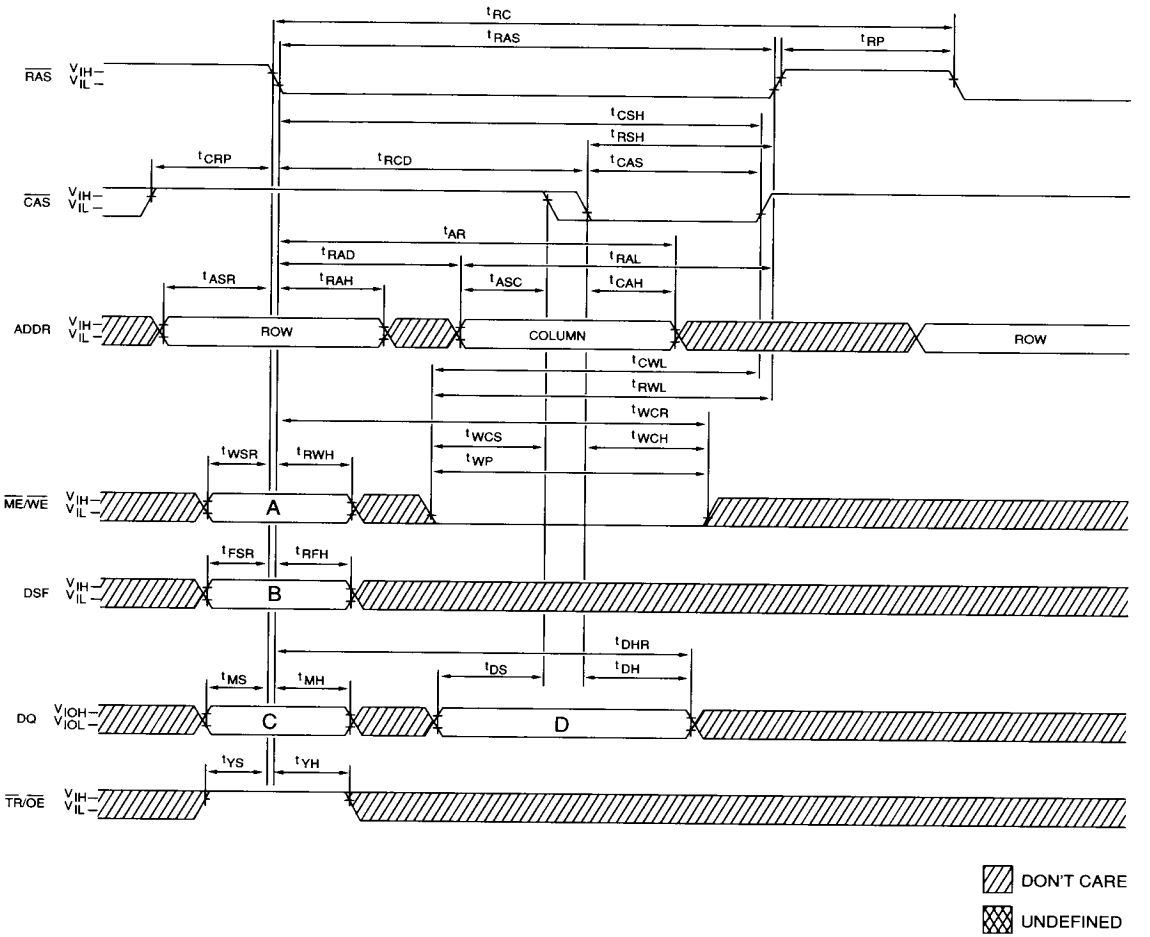
NOTE: WRITE or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST PAGE MODE.

WRITE CYCLE FUNCTION TABLE

LOGIC STATES				FUNCTION
RAS Falling Edge			CAS Falling Edge	
A ME/WE	B DSF	C DQ (Input)	D DQ (Input)	
1	0	X	DRAM Data	Normal DRAM WRITE
0	0	Write Mask	DRAM Data (Masked)	NONPERSISTENT (Load and Use Register) MASKED WRITE to DRAM
0	1	X	DRAM Data (Masked)	PERSISTENT (Use Register) MASKED WRITE to DRAM
1	1	X	Write Mask	Load Mask Register

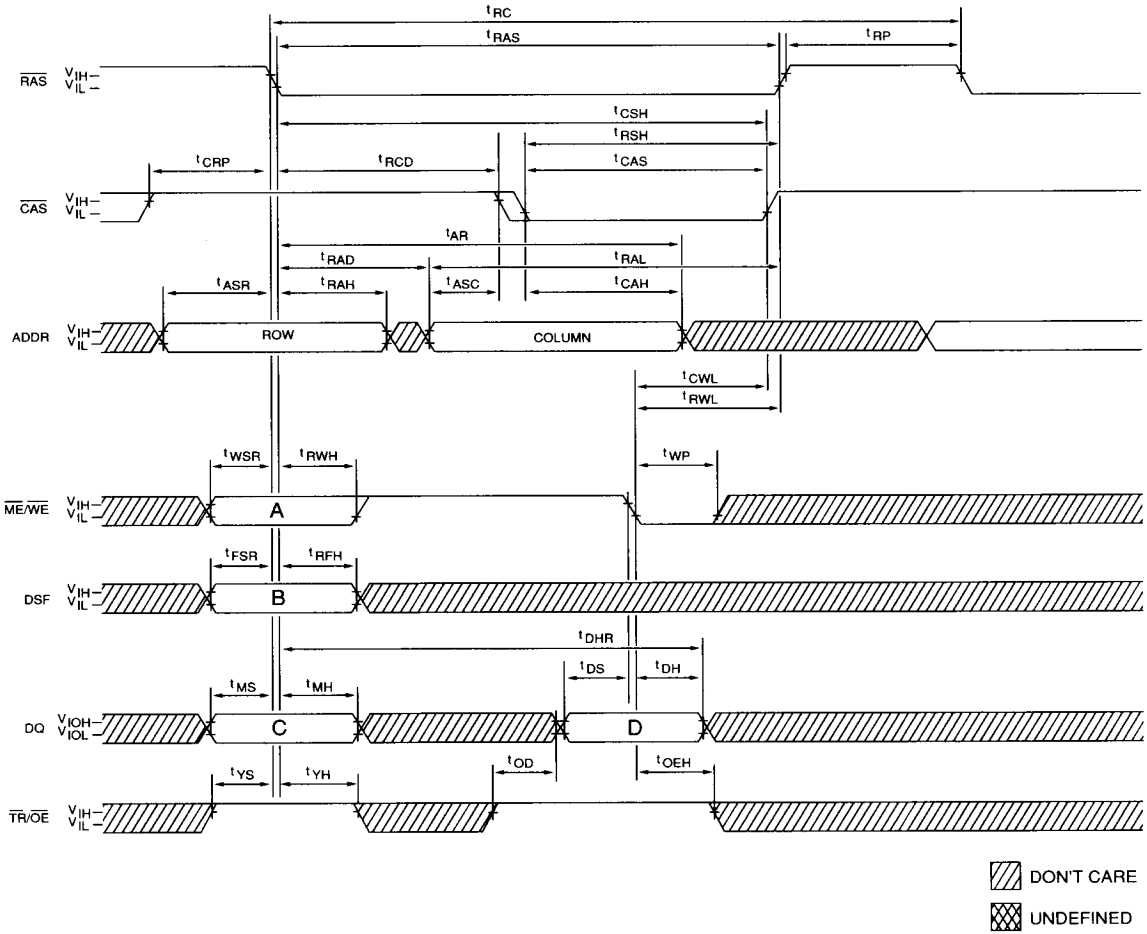
NOTE: Refer to this function table to determine the logic states of "A", "B", "C", and "D" for the WRITE cycle timing diagrams on the following pages.

DRAM EARLY-WRITE CYCLE



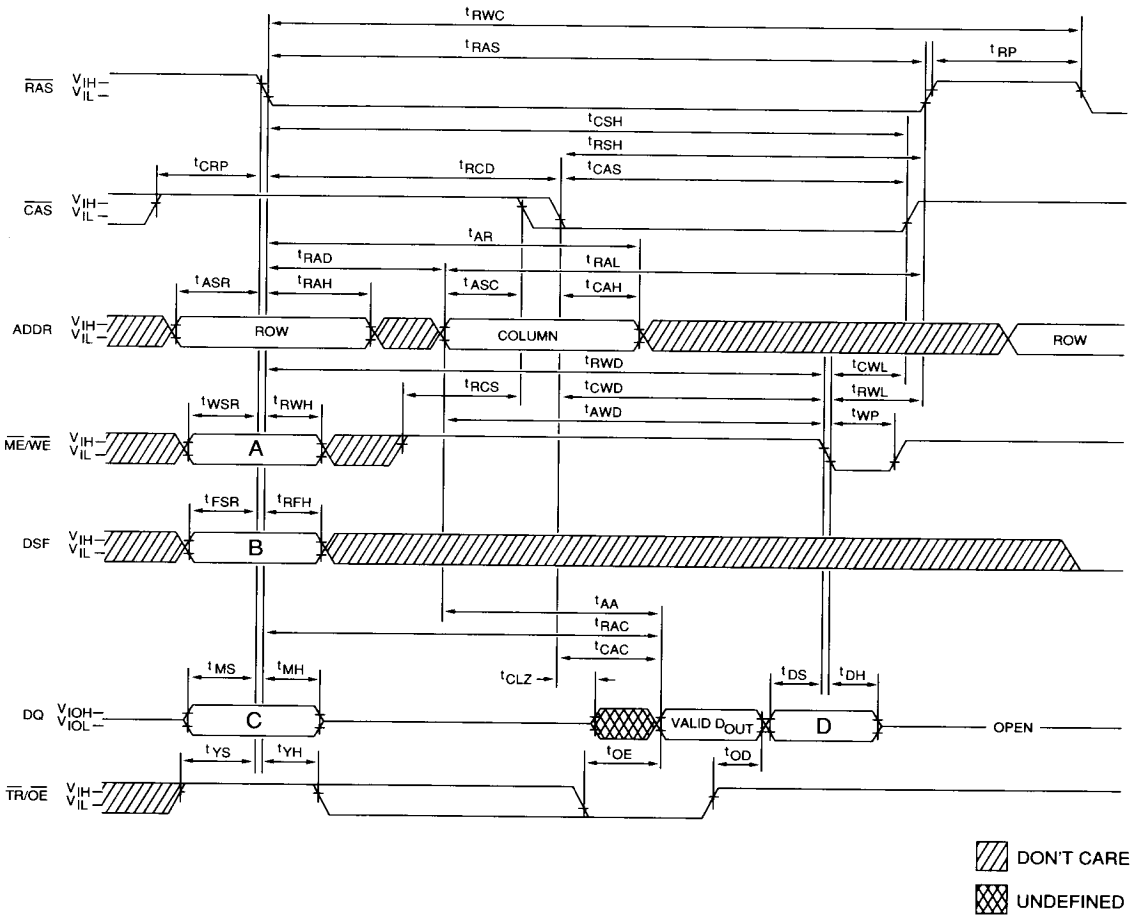
NOTE: The logic states of "A", "B", "C", and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM LATE-WRITE CYCLE



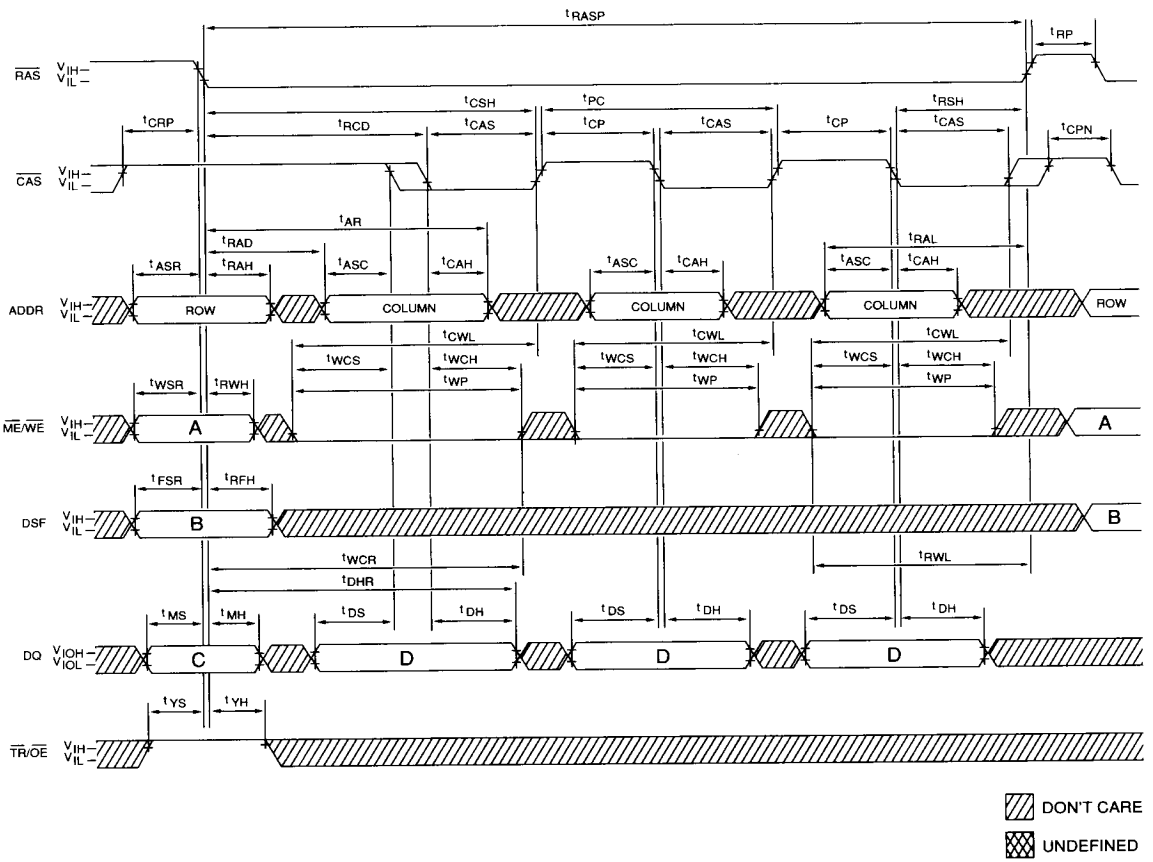
NOTE: The logic states of "A", "B", "C", and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



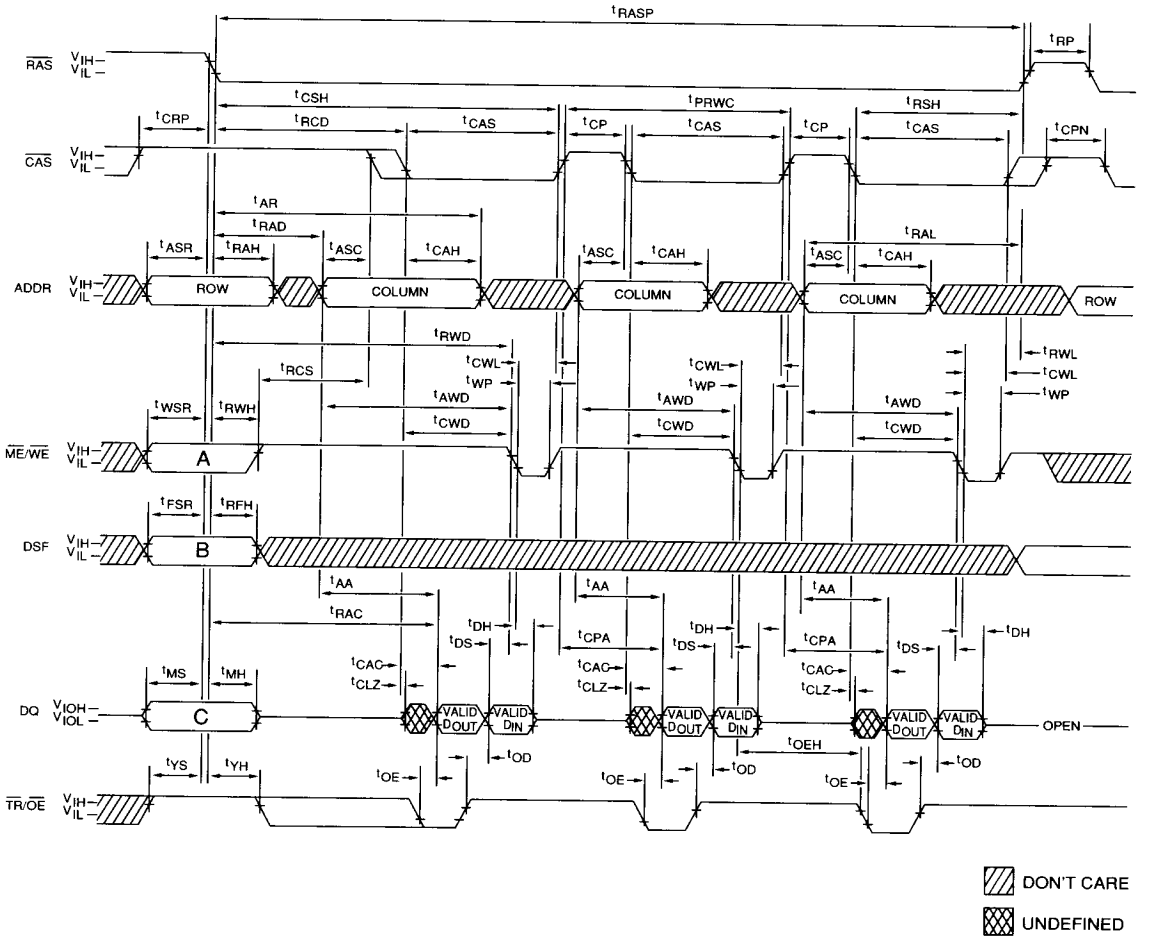
NOTE: The logic states of "A", "B", "C", and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



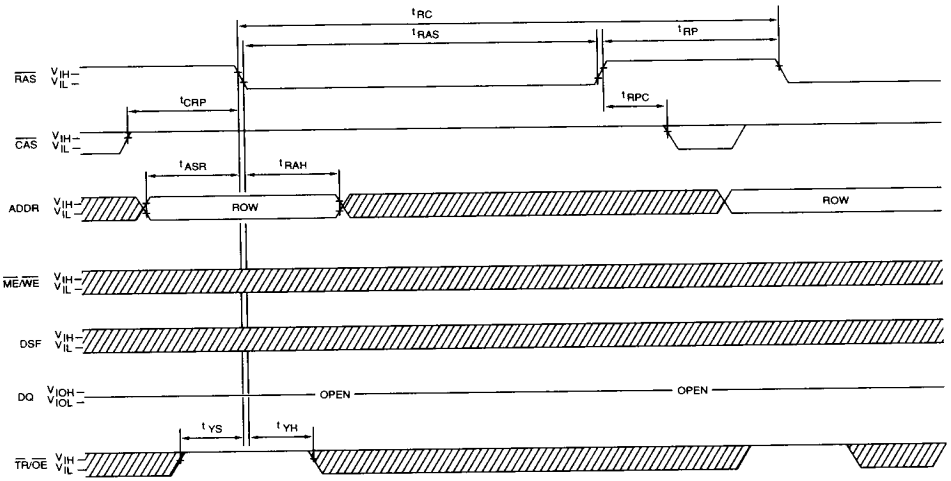
NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.
2. The logic states of "A", "B", "C", and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE or LATE-WRITE CYCLES)

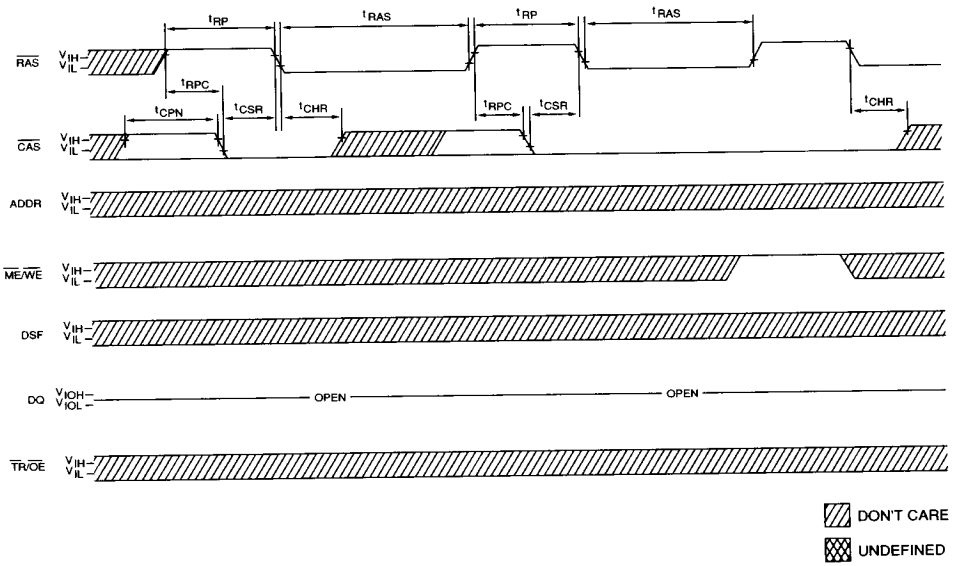


NOTE:
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

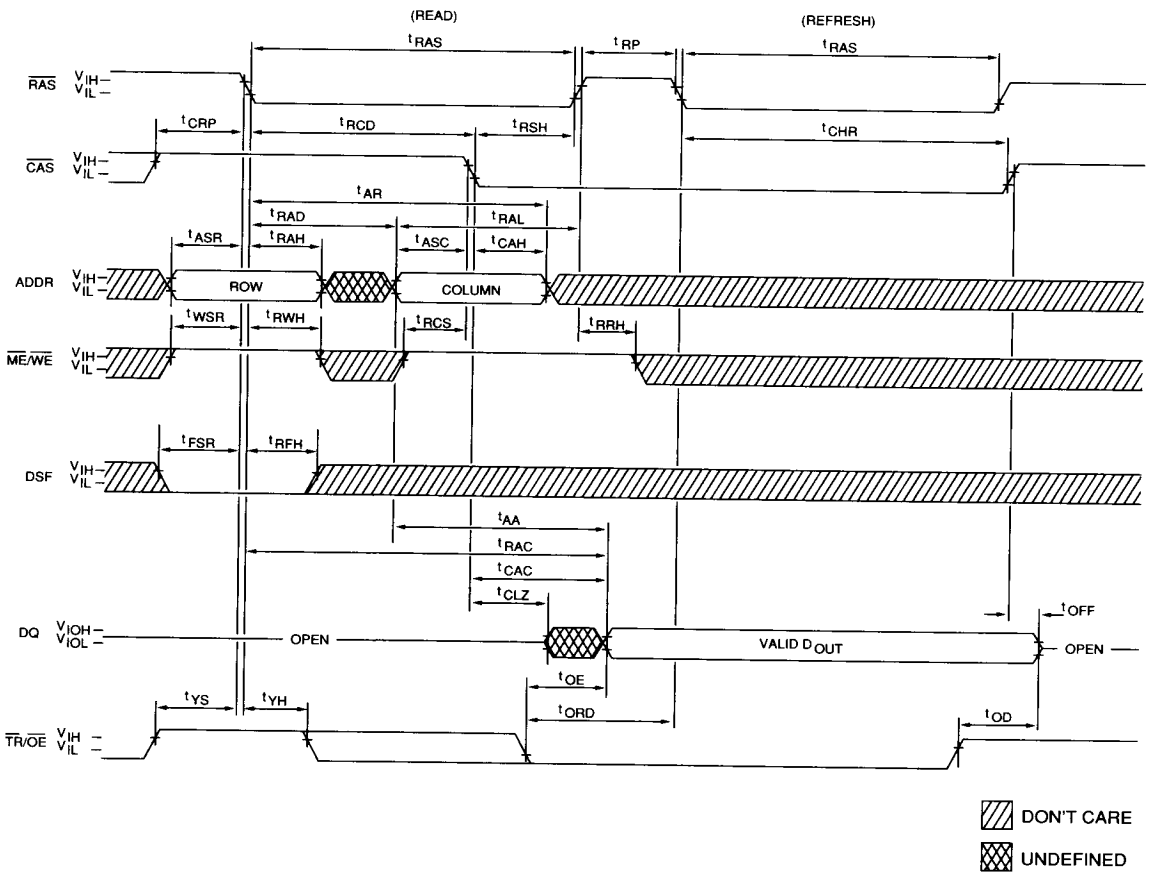
DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

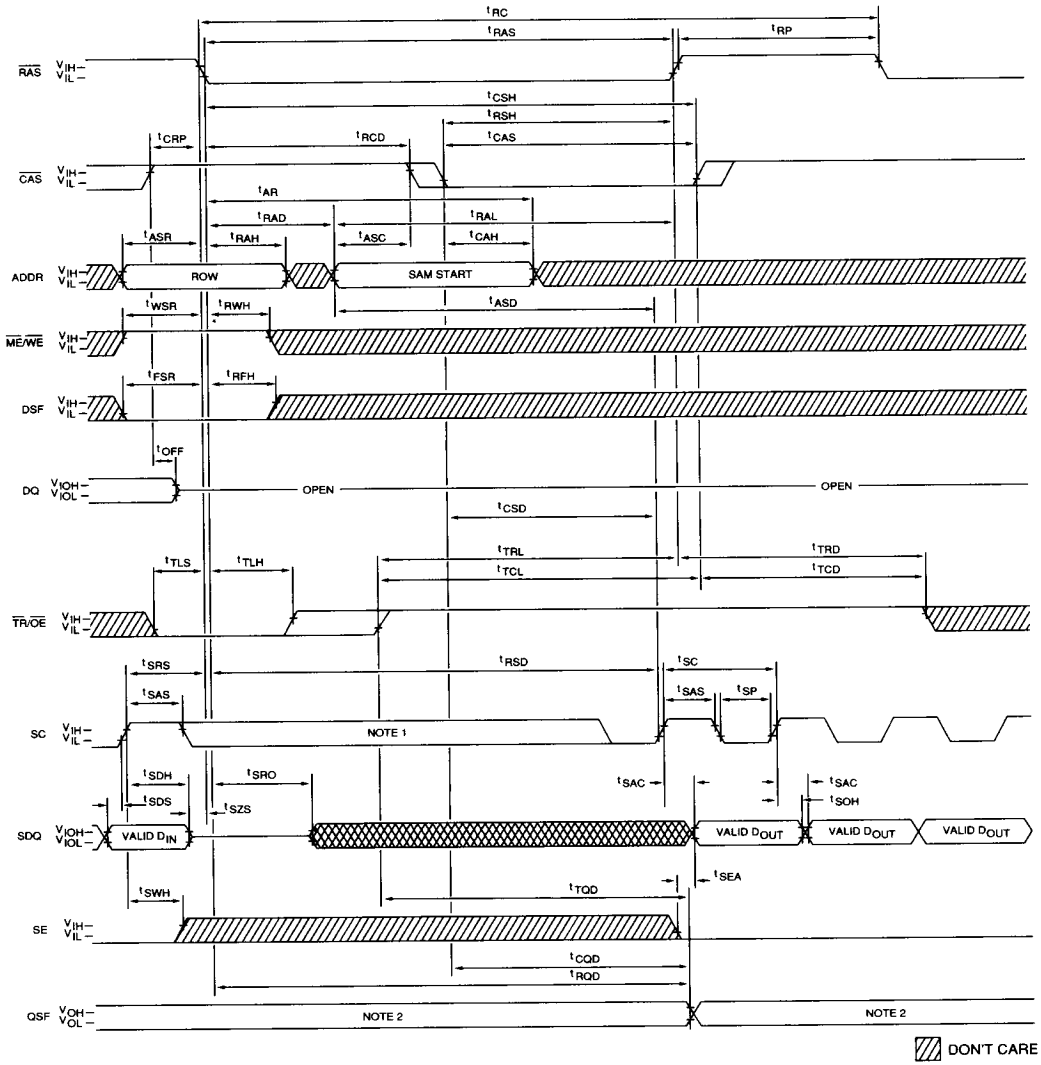


DRAM HIDDEN-REFRESH CYCLE



NOTE: A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.

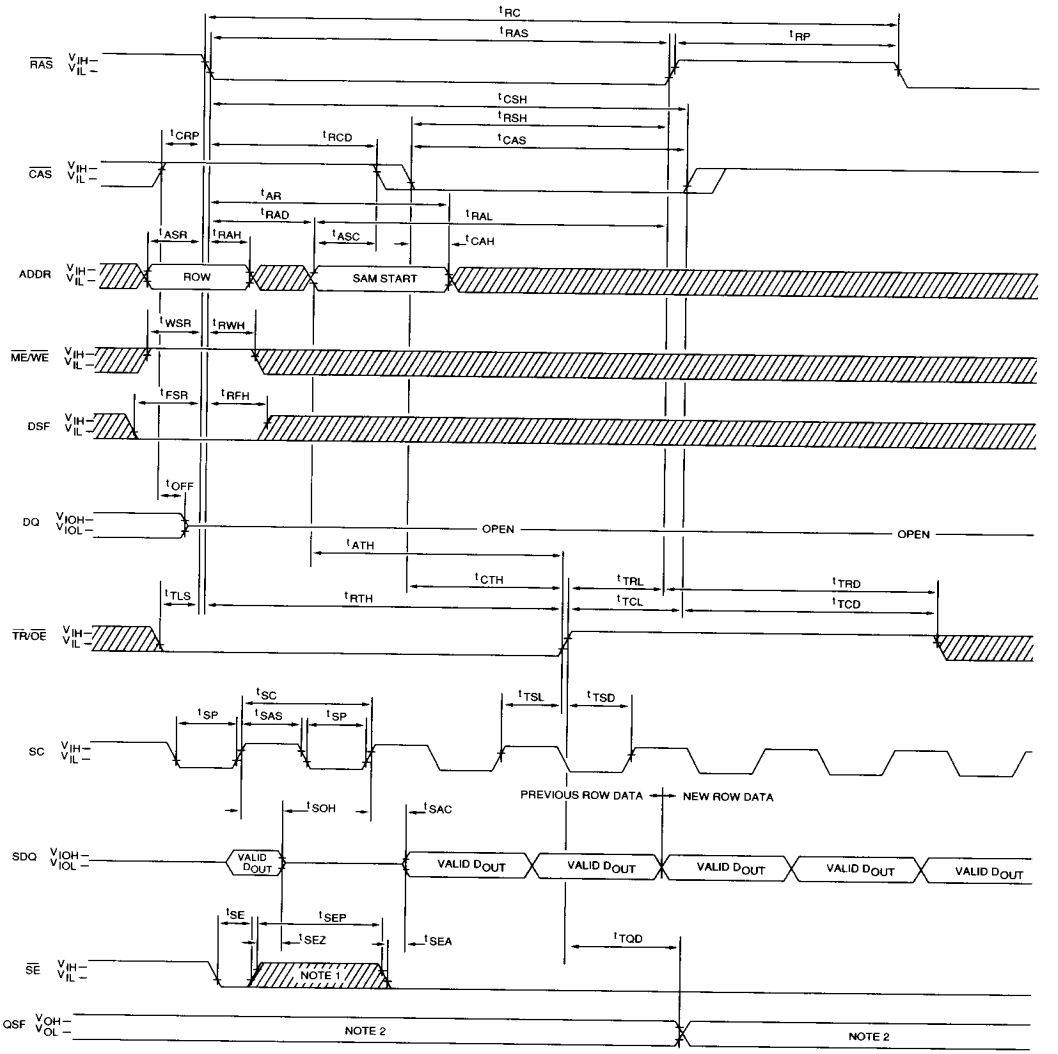
READ TRANSFER
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



NOTE: 1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

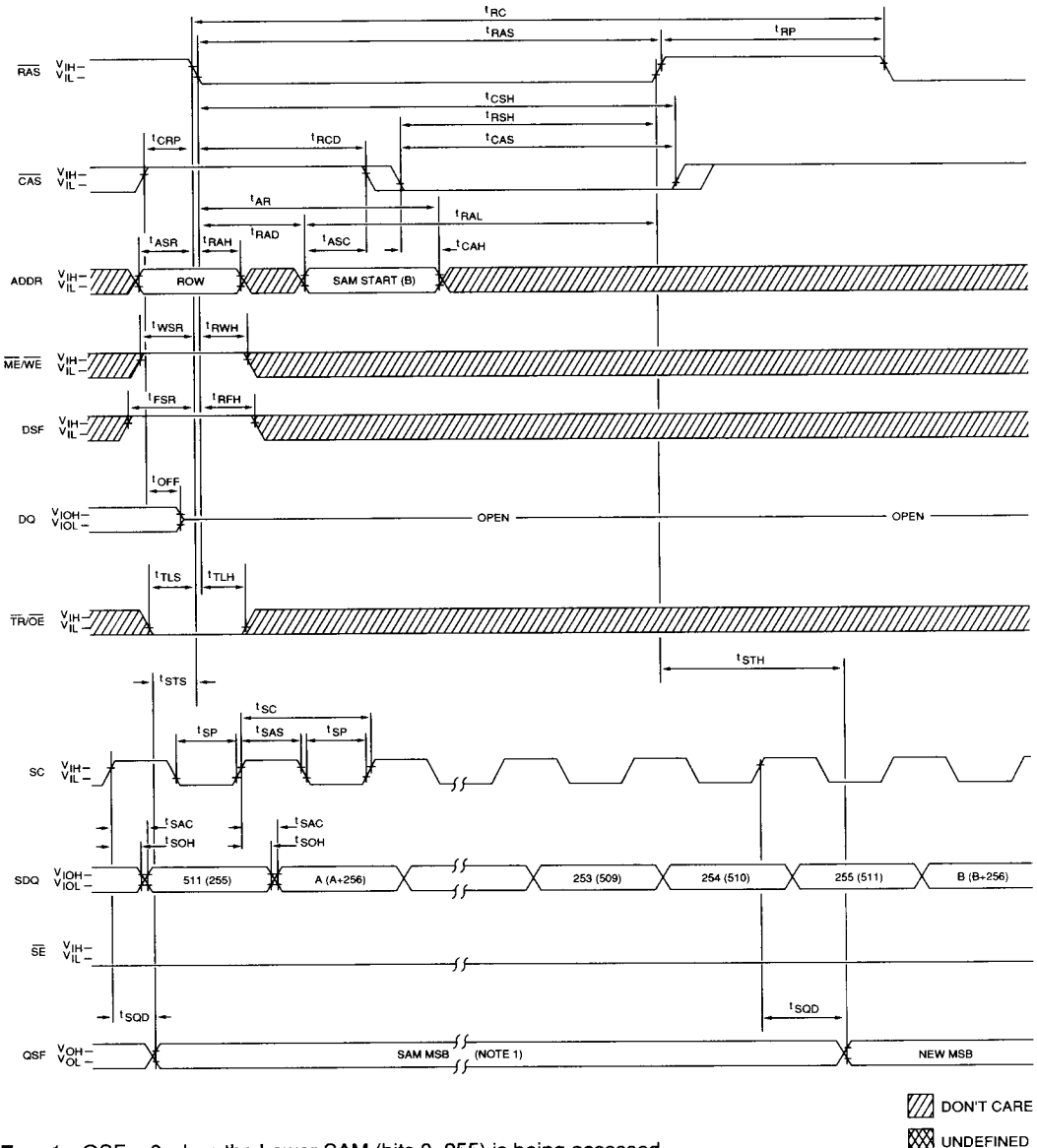
REAL-TIME READ TRANSFER (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



NOTE:
1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

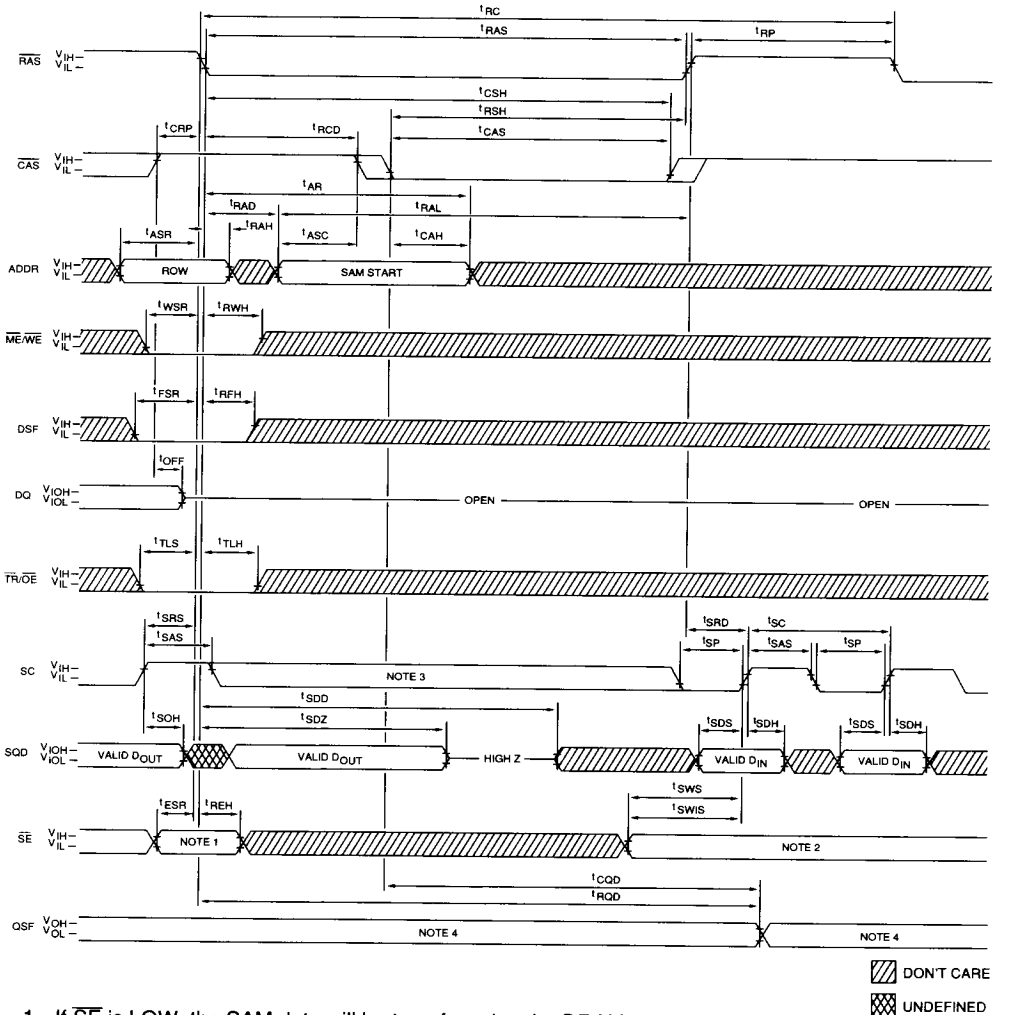
SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE: 1. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

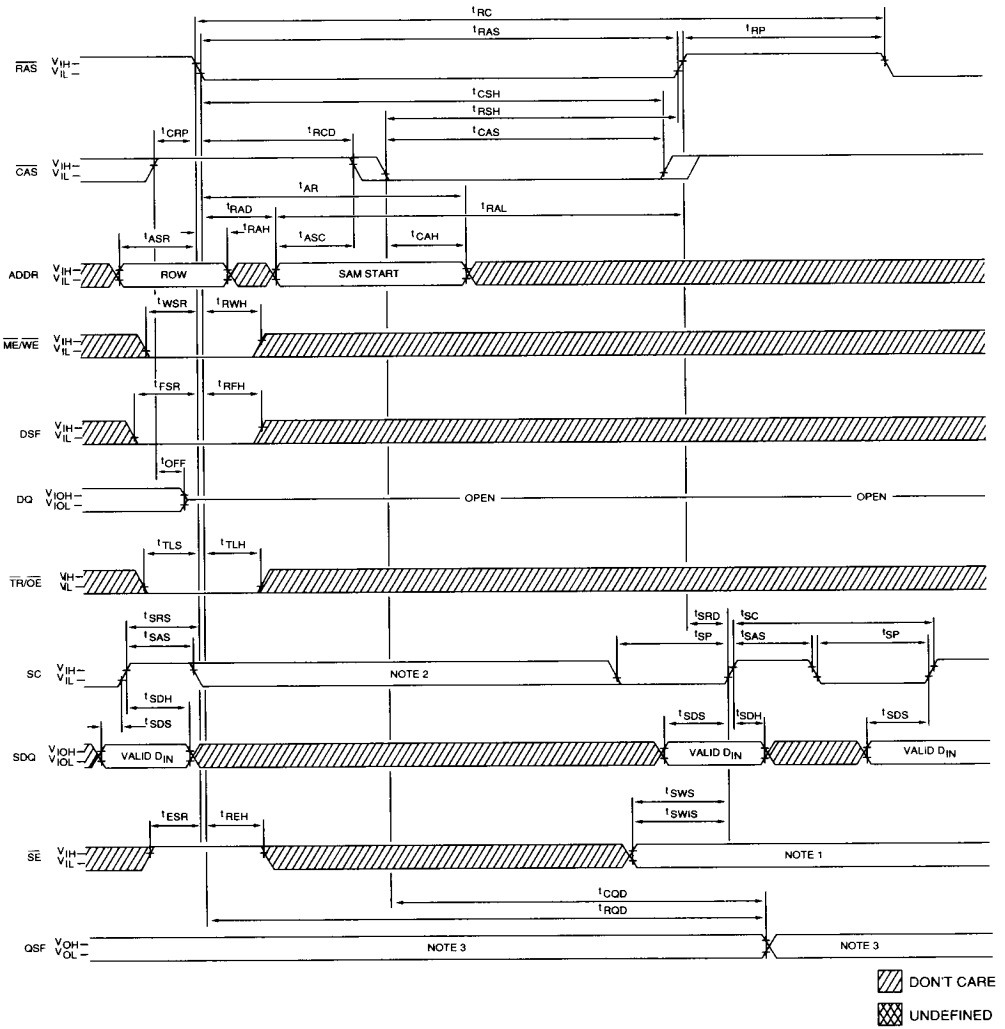
(When part was previously in the SERIAL OUTPUT mode)



NOTE:

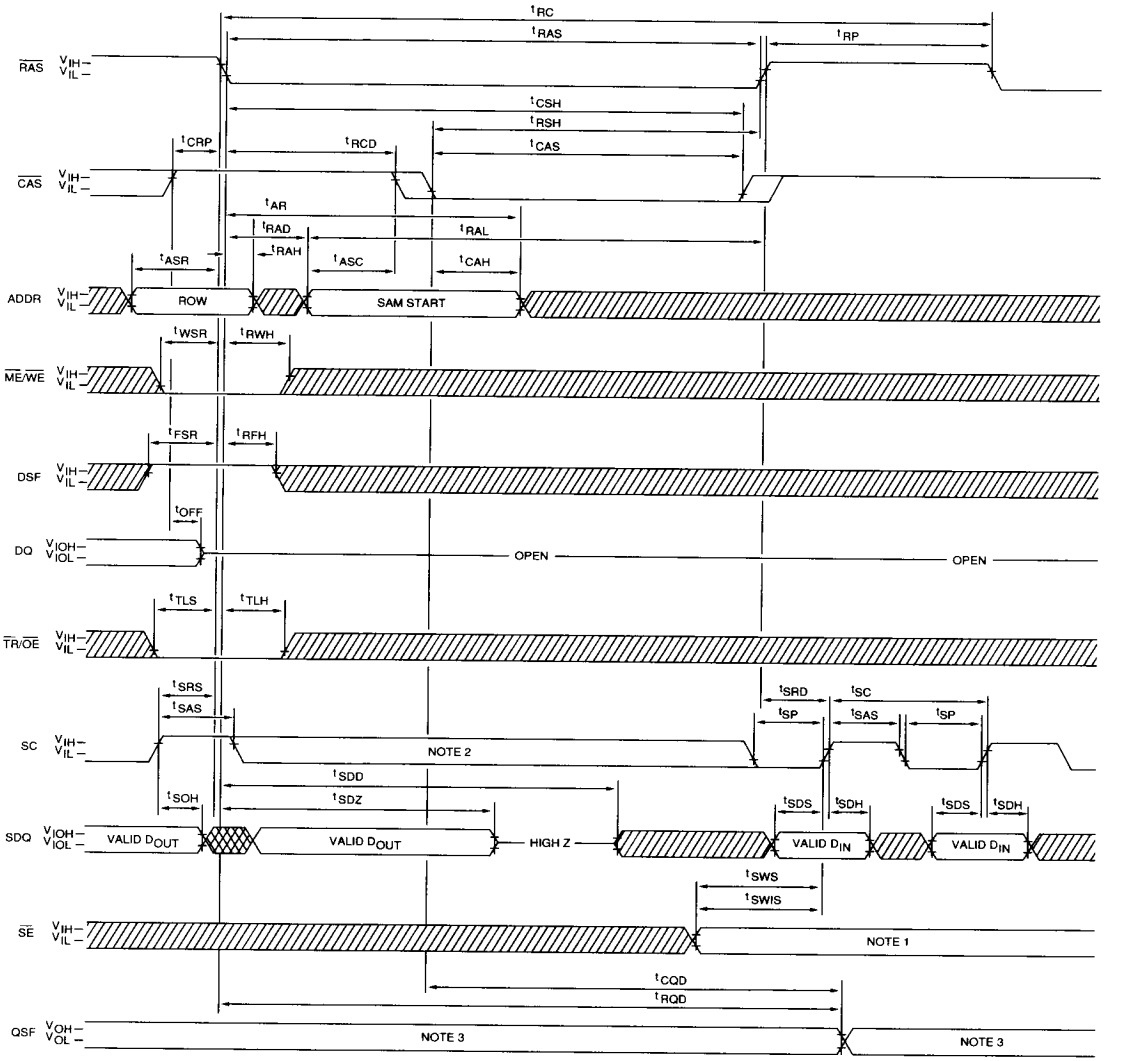
1. If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
   If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL-INPUT-MODE ENABLE cycle).
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of the state of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



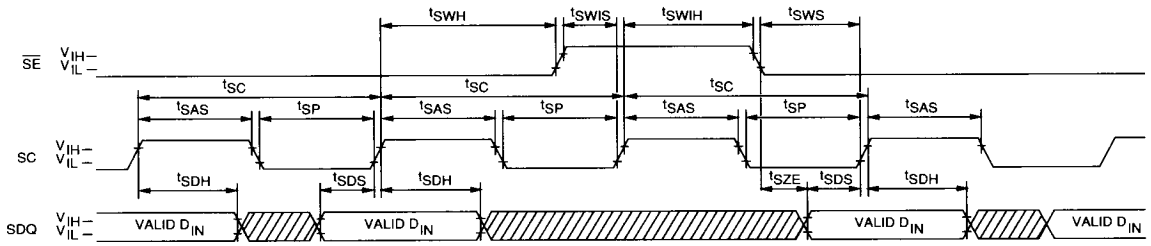
NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)



NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of the state of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

SAM SERIAL INPUT



SAM SERIAL OUTPUT