TO WATCH

GaAs EASES PC DESIGN

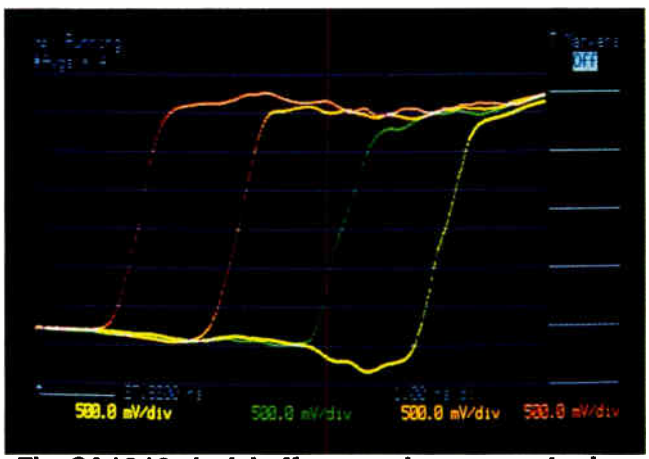
Two new GaAs chips from Gazelle Microcircuits Inc. of Santa Clara, Calif., will enable designers to use TTL design rules rather than more expensive emitter-coupled-logic implementations for high-speed PCs and workstations.

With the GA1110 multiphase clock generator and the GA1210 clock buffer, designers can use TTL design rules to build motherboards with components that run at up to 100 MHz, according to Gazelle.

Up to now, designers have had trouble stretching TTL beyond 30 MHz because of problems related to clock distribution on circuit boards.

Clock pulses distributed to different parts of a board can arrive at different times, depending upon the trace lengths. Adjustments to accommodate differences can result in performance penalties of up to 25%.

Gazelle says that its new clock buffer can advance or retard up to five individual clocks from a single clock input in increments of 2 ns. The clock generator can multiply an input frequency by 0.25 to 8 times. E



The GA1210 clock buffer can advance or retard up to five individual clocks in 2-ns increments.

SPARC-BASED MULTIPROCESSOR DEBUTS FROM SOLBOURNE

Solbourne Computer Inc. of Longmont, Colo., has unveiled what it calls the highest-performing Sparc product to date: a server that houses up to eight processors—each running 31 million instructions/s—in a symmetric multiprocessing (SMP) configuration. The Series 5E/900, or "Enterprise Server," is the first Sparc-based SMP system, Solbourne says. It is based on a 40-MHz microprocessor from Cypress Semiconductor Corp. and a 40-MHz floating-point controller from Weitek Corp. or Texas Instruments Inc. The server uses an 11-slot version of Solbourne's Kbus, with data-throughput rates of 128 Mbytes/s.

Enterprise Server is targeted at applications that require high speeds and high storage capacity. It can be configured with more than 1 Gbyte of memory and more than 27 Gbytes of disk storage. The server has a SPECmark rating of 19.1.

Prices for the 5E/900 range from $99,900 for a single-processor system up to $626,200 for an eight-processor version. Shipments are due to begin next month. Solbourne has also announced version 4.0D of its Unix variant, OS/SM. The new version supports SMP and will be shipped with all of the vendor's Series 4, 5, and 5E products. E

OAK BOOSTS VGA GRAPHICS RESOLUTION

A graphics controller from Oak Technology Inc. supports the new industry-standard Extended High-Resolution VGA specifications, offering resolution of 1,024 by 768 pixels. The Sunnyvale, Calif., company's new device, the OTI-067, extends its predecessor's 800-by-600-pixel resolution but is backward-compatible with previous video graphics standards, including EGA, CGA, MDA, and Hercules, Oak says.

Aimed at designers of VGA controller boards and IBM-compatible systems, the OTI-067 reduces the number of DRAMs needed to provide high resolution. Where most VGA controllers require eight 256K-by-4 DRAMs for noninterlaced operation, the Oak device requires just two to four. "Because we support flexible DRAM configurations, the OEM can create higher-performing graphics systems at less cost," says Oak president David Tsang. E

NATIONAL TAKES A STEP FORWARD WITH NEW BiCMOS PROCESS

Building on its Aspect III bipolar process and its high-performance CMOS technology, National Semiconductor Corp. is moving into the next generation of biCMOS with a new process: the 0.8-μm ABiC IV. The Santa Clara, Calif., company claims the new process—its fourth-generation biCMOS technology—delivers more performance at lower power and higher integration levels than any other now available.

ABiC IV's core Aspect III bipolar technology incorporates a newly enhanced recessed-emitter structure, which accounts for the performance boost, National says. The 0.8-μm lithography delivers effective n- and p-channel lengths of less than 0.65-μm, and the process is highly scalable. E

AT&T OFFERS 10BaseT CHIP SET

A three-chip family from AT&T Microelectronics is the first complete family of devices complying with the latest industry standards for twisted-pair Ethernet LANs. The CMOS chips are all that's needed to design a complete twisted-pair Ethernet system compliant with the IEEE's 802.3 LAN standard, says the Berkeley Heights, N. J., company. What's more, the chips also comply with the draft of the IEEE's proposed standard for 10BaseT devices.

The family comprises the T7220 twisted-pair medium attachment unit, the T7240 port receiver, and the T7201 multiport repeater. E