OAK TECHNOLOGY, INC.™
System Solutions in Silicon

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PRODUCT OVERVIEW

OTI-087
LOCAL BUS VGA GRAPHICS CONTROLLER

DESCRIPTION

The OTI-087 is a highly integrated, single chip Local Bus Color Graphics Controller compatible with the IBM VGA standard. The OTI-087 offers a low-cost implementation for 24-bit color at a resolution of 640x480 while being capable of higher resolutions including 1024x768 non-interlaced with 256 colors and 1280x1024 interlaced with 256 colors. The OTI-087 is completely compatible with the IBM VGA standard and implements all registers and data paths while providing improved performance and additional functionality. Especially attractive for motherboard applications, the OTI-087 supports high speed local bus implementations for cost-effective graphics co-processor class performance.

FEATURES

- IBM VGA compatible graphics controller with resolutions up to:
  - 1024x768, 256 colors Non-Interlaced
  - 1280x1024, 256 colors Interlaced
  - 640x480, 16.8 million colors (24-bit)
- 100% Hardware and BIOS compatible with IBM's VGA
- Supports up to 2 MBytes of memory:
  - 2, 4 or 8 64K X 16 DRAMs
  - 2, 4, 8 or 16 256K X 4 DRAMs
  - 2 or 4 256K X 16 DRAMs
  - 2 or 4 512K X 8 DRAMs
- Write cache for high speed local bus implementation
- Read cache optimizes memory bandwidth usage
- Integrated zero wait state AT bus performance
- Supports 8, 16, or 32-bit memory interface with fast page operation
- Supports VESA-standard high vertical refresh rates of 72 Hz for flicker-free displays
- Up to 80 MHz maximum video clock rate
- Complete linear addressability in protected mode
- Packed pixel format for 256 color modes
- Foreground/background color expansion registers for fast text output
- 16-bit graphics latch for true 16-bit operations in planar modes
- Special 256 color pattern and fill modes increase performance
- Supports 132 column text
- Integrated bus interface for PC/XT/AT and local bus implementations
- Supports portrait monitors
- True 16-bit I/O read/write operations
- EEPROM support provides switchless configurations

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SOFTWARE DRIVER SUPPORT

Oak Technology was the first graphics company to promote the importance of the hardware-software driver relationship. Thus, Oak is committed to providing customers with the most powerful software drivers. Oak's software driver support includes the fastest drivers available for popular applications including:

AutoCAD
AutoShade
CADvance
GEM
Lotus 1-2-3/Symphony
P-CAD
OS/2 Presentation Manager
Ventura
VersaCAD
VESA BIOS Extensions
WordPerfect/DrawPerfect/PlanPerfect
UNIX (ISC & SCO)
OrCAD
EasyCAD/FastCAD
Microsoft Windows
Wordstar

SUPPORTED SCREEN FORMATS

The OTI-087 provides support for all IBM standard VGA modes and the following Extended Modes:

Mode	Resolution	Color	Font	Alpha format	Dot Clk (MHz)	H-freq (KHz)	V-freq (Hz)	Memory Size	Interlaced
12h	640X480	16	8X16	80X30	31.500	37.86	72	256K/512K/1Meg	No
4Eh	80x60	16	8x8	80x60	25.175	31.50	60	256K/512K/1Meg	No
4Fh	132x60	16	8x8	132x60	40.000	31.50	60	256K/512K/1Meg	No
50h	132x25	16	8x14	132x25	40.000	31.50	70	256K/512K/1Meg	No
51h	132x43	16	8x8	132x43	40.000	31.50	70	256K/512K/1Meg	No
52h	800x600	16	8x16	100x37.5	40.000	37.88	60	256K/512K/1Meg	No
52h	800x600	16	8x16	100x37.5	50.000	48.08	72	256K/512K/1Meg	No
53h	640x480	256	8x16	80x30	31.500	37.86	72	512K/1Meg	No
54h	800x600	256	8x16	100x37.5	40.000	37.88	60	512K/1Meg	No
54h	800x600	256	8x16	100x37.5	50.000	48.08	72	512K/1Meg	No
55h	1024x768	4	8x16	128x48	65.000	48.36	60	256K/512K/1Meg	No
55h	1024x768	4	8x16	128x48	78.000	56.69	70	256K/512K/1Meg	No
56h	1024x768	16	8x16	128x48	65.000	48.36	60	512K/1Meg	No
56h	1024x768	16	8x16	128x48	78.000	56.69	70	512K/1Meg	No
57h	768x1024	16	8x16	96x64	65.000	59.74	55	512K/1Meg	No
58h	1280x1024	16	8x16	160x64	78.000	48.75	87	1Meg	Yes
59h	1024x768	256	8x16	128x48	65.000	48.36	60	1Meg	No
59h	1024x768	256	8x16	128x48	78.000	56.69	70	1Meg	No
5Bh	640x400	32K	8x16	80x25	63.000	37.86	72	512K/1Meg	No
5Ch	640x480	32K	8x16	80x30	63.000	37.86	72	1Meg	No
5Dh	800x600	32K	8x16	100x37.5	78.000	37.79	60	1Meg	No
5Eh	1280x1024	256	8x16	160x64	78.000	48.75	87	2Meg	Yes
5Fh	640x480	16.8M	8x16	80x30	78.000	31.55	60	1Meg	No

Display Memory Interface

The OTI-087 supports 64Kx16, 256Kx4, 256Kx16, and 512Kx8 DRAM devices. The OTI-087 provides all the necessary control signals and address and data lines to access the video memory in page mode. The control signals can be programmed to optimize memory cycles for a given memory type and speed for a specific memory clock. The maximum video buffer size is 2M bytes when used with 256Kx4, 256Kx16 or 512Kx8 DRAM's and 1M byte when used with 64Kx16 DRAM's. Minimum configuration is 256K bytes when used with 64Kx16 or 256Kx4 DRAM's and 1M byte when used with 512Kx8 or 256Kx16 DRAM. The video buffer can be addressed through either a programmable linear address range above 1M or through the conventional video address (A0000 to BFFFF) using the segment registers.

Clock Interface

Up to 16 external video clock frequencies can be selected by four programmable clock select pins. Video clock frequencies up to 80 MHz can be supported. When implemented with the OTI-068 Dual Clock Generator, the OTI-087 can select sixteen pixel clock frequencies providing support for both conventional and flicker-free VESA vertical refresh rates without any hardware switches. The OTI-068 also supports three memory clock frequencies which can be selected through hardware configuration to optimize performance with a wide variety of DRAM types and speeds.

System Bus Interface

The system bus of the OTI-087 can be connected to the PC system in four different configurations: on-board local bus, add-on local bus, on-board AT bus and add-on AT bus. The mode of operation is defined by the **Configuration Register 1** status, set through the MD[7:0] bus during reset time.

System Configuration	Bit 2	Bit 1
Local Bus Motherboard	0	0
Local Bus Add-on	0	1
On-board AT	1	0
Add-on AT	1	1

Local Bus Interface

In Local Bus configuration, the OTI-087 can interface to the 80286, 80386SX, 80386DX, and 80486 CPUs. Configuration of the OTI-087 for the proper CPU local bus is accomplished through the ADSn pin and the **Configuration Register 2** as detailed in the table below. **Configuration Register 2** is set through the MD[15:8] bus during reset.

Local Bus Mode	ADSn	Bit 1	Bit 0
80286 Local Bus	0	0	0
80386SX Local Bus	1	0	0
80386DX Local Bus	1	0	1
80486 Local Bus	1	1	0

To ensure the above detection scheme will operate properly, a weak pull-down resistor should be connected to the ADSn pin of the OTI-087. Since the 80286 processor does not have ADSn, this signal should remain low during reset in 80286 designs. For proper operation in 80386 and 80486 processor designs, this signal will be reset high.

OTI-087 LOCAL BUS WITH 80286 AND 80386SX PROCESSORS

The local bus interface of the OTI-087 provides an optimal implementation for 80286 and 80386SX designs which use Oak Technology's OTI-020 system chipset. An implementation of the OTI-087 with the OTI-020 requires no external logic for local bus interface.

The video space of the OTI-087/OTI-020 local bus video system is defined by the VIDEO1 register (port 'h1F index 5). When any one of the video segments in this register is enabled, the OTI-020 system chipset generates a video cycle to the external bus and terminates the CPU cycle. If the video segments are disabled, the local bus OTI-087 will terminate the CPU cycle. Graphics Register h3DF, Index 6 only affects the access to video memory and has no effect on the generation of SRDY. At system boot-up time, the system will scan for the presence of any off-board memory which occupies the A0000~BFFFF range. If off-board video memory is detected, the VIDEO1 register (present in both the OTI-020 system chipset and the OTI-087) will be programmed so that the local bus system responds to all the memory in A0000~BFFFF, excluding the enabled segments in the VIDEO1 register.

The OTI-087 supports 16-bit, zero-wait-state CPU memory operations through the CPU local bus. The OTI-087

uniquely employs both a read cache and a write cache to achieve zero-wait-state memory operations for local bus speeds up to 33 MHz. During the CPU memory cycle, the OTI-087 interprets the status lines (WRn, DCn) and the address CA19~CA17 (h101) gated with the VIDEO1 register to generate a local bus memory cycle. If during memory reads the requested data is already inside the OTI-087 read cache, SRDY is returned in the next CPU clock, thus a zero-wait-state memory cycle. Otherwise, SRDY is not returned until the data is read from the video memory and driven out to the bus. For writes to video memory, a memory write request is stored inside the write cache and SRDY is returned in the next CPU clock for a zero-wait-state memory cycle. If either the write cache is full or the write address does not share the same cache page as the previous write, then SRDY is not returned until the data is actually written to the video memory.

The OTI-087 supports 16-bit I/O access and 8-bit memory access for DMA and MASTER cycles. During a DMA or MASTER cycle, the OTI-087 receives I/O and memory commands from the AT-bus and transfers data to the local SD bus as if it were a 16-bit device. In this case, both SD[7:0] and SD[15:8] are driven with the same data. During I/O cycles, the OTI-087 receives commands from the AT-bus and transfers data on the local bus. The system chipset is responsible for routing the address and data to and from the AT-bus.

80386DX AND 80486 LOCAL BUS

This section refers to the 80386DX/80486 block diagrams following this section. The OTI-087 requires four buffers (A,B,E,F in the diagram) and 1 pal to interface with the 80386DX CPU. Two additional buffers (C,D in the diagram) are required to interface with the 80486 CPU. The pal is used to decode the upper address of the CPU and generate the CPU address 0,1 and the CPUBHEn signal for the OTI-087. The A,B buffers are used to interface the OTI-087 data bus to AT-data bus while the C,D,E,F buffers are used to interface the OTI-087 data bus to the CPU data bus.

During I/O, DMA or MASTER cycles the OTI-087 receives bus commands from the AT-bus. During a CPU memory cycle, the OTI-087 will use the CPUA0/A1/BHEn signals to execute the cycle. The LBSELn signal is the protocol between the system chip set and the OTI-087 to determine ownership of the current memory cycle. If the current memory cycle belongs to the OTI-087 address space, the OTI-087 forces the LBSELn signal low at the beginning of T2 and terminates the cycle with SRDY. If the current memory cycle does not belong to the OTI-087 address space the system chip set should terminate the cycle. In 80386DX and 80486 configurations, there are two reset signals connected to the OTI-087. The RSET signal is connected to the system reset and the CPURESET is connect to the CPU reset. The OTI-087 uses the CPURESET signal to synchronize the internal clock and uses the RSET signal to reset the OTI-087. If the system chipset does not drive a valid address to the CPU bus during DMA or MASTER cycles, then more buffers are necessary to route the address to the CPU bus. Buffer G in 80386DX/80486 block diagrams illustrate this implementation.

SUMMARY OF PERFORMANCE FEATURES

The OTI-087 implements all of the standard state-of-the-art features for high speed frame-buffer graphics controllers. These standard features include independent memory and pixel clocks, support for high refresh displays, highly integrated bus interfaces, and true 16-bit I/O read/write operations. In addition, the OTI-087 implements several next generation features which advance the state-of-the-art in graphics frame-buffer technology.

HIGH SPEED LOCAL BUS

The OTI-087 is one of the first PC graphics controllers designed from the ground up for motherboard architectures implementing direct CPU interfaces to the video controller. The local control signals of the OTI-087 provide for accelerated system to video memory transfers. Timing overhead is also reduced. To take advantage of the high transfer rates, the OTI-087 implements the most features of any frame-buffer controller for assisting CPU-based graphics operations.

WRITE CACHE

When writing to the OTI-087, both data and address are latched from the system bus and the zero-wait-state signal is activated, unless the cache is full. When implemented in the AT-bus configuration, the OTI-087 will exhibit zero-wait-state performance in lower resolution/color and planar modes. In higher resolution, the percentage of zero-wait cycles will decrease for packed pixel modes with increasing bus speed, resolution, color depth, and vertical refresh.

READ CACHE

The read cache of the OTI-087 was designed to accelerate bitblt functions. When executing block moves, often the next operation requires a read from an adjacent memory location. In this case, the desired data will be in the read cache and the operation can execute without waiting for a memory cycle.

LINEAR ADDRESSABILITY

In extended video modes where more than 256K bytes of video buffer are required, the video driver must perform segment checking and address calculation to determine a given pixel's location in video memory. At programmable addresses above 1 Mbyte, the OTI-087 provides memory mapping such that all of the video buffer fits into one segment, and therefore eliminates segment checking. When running applications in protected-mode, this speeds all functions.

FOREGROUND/BACKGROUND COLOR EXPANSION

In packed pixel modes, the output of simple text becomes more cumbersome. To reduce the number of individual memory operations required, the OTI-087 contains foreground/background color expansion registers which allow eight consecutive bytes to be expanded from one byte containing the foreground or background bits. A pixel masking capability is also implemented to be able to leave specified pixels unchanged. This also speeds masked bitblt functions.

256 COLOR PATTERNS AND FILLS

For packed pixel modes, the OTI-087 provides a pattern register for defining patterns and expanding the color information from either OTI-087 registers or CPU data. This allows fast pattern fill.

16-BIT GRAPHICS LATCH

Most currently available VGA controllers only allow for byte operations in many cases. The OTI-087, as with previous generations of Oak VGA controllers, provides true 16-bit move operations in all situations. Relative to other VGA controllers, this is particularly useful for pattern blts and source copy bitblts where MOVSW instructions can replace MOVSB instructions.

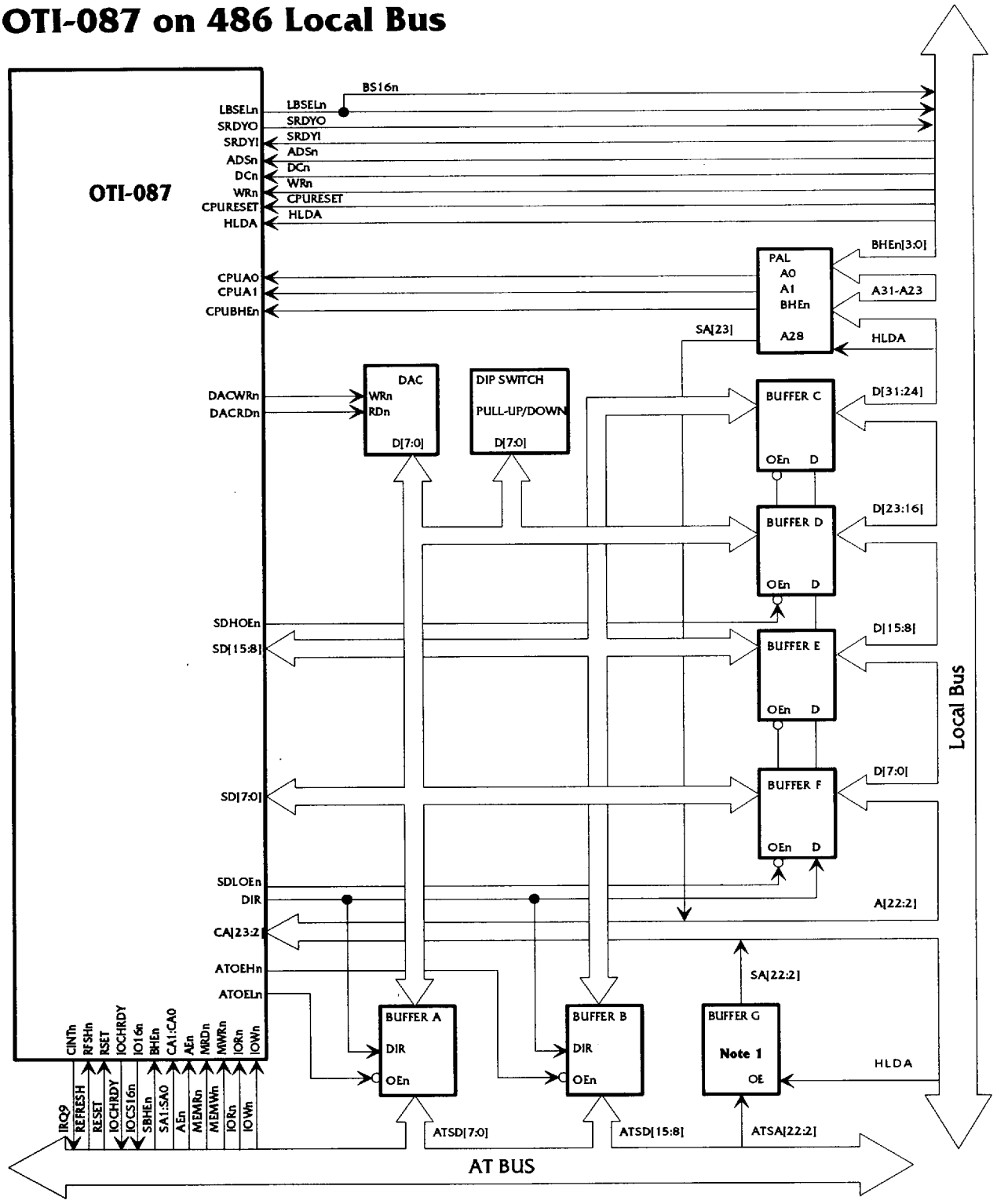
EEPROM SUPPORT

In a VGA-based video system, certain configuration information must be available to the video BIOS. It is common practice on many video adapter boards to use jumpers or switches to provide the proper settings. These switch settings can cause confusion for the consumer. To simplify the situation, the OTI-087 provides support for a serial EEPROM which stores the specific configuration information. The configuration is done through software, eliminating all jumpers and switches.

80 MBYTE/SEC VIDEO

Fixed clock rates to 80 MHz allow the OTI-087 to offer vertical refresh rates at 1024x768 that exceed the VESA standard of 70 Hz for high vertical refresh displays. Depending on the capabilities of the monitor, the OTI-087 can support up to 1024x768 with 256 colors at a 76 Hz vertical screen refresh.

OTI-087 on 486 Local Bus



Note 1: Buffer G is needed only if the system chipset does not route back these address signals during DMA/Master cycles.

PIN DESCRIPTION

AT-Bus Interface

Pin Name	Pin #	Pin Type	Description
SD[15:8]	46:42, 40:38	I/O	SYSTEM DATA BUS 15:8.
SD[7:0]	85:81, 77:75	I/O	SYSTEM DATA BUS 7:0.
SA[16:0]	67:62, 60:50	I	LATCHED SYSTEM ADDRESS BITS 16:0.
LA[23:17]	74:68	I	UNLATCHED SYSTEM ADDRESS BITS 23:17.
M16n	78	I/O	16-BIT MEMORY.
IOCHRDY	79	O	IO CHANNEL READY.
AEN	86	I	ADDRESS ENABLE.
RFSHn	87	I	REFRESH.
MRDn	88	I	MEMORY READ.
MWRn	89	I	MEMORY WRITE.
CINTn	90	O	CRT INTERRUPT REQUEST.
IO16n	91	O	16-BIT I/O.
MASTERn	92	I	MASTERn.
ALE	93	I	ADDRESS LATCH ENABLE.
ROMENL	95	I/O	ROM LOW BYTE ENABLE.
RSET	97	I	RESET.
ENVGA	98	I	VGA ENABLE.
ZEROWSn	99	I/O	ZERO WAIT STATE.
BHEn	100	I	BYTE HIGH ENABLE.
IORn	101	I	I/O READ.
IOWn	102	I	I/O WRITE.

Local Bus Interface

Pin Name	Pin #	Pin Type	Description
CA[23:17]	74:68	I	CPU ADDRESS BITS 23:17.
CA[16:0]	67:62, 60:50	I	CPU ADDRESS BITS 16:0.
ADSn	93	I	ADDRESS STATUS.
PROCLK	95	I/O	PROCESSOR CLOCK.
WRn	98	I	WRITE/READ.
DCn	99	I/O	DATA/CONTROL.
HLDA	92	I	HOLD ACKNOWLEDGE.
ATOEHn	47	O	AT-BUS HIGH BYTE DATA ENABLE.
ATOELn	10	I/O	AT BUS LOW BYTE DATA ENABLE.
DIR	11	I/O	DATA DIRECTION CONTROL.
SDLOEn	12	I/O	SYSTEM DATA LOW OUTPUT ENABLE.
SDHOEn	13	I/O	SYSTEM DATA HIGH OUTPUT ENABLE.
CPUA0	14	I/O	CPU ADDRESS BIT 0.
CPUA1	15	I/O	CPU ADDRESS BIT 1.
CPUBHEn	16	I/O	CPU BYTE HIGH ENABLE.
CPURESET	17	I/O	CPU RESET.
GA20	19	I	Gate A20.
SRDYI	20	I	SYSTEM READY INPUT.
LBSELn	23	O	LOCAL BUS SELECT.
SRDY	78	I/O	SYSTEM READY.

Clock Interface

Pin Name	Pin #	Pin Type	Description
VCLK	106	I	VIDEO CLOCK.
MCLK	107	I	MEMORY CLOCK.
CSEL[0]	105	O	CLOCK SELECT 0.
CSEL[1]	104	O	CLOCK SELECT 1.
CSEL[2]	103	I/O	CLOCK SELECT 2.
CSEL[3]	18	O	CLOCK SELECT 3.

CRT and Color Palette Interface

Pin Name	Pin #	Pin Type	Description
P[7:0]	33:30, 28:25	O	PIXEL DATA.
VSYNC	34	O	VERTICAL SYNC.
HSYNC	35	O	HORIZONTAL SYNC.
BLANKn	36	O	BLANK.
PCLK	37	O	PIXEL CLOCK.
DACRDn	48	O	COLOR PALETTE READ.
DACWRn	49	O	COLOR PALETTE WRITE.
BD[7:0]	17:10	I/O	AUXILIARY DATA BUS 7:0.
EPCLK	19	I	ENABLE PCLK.
EPDATA	20	I	ENABLE PDATA.
MXPCLK	23	O	MUX CLOCK.
SWSENSE	24	I	SWITCH SENSE.

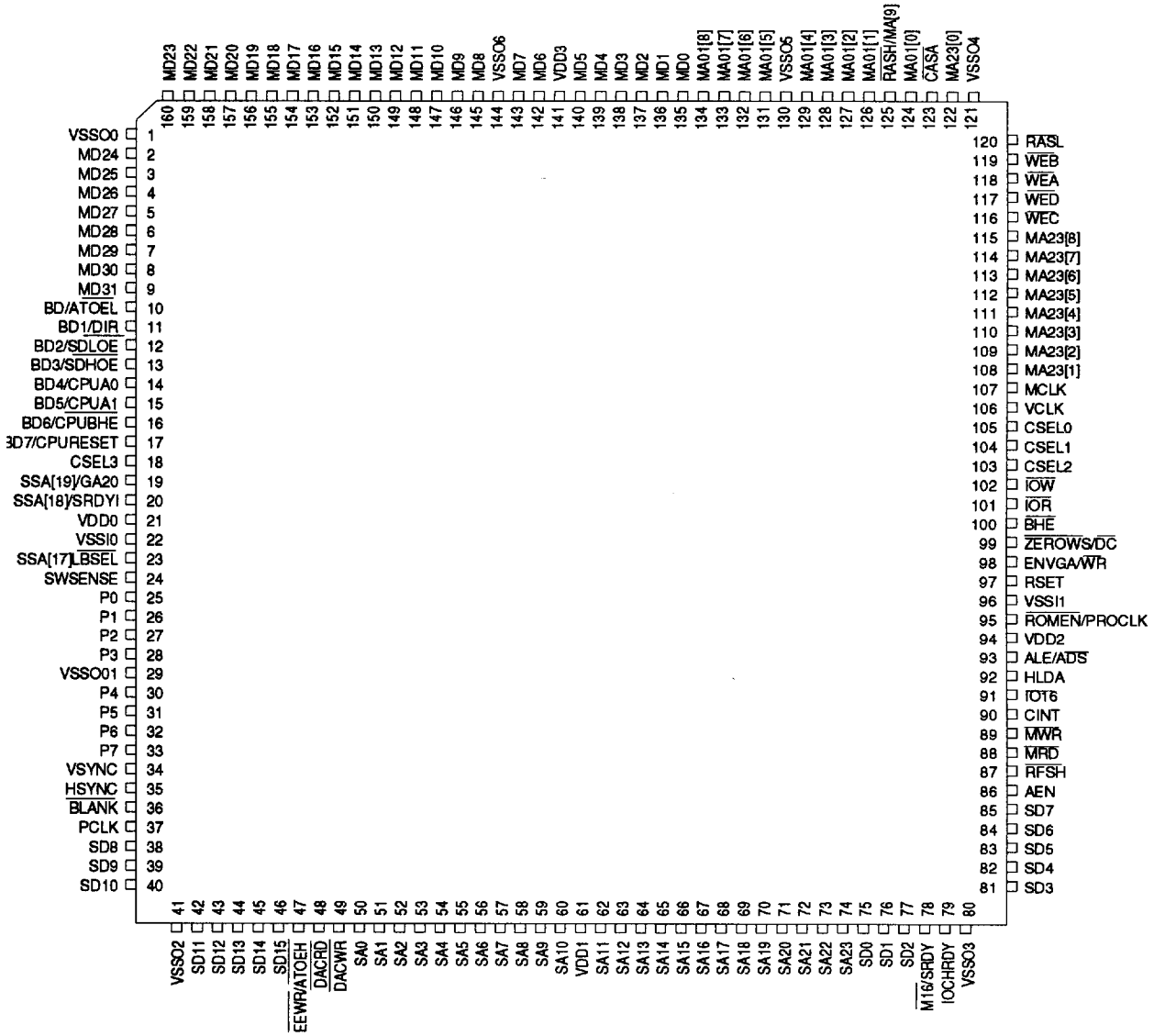
Video Memory Interface

Pin Name	Pin #	Pin Type	Description
MA01[8:1]	134:131, 129-126	O	MEMORY ADDRESS MAPS 0, 1.
MA23[8:1]	115-108	O	MEMORY ADDRESS MAPS 2, 3.
RASLn	120	O	ROW ADDRESS STROBE LOW.
RASHn/ MA9	125	O	ROW ADDRESS STROBE HIGH.
CASAn	123	O	COLUMN ADDRESS STROBE.
WEAn	118	O	WRITE ENABLE A.
WEBn	119	O	WRITE ENABLE B.
WECn	116	O	WRITE ENABLE C.
WEDn	117	O	WRITE ENABLE D.
MA01[0]/ CASBn	124	O	MEMORY AD DRESS BIT 0.
MA23[0]	122	O	MEMORY AD DRESS BIT 0.
MD[31:0]	9:2, 160:153, 152:145, 143:142, 140:135	I/O	MEMORY DATA.

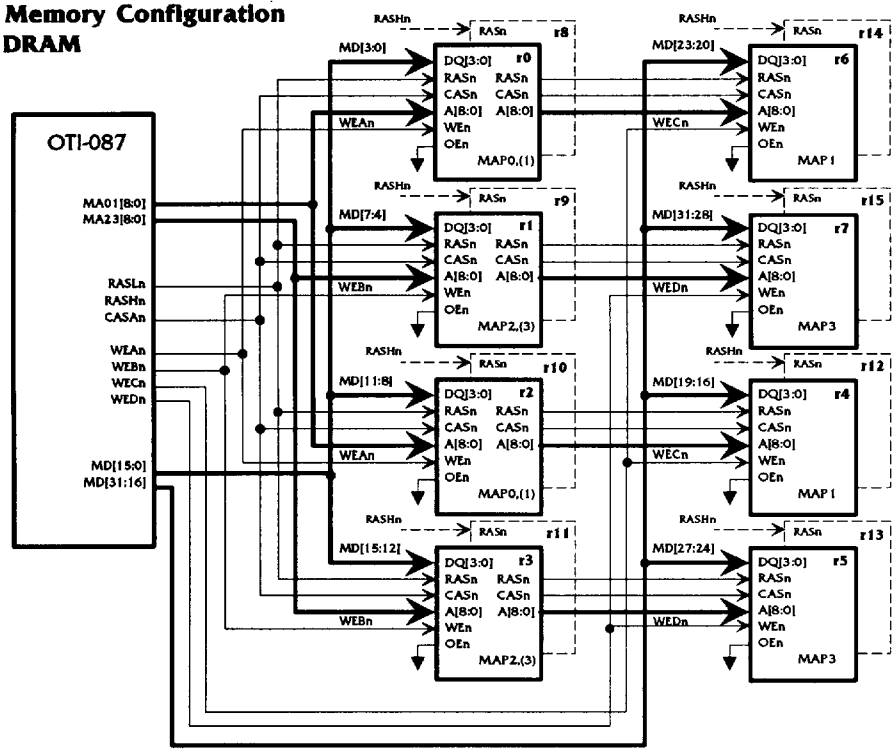
EEPROM Interface

Pin Name	Pin #	Pin Type	Description
EEPCSn	47	O	CHIP SELECT.
EEPSK	103	O	SHIFT CLOCK.
EEPWD	104	O	WRITE DATA.
EEPRD	105	I/O	READ DATA.

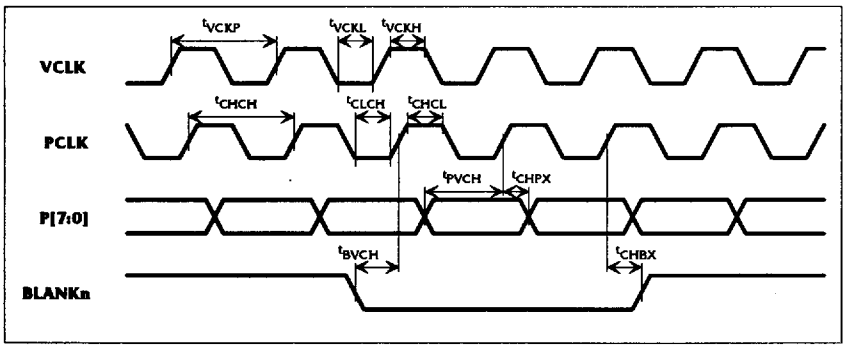
OTI-087 PIN DIAGRAM



OTI-087 Memory Configuration 256Kx4 DRAM

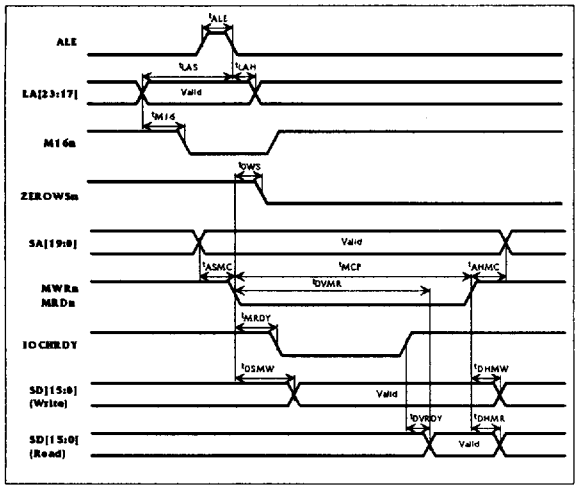


Video Pixel Timing



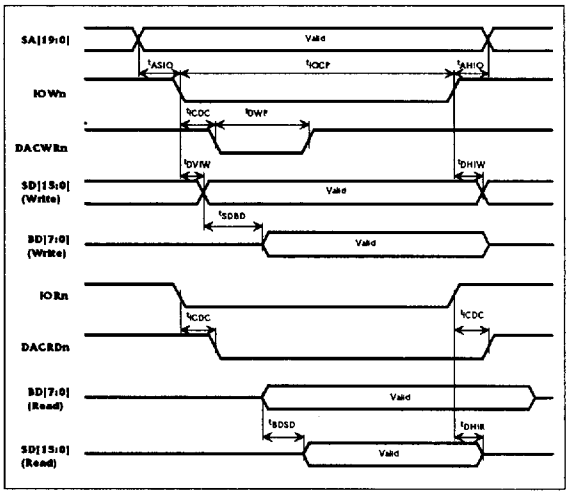
Symbol	Parameter	Min (ns)	Max (ns)
tVCKP	Video Input Clock Period	12	
tVCKH	VCLK Width High	6	
tVCKL	VCLK Width Low	6	
tCHCH	Pixel Clock Period	12	
tCHCL	PCLK Width High	tVCKH-1	
tCLCH	PCLK Width Low	tVCKL-1	
tPVCH	Pixel Word Setup Time	3	
tCHPX	Pixel Word Hold Time	3	
tBVCH	Blankn Setup Time	3	
tCHBX	Blankn Hold Time	3	

Video Memory Cycle Timing



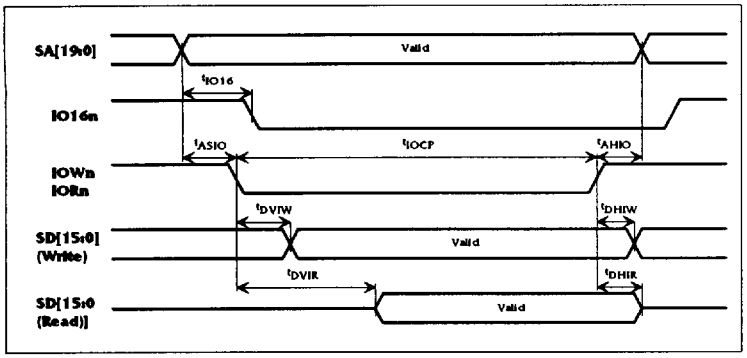
Symbol	Parameter	Min (ns)	Max (ns)
tALE	ALE Active to Inactive	40	
tLAS	LA[23:17] Setup to Falling Edge of ALE	80	
tLAH	LA[23:17] Hold from Falling Edge of ALE		15
tM16	M16n Active from Valid LA[23:17]		40
t0WS	ZEROWSn Delay from Command		25
tASMC	SA[16:0] Setup to Memory Command Active	25	
tMCP	Memory Command Pulse Width	165	
tAHMC	SA[16:0] Hold from Memory Command Inactive	20	
tDVMR	Read Data Valid from MRDn Active (0 Wait State)		65
tMRDY	RDY Inactive from Memory Command Active		30
tDSMW	Write Data Setup to MRWn Active	-45	
tDHMW	Write Data Hold from MWRn Inactive	15	
tDVRDY	Read Data Valid from RDY Active		5
tDHMR	Read Data Hold from MRDn Inactive	0	
tBDSD	BD[7:0] Valid to SD[15:0] Valid		35
tMRRE	ROMENLn Delay from MRDn		25

Video DAC I/O Timing

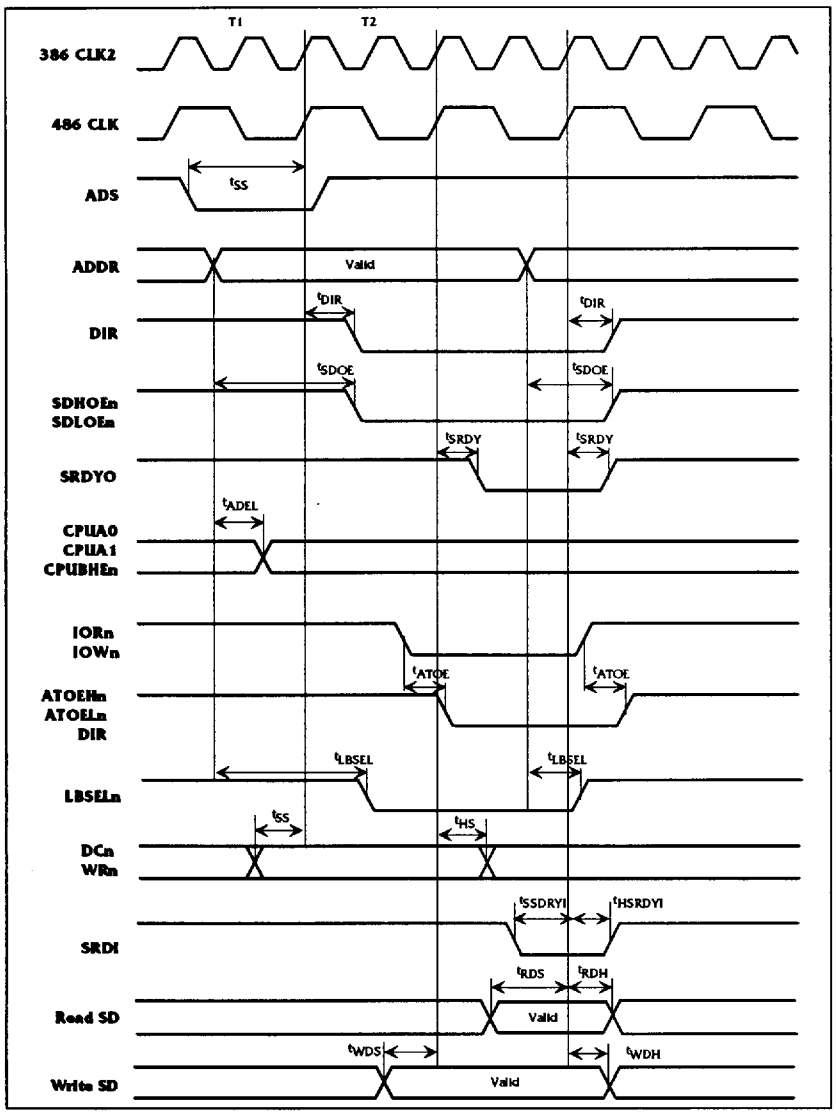


Symbol	Parameter	Min (ns)	Max (ns)
tASIO	SA[16:0] Setup to I/O Command Active	25	
tAHIO	SA[16:0] Setup from I/O Command Inactive	30	
tIOCP	I/O Command Pulse Width	115	
tDVIW	Write Data Valid from IOWn Active	-55	
tDHIW	Write Data Hold from IOWn Inactive	15	
tDHIR	Read Data Hold from IORn Inactive	0	
tICDC	DAC Command Delay from I/O Command		25
tDWP	DACWRn Pulse Width	70	
tSDBD	SD[7:0] Valid to BD[7:0] Valid		50
tBDSD	BD[7:0] Valid to SD[15:0] Valid		35

Video I/O Access Timing



Local Bus Interface Timing



Video I/O Access Timing

Symbol	Parameter	Min (ns)	Max (ns)
tIO16	IO16n Active from Valid SA[15:0]		60
tASIO	SA[16:0] Setup to I/O Command Active	25	
tAHIO	SA[16:0] Setup from I/O Command Inactive	30	
tIOCP	I/O Command Pulse Width	115	
tDVIW	Write Data Valid from IOWn Active	-55	
tDHIW	Write Data Hold from IOWn Inactive	15	
tDVIR	Read Data Valid from IORn Active		70
tDHIR	Read Data Hold from IORn Inactive	0	

Local Bus Interface Timing

Symbol	Parameter	Min (ns)	Max (ns)
tDIR	DIR Active from CPUCLK	6	20
tSDOE	SDHOEn, SDLOEn Active from Valid Address	6	15
tSRDY	SRDYn Active/Inactive from CPUCLK	6	15
tADEL	CPU A0, A1, BHEn Valid from BE0-3n		see Note 1
tATOE	ATOE Active from IOWRn/IORDn		12
tLBSEL	LBSELn Valid from SA		15
tSSRDYI	SRDYI Setup Time	5	
tHSRDYI	SRDYI Hold Time	3	
tSS	Status Setup Time	4	
tHS	Status Hold Time	4	
tRDS	Read Data Setup Time	12	
tRDH	Read Data Hold Time	7	
tWDS	Write Data Setup Time	7	
tWDH	Write Data Hold Time	5	

Note 1: This delay depends on the necessary external PAL. Please refer to the tables below for PAL speed requirements.

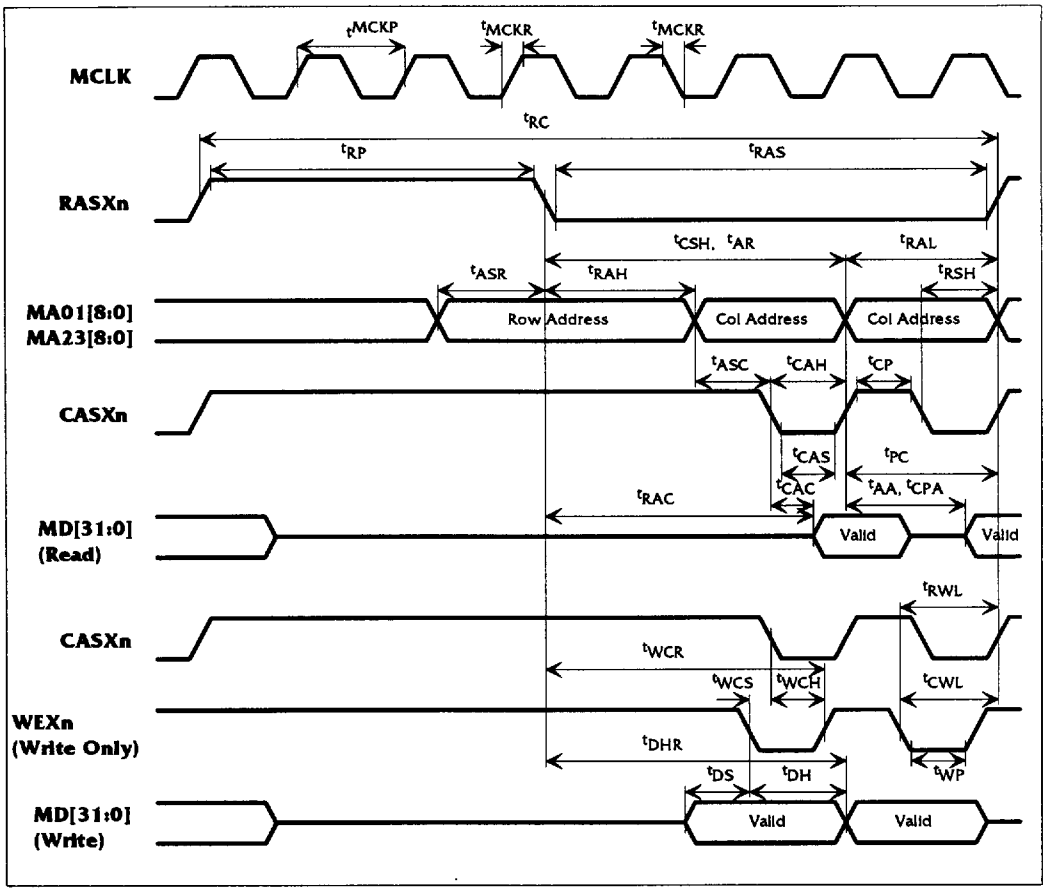
PAL Interface for 80386DX CPU

Local Bus Frequency	PAL 16L8
20 MHz	15 ns
25 MHz	15 ns
33 MHz	10 ns
40 MHz	7 ns

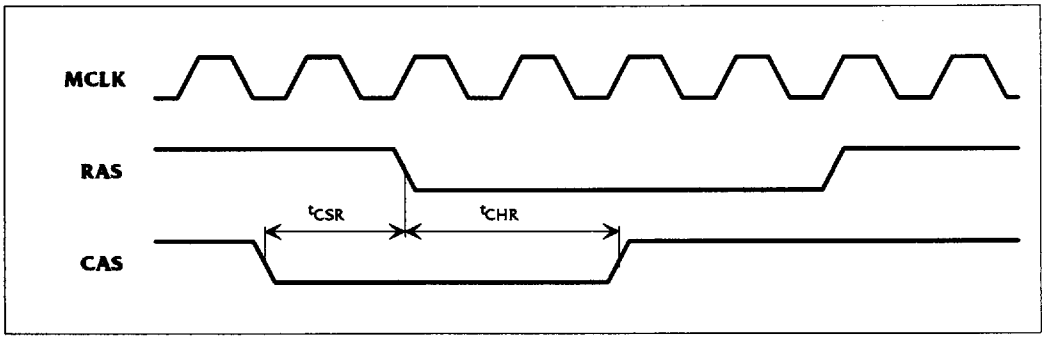
PAL Interface for 80486 CPU

Local Bus Frequency	PAL 16L8
20 MHz	15 ns
25 MHz	15 ns
33 MHz	10 ns

DRAM Interface Timing



Memory Refresh Timing



DRAM Interface Timing and Refresh Timing

SYMBOL	PARAMETER	DS1		DS2	
		Min (ns)	Max (ns)	Min (ns)	Max (ns)
tMP	Memory Clock Period	22	25	20	25
tMCKR	Memory Clock Rise/Fall		2.5		2.5
tRC	Random Rd/Wr Cycle Time	7tMP		7tMP	
tRP	RASn Precharge Time	3tMP		3tMP	
tRAS	RASn Pulse Width	4tMP		4tMP	
tCSH	CASn Hold Referenced to RASn	4tMP		4tMP	
tAR	Column Address Hold Ref. to RASn	4tMP		4tMP	
tRAL	Column Address to RASn Lead Time	2tMP		2tMP	
tASR	Row Address Setup Time	1tMP		1tMP	
tRAH	Row Address Hold Time	1tMP		1tMP	
tRSH	RASn Hold Referenced to CASn	1tMP		1.5tMP	
tASC	Column Address Setup Time	1tMP		0.5tMP	
tCAH	Column Address Hold Time	1tMP		1.5tMP	
tCP	CASn Precharge Time	1tMP		0.5tMP	
tCAS	CASn Pulse Width	1tMP		1.5tMP	
tPC	Fast Page Mode Cycle Time	2tMP		2tMP	
tRAC	Access Time from RASn		4tMP		4tMP
tCAC	Access Time from CASn		1tMP		1.5tMP
tAA	Access Time from Col. Addr. (MA)		2tMP		2tMP
tCPA	Access Time from CASn Precharge		2tMP		2tMP
tRWL	WExxn to RASn Lead Time	1tMP		1.5tMP	
tWCR	WExxn Hold Ref. to RASn	4tMP		4tMP	
tWCS	WExxn Setup to CASn	0tMP		0tMP	
tWCH	WExxn Hold Ref. to CASn	1tMP		1tMP	
tCWL	WExxn to CASn Lead Time	1tMP		1.5tMP	
tWP	WExxn Pulse Width	1tMP		1.5tMP	
tDHR	MD Hold Ref. to RASn	4tMP		4tMP	
tDS	MD Setup to WExxn	1tMP		0.5tMP	
tDH	MD Hold to WExxn	1tMP		1.5tMP	
tCSR	CASn Setup to RASn (Ref. Cycle) (2)	1tMP		1tMP	
tCHR	CASn Hold to RASn (Ref. Cycle) (2)	2tMP		2tMP	

NOTE: 1. Refresh Cycles are implemented as CASn before RASn REFRESH cycles.
2. Write cycles are implemented as EARLY WRITE cycles.

DC SPECIFICATION

Absolute Maximum Ratings

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V

Stresses above those listed may cause permanent damage to the OTI-087. These specifications are stress ratings only and do not apply to operatinal use. Functional operation of this device at these or any other conditions above those indicated in this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics: T_A=0°C to 70°C, V_{DD}=5V +/-5%, V_{SS} = 0V

Symbol	Parameter	Min	Max	Unit	Conditions
Voh	Output Voltage High	2.4		V	Ioh=400 uA
Vol	Output Voltage Low		.4	V	Iol=24 mA, Note 1,2
Vol	Output Voltage Low		.4	V	Iol=12 mA, Note 1
Vol	Output Voltage Low		.4	V	Iol=10 mA, Note 1
Vol	Output Voltage Low		.4	V	Iol=8 mA, Note 1
Vol	Output Voltage Low		.4	V	Iol=4 mA, Note 1
Vol	Output Voltage Low		.4	V	Iol=2 mA, Note 1
Vih	Input Voltage High	2	VCC+0.5	V	TTL, Note 3
Vil	Input Voltage Low	-0.5	0.8	V	TTL, Note 3
Vis	Schmitt Input Voltage	2.4	VCC+0.5	V	Schmitt, Note 3
Vic	CMOS Input Voltage	3.8	VCC+0.5	V	CMOS, Note 3
Iil	Input Leakage Current	-10	10	uA	
Oil	Output Leakage Current	-10	10	uA	
ICC	Operating Supply Current		TBD	mA	Input=VCC or GND, No Output Load
Ci	Input Capacitance		8	pF	
Co	Output Capacitance		8	pF	
Cio	I/O Capacitance		8	pF	

Notes:

1) Output Current (Iol) Capabilities:
   - 24mA: SD[15:0] with slew control.
   - 8mA: SRDY, RASLn, RASHn, CASAn, WEAn, WEBn, MA01[0], MA23[0], HSYNC, VSYNC, LBSELn BLANKn, P[7:0], PCLK
   - 4mA: BD[7:0], MA01[8:1], MA23[8:1], MD[31:0]
   - 2mA: CSEL[3:0], DACRn, RACWn, ROMENLn
2) Open Drain (open collector) Outputs:
   - 24mA: IOCHRDY, CINTn, IO16n, M16n, ZEROWSn
3) Input Structures:
   - TTL: All