NeoMagic Puts Graphics System in One Chip

Integrated Frame Buffer Lowers Cost, Power for Notebooks

by Linley Gwennap

With a wave of its wand, startup NeoMagic has combined memory and logic in a new way to create an integrated graphics subsystem for mobile computers. The MagicGraph NM2070 merges a Super VGA graphics accelerator, local-bus interface, RAMDAC, LCD controller, and nearly 1 Mbyte of frame-buffer memory, all in a single chip. This level of integration not only reduces board area and power, it offers the potential of desktop-level graphics performance in a notebook.

Founded less than two years ago, NeoMagic is led by several veterans from Cirrus Logic with expertise in PC system logic, graphics, and memory products. Their idea was to unite these features in a family of devices that integrate both memory and logic on a single chip, following the integration trends in other components.

The graphics subsystem is a ripe target for this approach. As the number of transistors that can be packed onto a single chip continues to increase, the amount of memory required by a typical graphics frame buffer remains 1 Mbyte, a value fixed by the resolution of the display. With 16-Mbit DRAM technology, a single memory chip has twice the capacity needed by this frame buffer. Most frame buffers today use two 4-Mbit chips and cannot take advantage of emerging 16-Mbit devices.

NeoMagic realized that by devoting half of a 16-Mbit die to frame-buffer memory, the other half could be used for logic. In fact, all the logic for a typical graphics subsystem, roughly 70,000 gates, can fit in this half of the die. The result is a single-chip device that replaces three to four chips in current systems, yet its die size is roughly the same as a standard 16-Mbit DRAM.

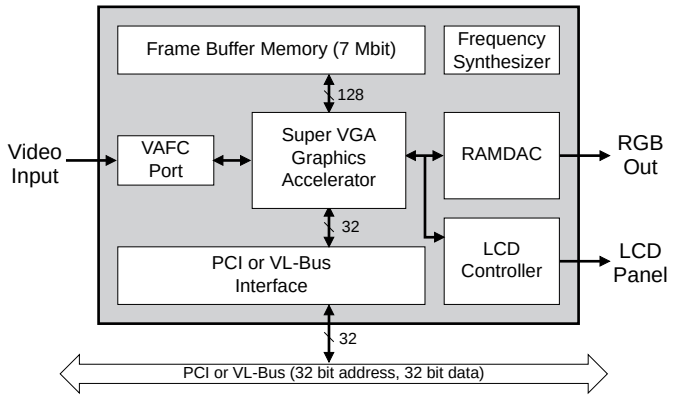

Figure 1. The NeoMagic chip integrates a complete frame-buffer memory along with a notebook-style graphics controller.

Single-Chip Design Is Unique

Figure 1 shows the NM2070, which includes features required by the latest mobile systems. The chip connects to the processor using either VL-Bus or PCI. The 32-bit PCI interface is capable of 3.3-V operation, reducing system power. It can accept video input through its VESA advanced-feature connector (VAFC) and display the images. The chip directly controls an LCD panel, the typical notebook display, and can also drive an external RGB monitor using its integrated RAMDAC. Even the clock synthesizer is integrated.

The graphics accelerator handles basic functions such as bitBLTs and raster operations, relieving the CPU of this tedium. The available gate count did not allow more advanced features, such as line drawing and video scaling, without increasing the die size. The graphics engine uses 64-bit data paths, improving performance when data can be processed in parallel.

To the above description, which could be satisfied by several competitive chips, NeoMagic adds a unique integrated frame buffer. The chip includes about 7 Mbits of memory for the frame buffer, adequate for standard resolutions up to $1024 \times 768 \times 8$. Shaving a megabit of memory from the standard 8-Mbit frame-buffer size, which is forced to a power of two in discrete solutions, offers a small cost reduction.

The data path to the frame buffer is 128 bits wide, providing far greater bandwidth than can be achieved by the 32-bit frame buffers typically found in notebook systems or even by the 64-bit memories used in some desktop PCs. The DRAM is banked to sustain high bandwidth.

Many Advantages to Integration

As processor designers found when combining cache and CPU onto a single chip, integration can lower cost while actually improving performance. One obvious benefit is a reduction in footprint. Even a highly integrated graphics solution requires three chips today: a single-chip controller plus two DRAMs. The NM2070 eliminates two of the three chips and gets rid of the 50 or more pins needed to connect to memory, fitting the new chip into a 176-pin TQFP package. As a result, the NeoMagic chip occupies about 60% less space than competitive solutions and, in most cases, is smaller than even the controller alone.

Getting rid of the memory bus also reduces power consumption. Much of the power used by a discrete design is spent driving signals to and from the frame

buffer. Moving this interface onto the chip eliminates many power-hungry pad drivers. As a result, the NeoMagic chip consumes less than 400 mW when operating at 3.3 V, about 50% less power than discrete solutions.

This power level can be reduced further by using standby and suspend modes. The former mode reduces consumption to less than 25 mW while continuing to refresh the screen; writes to the frame buffer are not permitted. In suspend mode, less than 1 mW maintains the DRAM contents.

A side effect of the integrated configuration is reduced electromagnetic interference (EMI) problems. Containing all high-frequency signals, including the memory bus, inside the chip cuts down on EMI, simplifying the system package design.

Integration also reduces manufacturing cost. The company would not reveal the exact die size of its part, making a precise comparison impossible, but the silicon cost of a single 16-Mbit-type device should be less than that of the three die in the discrete solution. In addition, the cost of a single 176-pin package is much less than that of a 208- or 240-pin PQFP plus two 40-pin SOJs for the DRAMs. NeoMagic would not reveal its foundry other than to say that it is a major Asian DRAM vendor.

From a system designer's standpoint, price, not manufacturing cost, is important. NeoMagic expects volume pricing for the NM2070 to be less than $75. Despite the cost savings noted above, the company is charging a premium for its solution, based on the reduced power and footprint of its design. Based on our cost analysis, we expect that the company will offer significant discounts for very large purchases.

NeoMagic expects the higher performance of the NM2070 to help justify its price. At 400 Mbytes/s, the part has four times the memory bandwidth of a typical notebook controller, which cannot even keep up with PCI. The new chip can accept data from the PCI bus at full speed and has enough headroom for accelerated drawing operations.

The chip's memory bandwidth is greater than that of 64-bit VRAM or EDO DRAM designs used in high-end desktop PCs, although the NM2070 controller does not offer the same feature set as high-end desktop controllers. NeoMagic expects its device to achieve more than 30 WinMarks with a Pentium CPU, exceeding the performance of most notebook controllers and matching the speed of midrange desktop chips.

Expanding Options for Notebook Designers

As notebook systems move to DX4 and Pentium processors, the graphics subsystem becomes a performance bottleneck. Notebook designers are loath to move to the wider frame buffers and more exotic memory chips used in desktop systems, because these alternatives increase board space and power consumption, critical factors for mobile systems. Yet the traditional 32-bit DRAM interface lacks the bandwidth to keep up with these fast new processors.

The NeoMagic chip gives notebook systems better graphics performance, similar to that of desktops, while reducing power and board space. The notebook designer can use these savings to offer a smaller system with longer battery life. Alternatively, these savings could allow for increasing the processor speed or adding other features without decreasing battery life.

Many corporations today are replacing desktop computers with portable systems. For mobile users who need a portable system, this move eliminates the cost of supporting a second PC on the desktop. Yet current notebook systems can't match the performance of the latest PCI-based Pentium PCs. NeoMagic hopes that its offering will help notebook designers close this gap.

Opportunities and Challenges

NeoMagic will be challenged to achieve the cost savings promised by the integrated design. Although the economics of die area favor integration, other cost factors come into play. It is always difficult to compete against a commodity technology, such as DRAM, because the higher volumes of standard parts drive down manufacturing cost, and the competition between multiple vendors keeps margins to a minimum. The price of 4-Mbit DRAMs, which have reached maturity, is now low, while the price of 16-Mbit parts remains artificially high, exacerbating NeoMagic's challenge.

Combining memory and logic raises other manufacturing issues, as the two device types are typically built using different IC processes. Some vendors, notably Toshiba, have developed processes that handle both, but these tend to be more costly than a stock DRAM process.

The NM2070 is NeoMagic's first product, but the company plans to expand its product line in the future. With a larger die, the company could increase the frame-buffer size and/or add graphics and video acceleration features; variations like these are likely to be announced later this year. The company is also looking for additional opportunities to combine memory and logic: one possibility is a single-chip PDA processor with an integrated memory system. As transistor counts increase, options will abound for this innovative new company. ♦

Price & Availability

The MagicGraph NM2070 will begin sampling later this month at a price of $85 per unit. The company expects volume production in 3Q95 with 1,000-piece pricing below $75. Contact NeoMagic (Santa Clara, Calif.) at 408.988.7020; fax 408.988.7032.

