NEC 3D Hi-Performance Graphics Accelerator(TE4)

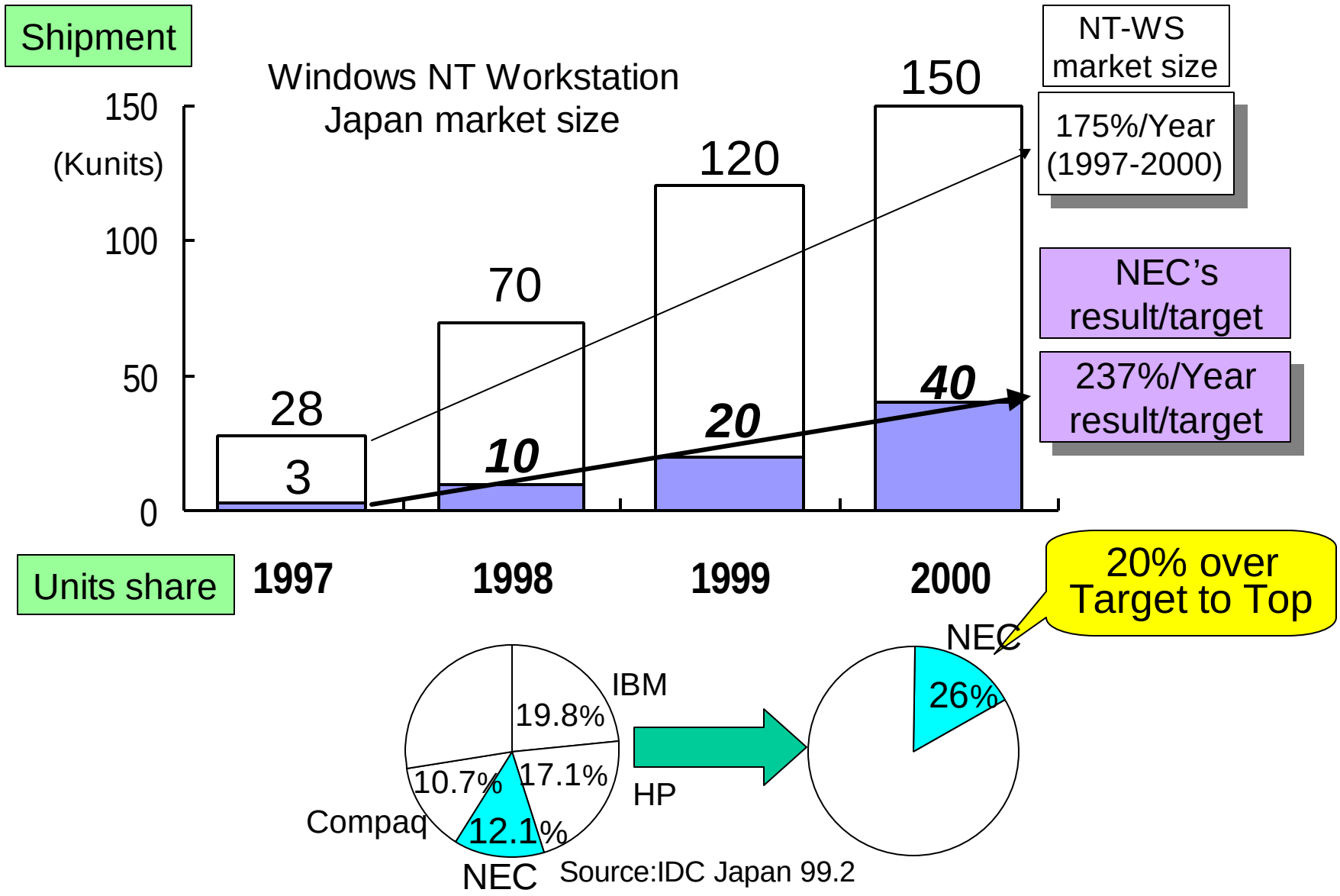
Aug 1999

NEC Corporation

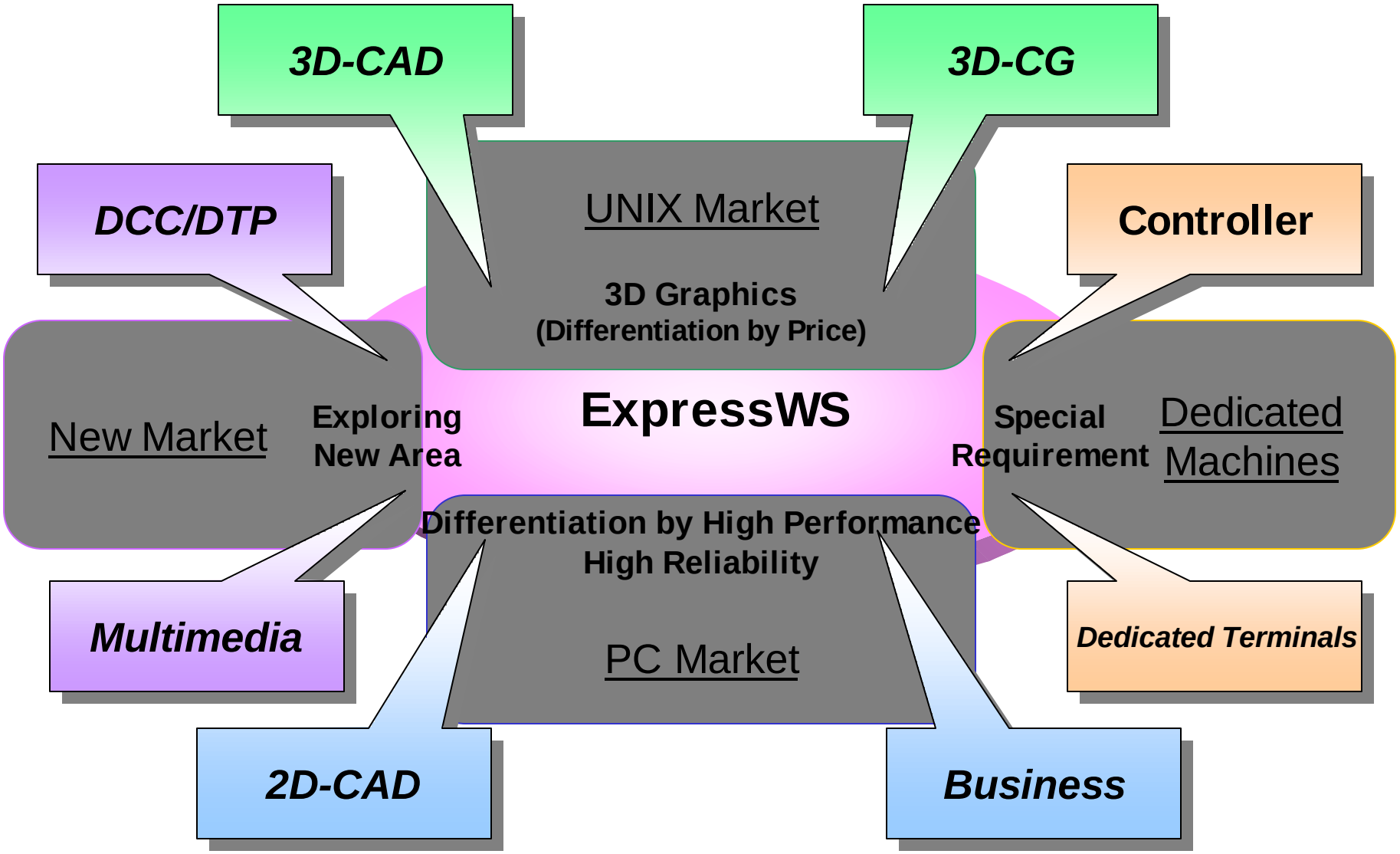
NEC

NEC Express5800/50 series Work Station

Market size and NEC's performance



Market Segment



Product Strategy

Express5800 Workstation

- Leading-edge CPU technology
  - Simultaneous product launch with Intel's latest CPU announcement

- High-performance Graphics
  - Fastest Graphics (NEC Designed) TE3A/TE3AL, TE4
  - Excellent performance driver

- High-reliability / Easy-to-use
  - Easy set-up using ExpressBuilder
  - Express remote monitor
  - ESMPRO system management
  - Remote wake up

- Wide-range AP certification

  I-DEAS, ProEngineer, SolidWorks, Mechanical Desktop etc.

Current Line-Up

LowEnd | Midrange | HighEnd

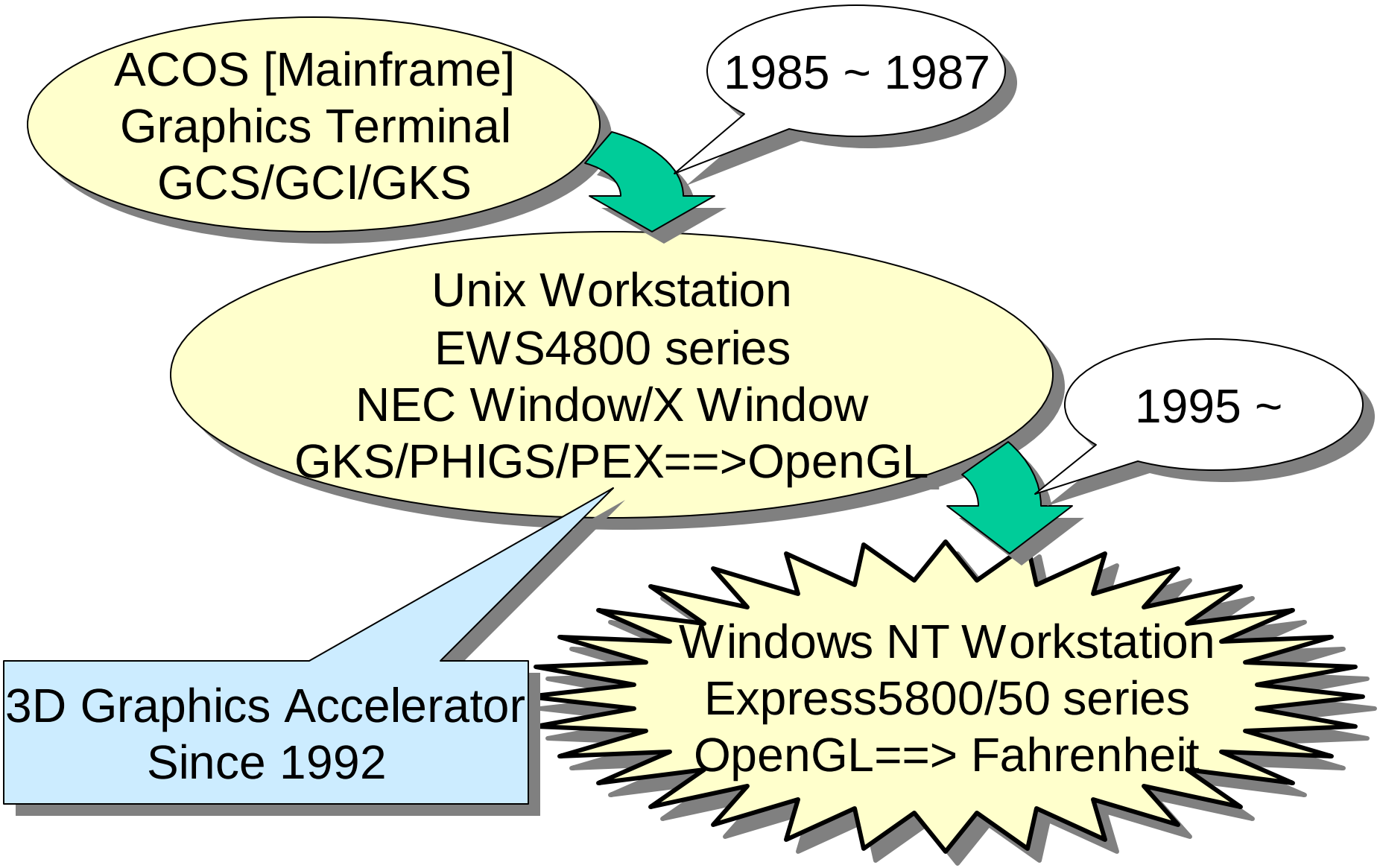
Express5800/53Wc	Express5800/55Wb	Express5800/56Wb	Express5800/58Wa
			
Pentium II(350/400) Pentium III(500/550) X1CPU 2D/Entry3D model	Pentium III(500/550) X1~2CPU Midrange CAD/CG	Pentium III Xeon(500/550) X1~2CPU Highend CAD-CG	Pentium II Xeon(400) X1~4CPU Analysys/E-CAD

Dedicated Terminal WS	3D-CG	
2D-CAD(Mechanical)		2D-CAD(IC/LSI/Circuit Design)
Entry3D-CAD(Mechanical/Architecture)	3D-CAD(Mechanical/Architecture)	
	GIS	Analysis/Simulation

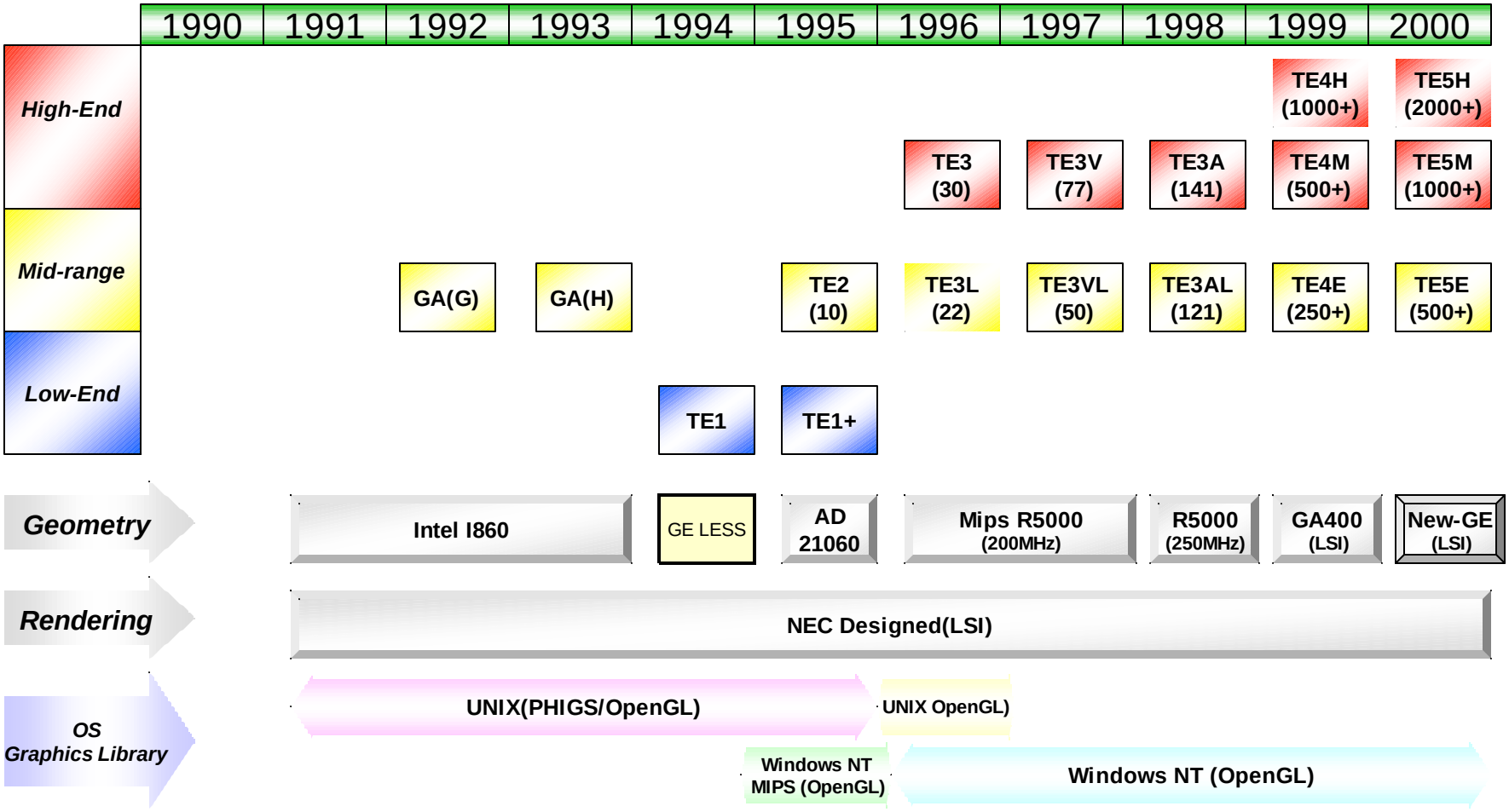
Graphics Accelerator TE4

Specifications
&
Architecture

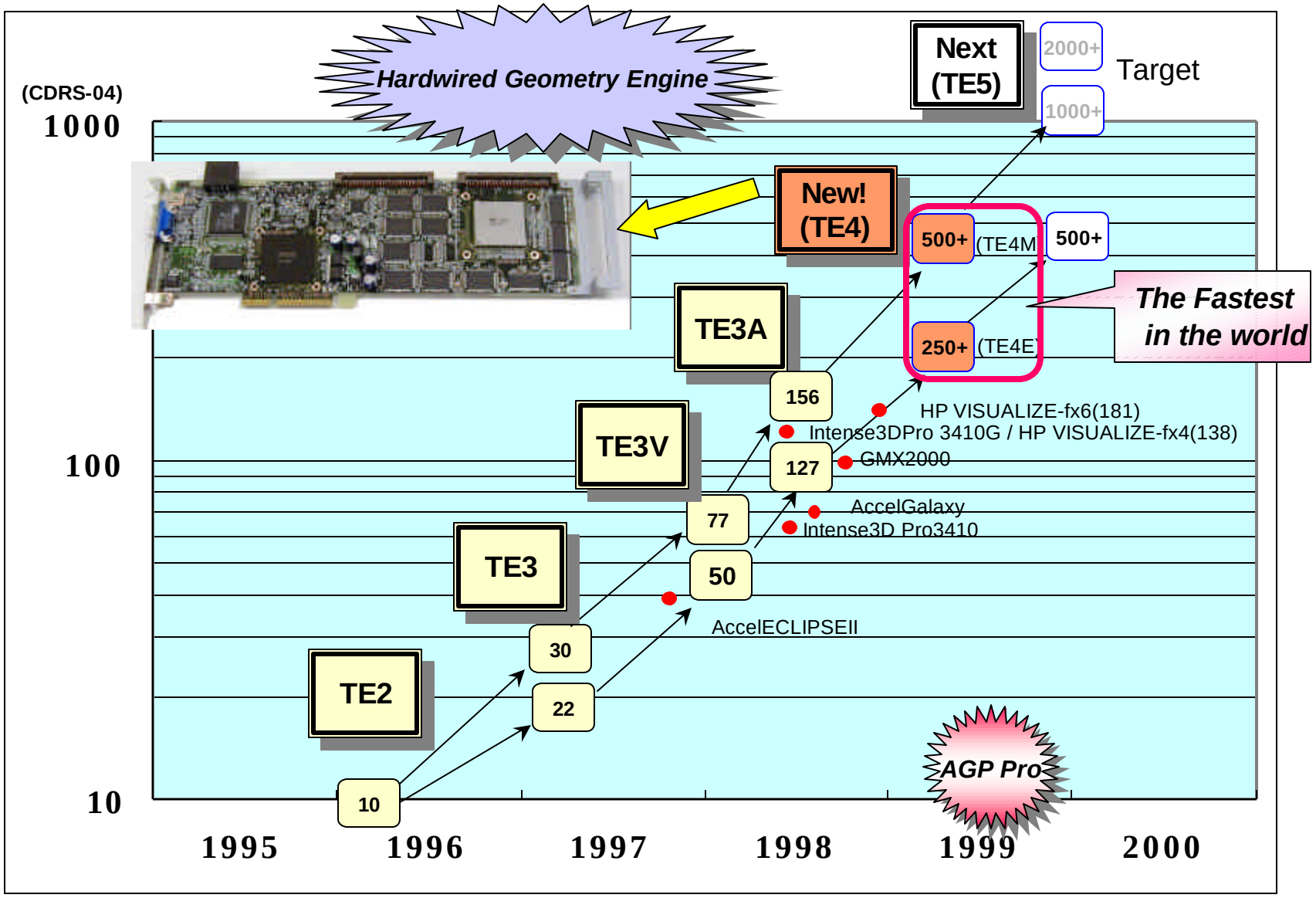
Platform/Window System/Graphics Library



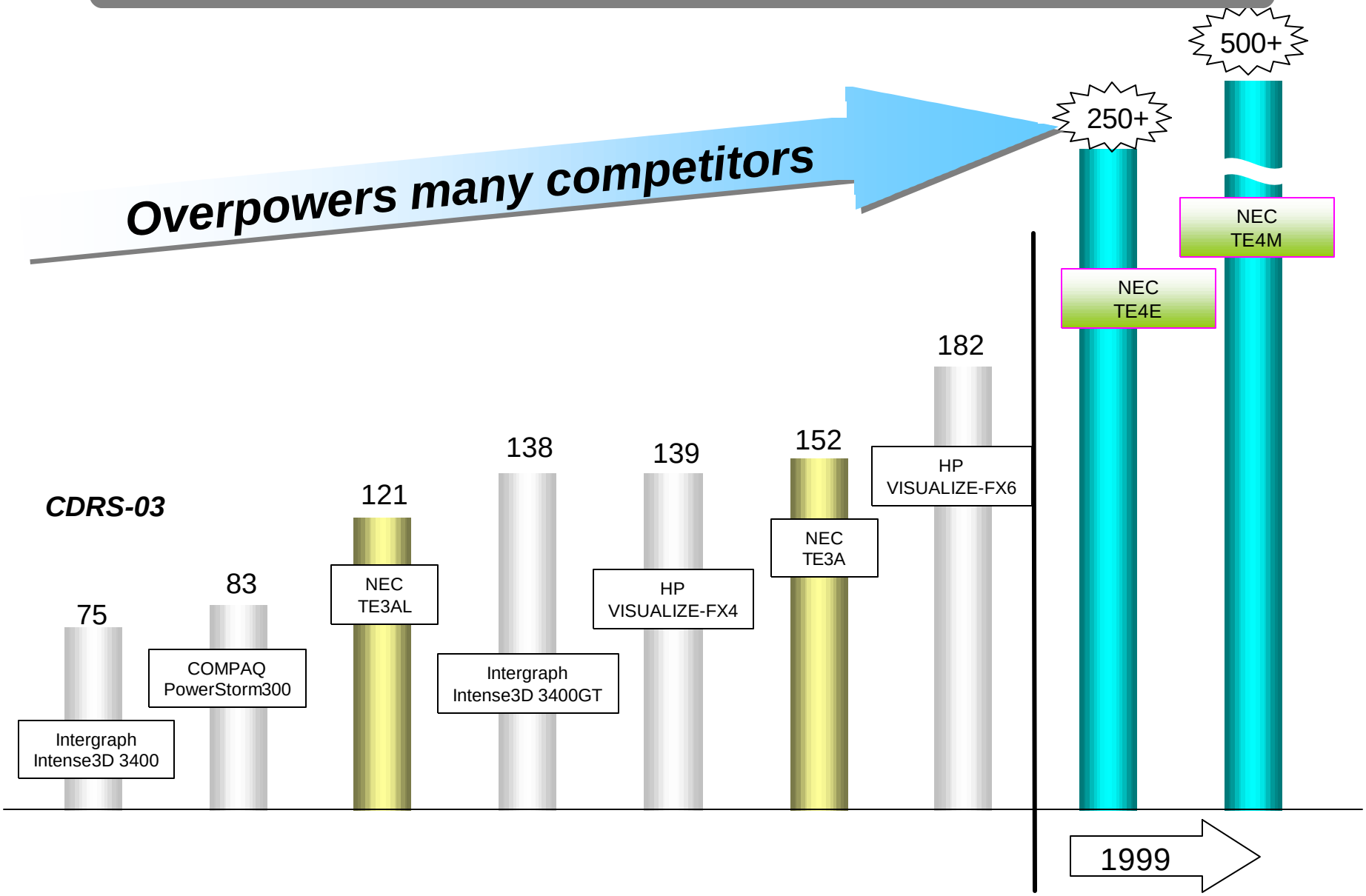
NEC 3D Graphics Accelerator Update



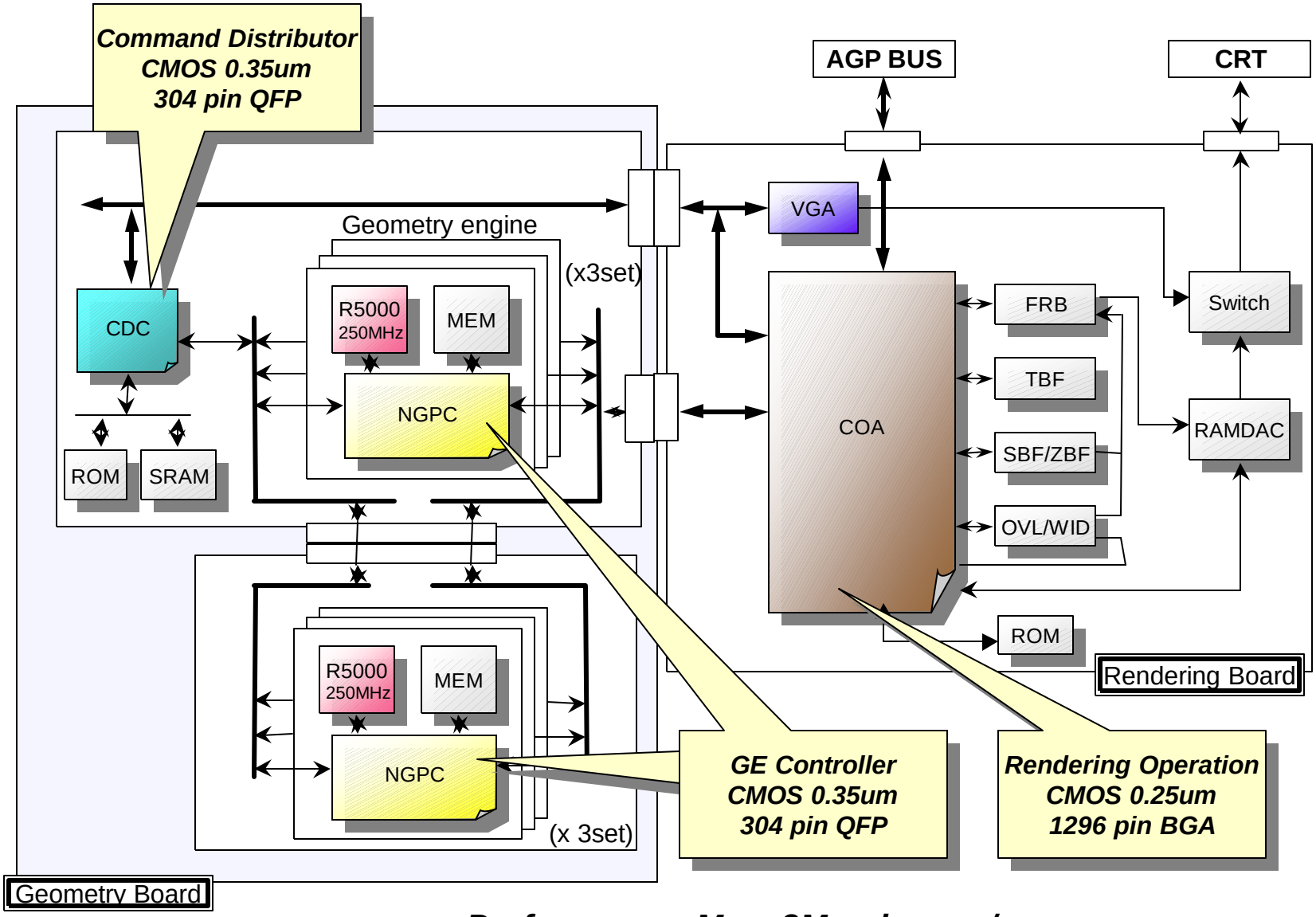
NEC 3D Graphics Accelerator TE series Roadmap



Next Generation 3D Graphics Accelerator TE4



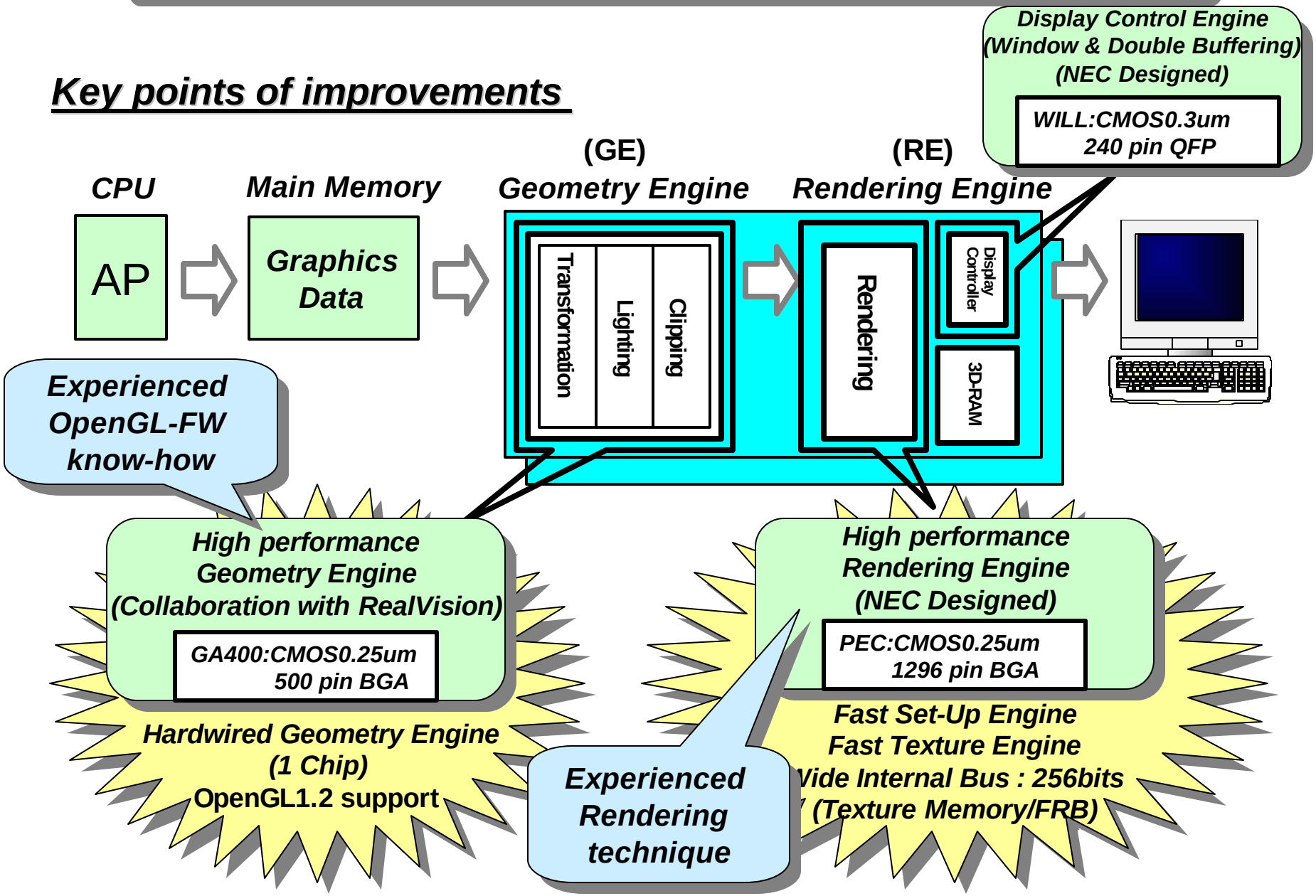
Old Product : 3D Graphics Accelerator TE3A



Performance: Max. 3M polygons/sec.

TE4 Architecture

Key points of improvements



Specification

•***Render function***

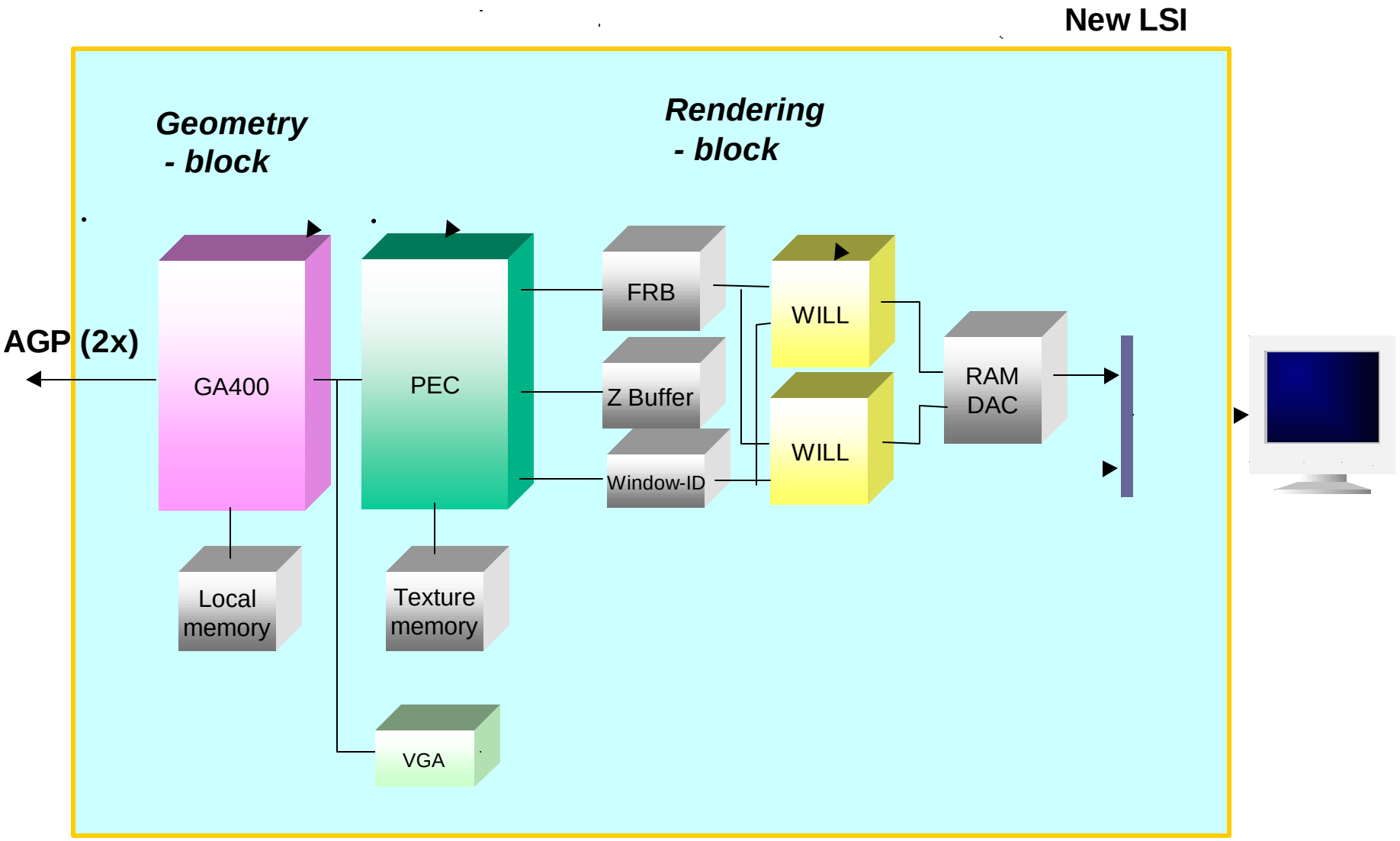
Item	Description
•Point, line, and triangle draw / Bit BLT / Fast clear	
•Gouraud shading	
•Z-buffer	24bit *or* 32bit *alternative*
•Stencil Plane	8bit *or* 0bit *alternative*
•Alpha Plane	8bit
•Very high quality anti-aliased lines,point,polygon	
•TextureMapping:Bilinear and trilinear filtering Mip mapping	64MB
•Perspective Correction	
•Fog	
•Window ID	8plane
•Overlay Plane	8bit x 2
•Per pixel double buffering	
•VGA support	on board
•Resolution	1280x1024-640x480 True Color

Specification

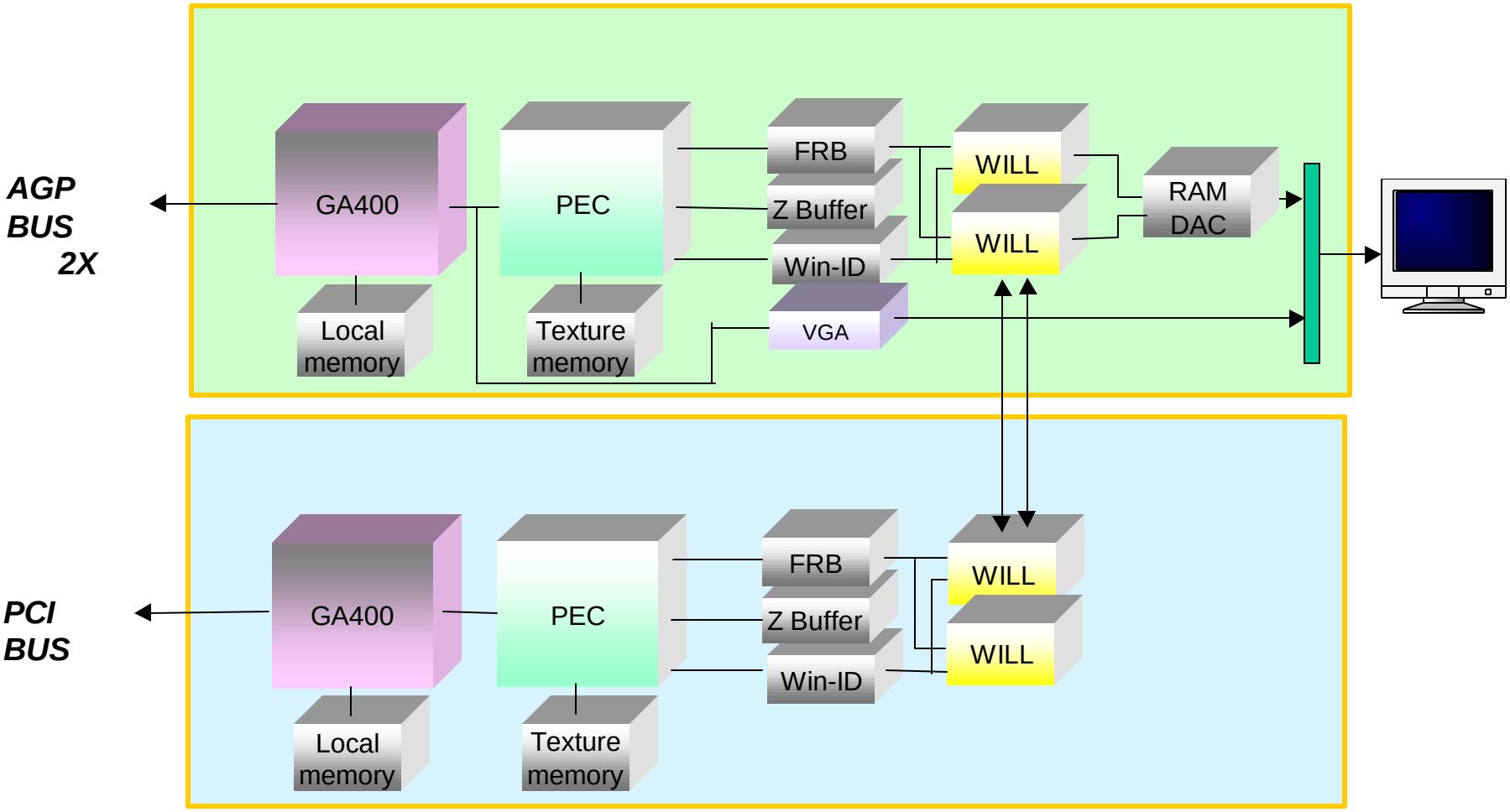
•***Geometry function***

Item	Description
***AGP/PCI Interface**	**AGP 32bit/66MHz 2x mode**
***2'nd PCI Interface**	**special PCI 64bit/66MHz**
***Local Memory control (command buffer / element buffer)**	**64MB**
***DMA data path priority scheduler**	**Low-priority / High-priority**
***Operational light source number**	**16 lights source**
***Operational floating point performance**	**9Gflops**
***Operational Vertex performance**	**12.5M vertices/s**

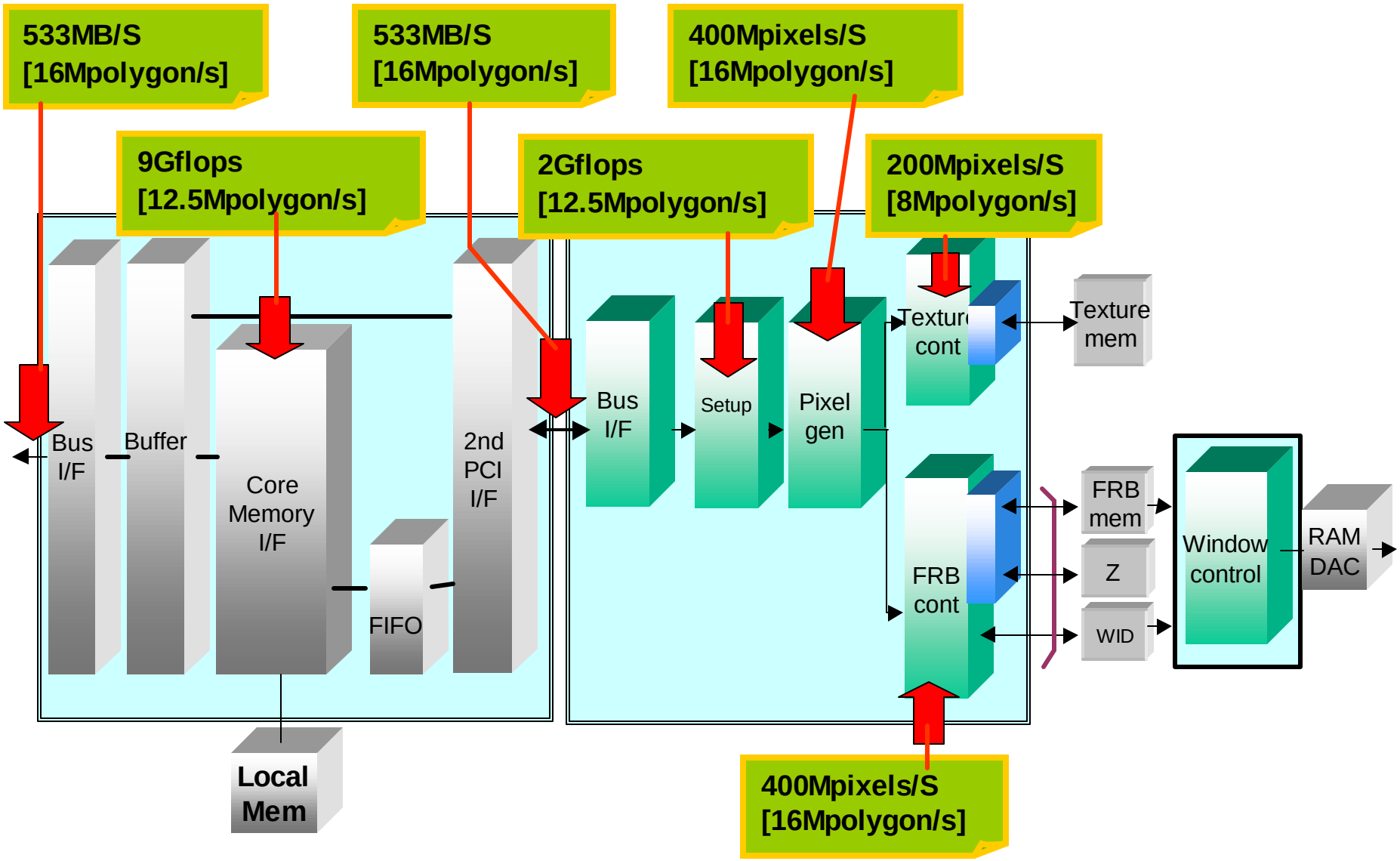
•TE4E Block Diagram



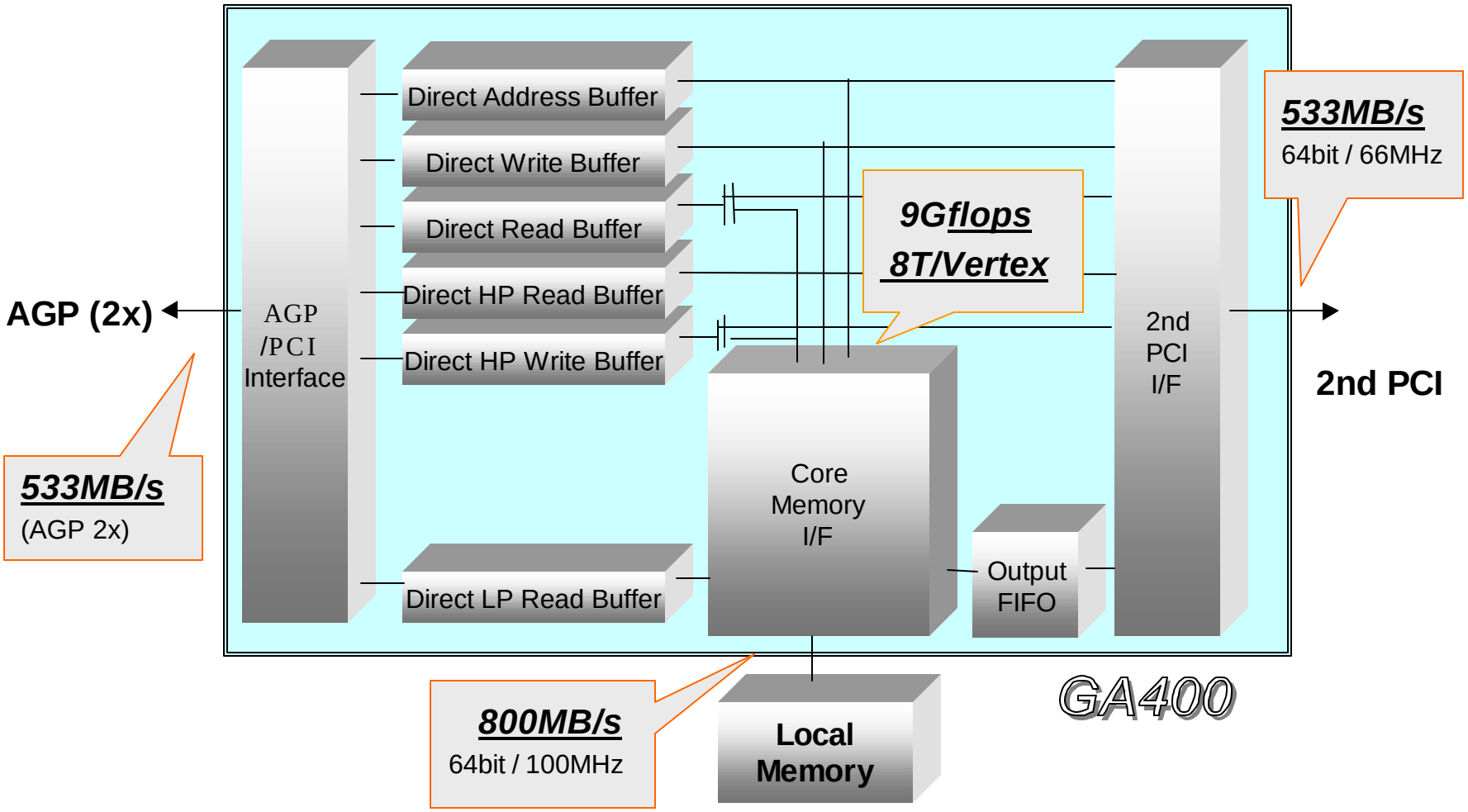
•TE4M Block Diagram



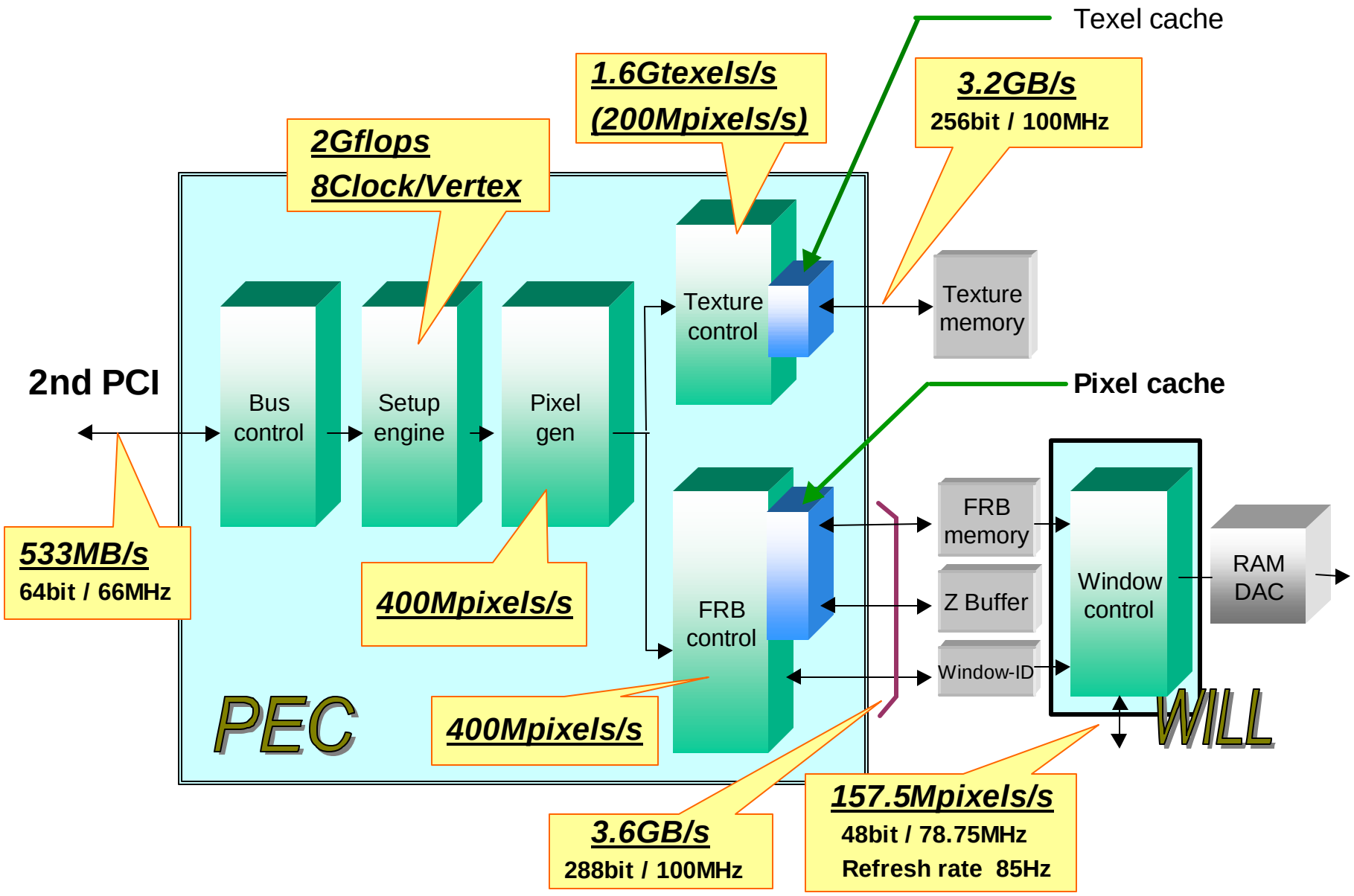
•Hardware performance Data



[Geometry Block(detail)]

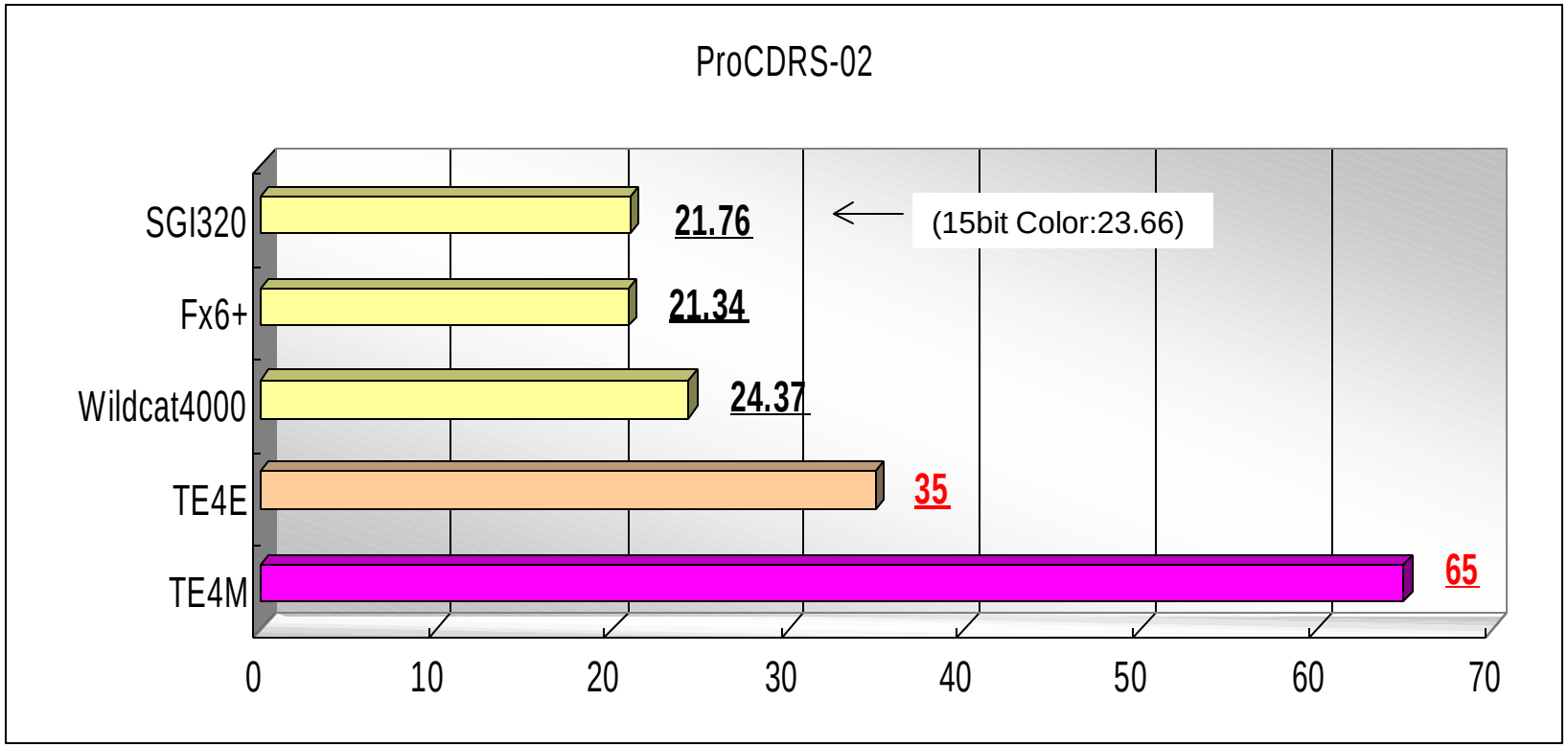


[Rendering Block(detail)]



•Benchmark Data

[Performance(ProCDRS-02)]



=Reference Condition=

TE4M: (estimate) 1280x1024 TrueColor

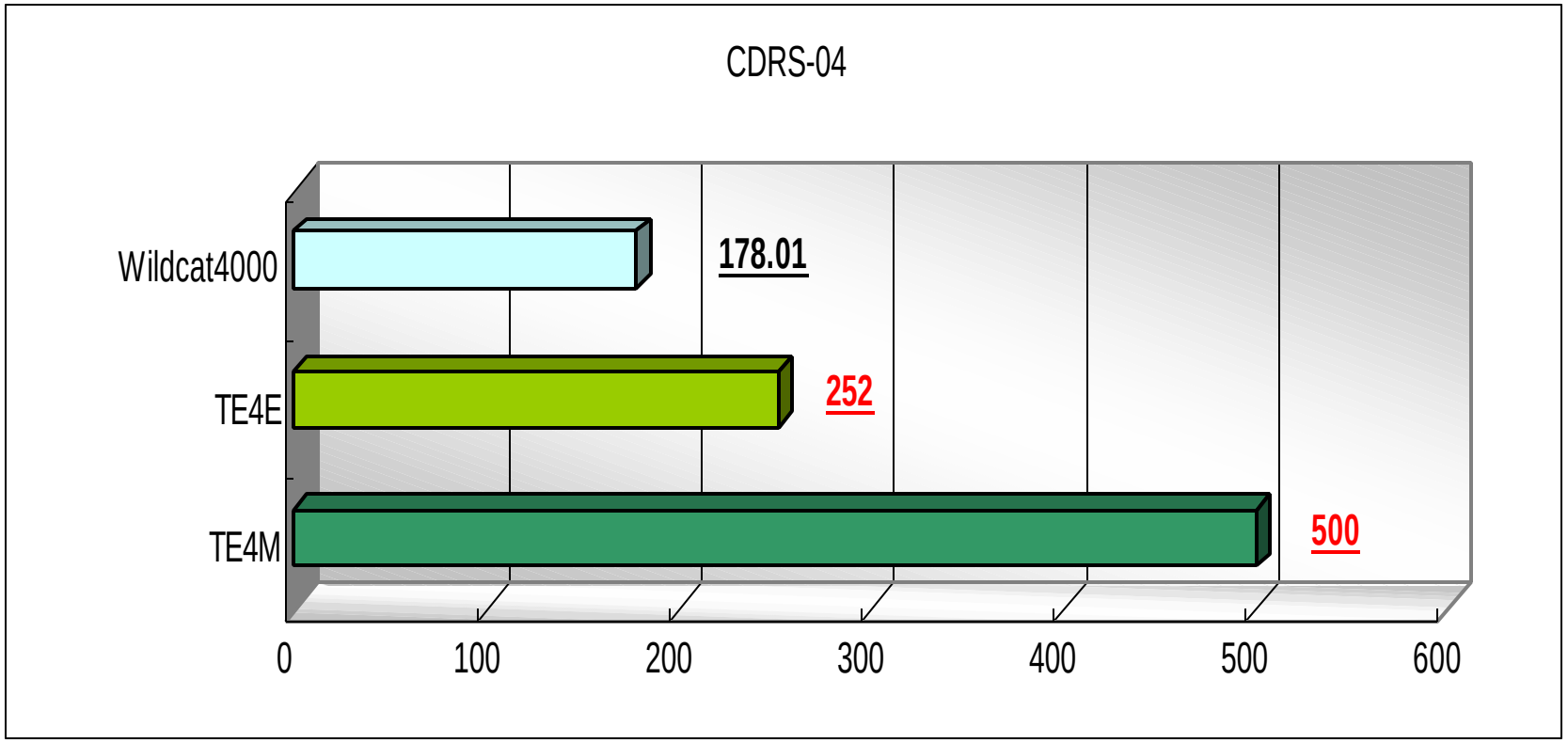
TE4E: 1280x1024 TrueColor

Wildcat4000:Intense3D Web-site - http://www.intense3d.com/scores.asp

Fx6:GPC-site http://www.specbench.org/gpc/opc.data/procdrs-perf.html

SGI320:SGI Web-site -http://visual.sgi.com/research/data/benchmarks.html

[Performance(CDRS-04)]



=Reference Condition=

TE4M: (estimate)1280x1024 TrueColor

TE4E: 1280x1024 TrueColor

Wildcat4000:Intense3D Web-site - http://www.intense3d.com/scores.asp

•Detail Performance for each function block

Setup engine

- operation : 8cycles/vertex for groud mode

  for 8 elements(X,Y,Z,R,G,B,a,C)

  12.5Mpolygon/s (frequency100MHz)

- operation : 11cycles/vertex for texture mode

  for 11 element(X,Y,Z,R,G,B,a,U,V,W,C)

  9Mpolygon/s (frequency:100MHz)

Pixel gen

- operation : 4pixels/cycle for groud mode

  Peak 16Mpolygon/s (400Mpixels/25pixels)

- operation : 2pixels/cycle for Texture mode

  Peak 8Mpolygon/s (200Mpixels/25pixels)

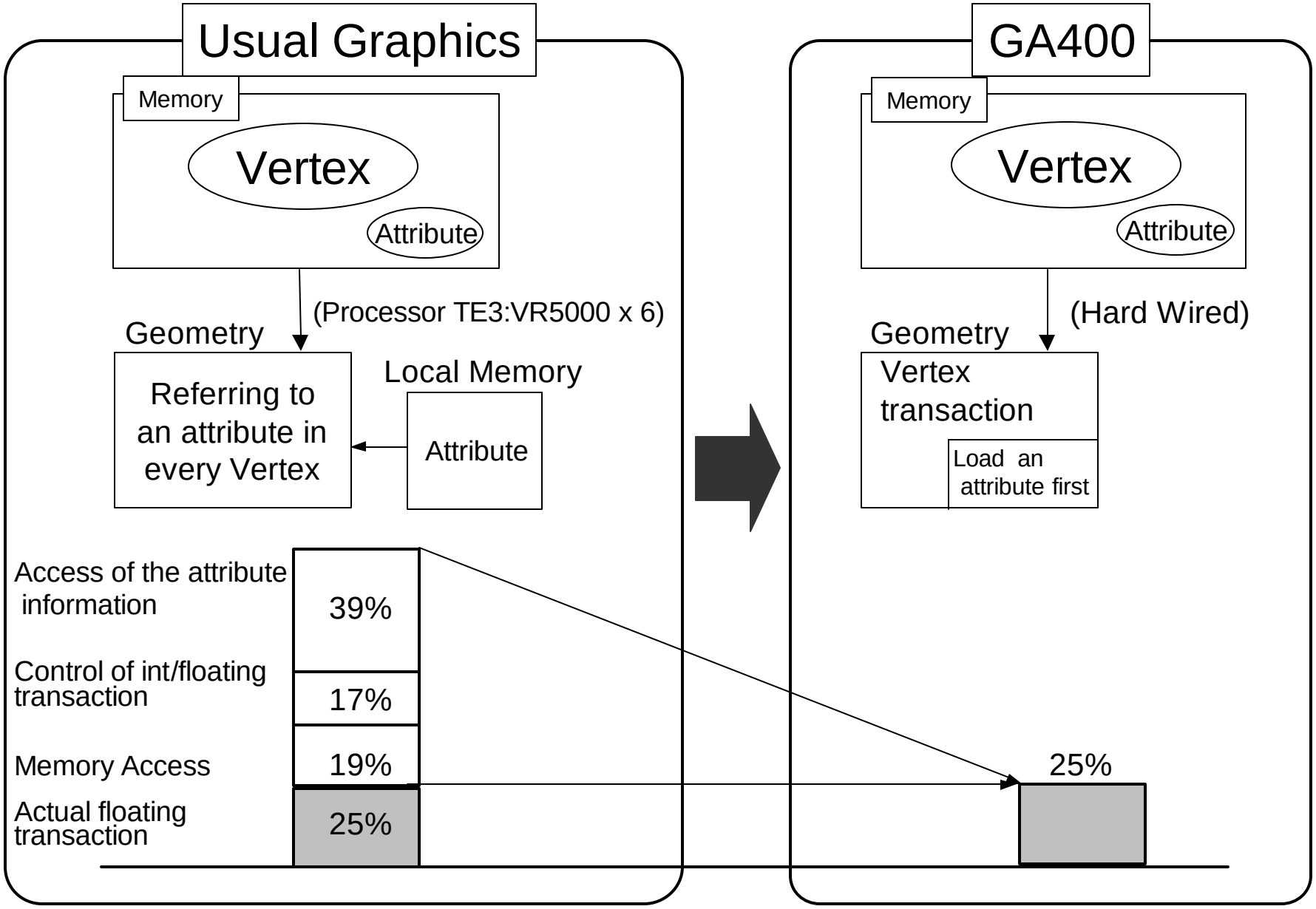
Texture gen

- operation : 2pixels/T(all filtering mode)

  200Mpixels/s(frequency:100MHz)

Hi-Speed Geometry 1/2

Advantage of the Hard wired



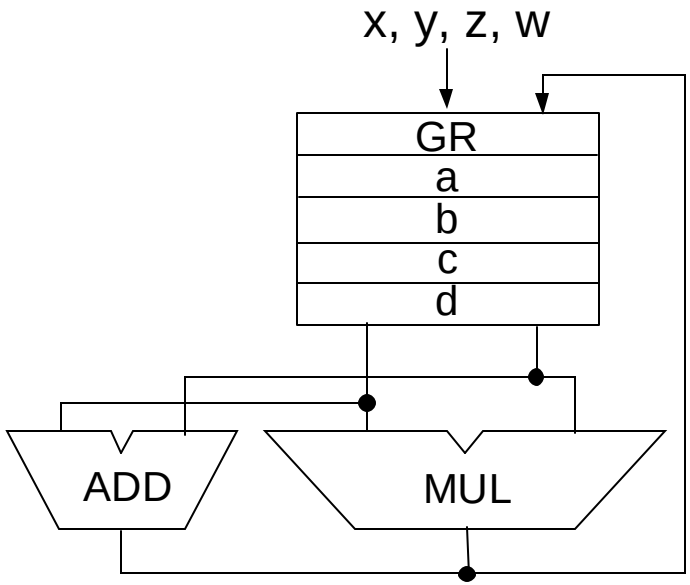
Hi-Speed Geometry 2/2

Parallel of the operation

$$(x, y, z, w) \begin{pmatrix} a \\ b \\ c \\ d \end{pmatrix} = ax + by + cz + dw$$

Vertex — Attribute

Usual : Processor

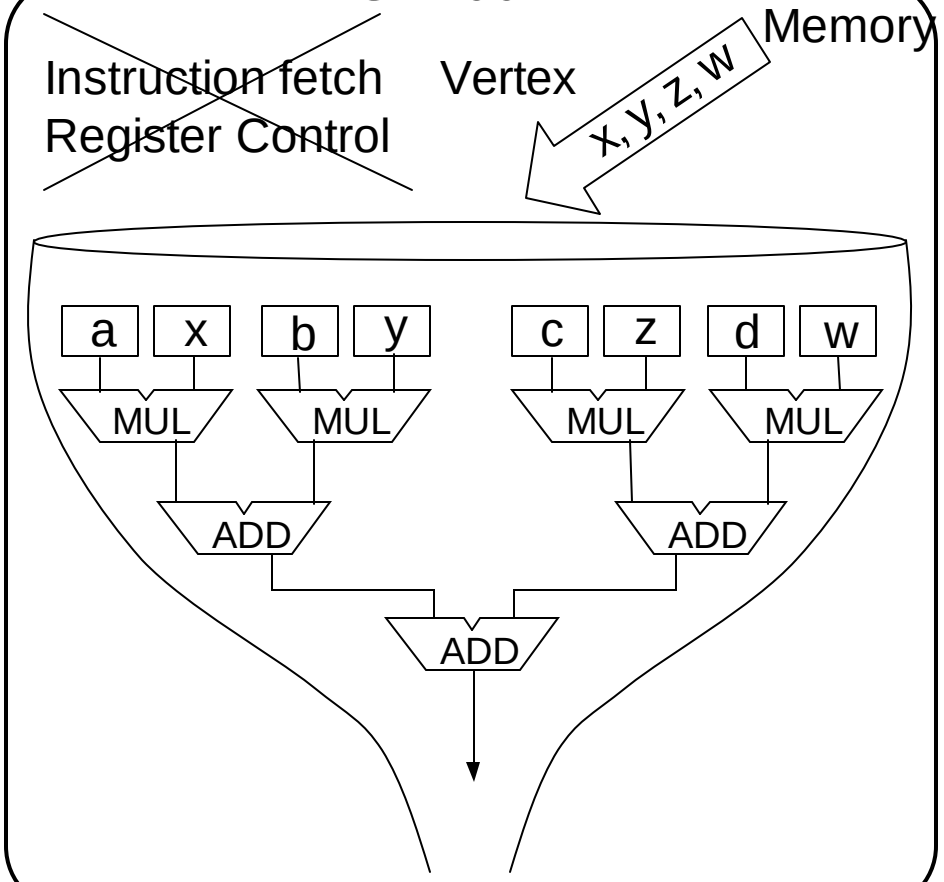


Proccessor FW Processing

GR ? a Xx
GR ? GR+b X y
GR ? GR+c X z
GR ? GR+d X w

Order fetch and control of a register are nece -ssary except that the following is computed.

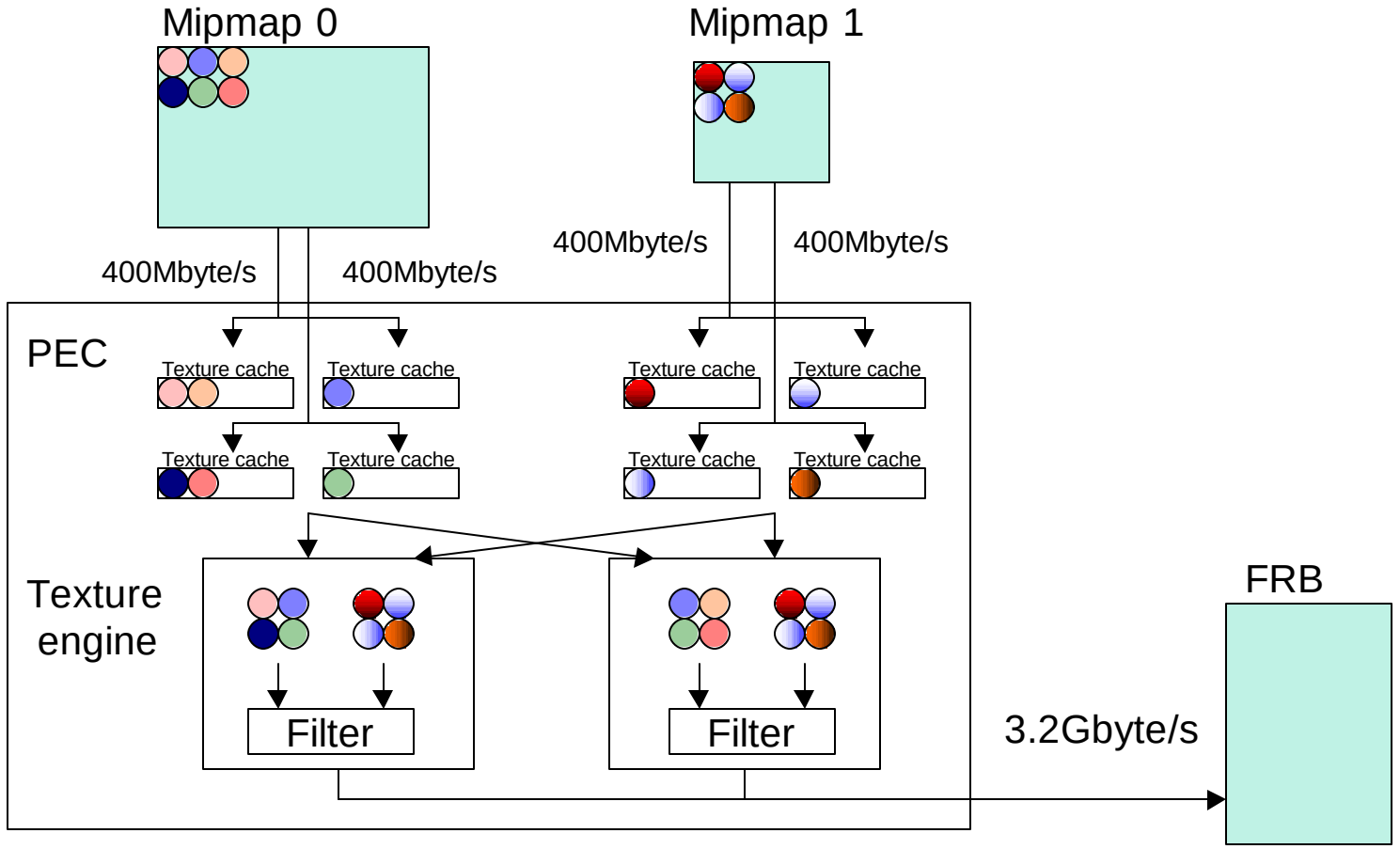
GA400



Hi-Speed Texturing

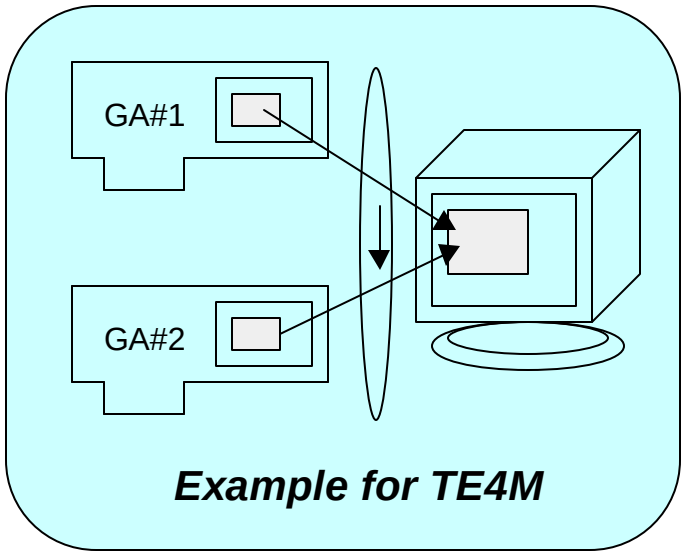
TE4 texture performance = **200Mpx/s** (Tri-linear filtering)

- **Two texture engine**(100Mpixel/s per engine)
- **Four texture memory controller**(400Mbyte/s per controller)
- **Eight texture Cache** which has two independent read port (400Mbyte/s per cache)

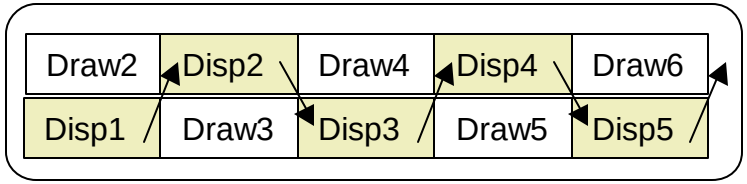


•TE4M Architecture

[Multi-screen-transfer architecture]for Scalable



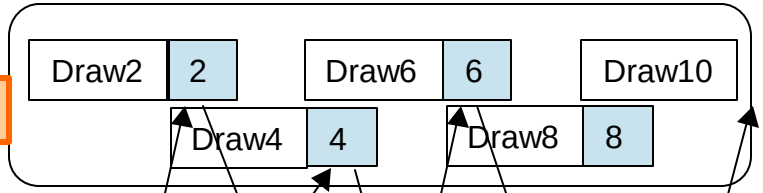
1PKG (TE4E)
:double-buffering



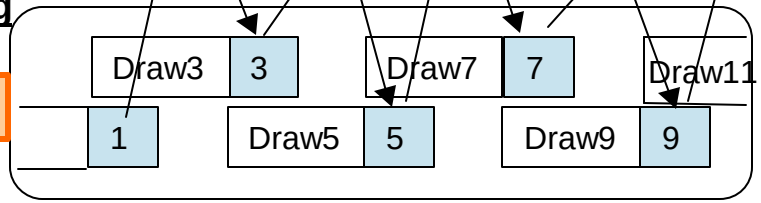
To CRT

2PKG (TE4M)
:double-buffering

GA#1



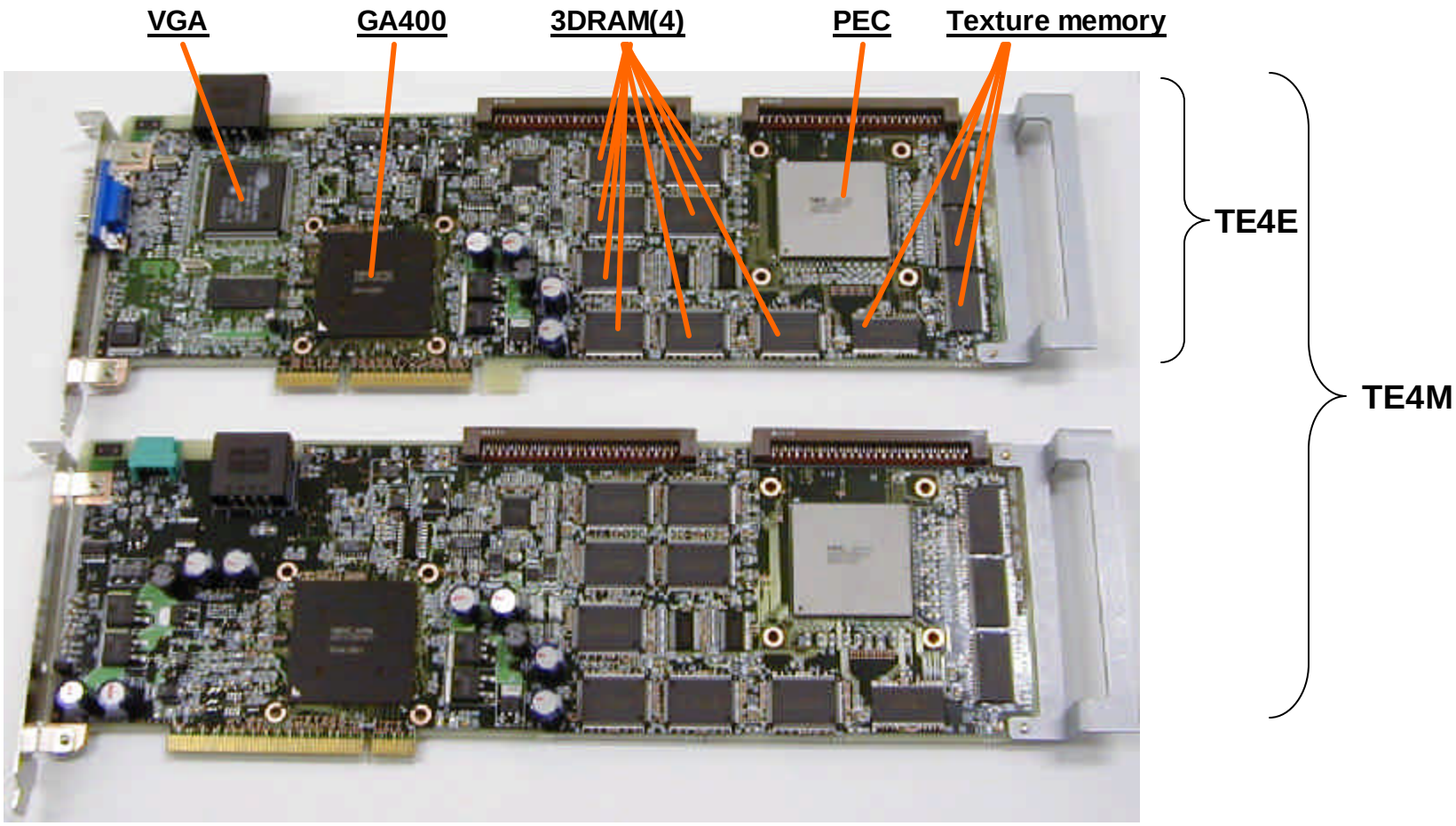
GA#2



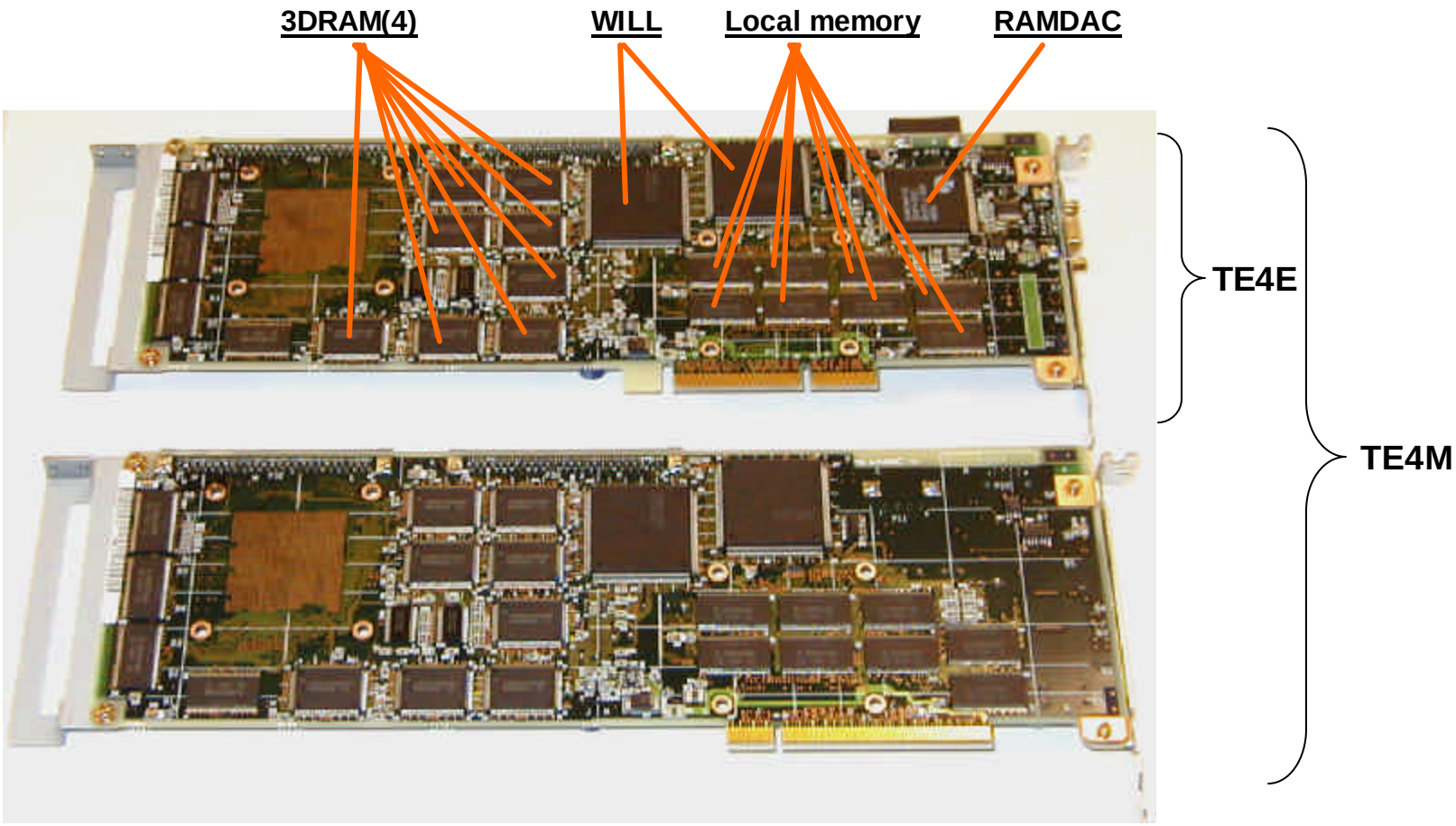
To CRT

Double Performance compared withTE4E

•PKG Layout (front view)



•PKG Layout (rear view)



- Key Devices

GA400	PEC	WILL	3DRAM
Geometory Engine	Rendering Engine	Window controller	Frame Memory
500pin BGA 0.25um(3.6MG)	**1296pin BGA 0.25um(3.5MG)**	**304pin QFP 0.35um(80KG)**	**240pin BGA eRAM(40Mb)**
			

NEXT Generation (TE5xx)

Target!!

Improve the performance

by 2X to 10X that of the TE4E


NEC