NCR AIMS ITS GRAPHICS CHIPS AT PC INSTEAD OF WORK STATION

COST OF MANUFACTURE IS DRIVING FORCE BEHIND 3.75-MIPS CHIP SET

Most graphics controllers and processors have been aimed at the high-performance—and higher-cost—business and engineering work-station end of the market. But NCR Corp. figured that the vast middle ground, the lower-cost but higher-volume personal computer market, was ready for a sophisticated graphics processor that could meet the market's demands at a reasonable cost. The vehicle for its strategy is a two-chip graphics-controller set—the NCR 7300 color graphics controller and 7301 memory interface controller.

"The trend in graphics is to load more and more software into hardware," says Alan Loftus, director of logic products at NCR's Microelectronics Division in Colorado Springs. "The more you can make chip-resident, the more powerful the controller or processor will be and the faster it will work. But it must be implemented with ultimate costs in mind." The company's solution was a two-chip implementation with a parallel architecture that handles color, windowing, and sophisticated text handling. "A picture may be worth a thousand words, but if you don't have 10 or 20 lines of text to describe what's going on, it won't be worth anything," says Loftus.

NCR combined standard approaches to graphics implementation such as frame buffering and presenting text in a graphics representation with innovative techniques such as a dual-text mode that allows generation of standard ASCII text, a variable memory-word width, a cache-memory drawing technique, and a two-stage color-lookup table. It also based its strategy on a stricter adherence to emerging graphics standards than many graphics processors currently on the market.

The 7300/7301 graphics chip set is fabricated using a 2-μm dual polysilicon n-MOS process. Despite the conservative design rules, it operates at an impressive 3.75 million instructions per second and can drive displays at rates up to 30 MHz, and it performs bit-block screen transfers at rates up to 2 million pixels per second.

The set's parallel architecture varies memory word width as the number of supported bit planes varies. This architecture uses memory more efficiently and allows the system to be expanded and upgraded easily.

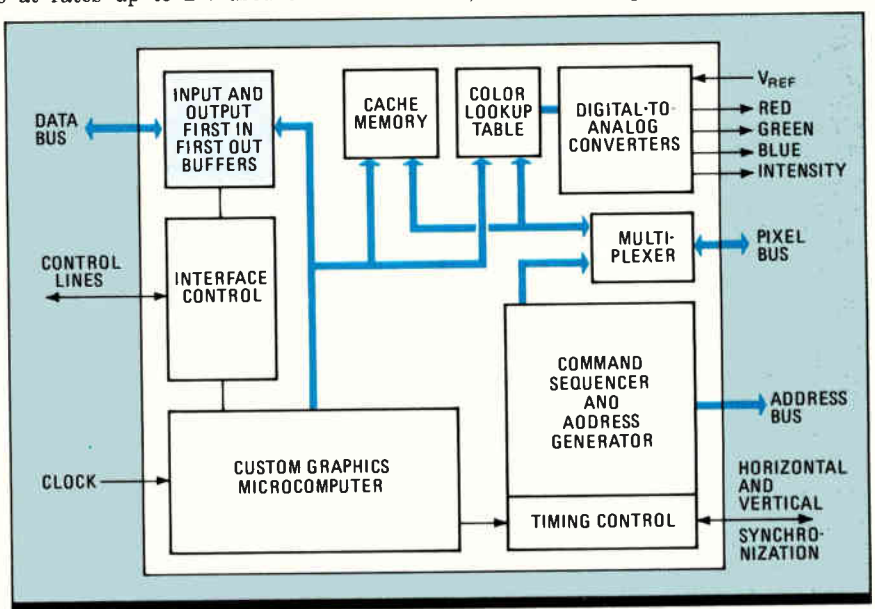
The system's variable word width and a cache-memory drawing method create high-performance graphics and the ability to use commercially available dynamic random-access memories, according to Loftus. The cache-memory drawing method uses an on-chip sequencer to refresh the display, while the drawing processor draws images to the cache memory. During display blanking intervals, the images in the cache memory are downloaded to the frame buffer. This approach draws images quickly without producing flashes on the display and allows the use of commercial DRAMs.

The 7300 color graphics controller (Fig. 1) contains a high-performance graphics processor that takes over many of the tasks usually performed by the host processor. It contains independent input and output first-in first-out registers, each 16 bits by 16 words deep. Although it has an 8-bit internal architecture, the interface logic works equally well for 8- or 16-bit processors. The FIFO registers are used for transferring commands and pixel data. The command register is utilized to specify the data bus width (8 or 16 bits), to handle resets, and to initialize handshake signals for DMA transfers. The status register holds FIFO-register status indicating when the output-FIFO register is empty. The Ready line signals input-FIFO-register status during write operations and output-FIFO-register status during reads.

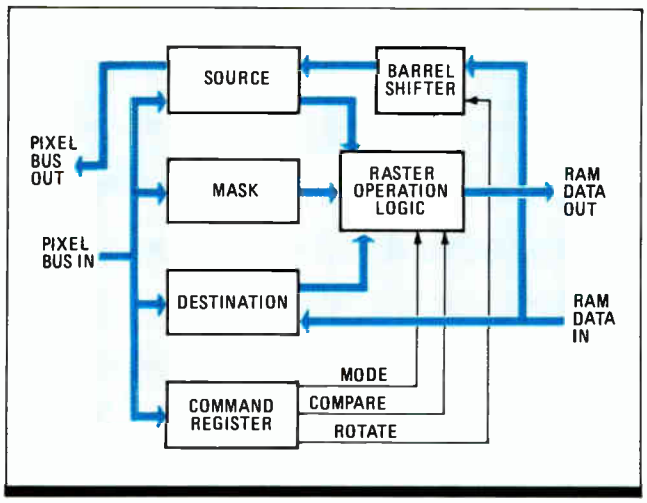
The cache memory is the key to a system that can produce video rates of up to 30 MHz while using standard commmercial DRAMs for the frame buffer. While the graphics microcomputer is drawing to the cache memory, a hardware sequencer performs the display refresh. The image in the cache is downloaded to the frame buffer. This design approach was chosen over an interleaved memory access, which would have required a higher memory bandwidth and faster, more expensive DRAMs.

A frame buffer of up to 1,024 by 1,024 pixels with 8 bits per pixel can be supported. The 7300 provides 8-bit row and column address strobes as well as read/write, CAS_1, and CAS_2 signals. The RAMs are automatically refreshed by a RAS-type refresh controller. The frame buffer uses absolute—that is, X-Y—addressing, which eliminates linear-address-to-screen-address conversions, a common technique that, however, slows the system and screen response time.

Because the 7300 can support up to 8 bits per pixel, NCR decided to divide the color lookup table into two four-bit subtables—a hue lookup table and an intensity table—for greater flexibility. Bit planes 0 to 3 are called the hue address and are used to select 16 of 4,096 hues. Bit planes 4 to 7 are the



1. MIGHTY MIX. The 7300 graphics controller combines a 16-bit graphics processor with cache memory, lookup tables, and logic. It performs many tasks usually done by the host.



2. MEMORY INTERFACE. Operating in parallel with the 7300, the 7301 memory interface circuit supervises memory-access operations.

intensity address and are used to select 16 of 32 intensity levels. When the hue data is decoded in the lookup table, one of 16 words is selected. These words are 12 bits wide and contain 4 bits each of red, green, and blue values. Each of these values is then multiplied by the intensity and converted to an analog output signal. In combination, the hue and intensity can provide 256 colors from a palette of about 60-K distinguishable colors.

GKS COMMAND SET

Strict adherence to a graphics standard was one of the major design goals for the 7300. A high-level command language simplifies and speeds the work of the systems programmer. Adherence to a graphics standard means that subsequent design changes are much less likely to force a major rewrite of system software.

Of the various graphics standards proposed (see p. 64), the NCR designers chose the American National Standards Institute's Graphics Kernel System standard. The 7300's on-board instruction set holds 25 GKS-compatible graphics, timing, and control commands. The advantages of using a GKS-based instruction set are device-independent software and portability of software among systems that run GKS, according to Loftus. In addition, many of the functions supported by the standard adopted by IBM Corp. in its Personal Computers are directly implemented in hardware by the 7300/7301. This increases execution speed because it is not necessary to perform a software emulation of the functions.

But the main advantage, says Loftus, is reduced software-development costs. For example, if the application program is used to create slide presentations, these can be plotted using equipment from a number of manufacturers without changing any of the software. All that is needed is a device driver for the particular equipment. The 7300 driver provides immediate compatibility with a wide base of applications including those run under MS-DOS, PC-DOS, and Unix.

TEXT HANDLER

A limitation of most existing graphics-controller and -processor chips, even some of the most advanced, has been the inability to handle text efficiently, Loftus points out. Although powerful drawing features are useful, in practice most applications for graphics systems are still very text-intensive. The 7300 was designed to facilitate this common task.

A typical solution is to use an external character generator. The 7300, however, has the on-chip capability to generate a character set and store it in a portion of the frame buffer that is not being displayed. The size of the characters—both width and height—are defined by the user, and up to 256 characters can be defined in a set. Two full character sets can be active at one time, provided sufficient memory exists in the frame buffer. The bit-mapped character images are then accessed with 8-bit codes, which eliminates the usual bottleneck of passing images between the host processor and the graphics controller every time they are needed for display.

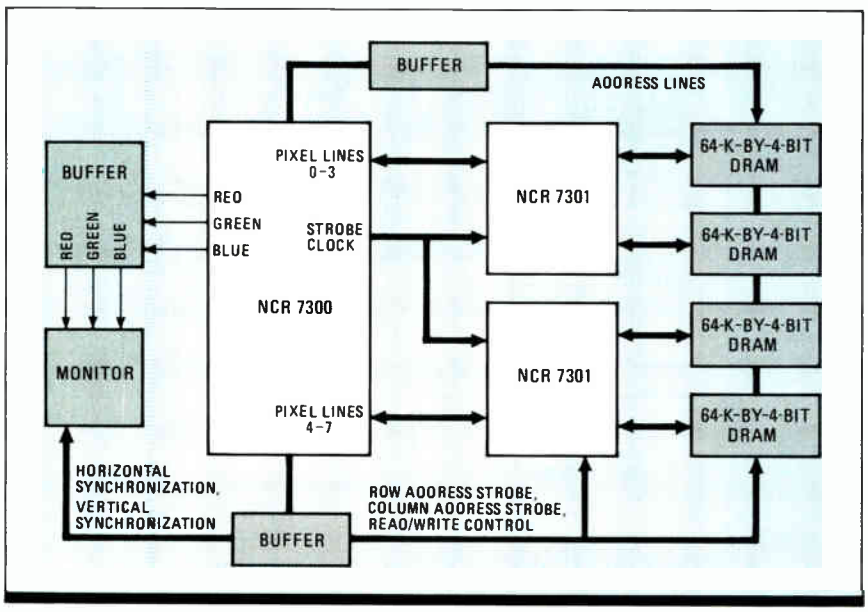
Dual text modes give the 7300 an added level of flexibility. In the Fastext mode, the 7300 generates standard ASCII-type text characters with user-selectable foreground and background colors. The graphics text mode provides proportionately spaced text drawn in any of four directions—up, down, right, or left—using a read-modify-write cycle. In this mode, the characters appear to be stenciled over the existing background.

Several text-handling features incorporated into the 7300/7301 chip set are especially useful for personal computer text-handling applications. These features are soft fonts and automatic lookup tables. The built-in soft-font capability permits the user to customize character sets by size and content and incorporate them into the text, and thus tailor the text to the application without using external character generators.

The auto lookup feature eliminates the bottleneck of passing bit-mapped images between the host and graphics processor every time a character is drawn. Instead, bit-mapped character images are stored in the frame buffer and are accessed with 8-bit codes.

The chip set allows display of up to eight full-width windows, plus viewports, says Loftus, making possible many of the window- and icon-management capabilities now done in software on most personal computers. Included in the chip's command set is a Move Viewport instruction, which allows block-copy transfers of more than 2 million pixels/s.

A feature not usually found on other graphics controllers and processors is the 7300's on-chip programmable color lookup table with overlay mode. This allows the user to display images in multicolors, or



3. LOW CHIP COUNT. With the 7300/7301 chip set, a 16-color display system having a 1,024- by 512-pixel frame buffer requires less than a dozen integrated circuits.

in a combination of colors and shades as the application warrants. The overlay mode provides a prioritized plane display in which images on higher-priority planes appear in front of images on lower-priority planes. Planes can be selectively written and displayed, enhancing windowing-type display formats. Animation is produced by writing different values to the lookup table.

For the display of 256 colors simultaneously from an on-chip palette of 64-K colors, the 7300 incorporates a 4-bit multiplying digital-to-analog converter with four analog outputs. An external buffer is necessary to provide isolation from the monitor's high-voltage environment and provide the TTL levels or 5-Ω drive for the monitor. Pixel rates to 30 MHz are supported, providing crisp, flicker-free displays.

The display formats and monitor timings on the 7300 are software defined, allowing the same hardware design to be used in a variety of applications. In addition, the 7300 provides a software clock option so that the graphics processor operates with a double-frequency clock for applications with a low video rate, increasing system performance.

The 7300's dual independent 16-bit-wide, 16-word-deep input and output FIFO registers provide an asynchronous interface to 8- and 16-bit processors. The 7300 occupies two locations within the host processor's address space. One location is used to read and write from the FIFO registers, the other is used to read the status register and to write to the command register. Handshake signals are provided for DMA transfers and a ready line can be used to insert wait states during I/O operations.

Though the NCR team managed to incorporate an impressive number of features on the color graphics controller, it faced a critical decision over the memory function. According to Loftus, system-cost and cost/performance considerations, rather than high density and high performance for their own sakes, dictated the development of a separate memory-interface controller. "Similar functions could have been achieved using TTL shift registers and associated glue logic, but the result would have been lower performance and higher cost," he says. "On the other hand, integrating the two circuits into one would have also increased performance, but only at the cost of going to a higher-density and higher-cost process."

The memory-interface controller is designed to serve as a master supervisory processor and as a memory multiplexer/demultiplexer, allowing the use of generic low-cost DRAMs. The 7300 controls operation of the 7301, which is transparent to the user.

To achieve high performance, a graphics system must be able to quickly transfer blocks of data within the frame buffer. Central to the performance of the NCR system is the ability to perform fast block transfers of data within the frame buffer, as well as block moves of data to and from the 7300's cache memory (Fig. 2). Pixel data can be shifted, masked, and overlaid or exclusive OR'd with existing pixels. Each 7301 supports two bit planes.

A 16-color system with a 1,024-by-512-frame buffer (Fig. 3) uses the 7300 color graphics controller, two 7301 memory-interface controllers, eight 64-K-by-4-bit RAMs, and two TTL buffers for the RAM address and control signals. A two-transistor buffer for each analog output is also needed.

This system can be configured to serve multiple application environments, says Loftus. The time, the number of lines displayed and the number of pixels per line are all software programmable. The only limitation is the maximum size of the frame buffer, which is 1,024 by 1,024 by 8 bits, and the maximum video rate of 30 MHz. Within these boundaries, this system could be used for a variety of display formats, including 640 by 200, 640 by 400, 640 by 480, 800 by 400, and 960 by 350 pixels, all noninterlaced with a 60-Hz refresh rate. With the maximum 1-megabyte frame buffer, it can also support a large interlaced display, such as 1,000 by 700 pixels.

Although NCR has implemented its graphics processor in two chips, it plans eventually to integrate most of the functions of the 7300 and 7301 in a single-chip graphics controller, which will further improve chip count in systems, says Loftus. The company will fabricate the chip using a sub-2-μm CMOS process. The single-chip version is expected to be available during 1987. □

A THREE-YEAR EFFORT BY THE NCR DESIGN TEAM

Development of the 7300/7301 graphics chip set at NCR can justifiably be called a group effort. It involved six engineers and designers who for the most part have been with the project from its inception three years ago.

The team was headed by 39-year-old Dave Henderson, an alumnus of Texas Instruments Inc. who has been at NCR for six years. Working with him were senior topology manager Dan Hackney, who was responsible for implementing the design of the company's computer-aided design tools; Brian Herbert, who as applications leader and technical coordinator worked with Henderson in analyzing the market and defining the product; Steve Johnson, who was responsible for the design of the color graphics chip; Mike Lahey, responsible for the 7301 design; and James Robbins, who worked with Johnson and Lahey on both chips.

According to Henderson, the toughest part of the project was the definition phase. He and Herbert had to analyze the marketplace, recommend to the company which direction to go in as a follow-on to its earlier CRT controller products, then define the basic architecture.

"It became clear after about six to nine months of study that certain trends were emerging: color graphics, multitasking, windowing, sophisticated text and character management, and the ability to merge the two in the same display," says Henderson. "The problem was in determining what mix of these features to implement."

Although the temptation was there to design a high-end chip, with all the bells and whistles, decision making was simplified when the company determined to go after the largest part of the market, based on units sold—the medium-performance segment typified by many personal computer designs.

"Unlike the high end of the graphics market, such as engineering and scientific work stations, where the name of the game is performance no matter what the cost, the rules are somewhat different in the medium-perfomance segment," says Henderson. "There the goal is cost-effective performance—that is, users want as much performance as they can get but only within specific price parameters."

With that perception, definition and eventual design of the chip set were relatively straightforward. The NCR design team focused on achieving reasonably good color graphics, but not at the cost of text display and management; multitasking and windowing, but not at the cost of overall performance or system cost; and integration of as many functions as possible on as few chips as possible, but not to the point of pushing the process technology beyond its density and reliability limits.

GRAPHICS TEAM. NCR's Robbins, Herbert, Henderson, Hackney, Lahey, and Johnson, from left.

PROBING THE NEWS

THE SCRAMBLE TO WIN IN GRAPHICS CHIPS

INTEL AND NCR ARE THE LATEST TO ENTER THIS HOT NEW MARKET

by J. Robert Lineback

DALLAS

The race for the lead in the graphics chip business is turning into a stampede. Two more contenders galloped into the fray this week: Intel Corp. with its much-anticipated 82786 graphics coprocessor and NCR Corp. with a two-chip set for color graphics control.

It's still anyone's race for the market that was opened by Hitachi Ltd. and NEC Corp. two years ago. But Texas Instruments Inc. got out of the gate first with the next wave of chips earlier this year when it started shipping samples of its speedy programmable 32-bit graphics microprocessor. Nearly a dozen other new designs are in the works at such chip houses as Advanced Micro Devices, Fujitsu, Honeywell, Inmos, National Semiconductor, Signetics, and Toshiba, plus pioneers Hitachi and NEC.

"The thing that triggered all of this was the dramatic drop in memory prices of a couple of years ago," says Intel's Mark Olson, product manager in the Graphics Component Operation in Santa Cruz, Calif. Inexpensive dynamic random-access memories made RAM-intensive, bit-mapped displays affordable for desktop personal computers. But handling high-resolution color graphics has proven daunting for the microprocessors in today's personal computers.

So chip designers decided to take the opportunity to move this tough graphics-control job out of the CPU and into a special-purpose microprocessor they would come up with for the systems designer. The idea is to send system designers back to the drawing board by giving them far greater power to manipulate video-display pixels independent of a computer's busy host processor. To do this, they are packing the new graphics chips with more intelligence, enhanced embedded drawing algorithms, support for emerging industry interface standards, and bit-mapped display features. Some designs have parallel-processing capabilities, allowing these devices to execute graphics while the host processor applies its muscle to the application.

GROWING MARKET. This embryonic market is attracting a crowd of chip makers because of its mind-boggling potential: sockets in every personal computer and many engineering work stations. Estimates from TI show that some 9 million home computers, desktop business models, and work stations worldwide could have used such graphics chips in 1985. And that number is expected to nearly double by 1988 (chart). In addition, graphics chip makers are hungrily eyeing such applications as laser printers, plotters, office copiers, facsimile transmitters, instrument equipment, machine-vision systems, and automotive dashboard displays.

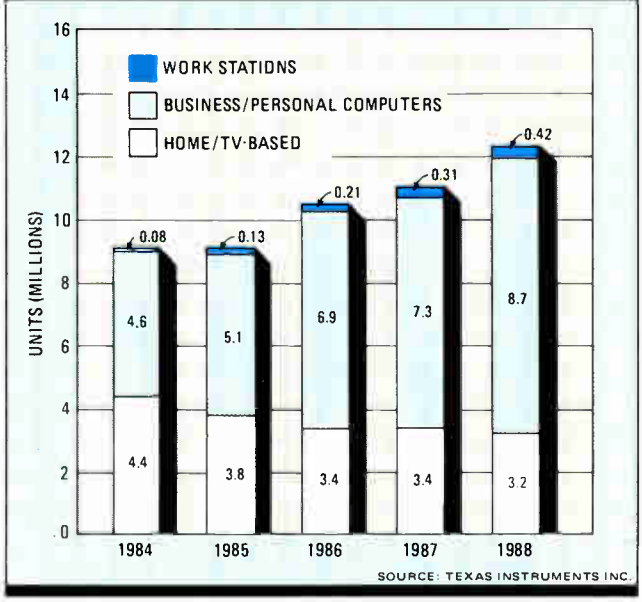
For their part, personal computer makers hope the new chips will enable them to offer fast color displays akin to those of the expensive engineering work stations. Even a few work-station makers are considering the new chips as lower-cost replacements for bipolar bit-slice processors in graphics-display engines. That would help them fight off the onrushing high-end personal computers, such as IBM Corp.'s AT model.

But personal computers will undoubtedly be the first battleground for the competing graphics chips. In fact, NCR sees the market for its new chip set as the lower-cost part of that segment (see story, p. 61). The other newcomer, Intel, is looking to the same market as TI: computer-aided-design and business machines as well as high-end personal computers (see story, p. 57).

The new ICs are getting a hearty welcome from graphics specialists. "I think these chips will revolutionize the DOS market [IBM PCs and compatibles]," says Kim DeWindt, program manager for the Direct Graphics Interface Specification hardware standard proposed by Graphics Software Systems Inc. The Beaverton, Ore., software house worked with both Intel and TI on their chip designs. In return, the two rivals are part of a group of companies endorsing DGIS for the IBM PC market.

Enthusiasm for the chips is also starting to surface at some third-party vendors of graphics boards. "These families of new graphics chips are definitely opening the door for the next-generation products," says Charles Mauro, engineering fellow at Video-7 Inc. The Milpitas, Calif., company is planning to use TI's 34010 graphics processor in a prototype add-on card for IBM PCs and compatibles. "Considering what today's nonintelligent graphics adapters give you in the AT, just imagine what will happen when graphics are offloaded [from the 80286 central processor]," Mauro says. "In many ways it will match or beat the capabilities of today's

WORLD BUSINESS MARKET MAKES BIGGEST TARGET



work stations. And that is for plug-in adapters costing under $1,000."

Some customers are discouraged by the popularity of the graphics processor ICs. Take, for example, the experience Vectrix Corp. had with the widely used 7220 chip from NEC. Vectrix was one of the first to design it in, introducing its product at Comdex several years ago. "The next year, we went back and there were 8 million other companies using the 7220," says Larry Addison, director of marketing at the Greensboro, N. C., graphics-subsystem house. As a result, Vectrix is planning to use semicustom and custom chip designs to widen the space between its boards and those from its competition.

Meanwhile, the field will likely become quite crowded before the dust settles. The list of entrants is a veritable directory of the semiconductor business.

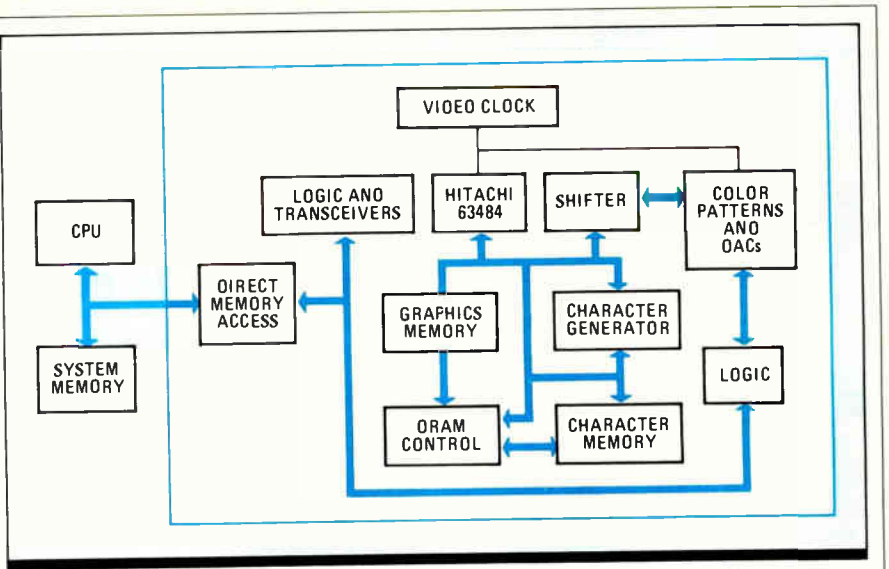
Later this year, for example, National Semiconductor Corp. will start offering samples of its DP8500 raster-graphics processor and the DP8510 bit-block-logic-transfer processor, or BitBLT. The two CMOS processors represent a divide-and-conquer strategy, says Charles Carinalli, director of advanced peripheral and software products in Santa Clara, Calif. The 44-pin BitBLT processor will be an inexpensive slave dedicated to each display plane and operating in parallel with the 68-pin master.

"We've got an SIMD architecture, meaning single-instruction processor and multiple-data manipulators," says Carinalli. "We originally started out doing one processor, but realized we would reach a performance limitation after two or three display planes."

THIRD QUARTER. Over in Sunnyvale, Calif., Advanced Micro Devices Inc. is preparing to introduce in the third quarter its Am95C60 quad-pixel data-flow manager, the design of which was influenced by work-station vendors who decided to use AMD's bit-slice products rather than earlier generations of graphics processors.

"We started looking at what the missing pieces were when our customers opted not to use the first graphics engines, like NEC's 7220," says Steve Dines, strategic marketing director of AMD's Logic Products Division. Embedded into the 95C60 are fast BitBLT algorithms along with basic drawing primitives. The chip can paint an average of 40,000 characters per second into a bit-mapped memory.

Others also have designs in the wings. In Japan, Hitachi—which helped start the stampede of graphics processors in 1984 with the introduction of the HD63484—says it is improving the speed of the device and adding support for the Computer Graphics Interface (CGI) standard as well as developing a next-generation chip. Toshiba Corp. and Fujitsu Ltd. both report they are working on high-end graphics introductions.



A PIONEER. The Hitachi HD63484 graphics processor, which appeared in 1984, was, along with a chip from NEC, the forerunner of the present generation of graphics processors.

In the U. S., Signetics Corp., which recently began second-sourcing Hitachi's 63484, plans to introduce a coprocessor aimed at boosting windowing capabilities. Dubbed BMAP, the chip translates alphanumerics into bit-mapped graphics. It will be unveiled at Wescon in November. Inmos Ltd., in Colorado Springs, is expected to debut a graphics processor, the G412, based on its transputer architecture. Motorola Inc., which dropped its 68940 raster-graphics processor in January, is developing a new strategy centered on its 32-bit 68020 microprocessor. And Fairchild Semiconductor Corp. is putting together its own plans.

With Intel and TI going head to head, the consensus among third-party board suppliers gives Intel's coprocessor an edge in IBM AT and AT-compatible markets because the 82786 is designed to work with Intel's 80286 host CPU.

30 FOR INTEL. "At this point, we've got over 30 solid design wins," claims Intel's Olson. Among software and hardware suppliers that announced this week they will use or support the 82786 are Ashton-Tate, Digital Research, Graphics Software Systems, Lotus Systems, Microsoft, Nova Graphics International, Number Nine Computer, and Reuters.

The 82786 coprocessor's introductory price is $81.25 each in 10,000-piece quantities. In 1,000-piece lots, the chip will cost just under $100. Samples are now available and volume deliveries will start in the fourth quarter.

Still, many observers believe the race between Intel and TI is far from over. Unlike Intel's device, TI's programmable processor—the 68-pin 34010—is a general-purpose 32-bit microprocessor containing a graphics-oriented reduced-instruction-set computer. "I think [the differences between the TI and Intel chips] could be traced back to the culture of the companies," says Kevin McDonough, graphics product manager at TI, Houston. "If you are a host-processor-oriented company—such as Intel—you are not about to create a new general programmable element into the system. The controller peripheral is going to be built around your own host."

Introduced in the first quarter [*Electronics*, Jan. 27, 1986, p. 15], the TI chip has a sample price of $500 apiece and will also enter volume production in the fourth quarter. It executes 6 million instructions per second, addresses a gigabit of storage, and completes raster-manipulating operations in a single cycle. The 34010 may be programmed in high-level languages such as C.

HANDY MIX. TI's chip holds user-programmed drawing algorithms, and McDonough believes the programmable approach will enable companies to mix proprietary graphics algorithms with emerging industry standards, such as CGI or the Graphics Kernel Standard, known as GKS. Intel's chip has hard-wired graphics primitives, which the company believes will prove faster than TI's programmable approach.

"It will be interesting to watch what happens," he adds. "I think you will see a lot of design engineers get excited about programming algorithms in the TI chip, but you'll see a lot of management being more interested in the Intel chip because there is more safety in having all of this hardwired. You don't have to worry about software bugs." □

Reporting provided by Michael Berger, Clifford Barney, Bernard Conrad Cole, and Debra Michals