The specifications of the controller include 17 512-byte sectors/track, eight head-select inputs, as well as two drive-select lines; and the write-precompensation time is 12 ns. The maximum allowable cable length is 20 ft for both control of a daisy-chain setup and for data applications. Power requirements are +5 V dc and +12 V dc, with a maximum current drain of 1.5 A on the +5-V supply and 100 mA on the +12-V supply.

The WD1002-WX2 is available in production quantities now. It sells for $245 in lots of 100, with volume discounts available.

Western Digital Corp. 2445 McCabe Way, Irvine, Calif. 92714. Phone (714) 863-0102 [Circle reader service number 338]

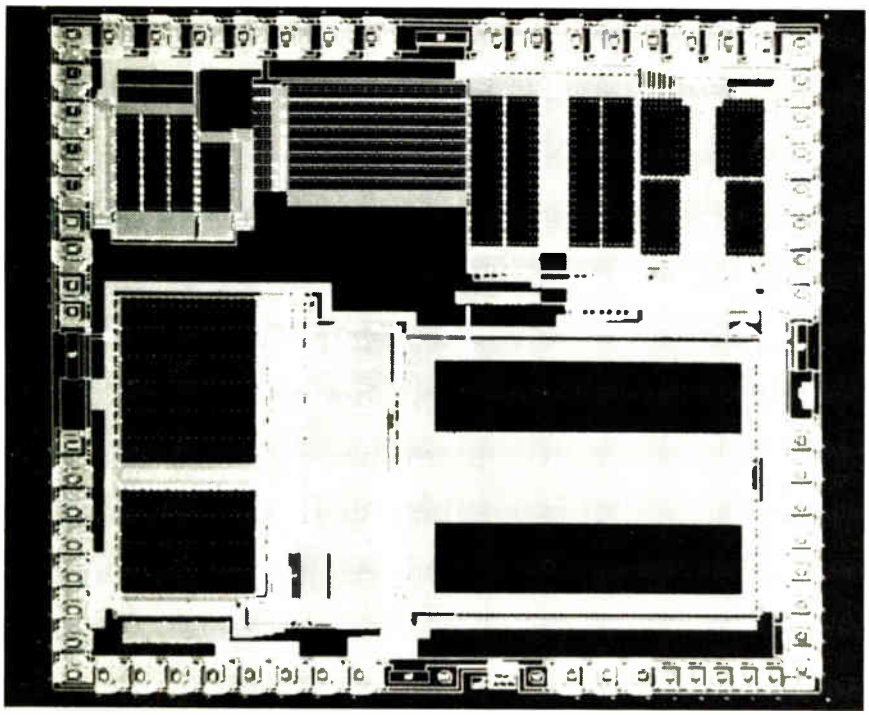
Color-graphics controller chip set reduces parts count, incorporates microcomputer

Microcomputer-based graphics systems may soon be easier to design and use and could offer significantly improved price-performance characteristics with far fewer components, thanks to a new color graphics controller chip set from NCR Corp.

Indeed, officials at the firm's Microelectronics division in Colorado Springs, Colo. are billing the NCR 7300 color-graphics controller chip (pictured) and associated 7301 memory-interface controller as the first of a new generation of graphics-controller chips with improved capabilities. For many applications, the 7300 will offer performance four to five times that of the widely used 7220 from Japan's NEC Corp., contends Michael R. Shapiro, NCR's marketing manager for logic products.

With initial samples set for availability in late summer, the 7300 will be fabricated in n-channel MOS using NCR's 3-μm, VLSI-2 process that can integrate over 100,000 transistors on chip. The 7301 will integrate about 15,000 transistors and will be built with the same process.

The NCR chip set will work in any 8- or 16-bit microprocessor-based system. Unlike the 7220, the 7300 incorporates a complete 10-bit microcomputer on chip. When used in conjunction with one to four 7301 chips that provide an interface to a frame buffer up to 1 megabyte in size, the 7300 can unburden the host processor by taking over a variety of graphics-processing tasks. These include computation of picture-element addresses for the frame buffer, control of frame-buffer refreshing and timing, and handling direct-memory-access control.



Firmware. One feature that will make the 7300 easier to use is its on-chip firmware for interpreting high-level graphics commands from the host processor. The command set is based on that proposed for the Virtual Device Interface standard currently under development by the American National Standards Institute.

Other special-feature commands in the set include an extensive windowing capability. This feature will greatly simplify the programmer's task by allowing him or her to write in terms of high-level graphics primitives, explains 7300 designer David L. Henderson. "It should really cut down the amount of time required to write new device drivers or write applications programs," he adds.

The basic data type for the 7300 is the picture element. Each pixel can contain from 1 to 8 bits of information, with each 7301 in a system contributing 2 bits of data. Thus, for a full 8-bit pixel depth, which results in the maximum-displayable 256 colors, four 7301 devices must be used. A system equipped with a single 7301 could display only four colors simultaneously.

Pixel bus. Each 7301 in a system handles 16 dynamic random-access-memory data lines from the frame buffer and provides a 4-to-1 multiplexing and demultiplexing function in transferring data back and forth between the frame buffer and the 7300. Each 7301 is connected to the 7300 by a 4-bit pixel bus. During screen refreshing, data is transferred from the frame buffer through the 7301 and into the 7300, which performs an additional 2-to-1 multiplexing function before sending the data on to the display monitor at clock rates up to 30 MHz.

Whereas chips like the 7220 re-

quire off-board circuitry to convert digital data from the frame buffer to analog form to drive a display monitor, the 7300 integrates the digital-to-analog conversion function on the chip, Henderson points out. Separate red, green, and blue analog output ports on the 7300 controller chip can thus drive a display monitor directly with only a minimum amount of buffering to provide high-voltage isolation.

This feature alone will provide a system-level saving of at least $100, compared to using a hybrid circuit to provide the d-a conversion, Henderson estimates. Additional savings in space and cost come with the 7301 chips, each of which can replace between 12 and 20 TTL parts commonly used to do multiplexing and demultiplexing in current graphics systems, he says.

In 1,000-piece quantities, the 7300 controller chip will be priced initially at about $80 each. The 7301 memory-interface controller will go for about $15 each in similar quantities. NCR plans to begin production on the chips during the fourth quarter.

NCR Microelectronics Division, 1635 Aeroplaza Dr., Colorado Springs, Colo. 80916. Phone (800) 525-2252 or (303) 596-5612

[Circle 342]

Dense 256-K pseudo-static RAM uses C-MOS peripheral circuitry for low power

Many of the advantages of a 256-K static complementary-MOS random-access memory, but at a price comparable to that soon to be charged for dynamic RAMs, are incorporated in Hitachi's HM65256P pseudo-static RAM. The memory cells feature a dynamic single-transistor design fabricated in the same 2-μm process used in the firm's dynamic RAMs to attain a much higher packing density than is possible in static RAM cells, which need four transistors and two resistors. The memory's peripheral circuitry uses 2-μm C-MOS processing for low standby current.

The chip's 32-K-by-8-bit configuration makes it a natural for small systems such as personal computers, terminals, and printer buffer memories. It is equally suitable for graphics-processing equipment where a large memory capacity is required, and its by-8-bit configuration provides higher bandwidth than a by-1-bit or by-4-bit memory chip. The firm is now developing a 32-K-by-9-bit chip for customers who need a parity bit with each byte.

Versions are available with 150- and 200-ns access times. Internal operation is initiated when an address change is detected by the address-transition detector. Because precharging is eliminated, the part features identical cycle and access times.

In many systems, the chip's combination of low operating-power consumption and extremely low standby-power consumption permit higher packing density, eliminate the need for cooling, and cut power-supply size and cost. Moreover, the incorporation of automatic- and self-refresh modes in this RAM favors its use in simple systems, without the bother of complex refresh control, and in some battery-backup applications.

The new chip can be used in its automatic-refresh mode in many systems that now use static RAMs because of difficulty in coordinating column- and row-address-strobe timing with read and write cycles. The self-refresh mode makes backup by battery or supercapacitor possible over a period of one to several days. True low-current static-memory chips are superior for intermittently used portable equipment with battery backup, though.

Refresh. Automatic refresh is nearly as simple as its name implies. A logic high signal is applied to the chip-select pin, and then the output-enable/chip-refresh pin is driven high at least 256 times during each 4-ms interval. Circuits within the chip detect the positive-going transition and a refresh-address counter generates the proper refresh signals in sequence.

If the refresh pin is held high for more than about 4 μs, the chip goes into its self-refresh mode. In this mode, one refresh pulse is generated approximately every 15 μs. Typical power drain is 10 mW. Power drain is higher than for static C-MOS, which flows in short, high-current pulses.

The cells' dynamic nature necessitates a 5-V power-supply voltage. True static memories can often retain information with supply voltages as low as 2 V. The RAM is housed in a 600-mil 28-pin dual in-line package with a Joint Electron Devices Engi-