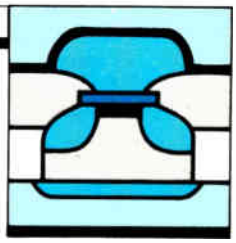
# NATIONAL'S ALTERNATIVE TO 'ALL-IN-ONE' GRAPHICS ICs



The new raster processor is the centerpiece of a family of graphics building blocks designed to remove the limited architectural options of the single-chip approach

Designers of graphics systems who feel constrained by the limited architectural options available with the current generation of "all-in-one" graphics chips will welcome a new raster graphics processor from National Semiconductor Corp., Santa Clara, Calif.

Designated the DP8500, it is the centerpiece and final element in a family of graphics building blocks that partition onto separate chips functions such as frame-buffer processing, bit-plane-data manipulation, video-data conversion, clock generation, and memory control. What makes this possible is the architecture of the DP8500 raster processor, which separates arithmetic logic units for addressing and data processing, functions normally combined into a single ALU in conventional designs.

As a result, system designers can build graphics systems which perform both pixel and bit-plane operations equally well, says Roger Reak, director of graphics processing at National. Pixel-oriented systems are used in high-resolution, three-dimensional, and color-graphics applications; bit-plane-based systems are important in such functions as byte-oriented and text-processing applications. With all-in-one chip solutions, graphics processors are usually optimized for one or the other.

At 20 MHz, the 2-$\mu$m CMOS 8500 is the fastest component of its type on the market, Reak says, featuring a 100-ns bus cycle time on back-to-back vector and block operations. With a line-drawing speed of 300 ns/pixel, four times faster than its closest competitor, typical system performance ranges from 10 million to 160 million pixels per second.

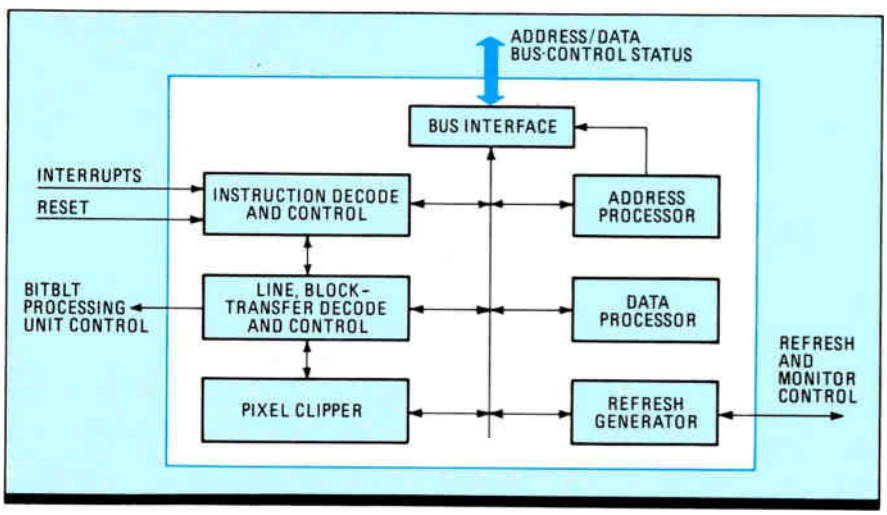
Being sampled now, with production quantities expected by the third quarter, it joins a family of devices which includes the already-introduced 20-MHz DP8510 bit-block transfer processor and the 225-MHz DP8512 video clock generator. The group is rounded out by the DP8515 family of video shift registers and a variety of standard dynamic random-access memory and video dynamic RAM controllers. Production pricing on the 8500 will be $95 in quantities of 10,000 or more.

What makes the partition building-block approach possible is the chip-level architecture of the DP8500, Reak says. One 100,000-mil$^2$ chip (see fig. 1) contains a general-purpose microcoded processor divided into two units, as well as a programmable video refresh generator, vector generator, bit-block transfer controller, and rectangle clipper.

The 8500's processor is divided into two blocks. Driven by a common microcoded instruction set, two arithmetic logic units—one each for addressing and data—operate concurrently.

The address processor consists of a 28-bit ALU with an instruction set and bank of sixteen 28-bit address registers. The data processor, on the other hand, is a 16-bit ALU with a relatively rich instruction set optimized for graphics applications and a bank of sixteen 16-bit registers. Other registers have dedicated functions in support of graphics or video refresh operations. In addition, certain graphics operations, notably bit-block transfers, line drawing, and clipping are implemented on chip with dedicated circuitry.

A single stream of instructions, fetched from external memory, serves both processors via mi-




**1. DUAL PROCESSORS.** The DP8500 graphics chip employs two processors, one for addressing and one for data, driven by a common microcoded instruction set and operate concurrently.

crocode control. The instructions include the register-to-register functions of both processors, and the load/store instructions for data transfers between the chip's registers and its memory. Additional instructions make use of both processors as well as other on-chip resources.

As a result of its dual ALU architecture, the 8500 can be adapted to a wide variety of system architectures without sacrificing performance, says Reak. In a work-station application, he says, it might execute a communications protocol with another processor upstream in the graphics pipeline, awaiting arrival of a display list to be executed. Upon receipt, the 8500 can either directly execute or interpret the display list, rasterizing graphics primitives into the display buffer. Upon executing the final display-list instruction, the processor signals completion, ending the exchange of protocols with the upstream processor and allowing the process to continue.

Alternatively, says Reak, in a stand-alone application such as a computer terminal, the 8500 enters a control program, servicing peripherals and executing a command interpreter. In this application, it would be responsible for the keyboard, mouse, and UART service, at the same time executing a graphics language interpreter, responding to host commands by maintaining the graphics environment, and drawing into the display buffer.

Unlike competitive integrated graphics processors, the 8500 is not limited to one type of graphics frame-buffer architecture. "It can be used not only in either of the two major approaches, pixel and plane, but also in a system that mixes the two," Reak says.

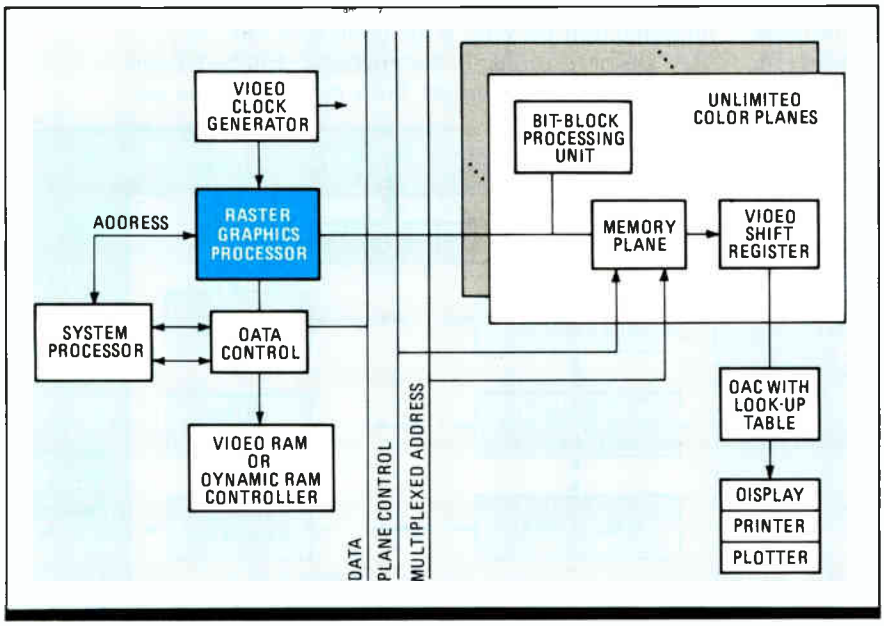
In a pixel-based architecture, frame-buffer data is handled one pixel at a time. For multiple planes, typical in color applications with one plane per color, the address to the frame buffer generates a data word composed of pixels at the same location across multiple planes. These applications often require 16 to 32 memory planes.

In a plane architecture, the frame buffer is manipulated a word at a time within each plane; each word is usually 16 bits long. To change 1 bit, the other 15 must be carried along. Also, a barrel shifter circuit is required if image placement and movement accuracy is needed down to the actual pixel level. Engineering and business applications often use plane architecture, because they require much data manipulation and image movement.

Many other graphics processors cannot work in pixel and plane architectures on the same chip. "In most cases, this has restricted the performance and applicability of these devices across the spectrum of graphics applications," Reak says. Because they are designed to support only up to 8 planes of memory, conventional graphics adapters require additional processors to accomplish transition to more planes, increasing system cost and degrading performance.

Most other graphics processing architectures have the main controller intimately involved with both frame buffer addressing and data manipulation. "This approach severely affects performance, especially as the number of planes increases," Reak says. National's solution is to separate the graphics processing function into two different chips with the 8500 processor performing all of the address and timing functions associated with the graphics frame buffer while maintaining the classical address and data interface with the system's host central processing unit. The actual data manipulation associated with each memory plane is assigned to a separate slave processor, the DP8510, responsible for masking, barrel shift operations, and bit-block boundary operations.

In a typical multiplane color graphics system (fig. 2), a control bus separate from the graphics processor passes all control and setup information to the slave manipulators in parallel with the control information via the data bus. Once this initial information is set up, and the graphics function is being implemented, the graphics processor is no longer involved in graphics manipulation. The slave processors can be configured via the control and data bus for exact destination, left and right asking, bit-block operations, and the barrel shift. When plane-to-plane transfers are required, one slave processor acts as the source and any combination of slave processors the destination. □




**2. PLANE AND FANCY.** National uses the DP8500 raster processor and the DP8510 slave processor, responsible for masking, barrel shift operations, and bit-block boundary operations.

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