MGA (Matrox Graphics Architecture)

MGA ATLAS Specification

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Trademarks

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Appendix A: Technical Data

Chapter 1: MGA Product Overview

This chapter contains an overview of the Matrox MGA chipset features and software products.

1.1 Introduction

Matrox MGA is a high-speed, high-resolution graphics accelerator series of products designed for the power user. MGA is very suitable for GUI environments such as Microsoft Windows 3.1 and Windows NT, IBM OS/2 PM, and AutoCAD. It offers ultra high resolution displays with true color and many other innovative hardware and software enhancements.

MGA's 64-bit graphics power, in combination with a 486 or Pentium-class PC is in our opinion the best graphics solution if you require true workstation-level performance at a reasonable price.

1.1.1 MGA Chipset

The Matrox ATLAS chip lies at the heart of MGA's powerful graphics capabilities. It offers an ISA interface for ISA bus products, and a PCI interface for PCI systems. Several possible memory configurations permit design of 8, 16, 24, and 32 bits/pixel displays at resolutions up to 1600 x 1200 pixels. Figure 1.1 shows a block diagram of a typical graphics display adapter which uses the MGA ATLAS chip.

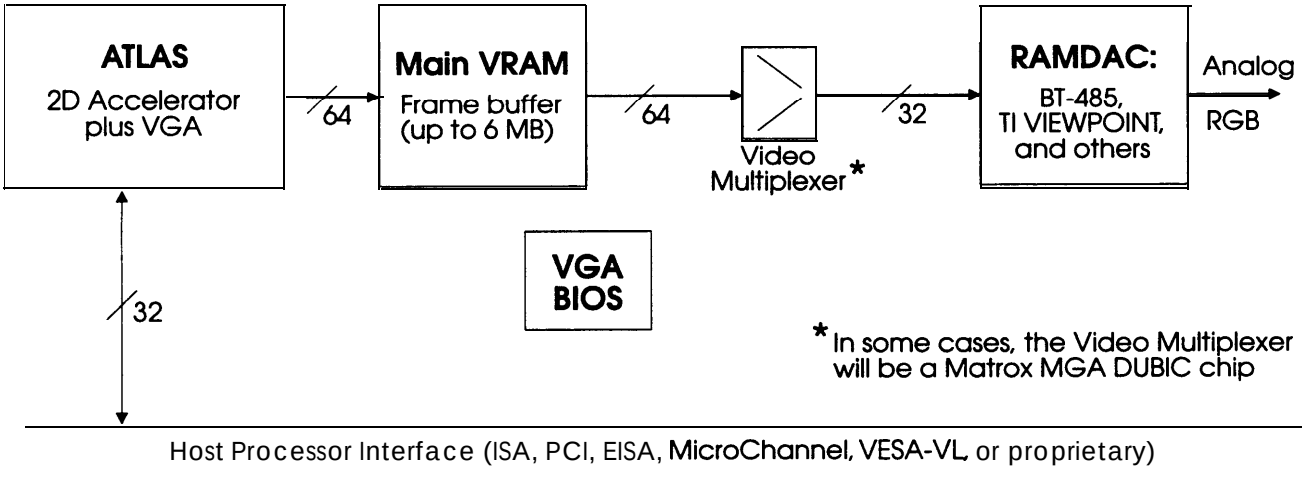


Figure l-l: Typical Implementation Block Diagram

The chipset functions as a stand-alone graphics controller that features an integrated VGA to offer both VGA Mode and high-resolution Power Graphic mode operation. It contains a 32-location Command FIFO and address and data processing units (APU, DPU). In addition, LINE, Trapezoid, and BITBLT drawing operations are available, supported by DMA and Pseudo DMA transfers. These enhancements make screen operations such as redrawing and scrolling appear instantaneous.

1.1.2 Features

- From 1 to 6 MB of frame buffer VRAM in configurations up to 32 bits/pixel
- VRAM block write operations for maximum speed
- Photo-realistic true color display, and QCDP (Quality Color Dithering Process) for displays of less than 24 bits/pixel
- Ultra-high resolution of 1600 x 1200, with 256 colors
- Workstation performance with speeds from 2 to 12 times faster than competitors' boards
- 64-bit frame buffer data bus width
- Integrated VGA, for full support of all DOS applications, eliminating the need for a separate VGA card
- Integrated PCI interface
- Direct RAMDAC interface
- Fast, flicker-free refresh rates up to 120 Hz
- Support for ISA, VESA VL, Micro Channel, EISA, PCI, and other architectures
- Installation of up to four boards in a system

1.1.3 Driver Support

MGA Power Drivers are available for Windows 3.1 and AutoCAD Rel. 11/12. The 'MGA Supplementary Drivers' package contains drivers for Windows NT, OS/2, and MicroStation (with dual display).
We provide:

- Support for popular Windows and DOS design and presentation applications
- DynaView driver for AutoCAD Release 11 and 12 that includes real-time scroll bars, spy glass, and bird's eye view, etc.
- Support for AutoCAD 12 for Windows, and MicroStation PC

1.1.4 Windows Support

- Control Panel for Windows controls the PixelTouch hardware pan and zoom, Virtual Desktop, and 'on the fly' resolution switching (without rebooting Windows) through the use of hotkeys
- Font anti-aliasing in hardware
- In addition to the drivers listed above, the 'MGA Supplementary Drivers' package also contains the ConsistentColor monitor calibration utility to ensure accuracy between your screen display and the printed output, and the WinSqueeze! on-the-fly JPEG file compression utility, which can achieve compression ratios of up to 28: 1

1.1.5 Video Support

- MGA interfaces with the Matrox Marvel video capture/video windowing board
- The MGA **VideoPro** NTSC/PAL encoder provides output capability for recording presentations, animations, and **AutoCAD** walk-throughs to tape
- Hardware-assisted Video for Windows **(VfW)** and Indeo are supported

1.1.6 Documentation

Other documentation available for Matrox MGA products includes:

- *MGA TITAN Specification* (10318-MS)* A description of the Matrox MGA TITAN chip.
- *MGA DUBIC Specification* **(10232-MS)*** A description of the Matrox MGA DUBIC chip.
- *MGA SDK Manual* (10330-MF) A user/reference manual for the MGA software developer's kit for DOS and Windows 3.1.
- *MGA **DynaView /2D** for **AutoCAD** Manual* (10345-MN) A user/reference manual for the Matrox MGA **DynaView** driver for **AutoCAD** and 3D Studio.
- MGA ***Supplemantary** Drivers Manual* **(10352-MN)** An installation/user manual which describes our **OS/2**, Windows NT, and **MicroStation** PC drivers, as well as the MGA **WinSqueeze!** and **ConsistentColor** programs for the Windows platform.

* Like the *ATLAS Specification*, these are restricted documents. See your Matrox Sales representative for more details.

The ***PCI** Bus Specification* from the PCI Special Interest Group contains additional information on hardware implementation for the PCI architecture.

Chapter 2: ATLAS Overview

This chapter introduces the Matrox MGA ATLAS chip and its component sections.

2.1 Introduction

The Matrox ATLAS chip supports both VGA and Power Graphic mode displays. VGA mode supports the VGA standard, while Power Graphic mode provides additional high-speed, ultra-high resolution displays. You can switch between the two modes while using the same monitor for both. ATLAS can be configured for PCI bus systems, or for ISA (and other) bus systems.

The ATLAS chip is a stand-alone graphics controller which is composed of several sections that work together to accomplish the many tasks required of them. The ATLAS sections are listed below, and discussed in the following sections of this chapter.

- Bus Interface
- VGA
- Bus Interface FIFO (BFIFO)
- Address Processing Unit (APU)
- Data Processing Unit (DPU)

2.1.1 Bus Interface

This section of ATLAS implements the interface with the host. Two bus interfaces are supported: an ISA interface and a PCI interface for the PCI bus.

The Bus Interface section includes:

- All of the control circuitry for the ISA and PCI buses
- PCI control, decoding, and re-mapping circuitry
- Configuration registers
- I/O buffers (8-location FIFO for writable devices; 4-location FIFO for ILOAD operations)
- Byte-alignment circuitry; 32-to-8 bit access conversion for VGA and I/O
- The control circuitry for external devices

2.1.2 VGA

This section implements the VGA functions, and includes:

- The VGA core, which interfaces directly with the frame buffer in VGA mode.
- The circuitry for video refresh in Power Graphic mode (see Section 6.3.5), which includes address generation, data transfer requests, and video control circuitry.

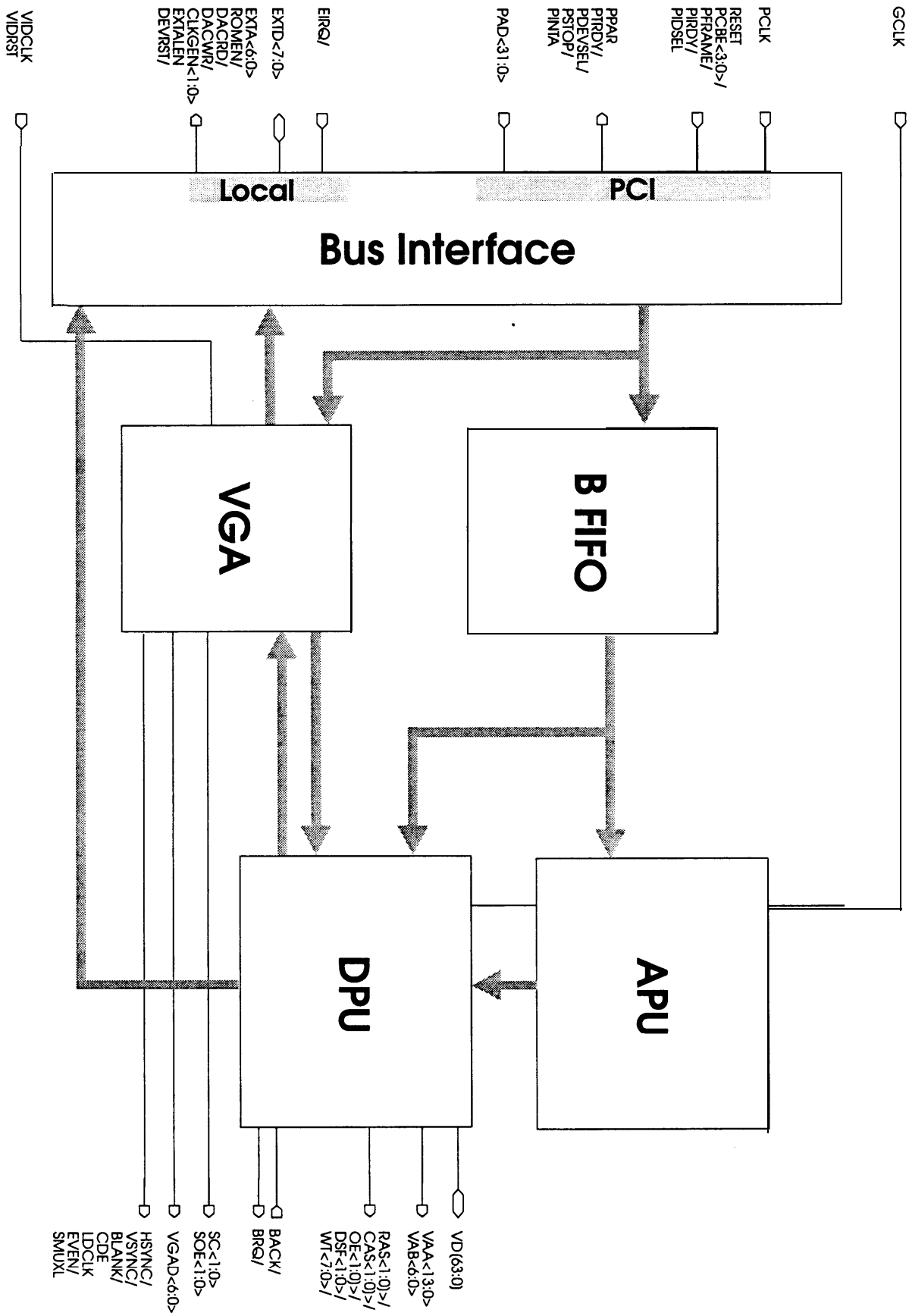


Figure 2-1: ATLAS Block Diagram

2.1.3 Bus Interface FIFO (BFIFO)

This section implements the Command FIFO from the host to the drawing engine. All access to the drawing registers passes through this 32-location FIFO, which holds the data as well as the address of the targeted register in the drawing engine.

2.1.4 Address Processing Unit (APU)

This section of ATLAS generates the sequencing of the drawing operations. Each drawing operation is broken down into a sequence of read and write commands which are sent to the DPU. The APU includes:

- Generation of the sequence for each drawing operation, and the addresses and mask
- Processing of the slope for vectors and trapezoid edges
- Rectangle clipping

2.1.5 Data Processing Unit (DPU)

This section manipulates the data according to the currently-selected operation. It also converts read and write commands from the APU into memory cycles to the frame buffer. The DPU includes:

- Generation of memory cycles
- Host compress, decompress, and data formatting
- The funnel shifter for data alignment
- The Boolean ALU
- Anti-aliasing
- The patterning and dithering circuitry
- The Data FIFO for BitBLIT operations
- The color expansion circuitry for character drawing

2.2 Frame Buffer

ATLAS can interface directly with the VRAM and DRAM. Memory combinations of 128K x 8 VRAM, 256K x 8 VRAM, 256K x 16 VRAM, and 256K x 16 DRAM are supported in order to permit design of different configurations. This allows ATLAS to support 8, 16, 24 and 32 bits/pixel formats and resolutions up to 1600 x 1200.

VRAM is used for the frame buffer itself. Since VRAM has two ports, the serial port of the VRAM is used for the screen refresh while the random port is devoted to drawing operations. Useful VRAM functions such as split data transfer, block mode, and write/bit are all exploited.

Chapter 3: Operation Modes

This chapter explains the VGA and Power Graphic operation modes of the Matrox MGA ATLAS chip. The Power Graphic mode description contains explanations of the memory configuration, frame buffer formats, drawing operations, DMA, and initialization, configuration, and reset.

3.1 VGA Mode

ATLAS's VGA contains all of the functions and support logic required to implement the IBM VGA, EGA, and CGA display adapter and MDA/ Hercules graphics card standards at a register-compatible level.

Since ATLAS is register-compatible with VGA, EGA, CGA and MDA/Hercules adapters, all display modes for these adapters can be supported. As with most display adapters, a BIOS is required to configure ATLAS for each display mode.

As well as the standard control registers required by the various display adapters, ATLAS uses auxiliary registers to enable enhanced modes and emulation functions.

3.1.1 FlexFont

In all alphanumeric modes, FlexFont is an available option. When enabled, it forces the character backgrounds to a single color and allows bits D4-D6 of the attribute byte to be used for character font selection. Up to eight character fonts can be displayed simultaneously. The character fonts are programmable and are stored in Dynamic Memory Plane 2.

3.1.2 Enhanced Modes

ATLAS enhances some display modes, and provides new high-resolution 256 and 16-color VGA modes.

The ATLAS chip permits high resolution VGA display modes of 640 x 400, 640 x 480, 800 x 600, or 1024x768 pixels with 256 simultaneous colors, both interlaced and non-interlaced. ATLAS also permits 16 color resolutions of up to 1024x768 interlaced and non-interlaced. Bits in the ATLAS auxiliary registers are used to enable these modes. Otherwise, the programming for these modes is similar to that for VGA modes 13h and 12h.

VGA mode 13h can be enhanced to provide up to 16 pages at 320x200 resolution with 256 colors (standard VGA supports only one page). The CPU can access two pages simultaneously, and the others are selected for access using page select bits in ATLAS's auxiliary ports. The CRTC start address register is used to select a page to display, or to scroll through all pages.

3.1.3 Display Adapter Support

Four modes of ATLAS VGA operation and emulation are available: VGA, EGA, CGA, and MDA/Hercules.

The VGA and EGA CRTCs are fully implemented and are used to perform the operations of a 6845 CRTC for the CGA and MDA/Hercules modes.

The control registers of the CGA and MDA/Hercules adapters are fully supported in the ATLAS hardware. When a control register bit is changed, a trap interrupt (NMI) is generated. The interrupt handler then interprets the control register's contents and sets up the VGA CRTC to perform the required operation. In addition, the chip can be configured to allow software emulation to override any or all of the hardware functions to permit support of special display modes.

3.1.4 Differences Between ATLAS Ports and IBM VGA Display Adapter Ports

There are differences between ATLAS's VGA mode and the IBM display adapters that it emulates. Some ports are changed from write-only to read/write to simplify emulation. Other ports have been deleted because they aren't required. The following subsections describe the differences.

3.1.4.1 Hercules Mode Port Differences

The 6845 CRTC is replaced by the EGA or VGA CRTC. Hardware emulation of the 6845 requires software assistance and is enabled through the trap and emulation control registers.

The mode control and configuration registers are now read/write.

3.1.4.2 CGA Mode Port Differences

The 6845 CRTC is replaced by the EGA or VGA CRTC. Hardware emulation of the 6845 requires software assistance and is enabled through the trap and emulation control registers.

The mode control and color select ports are now read/write.

3.1.4.3 EGA Mode Port Differences

The CRTC registers are now read/write. Otherwise, the CRTC is identical to the IBM EGA CRTC when the EGA CRTC mode is selected. The VGA CRTC can be selected when ATLAS is in EGA mode.

The attributes controller registers are now read/write. The address and data registers of the sequencer and graphics controller are also read/write.

Graphics position registers A and B have been deleted and replaced by read-only ports for the feature control and miscellaneous registers. Graphics position A is fixed at 0 and B is fixed at 1, according to standard EGA programing practice.

3.1.4.4 VGA Mode Port Differences

In VGA mode, ATLAS is register compatible with the IBM VGA. The light pen set and clear ports remain accessible. The EGA CRTC can be selected when ATLAS is in VGA mode.

3.2 Power Graphic Mode

Power Graphic mode employs hardware-coded graphical acceleration to improve the speed of GUI (Graphical User Interface) environments.

3.2.1 Memory Configurations

Several hardware memory configurations are supported in Power Graphic mode. These configurations can further be organized by the fbm (frame buffer mode) field of the OPMODE register. The three basic configurations are:

1. Support of up to 2 MB of VRAM and 2 MB of DRAM using 128K x 8 VRAM. This configuration supports 8, 16, and 32 bit/pixel displays.
2. Support of up to 3 MB of VRAM and 2 MB of DRAM using 128K x 8 and 256K x 8 VRAM. This configuration supports 8, 16, and 32 bit/pixel displays.
3. Support of up to 6 MB of VRAM and 4 MB of DRAM. This configuration supports 24 or 32 bit/pixel displays. Use fbm = 1 XX, depending on the amount of available memory and whether the frame buffer is configured as 24 or 32 bits.

- :* Note: In No DUBIC mode, only Banks 0, 1, 2, and 3 are supported. Therefore, only fbm= 0, 1, 2, and 3 may be used.

In all cases, the resolution depends on the amount of available memory. Section 6.3, 'VRAM Interface' contains tables that show which fbms can be used with which hardware configurations. The following figures show the memory mapping of the hardware memory configurations.

Memory Configuration Tables:

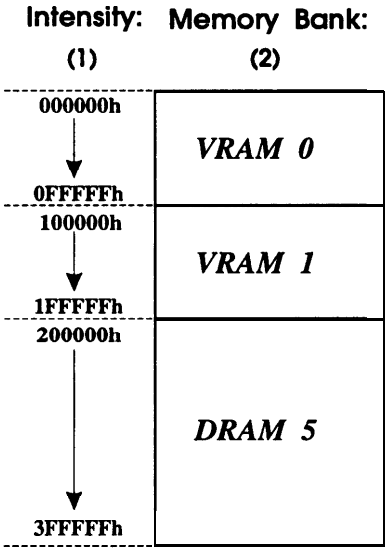


Figure 3-1: fbm = 0

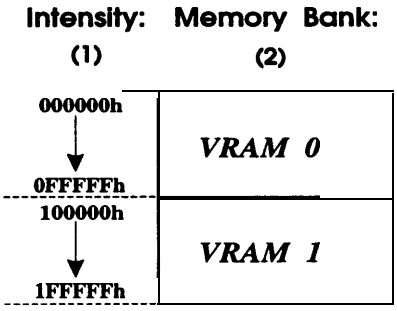


Figure 3-2: fbm = 1

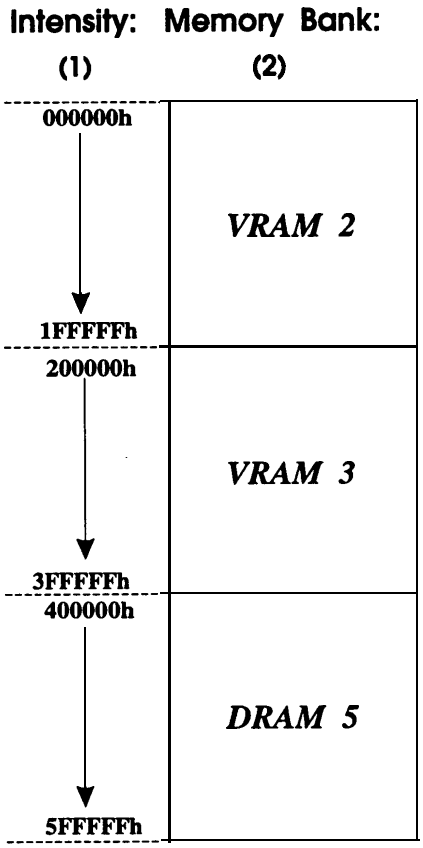


Figure 3-3: fbm = 2

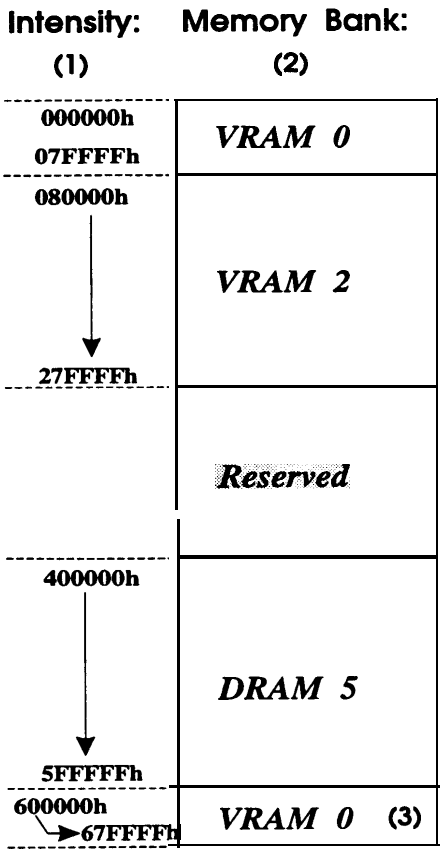


Figure 3-4: fbm = 3

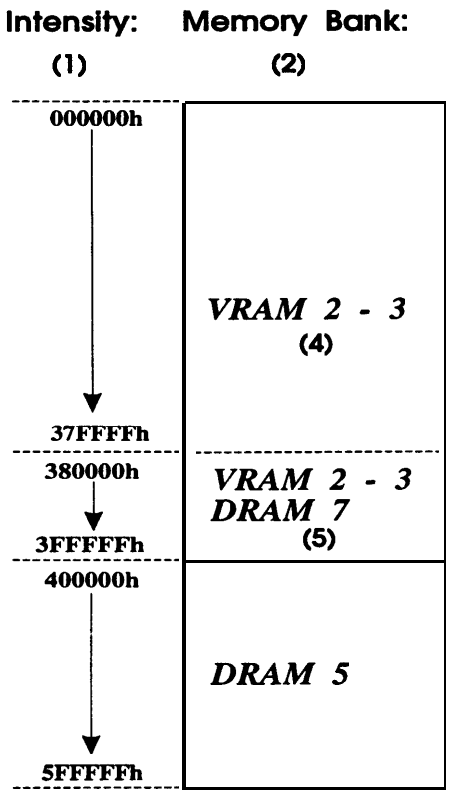


Figure 3-5: fbm = 4

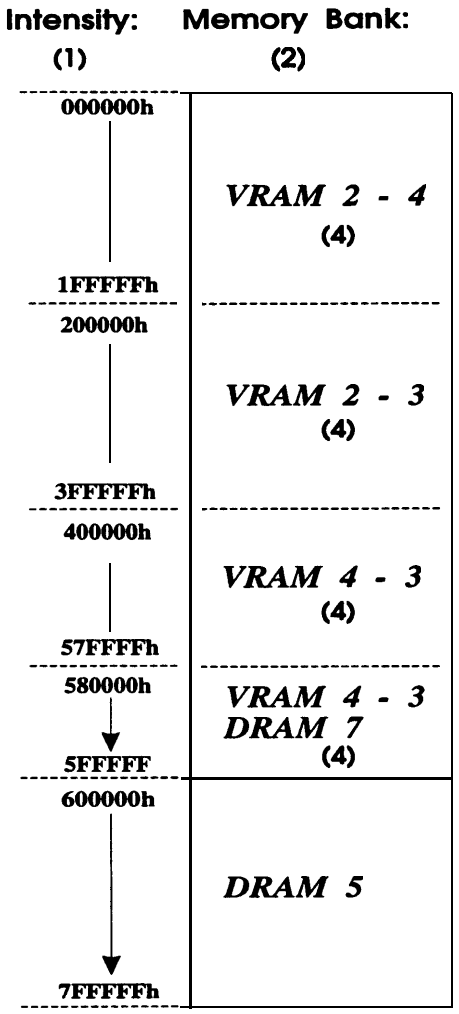


Figure 3-6: fbm = 5

Notes (Figures 3-1 to 3-8):

(1) All addresses are hexadecimal byte addresses. These addresses correspond to pixel addresses in 8 bits/pixel mode.

(2) 'Memory Bank' indicates the type of memory used, as well as which bank of memory is used in this space. Refer to Section 6.3 for details on the frame buffer modes.

(3) This part of the frame buffer can't be used for display.

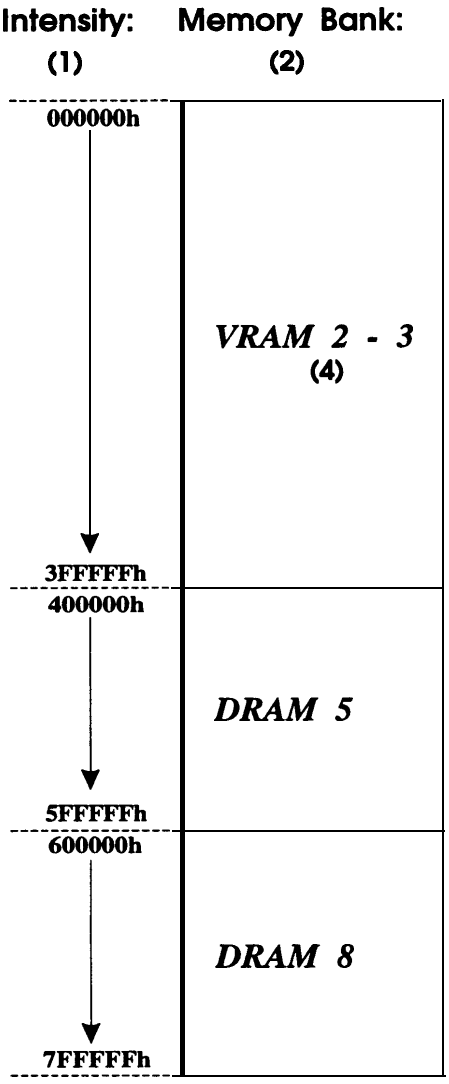


Figure 3-7: fbm = 6

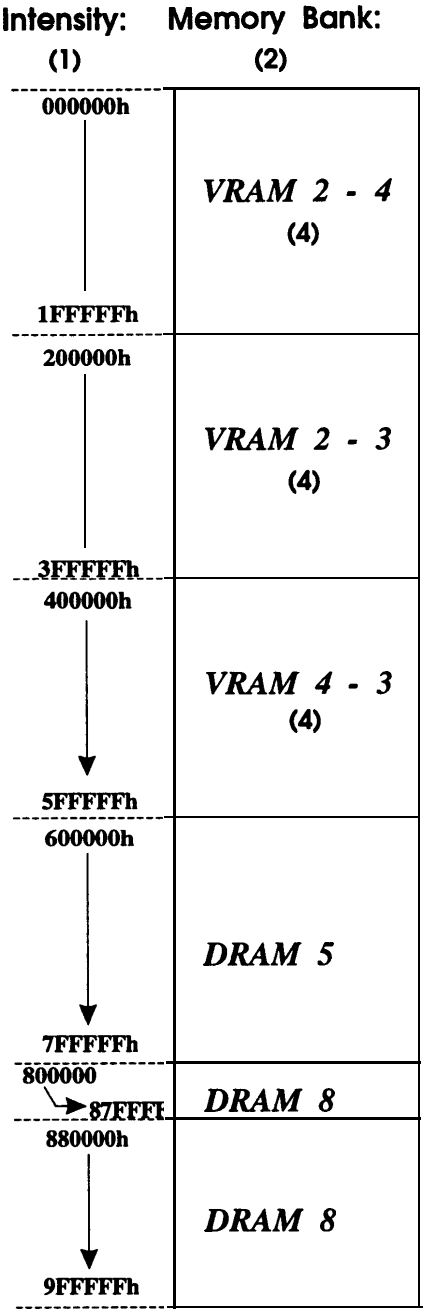


Figure 3-8: fbm = 7

Notes (continued):

(4) Depending on the number of chips/banks populated in this section, any data, or possibly only 24-bit data may be stored in this section of memory.

(5) Depending on the number of chips/banks populated in this section, and if bank 7 is populated, any data, or possibly only 24-bit data may be stored in this section of memory.

3.2.2 Pixel Format

The pixel slice is 64 bits long and is organized as shown below. In all cases, the least significant bit is 0. The Alpha part of the color refers to a section of the pixel which is not used to drive the RAMDAC. In the following illustrations, 'A' refers to Buffer A and 'B' to Buffer B when a double buffer mode is selected. ANTI refers to anti-aliased pixels, and MONO is a monochrome pixel slice.

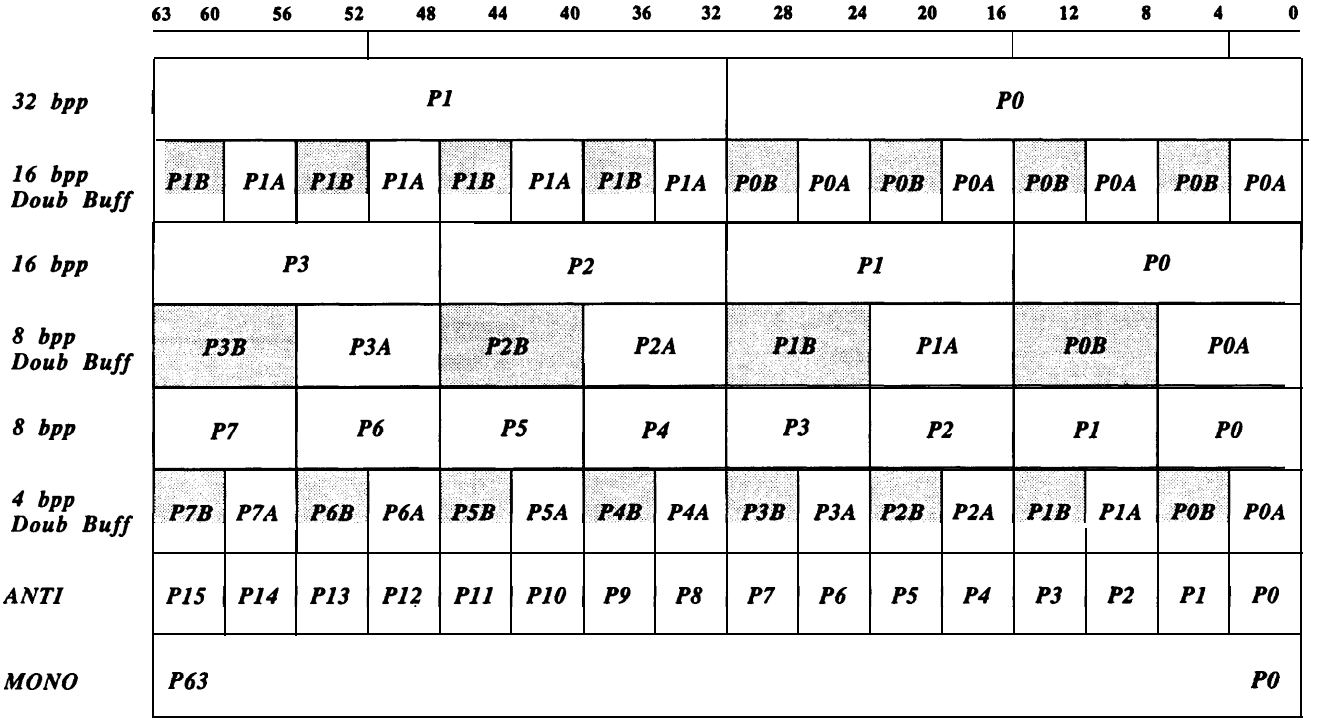


Figure 3-9: Pixel Slice

In all cases the data is true color; however in 8 bits/pixel and 4 bits/pixel formats, pseudo color can be used when shading and anti-aliasing are not used.

The following figure shows how the data is organized for each pixel (for all supported pixel depths).

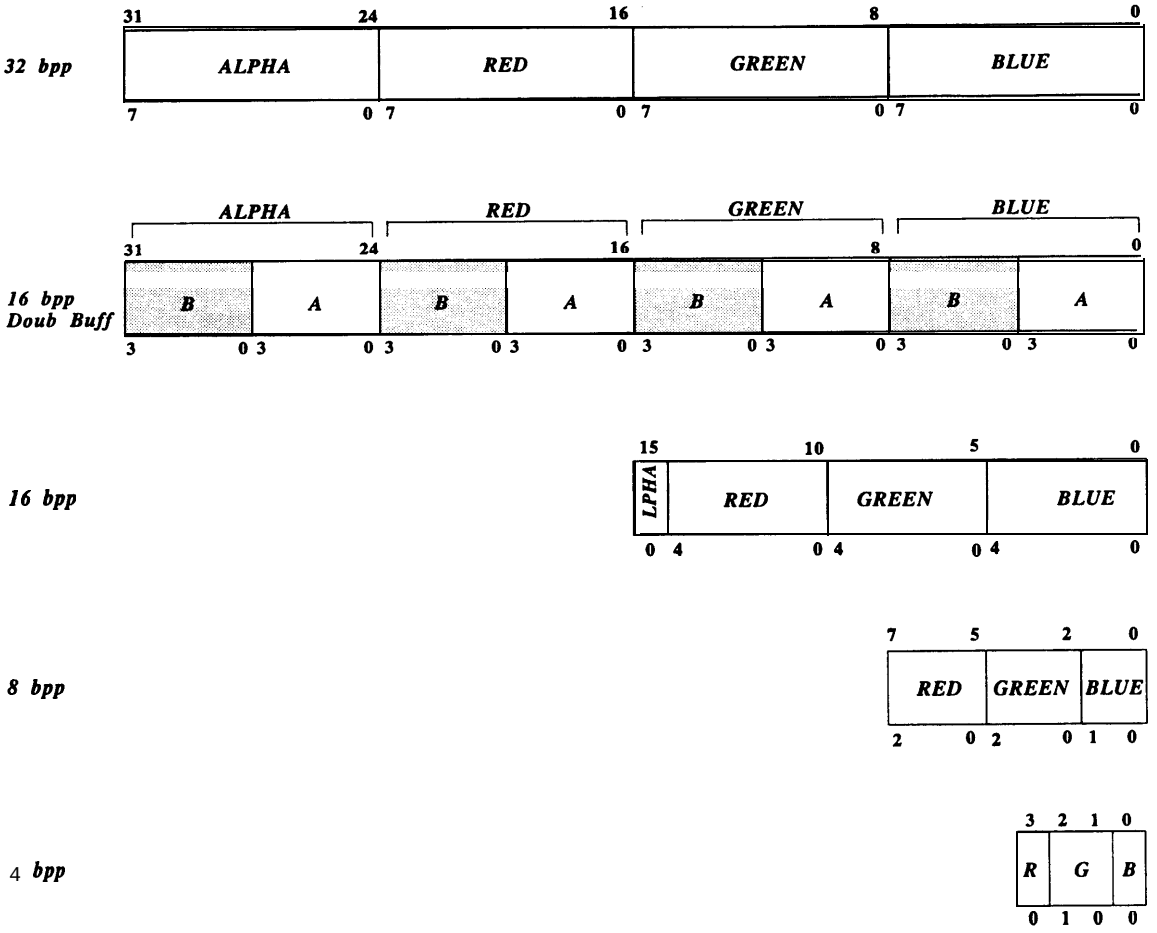


Figure 3-10: Pixel Data

When performing direct frame buffer access, 32-bit access depends on the format of the memory at this location. Data is organized as follows for the various pixel sizes:

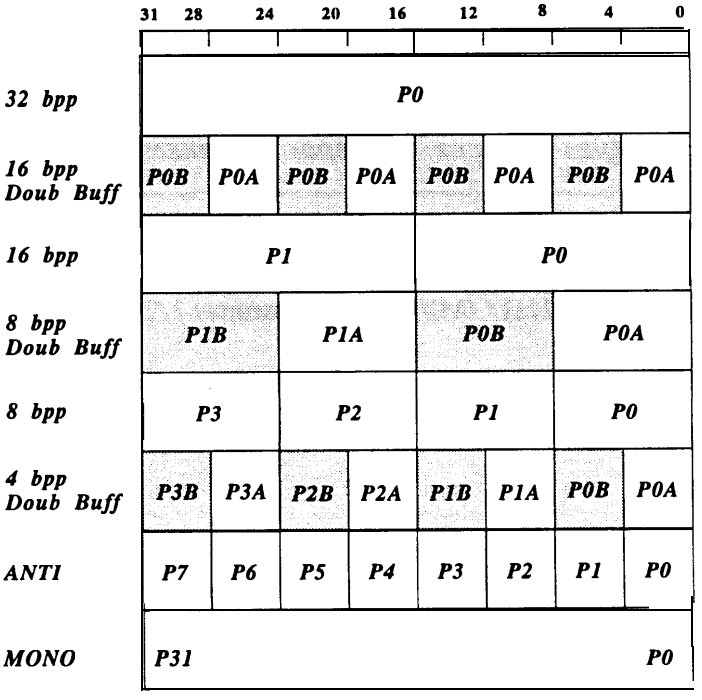


Figure 3-11: 32-bit Access

In addition to the direct **frame** buffer access format, the following formats are supported for **ILOAD** and **IDUMP** operations in **1, 24,** and 32-bits/pixel modes. These formats are selected by the RGB (hbgr) and compress (hcprs) fields of the Drawing Control (DWGCTL) register:

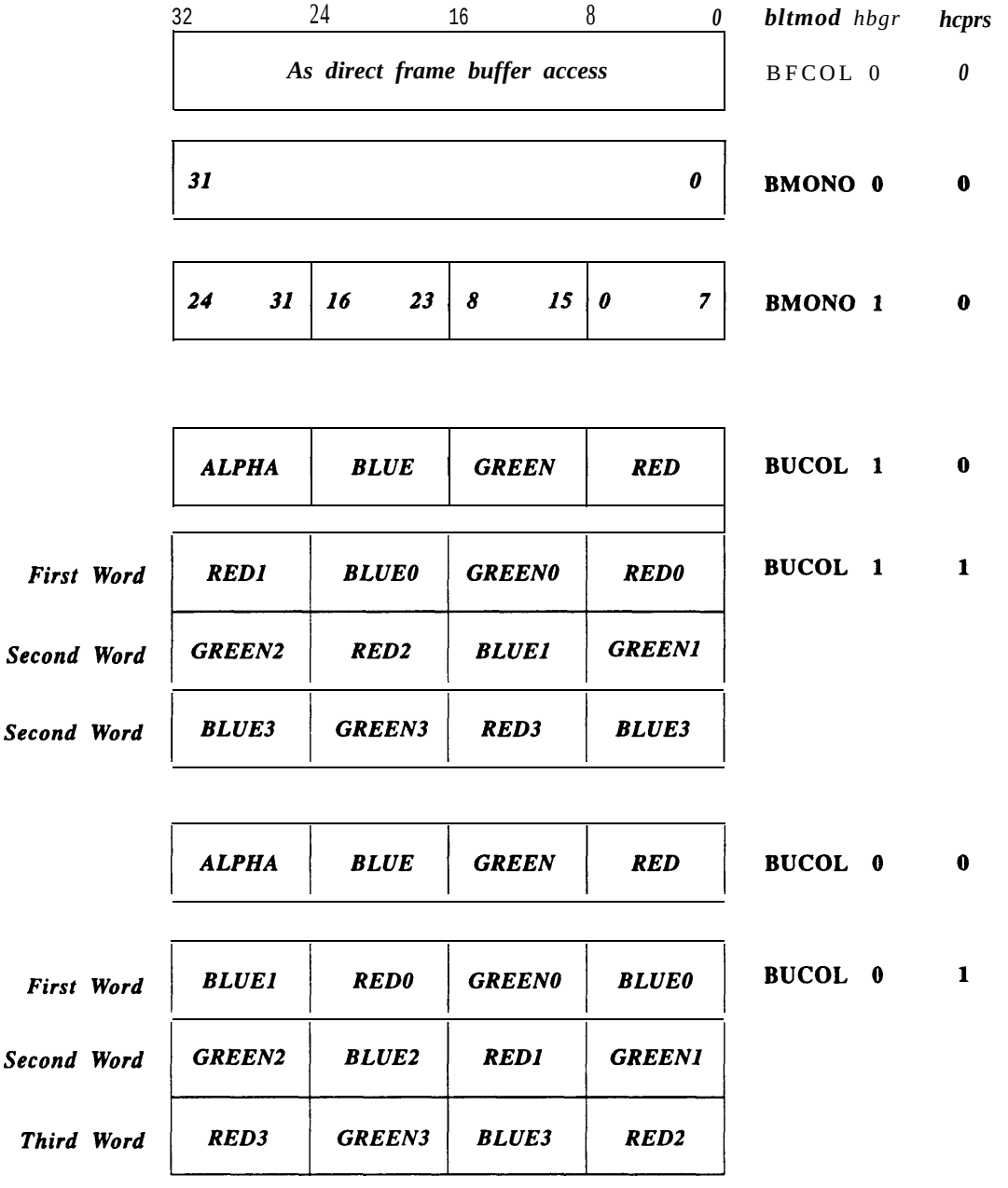


Figure 3-12: ILOAD/IDUMP Formats / 1, 24, 32 bpp

3.2.3 Overview of Drawing Operations

The following three groups of drawing operations are supported by ATLAS:

- **LINE:** Used for vectors. These operations can be auto-initialized. In this case, the Brezenham parameters are automaticaly computed by ATLAS. Brezenham parameters can also be provided directly by the host processor.
- **TRAP:** Used for rectangle fills (1 operand BITBLTs) and polygon drawing.
- **BITBLT:** Used for copy and other operations (2 operand BITBLTs with or without expansion).

All of these drawing operations support several attributes in order to perform different type of actions. The attributes include: line style, patterning, block mode, raster, anti-aliasing, and others.

The following table summarizes how the drawing engine registers must be initialized for these basic operations:

		REGISTERS								
opcode	***event***	***ar0***	***ar1***	***ar2***	***ar3***	***ar4***	***ar5***	***ar6***	***length***	***SGN***
AUTO	INIT	Xend		Yend			Xstar	Ystar		
LINE	END	2b	err	2b-2a			Xend	Yend	0	signs
LINE	INIT	2b	2b-a-Sdy	2b-2a					a	signs
DRAW	END	2b	err	2b-2a					0	signs
TRAP	INIT	dY1	eol	-ldX1l		eor	-ldXrl	dYr	lines	signs
	END	dY1	err1	-ldX1l		errr	-ldXrl	dYr	0	signs
BITBLT	INIT	sea	ssa		sca		syinc		lines	signs
	END	X	X		X		syinc		0	signs

$dX = Xend - Xstart$
$dY = Yend - Ystart$
$a = max(|dx|,|dy|)$
$b = min(|dx|,|dy|)$

$eor = dX_r >= 0 ? - dX_r : dX_r + dY_r - 1$
$eol = dX_l >= 0 ? - dX_l : dX_l + dY_l - 1$
Where x_l = left edge; x_r = right edge
sea = source and address
ssa = source start address
sca = source current address

Table 3-1: Initialization of Drawing Registers

Every time a drawing engine operation is started, the following steps must be taken:

1. Since all drawing registers are accessed through the FIFO, check that there is enough room in the FIFO.
2. Initialize all the drawing registers, preferably starting with the 'K' flag register (see Note (2) following Table 4-4), since some degree of parallelism can be achieved doing this.
3. Start the drawing engine when you write the last register by offsetting the register by 100h.

3.2.4 DMA and Pseudo DMA

ATLAS supports two operating modes in which both the address and data are sent via the data bus:

DMA A DMA channel on the host system is used to sequence operations (ISA interface only).

Pseudo DMA The host processor must sequence all access through the DMAWIN memory space (ISA and PCI interface).

In both cases, the address of the modified register is generated internally by the ATLAS chip. Additional operation modes are available for both DMA and Pseudo DMA:

DMA	*Pseudo DMA*
DMA General Purpose Write	DMA General Purpose Write
DMA Vector Write	DMA Vector Write
DMA BLIT Write	DMA BLIT Write
	DMA BLIT Read

DMA General Purpose Write

The first double word (dw) transferred is loaded into the Address Generator. This dw contains the addresses of the next four drawing registers to be written, and the next four dw transfers contain the data to be written to those four registers.

When each dw of data is transferred, the Address Generator will send the appropriate 7-bit address to the Bus FIFO. When the fourth (final) address has been used, the next double word transfer reloads the Address Generator.

A direct access to a drawing register during a Pseudo DMA General Purpose write resets the Address Generator state machine to the 'LD ADR_GEN' state. The following Pseudo DMA write transfer must contain the addresses of the data for the next four drawing registers. The cycle is illustrated below.

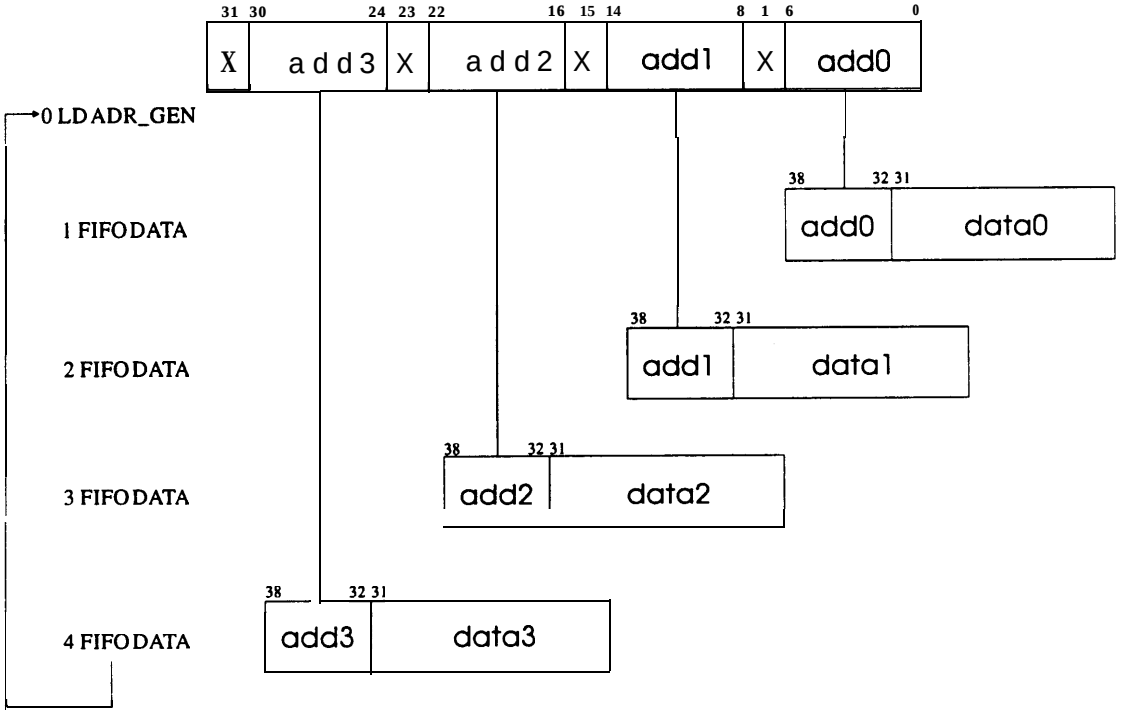


Figure 3-13: DMA General Purpose Write Sequence

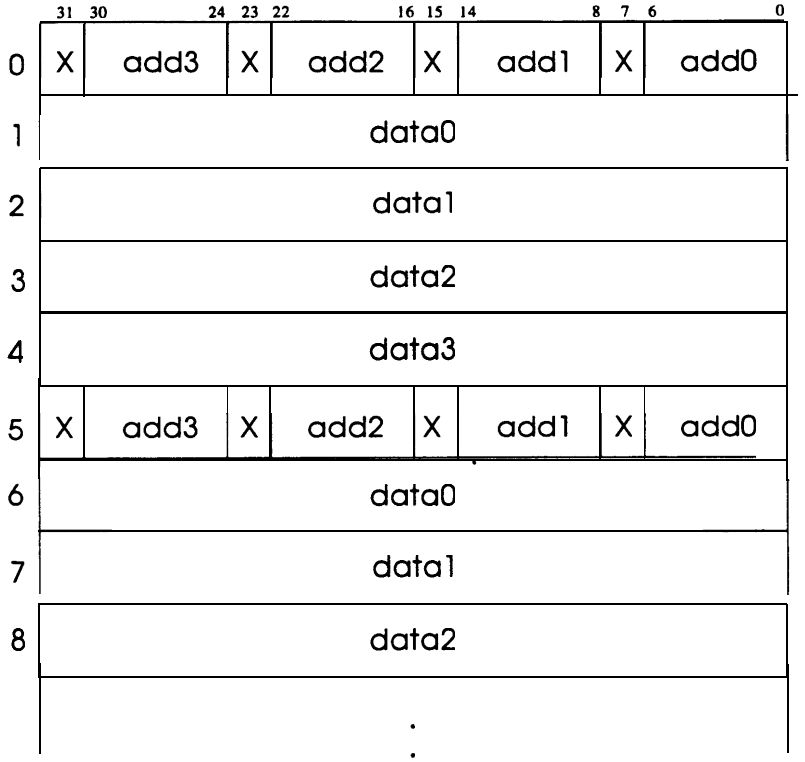


Figure 3-14: DMA Gen. Purpose Transfer Buffer Structure

DMA Vector Write

The first double word transferred is loaded into the Address Generator. This dw contains one bit of 'address select' for each of the next 32 vector vertices to be sent to the drawing registers. These 32 bits are called the vector tags. The next 32 double word transfers contain the XY address data to be written to the drawing registers.

When the tag bit is set to zero (0), the address generator will force the address to that of the XYStart register without setting the bit to start the drawing engine. When the tag bit is set to one (1), the address generator will force the address to that of the XYEnd register with the flag set to start the drawing engine.

When each dw of data is transferred, the Address Generator checks the associated tag bit and sends the appropriate 7-bit address to the Bus FIFO. When the 32^{nd} (final) tag has been used, the next double word transfer reloads the Address Generator with the next 32 vector tags.

A direct access.to a drawing register during a Pseudo DMA VECTOR resets the Address Generator state machine to the 'LD ADR_GEN' state. The following Pseudo DMA write transfer must contain the vector tags for the next XY coordinate data.

The cycle is illustrated on the next page.

When Vn = 0, addn = XY_START address (10h)

When Vn = 1, addn = XY_END address + START DWG ENG (51h)

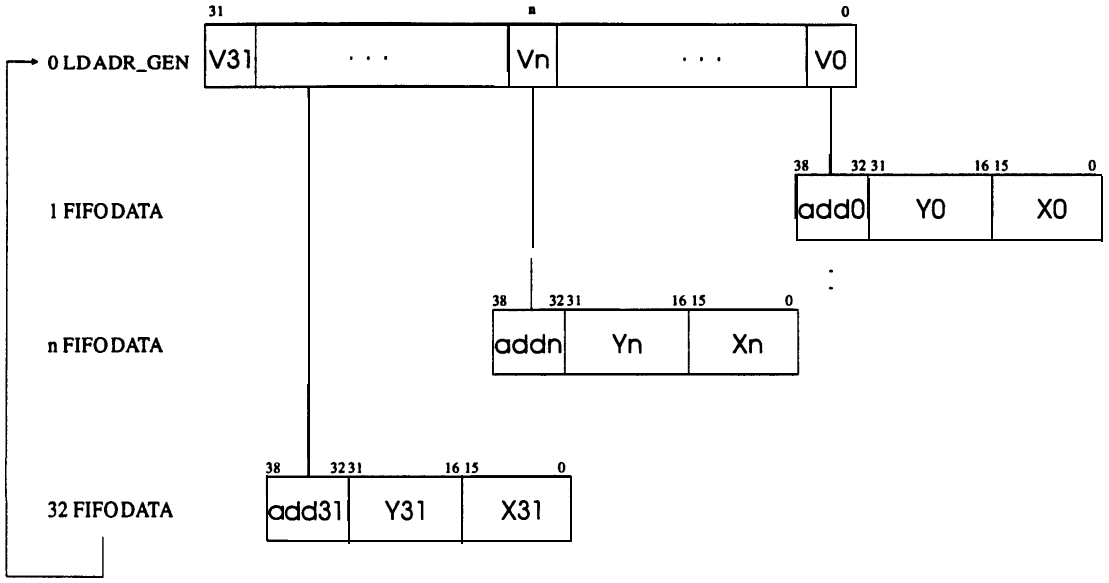


Figure 3-15: DMA Vector Sequence

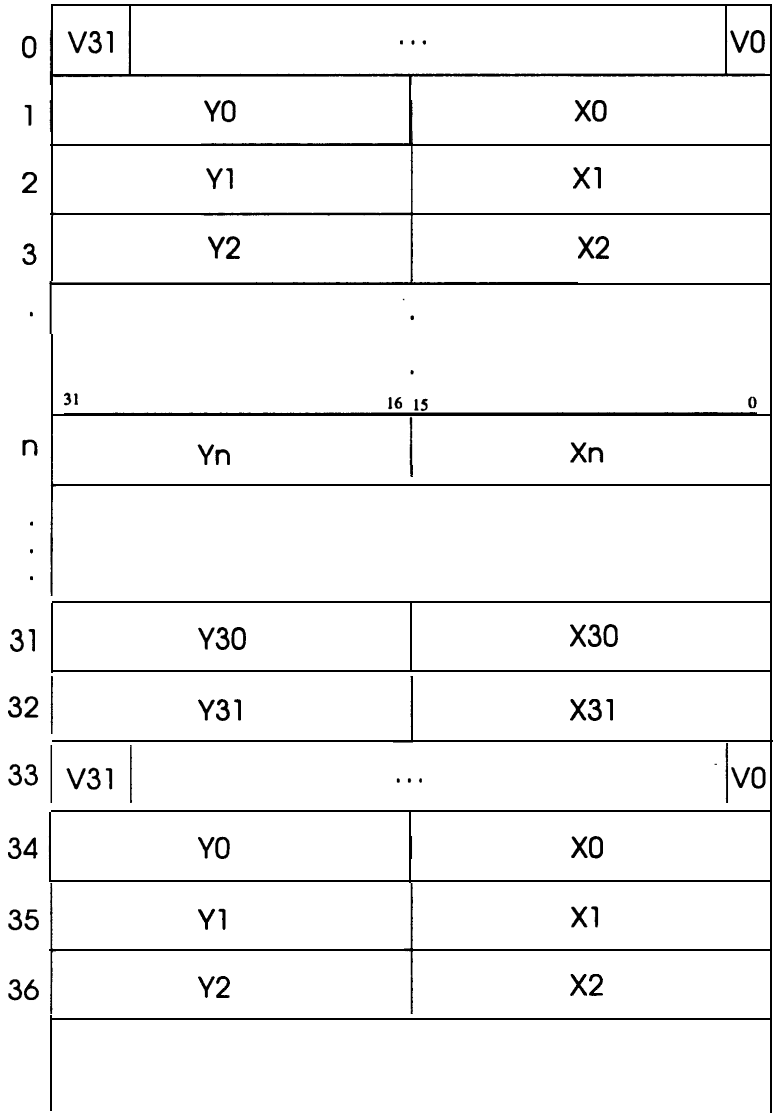


Figure 3-16: DMA Vector Transfer Buffer Structure

DMA BLIT Write

The DMA BLIT write is hard coded, so there's no reason to load the Address Generator. The result is that every transfer consists of data to be transferred.

When each dw of data is transferred, the Address Generator sends the srcregblit register address to the Bus FIFO. The address generator state machine is not used for this type of DMA.

All pixels expected by the drawing engine must be transferred, otherwise it could jam. The total number of dword transfers needed to complete the BLIT operation depends on, among other factors:

- The size of the window to be drawn (upper left comer coordinate, length in X and Y)
- The number of bits per pixel (8, 16, or 32)

The cycle is illustrated below. No address is required for data transfer during DMA blits, so 'add' is 'don't care'.

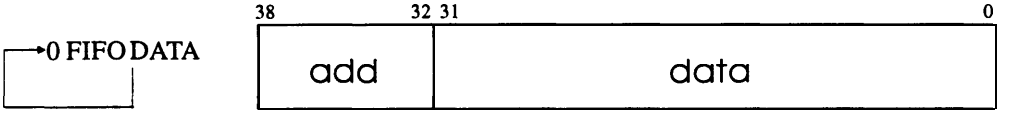


Figure 3-17: DMA BLIT Write Sequence

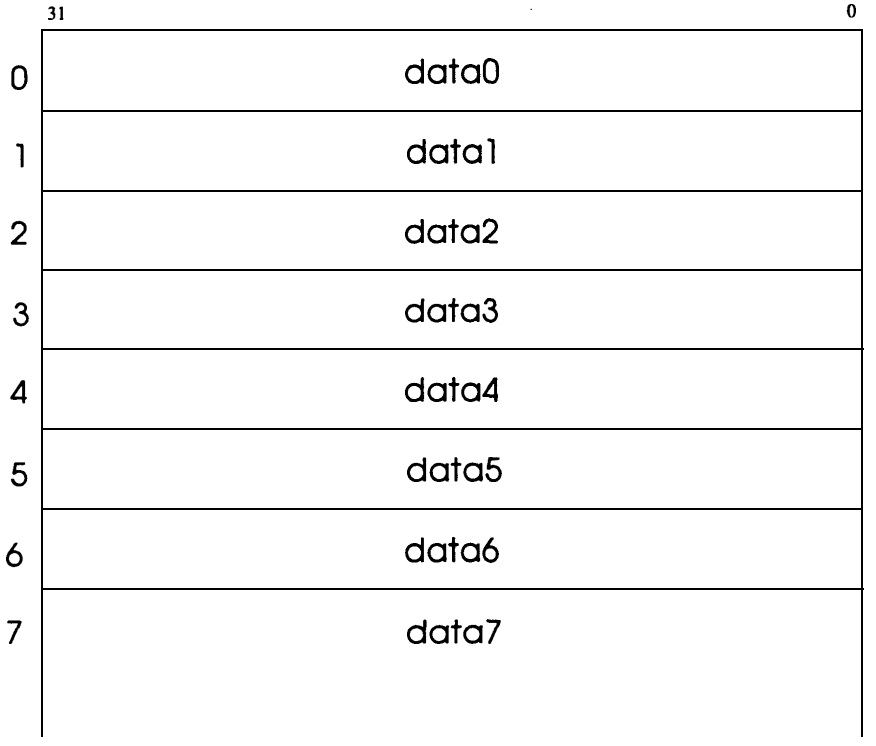


Figure 3-18: DMA BLIT Write Transfer Buffer Structure

DMA BLIT Read

As specified earlier, the DMA BLIT Read mode is available for Pseudo DMA only, and is used to dump pixels from a window of the screen to system memory. Each double word that's transferred may contain 4, 2, or 1 pixel(s), depending on the configuration (8, 16, or 32 bits per pixel, respectively).

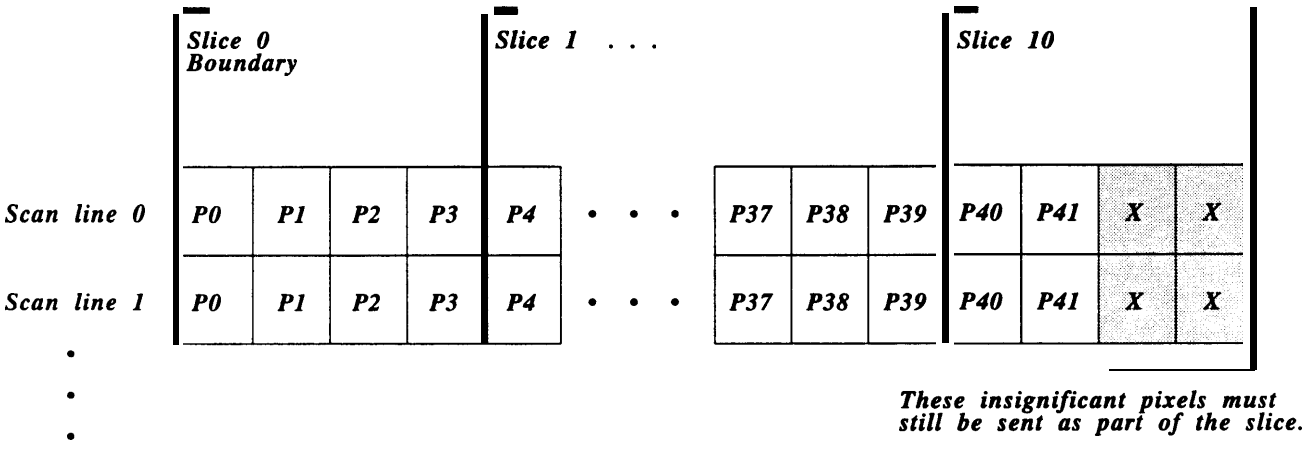
The coordinate of the upper left comer and the length in X and Y are a few of the parameters that are required by the graphic engine for this operation.

A ***Important Note:***

It is ***extremely important*** that the number of dwords dumped accounts for all of the pixels that are to be transferred. The last dword for ***each scan line of pixels*** may contain insignificant information in the case of 8 or 16 bit/pixel modes if the number of transferred pixels is not evenly divisible by 4 (for 8 bpp modes) or by 2 (for 16 bpp modes).

- If the window to be drawn is not aligned at the beginning of a slice, the insignificant pixels to the left of the window are effectively disregarded, and the slice alignment begins at the start of the window.

The following illustration shows the case of an 8 bits/pixel mode transfer that is 42 pixels wide:



3.2.4.1 DMA

- The ATLAS chip's DMA capabilities can only be used with the AT (ISA) interface.

ATLAS supports only DMA I/O write transfers. The goal is use the host's DMA controller to transfer a block from the system memory into ATLAS's Bus IWO (only the Bus FIFO is accessed during DMA write). This provides a means to write to drawing registers for specific drawing operations.

Only **16-bit** DMA transfers are supported. The total number of transfers must be an integral number of double words, to align with ATLAS's internal 32-bit data bus. The words are accumulated before sending double words to the Bus FIFO. The memory block to be transferred must be aligned on a double word boundary.

Timing Type	*Mode*	*Data Size*	*System*
ISA Compatible	Single	16	ISA/EISA
Type 'B'	Single	16	EISA
	Demand	16	EISA

Table 3-2: DMA Access Types

To initiate a DMA transfer, take the following steps:

1. Ensure that 'dmaact' and 'pseudodma' (OPMODE register bits 1 and 0) are not active (active if '1').
2. Program the dmamod bits (OPMODE register bits 2 and 3) to one of three modes listed below (keep dmaact and pseudodma at '0'):
   - DMA General Purpose Write
   - DMA BLIT Write
   - DMA Vector Write

   The function of the dmamod bits is explained later on.
3. Program the host DMA controller.
4. Start the DMA transfer by setting dmaact to '1' (keep pseudodma at '0').

Once dmaact is set, ATLAS will request DMA service by asserting DRQ. The requests will continue until the terminal count is reached. If the Bus FIFO becomes full during the DMA transfer, the request will stop automatically and resume when there is space available in the Bus FIFO.

When the DMA transfer is in progress, any access to the following devices is forbidden:

- The drawing registers (offset 1C00h - 1DFFh)
- VRAMWIN (offset 0000h - 1BFFh, vgaen = '0' and pseudodma = '0' - see Chapter 4)
- DMAWIN (offset 0000h - 1BFFh, vgaen = '0' and pseudodma = '1')

Access to other MGA resources is still possible, however.

Dmaact will be automatically reset after the last transfer, when the DMA terminal count (TC) is sampled active.

DRQ is normally tri-state. When dmaact is active, DRQ is driven to the appropriate state. This allows for resource sharing in a system with multiple MGAs. Only one MGA can have dmaact active at any time. When dmaact becomes inactive due to TC, ATLAS will have been driving DRQ low, then it will tri-state the signal.

It's possible to generate an interrupt when a DMA terminal count occurs. For more information, refer to Section 3.2.6.

3.2.4.2 Pseudo DMA

The goal of Pseudo DMA is the same as that of DMA, with the only difference being that read transfers are possible. Instead of using the DMA controller, Pseudo DMA transfers are 'move string' instructions in the DMAWIN memory space (offset 0000h - 1BFFh, vgaen = '0' and pseudodma = '1').

Only double word accesses (read or write) are allowed in the DMAWIN memory space. When performing Pseudo DMA transfers, all of the MGA map is available, except the VRAMWIN memory space, which is disabled.

Write Transfers

To transfer a block of data from the system memory to the Bus FIFO of the ATLAS chip, the steps listed below must be followed:

1. Make sure that 'dmaact' and 'pseudodma' are not active.
2. Program the dmamod bits to one of the three modes listed below (keep dmaact and pseudodma at '0'):
   - DMA General Purpose Write
   - DMA BLIT Write
   - DMA Vector Write

   a) If DMA BLIT Write is used, program all affected drawing registers. Note that all writes to the drawing registers must be double word accesses.

   b) If DMA BLIT Write is used, send the ILOAD opcode to the drawing engine.
3. Set 'pseudodma' to '1' (keep dmaact at '0').
4. Transfer system memory data to the MGA DMAWIN memory space, with 'move string' or 'read and write' instructions.
5. Reset 'pseudodma' to '0' at the end of the block transfer.

As long as the Bus FIFO isn't full, and if the **nowait** bit of the OPMODE register is set to '1' , then no wait will be generated for write cycles to the DMAWIN memory space. When the Bus FIFO is full, there is one more dword location, which is the Byte Accumulator of the host section. Once the Byte Accumulator and the Bus FIFO are full, the next write to the DMAWIN space will be put in waiting as long as the Byte Accumulator data isn't loaded in the Bus FIFO.

If the CHRDY ready signal is kept inactive for more than 64 gclks, the STATUS register bferrsts bit will be set. This will cause an interrupt if the proper interrupt enable is set. If CHRDY is still inactive after 128 gclks, the host section will abort the write cycle by reasserting CHRDY and by resetting the Byte Accumulator full flag.

For DMA BLIT Write operations, the drawing engine will fetch data until all pixels have been loaded, once the ILOAD opcode is sent, and if the Bus FIFO isn't empty.

Read Transfers

To dump screen data to the system memory, take these steps:

1. Make sure that ‘dmaact’ and ‘pseudodma’ are not active.
2. Program the dmamod bits to DMA BLIT Read (keep dmaact and pseudodma at ‘0’).
3. Program all affected drawing registers. Note that all writes to the drawing registers must be double word accesses.
4. Set ‘pseudodma’ to ‘1’ (keep dmaact at ‘0’).
5. Send the IDUMP opcode to the drawing engine.
6. Transfer data from the DMAWIN memory space to the system memory, with ‘move string’ or ‘read and write’ instructions.
7. Reset ‘pseudodma’ to ‘0’ at the end of the dump.

Once the IDUMP opcode is sent to the drawing engine, it begins fetching pixels from the VRAMs. During a read in the DMAWIN memory space, CHRDY will be deactivated (ISA bus system), or a retry will be generated (PCI bus system) if the data from the drawing engine isn’t ready. When the data is available, it will be latched in the host section of ATLAS, and the access is completed. A new request will be sent to the drawing engine for the next dword when the last byte, the last word, or the current dword is being read, depending on whether ATLAS is 8, 16, or 32-bit. The latched dword will be present until all bytes are read.

If an access takes more than 64 gclks, the bferrsts bit will be set in the STATUS register. This may cause an interrupt if the proper interrupt enable is set. If an access takes more than 128 gclks, the host section will abort the read cycle.

3.2.5 Programming the CRTC for Power Graphic Mode

This section explains the video parameters required for the Power Graphic display modes.

3.2.5.1 Registers

In Power Graphic mode (for all resolutions and pixel depths), the video parameters that are programmed in the registers are **always** based on a video clock that is divided by 8.

- :* Note: When you change any video parameters, it is important to halt the video operation circuitry of the VRAM chips to prevent the VRAMs from entering an unrecoverable state. The 'Screen Off' bit in the Clocking Mode sequencer register (Address 1FC5, Index 01, Bit 5) will force the screen to blank and halt the VRAM circuitry mentioned above. This bit must be maintained to 'off' for at least 10 µs after the last video parameter modification.

The CRTC_CTRL register is used as specified. Table 3-3 shows the registers that are implicated in programming the video for the Power Graphic modes.

3.2.5.2 Interlace Modes

In Power Graphic mode, the hardware can only be properly programmed in interlace modes at specific memory pitches (768, 1024, and 1280). For other pitches, the hardware must be programmed in such a way that the display area is less than the memory pitch.

It is not possible to have a horizontal resolution greater than 1280 pixels in interlace mode.

3.2.5.3 Hardware Panning

Panning is achieved by programming a start address that is equivalent to the desired region. The start address is programmed in two VGA CRTC registers and one auxiliary register. Panning must be done on a multiple of 16 pixels.

3.2.5.4 Hardware Zooming

Zooming by lx, 2x, and 4x is supported.

Zooming in the X direction is performed by the clock generator. For the CRTC, this is seen simply as a division of the video clock. However, the CRTC registers that control the horizontal signals must be reprogrammed properly (relative to the divided clock) to deliver the same frequency to the monitor.

It's important to note that if you wish to maintain a constant image between each zoom switch, the horizontal parameters must be exact multiples. For this reason, multiples of 32 must be used for each parameter (front porch, sync, etc.), even if you zoom by lx.

To zoom in the Y direction, you must reprogram the Maximum Scan Line register in the CRTC. This will affect the way that the CRTC address counter generates line addresses.

The dt request module must also operate in non-automatic line wrap mode (refer to Bit 2 of the CRTC_CTRL Power Graphic mode register description on page 5-53) when not zooming by **1x.**

3.2.5.5 Programming Constraints

In order to have a correct image on the screen, you must respect different constraints when calculating the video parameters. The videodelay field of the CRTC_CTRL register can be programmed for 3, 4, 5, 11, 24, or 28 vidclks. The video parameters must be calculated so that at least one of the six possible values of videodelay meets the three constraints. Unexpected video results could occur otherwise.'

Section	*Index*	*Name*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*DO*
CRTC	00	Horizontal Total	S	S	S	S	S	S	S	S
	01	Horizontal Display Enable End	S	S	S	S	S	S	S	S
	02	Horizontal Blanking Start	S	S	S	S	S	S	S	S
	03	Horizontal Blanking End	0	0	0	S	S	S	S	S
	04	Horizontal Retrace Start	S	S	S	S	S	S	S	S
	05	Horizontal Retrace End	S	0	0	S	S	S	S	S
	06	Vertical Total	S	S	S	S	S	S	S	S
	07	Overflow	S	S	S	1	S	S	S	S
	08	Preset Row Scan	0	0	0	0	0	0	0	0
	09	Maximum Scan Line	0	1	S	Z	Z	Z	Z	Z
	0A	Cursor Start	0	0	1	X	X	X	X	X
	0B	Cursor End	0	X	X	X	X	X	X	X
	OC	Start Address High	S	S	S	S	S	S	S	S
	OD	Start Address Low	S	S	S	S	S	S	S	S
	OE	Cursor Position High	X	X	X	X	X	X	X	X
	OF	Cursor Position Low	X	X	X	X	X	X	X	X
	10	Vertical Retrace Start	S	S	S	S	S	S	S	S
	11	Vertical Retrace End	S	X	S	S	S	S	S	S
	12	Vertical Display Enable End	S	S	S	S	S	S	S	S
	13	Offset	S	S	S	S	S	S	S	S
	14	Underline Location	0	0	0	X	X	X	X	X
	15	Vertical Blanking Start	S	S	S	S	S	S	S	S
	16	Vertical Blanking End	S	S	S	S	S	S	S	S
	17	Mode Control	S	X	X	0	0	S	X	X
	18	Line Compare	1	1	1	1	1	1	1	1
AUX	00	Mode Control Register	x	x	x	0	0	0	0	0
	02	Emulation Control Register	0	x	x	x	x	x	x	x
	OA	CRTC Extended Address Register	S	X	X	1	X	X	S	S
	OD	Interlace Support Register	x	s	x	x	x	x	x	x
	OE	Vertical Sync Adjust Register	s	s	s	s	s	s	s	s
SEQ	01	Clocking Mode	x	x	s	x	x	x	x	x
		Miscellaneous Output Register	1	1	x	0	s	s	x	s

Legend:
- 0 The bit must always be programmed to 0
- 1 The bit must always be programmed to 1
- X The bit can be programmed to either 0 or 1
- S The bit works as specified
- Z The bit is used by the zoom in the Y direction

Table 3-3: Power Graphic Mode Video Registers

The following formula explains how to calculate the three constraints. The drawing engine response (in video clocks) is:

$$dw\_eng\_res = \frac{int(925ns * videofrequency + 0.9)}{8}$$

Constraint #1: Videodelay >= ***Horizontal FrontPorch+2–3***

Constraint **#2:** Videodelay >= ***dw_eng_res+l-*** $1^5/_8$

Constraint **#3:** Videodelay **=<** ***Horizontal blank+l-dw_eng_res-3***

3.2.5.6 Frame Buffer Alignment

When 'No DUBIC' mode is selected, the frame buffer display must be arranged in such a way that bank switching appends during the blank (between two lines).

For example:

Assume that we want to display 1280x1024x8 using two 1MB banks. The bank transition occurs after 1M pixels:

1048576	/	1280	=	819.2
pixels		***pixels/line***		***lines***

Round this up to 819 lines, and up-front padding will have to be added in order to ensure that the bank transition takes place between two lines:

1048576	-	(1280	*	819)	=	256
pixels		***pixels/line***		***lines***		***pixels***

This means that the frame buffer will have to be started at address 256 (rather than at address 0). This produces the following results:

- The CRTC start address must be 256, rather than 0.
- The drawing operation must be moved by 256 pixels. This can be done automatically by the drawing engine for the destination address by initializing YDSTORG to 256. Note that this will affect the value loaded in CYBOT and CYTOP. For source addresses this adjustment will have to be done manually.
- Off-screen memory is reduced by 256 bytes.

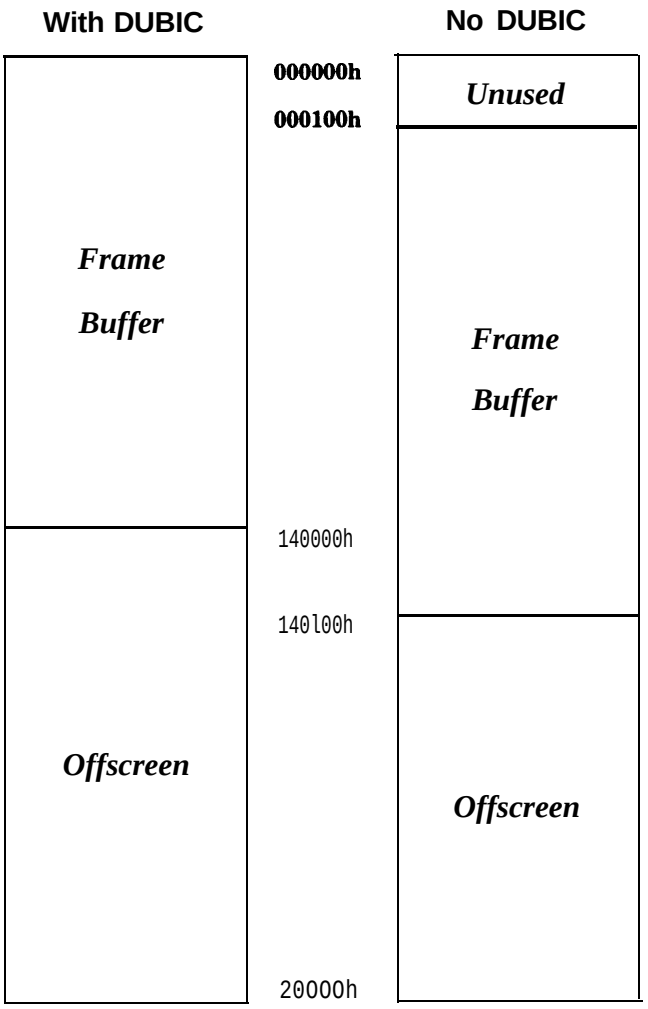


Figure 3-19: Memory Org. (1280x1024x8 - two 1M Banks)

3.2.5.7 Overscan

The hardware can support the overscan feature, but using it will reduce the length of the blank period. This reduced blank will have a direct impact on your ability to meet the constraints of the video delay. It might be possible to lose the zoom feature at low resolutions, or even the integrity of the display itself if the overscan is large.

3.2.6 Interrupts

ATLAS supports interrupts for both ISA and PCI configurations.

- In the ISA configuration, ATLAS can generate two types of interrupts: edge interrupts, and level interrupts. The choice of interrupts is system-dependent, and is programmed by the CONFIG register's levelirq bit. In the Power Graphic modes, several interrupt sources exist:

Interrupt	*Description*
Bus FIFO Error Interrupt	This interrupt is generated when a cycle is aborted. It is useful during software debugging and testing.
DMA TC Interrupt	This interrupt is generated when a terminal count occurred at the end of a DMA transfer.
Picking Interrupt	This interrupt is generated when a pixel is written by the drawing engine.
Vertical Sync Interrupt	This interrupt is generated at every vertical sync. ***Note:*** The vertical sync interrupt behaves differently than the others, because two other bits must be set for it to be enabled. Bit 7 of the AUX_DATA register, and Bit **5** of the Vertical Retrace End register (lFB5/1FD5, Index 11) must be set before the vertical sync interrupt can be enabled. ***Note:*** This interrupt must be cleared by accessing Bit 4 of the Vertical Retrace End register (lFB5/lFD5, Index 11).

Table 3-4: Interrupt Sources

- In the PCI configuration, ATLAS uses only one interrupt line (INTA), and is a single function device. In order to integrate the DUBIC interrupts, the other external interrupts, and the current TITAN interrupt, a new register has been added.

  In the PCI configuration, the interrupts must be programmed as level interrupts (levelirq) in the CONFIG register.

Three registers are used for interrupt control:

STATUS This register indicates the status of each of the interrupt sources.

IEN This register is used to individually enable each of the four interrupt sources.

ICLEAR This register is used to individually reset each of the four interrupt sources. Note that there is no bit in this register to clear the vertical sync interrupt, which is cleared by accessing Bit 4 of the Vertical Retrace End register (lFB5/lFD5, Index 11).

3.3 Access Restrictions to Some Resources

Consideration must be given to several resource access restrictions (which vary depending on how the ATLAS chip is used in a system). Refer to the information on bus sizing in Sections 6.2.1.3 and 6.2.2.1.

3.4 Initialization and Configuration

3.4.1 Configuration Elements

Note: In the lists which follow, ***H*** indicates that a field is hard-reset. All others are soft-reset. When MGA is powered up, ATLAS's **DSTx** registers are loaded with the following configuration elements:

pcbrev<3:0>	**rambank<8:0>**	ramspeed<l:0>	expdev
product<3:0>	**vgabank0**	hyperpg<1:O>	tram

As well, ATLAS's host interface section receives these configuration elements:

H config<1:0>	***H*** vgaen	***H*** above lmeg	***H*** poseidon	***H*** **vbank0**
H driverdy	*H* biosen (indirectly, according to vgaen)	***H*** mapsel<2:0>	***H*** **isa**	

The following configuration elements are not programmed at power up:

ATLAS drawing engine:

mctlwtst (RO)

ATLAS host interface:

ien<3:0>	*H* **mouseen**	hyperpg<l:O>*	interlace<1:O>	*H* vesafeat
H levelirq	*H* **mousemap**	tram*	videodelay<l:0>	
expdev*	rfhcnt<3:0>	crtcbpp<1:0>	*H* hrsten	
H **nowait**	**fbm<2:0>**	alw	*H* vrsten	

* Value available in DST0

3.4.2 Booting in VGA Mode

The following configuration elements from the ATLAS host interface affect the VGA, and are not programmed at power up. All the other elements are VGA-standard, and are taken care of by the BIOS.

H levelirq	*H* vesafeat	*H* hrsten	*H* vrsten

3.4.3 Booting in Power Graphic Mode

The following operations take place during the Power Graphic mode boot procedure:

1. In a PCI system, the PCI Configuration Space is initialized by the system booting procedure.
2. The card is detected
3. Configuration straps/switches are read
4. Depending on the configuration information and the selected hardware mode, the following non-initialized configuration elements must be programmed at power up:

- ATLAS host interface
- ATLAS drawing engine
- Video Interface (DUBIC if present)
- RAMDAC
- CLOCK GEN
- VGA-CRTC

3.5 Mode Switching

3.5.1 Switching From VGA Mode to Power Graphic Mode

If the system has no DUBIC, disregard any step that mentions the DUBIC chip.

1. Make a call to the BIOS to select VGA Mode 3.
2. Disable VGA Mode.

   - Once the VGA has been disabled, reset the vgaen bits in ATLAS's CONFIG register.

3. Disable interrupts from DUBIC.

   ❖ Note: If you'll be returning to Power Graphic mode later, make a note of the current value of DUBIC's DUB_SEL register.

   - Set DUBIC's DUB_SEL register to 40h.

4. Stop the enhanced mode sequencer.

   - Set the softreset bit in ATLAS's RESET register, then wait 1.5 µsec.

5. Set DUBIC to Power Graphic mode.

   - Reset the blankdel and vga_en bits in DUBIC's DUB_CTL register.

6. Restart the Power Graphic sequencer.

   - Reset the softreset bit in ATLAS's RESET register, then wait 1.5 µsec.

7. Restore the value of the DUB_SEL register of the DUBIC.
8. Restart Initialization of Power Graphic mode.

3.5.2 Switching From Power Graphic Mode to VGA Mode

If the system has no DUBIC, disregard any step that mentions the DUBIC chip.

1. Place the card in ISA mode if it's currently in WIDEISA mode.

   - If the isa bit in ATLAS's CONFIG register is 0:

     - Unlock access to the isa bit by writing 1000 1101 b to the MSB byte in ATLAS's TEST register.
     - Set the isa bit in ATLAS's CONFIG register.
     - Lock access to the isa bit.

2. Disable the interrupts from DUBIC.

   Note : If you'll be returning to Power Graphic mode later, make a note of the current value of DUBIC's DUB_SEL register.

   - Set DUBIC's DUB_SEL register to 40h.

3. Stop the Power Graphic sequencer.

   - Set the softreset bit in ATLAS's RESET register, then wait 1.5 µsec.

4. Place DUBIC in VGA mode.

   - Set the srate bit in DUBIC's DUB_CTL register. If the bus mouse is enabled, set SRATE = 18. If the laser printer port is enabled, set SRATE = 2

   - Set the blankdel and vga_en bits of DUBIC's DUB_CTL register.

5. Restart the Power Graphic mode sequencer.

   - Reset the softreset bit in ATLAS's RESET register, then wait 1.5 µsec.

6. Place the RAMDAC in VGA mode. Program the appropriate registers as shown below:

   For the BT485 RAMDAC:

   Command register 0 = 0000 0000 b

   Command register 1 = 0000 0000 b

   Command register 2 = 0000 0000 b

   Command register 3 = 0000 0000 b

   For the BT482 RAMDAC:

   Command register A = 0000 0000 b

   Command register B = 0001 1110 b

   Command register C = 0000 0000 b

7. Program the LookUp Table (LUT) for VGA

8. Activate VGA Mode

   - Set the vgaen and biosen bits of ATLAS's CONFIG register.

9. Restore the value of DUBIC's DUB_SEL register.

10. Make a call to the BIOS to select a VGA mode (for example: Mode 3 for text).

3.6 Power up and Reset

It's possible to reset ATLAS with a hard or soft reset. Both methods are explained in the following subsections.

3.6.1 Hard Reset

A hard reset results when a low pulse is applied to the reset pin of the ATLAS chip. The minimum pulse width required is 8 µs.

On a hard reset, the following resources are reset:

- VGA section
- Drawing engine
- Bus FIFO
- Host section
- All registers

As well, external configurations are loaded into registers, as appropriate.

Three rules must be followed for proper chip reset:

1. In the PCI configuration, no host access must occur within the first two PCLKs of a hard reset.
2. LDCLK, GCLK, and PCLK must be active during reset.
3. You must ensure that a PLL or clock oscillator oscillates within specifications when the power-up reset ends.

3.6.2 Soft Reset

A soft reset results when bit 0 of the RESET register is set to '1', then reset to '0'. On a soft reset, external strapping is not loaded.

The soft reset also initializes the Bus FIFO and all of the drawing engine. The values of the drawing registers are lost.

On the host section, some register bits are hard reset only. See Chapter 5 for more details. On the control section of the host, only three state machines are affected by the soft reset:

- IDUMP state machine
- DMA state machine (note that **DMA is not available on PCI bus boards)**
- ADRGEN state machine

3.6.3 Configuring ATLAS in a Board-level Design

The ATLAS requires that configuration information be placed on the VD<63:0> bus during reset. The configuration information defines the available resources as well as the mode in which ATLAS will operate. More specifically, the following types of information are contained in the configuration bits:

- Hardware resources (memory banks, memory speed, etc.)
- Product ID and revision
- Host Interface information (Address mapping, 8/16-bit, etc.)
- Information used internally to control the operation of the ATLAS

There are two types of configuration bits:

- **Soft** configuration bits are read and used by software
- **Hard** configuration bits are loaded directly into internal registers

Upon reset, the contents of VD<31:0> are sent to DST0<31:0>; **VD<63:32>** is sent to DST1<31:0>.

- Z* Note that the destination registers must be read before any direct access to the frame buffer, or drawing engine operation is performed, in order to obtain valid data.

Configuration bus VD<63:0>

A summary of the configuration bus follows, along with a table which defines each of the configuration bits.

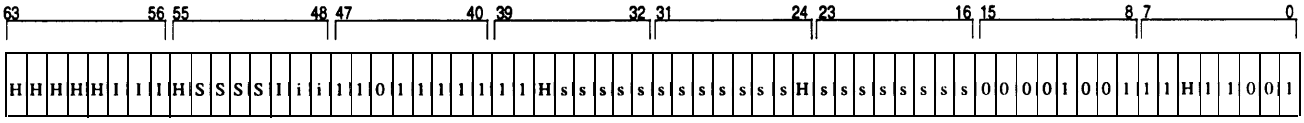


Figure 3-20: Configuration Bus

Legend:

0,1 Hard bits which must be set to the indicated value upon reset.
H Hard bits which are loaded directly into internal registers upon reset.
i Soft bits which software must read from the bus, invert, and then load into the appropriate internal register. *
I Hard bits which are automatically inverted and then loaded into an internal register upon reset. *
s Soft bits which software must read from the bus. These bits are not stored internally.
S Soft bits which software must read from the bus and then load into the appropriate internal register.

Hard bits (H, I) which are loaded into other registers should be read from those destination registers, not from DST0/DST1.

* Since the bit is inverted, a pull-up will initialize it to 0, and a pull-down will initialize it to 1.

VD Bus Bit	*Definition*	*Hard/Soft Configuration*		*Where Used*
4:0	Internal	Hard	(H)	Internally (See Figure 3-20 for values)
5	vgaen0	Hard	(H)	Host (CONFIG<10:9>), VGA
15:6	Internal	Hard	(H)	Internally (See Figure 3-20 for values)
19:16	PCB Revision	Soft	(s)	Read from board
23:20	Product ID	Soft	(s)	Read from board
24	vgabank0	Hard	(H)	Host (OPMODE<11>)
32:25	rambank	Soft	(s)	Read from board
34:33	ramspeed	Soft	(s)	Read from board
35	rambank	Soft	(s)	Read from board
36	HiRes/	Soft	(s)	Read from board
37	vgaen1	Hard	(H)	Host (CONFIG<10:9>)
38	testwren	Hard	(1)	Host (TEST<9>)
47:39	Internal	Hard	(H)	Internally (See Figure 3-20 for values)
48	200MHz	Soft	(i)	Host (CONFIG<2>)
49	misc<1>	Soft	(i)	Host (CONFIG<3>)
50	nodubic	Hard	(I)	Host (CONFIG<4>)
52:51	hyperpg	Soft	(S)	Host (OPMODE<25:24>)
53	expdev	Soft	(S)	Host (CONFIG<16>)
54	tram	Soft	(S)	Host (OPMODE<26>)
63:55	Internal (Host):			
55	isa	Hard	(H)	Host (CONFIG<28>)
56	pci	Hard	(I)	Host (CONFIG<27>)
57	above1meg	Hard	(I)	Host (CONFIG<12>)
58	driverdy	Hard	(I)	Host (CONFIG<8>)
61:59	mapsel	Hard	(H)	Host (CONFIG<26:24>)
63:62	config	Hard	(H)	Host (CONFIG<1:0>)

Table 3-5: Strapping Definition: ATLAS-based Design

Note: To ensure compatibility with future software, bits VD<49:48> should be enabled high ('1') during reset.

3.6.3.1 Special Considerations for PCI

Since the coarse decoding is done by the PCI interface module, the host-module decoding section of ATLAS is not used. This means that ATLAS will always be configured the same way:

Register Bits	*VD Bit*	*Inversion*	*Strapping*
config<1>	63	No	PD
config<0>	62	No	PD
mapsel<2>	61	No	PD
mapsel<1>	60	No	PU
mapsel<0>	59	No	PD
driverdy	58	Yes	PD
above1meg	57	Yes	PU
pci	56	Yes	PD
isa	55	No	PD
vgabank0	24	No	PD
vgaen0	5	No	PD

3.6.4 Reset Field Definitions

The reset fields listed in the Table 3-5 are explained in detail below:

Internal These bits are read from VD<4:0> on reset. These lines must present the value 19h during reset.

vgaen<1:0> DST<5>,CONFIG<10> VGA enable. Refer to the CONFIG register description in Chapter 5 for more details.

VGAEN0 and VGAEN1 are used to enable/disable the VGA. Only one bit is used at a time (the other one is tied to GND). The following table shows how the internal bits are initialized at reset:

- When VGAEN0 is used, the 46E8 feature is enabled when the VGA is turned on.
- When VGAENl is used, the 46E8 feature is not enabled with the VGA. VGAEN1 should be used with the PCI interface, since PCI incorporates auto-configuration which may cause problems with the fixed decoding of the 46E8 feature.

VGAEN1	*VGAEN0*	*en46E8*	*CONFIG<10,9>*	
0	0	0	0	0
0	1	1	1	1
1	0	0	1	1

This field is read from VD<37,5>.

Internal This field is read from VD<15:6> on reset. These lines must present the value 027h during reset.

PCB Revision

DST0<19:16> Indicates the revision of the PCB. Refer to the DST1-0 register description in Chapter 5 for more details.

Value	*PCB Revision Level*
1111h	0
1110h	1
:	:

These bits are read from VD<19:16> on reset.

Product ID

DST0<23:20> Indicates the Product ID/Platform. Refer to the DST1-0 register description in Chapter 5 for more details.

Product ID	*Product Platform*
llxx	ISA Bus
101x	VL Bus
100x	MCA Bus
0110	PCI Bus
0111	Reserved (do not use)
0101	To be defined (future platforms)
0000	

These bits are read from VD<23:20> on reset.

vgabank0

OPMODE<ll> VGA Bank 0. Refer to the OPMODE register description in Chapter 5 for more details.

This bit is read from VD<24> on reset, and stored here.

rambank <8:0>

DST1<0>, DST0<31:25> DST1<3> indicates the presence (when '1') of Banks 1-8. Refer to the DST1-0 register description in Chapter 5 for more details.

Value	Bank	Description
xxxxxxxx1	0	8x 128K x 8 VRAM
xxxxxxxlx	1	8x l28K x 8 VRAM
xxxxxxlxx	2	6 or 8 x 256K x 8 VRAM
xxxxxlxxx	3	6 or 8 x 256K x 8 VRAM
xxxxlxxxx	4	6 x 256K x 8 VRAM
xxxlxxxxx	5	4 x 256K x 16 DRAM
xxlxxxxxx	6	Reserved
xlxxxxxxx	7	2 x 128K x 8 DRAM - Patch DRAM
lxxxxxxxx	8	4 x 64K or 256K x 16 DRAM

These bits are read from VD<32:25>, VD<35> on reset.

ramspeed <1:0> DST1<2:1> Indicates the speed of the on-board memory. Refer to the DST 1-O register description in Chapter 5 for more details.
Note: ***All memory must be the same speed.***

Value	*Memory Speed*
11h	-80 (80 nanosecond access time)
Others	Reserved

These bits are read from VD<34:33> on reset.

HiRes/ DST1<4> Indicates that the board is capable of displaying at a resolution of 1600 x 1200. Refer to the DST1-0 register description in Chapter 5 for more details.

Value	*Meaning*
0	Board supports 1600 x 1200
1	Board does not support 1600 x 1200

This bit is read from VD<36> on reset

testwren DST1<6> Must be pulled up. See the TEST register description on page 5-41 for more details. This bit is read from VD<38> on reset.

Reserved These bits, which are read from VD<39> on reset, should be pulled high during reset.

Internal These lines are read from VD<47:40> on reset. They must present the data DFh during reset.

200MHz This bit, which is read from VD<48> on reset, indicates the presence of a 200 MHz RAMDAC. Refer to the CONFIG register description in Chapter 5 for more details.

misc<1> CONFIG<3> Miscellaneous software bit that is currently unused. Refer to the CONFIG register description in Chapter 5 for more details.

This bit is read from VD<49> during reset. Software must read this bit from DST1<17>, invert it, then load the result into CONFIG<3>.

nodubic CONFIG<4> Indicates whether or not a DUBIC chip is present in the system. Refer to the CONFIG register description for more details.

hyperpg OPMODE<25:24> Support for Hyper Page mode. Refer to the OPMODE register description in Chapter 5 for more details.

These bits are read from VD<52:51> during reset. Software must read these bits from DST 1<20:19> and load them here.

expdev CONFIG<16> Expansion device. Refer to the CONFIG register description in Chapter 5 for more details.

Read from VD<53> during reset. Software must read this bit from DST1<21> and load it here.

tram OPMODE<26> Type of VRAM. Refer to the OPMODE register description in Chapter 5 for more details.

Read from VD<54> during reset. Software must read this bit from DST1<22> and load it here.

isa CONFIG<28> ISA bus identification. Refer to the CONFIG register description in Chapter 5 for more details.

Sampled from VD<55> on reset, this bit assumes the external strapping configuration value.

pci CONFIG<27> In conjunction with the isa bit, determines the type of host interface. Refer to the CONFIG register description in Chapter 5 for more details.

The value sampled from VD<56> on reset is inverted and stored in this bit.

above1meg CONFIG<12> Mapped above 1 MB. Refer to the CONFIG register description in Chapter 5 for more details.

The value sampled from VD<57> on reset is inverted and stored in this bit.

driverdy CONFIG<8> Drive channel ready. Refer to the CONFIG register description in Chapter 5 for more details.

The value sampled from VD<58> on reset is inverted and stored here.

mapsel <2:0> CONFIG<26:24> Select base address of MGA board in system. Refer to the CONFIG register description in Chapter 5 for more details.

The value is sampled from VD<61:59> on reset and loaded here.

config CONFIG<1:0> Configuration bits. Refer to the CONFIG register description in Chapter 5 for more details.

This value is sampled from VD<63:62> on reset and loaded here.

Chapter 4: Memory Mapping

This chapter summarizes the memory map for the ATLAS in both the ISA and PCI configurations, and provides an overview of the I/O space mapping for the VGA I.0 and mouse port registers.

4.1 ISA and PCI Configurations

The ATLAS chip supports two bus configurations: ISA (Industry Standard Architecture, often called 'AT-bus') and PCI (Peripheral Component Interconnect). The major differences between the two configurations are that the ATLAS memory mapping is different for each, and the PCI configuration includes space that is reserved for system configuration (the ISA configuration has no configuration space).

4.1.1 Configuration Space Mapping

The configuration space is supported only for PCI devices. When modes other than PCI are selected, this space (and its registers) are invisible and unused. The entire configuration space is decoded by ATLAS.

Offset (1)	*Name*	*Access*	*ResetValue*
00	DEVID	R	0000 0101 0001 1000 0001 0000 0010 1011b
04	DEVCTRL	R/W	0000 0100 0000 0000 0000 0000 1000 0000b
08	CLASS	R	0000 0011 S000 0000 0000 0000 0000 0000b
0C	HEADER	R	0000 0000 0000 0000 0000 0000 0000 0000b
10	TERMBASE	R/W	0000 0000 0000 0000 0000 0000 0000 0000b
30	ROMBASE	R/W	0000 0000 0000 0000 0000 0000 0000 0000b
C3	INTCTRL	R/W	0000 0000 0000 0000 0000 0001 1111 1111b
40	OPTION	R/W	0000 0000 0000 0000 0000 0000 0000 0000b

4.2 Memory Space Mapping

4.2.1 ISA Interface

All extensions to Power Graphic mode are mapped in the memory space, as well as in the VGA frame buffer and in the VGA BIOS.

Address	*Device Decoded*	*Condition (1)*
0A0000h-0BFFFFh	VGA frame buffer	If vgaen is active.
0C0000h-0C7FFFh	VGA BIOS ROM	If biosen is active.
0AC000h-0AFFFFh	MGA Power Graphic Mode	If MAPSEL1 is selected **and** the VGA is **either** disabled **or** VMAPSEL = 1 (2)
0C8000h-0CBFFFh	"	If MAPSEL2 is selected.
0CC000h-0CFFFFh	"	If MAPSEL3 is selected.
0D0000h-0D3FFFh	"	If MAPSEL4 is selected.
0D4000h-0D7FFFh	"	If MAPSEL5 is selected.
0D8000h-0DBFFFh	"	If MAPSEL6 is selected.
0DC000h-0DFFFFh	"	If MAPSEL7 is selected.

Table 4-1: ATLAS Memory Mapping

(1) Refer to the CONFIG register description in Chapter 5 for information on the control bits used to select the map options.

(2) VMAPSEL is located at I/O address 3CF, Index 6, Bit 3.

Refer to Table 4-3 for the Power Graphic Mode memory mapping for both the ISA and PCI interfaces.

4.2.2 PCI Interface

The memory mapping for the PCI configuration is shown below:

Address Offset Range	*Device Decoded*	*Condition*
000A0000h-000BFFFFh	VGA Frame Buffer	If vgaen and memspace are active
nnnn0000h-nnnn7FFFh or nnnn8000h-nnnnFFFFh	VGA BIOS ROM (1)	If biosen and memspace are active
mmmm0000h-mmmm3FFFh or mmmm4000h-mmmm7FFFh or mmmm8000h-mmmmBFFFh or mmmmC000h-mmmmFFFFh	MGA Power Graphic Mode (2)	If memspace is active

Table 4-2: ATLAS PCI Mode Memory Mapping

(1) The exact location in the memory space depends on the ROMBASE register. Because ATLAS is decoded as a VGA device, the ROM should be mapped at 000C0000h by the system BIOS as specified in the ***PCI Bus*** *Specification.*

(2) The exact location in the memory space depends on the TERMBASE register.

4.2.3 Power Graphic Mode Mapping (ISA and PCI)

Address Offset Range	*Condition*	*R/W*	*Mnemonic*	*Device Decoded*	
0000h-1BFFh	VgaEn/ & PseudoDma/	R/W	VRAMWIN	7K VRAM window	
0000h-1BFFh	VgaEn/ & PseudoDma	W	DMAWIN	7K Pseudo-DMA window	(1)
0000h-1BFFh	VgaEn/ & PseudoDma	R	IDUMP	7K Pseudo-DMA window	(1)
1C00h-1FFFh		R/W	INTREG	ATLAS internal registers	(2)
2000h-3BFFh	VgaEn/ & PseudoDma/	R/W	Reserved	7K VRAM window (redundant) Reserved	
3C00h-3C7Fh		R/W	RAMDAC	RAMDAC	(3)
3C80h-3CFFh		R/W	DUBIC	DUBIC	(3)
3D00h-3D7Fh		R/W	VIWIC	VIWIC	(3)
3D80h-3DFFh	ExpDev	W	CLKGEN	EXPSL/	(3)
3D80h-3DFFh	ExpDev	R/W	CLKGEN	EXPSL/	(3)
3E00h-3FFFh	ExpDev	R/W	EXPDEV	EXPSL/	(3)

Table 4-3: ATLAS Power Graphic Mode Memory Mapping

(1) Refer to Section 3.2.4.2, 'Pseudo DMA', for more information.

(2) Refer to the following tables for definitions and specific addresses of the ATLAS internal registers.

(3) In the external device range, all devices are double-word aligned and only accessible on byte 0. Only byte 0 accesses are allowed. Word and double-word accesses will cause unpredictable results.

Offset (1)	*Name*	*Category (2)*	*Access*	*Reset Value*
1C00	DWGCTL	F	W	0000 0000h
1C04	MACCESS	F	W	0000 0000h
1C08	MCTLWTST	F	W	FFFF FFFFh
1C10	DSTI-0	D	R	Loaded from vd<63:0>
1C18	Reserved			
1C1C	PLNWT	F	W	XXXXXXXXh
1 C20	BCOL	F	W	XXXXXXXXh
1C24	FCOL	F	W	XXXXXXXxh
1C30	SRCO-3	FD	W	XXXXXXXXh
1C40	XYSTRT	FKD	W	XXXXXXXXh
1C44	XYEND	FKD	W	XXXX XXXXh
1C50	SHIFT	FKD	W	XXXXXXXXh
1C58	*SGN*	FKD	W	XXXXXXXXh
1C5C	LEN	FKD	W	XXXX XXXXh
1C60	AR0	FKD	W	XXXXXXXXh
1C64	AR1	FKD	W	XXXX XXXXh
1C68	AR2	FKD	W	XXXX XXXXh
1C6C	AR3	FKD	W	XXXX XXXXh
1C70	AR4	FKD	W	XXXX XXXXh
1C74	AR5	FKD	W	XXXXXXXxh
1C78	AR6	FKD	W	XXXXXXXXh
1C8C	PITCH	FK	W	XXXXXXXXh
1C90	YDST	FKD	W	(7)
1C94	YDSTORG	FK	W	XXXXXXXXh
1C98	YTOP	FK	W	XXXXXXXXh
1C9C	YBOT	FK	W	XXXX XXXXh
1CA0	CXLEFT	FK	W	XXXXXXXXh
1CA4	CXRIGHT	FK	W	XXXXXXXXh
1 CA8	FXLEFT	FKD	W	XXXX XXXXh
1CAC	FXRIGHT	FKD	W	XXXXXXXXh
1CB0	XDST	FKD	W	XXXXXXXXh
1D00-1DFC	Same register mapping as 000-0FFC range (3)			
1E00	VRAMPAGE	–	R/W	XXXXXXXXh
1E08	BYTACCDATA		R	XXXX XXXXh
1E0C	ADRGEN		R	XXXXXXXxh
1E10	FIFOSTATUS	–	R	21XX 0220h
1E14	STATUS	–	R	0000 000Xh
1E18	ICLEAR		W	0000 0000h
1E1C	IEN		R/W	0000 0000h
1E28	INTSTS (10)		R/W	
1E40	RST		R/W	0000 0000h
1E44	TEST		R/W	(7)
1E48	REV		R	A268 1700h
1E50	ZONFIG		R/W	(7)
1E54	OPMODE		R/W	(7)
1E5C	CRTC CTRL		R/W	0000 0000h

Offset (I)	*Name*	*Cat.(2)*	*Access*	*Her-ules*	*CGA*	*EGA*	*VGA*
1FB0	(8)	V	R/W	√		√	
1FB1	(9)	V	R/W	√		√	
1FB2	(8)	V	R/W	√		√	
1FB3	(9)	V	R/W	√		√	
1FB4	CRTC-ADDR (5)	V	R/W	√		√	√
1FB5	CRTC-DATA (5)	V	R/W	√		√	√
1FB6	(8)	V	R/W	√		√	
1FB7	(9)	V	R/W	√		√	
1FB8	HER-MODE	V	R/W	√			
1FB9	HER_LP_SET	V	R/W	√			
1FBA	MISC_ISTAT1(5)	V	R	√		√	√
	FEAT_CTL	V	W			√	√
1FBB	HER_LP_CLR	V	R/W	√			
1FBF	HER_CONF	V	R/W	√			
1FC0	ATTR_ADDR (4)	V	R/W			√	√
1FC1	Am-DATA	V	R			√	√
1FC2	MISC_ISTAT0	V	R			√	√
	MISC-OUT	V	W			√	√
1FC3	MISC_ISTAT0	V	R/W			√	
	MISC_OUT	V	W			√	
1FC4	SEQ_ADDR	V	R/W			√	√
1FC5	SEQ_DATA	V	R/W			√	√
1FC7	DACSTATUS	V	R				√
1FCA	FEAT_CTL	V	R			√	√
1FCC	MISC_OUT	V	R				√
1FCE	GCTL_ADDR	V	R/W			√	√
1FCF	GCTL_DATA	V	R/W			√	√
1FD0	(8)	V	R/W		√	√	
1FD1	(9)	V	R/W		√	√	
1FD2	(8)	V	R/W		√	√	
1FD3	(9)	V	R/W		√	√	
1FD4	CRTC-ADDR (5)	V	R/W		√	√	√
1FD5	CRTC-DATA (5)	V	R/W		√	√	√
1FD6	(8)	V	R/W		√	√	
1FD7	(9)	V	R/W		√	√	
1FD8	CGA-MODE	V	R/W		√		
1FD9	CGA_COL_SL	V	R/W		√		
1FDA	MISC_ISTAT1 (5)	V	R		√	√	√
	FEAT_CTL	V	W			√	√
1FDB	CGA-LPCLR	V	R/W		√	√	√
1FDC	CGA_LP_SET	V	R/W		√	√	√
1FDE	AUX_ADDR	V	R/W	√	√	√	√
1FDF	AUX_DATA	V	R/W	√	√	√	√

Table 4-4: ATLAS Register Mapping

Notes:

Any location within the 1C00h – 1FFFh offset range that is not identified in Table 4-4 should be considered as reserved.

(1) The address offsets provided are relative to the MGA Power Graphic mode base memory address, as shown in Table 4-1.

(2) The ***Category*** refers to the special characteristics of each register. The following categories are defined:

- D — This register is a drawing engine dynamic register. This means that the contents of the register may be modified by a drawing cycle. You must wait until the drawing engine is idle before you can read dynamic registers.
- F — The data for this register is passed through the Command FIFO. The Command FIFO contents are sent to the drawing engine only when it is ready to use them. This is the method used to synchronize the software with the drawing engine (no access to drawing engine registers should be attempted when the FIFO is full). This means that it is guaranteed that a register will be written only when the FIFO is empty. A register should only be read when the FIFO is empty, in order to be sure that the contents of that register are stable.
- K — These registers can be initialized when the memory sequencer is not idle. It is then preferable to initialize them first (when required) in order to achieve higher performance.
- V — These BYTE registers are in the VGA module. They are accessed in the same way as the VGA I/O port, except that they are memory mapped.

(3) When a register is accessed in this range, this indicates to the drawing engine to start a drawing cycle.

(4) A read from port 1FBA/1FDAh resets this port to the Attributes Address register. The first read or write to this register after a 1FBA/1FDAh reset accesses the attributes index, and the next read or write accesses the palette. Subsequent reads or writes to this register toggle between index and palette.

(5) D0=0 of the MISC_OUT register sets the CRTC registers to 1FBXh and the input status 1 to 1FBA. D0=1 of the MISC_OUT register sets the CRTC registers to 1FDXh and the input status 1 to 1FDAh.

(6) See the VGA_SUBSYS register description for more information.

(7) ***Reset*** Values. The following table lists register reset values that were too wide for the previous tables:

Byte Offset (1)	*Name*	*Reset Value*
1C90	YDST	XXXX XXX0 XXXX XXXX XXXX XXXX XXXX XXXX b
1E44	TEST	0000 0000 0000 0000 0000 00H0 0000 0000 b
1E50	CONFIG	000H HHHH 0000 0000 000H 0HHH 0000 00HH b
1E54	OPMODE	0000 0000 0000 0000 0000 H000 0000 0000 b

Legend:
X = Undefined
H = Sampled on hard reset

(8) Alternate addresses of 1FB4h./1FD4h.

(9) Alternate addresses of 1FB5/1FD5h.

(10) This register only exists in the PCI configuration.

4.3 I/O Mapping

Two different devices are mapped in the I/O space: the VGA I/O registers, and the mouse port. The I/O mapping remains the same for both the ISA and PCI configuration.

			Decoded as:			
Port	***Name***	***Access***	***Hercules***	***CGA***	***EGA***	***VGA***
238h	Mouse data register (6)	R				
23Ah	Mouse control register (6)	R/W				
23Bh	Mouse configuration register (no write effect) (6)	W				
23Ch	Mouse data register (6)	R				
23Eh	Mouse control register (6)	R/W				
23Fh	Mouse configuration register (no write effect) (6)	W				
3B0h	(3)	R/W	√		√	
3B1h	(4)	R/W	√		√	
3B2h	(3)	R/W	√		√	
3B3h	(4)	R/W	√		√	
3B4h	CRTC_ADDR (2)	R/W	√		√	√
3B5h	CRTC_DATA (2)	R/W	√		√	√
3B6h	(3)	R/W	√		√	
3B7h	(4)	R/W	√		√	
3B8h	HER_MODE	R/W	√			
3B9h	HER_LP_SET	R/W	√			
3BAh	MISC_ISTAT1 (2)	R	√		√	√
	FEAT_CTL	W			√	√
3BBh	HER_LP_CLR	R/W	√			
3BCh	Reserved	R/W				
3BDh	Reserved	R/W				
3BEh	Reserved	R/W				
3BFh	HER_CONF	R/W	√			
3C0h	ATTR_ADDR (1)	R/W			√	√
3C1h	ATTR_DATA	R			√	√
3C2h	MISC_ISTAT0	R			√	√
	MISC_OUT	W			√	√
3C3h	MISC_ISTAT0	R			√	
	MISC_OUT	W			√	
3C4h	SEQ_ADDR	R/W			√	√
3C5h	SEQ_DATA	R/W			√	√
3C6h	Pixel Mask Register (7)	R/W				√
3C7h	Pixel Read Address Register (7)	W				√
	DAC_STATUS	R				√
3C8h	Palette Write Address Register (7)	R/W				√
3C9h	16/8-bit Color Palette Data (7)	R/W				√
3CAh	FEAT_CTL	R			√	√
3CBh	Reserved	W	√	√	√	√
3CCh	MISC_OUT	R				√
3CDh	Reserved	W	√	√	√	√
3CEh	GCTL_ ADDR	R/W			√	√
3CFh	GCTL_ DATA	R/W			√	√

Port	Name	Access	Decoded as:			
			Hercules	CGA	EGA	VGA
3D0h	(3)	R/W		√	√	
3D1h	(4)	R/W		√	√	
3D2h	(3)	R/W		√	√	
3D3h	(4)	R/W		√	√	
3D4h	CRTC_ADDR (2)	R/W		√	√	√
3D5h	CRTC_DATA (2)	R/W		√	√	√
3D6h	(3)	R/W		√	√	
3D7h	(4)	R/W		√	√	
3D8h	CGA_MODE	R/W		√		
3D9h	CGA_COL_SL	R/W		√		
3DAh	MISC_ISTAT1 (2)	R		√	√	√
	FEAT_CTL	W			√	√
3DBh	CGA_LP_CLR	R/W		√	√	√
3DCh	CGA_LP_SET	R/W		√	√	√
3DDh	Reserved	R/W				
3DEh	AUX_ADDR	R/W	√	√	√	√
3DFh	AUX_DATA	R/W	√	√	√	√
3B0 to 3DF	EXPSL/ (8)	R/W	√	√	√	√
46E8h	Video Subsystem Access/Setup Enable (5)	W	√	√	√	√
102h	Video Subsystem Enable (5)	W	√	√	√	√

Table 4-5: I/O Mapping

(1) A read from Port 3BA/3DAh resets this port to the attributes address register. The first read/write to this register after a 3BA/3DAh reset accesses the attributes index, and the next read/write accesses the palette. Subsequent reads or writes to this register toggle between index and palette.

(2) D0=0 of the miscellaneous output register sets the CRTC registers to 3BXh and the input status 1 to 3BA.
D0=1 of the miscellaneous output register sets the CRTC registers to 3DXh and the input status 1 to 3DA.

(3) Alternate addresses of 3B4/3D4h.

(4) Alternate addresses of 3B5/3D5h.

(5) In the PCI configuration, these locations are only decoded for write operations. Snooping is always enabled. These locations are decoded only when the 'VGAEN0' bit is sampled active on reset, otherwise, they are not decoded.

(6) For more details refer to the OPMODE register description for bits 8 and 9 contained in Chapter 5. Refer to the *MGA DUBIC Specification* for more information about these registers.

(7) In the PCI configuration, snooping is enabled on these locations if 'vgasnoop' is active. Otherwise, normal access is performed.

(8) In the PCI configuration, external expansion space is never enabled during an I/O cycle.

❖ :* Note that the 3B0-3C5 and 3CA–3DF ranges are always decoded when VGA is enabled, even when there is no register located at a specific address.

Chapter 5: Register Descriptions

This chapter contains a description of each of the Power Graphic and VGA mode registers of the ATLAS chip, listed in address order for each mode.

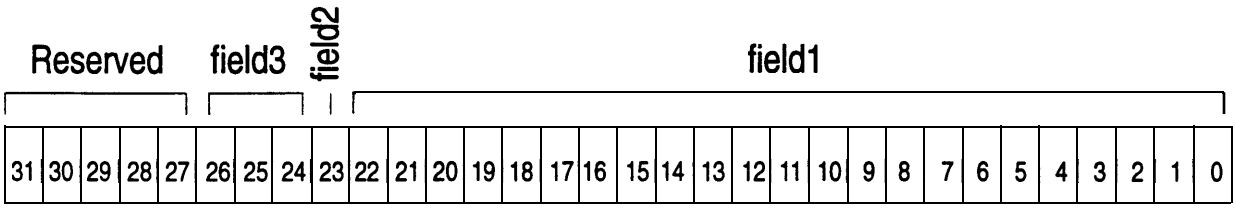
Note that Tables 4-4 and 4-5 list all of the registers in address order. In addition, lists of all registers (and the Power Graphic mode register fields) are presented in alphabetical order at the back of this manual.

5.1 Register Descriptions

5.1 .1 Power Graphics Mode Registers

Sample Power Graphic Mode Register Description **SAMPLE-PG**

Memory Address <address> **Attributes** W-F **Reset Value <value>**



field1 <22:0> FIELD1. Detailed description of the <field1> field, which comprises bits 22 to 0.

field2 <23> FIELD2. Detailed description of the <field2> field, which is bit 23.

field3 <26:24> FIELD3. Detailed description of the **<field3>** field, which comprises bits 26 to 24.

Reserved <31:27> Reserved: Writing has no effect.

Power Graphic Mode register descriptions contain a (double-underlined) header which indicates the register's mnemonic abbreviation and its full name. Below the header, the memory address (1C00 for example), attributes, and reset value for the register are provided. Next, an illustration of the register identifies the locations of all the bits, which are then described in detail below the illustration.

Memory Address

The addresses of all the Power Graphic mode registers are provided in Chapter 4.

Attributes

The Power Graphic mode attributes are:

R: Read Only

W: Write Only

R/W: Read and Write

D: Dynamic. The contents of the register may be modified by a drawing cycle. Before such registers can be read, the drawing engine must be idle.

F: FIFO. Data for this type of register is passed through the Command FIFO. The contents of the Command FIFO are used by the drawing engine only when the drawing engine is ready to access them. This is the method used to synchronize the software with the drawing engine **(no access to the drawing engine registers should be attempted when the FIFO is full).** This also means that a register is guaranteed to be written only when the FIFO is empty. The drawing engine registers should only be read when the FIFO is empty to make sure that the contents of the register are stable.

K: These registers can be initialized when the memory sequencer isn't idle, so it's preferable to initialize them first (when required) to achieve higher performance.

Reset Value

The reset values for the Power Graphic mode registers can be expressed as hexadecimal or binary values. Most bits are reset on both soft and hard reset. Some bits are reset on hard reset only (those bits are underlined when they appear in the register description header next to **Reset Value).**

- 000X 0000h (h = Hexadecimal)
- 0000 0000 0X00 00H0 0000 0000 0000 0000b (b = Binary)

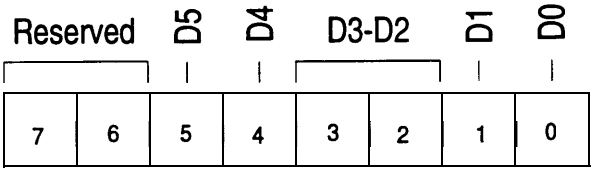
Legend:

X= Undefined
H = Sampled on hard reset

5.1.2 VGA Mode Registers

Sample VGA Mode Register Description **SAMPLE_VGA**

Memory Address <addr> **I/O Address** <addr> **Index** <index>



DO A detailed description of the function of data bit 0.

D1 A detailed description of the function of data bit 1.

D3-D2 A detailed description of the function of the data field which contains bits 2 and 3, etc.

ATLAS VGA Mode register descriptions contain a (single-underlined) header which indicates the register's name and type (such as CRT Controller or Sequencer, etc.). Below the header, the memory address (1 COO for example), I/O address, and the offset index for the register are indicated. Next, an illustration of the register identifies the locations of all the bits, which are then described in detail below the illustration.

Memory Address

This address is an offset from the Power Graphic mode base memory address. The memory addresses can be read, write, color, or monochrome, as indicated. Note that some of the VGA mode registers have no memory address and some have no index.

I/O Address

These addresses are I/O ports. The I/O addresses can be read, write, color, or monochrome, as indicated.

Index

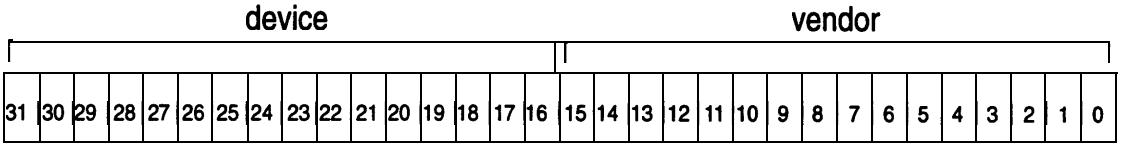
This is the indexed address of the specific register.

5.2 Power Graphic Mode Register Descriptions

DEVID — Device ID

Configuration Space Address 00 **Attributes** R

Reset Value 0000 0101 0001 1000 0001 0000 0010 1011lb



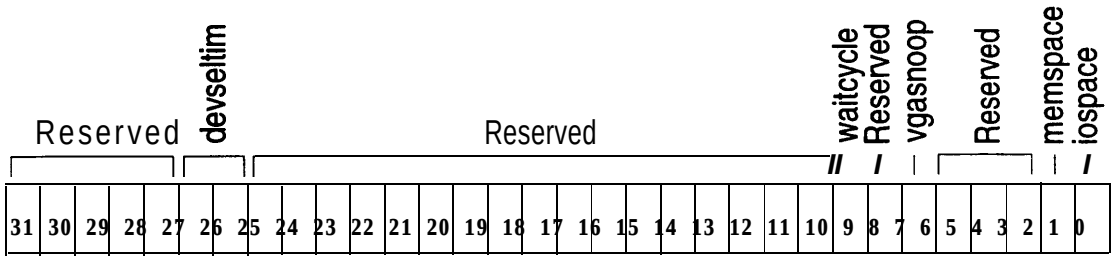
device <31:16> DEVICE identifiers. The data is the 5-bit ASCII code for the first three characters of the string: "ATLAS".

0518

vendor <15:0> The Matrox VENDOR identifier for PCI: 0x102B.

Configuration Space Address 04 **Attributes** R/W

Reset Value 0000 0100 0000 0000 0000 0000 1000 **0000b**



Reserved <31:27> Reserved: This field is always read as 0.

devseltim R <26:25> DEVice SELect TIMing. Specifies the timing of devsel. It is read as 01.

Reserved <24:8> Reserved: This field is always read as 0.

waitcycle R <7> WAIT CYCLE: Specifies that ATLAS will perform continuous address/data stepping. This bit is always read as 1.

Reserved <6> Reserved: This field is always read as 0.

vgasnoop R/W <5> VGA SNOOPing. Controls how ATLAS will handle access to the PCI system palette register (as described in Section 3.10 of the *PCZ Local Bus Specification*, Revision 2.0).

. 0: Respond to a palette access.

. 1: Enable special snooping behavior.

Reserved <4:2> Reserved: This field is always read as 0.

memspace R/W <1> Device response to MEMory SPACE access. This bit controls all memory spaces (EPROM, VGA frame buffer, and Power Graphic mode memory space).

- 0: Disable the device response
- 1: Enable the device response

iospace R/W<0> Device response to I/O SPACE access. This bit controls all I/O space (VGA I/O, and Mouse port).

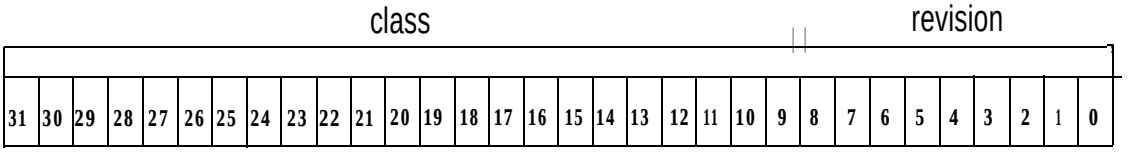
. 0: Disable the device response

. 1: Enable the device response

CLASS — Class Code

Configuration Space Address 08 **Attributes** R

Reset Value 0000 0011 S000 0000 0000 0000 0000 0000b



class<31:9> Device CLASS. Identifies the generic function of the device and a specific register-level programming interface according to the PCI specification. Two values can be read in this field according to the value of the CONFIG register's vgaen field in the host interface:

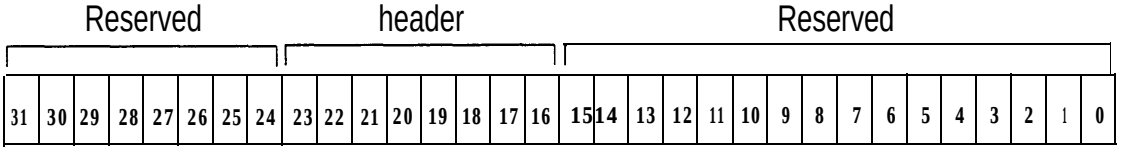
vgaen	*Value*	*Meaning*
0	038000h	Other display controller
1	030000h	Super VGA-compatible controller

revision <8:0> REVISION. Contains the current board revision. This value is always read as 0.

HEADER — Header

Configuration Space Address 0C **Attributes** R

Reset Value 0000 0000 0000 0000 0000 0000b



Reserved <31:24> Reserved: This field is always read as 00h.

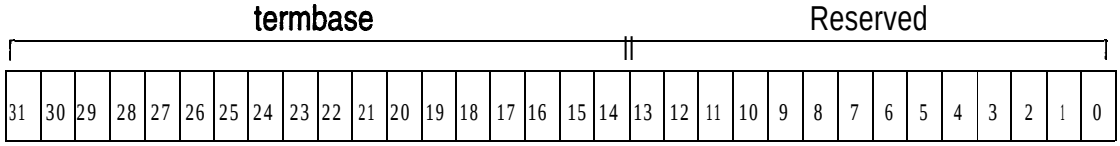
header <23:16> HEADER layout. Specifies the layout of bytes 10h through 3Fh in the configuration space. Also specifies that the current device is a single function device. This field is always read as 00h.

Reserved <15:0> Reserved: This field is always read as 0000h.

Terminator Base Address — TERMBASE

Configuration Space Address 10 **Attributes** R/W

Reset Value 0000 0000 0000 0000 0000 0000 0000 0000b



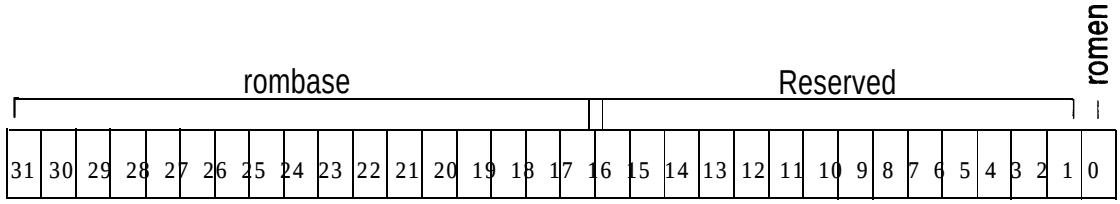
termbase <31:14> TERMinator (Power Graphic) BASE Address. Specifies the base address of the Power Graphic mode memory space. Mapping in this 16KB space is decoded by ATLAS itself. Refer to Chapter 4 for more information.

Reserved <13:0> Reserved: This field is always read as 0.

ROM Base Address — ROMBASE

Configuration Space Address 30 **Attributes** R/W

Reset Value 0000 0000 0000 0000 0000 0000 0000 0000b



rombase <31:15> EPROM BASE address. Specifies the base address of the EPROM. This field's attribute changes, depending on the value of the CONFIG register's biosen field:

biosen	*ROMBASE Attribute*
0	RO. Read as 0
1	R/W

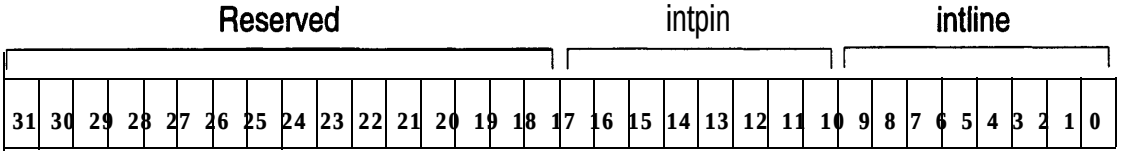
Reserved <14:1> Reserved: This field is always read as 0000h.

romen<0> ROM ENable. Enable the ROM. This field's attribute changes, depending on the value of the CONFIG register's biosen field:

biosen	*ROMEN Attribute*
0	RO. Read as 0
1	R/W

Configuration Space Address 3C **Attributes R/W**

Reset Value 0000 0000 0000 0000 0000 0001 1111 1111b



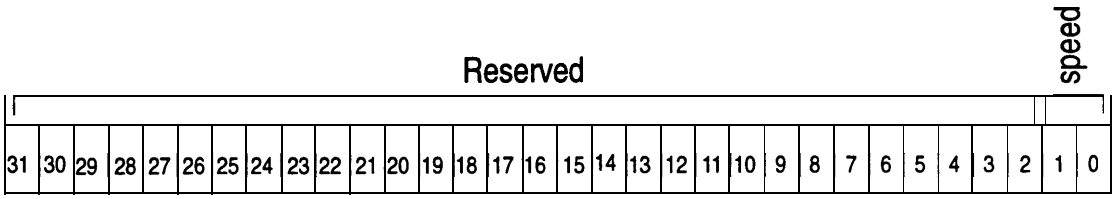
Reserved <31:16> Reserved: This field is always read as **0000h.**

intpin R <15:8> Selected **INTerrupt** PINs. This field is always read as 1h, since INTA is used as the interrupt pin.

intline R/W <7:0> **INTerrupt** LINE routing. This R/W field is used to communicate interrupt line routing information. It is initialized at power-up to identify for the device drivers which device interrrupt pin has been connected to which system interrupt controller pin. The value FFh is defined as 'unknown' or 'no connection' to the interrupt controller.

Configuration Space Address 40 **Attributes R/W**

Reset Value 0000 0000 *0000 0000* 0000 0000 **0000 0000b**

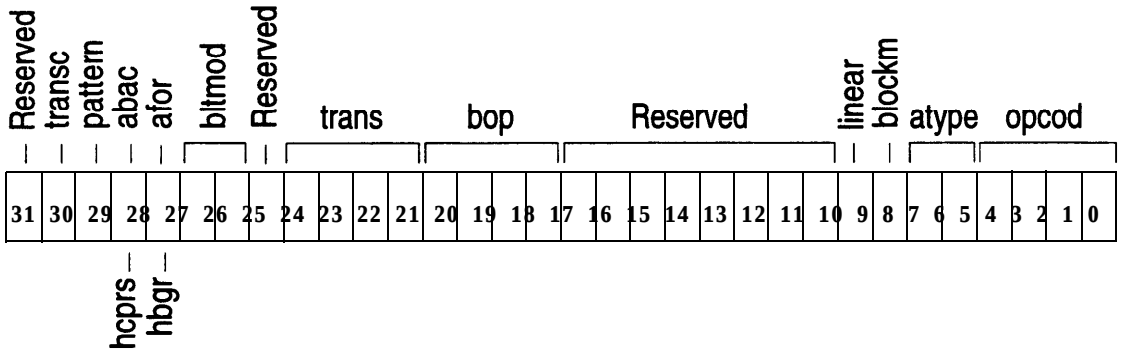


Reserved <31:2> Reserved: This field is always read as 0000h.

speed<1:0> SPEED. This field is used to select the sequence access on the TAD bus, depending on the current PCI bus speed. This field only affects the 0000-1FAF and 1FE0-3FFF ranges in the 16K window.

speed<1:0>	*PCLK*	*GCLK Max. (ns)*	*GCLK Min. (MHz)*
00	30 ns / 33 MHz	28.2	35.5
	40 ns / 25 MHz	40.7	24.6
01	30 ns / 33 MHz	22.3	44.9
	40 ns / 25 MHz	29.3	34.2
10	Reserved		
11	Reserved		

Memory Address lC00 **Attributes** W-F **Reset Value** 0000 0000 h



opcod <3:0> Operation CODe: The opcod field defines the operation selected by the drawing engine, and also affects the operation of the VRAM interface section.

		opcod	
Function	***Subfunction***	***Value***	***Mnemonic***
Line		0000	LINE_OPEN
	AUTO	0001	AUTOLINE_OPEN
	WRITE LAST	0010	LINE_CLOSE
	AUTO, WRITE LAST	0011	AUTOLINE_CLOSE
Trapeziod		0100	TRAP
Bitblit	VRAM -> VRAM	1000	BITBLT
	HOST -> VRAM	1001	ILOAD
	VRAM -> HOST	1010	IDUMP

All other opcodes are reserved and should not be used.

atype **<5:4>** Access TYPE: The atype field is used to define the type of access to the VRAM that is performed.

atype		
Value	***Mnemonic***	***VRAM Access***
00	RPL	Write (replace)
01	RSTR	Read modify write (raster)
10	ANTI	Anti-aliased
11	–	Reserved

blockm <6> BLOCK Mode: Specifies whether or not the destination will be written in block mode.

- 0 Normal write access
- 1 Block mode write selected

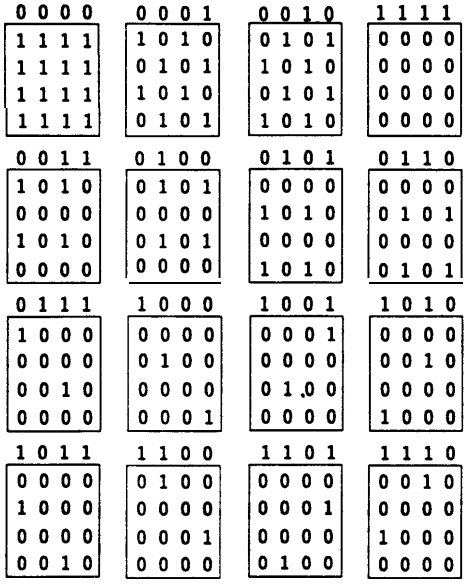
linear <7> LINEAR mode: Specifies if the BITBLIT source is linear or XY.

- 0 XY bitblit
- 1 Linear bitblit

bop <19:16> Boolean OPeration between a source and a destination. The table below shows the various functions performed by the Boolean ALU in 1, 8, 16, and 32 bits/pixel modes. During block mode operations, bop must be set to 1100 (Ch).

bop	*Function*
0000	0
0001	~(D | S)
0010	D & ~S
0011	~S
0100	(~D) & S
0101	~D
0110	D ^ S
0111	~(D & S)
1000	D & S
1001	~(D ^ S)
1010	D
1011	D | ~S
1100	S
1101	(~D) | S
1110	D | S
1111	1

trans <23:20> TRANSlucidity: Specifies the percentage of opacity of the object. The opacity is realized by writing one over 'n' pixels. The trans field specifies the following transparency patterns (where 1 is opaque and 0 is transparent):



bltmod <26:25> BLiT MODe selection: This field must be valid for BLITs without anti-aliasing:

bltmod		
Value	*Mnemonic*	*Usage*
00	BMONO	Source operand is monochrome in 1 bits/pixel.
01	BPLAN	Source operand is monochrome from one plane.
10	BFCOL	Source operand is color. Source is formatted when it comes from the host. Fast clipping can be used during VRAM to VRAM BLITs.
11	BUCOL	Source operand is color. Source is in 32 bits/pixel when it comes from the host. Fast clipping can't be used during VRAM to VRAM BLITs.

This field must contain the value BFCOL in order to handle the line style properly for line drawing using line style.

afor <27> Anti-aliasing FOReground color selected: This field is shared with the hgbr field. It must be '1' when anti-aliasing is selected.

hbgr <27> Host data in BGR format: This field is shared with the afor field.

For ILOAD when bltmod = BUCOL

- 0 Source data is in BGR format
- 1 Source data is in RGB format

For ILOAD when bltmod = BMONO

- 0 Source data is in endian format
- 1 Source data is in Windows format

abac <28>

Anti-aliasing BACkground color selected: This field is shared with the hcprs field. It must be valid when anti-aliasing is selected. This bit performs the second color selection for the anti-aliasing.

- 0 Current pixel is selected
- 1 BACKCOL<23:0> is selected

hcprs <28>

Host data is ComPReSsed: This field is shared with the abac field. It must be valid for color BLITs when the source data comes from the host and the data is in 24-bit true color format.

- 0 Source data is 32 bit/pixel
- 1 Source data is 24 bit/pixel

pattern <29>

PATTERNing enable: This bit specifies whether patterning is enabled when performing BLIT operations.

- 0 Patterning is disabled
- 1 Patterning is enabled

This bit also specifies whether the two banks are to be cleared in parallel when block mode is enabled when fbm = 1XX. Note that when the two banks are cleared in parallel, the fringes aren't processed correctly, and so must be processed separately.

- 0 One bank only
- 1 Two banks in parallel

transc <30>

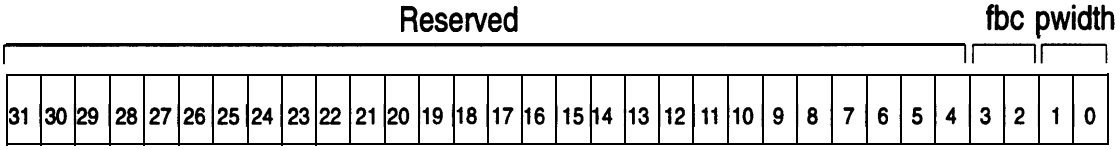
TRANSparency Color enabled: This field must be valid for BLITs with color expansion. This bit specifies whether the background color is written.

- 0 Background color is opaque
- 1 Background color is transparent

Reserved <31,24,15:8>

Reserved: Writing has no effect.

Memory Address 1C04 **Attributes** W- F **Reset Value** 0000 0000 h



pwidth <1:0> Pixel WIDTH: Specifies the pixel width for drawing.

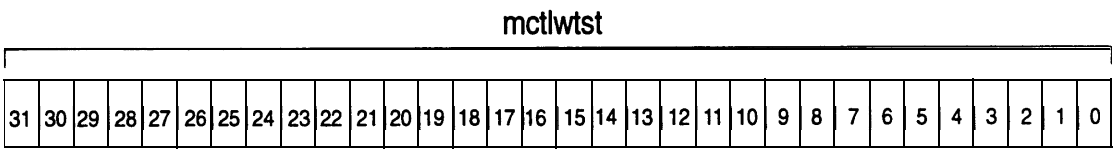
pwidth		
Value	*Mnemonic*	*Mode*
00	PW8	8 bits/pixel
01	PW16	16 bits/pixel
10	PW32	32 bits/pixel
11	—	Reserved

fbc **<3:2>** Frame Buffer Configuration: Specifies if the double buffer is used when drawing.

fbc		
Value	*Mnemonic*	*Mode*
00	SBUF	Full pixel width
01	—	Reserved
10	DBUFA	Buffer A
11	DBUFB	Buffer B

Reserved <31:4> Reserved: Writing has no effect.

Memory Address 1C08 **Attributes** W- F **Reset Value FFFF FFFF** h



mctlwtst <31:0>

Memory ConTroL WaiT STate register: Specifies the number of wait states added to the memory sequencer. For each part of the memory cycle, a different 2-bit subfield is used. The contents of this register depend on of the type and speed of the RAM, and on the board configuration. Each subfield is defined as follows:

mctlwtst<x+1:x>
00 1 gclk
01 2 gclks
10 3 gclks
11 4 gclks

Description	*Mnemonic*	*Register Field*
DEFAULT	DFLT	mctlwtst<1:0>
RAS SETUP	R_SU	mctlwtst<3:2>
RAS HOLD	R_HD	mctlwtst<5:4>
CAS SETUP	C_SU	mctlwtst<7:6>
HOST DELAY	HOST_D	mctlwtst<9:8>
CAS HOLD	C_HD	mctlwtst<11:10>
READ CAS HOLD	RC_HD	mctlwtst<13:12>
HYPER READ CAS HOLD	HRC_HD	mctlwtst<15:14>
Reserved (00)		mctlwtst<17:16>
RAS PRECHARGE	R_PR	mctlwtst<19:18>
Reserved (00)		mctlwtst<21:20>
HYPER READ RAS PRECHARGE	HRR_PR	mctlwtst<23:22>
Reserved (00)		mctlwtst<25:24>
SWITCH BUS	SWT_B	mctlwtst<27:26>
WAIT	W_	mctlwtst<29:28>
LAST PIXEL	L_P	mctlwtst<31:30>

Programming mctlwtst (80 ns VRAMs):

1. C4001010h

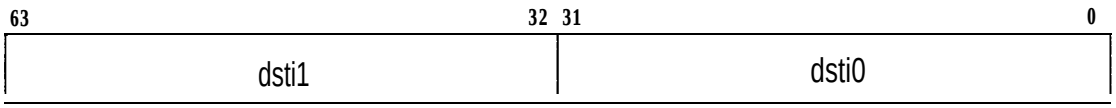
2. C4001110h (one more gclk for BUCOL ILOAD access)

C4001010h is the default value to use, except for BUCOL ILOADs. In the latter case, mctlwtst is programmed to C4001110h prior to the BUCOL ILOAD execution. It's put back to C4001010h when the BUCOL ILOAD execution has finished.

DST1-0 Destination in

Memory Address 1C10 **Attributes** R- D

Reset Value Loaded from vd<63:0>



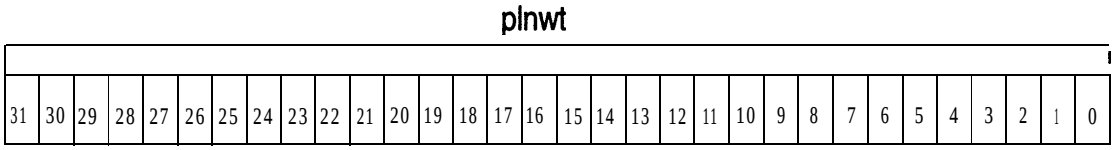
dsti0 <31:0>
dsti1 <63:32>

DeSTination In register: The dsti0 and dsti1 fields are used to load configuration data on reset. The destination registers are normally used by the drawing engine. They are readable, however, since their values are initialized from the data bus on reset (breset). Note that the registers must be read before any direct access to the frame buffer or drawing engine operation is performed in order to obtain valid data.

For more information on the definition of each bit on power up, refer to Section 3.6, 'Power Up and Reset'.

Plane write mask — PLNWT

Memory Address 1C1C **Attributes** W-F **Reset Value** XXXX XXXX h



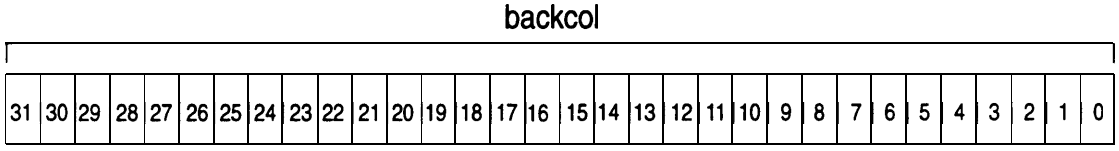
plnwrmsk <31:0> PLaNe WRite MaSK: Specifies the plane or planes to be protected during any write operations. During intensity buffer write operations, the contents of this register are transmitted to the VRAMs through the vd<63:0> bus where they are latched on the falling edge of RAW.

- 0 = Inhibit write
- 1 = Permit write

In 8 and 16 bits/pixel modes, some bits have to be replicated. Refer to Figure 3-9 for the definition of the slice for each mode.

Backsround Color — BCOL

Memory Address 1C20 **Attributes** W-F **Reset Value** XXXX XXXX h



backcol <31:0> BACKground COLor: The backcol field is used by the color expansion module to generate the source pixels when the background is selected. As well, the backcol field is used as the background color for anti-aliased characters.

In 8 and 16 bits/pixel modes, some bits have to be replicated. Refer to Figure 3-9 for the definition of the slice for each mode and to Figure 3-10 for the pixel data organization for each mode.

FCOL — Foreground color

Memory Address 1C24 **Attributes** W-F **Reset Value** XXXX XXXX h

forcol

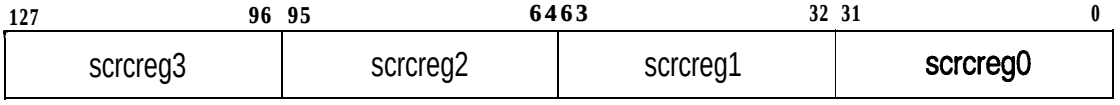
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
forcol																															

forcol <31:0>

FOReground COLor: The forcol field is used by the color expansion module to generate the source pixels when the foreground is selected. As well, forcol is used as foreground color for anti-aliased characters.

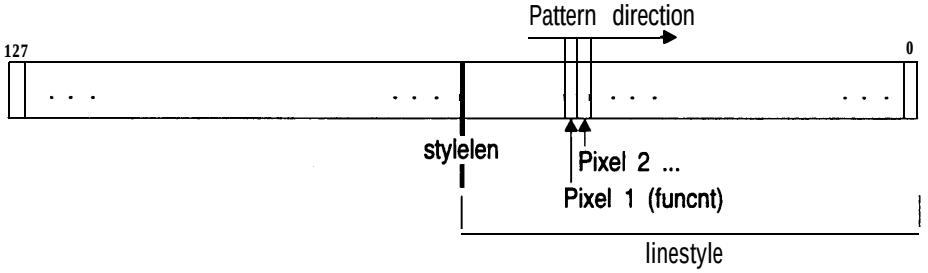
In 8 and 16 bits/pixel modes some bits have to be replicated. Refer to Figure 3-9 for the definition of the slice for each mode and to Figure 3-10 for the pixel data organization for each mode.

Source register	SRC0, SRC1, SRC2, SRC3
Memory Address 1C30 1C34 1C38 1C3C	Attributes W-FD
Reset Value XXXX XXXX h	

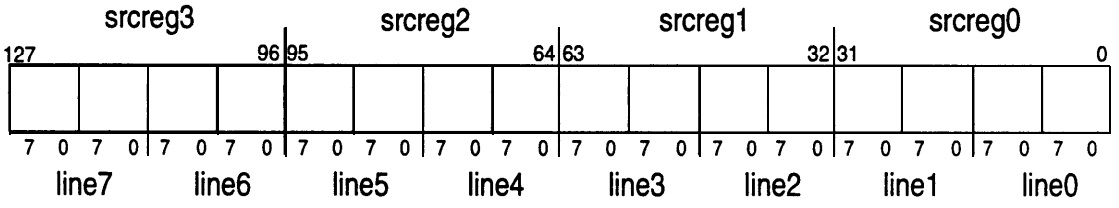


srcreg<127:0> SouRCe REGister: The Source register is used for all drawing operations.

- For LINE with the RPL or RSTR attribute, the source register is used to store the line style. The funcnt field of the SHIFT register points to the selected source register bit which is being used as the linestyle for the current pixel. The following illustration shows how the linestyle is stored in the source register.

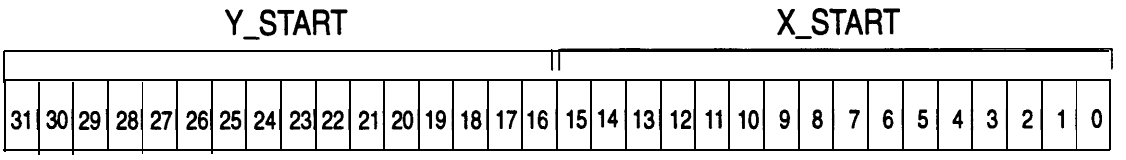


- For TRAP with the RPL or RSTR attribute, the source register is used to store the pattern. The following format is used:



- The source register is used internally for intermediate data for all BITBLT operations.

Memory Address 1C40 **Attributes W-FKD** **Reset Value XXXX XXXX h**



The XYSTRT register is not a physical register. It is simply an alternative way to load registers **AR5,** AR6, XDST and YDST. This register is not readable.

The XYSTRT register is only used for LINE and AUTOLINE. XYSTRT does not require initialization for polylines because all the registers affected by XYSTRT are updated to the endpoint of the vector at the end of the AUTOLINE.

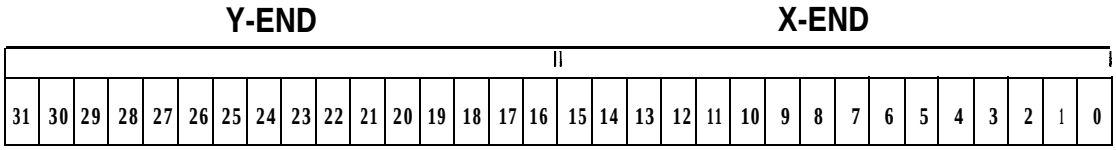
When XYSTRT is written, the following registers are affected:

- X_START<15:0> --> xdst<15:0>
- X_START<15:0> **--> ar5<17:0>** (sign extended)
- Y_START<15:0> **-->** ydstc<23:0> (sign extended)
- 0 **--> sellin**
- 1 **-->** newy
- Y_START<15:0> **-->** ar6<17:0> (sign extended)

x-start <15:0> X **STARTing** coordinate: x-start contains the starting X coordinate of the starting point of the vector. It is a 16-bit signed value in two's complement notation.

y-start **<31:16>** Y **STARTing** coordinate: y-start contains the starting Y coordinate of the starting point of the vector. This coordinate is always XY (this means that to use the XYSTRT register the linearizer must be used). It is a M-bit signed value in two's complement notation.

Memory Address 1C44 Attributes W-FKD Reset Value XXXX XXXX h



The XYEND register is not a physical register. It is just an alternative way to load registers AR0 and AR2.

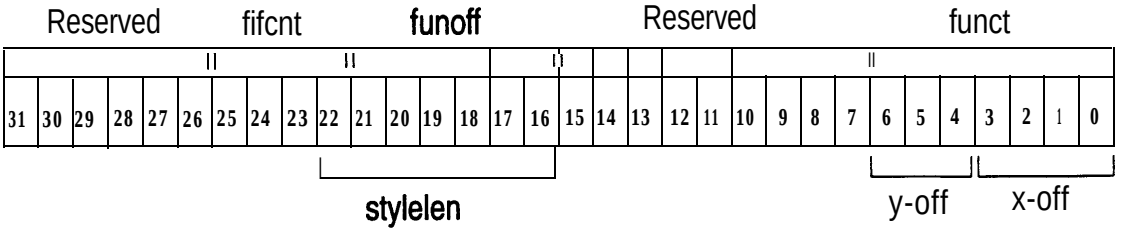
XYEND register is only used for AUTOLINE drawing.When XYEND is written, the following registers are affected:

- X_END<15:0> --> ar0<17:0> (sign extended)
- Y_END<15:0> --> ar2<17:0> (sign extended)

x_end <15:0> X ENDing coordinate: x-end contains the X coordinate of the end point of the vector. It is a 16-bit signed value in two's complement notation.

y_end <31:16> Y ENDing coordinate: y-end contains the Y coordinate of the end point of the vector. It is a 16-bit signed value in two's complement notation.

Memory Address 1C50 **Attributes** W-FKD **Reset Value** XXXX XXXX h



funcnt <6:0> FUNnel COUNT value: This field is used to drive the funnel shifter bit selection.

- For LINE operations, this is a countdown register. This register is used to initialize and select the first bit of the line style.
- For BLIT operations, this register is incremented by the slice value to select source bits.

x_off <3:0> pattern X OFFset: This field is used for TRAP operations to specify the X offset in the pattern. This offset must be in the range O-7 (bit 3 is always 0).

y_off <6:4> pattern Y OFFset: This field is used for TRAP operations to specify the Y offset in the pattern.

Reserved <15:7> Reserved: Writing has no effect.

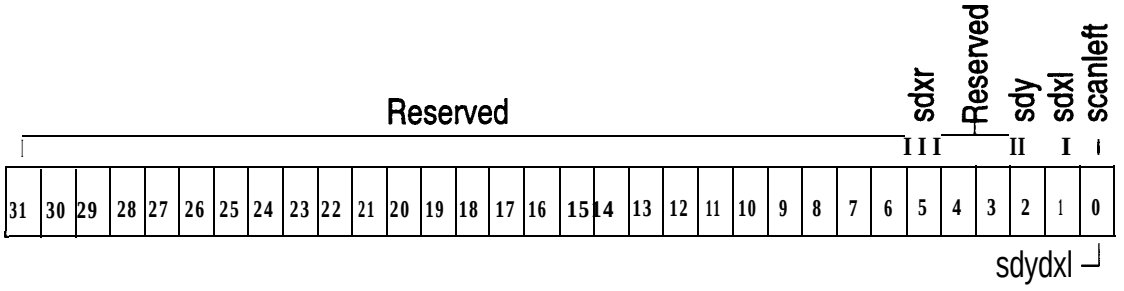
funoff <21:16> FUNnel shifter OFFset: For BLIT operations, this field is used to specify a bit offset in the funnel shifter count. In this case, **funoff** is interpreted as a 6-bit signed value.

fifcnt <25:22> FIFo COUNT: For BLIT operations, this field is used by the sequencer to determine how many source slices are available. In this case, the field does not need to be initialized.

stylelen <22:16> line STYLE LENgth: For LINE operations, this field specifies the linestyle length.

Reserved <31:26> Reserved: Writing has no effect.

Memory Address 1C58 **Attributes** W-FKD **Reset Value** XXXXXXXX h



sdydxl <0> Sign of Delta Y minus Delta X: This bit is shared with scanleft. It is defined for LINE drawing only and specifies the Major axis. This bit is automatically initialized during AUTOLINE operations.

. 0 Major axis is Y

- 1 Major axis is X

scanleft co> Horizontal SCAN direction LEFT (1) vs RIGHT (0): This bit is shared with sdydxl. It is used for TRAP and BLIT drawing. The **scanleft** bit is set according to the X scanning direction in a BLT or filled trapezoid.

Normally, this bit is always programmed to zero except for BITBLT when bltmod = BPLAN or BFCOL.

sdxl <1> Sign of delta X (line draw or left trapezoid edge): The sdxl bit specifies the X direction for a line draw (opcod = LINE) or the X direction when plotting the left edge in a filled trapezoid draw. This bit is automatically initialized during AUTOLINE operations.

- 0 delta X is positive

. 1 delta X is negative

sdy <2> Sign of delta Y: The sdy bit specifies the Y direction of the destination address. This bit is automatically initialized during AUTOLINE operations.

. 0 delta Y is positive

- 1 delta Y is negative

Reserved <4:3> Reserved: Writing has no effect.

sdxr <5> Sign of delta X (right trapezoid edge): The sdxr bit specifies the X direction of the right edge of a filled trapezoid.

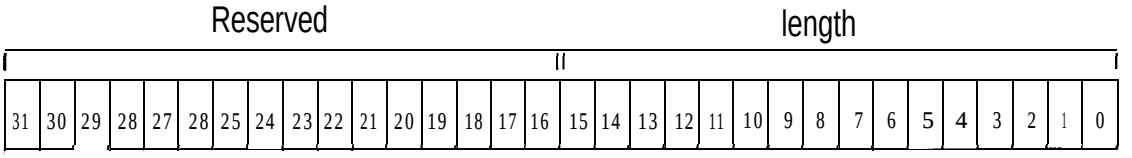
. 0 delta X is positive

- 1 delta X is negative

Reserved <31:6> Reserved: Writing has no effect.

LEN — Length

Memory Address 1C5C **Attributes** W-FKD **Reset Value** XXXX XXXX h



length <15:0> LENGTH: The length bit is a 16-bit unsigned value.

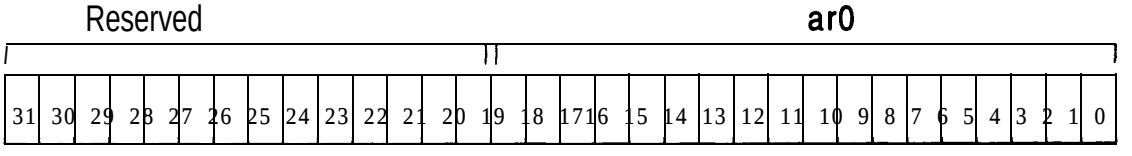
. The length field doesn't require initialization for **auto-init** vectors.

- For a vector draw, length is programmed with the number of pixels to be drawn.
- For Blits and trapezoid fills, length is programmed with the number of lines to be filled or **BLITed.**

Reserved <31:16> Reserved: Writing has no effect.

AR0 — Multi-purpose address register 0

Memory Address 1C60 **Attributes** W-FKD **Reset Value** XXXX XXXX h



ar0 <17:0> Address Register 0: The **ar0** field is an **18-bit** signed value in two's complement notation.

. For AUTOLINE, this register holds the X end address (see the XYEND register description on page 5-21).

- For LINE, it holds 2 x 'b'.

. For a filled trapezoid, it holds **'dYl'**.

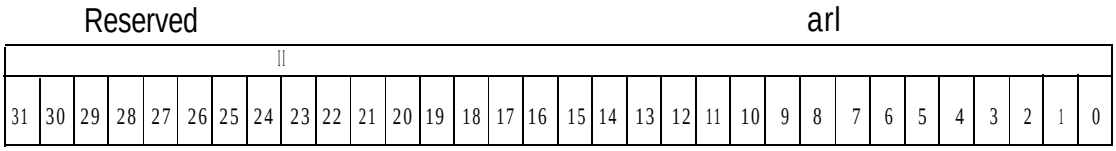
- For a BLIT, **ar0** holds the line end source address 'sea'.

Refer to Table 3-l for more information.

Reserved <31:18> Writing has no effect.

Multi-purpose address register 1 — AR1

Memory Address 1 C64 **Attributes** W-FKD **Reset Value** XXXX XXXX h



ar1 <23:0> Address Register 1: The arl field is a 24-bit signed value in two's complement notation. This register is also loaded when ar3 is accessed.

- For LINE, it holds the error term (initially 2 x 'b' - 'a' -[sdy]).

. This register does not need to be loaded for AUTOLINE.

- For a filled trapezoid, it holds the error term in two's complement notation; initially:

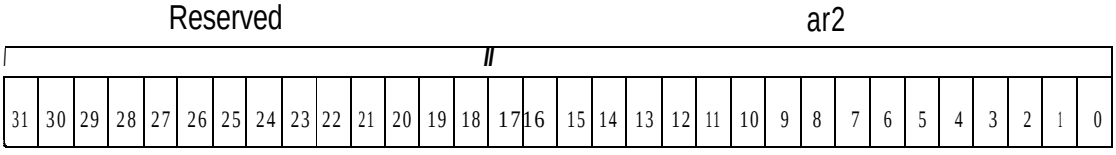
  'errl' = [sdxl] ? 'dXl' + 'dYl' - 1 : -'dXl'

. For a BLIT, arl holds the line start source address 'ssa'. Because 'ssa' is also required in ar3 and when writing ar3, arl is loaded, this register doesn't need to be explicitly initialized.

Reserved <31:24> Reserved: Writing has no effect.

Multi-purpose address register 2 — AR2

Memory Address 1C68 **Attributes** W-FKD **Reset Value** XXXX XXXX h



ar2 <17:0> Address Register 2: The ar2 field is an 18-bit signed value in two's complement notation.

- For AUTOLINE, this register holds the Y end address (see the XYEND register description on page 5-21).
- For LINE, it holds the minor axis error increment (initially 2 x 'b' - 2 x 'a').

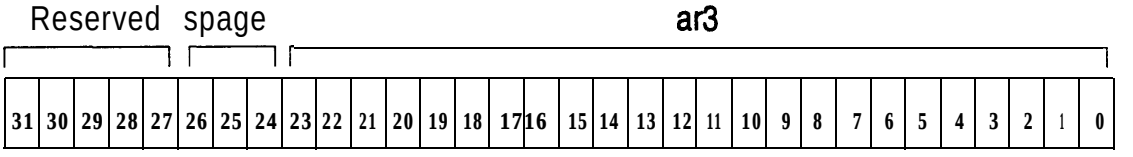
. For a filled trapezoid, it holds the minor axis increment -|dXl|.

- This register is not used for BLIT operations.

Reserved <31:18> Reserved: Writing has no effect.

AR3 — Multi-purpose address register 3

Memory Address 1C6C **Attributes** W-FKD **Reset Value** XXXX XXXX h



ar3 <23:0> Address Register 3: The ar3 field is a 24-bit signed value in two's complement notation or a 24-bit unsigned value.

- This register is used during AUTOLINE, but does not need to be initialized.
- This register is not used for LINE without Auto initialization, nor is it used by TRAP.

. In the two operand Blit algorithms, ar3 contains the source current address 'sca'. This value must be initialized as the starting address for a Blit. The 'sca' is always linear.

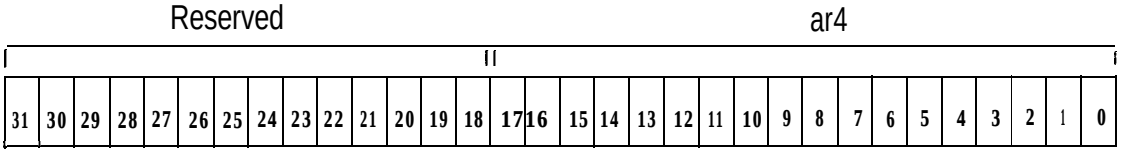
spage <26:24> These three bits are used as an extension to ar3 in order to generate a 27-bit source or pattern address. They are not modified by ALU operations.

The spage field is not used for TRAP, LINE or AUTOLINE operations.

Reserved <31:27> Reserved: Writing has no effect.

AR4 — Multi-purpose address register 4

Memory Address 1C70 **Attributes** W-FKD **Reset Value** XXXX XXXX h



ar4 <17:0> Address register 4: The ar4 field is an 18-bit signed value in two's complement notation.

. For TRAP, it holds the error term. Initially:

'errr' = [sdxr] ? 'dXr' + 'dYr' - 1 : -'dXr'

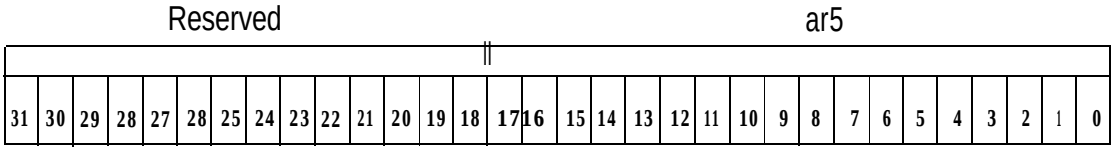
. This register is used during AUTOLINE, but it doesn't need to be initialized.

. This register is not used for LINE or BLIT operations.

Reserved <31:18> Reserved: Writing has no effect.

Multi-purpose address register 5 — AR5

Memory Address 1C74 **Attributes** W-FKD **Reset Value** *XXXX* XXXX h



ar5 <17:0> Address Register 5: The **ar5** field is an 1 8-bit signed value in two's complement notation.

. At the begining of AUTOLINE, **ar5** holds the X start address (see the XYSTRT register on page 5-20). At the end of AUTOLINE the register is loaded with the X end, so it is not necessary to reload the register when drawing a polyline.

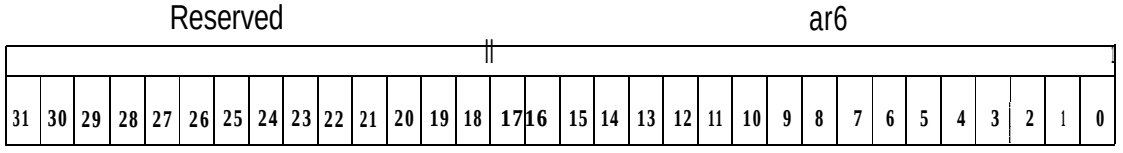
- This register is not used for LINE without Auto initialization.
- For TRAP, it holds the minor axis increment -ldYrl.

. In BLIT algorithms, ar5 holds the pitch of the source operand 'syinc' (see Table 3- 1). A negative pitch value specifies that the source is scanned from bottom to top while a positive pitch value specifies a top to bottom scan.

Reserved <31:18> Reserved: Writing has no effect.

Multi-purpose address register 6 — AR6

Memory Address 1C78 **Attributes** W-FKD **Reset Value** *XXXX XXXX* h



ar6 <17:0> Address Register 6: This field is an 1 8-bit signed value in two's complement notation. It is sign extended to 24 bits before being used by the ALU.

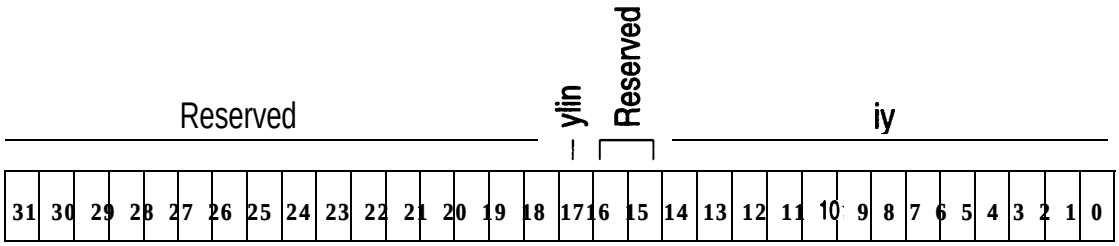
- At the begining of AUTOLINE, ar6 holds the Y start address (see the XYSTRT register description on page 5-20). During AUTOLINE processing, this register is loaded with the signed Y displacement. At the end of AUTOLINE the register is loaded with the Y end, so it is not necessary to reload the register when drawing a polyline.
- This register is not used for LINE without Auto initialization.

. For TRAP, it holds the major axis increment 'dYr'.

- This register is not used for BLIT operations.

Reserved <31:18> Reserved: Writing has no effect. These bits return all zeroes when read.

Memory Address 1C8C **Attributes** W-FKD **Reset Value** XXXXXXXX h



iy <12:0> Y Increment: This field is a 13-bit unsigned value. The Y increment value is a pixel unit, and it must be a multiple of 32 (the five LSB = 0). This field specifies the increment to be added to or subtracted from ydst between two destination lines. This field is also used as the multiplicator factor for linearizing the iy register.

It should be noted that only a few values are supported for linearization. If the pitch selected can't be linearized, the ylin bit should be used to disable the linearization operation. The following table provides the supported pitch for linearization:

Pitch	*iy*	*Pitch*	*iy*
512	0010000000000	1152	0010010000000
640	0010100000000	1280	0010100000000
768	0011000000000	1536	0011000000000
800	0011001000000	1600	0011001000000
1024			

Reserved <14:13> Reserved: Writing has no effect.

ylin <15> Y LINearization: This bit specifies if the address must be linearized or not.

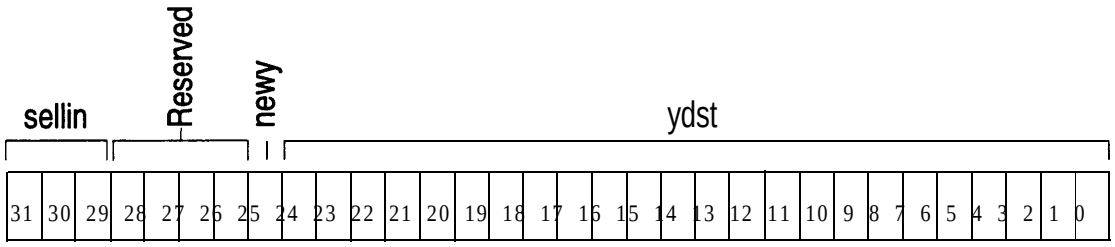
. 0 Linearize the address

- 1 Don't linearize the address

Reserved <31:16> Reserved: Writing has no effect.

Memory Address 1C90 **Attributes** W-FKD

Reset Value XXXXXXX 0 XXXXXXXXXXXXXXXXXXXXXXXX b



ydst <23:0>

Y DeSTination: The ydst field contains the current Y coordinate of the destination address as a signed value in two's complement notation. Two formats are supported: linear format and XY format. The current format is selected by ylin.

When XY format is used, ydst represents the Y coordinate of the address. The valid range is -32768 to +32767 (16-bit signed). The XY value is always converted to a linear value before being used.

When linear format is used, ydst must be programmed as follows:

ydst <-- (Y coordinate) x PITCH >> 5

The Y coordinate range is from -32768 to +32767 (16-bit signed) and the pitch range is from 32 to 6144. Pitch is also a multiple of 32.

. Before starting a vector draw, ydst must be loaded with the Y coordinate of the starting point of the vector. This can be done by accessing the XY_START register. This register does not require initialization for polyline operations.

. Before starting a BLIT, ydst is loaded with the Y coordinate of the starting comer of the destination rectangle.

. For trapezoids, this register must be loaded with the Y coordinate of the first scanned line of the trapezoid.

newy <24>

NEW Y: The newy field is a l-bit field which is always set every time the register is written by the processor (bit 24 of the data bus is discarded). This bit is cleared when ydstorg is added to ydst. This bit is used to inhibit the linearization of an address which has already been linearized. This bit is also set when the host accesses the XYSTRT register.

Reserved <28:25>

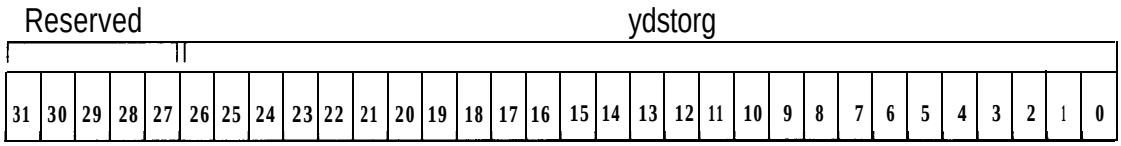
Reserved: Writing has no effect.

selli n <31:29>

SELected LINe. The sellin field is used to perform the dithering, patterning, and transparency functions. During linearization, this field is loaded with the three LSB of ydst. If no linearization occurs, then those bits have to be initialized correctly if one of the above-mentioned functions is to be used.

YDSTORG — Memory origin

Memory Address 1 C94 **Attributes** W-FK **Reset Value** XXXX XXXX h



ydstorg <26:0>

DeSTination Y ORiGin: The ydstorg field is a 27-bit unsigned value. It gives an offset value in pixel units, in order to position the first pixel of the first line of the screen. This register is used to initialize the YDST address.

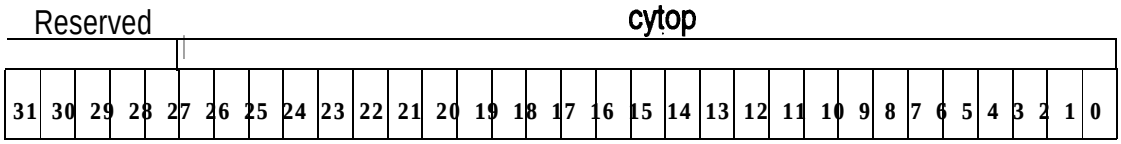
This register must be loaded with a multiple of 32 (the five LSB = 0).

Reserved <31:27>

Reserved: Writing has no effect.

YTOP — Clipper Y top boundary

Memory Address 1 C98 **Attributes** W-FK **Reset Value** XXXX XXXX h



cytop <26:0>

Clipper Y top boundary: The cytop field contains an unsigned 27-bit value which is interpreted as a positive pixel address and compared with the current ydst. The value of the ydst field must be greater than or equal to cytop to be inside the drawing window.

This register must be programmed with a linearized line number:

cytop = (TOP LINE NUMBER) x PITCH + YDSTORG

This register must be loaded with a multiple of 32 (the five LSB = 0).

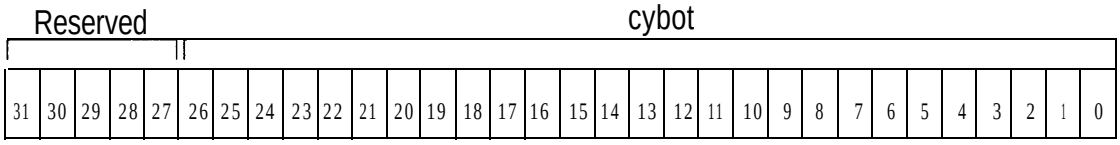
Note that since the cytop value is interpreted as positive, any negative ydst value is automatically outside the clipping window. There is no way to disable clipping.

Reserved <31:27>

Reserved: Writing has no effect.

Clipper Y maximum boundary — YBOT

Memory Address 1C9C **Attributes** W-FK **Reset Value** XXXX XXXX h



cybot <26:0> Clipper Y BOTtom boundary: The cybot field contains an unsigned 22-bit value which is interpreted as a positive pixel address and compared with the current ydst. The value of the ydst field must be less than or equal to cybot to be inside the drawing window.

This register must be programmed with a linearized line number:

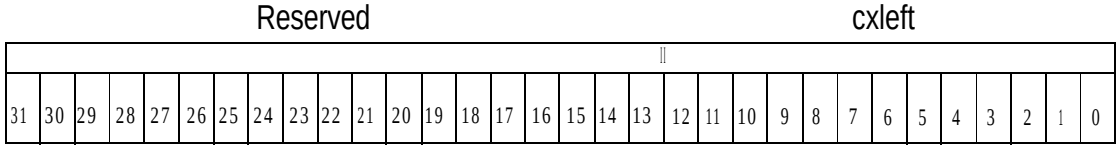
cybot = (BOTTOM LINE NUMBER) x PITCH + YDSTORG

This register must be loaded with a multiple of 32 (the five LSB = O).There is no way to disable clipping.

Reserved <31:27> Reserved: Writing has no effect.

Clipper X minimum boundary — CXLEFT

Memory Address 1CA0 **Attributes** W-FK **Reset Value** XXXX XXXX h



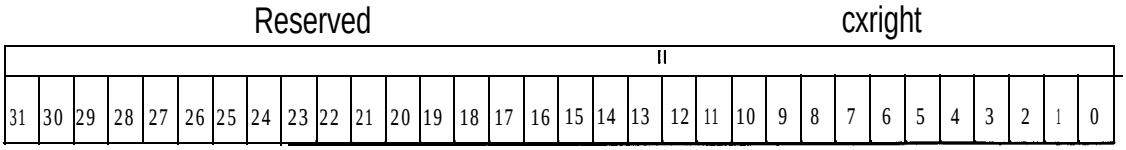
cxleft <12:0> Clipper X LEFT boundary: The cxleft field contains an unsigned 13-bit value which is interpreted as a positive pixel address and compared with the current xdst. The value of xdst must be greater than or equal to cxleft to be inside the drawing window.

Note that since the cxleft value is interpreted as positive, any negative xdst value is automatically outside the clipping window. There is no way to disable clipping.

Reserved <31:13> Reserved: Writing has no effect.

CXRIGHT — Clipper X maximum boundary

Memory Address 1CA4 **Attributes** W-FK **Reset Value** XXXX XXXX h

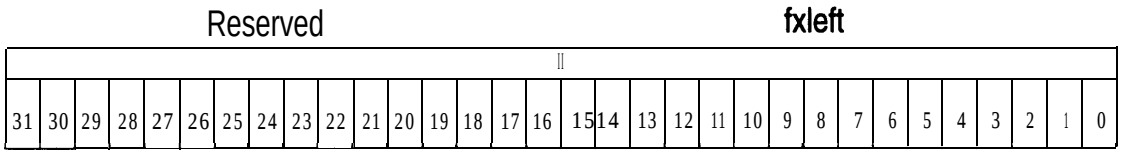


cxright <12:0> Clipper X RIGHT boundary: The cxright field contains an unsigned 13-bit value which is interpreted as a positive pixel address and compared with the current xdst. The value of xdst must be less than or equal to cxright to be inside the drawing window. There is no way to disable clipping.

Reserved <31:13> Reserved: Writing has no effect.

FXLEFT — X address register (left)

Memory Address 1CA8 **Attributes** W-FKD **Reset Value** XXXX XXXX h



fxleft <15:0> Filled object X LEFT coordinate: The fxleft field contains the X coordinate of the left boundary of any filled object being drawn. It is a 16-bit signed value in two's complement notation.

. The fxleft field is not used for line drawing.

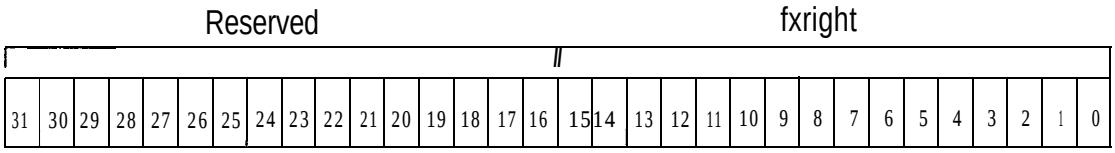
. During filled trapezoid drawing, fxleft is updated during the left edge scan.

- During a BLIT operation, fxleft is static, and specifies the left pixel boundary of the area being written to.

Reserved <31:16> Reserved: Writing has no effect.

X address register (right) FXRIGHT

Memory Address 1 CAC **Attributes** W-FKD **Reset Value** XXXX XXXX h



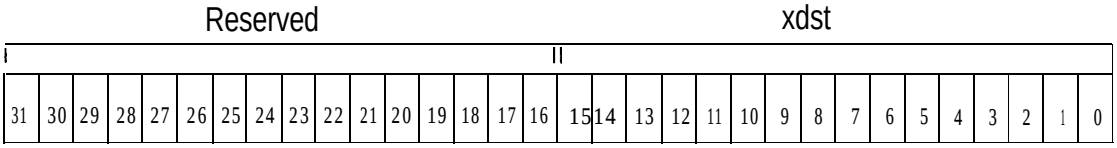
fxright <15:0> Filled object X RIGHT coordinate: The fxright field contains the X coordinate of the right boundary of any filled object being drawn. It is a 16-bit signed value in two's complement notation.

- The fxright field is not used for line drawing.
- During filled trapezoid drawing, fxright is updated during the right edge scan.
- During a BLIT operation, fxright is static, and specifies the right pixel boundary of the area being written to.

Reserved <31:16> Reserved: Writing has no effect.

X Destination address register XDST

Memory Address 1 CBO **Attributes** W-FKD **Reset Value** XXXX XXXX h



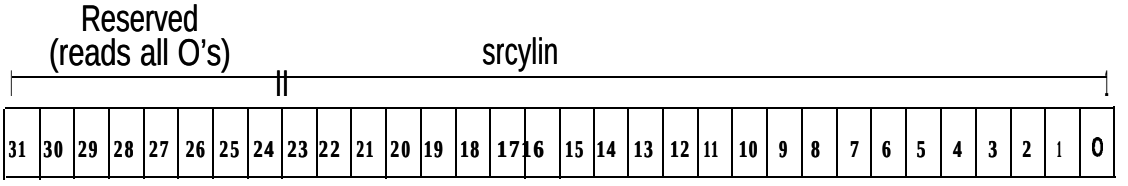
xdst <15:0> X coordinate of the destination address: The xdst field contains the running X coordinate of the destination address. It is a 16-bit signed value in two's complement notation.

. Before starting a vector draw, xdst must be loaded with the X coordinate of the starting point of the vector. At the end of a vector xdst contains the address of the last pixel of the vector. This can also be done by accessing the XYSTRT register.

- This register does not require initialization for polyline operations.
- For trapezoids and BLITs, this register is automatically loaded from fxleft and fxright and no initial value must be loaded.

Reserved <31:16> Reserved: Writing has no effect.

Memory Address 1E00 **Attributes** R/W **Reset Value** XXXX XXXX h



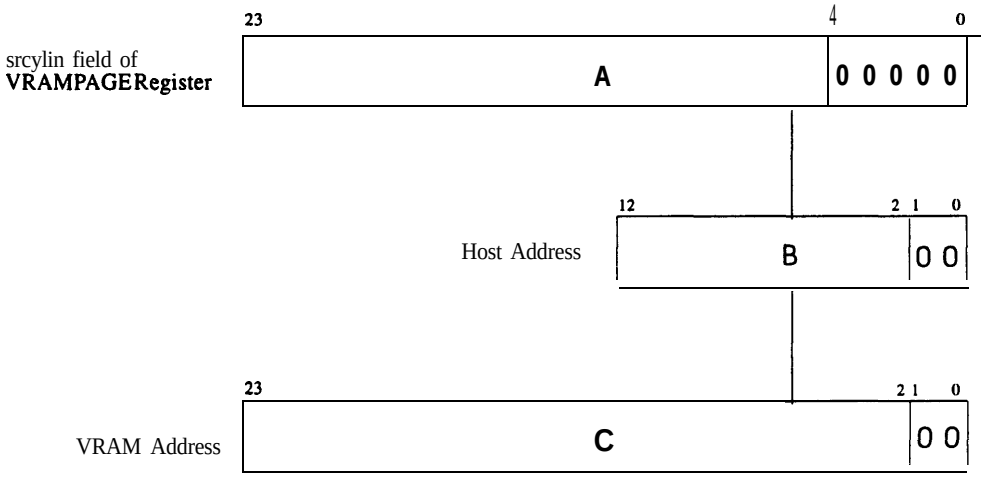
srcylin <23:0> **SouRCe LINear** Y coordinate: Represents the linearized Y coordinate when accessing the VRAM window memory region.

SrcYLin = Y x (byte pitch)
where byte pitch = (# pixels/line) x (# bytes/pixel)

This register must be loaded with a multiple of 32 (the five LSB = 0). The five LSB of this register are always read as zero.

During VRAM read or write direct access, the address that is used by the **VRAM** is generated from srcylin and the host address bits **<12:2>**.

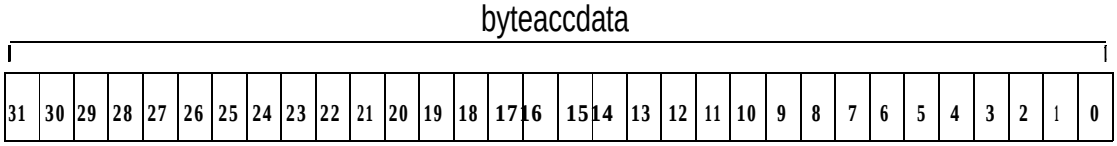
The figure below illustrates how vaddr (the VRAM address) is generated. The 'A' variable represents bits **23:5** of the VRAMPAGE register, 'B' represents host address bits, and 'C' is the result of the addition of A and B, aligned as shown below.



Reserved <31:24> Reserved: Writing has no effect. These bits return all zeroes when read.

Byte Accumulator Data — BYTACCDATA

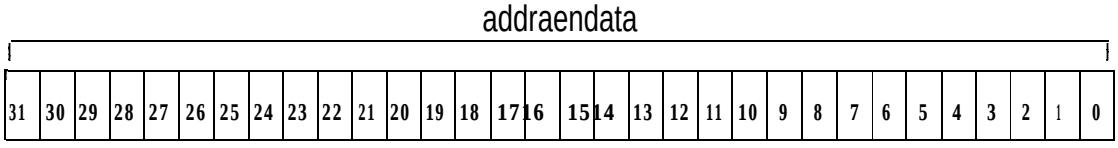
Memory Address 1E08 **Attributes** R **Reset value** XXXX XXXXh



byteaccdata <31:0> BYTE ACCumulator DATA: This register is used for test purposes only.

Address Generator — ADRGEN

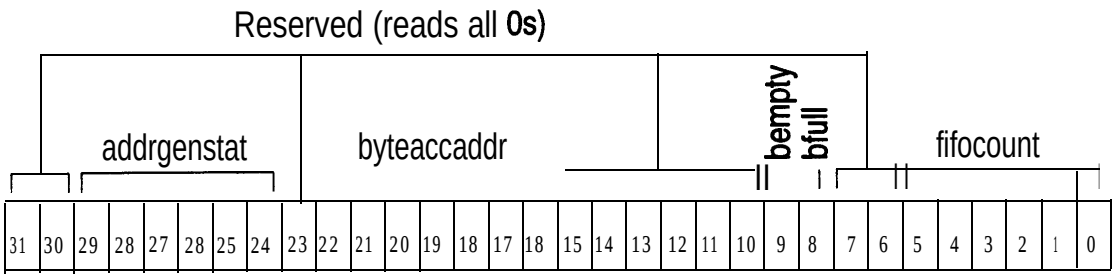
Memory Address 1E0C **Attributes** R **Reset value** XXXX XXXXh



addrgendata <31:0> ADDRess GENerator DATA: This register is used for test purposes only.

FIFOSTATUS — BUS FIFO status register

Memory Address 1E10 **Attributes** R **Reset value** 21XX 0220h



fifocount <5:0> FIFO COUNT: Indicates the number of free locations in the Bus FIFO. On reset, the Bus FIFO is empty (there are 32 locations available). The **readback** path is protected so that a valid count is always read.

Reserved <7:6> Reserved: Writing has no effect. These bits return all zeroes when read.

bfull <8> Bus FIFO FULL flag: When set to '1', indicates that the Bus FIFO is full.

bempty <9> Bus FIFO EMPTY flag: When set to **'1',** indicates that the Bus FIFO is empty.

Reserved <15:10> Reserved: Writing has no effect. These bits return all zeroes when read.

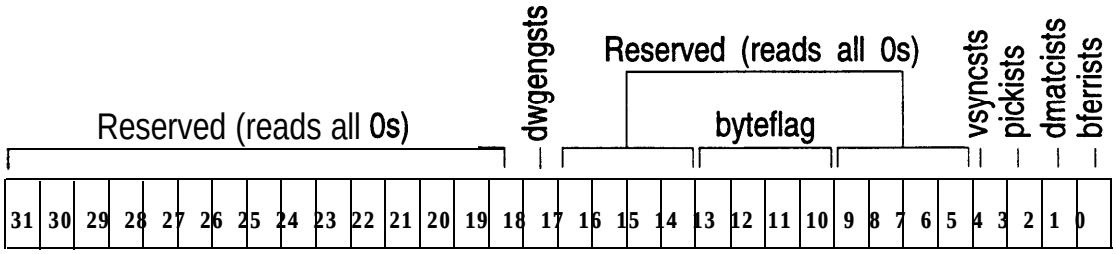
byteaccaddr <22:16> BYTE ACCumulator ADDRess: This field is used for test purposes only.

Reserved <23> Reserved: Writing has no effect. These bits return all zeroes when read.

addrgenstate <29:24> ADDRess GENerator STATE: This field is used for test purposes only.

Reserved <31:30> Reserved: Writing has no effect. These bits return all zeroes when read.

Memory Address 1E14 **Attributes** R **Reset value** 0000 00XXh



bferrists <0> Bus FIFO ERRor Interrupt STatuS: Bus FIFO error flag. When set to '1', indicates that a cycle may have caused a timeout error.

This status bit is set when an access to any device other than the VGA frame buffer causes a wait that lasts more than 64 gclks. If the wait lasts 128 gclks, the cycle is aborted. This status bit may be used by software during the debugging cycle as a problem indicator.

dmatcists <1> DMA Terminal Count Interrupt STatuS: When set to '1', indicates that a DMA Terminal count has occurred. If DmaTc interrupt is enabled, DmaTcists is activated by a valid Terminal count, and held until it is cleared through the ICLEAR register's dmatcclr bit.

pickists <2> PICKing Interrupt STatuS: When set to '1', indicates that a picking interrupt has occurred. This bit is cleared through the pickiclr bit.

vsyncsts<3> VSYNC STatuS: Set to '1' during the VSYNC period. This bit follows the vsync signal.

Reserved <7:4> Reserved: Writing has no effect. Reading will give 0's.

byteflag <11:8> BYTE FLAG: This field is used for test purposes only.

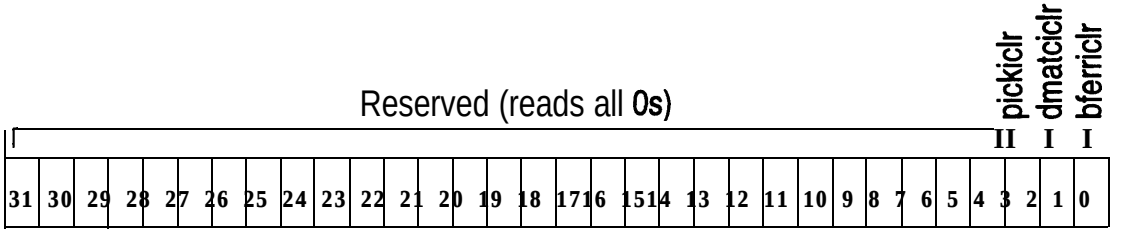
Reserved <15:12> Reserved: Writing has no effect. These bits return all zeroes when read.

dwgengsts <16> DraWinG ENgine STatuS: Set to '1' when the drawing engine is busy (that is, when there is something in the bfifo, afifo, actl, or mctl – other than refresh, data transfer, or a direct access).

Reserved <31:17> Reserved: Writing has no effect. These bits return all zeroes when read.

ICLEAR — Interrupt Clear register

Memory Address 1E18 **Attributes** W **Reset value** 0000 0000 h



bferriclr <0> Bus FIFO Error Interrupt CLeaR: Writing a '1' to this bit clears the bferror interrupt status flag. Writes to this field are glitch-free.

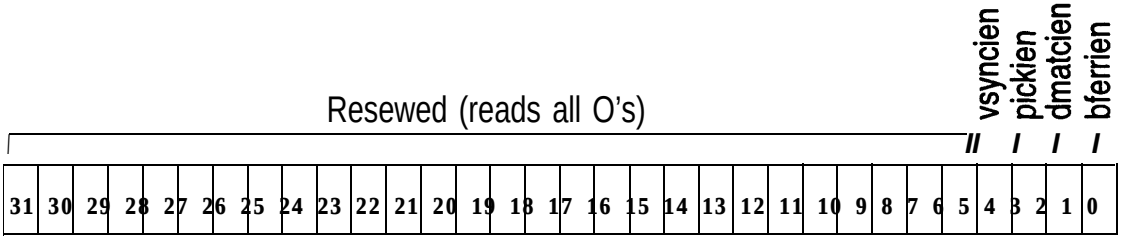
dmatciclr <1> DMA Terminal Count Interrupt CLeaR: Writing a '1' to this bit clears the dmatc interrupt status flag. Writes to this field are glitch-free.

pickiclr <2> PICKing Interrupt CLeaR: Writing a '1' to this bit clears the picking interrupt status flag. Writes to this field are glitch-free.

Reserved <31:3> Reserved: Writing has no effect. These bits return all zeroes when read.

IEN — Interrupt Enable register

Memory Address 1E1C **Attributes** R/W **Reset value** 0000 0000 h



bferrien <0> Bus FIFO Error Interrupt ENable: When set to '1', enables interrupt if a Bus FIFO error occurs. Writes to this field are glitch-free.

dmatcien <1> DMA Terminal Count Interrupt ENable: When set to '1', enables interrupt if a DMA terminal count occurs, with DmaAct set. Writes to this field are glitch-free.

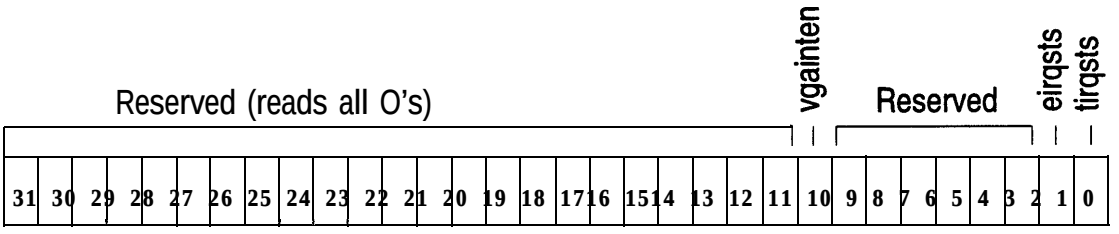
pickien <2> PICKing Interrupt ENable: When set to '1', enables interrupt if a picking interrupt occurs. Writes to this field are glitch-free.

vsyncien <3> VSYNC Interrupt ENable: When set to '1', enables interrupts from the VGA when in Power Graphic mode (vgaen = 0). Writes to this field are glitch-free.

Reserved <31:4> Reserved: Writing has no effect. These bits return all zeroes when read.

Memory Address 1E28 (MEM PCI) **Attributes** R/W

Reset Value 0000 0000 0000 0000 0000 0000 0000 0000b



❖**Note** that this register only exists in the PCI configuration.

Reserved <31:9> This field is always read as OOOOh.

vgainten <8> This bit indicates whether or not the VGA interrupt is enabled. As the other internal ATLAS interrupt, VGA interrupt status is available on tirqsts.

- 0: VGA interrupts are disabled
- 1: VGA interrupts are enabled

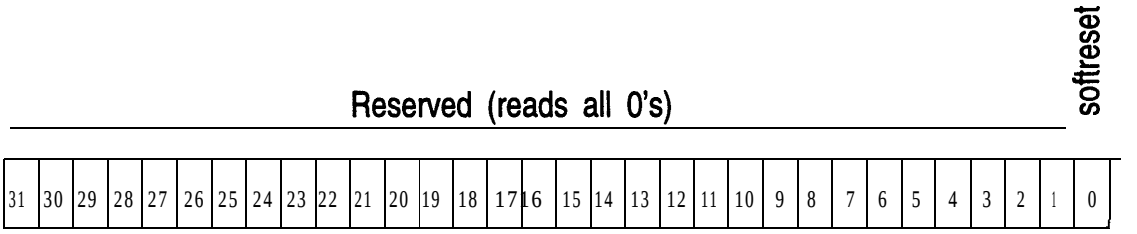
Reserved <7:2> This field is always read as OOOOh.

eirqsts<1> Indicates when read as '1' that an external interrupt has occured. This status is set when an edge is detected on the eirqN pin.

A read to this bit accesses its value normally. A write, however, is slightly different in that the bit can be reset, but not set. This bit is reset whenever the register is written, and the data in the corresponding bit location is 1.

tirqsts<0> Status of the tirq pin. When 0, indicates that the source of the interrupt on INTA is from the ATLAS chip.

Memory Address 1E40 **Attributes** R/W **Reset value** 0000 0000h



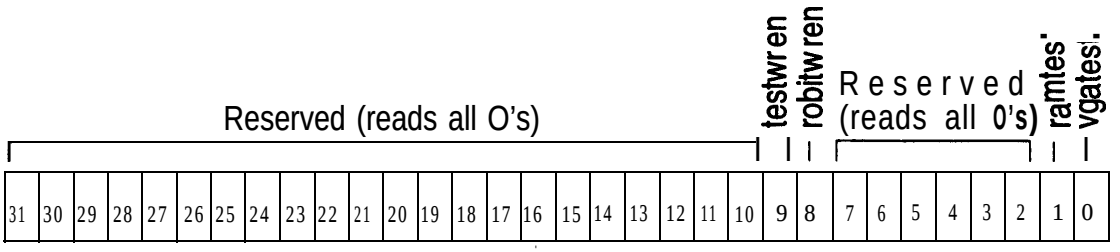
softreset <0> SOFT RESET: When set to '1', resets all host register bits, except those which are hard reset only. The softreset signal is synchronous on gclk, and takes place at the end of the write cycle. On the next read, all concerned bits will be reset.

A '0' must be programmed to remove the softreset. Writes to this field are glitch-free.

Reserved <31:1> Reserved: Writing has no effect. These bits return all zeroes when read.

Memory Address 1E44 (MEM) **Attributes** R/W - STATIC **Reset Value**

Reset Value 0000 0000 0000 0000 0000 OOHO 0000 0000 b



vgatest <0> R/(W) VGA TEST bit: This bit is used for test purposes, and should always be set to zero for normal operation. Writes to this field are glitch-free.

ramtest <1> R/(W) RAM TEST bit: Reset to '0'. This bit is used for test purposes, and should always be set to zero for normal operation. Writes to this field are glitch-free.

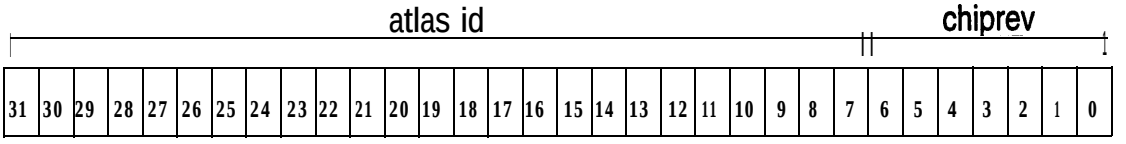
Reserved <7:2> Reserved: Writing has no effect. These bits return all zeroes when read.

robitwren <8> RO Read Only BIT **WRite ENable:** When set to **'1',** enables write to the **mapsel<2:0>, isa,** pci, and above1 meg bits. Writing ' 10001101' to byte 3 of the TEST register will set robitwren to ' 1'. Writing values other than ' 10001101' will reset the bit to '0'.

testwren <9> RO TEST **WRite ENable:** Sampled (inverted) at hard reset on **VD<38>**. In functional mode, **VD<38>** must always have an external PU. In order to place the ATLAS in **ramtest** or vgatest mode on the tester, **VD<38>** should be driven low during the reset vectors. This way, **testwren** will be active after the reset, and the **ramtest** and vgatest test bits may be written to enable the appropriate test mode. Since **testwren** is read-only, the test bits can't be modified in functional mode.

Reserved <31:10> Reserved: Writing has no effect. These bits return all zeroes when read.

Memory Address 1E48(MEM) **Attributes** R - STATIC **Reset value** A268 1701h

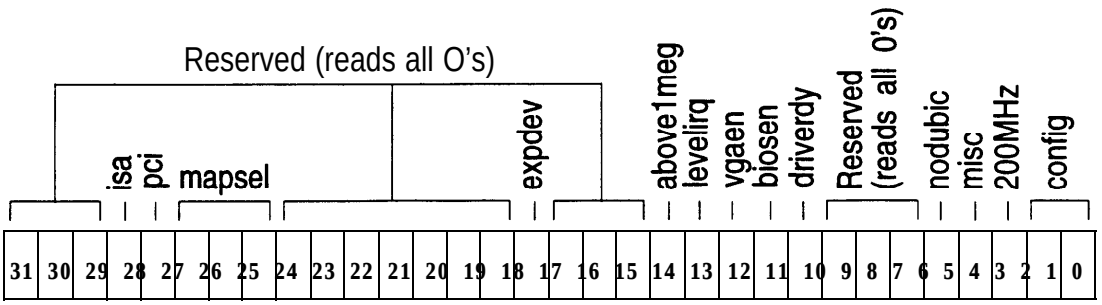


chiprev <6:0> CHIP REVision code: Read value is Olh. This value will change if there are any chip revisions.

atlas id <31:7> ATLAS IDentification: This field provides a fixed non-zero identification. It may be used to help locate the MGA when the value of mapsel is unknown to the software.

Since MGA ATLAS is part of the same family as the MGA TITAN chip (a precursor of ATLAS), and in order to make software programming easier, the same ID is used for the TITAN and ATLAS chips. ATLAS can be differentiated from TITAN by the **chip revision number.** The data is the 5-bit ASCII code for the name "TITAN".

Memory Address 1E50(MEM) **Attributes** R/W
Reset Value OOOH HHHH 0000 0000 OOOH 0HHH OOOH 00HHb



❖ Note: In order to respect the Tr24 timing, software must wait after accessing this register. Only byte accesses should be made to this register.

config <1:0> R/W

CONFIGuration bits: Sampled on reset, this field assumes the external strapping configuration value. The reset value can be overwritten. Writes to this field are glitch-free. Note that only byte access (byte 0) is permitted for modification of the config bits.

Bit 1 is used as the narrow decode configuration bit. When '1', mcs16N is a decode based on ISA bus addresses LA<23:17>, which represents a 128K range. When '1', mcs16N will also depend on SA<16:14>, which represents the narrow decode of the 16K MGA space and 32K ROM space. No mcs16N sampling is supported.

The VGA frame buffer and IO port are always 8-bit devices.

The configuration determines whether ATLAS's resources are 8-16- or 32-bit devices, according to the tables which follow.

biosen	*config<1:0>*	*BIOS*	*mcs16N*	*ex32N*
0	xx	No decode	1	1
1	00	8	1	1
	01	16	0	1
	10	Reserved	1	1
	11	16 narrow	0	1

isa	*mapsel*	*vgaen*	*config<1:0>*	*MGA*	*mcs16N*	*ex32N*
0	000	X	XX	No decode	1	1
	001	0	XX	32 narrow	1	0
	001	1	XX	8	1	1
	010–111	X	XX	32 narrow	1	0

X = 'don't care'

❖ Note: Only byte accesses (byte0) are permitted for modification of these bits. In the PCI configuration, these bits must be set to '00'.

Refer to Section 3.6.3 to determine the reset value of config<1:0>.

200MHz<2> 200 MHz function. A strap exists on the RESET configuration bus to identify boards that are capable of functioning with a pixel clock of up to 200 MHz. This strap, called '200MHz', is read from VD<48> at reset. This bit must be read by software, inverted, then loaded into CONFIG<2>. It is interpreted as follows:

200MHz	*Meaning*
1	Board supports 200 MHz operation
0	Board only supports regular (135 MHz-170 MHz) operation

misc<3> R/W MISCellaneous bit: Reserved for future use. This field has no definition. This is a multi-purpose software bit.

Refer to Section 3.6.3 to determine the reset value of this bit.

nodubic<4> R/W NO DUBIC in the system: Sampled on reset, this bit assumes the external strapping configuration value. Writes to this bit are glitch-free.

This bit indicates whether or not ATLAS is being used in conjunction with a DUBIC chip:

. 0: DUBIC present (TITAN-compatible mode).

- 1: No DUBIC present. ATLAS controls the VRAM and RAMDAC directly.

Refer to Section 3.6.3 to determine the reset value of this bit.

Reserved <7:5> Reserved: Writing has no effect. These bits return all zeroes when read.

driverdy <8> RO DRIVE channel ReaDY: Sampled on reset, this bit assumes the external strapping configuration value. The reset value can't be overwritten. All interrupts should be disabled when writing to this bit.

This field determines how the CHRDY/ signal is generated:

Value	*Meaning*
0	The CHRDY signal output is tri-stateable, and the CHRDYEN/ enable signal is a delayed version of CHRDY.
1	The CHRDY signal is always driven by ATLAS, and an external tri-state buffer is required.

In the PCI configuration, this bit must be set to '1'. Refer to Section 3.6.3 to determine the reset value of this bit.

biosen <9> R/W BIOS ENable: Set to ' 1' on reset if vgaen is sampled active (' 1'). The reset value can be overwritten. When set to '1', the VGA BIOS is enabled.

Note that the BIOS can be enabled separately from the VGA I/O and the frame buffer. This way, the board that boots as the VGA device can always keep its BIOS active if desired. Also, there can always be a BIOS active, even when there's no active VGA (except at boot-up). All interrupts should be disabled when writing this bit.

vgaen <10> R/W

VGA ENable: Sampled on reset, this bit assumes the external strapping configuration value. The reset value can be overwritten. All interrupts should be disabled when writing this bit. Writes to this field are glitch-free.

Value	*Meaning*
0	VGA is disabled
1	VGA is enabled

Refer to Section 3.6.3 to determine the reset value of this bit.

levelirq <11> R/W

LEVEL Interrupt Request: This bit is used to select between a positive edge triggered or a level-sensitive interrupt.

. When '0' (hard reset value), ATLAS produces a positive edge interrupt.

. When set to ' 1' , ATLAS produces a negative level interrupt.

See Section 3.2.6 for more details about ATLAS's interrupts.

This field should be written to only when necessary. When written, it may glitch or pass through an intermediate value, even when rewriting the same value. All interrupts should be disabled when writing this bit.

abovelmeg <12> R/(W)

Mapped ABOVE 1 MEG: Sampled on reset, this bit assumes the external strapping configuration value.

For test purposes, this bit can be modified by a write. To do this, the robitwren bit from the TEST register must be set to ' 1'. All interrupts should be disabled when writing this bit. Writes to this field are glitch-free.

Refer to Section 3.6.3 to determine the reset value of this bit.

- When abovelmeg is active (1):
  - decodeN<1> may be used to decode any address bits down to bit 20. It should be active when la<31:20> (or just la<23:20> on an ISA machine) decodes the MGA range.
  - decodeN<0> should be tied to '0' in an ISA machine. In other systems, it should be active when la<31:24> = 00h is decoded.

. When abovelmeg is inactive (0):

- decodeN<1> and decodeN<0> should be tied to '0'.

In the PCI configuration, this bit must be set to '0'.

Reserved <15:13>

Reserved: Writing has no effect. These bits return all zeroes when read.

expdev <16> R/W

EXPansion DEVice: This bit affects EXPSL/. On power up, software must read the external strapping value in the destination register, and set this bit properly.

This field is considered semi-static. It should be written to only when necessary. When written, it may glitch or pass through an intermediate value, even when rewriting the same value. This field indicates the availability of external expansion devices:

Value	*Meaning*
0	No expansion device is available
1	Expansion device is accessible

Refer to Section 3.6.3 to determine the reset value of this bit.

Reserved <23:17>

Reserved: Writing has no effect. These bits return all zeroes when read.

mapsel <26:24> R/(W)

Sampled on reset, this field assumes the external strapping configuration value. The mapsel field determines the base of the MGA address map. For more details, see Chapter 4. Writes to this field are glitch-free.

For test purposes, mapsel<2:0> can be modified by a write. To do this, the robitwren bit from the TEST register must be set to ' 1' .

Refer to Section 3.6.3 to determine the reset value of these bits.

- MAPSEL1 should only be used if you boot in VGA mode
- MAPSELO can be used if you boot in VGA mode for system debugging. In this mode, MGA is not mapped. But you may still boot and configure your system using the VGA display.

In the PCI configuration, these bits must be set to '010'.

pci<27> R/(W)

PCI Bus Identification: Sampled on reset, this bit assumes the external strapping configuration value. It is used in conjunction with the isa field to determine the current host interface type.

To write this bit, the robitwren bit in the TEST register must be set to ' 1'. Writes to this field are glitch-free.

Refer to Section 3.6.3 to determine the reset value of this bit.

isa<28> R/(W)

ISA Bus Identification: Sampled on reset, this bit assumes the external strapping configuration value. This bit is used in conjunction with the pci field to determine the current host interface type.

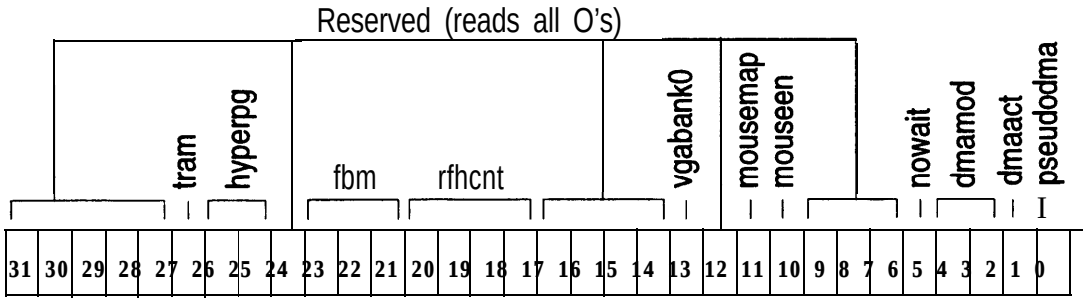
To write this bit, the robitwren bit in the TEST register must be set to ‘1’. Writes to this field are glitch-free.

isa	*pci*	*Bus Type*
0	***0***	Reserved
0	1	PCI Bus
1	0	ISA Bus
1	1	Reserved

Refer to Section 3.6.3 to determine the reset value of this bit.

Reserved <31:29> Reserved: Writing has no effect. These bits return all zeroes when read.

Memory Address 1E54 **Attributes** R/W
Reset value 0000 0000 0000 0000 0000 H000 0000 0000 b



- 3 Note: In order to respect the Tr24 timing, software must wait after accessing this register. Only byte accesses should be made to this register.

pseudodma <0> R/W PSEUDO **DMA:** When set to '1', the VRAM window becomes a DMA access port. This will allow movestring access to the Bus FIFO. In order to start a new Pseudo DMA sequence, this bit and dmaact must be 'O', dmamod must be initialized, then, in a separate access, this bit should be set to '1'.

Writes to this field are glitch-free.

dmaact <1> R/W **DMA ACTive:** When set to '1', indicates the beginning of a DMA transfer. This bit is reset to '0' automatically, when the DMA terminal count (TC) is sampled active.

Once set to '1' , only a DMA terminal count, a hard reset, or a soft reset will return dmaact to '0'. Writing a '0' to this bit will have no effect. In order to start a new DMA sequence, this bit and pseudodma must be 'O', dmamod must be initialized, then, in a separate access, this bit should be set to '1'.

Writes to this field are glitch-free.

dmamod <3:2> R/W **DMA MODe:** There are four DMA or Pseudo DMA transfer modes on the ATLAS, selected through the DmaMod bits. These bits must be programmed before starting DMA or Pseudo DMA transfer. The dmaact and pseudodma bits must be '0' **before** modifying these bits.

dmaMod<1:0>	*DMA*	*PSEUDO DMA*	*DMA transfer mode description*
00	***Yes***	***Yes***	DMA General Purpose Write
01	Yes	Yes	DMA BLIT Write
10	Yes	Yes	DMA Vector Write
11		Yes	DMA BLIT Read (IDUMP)

Writes to this field are glitch-free.

nowait <4> R/W

NO WAIT: This bit is used to select between: always adding waits (0); and only adding waits when necessary (1).

When '0' (the reset value), ATLAS will automatically generate wait states on all accesses to the board. Normally, this bit should be set to ' 1' by software so as not to unnecessarily deteriorate the performance.

This feature may be used to help prevent problems in AT clones and compatibles that have bus speeds above 8.33 Mhz. Software should provide a configuration mechanism so that the bit may remain inactive in problem systems. Writes to this field are glitch-free.

Automatic wait mechanism

Some devices decoded by ATLAS do not require any additional wait states. An automatic wait mechanism has been implemented in ATLAS for the case of devices that may not follow the speed of some rapid systems.

When the automatic wait is required (**nowait** = 'O'), the bus will be put into wait for an equivalent time of 100 ns to 125 ns when an access to some devices is decoded.

These devices are:

. Drawing registers (read and write to offset range 1C00h - 1DFFh)

- Host registers (read and write to offset range 1E00h - 1EFFh)
- Pseudo-DMA window (read and write to offset range OOOOh - 1BFFh, with vgaen = 0 and pseudodma = 1)
- VRAM direct write (write to offset range OOOOh - 1BFFh, with vgaen = 0 and pseudodma = 0)

Note: Some devices do not use automatic wait because they're already using wait states in normal operation. These devices are:

- BIOS ROM
- VRAM direct read
- VGA frame buffer read and write
- External devices read and write, I/O or memory
- VGA register in the Power Graphic mode memory space (read and write to offset range 1F00h - 1FFFh, with vgaen = 0)

Reserved <7:5>

Reserved: Writing has no effect. These bits return all zeroes when read.

mouseen <8> *R/W*

MOUSE ENable: When set to ' 1' , this bit enables mouse decode for the DUBIC chip. The **mousemap** field should be programmed at the same time as this field, so the appropriate map will be selected when the decode is enabled.

This field should be written to only when necessary. When written, it may glitch or pass through an intermediate value, even when rewriting the same value.

mousemap <9> R/W

MOUSE MAR: When **mouseen** is active ('1') and mousemap=O, the mouse port is decoded in I/O space at **23Ch-23Fh.**

When **mouseen** is active and mousemap=l, the mouse port is decoded in I/O space at **238h-23Bh.**

This field should be written to only when necessary. When written, it may glitch or pass through an intermediate value, even when rewriting the same value.

Reserved <10>

Reserved: Writing has no effect. These bits return all zeroes when read.

vgabank0 <11> R/W

VGA BANK 0: Sampled on hard reset, this bit assumes the external strapping configuration value.

During hard reset, the control signal derived from this register bit is forced to guarantee the reset path to the VGA straps which come from the vd bus.

This field should be written to only when necessary. When written, it may glitch or pass through an intermediate value, even when rewriting the same value. When fbm = 3, **vbank0** should be set to 0 (Bank 2).

Value	*Meaning*
0	Boot in Bank 2
1	Boot in Bank 0

Refer to Section 3.6.3 to determine the reset value of this bit.

Reserved <15:12>

Reserved: Writing has no effect. These bits return all zeroes when read.

rfhcnt <19:16> R/W

ReFresH CouNTer: This field defines the rate of VRAM/DRAM refresh requests.

Program (round the fraction to the nearest integer):

rfhcnt = RAM refresh period uS x clock-frequency Mhz / 64.

For a typical 40Mhz system, a value of 9 is programmed in xfhcnt.

rfhcnt = 15.625 uS x 40 Mhz / 64.

During the reset period, the refresh request is continuously forced to its inactive state so that no VRAM activities will occur. By maintaining the reset low for 200 uS, a proper VRAM initialisation will occur (valid for power up or after a VRAM error).

Writes to this field are glitch-free.

fbm <22:20> R/W

Frame Buffer Mode: This field specifies the mode used to draw in the frame buffer. The modes are used to generate all **xRAM** control strobes and addresses. For more information about frame buffer mode, refer to Section 3.2.1.

Writes to this field are glitch-free.

Reserved <23>

Reserved: Writing has no effect. These bits return all zeroes when read.

hyperpg <25:24> R/W

HYPER PaGe: On power up, software must read the external strapping value in the destination register (DST1), and set this bit accordingly.

hyperpg<1:0>		
dmaMod<1:0>	*Mnemonic*	*Operation*
00	NOHYPER	NO HYPER-PAGE (default)
01	SELHYPER	HYPER-PAGE on 256K×8 SECTIONS (Bank = 2, 3, 4)
10	ALLHYPER	ALL HYPER-PAGE
11	–	Reserved

This field should be written to only when necessary. When written, it may glitch or pass through an intermediate value, even when rewriting the same value. Writing this field may cause spurious errors. It should only be written during the product configuration process.

These bits are read from VD<52:51> during reset. Software must read these bits from DST1<20:19> and load them here.

tram <26> R/W

Type of VRAM: The tram field is used by the CRTC for data transfer request generation. Specifies the type of 256K×? VRAM used for Banks 2, 3, and 4 (note that all banks should have the same type of VRAM). On power up, software must read the external strapping value in the destination registers (DSTO, DST1), and set this bit accordingly.

This field should be written to only when necessary. When written, it may glitch or pass through an intermediate value, even when rewriting the same value. Writing this field may cause spurious errors. It should only be written during the product configuration process.

Value	*Meaning*
0	256K x 16 (SAM = 256)
1	256K x 4 or 256K x 8 (SAM = 512)

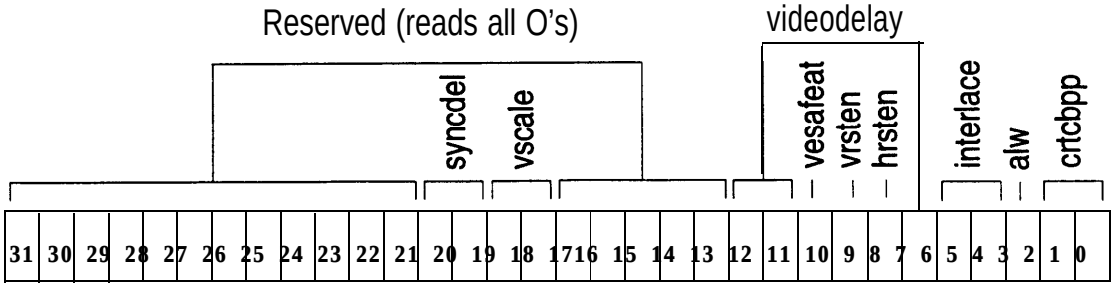
Read from VD<54> during reset. Software must read this bit from DST1<22>, invert it, then load it here.

Reserved <31:27>

Reserved: Writing has no effect. These bits return all zeroes when read.

Memory Address 1E5C (MEM) **Attributes** **R/W** - STATIC

Reset Value 0000 0000 0000 0000 0000 0000 0000 0000b



crtcbpp <1:0> CRTC Bits Per Pixel: Specifies the number of bits per pixel for the video. Writes to this field are glitch-free.

crtcbpp	*Number of bits*
00	***8***
01	16
10	32
11	Reserved

alw <2> Automatic Line Wrap: Specifies that the video is in automatic line wrap. If set to 0, the video is in non-automatic line wrap. If set to 1, the video is in automatic line wrap. Writes to this field are glitch-free.

interlace <4:3> INTERLACE: Indicates interlace mode and pitch. Writes to this field are glitch-free.

interlace<1:0>	*Mode*
00	Non interlaced
01	Interlace : pitch = 768 (768 and 640)
10	Interlace : pitch = 1024 (800 and 1024)
11	Interlace : pitch = 1280 (1280)

videodelay <10,9,5> VIDEO DELAY: Specifies the delay in the dtrequest module between the CRTC signals and the delayed signals sent to the VCTL. The delay must respect three constraints which are described at the end of Section 3.2.5.5. Writes to this field are glitch-free.

videodelay<2:0>	*Delay*
000	5 vidclk
001	11 vidclk
010	24 vidclk
011	28 vidclk
100	3 vidclk
101	4 vidclk
11x	Reserved

hrsten <6> HoRizontal video ReSeT ENable: When set to 1, the horizontal counter of the CRTC can be reset by the VIDRST pin.

This field should be written to only when necessary. When written, it may glitch or pass through an intermediate value, even when rewriting the same value.

vrsten <7> Vertical video ReSeT ENable: When set to 1, the vertical counter of the CRTC can be reset by the VIDRST pin.

This field should be written to only when necessary. When written, it may glitch or pass through an intermediate value, even when rewriting the same value.

vesafeat <8> Activates the extra memory page select bit. Used in VGA mode by the VESA driver to reduce the first memory access window from 64K to 32K.

This field should be written to only when necessary. When written, it may glitch or pass through an intermediate value, even when rewriting the same value.

vscale <17:16> Video clock pre-SCALing:

These bits are used to specify a pre-scaling factor to the clock that is sent to the CRTC. Writes to this field are glitch-free.

nodubic	*vgaen*	*vscale*	*Clock divide ration*
0	X	XX	1 (bypass)
1	0	00	1 (bypass)
		01	2
		10	4
		11	8
	1	XX	1 (bypass)

syncdel <19:18> SYNC DELay: These bits specify the delay that is to be added to the horizontal and vertical sync. The syncdel field has no effect when a DUBIC chip is present, since HSYNC/ and VSYNC/ are not generated by ATLAS. Writes to this field are glitch-free.

vgaen	*syncdel*	*Delay added to HSYNC/ and VSYNC/*
0	*X*	1 (bypass)
1	0	1 (bypass)
		2
		4
		8
	1	1 (bypass)

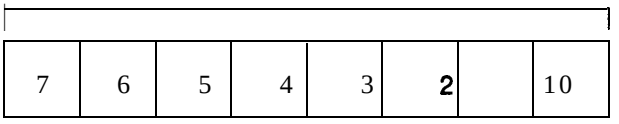
Reserved <31:20, 15: 11> Reserved: Writing has no effect. These bits return all zeroes when read.

5.3 VGA Mode Register Descriptions

CRTC Address **(CRT Controller Register)**

Memory Address Mono 1FB4 Color 1FD4 **I/O Address** Mono 3B4 Color 3D4

CRTC register index address 7:0

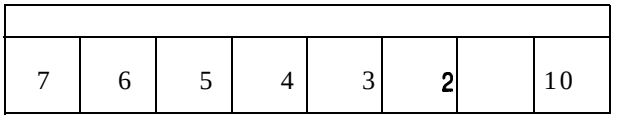


D7-D0 CRTC Register Index Address
These bits select which CRTC register is to be accessed.

Horizontal Total **(CRT Controller Registers)**

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 00

Horizontal total 7:0

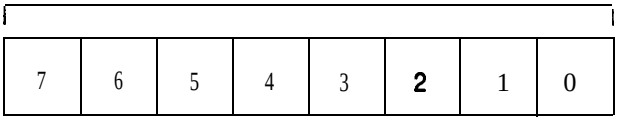


D7-D0 Horizontal Total
These bits define the total number of characters, minus five, in the horizontal scan interval including retrace time. The horizontal period is $T_H = (R0+5) \times T_C$; where RO is the contents of this register, and T_C is the period of the input character clock.

Horizontal Display Enable End **(CRT Controller Registers)**

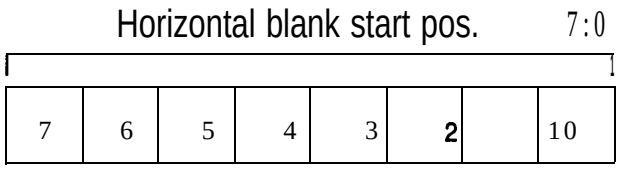
Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** *01*

Horizontal displayed characters 7:0



D7-D0 Horizontal Displayed Characters
These bits define the length of the horizontal display period. This period is equal to $(R1+1) \times T_C$; where R1 is the contents of this register, T_C is the period of the input character clock, and providing R1 is less than RO.

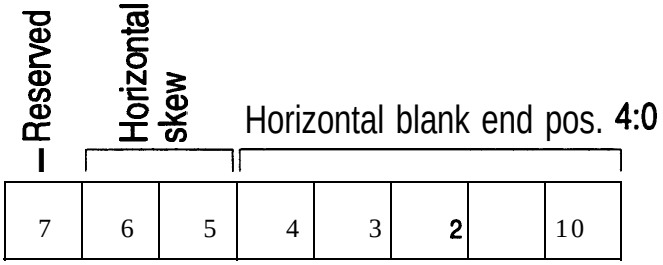
Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 02



D7-D0 Horizontal Blank Start Position

The value of this register determines when the horizontal component of the blanking signal becomes active. This component goes high at time (R2+1) x Tc after the start of a horizontal cycle; where R2 is the contents of this register, Tc is the period of the input character clock, and providing R2 is less than RO.

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 0 3



D6-D5 Horizontal Skew Bits 1 And 0

These bits determine the skew of the display enable signal as follows:

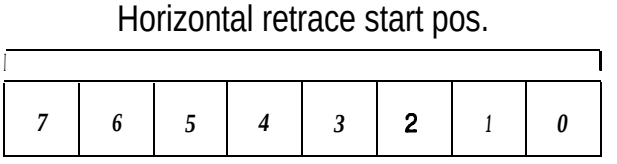
D6	*D5*	*Disable Enable Skew*
0	0	Display enable is not delayed
0	1	Display enable delayed by one character clock
1	0	Display enable delayed by two character clocks
1	1	Display enable delayed by three character clocks

D4-D0 Horizontal Blank End Position Bits 4 To 0

These five bits are the least significant bits of a six-bit total which determines the length of the active horizontal blanking signal. The sixth bit is located at D7 of the horizontal retrace end (Index 05h) register. Horizontal blank end occurs at (using 8-bit math) R2+{ [(Horizontal blank end value AND 3Fh) - (R2 AND 3Fh)] AND 7Fh}.

Horizontal Retrace Start (CRT Controller Registers)

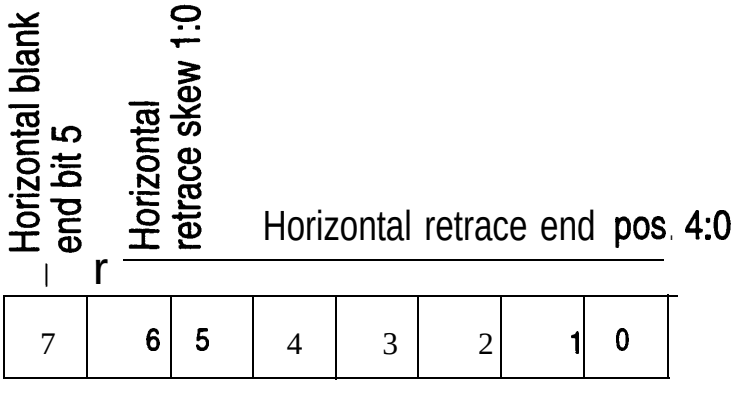
Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 04



D7-D0 Horizontal Retrace Start Position Bits
The value of these bits determines when the horizontal retrace will start.

Horizontal Retrace End (CRT Controller Registers)

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 05



D7 Horizontal Blank End Position Bit 5
This is the horizontal blank end position MSB. The first five bits are in the horizontal blanking end register (Index 03h).

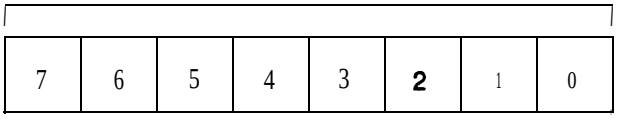
D6-D5 Horizontal Retrace Skew Bits 1 And 0
These bits determine the skew of the horizontal retrace signal as follows:

D6	D5	Horizontal Retrace Skew
0	0	Horizontal retrace is not delayed
0	1	Horizontal retrace delayed by one character clock
1	0	Horizontal retrace delayed by two character clocks
1	1	Horizontal retrace delayed by three character clocks

D4-D0 Horizontal Retrace End Position Bits 4 To 0
These bits determine the length of the active horizontal retrace signal. The horizontal retrace end position occurs at (using 8-bit math) R4+{[(R5 AND 1Fh) - (R4 AND 1Fh)] AND 3Fh}

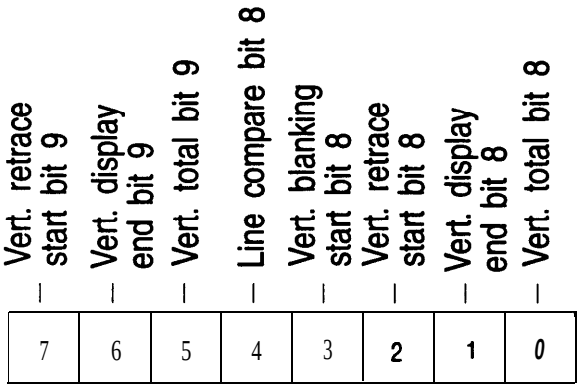
Memory Address Mono 1FB5 Color 1FD5 **I/O** Address Mono 3B5 Color 3D5 Index 06

Vertical total 7:0



D7-D0 Vertical Total Bits 7 To 0
These are the low-order eight-bits of the ten-bit vertical total. Bits eight and nine are located in the ovefflow register (Index 07h). Vertical total = Vertical total value+2.

Memory Address Mono 1FB5 Color 1FD5 **I/O** Address Mono 3B5 Color 3D5 **Index** 0 7



D7 Vertical Retrace Start Bit 9: This is bit nine, the MSB of the vertical retrace start register (Index 10h). This bit is reserved in EGA mode.

D6 Vertical Display End Bit 9: This is bit nine, the MSB of the vertical display enable end register (Index 12h). This bit is reserved in EGA mode.

D5 Vertical Total Bit 9: This is bit nine, the MSB of the vertical total register (Index 06h). This bit is reserved in EGA mode.

D4 Line Compare Bit 8: This is bit eight of the line compare register (Index 18h).

D3 Vertical Blanking Start Bit 8: This is bit eight of the vertical blanking start register (Index 15h).

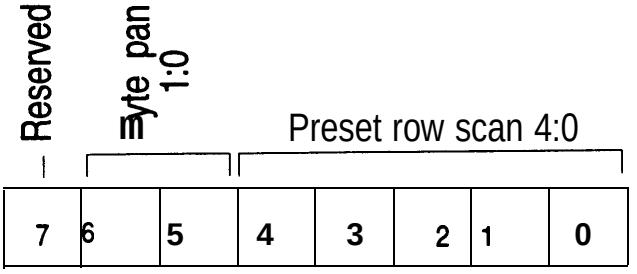
D2 Vertical Retrace Start Bit 8: This is bit eight of the vertical retrace start register (Index 10h).

D1 Vertical Display End Bit 8: This is bit eight of the vertical display enable end register (Index 12h).

D0 Vertical Total Bit 8: This is bit eight of the vertical total register (Index 06h).

Preset Row Scan (CRT Controller Regisr

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 08

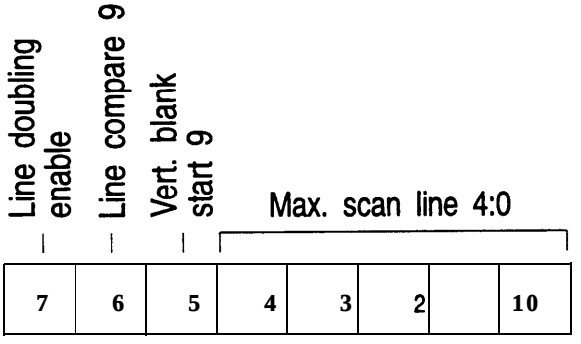


D6-D5 Byte Pan Bits 1 And 0
These bits control the byte panning in modes programmed as multiple shift modes.

D4-D0 Preset Row Scan Bits 4 To 0
The value of these bits is the first row value at the start of a vertical period.

Maximum Scan Line (CRT Controller Registers)

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 09



D7 Line Doubling Enable: This bit is reserved in EGA mode.

. 0: Disables double scan.

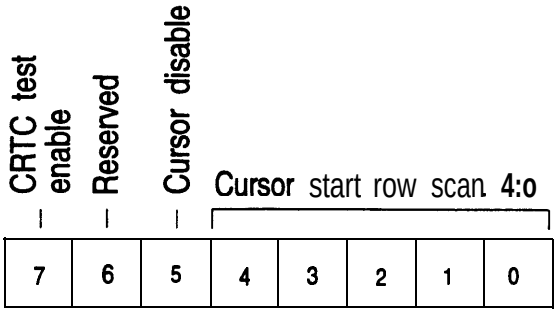
■ 1: Enables double scan.

D6 Line Compare Bit 9
This is bit nine, the MSB of the line compare register (Index 18h). This bit is reserved in EGA mode.

D5 Vertical Blanking Start Bit 9
This is bit nine, the MSB of the vertical blanking start register (Index 15h). This bit is reserved in EGA mode.

D4-D0 Maximum Scan Line Bits 4 To 0
These bits specify the number of scan lines in a character row.

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** O A



D7 CRTC Test Enable

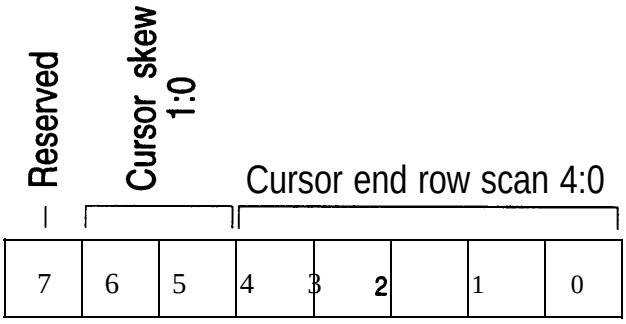
- 0: Disables the CRT test circuitry.
- 1: Enables the CRT test circuitry if bit D7 of the extended function register, 3DFh Index 01, is also 1.

D5 Cursor Disable. This bit is reserved in EGA mode.

- 0: Turns the cursor on.
- 1: Turns the cursor off.

D4-D0 Cursor Start Row Scan Bits 4 To 0
These bits specify the row scan of a character line where the cursor is to begin.

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** O B



D6-D5 Cursor Skew Bits 1 And 0
These bits determine the skew of the cursor signal as follows:

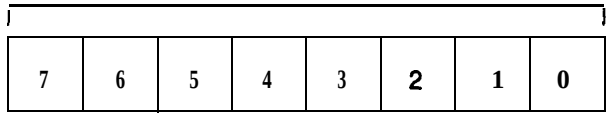
D6	*D5*	*Cursor Skew*
0	0	Cursor signal is not delayed
0	1	Cursor signal delayed by one character clock
1	0	Cursor signal delayed by two character clocks
1	1	Cursor signal delayed by three character clocks

D4-D0 Cursor End Row Scan Bits 4 To 0
These bits specify the row scan of a character line where the cursor is to end.

Start Address High (CRT Controller Registers)

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** oc

Start address 15:8

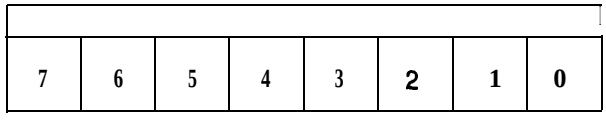


D7-D0 Start Address Bits 15 To 8
These are the eight MSB's of the 16-bit start address of the screen buffer.

Start Address Low (CRT Controller Registers)

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 0D

Start address 7 : 0

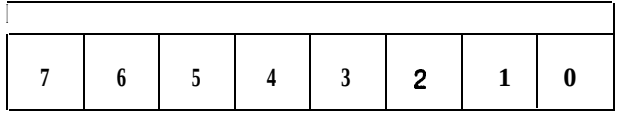


D7-D0 Start Address Low Bits 7 To 0
These are the eight LSB's of the 16-bit start address of the screen buffer.

Cursor Position High (CRT Controller Registers)

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** O E

Cursor address 15:8



D7-D0 Cursor Address Bits 15 To 8
These are the eight MSB's of the 16-bit address of the cursor location in memory.

(CRT Controller Registers) Cursor Position Low

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** O F

Cursor address **7 : 0**

7	**6**	**5**	**4**	**3**	**2**		**10**

D7-D0 Cursor Address Low Bits 7 To 0
These are the eight LSB's of the 16-bit address of the cursor location in memory.

(CRT Controller Registers) Vertical Retrace Start

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 10

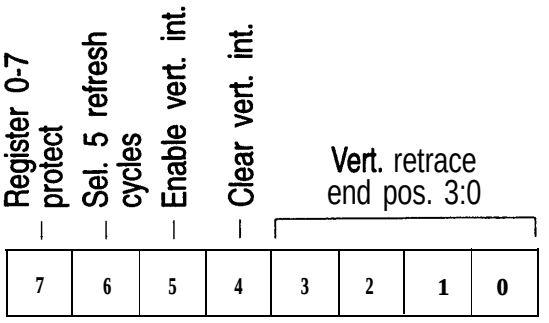
Vertical retrace start pos. **7 : 0**

7	**6**	**5**	**4**	**3**	**2**		**10**

D7-D0 Vertical Retrace Start Position Bits 7 To 0
These are the eight LSB's of the vertical retrace start position, and is programmed in horizontal scan lines. Bits eight and nine are in the overflow register (Index 07h).

Vertical Retrace End (CRT Controller Registers)

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 11



D7 Register 7-O Protect. This bit is reserved in EGA mode.

. 0: Enables the writing of data to CRTC registers 7 To 0.

. 1: Disables the writing of data to CRTC registers 7 To 0.

D6 Select 5 Refresh Cycles. This bit is reserved in EGA mode.

. 0: Allows three dynamic RAM refresh cycles per horizontal line.

. 1: Allows five dynamic RAM refresh cycles to be generated in every horizontal line.

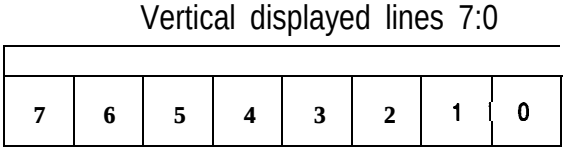
D5 Enable Vertical Interrupt
D5=0 enables the vertical retrace interrupt.

D4 Clear Vertical Interrupt
D4=0 clears the vertical retrace interrupt. After being cleared this bit must be set to 1 so that interrupts are not held inactive.

D3-D0 Vertical Retrace End Position Bits 3 To 0
These bits determine the length of the vertical retrace signal. Since this value is only four bits in length, The maximum length of the vertical retrace signal is 15 clock periods.

Vertical Display Enable End (CRT Controller Registers)

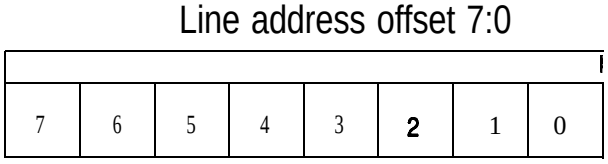
Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 12



D7-D0 Vertical Displayed Lines Bits 7 To 0
These are the least significant eight bits of the ten-bit value which defines the vertical display enable end position. The value of these ten bits is the total number of lines to be displayed minus one.

(CRT Controller Registers) Offset

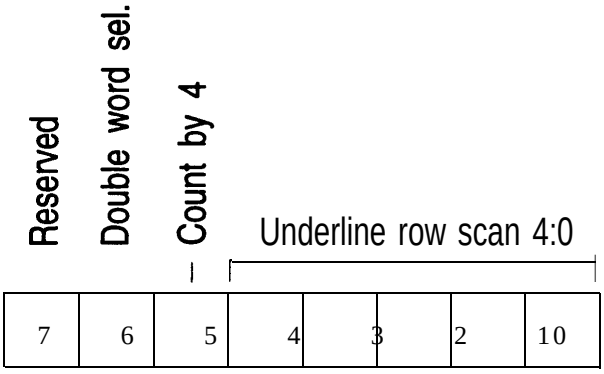
Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 1 3



D7-D0 Line Address Offset Double Words
These bits are the value used to offset the memory address counter to the begining of the next displayed character line. This value is the number of double words (or single words) in one character line.

(CRT Controller Registers) Underline Location

Memory Address Mono 1FB5 Color lFD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 1 4



D6 Double Word Select. This bit is reserved in EGA mode.

- 0: Causes the memory addresses to be single word addresses.
- 1: Causes the memory addresses to be double word addresses.

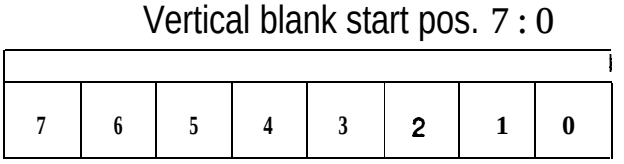
D5 Count By four. This bit is reserved in EGA mode.

- 0: Causes the memory address counter to be clocked with the character clock.
- 1: Causes the memory address counter to be clocked with the character clock divided by four. If the count by two bit (Index 17h bit D3) is set to 1, then this bit has no effect.

D4-D0 Underline Row Scan Bits 4 To 0
These bits specify the horizontal row scan of a character row on which an underline occurs.

Vertical Blanking Start (CRT Controller Registers)

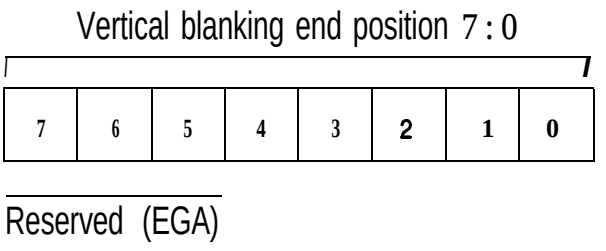
Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 15



D7-D0 Vertical Blanking Start Position Bits 7 To 0
These are the least significant eight bits of the ten-bit start vertical blanking value. Bits eight and nine are found in the overflow register (Index 07h) and the maximum scan line register (Index 09h). The value of these ten bits is one less than the horizontal scan line count at which the vertical blanking signal becomes active.

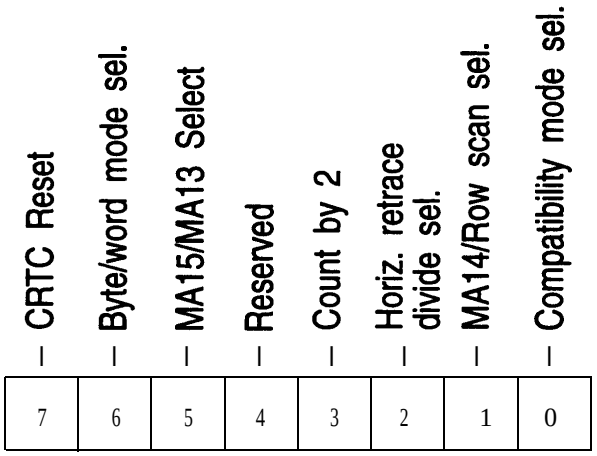
Vertical Blanking End (CRT Controller Registers)

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 16



D7-D0 Vertical Blanking End Position Bits 7 To 0
The value of these bits specify the horizontal scan count when the vertical blanking signal becomes inactive. This value is in horizontal scan lines.

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 17



D7 CRTC Reset

- 0: Clears both the horizontal and vertical retrace.
- 1: Enables both the horizontal and vertical retrace.

D6 **Byte/Word** Mode Select

- 0: Selects word mode. The memory address counter bits are shifted left before being applied to the video memory. Address bit 0 is replaced with either bit 15 or bit 13 of the memory address counter, as selected by the MA **15/MA13** select bit
- 1: Selects the byte mode. The memory address counter bits are applied directly to the video memory.

D5 MA **15/MA13** Select

- 0: Selects memory address counter bit 13 to be used as memory address bit 0 in word mode. In byte mode, memory address counter bit 0 is used for memory address bit 0.
- 1: Selects memory address counter bit 15 to be used as memory address bit 0 in word mode. In byte mode, memory address counter bit 0 is used for memory address bit 0.

D3 Count By Two

- 0: Causes the memory address counter to be clocked by the character clock.
- 1: Causes the memory address counter to be clocked by every second character clock.

D2 Horizontal Retrace Divide Select

- 0: Causes the vertical timing counter to be clocked on every horizontal retrace. The maximum number of horizontal scan lines is 1024.
- 1: Causes the vertical timing counter to be clocked by every second horizontal retrace. The maximum number of horizontal scan lines is 2048.

D1 **MA14/Row** Scan Select

This bit is used to select the internal signal used for memory address 14.

. 0: Causes the row scan counter bit 1 to be used as memory address bit 14 during CRTC reads from display memory.

■ 1: Causes memory address bit 14 to be used as memory address bit 14 during CRTC reads from display memory.

DO Compatability Mode Select

This bit is used for compatibility with IBM CGA.

■ 0: Causes the row scan address bit 0 to be used as memory address bit 13 during CRTC reads from display memory.

. 1: Causes memory address counter bit 13 to be used as memory address bit 13 during CRTC reads from display memory.

Line Compare (CRT Controller Registers)

Memory Address Mono 1FB5 Color lFD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 1 8

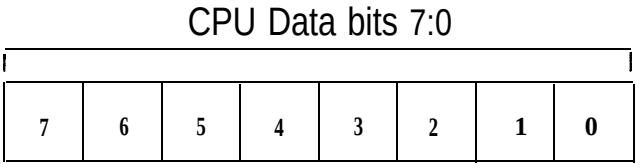
Line Compare 7:0

7	6	5	4	3	2	1	0

D7-D0 Line Compare Bits 7 To 0

These are the eight least significant bits of the ten-bit line compare value. When the number of displayed lines reaches this value, the display memory address is reset following two horizontal lines. Bit eight and bit nine are in the overflow register (Index 07h) and the maximum scan line register (Index 09h).

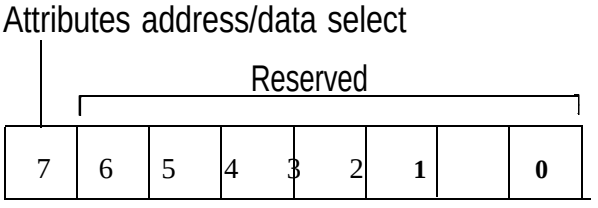
Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 2 2



D7-D0 CPU Data Bits 7 To 0

This register reads one of four 8-bit registers of the graphics controller CPU data latch. These latches are loaded when the CPU reads from display memory. Bits 1 and 0 of graphics controller register Index 04h (read plane select) determine which of the four latches (planes O-3) is read. This register contains color compare data in mode 1.

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 2 4



D7 Attributes Address/Data Select:

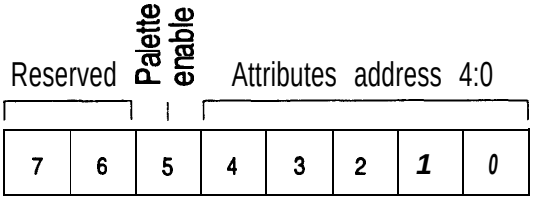
. 0: Indicates the attributes controller is prepared to accept an address value.

- 1: Indicates the attributes controller is prepared to accept a data value.

A read from port 1FBA/1FDAh resets D7. Each data write to the attributes controller will toggle this bit.

Attributes Address (CRT Controller Register)

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** 2 6

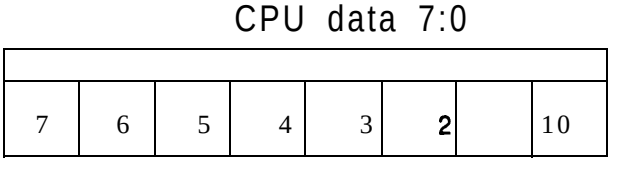


D5 Palette Enable

D4-D0 Attributes Address Bits 4 To 0:
These bits return the value of the attributes controller address register.

Graphics Controller CPU Data Latch, Map 0 (CRT Controller Registers)

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** E O

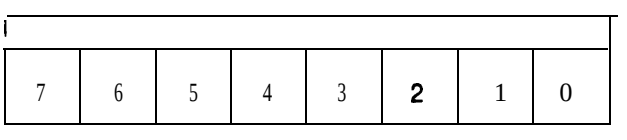


D7-D0 CPU Data Bits 7 To 0
This register contains the data which is to be written to, or has been read from the 8-bit register for plane 0 of the graphics controller CPU data latch.

After this register is accessed, the index will automatically increment to El.

Graphics Controller CPU Data Latch, Map 1 (CRT Controller Registers)

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** E l



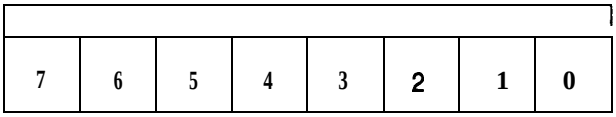
D7-D0 CPU Data Bits 7 To 0
This register contains the data which is to be written to, or has been read from the 8-bit register for plane 1 of the graphics controller CPU data latch.

After this register is accessed, the index will automatically increment to E2.

(CRT Controller Registers) Graphics Controller CPU Data Latch, Map 2

Memory Address Mono 1FB5 Color lFD5 **I/O Address** Mono 3B5 Color 3D5 **Index** E 2

CPU data 7:0



D7-D0 CPU Data Bits 7 To 0

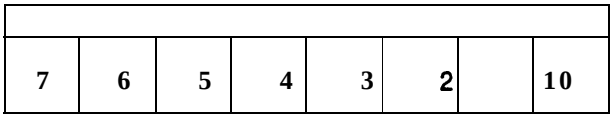
This register contains the data which is to be written to, or has been read from the 8-bit register for plane 2 of the graphics controller CPU data latch.

After this register is accessed, the index will automatically increment to E3.

(CRT Controller Registers) Graphics Controller CPU Data Latch, Map 3

Memory Address Mono 1FB5 Color 1FD5 **I/O Address** Mono 3B5 Color 3D5 **Index** E 3

CPU data 7:0

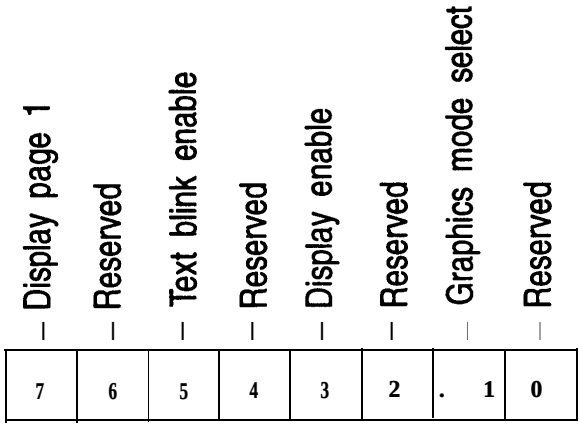


D7-D0 CPU Data Bits 7 To 0

This register contains the data which is to be written to, or has been read from the 8-bit register for plane 3 of the graphics controller CPU data latch.

After this register is accessed, the index will automatically increment to EO.

Memory Address 1FB8 **I/O Address** 3B8



D7 Display Page 1

. 0: Causes memory page 0 (B0000-B7FFFh) to be displayed.

■ 1: Causes memory page 1 (B8000-BFFFFh) to be displayed. Bit D1 of the configuration register (3BFh) must be high before this bit can be set.

D5 Text Blink Enable

. 0: Causes attribute bit 7 to be used for background intensity in text mode.

■ 1: Causes all characters with attribute bit 7 high to blink and all characters to have low background intensity.

D3 Display Enable

■ 0: Blanks the display.

. 1: Enables the display. Bit D5 of auxiliary register 2 (emulation control) must be 1 before the display can be blanked.

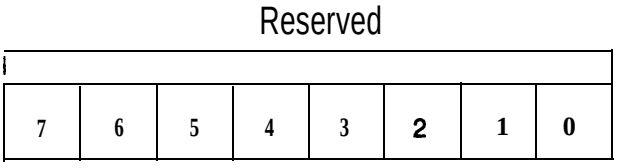
D1 Graphics Mode Select

■ 0: Selects text mode.

■ 1: Selects graphics mode. This bit can be set only if DO of the configuration register (3BFh) is 1.

(Hercules Registers) Light Pen Set

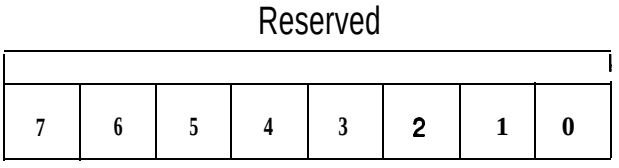
Memory Address 1FB9 **I/O Address** 3B9



When this port is read from or written to the light pen latch is set.

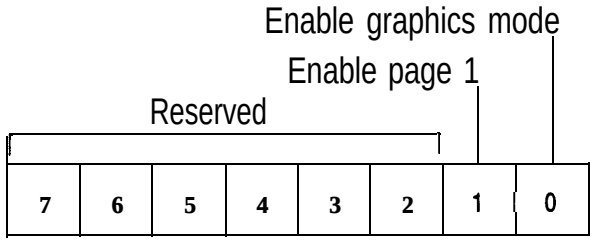
(Hercules Registers) Light Pen Clear

Memory Address 1FBB **I/O Address** 3BB



When this port is read from or written to the light pen latch is cleared.

Memory Address 1FBF **I/O Address** 3BF



D1 Enable Page 1

- 0: Prevents D7 of the mode control register (3B8h) from being set.
- 1: Allows D7 of 3B8h to be set. The logical AND of this bit and data bus D7 is applied to the bit 7 latch of the mode control port.

D1=0 causes the display memory to appear in the BOOOO-B7FFFh CPU address range. In text mode, the memory is actually only 4K in size and is repeated (B 1000-B 1 FFFh, B2000-B2FFFh, etc. are the same memory as B0000-B0FFFh). D1=1 allows 64K of unique memory to be accessed in the B0000-BFFFFh range.

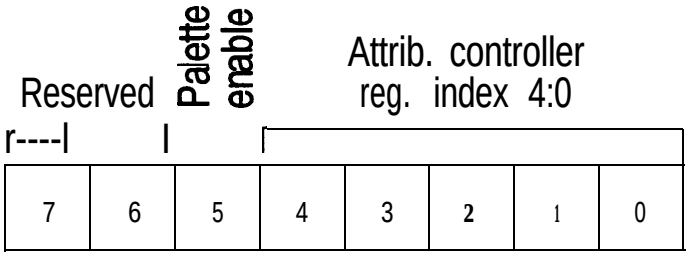
When in graphics mode, 64K of unique memory is always available. The CPU can access the upper 32K (B8000-BFFFFh) only when D1=1.

DO Enable Graphics Mode

- 0: Prevents D1 of 3B8h from being set.
- 1: Allows D1 of the mode control register (3B8h) to be set.

The logical AND of this bit and data bus D1 is applied to the bit 1 latch of the mode control port.

Memory Address 1FC0 **I/O Address** 3C0



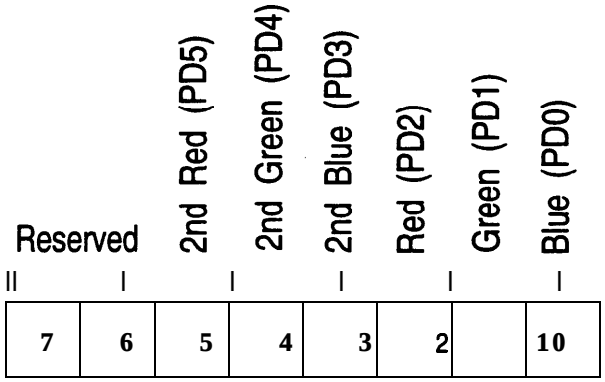
A read from port 3BA/3DAh resets this port to the attributes address register. The first read or write to this register after a 3BA/3DAh reset accesses the attributes index, the next read or write accesses the palette. Subsequent reads or writes to this register toggle between index and palette.

D5 Palette Enable

- 0: Enables the loading of the palette registers. The display is forced to the overscan color.
- 1: Enables the application of video pixel data to the color palette address inputs.

D4-D0 Attributes Controller Register Index Address Bits 4 To 0
Bits D4-D0 of this register select which attributes register is to be accessed at 03Clh.

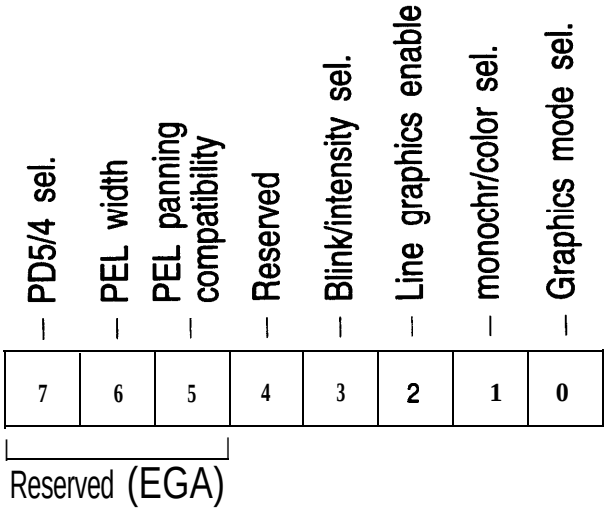
Memory Address Read 1FC1 Write 1FC0 **I/O Address** Read 3C1 Write 3C0 **Index** 00-OF



There are 16 palette registers. Each of these registers corresponds to one possible combination of the four video plane inputs to the attributes controller system.

Bits D5-D0 allow a dynamic mapping of text attribute or graphic color input value for the displayed color. The value of these six bits determine the color to be displayed.

Memory Address Read 1FC1 Write 1FC0 **I/O Address** Read 3C1 write 3C0 **Index** 10



D7 PD5/4 Select

. 0: Enables PD5 and PD4 to become the outputs of the palette registers.

. 1: Causes PD5 and PD4 to be used as bits 0 and 1 of the color select register.

D6 PEL Width

. 1: Causes the video pipeline to be sampled such that eight bits are available for color selection in the 256-color mode.

- 0: This bit should be 0 in all other modes.

D5 PEL Panning Compatibility

. 0: Has no effect on the output of the PEL panning register.

- 1: Causes a successful line compare in the CRT controller to force the output of the of the horizontal panning register to 0 until "+VSYNC" becomes active. The output then returns to its programmed value. This bit allows the panning of only the top portion of the display.

D3 Blink/Intensity Select

. 0: Selects the use of bit D7 of the character attribute to be used for the background intensity.

- 1: Selects the use of bit D7 of the character attribute to be used for blink. This bit is also 1 to enable blinking in graphics modes.

D2 Line Graphics Enable

. 0: Causes the ninth horizontal bit position of a displayed character cell to be the same color as the background.

- 1: Causes the ninth horizontal bit position of a displayed character cell to be the same as the eighth bit position if the character code being displayed is between 0C0h and 0DFh.

D1 Monochrome/Color Select

. 0: Selects color display attributes.

- 1: Selects monochrome display attributes.

DO Graphics Mode Select

. 0: Selects the alphanumeric mode.

- 1: Selects the graphics mode.

(Attributes Controller Registers) Overscan Color

Memory Address Read 1FC1 Write 1FC0 **I/O Address** Read 3C1 Write 3C0 **Index** 11

Overscan PD7:0

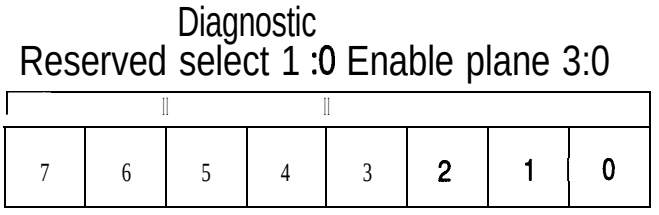
7	6	5	4	3	2	1	0

Resewed (EGA)

D7-D0 Overscan PD7 To PDO: These eight bits determine the border color of the CRT display.

Color Plane Enable (Attributes Controller Registers)

Memory Address Read 1FC1 Write 1FC0 **I/O Address** Read 3C1 Write 3C0 **Index** 12



D5-D4 Diagnostic Select Bits 1 And 0

These bits select two of eight color outputs for the status port (see ports 3BAh, 3DAh bits D4 and D5) as follows:

Diagnostic Select		*Status Port*	
D5	*D4*	*D5*	*D4*
0	0	PD2	PD0
0	1	PD5	PD4
1	0	PD3	PD1
1	1	PD7	PD6

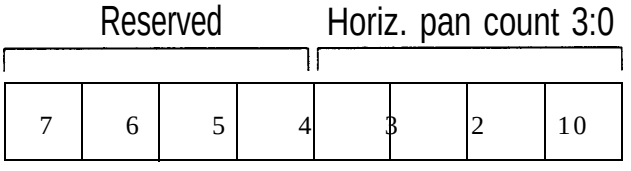
D3-D0 Enable Planes 3 To 0

. 0: Disables the corresponding memory plane.

- 1: Enables the corresponding memory plane.

Horizontal Panning (Attributes Controller Registers)

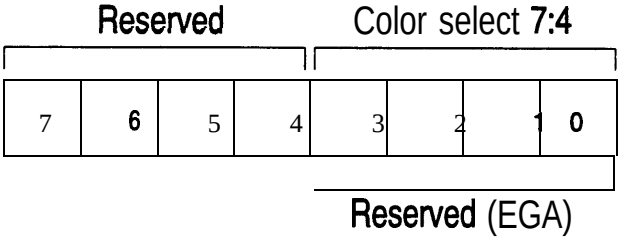
Memory Address Read 1FC1 Write 1FC0 **I/O Address** Read 3C1 Write 3C0 **Index** 13



D3-D0 Horizontal Pan Count Bits 3 To 0

These bits are used for horizontal panning. In 8-PELs-per-character modes, this register is normally programmed with the value 0. The displayed image is shifted left by the number of pixels specified using this register. The maximum allowed is seven. In 9-PELs-per-character modes this register is normally programmed with the value of eight. Programming the values zero to seven will shift the display increasingly to the left.

Memory Address Read 1FC1 Write 1FC0 **I/O Address** Read 3C1 Write 3C0 **Index** 14

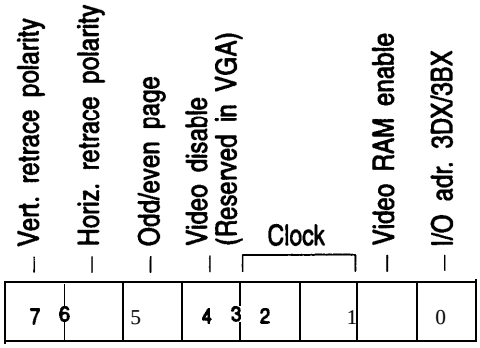


D3-D2 Color Select Bits 7 And 6
These bits are the two most significant bits of the eight-bit color value in all modes except 256-color graphics.

D1-D0 Color Select Bits 5 And 4
These bits can be used in place of the PD5 and PD4 outputs from the palette registers to form the eight-bit color value.

Memory Address Read 1FCC Write 1FC2
Write EGA 1FC3

I/O Address Read 3CC Write 3C2
Write EGA 3C3



D7 Vertical Retrace Polarity Select

. 0: Selects positive vertical retrace.

■ 1: Selects negative vertical retrace.

D6 Horizontal Retrace Polarity Select

- 0: Selects positive horizontal retrace.
- 1: Selects negative horizontal retrace.

D5 Odd/Even Page Select
This bit selects between two 64K pages of memory when in the Odd/Even mode.

■ 0: Selects the low page of RAM.

. 1: Selects the high page of RAM.

D4 Video Disable (EGA mode only)

- 0: Activates internal video drivers.
- 1: Deactivates the internal video drivers.

D3-D2 Clock Select Bits 1 And 0
Bits D3 and D2 select the clock source as dictated by Auxiliary register 01, D6. See Auxiliary register 01, D6 for further details.

D1 Video RAM Enable

. 0: Disables the video RAM.

- 1: Enables the video RAM at the address set by the Graphics Controller Miscellaneous register, Index 6, bits D2 and D3.

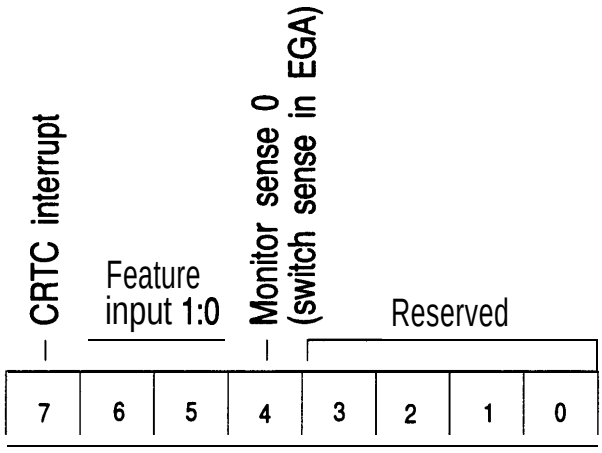
DO I/O Address 3DX/3BXh Select

. 0: Sets the CRT controller address to 3BXh and the input status register 1 address to 3BAh for monochrome adapter emulation. The second video RAM window, when enabled, is accessable from B0000h to B7FFFh.

- 1: Sets the CRT controller address to 3DXh and the input status register 1 address to 3DAh for CGA emulation. The second video RAM window, when enabled, is accessable from B8000h to BFFFFh.

Memory Address 1FC2
EGA 1FC3

I/O Address 3C2
EGA 3C3



D7 CRTC Interrupt
D7=1 signifies that a CRTC interrupt is pending. The interrupt is cleared when this bit is set to 0.

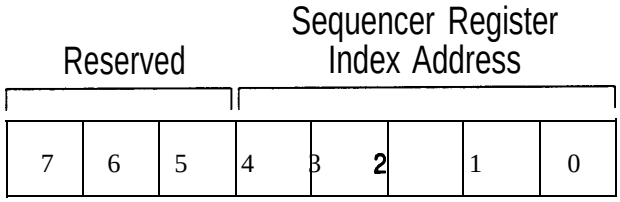
D6-D5 Feature Input 1 And 0
These bits are always read as "11".

D4 Monitor Sense 0 (Switch Sense in EGA mode)
In VGA mode, D4 is always read as 1. In EGA mode, the value read depends on bits D3:D2 of the Misc. Output register.

D3:D2	*D4*
00	1
01	**0**
10	**0**
11	1

Address (Sequencer Registers)

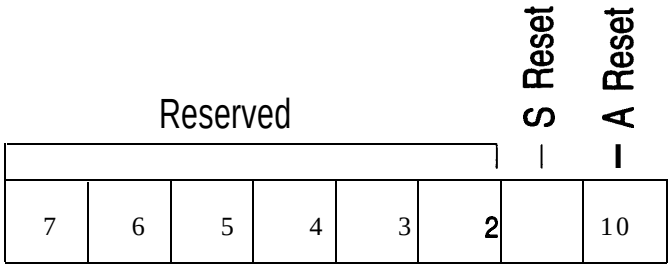
Memory Address 1FC4 **I/O Address** 3C4



D4-D0 Sequencer Register Index Address Bits 4 to 0
The index specified by these address bits indicate the location of the register to which data is being written to or read from.

Reset (Sequencer Registers)

Memory Address 1FC5 **I/O Address** 3C5 **Index** 00



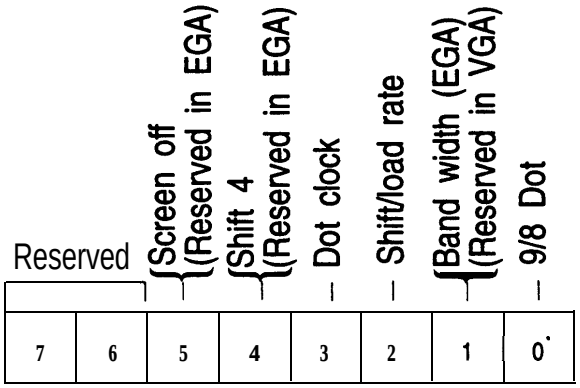
D1 Synchronous Reset

- 0: Clears and stops the sequencer at the end of a memory cycle, and the memory buses are placed in the high impedance state. This bit must be set to 0 before changing any of the following:
  - DO and D3 of 1FC5h Index 01
  - D2 and D3 1FC2h
  - DO, D 1 and D5 of 1FDFh Index 01
  - D3 and D6 of 1FDFh Index 2

DO Asynchronous Reset

- 0: Clears and stops the sequencer at the end of a memory cycle and the DIP switch latch becomes transparent. Resetting the sequencer with this bit can cause the loss of data.

Memory Address 1FC5 **I/O Address** 3C5 **Index** 0 1



D5 Screen Off

- 0: Normal video operation.
- 1: Turns off the video and maximum memory bandwidth is assigned to the system. The display is blanked and all sync pulses are maintained

D4 Shift 4

- 0: Causes the graphics controller shift registers to be reloaded every character clock.
- 1: Causes the graphics controller shift registers to be reloaded on every fourth character clock. This is used for 32-bit fetches.

D3 Dot Clock Rate

- 0: Causes the dot clock rate to be the same as the sequencer clock rate.
- 1: Causes the dot clock rate to be slowed to one-half of the sequencer clock rate. The character clock and shift/load signals are also slowed to half their normal speed.

D2 Shift/Load Rate

- 0: Causes the graphics controller shift registers to be reloaded every character clock.
- 1: Causes the graphics controller shift registers to be reloaded every other character clock. This is used for word fetches.

Dl Band Width (EGA mode only)

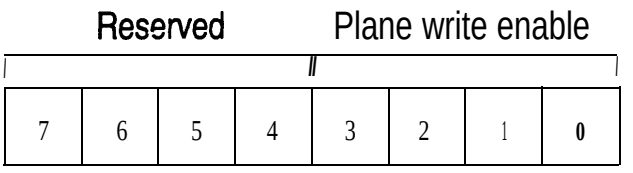
- 0: Causes CRT memory cycles to occur in four of every five sequencer memory cycles.
- 1: Causes CRT memory cycles to occur in two of every five sequencer memory cycles.

DO 9/8 Dot Mode

- 0: Causes the sequencer to generate a 9 dot character clock.
- 1: Causes the sequencer to generate an 8 dot character clock.

Plane Mask (Sequencer Registers)

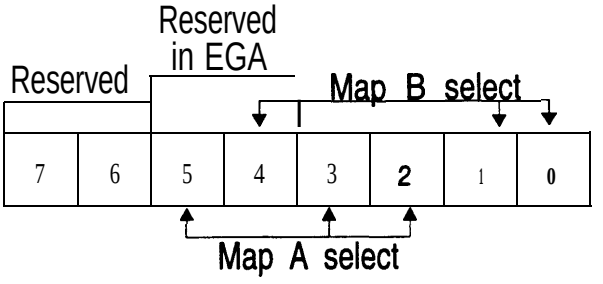
Memory Address 1FC5 **I/O Address** 3C5 **Index** 02



D3-D0 Plane 3, 2, 1 And 0 Write Enable
A 1 in any bit location will enable system writes to the corresponding video memory plane. Simultaneous writes occur when more than one bit is 1.

Character Map Select (Sequencer Registers)

Memory Address 1FC5 **I/O Address** 3C5 **Index** 03



D5, D3-D2 Map A Select Bits 2, 1 And 0: These bits are used for alpha character generation, when character attribute bit D3 is 1, according to the following table:

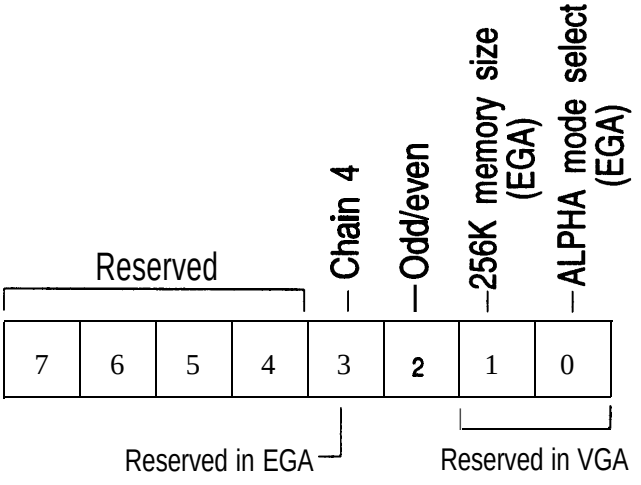
D5	*D3*	*D2*	*Map Selected*	*Map Location*
0	0	0	0	1st 8KB of Plane 2
0	0	1	1	3rd 8KB of Plane 2
0	1	0	2	5th 8KB of Plane 2
0	1	1	3	7th 8KB of Plane 2
1	0	0	4	2nd 8KB of Plane 2
1	0	1	5	4th 8KB of Plane 2
1	1	0	6	6th 8KB of Plane 2
1	1	1	7	8th 8KB of Plane 2

D4, Dl-DO Map B Select Bits 2, 1 And 0

These bits are used for alpha character generation, when character attribute bit D3 is 0, according to the following table:

D4	*D l*	*DO*	*Map Selected*	*Map Location*
0	*0*	*0*	*0*	1st 8KB of Plane 2
0	*0*	1	1	3rd 8KB of Plane 2
0	1	0	2	5th 8KB of Plane 2
0	1	1	3	7th 8KB of Plane 2
1	0	0	*4*	2nd 8KB of Plane 2
1	0	1	*5*	4th 8KB of Plane 2
1	1	0	6	6th 8KB of Plane 2
1	1		7	8th 8KB of Plane 2

Memory Address 1FC5 **I/O Address** 3C5 **Index** 04



D3 Chain 4

- 0: Causes the system to access the data sequentially within a memory plane.
- 1: Causes the two low-order bits A0 and Al to select the memory plane to be accessed by the system as follows:

A l	*A0*	*Map Selected*
0	*0*	*0*
0	1	1
1	0	2
1	1	3

D2 Odd/Even Mode

. 0: Enables the system to write to planes 0 and 2 only at even addresses and planes 1 and 3 at odd addresses.

. 1: Enables the system to write to any plane which is enabled by the plane mask register.

D1 256K Memory Size (EGA mode only)

. 0 when 256K of memory is not installed. Address bits 14 and 15 are forced to 0.

- 1 when 256K of memory is installed. D1 should always be 1 for this multi-function video controller.

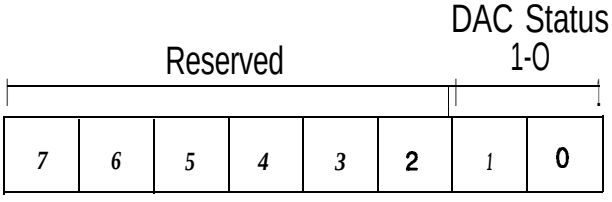
D0 Alpha Mode Select (EGA mode only)

- 0: Causes the graphics mode to be active. Address bits 13, 14 and 15 of the B video memory planes will be the same as those of the A video memory planes.

. 1: Causes the alphanumeric mode to be active. This causes address bits 13, 14 an 15 of the B video memory planes to be selected from the character map select register.

DAC Status (VGA/Miscellaneous)

Memory Address 1FC7 **I/O Address** 3C7



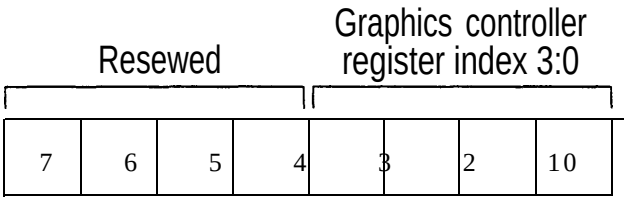
D1-D0 DAC Status. This port returns the last access cycle to the palette.

D1	*D0*	*Most Recent Cycle*
0	*0*	Write palette cycle
1	1	Read palette cycle

Reads from the DAC Write (3C8) or DAC Status registers do not interfere with read or write cycles, and may take place at any time.

(Graphics Controller Registers) Address

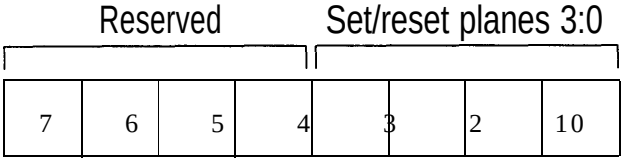
Memory Address 1FCE **I/O Address 3CE**



D3-D0 Graphics Controller Register Index Address Bits 3 to 0
These bits select which register is to be accessed at port 3CFh.

(Graphics Controller Registers) Set/Reset

Memory Address 1FCF **I/O Address 3CF** **Index 00**



D3-D0 Set/Reset plane 3 to 0
These bits allow the set or reset of byte values in the four video planes:

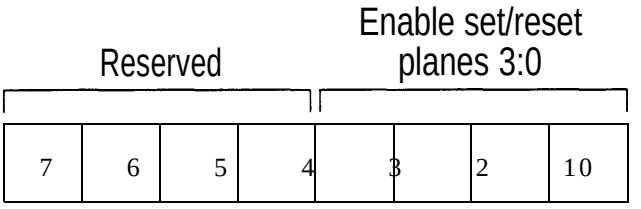
. 1: Sets the byte

. 0: Resets the byte.

This register is active when the graphics controller is in write mode 0 and enable set/reset is activated.

Enable Set/Reset (Graphics Controller Registers)

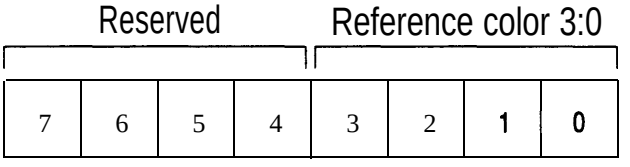
Memory Address 1FCF **I/O Address** 3CF **Index** 01



D3-D0 Enable Set/Reset Plane 3 to 0
These bits control the activation of the set/reset register. Setting any bit to 1 enables the corresponding bit in the set/reset register. Writing a 0 will disable the corresponding set/reset bit.

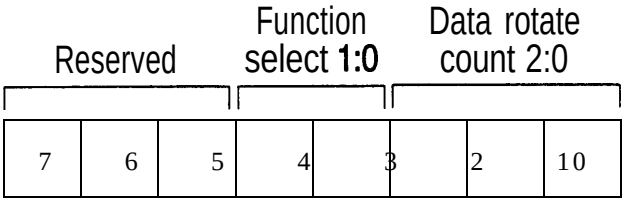
Color Compare (Graphics Controller Registers)

Memory Address 1FCF **I/O Address** 3CF **Index** 02



D3-D0 Reference Color
These bits represent a 4-bit color value for reference by read mode (bit D3, Index 05h, mode control register). In this mode, when the system reads from display memory, the data byte returned will have a 1 in each bit position where the data in the four memory planes matches the value in the color compare register. Only the planes enabled by the color don't care register will be tested.

Memory Address 1FCF **I/O Address** 3CF **Index** 03

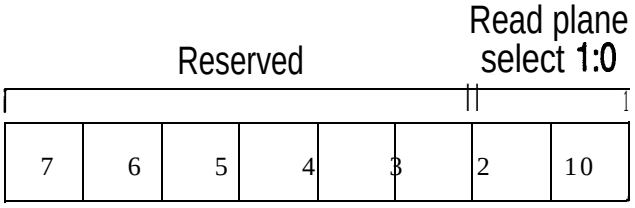


D4-D3 Function Select Bits 1 and 0
These two bits are used to select hardware logic functions to be performed between the video memory data latches and any data. Selected by the mode control register bits DO and D1.

D4	D3	Function
0	0	Data unmodified
0	1	Logical AND with latched data
1	0	Logical OR with latched data
1	1	Logical XOR with latched data

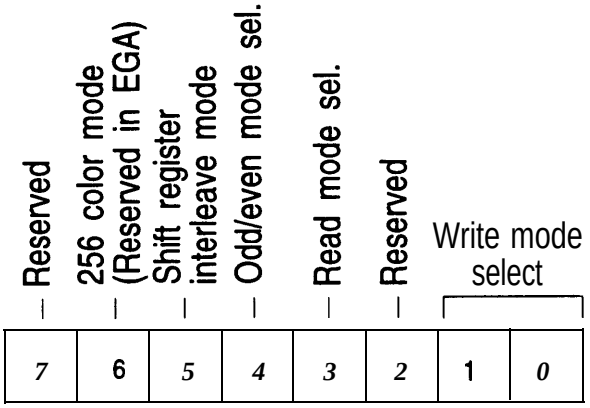
D2-D0 Data Rotate Count Bits 2 to 0
These bits produce a 3-bit binary value which specifies the number of bit positions to rotate the system data on writes to video memory in write mode 0.

Memory Address 1FCF **I/O Address** 3CF **Index** 04



D1-D0 Read Plane Select
This register is used to select the video memory plane to be read by the system. This register will select planes 3 to 0, as programmed in binary, for read operation.

Memory Address 1FCF **I/O Address** 3CF **Index** 0 5



D6 256-Color Mode (VGA mode only)

- 0: Allows the loading of the shift registers to be controlled by bit D5.
- 1: Causes the shift registers to be loaded in a manner which supports the 256-color mode

D5 Shift Register Interleave Mode

. 1: Causes the shift registers in the Graphics Controller to format the serial data with odd numbered bits from both planes in the odd numbered planes and the even numbered bits from both planes in the even numbered planes.

D4 Odd/Even Mode Select

- 0: Makes the read plane select register control which plane the system reads data from.
- 1: Causes system address bit A0 to replace bit 0 of the read plane select register, thus allowing A0 to determine odd or even plane selection.

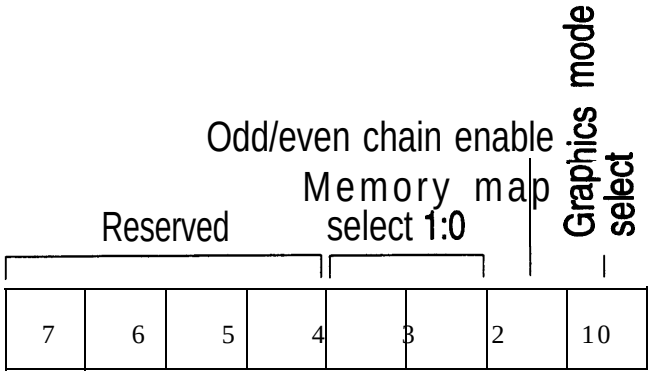
D3 Read Mode Select

- 0: Causes the system to read data from the active video memory plane.
- 1: Enables the color compare register.

D2 Reserved.

D1-D0 Write Mode Select
These two bits select the write mode as follows:

DI	*DO*	Write *Mode*
0	*0*	Data rotate. logical functions and set/reset are enabled in this mode.
0	1	The active video memory plane(s) are written with the contents of the 32-bit system data latches.
1	0	In this mode the bit position corresponding to the video plane address is used as the value of an 8-bit write to that video plane.
1	1	Each plane receives 8 bits of the value contained in the set/reset register for that plane. Rotated system data is ANDed with the bit mask register to give an 8-bit value which performs the same function as the bit mask register does in modes 0 and 2. In EGA this mode is the same as mode 1.



D3-D2 Memory Map Select Bits 1 and 0
These bits select where the video memory is mapped as follows:

D3	*D2*	*Address*
0	*0*	A0000 - BFFFFh
0	1	A0000 - AFFFFh(1)
1	0	BOOOO-B7FFFh
1	1	B8000 - BFFFFh

(1) Second video RAM window, when enabled, will occupy either B0000h to B7FFFh or B8000h to BFFFFh. See auxiliary register 0Ch.

D1 Odd/Even Chain Enable

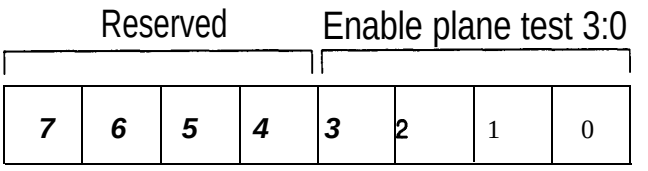
- 0: Causes A0 of the memory address bus to be used during system memory addressing.
- 1: Allows A0 to be replaced by either Al 6 of the system address (if bits D3 and D2 are 0), or the odd/even page select bit from the miscellaneous output register.

DO Graphics Mode Select

- 0: Enables alpha mode and the character generator addressing system is activated.
- 1: Enables graphics mode and the character addressing system is not used.

Color Don't Care (Graphics Controller Registers)

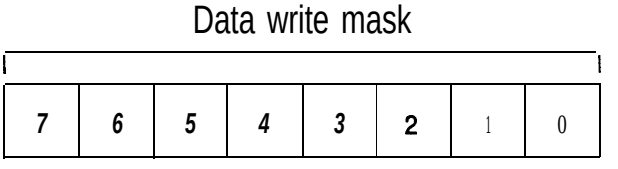
Memory Address 1FCF **I/O Address** 3CF **Index** 07



D3-D0 Enable Plane 3 to 0 Test
When any of these bits are set to 1 the associated plane is included in the color compare read cycle.

Bit Mask (Graphics Controller Registers)

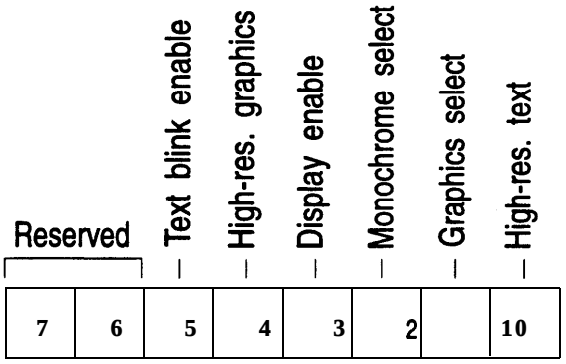
Memory Address 1FCF **I/O Address** 3CF **Index** 08



D7-D0 Data Write Mask Bits 7 to 0
If any bit in this register is set to 1 the corresponding bit in all planes may be altered by the selected write mode and system data.

If any bit is set to 0 the corresponding bit in each plane will not change.

Memory Address 1FD8 **I/O Address** 3D8



D5 Text Blink Enable

. 0: Causes attribute bit 7 to be used for background intensity control.

- 1: Characters with attribute bit 7 high will blink and all characters will have low background intensity.

D4 High Resolution Graphics: When in graphics mode (D1=1), D4=0 selects 320 x 200 mode and D4=1 selects 640 x 200 mode. This bit only has an effect when in graphics modes.

D3 Display Enable

- 0: Blanks the display.

. 1: Enables the display. Bit D5 of auxiliary port 2 must be high before the display can be blanked.

D2 Monochrome Select: This bit alters the foreground color palette in the 320 x 200 graphics mode. It has no effect in other modes. For foreground pixels, D2=0 (color) causes the blue output to have the same state as port 3D9h D5. When D2=1 (monochrome), the blue output is the same as pixel data bit CO. This bit only has an effect in the 320 x 200 graphics mode. If the CGA hardware palette is disabled (auxiliary port 3 D4=1) this bit has no effect on hardware.

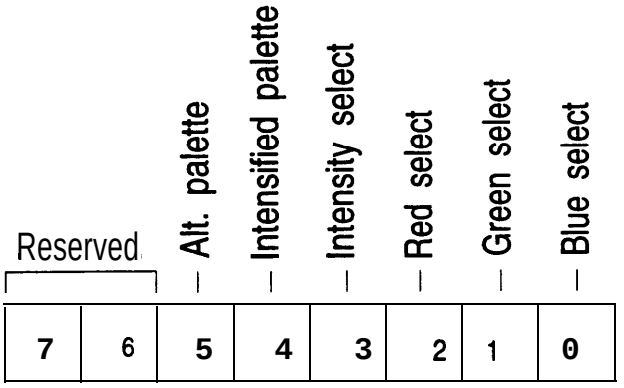
D1 Graphics Select

. 0: Selects text mode

- 1: Select graphics mode.

DO High Resolution Text: This bit has no effect in hardware, but must be interpreted by emulation software to set up the sequencer and CRTC. When in text mode (D1=0), D0=0 selects 40 x 25 characters and D0=1 selects 80 x 25 characters. This bit has no effect in graphics modes.

Memory Address 1FD9 **I/O Address** 3D9



D5 Alternate Palette: In the 320 x 200 graphics mode, D5 selects one of two foreground color palettes. D5 has an effect only in color mode (port 3D8h D2=0). When D5=0, the blue video output is low for all foreground pixels. When D5=1, the blue video output is high for all foreground pixels. D5 does not change the background (CO=Cl=O) color. If the CGA hardware palette is disabled (auxiliary port 2 D4=1) then this bit has no effect.

This bit has an effect only in the 320 x 200 graphics mode.

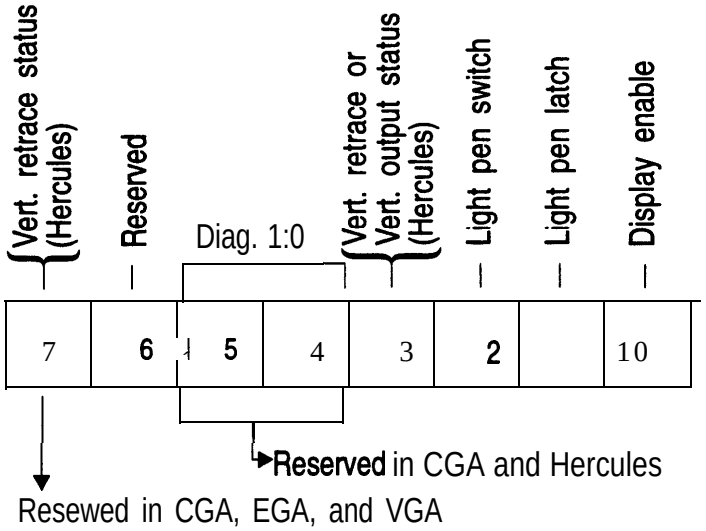
D4 Intensified Palette: In 320 x 200 graphics mode, D4=0 causes the foreground pixels to be intensified and D4=1 causes them to be low intensity. If the CGA hardware palette is disabled (auxiliary port 2 D4=1) then this bit has no effect.

This bit has an effect only in the 320 x 200 graphics mode.

D3-D0 Intensity, Red, Green, and Blue Select: In the text modes, these bits determine the overscan (border) color. In the 320 x 200 graphics mode, these bits determine the background pixel (CO=C 1=0) and overscan colors. In 640 x 200 graphics mode, these bits determine the foreground pixel color.

These bits have no effect if the CGA hardware palette is disabled (auxiliary port 2 D4=1). The overscan color is always determined by the contents of the attributes controller overscan register if the CGA overscan is disabled (auxiliary register 2 D3=1).

Memory Address Mono 1FBA Color 1FDA **I/O Address** Mono 3BA Color 3DA



D7 Vertical Retrace Status (Hercules mode)

- 0: Indicates that the CRTC is in a vertical retrace period.
- 1: Vertical Retrace is inactive.

D5-D4 Diagnostic 1 And 0
D4 and D5 are selectively connected to two of the eight color outputs of the attribute controller. Bits D4 and D5 of the color plane enable register determine which color outputs are used.

Color Plane Register		*Input Status Register 1*	
D5	*D4*	*D5*	*D4*
0	0	PD2	PD0
0	1	PD5	PD4
1	0	PD3	PD1
1	1	PD7	PD6

D3 This bit has no effect in Power Graphic mode.

Vertical Retrace: (VGA, EGA, or CGA mode)

- 0: Indicates that video information is being displayed.
- 1: Indiates that a vertical retrace interval is occurring.

Video Output Status: (Hercules mode) This bit monitors the direct drive video output.

- 0: Indicates that the driver output is high.
- 1: Indicates that the driver output is low.

D2 Light Pen Switch

- 0: Indicates that the light pen switch is closed.
- 1: Indicates that the light pen switch is open.

D1 Light Pen Latch

. 0: Indicates that the light pen latch is reset.

■ 1: Indicates that the light pen latch is set.

DO This bit has no effect in Power Graphic mode.

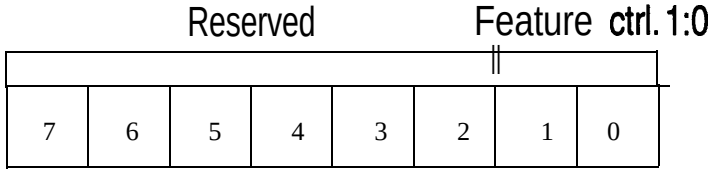
Display Enable

■ 0: Indicates an active display interval.

. 1: Indicates a horizontal or vertical retrace interval.

Feature Control (VGA/EGA/Misc Registers)

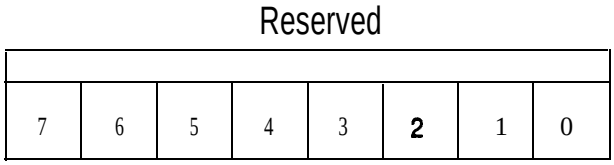
Memory Address Mono W 1FBA Color W 1FDA **I/O Address** Mono W 3BA Color W 3DA
Read 1FCA Read 3CA



Dl-DO Feature Control Bits 1 And 0
These bits can be used as internal general purpose bits.

Light Pen Clear (Misc Registers)

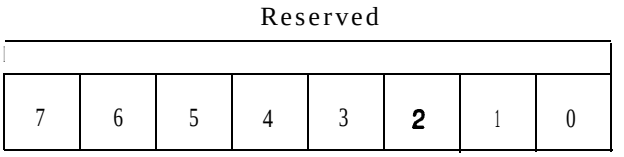
Memory Address 1FDB **I/O Address** 3DB



When this port is read from or written to, the light pen latch is cleared.

(Misc Registers) — Light Pen Set

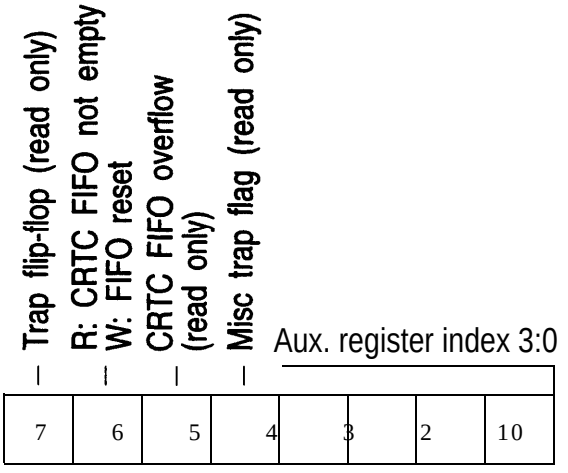
Memory Address 1FDC **I/O Address** 3DC



When this port is read from or written to, the light pen latch is set.

(Auxiliary Registers) — Auxiliary Index

Memory Address 1FDE **I/O Address** 3DE



A read from the auxiliary index register clears the trap flip-flop and returns the TRAP output to its inactive state. The CRTC FIFO overflow flag is also reset and the FIFO is prepared for reads. Software must wait for 3 BUSCLK cycles (2 10 nS at 14.3 18 MHz) before reading the FIFO.

D7 (R): Trap Flip-Flop: If the ATLAS caused a trap interrupt then D7=1. This bit will only be 1 for the first read after a trap interrupt. Reading the auxiliary Index register clears this flag and returns the TRAP output to its inactive state.

D6 (R): CRTC FIFO Not Empty: If a CRTC emulation trap condition occurred and the CRTC FIFO is not empty then reading D6 returns 1. This flag is cleared by reading all data from the CRTC FIFO.

(W): FIFO Reset: Writing a 1 to D6 will reset the CRTC FIFO register and overflow flag. A 0 must be written to D6 before the FIFO can be used again.

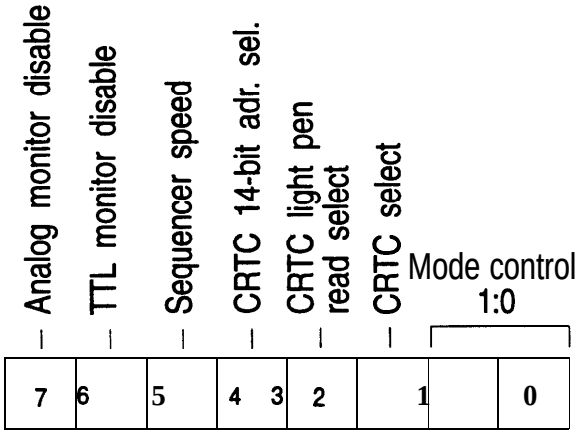
D5 (R). CRTC FIFO Overflow: If more than 4 writes occurred to CRTC registers since the last trap interrupt service (the CRTC emulation FIFO has overflowed) then D5=1. This bit will only be 1 for the first read after a trap interrupt. Reading the auxiliary Index register clears this flag.

D4 (R). Miscellaneous Trap Flag: If D4=1, a trap was generated which was not a CRTC emulation trap. This indicates that one of the bits in the trap flag register is set.

D3-D0 (R/W). Auxiliary Register Index: Bits D3-D0 of this register select which auxiliary register is to be accessed at port 3DFh.

Mode Control (Auxiliary Registers)

Memory Address 1FDF **Read** 3DF **Index** 00



D7 Analog Monitor Disable: When D7=0, the analog monitor synchronous drivers are enabled. If D7=1 then the analog monitor drivers are disabled. The drivers are also disabled if port 3C2h, D4=1.

D6 TTL Monitor Disable: When D6=0, the TTL monitor drivers are enabled. If D6= 1 then the TTL monitor drivers are disabled.

D5 Sequencer Speed: D5=0 selects sequencer cycles with high CPU interleave. High CPU interleave is usually selected with sequencer clocks of less than 30 MHz. Higher sequencer clock frequencies require D5=1 to select low interleave cycles which meet the DRAM timing specifications. Halt the sequencer by a synchronous or asynchronous reset before changing this bit.

D4 CRTC 14-Bit Address Select: If D4=0 then the CRTC start address, cursor address, and light pen registers and address counter are 16-bit. If D4=1 then the most significant 2 bits of the registers and counter are forced to 0. This is used for 6845 CRTC emulation.

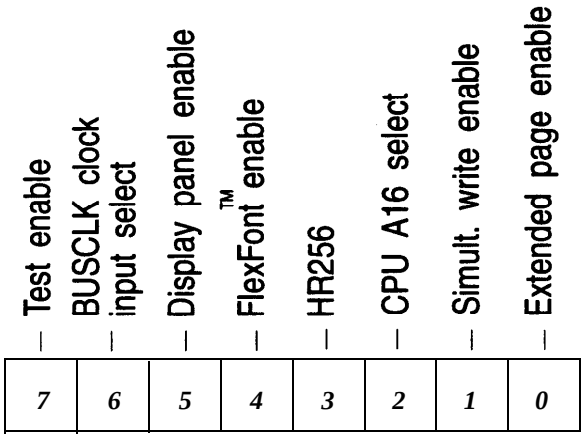
D3 CRTC Light Pen Read Select: D3=0 causes the vertical retrace start and end registers to be read at CRTC register addresses 1 Oh and 11 h. D3=1 causes the light pen registers to be read at those addresses.

D2 CRTC Select: The VGA CRTC is used when D2=0 and the EGA CRTC is used when D2=1.

Dl-DO Mode Control 1 and 0: These bits select which display adapter the ATLAS is to emulate. They determine which registers may be accessed and which hardware emulation functions are enabled. Halt the sequencer by a synchronous or asynchronous reset before changing these bits.

D1	*DO*	*Mode*
0	*0*	VGA
0	1	EGA
1	0	CGA
1	1	MDA/Hercules

Memory Address 1FDF **I/O Address** 3DF **Index** 01



D7 Test Enable: For normal operation, D7=0. To enable test functions, D7=1. When test functions are enabled, auxiliary register 4 (general storage) can be used to control ATLAS's hardware test functions.

D6 BUSCLK Clock Select: Port 3C2h is used to select the clock source. Halt the sequencer by a synchronous or asynchronous reset before changing this bit. The state of D6 affects the clock input selection as follows:

3C2h *D3, D2*	*D6 = 0*	*D6 = 1*
00	CLKIN0	CLKIN1÷2
01	CLKIN1	CLKIN3
10	CLKIN2	CLKIN2
11	BUSCLK	CLKIN1

D5 Display Panel Enable: The ENABLE output (pin 70) is controlled by this bit, and is used to enable the display panel. The state of the ENABLE pin is the same as D5.

D4 FlexFont Enable: Normal text mode font selection is in effect when D4=0. When D4=1, attribute bits D6-D4 are used to select from one of eight simultaneously displayable fonts. The background color bits are disabled (forced low), attribute bit D7 (intensity/blink) still has effect, and D3 is not used for font selection.

D3 HR256 Select: When this bit is high, the required hardware functions are enabled to permit a high resolution, 256 color, display mode. This function is enabled only when the LS-004 is in VGA mode on a CRT display. Halt the sequencer by a synchronous or asynchronous reset before changing this bit.

D2 CPU Al6 Select: When high, CPU page select bit 0 (DO) is replaced by address bit A16. This allows the use of a 128K memory map (A0000-BFFFFh) so that the CPU can access 2 pages in VGA 256 color mode without page switching.

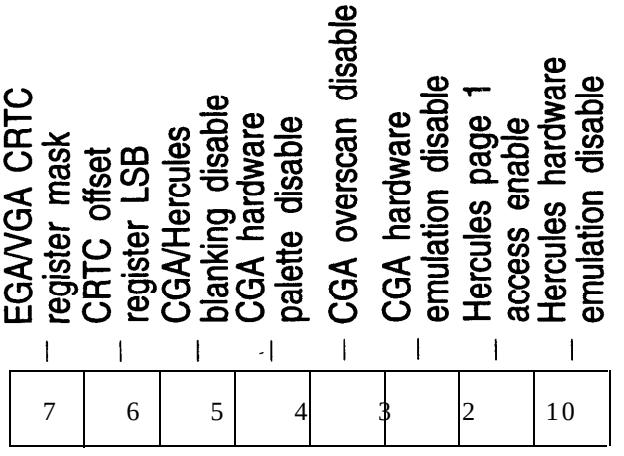
D1 Simultaneous Write Enable: When the 5 12 KB memory option is selected internal DRAM address bit 16 selects one of /CAS0 or /CAS1 to go active during a memory cycle. During a CPU write cycle both /CAS0 and /CAS 1 will go active if the simultaneous write enable bit is high. This is required in alphanumeric modes where multiple pages are desired. The character font must be loaded into both banks of plane 2 DRAM so that characters are displayed properly when ASCII and atribute data are taken from the upper DRAM bank.

DO Extended Page Enable: When this bit is 0 display memory in 13h is limited to 1/4 of the installed DRAM. This gives full compatibility with the IBM VGA. Multiple display pages are available when this bit is 1. If D3 of this register (high resolution select) is 1 then the extended page enable should also be 1.

The extended page enable bit only affects CPU cycle addressing if D3 of sequencer register 4 (Chain 4) is 1. If DO is 0 then A0 and Al of the DRAM address are forced low. If DO is 1 then page page select bits 1 and 0 of the auxiliary register 9 are used for the low DRAM address bits.

If D3 (high resolution select) of auxiliary register 1 is 0, then DO affects CRT cycle addressing. If bit D6 (double word mode) of CRTC register 14h is 1, and DO is 0, then both Al and A0 are 0 and the display wraps in the same way as the IBM VGA. If DO is 1, then the high CRTC counter bits replace A0 and Al so that more memory may be accessed for high resolution displays

Memory Address 1FDF **I/O Address** 3DF **Index** 0 2



This register determines the degree of hardware emulation desired and also provides functions required for software emulation.

D7 VGA/EGA CRTC Register Mask

- 0: Allows access to all VGA/EGA CRTC registers.
- 1: Prevents access to CRTC registers for which traps are enabled by D4 and D5 of the trap control register.

D6 CRTC Offset Register LSB: This bit is used to achieve odd CRTC offset register values so that full software-aided emulation of the 6845 CRTC is possible. It should be enabled, D6= 1, at all times.

D5 CGA/Hercules Blanking Enable

- 0: Forces the display to be enabled in CGA and Hercules modes. This overrides the display enable bits in registers 3B8h and 3D8h so that the display will not flicker during scrolling.
- 1: Allows registers 3B8h (Hercules mode) and 3D8h (CGA mode) to control the display if hardware emulation is enabled.

D4 CGA Hardware Palette Disable

- 0: Causes the CGA hardware palette to be used in CGA mode if D2=0.
- 1: Allows the use of the attributes controller palette and enables extra trap conditions to aid in emulation of CGA register 3D9h. This allows flexibility in the way CGA colors are displayed so that various monitors can be used.

D3 CGA Overscan Disable

- 0: Causes the overscan (border) color to be taken from CGA register 3D9h as required in CGA mode if D2=0.
- 1: Forces the overscan color to be taken from the attributes controller overscan register. This allows software control of the overscan. The overscan must be forced to black on monitors which are not blanked during retrace.

D2 CGA Hardware Emulation Disable

- 0: Enables hardware emulation for CGA ports 3D8h and 3D9h.
- 1: Hardware emulation is disabled so that the contents of 3D8h and 3D9h have no effect on hardware. Extra trap conditions are enabled to permit software emulation. The CGA overscan and hardware palettes are also disabled.

D1 Hercules Page 1 Access Enable

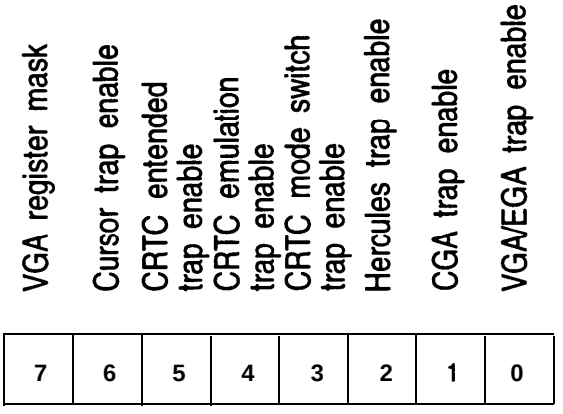
- 0: Allows Hercules port 3BFh to control CPU access to Hercules memory page 1 (B8000-BFFFFh) if DO=O.
- 1: Enables CPU access to memory page 1 when in Hercules mode. This allows software to control emulation of Hercules port 3BFh.

DO Hercules Hardware Emulation Disable

- 0: Enables hardware emulation for Hercules ports 3B8h and 3BFh.
- 1: Hardware emulation is disabled so that the contents of 3B8h and 3BFh have no effect on hardware. Extra trap conditions are enabled to permit software emulation.

Trap Control (Auxiliary Registers)

Memory Address 1FDF **I/O Address** 3DF **Index** 0 3



This register determines which conditions cause a trap interrupt (NMI) and also controls access to the VGA CRTC registers and CRTC emulation FIFO.

D7 VGA Register Mask

- 0: Allows access to VGA registers in the 3C0-3CFh. This bit is used by emulation software when it must alter the VGA registers. Power-up default is D7=0.
- 1: Causes the VGA registers in the 3C0-3CFh range to be masked from CPU access.

D6 Cursor Trap Enable

- 0: Trap disabled (power-up default)
- 1: Enables traps on writes to cursor locations.

D5 CRTC Extended Trap Enable

- 1: Enables traps and FIFO writes for CRTC registers 0C-0Fh.

D4 CRTC Emulation Trap Enable

- 1: Enables trap interrupts on writes to CRTC registers 00h-0Bh and 1 Oh-18h. Writes to the CRTC emulation FIFO are also enabled. This is used for software-aided emulation of the 6845, VGA, or EGA CRTC's, See the trap conditions described elsewhere.

D3 CRTC Mode Switch Trap Enable

- 1: Enables trap interrupts to CRTC ports which might indicate that an automatic mode switch is required. The CRTC Index register can be accessed at port addresses in the 3BXh and 3DXh ranges. See the trap conditions described elsewhere.

D2 Hercules Trap Enable

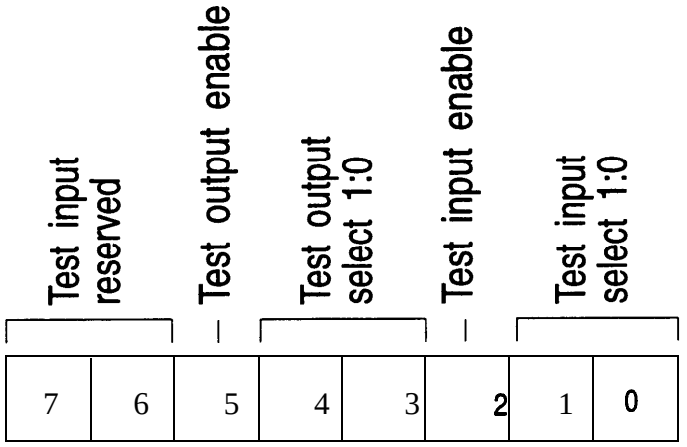
. 1: Enables trap interrupts on writes to Hercules ports. CPU access to Hercules ports 3B8h and 3BFh is also enabled. See the trap conditions described elsewhere.

Dl CGA Trap Enable

. 1: Enables trap interrupts on writes to CGA ports. CPU access to CGA ports 3D8h and 3D9h is also enabled. See the trap conditions described elsewhere.

DO . 1: Enables trap interrupts on writes to ports in the 3C0h-3CFh addresss range. Refer to the trap conditions described elsewhere.
Enabling the traps does not enable CPU access to the registers. The VGA registers must be unmasked (see D7) before the CPU can access the registers.

Memory Address 1FDF **I/O Address** 3DF **Index** 04



D7-D0 General Storage and Test Control

This register is normally used for flag storage by the BIOS software. When D7 of the extended function register (test enable) is high, these bits control ATLAS's test functions. Some of the input and output pins can be selected to drive or monitor internal signals of the ATLAS for testing.

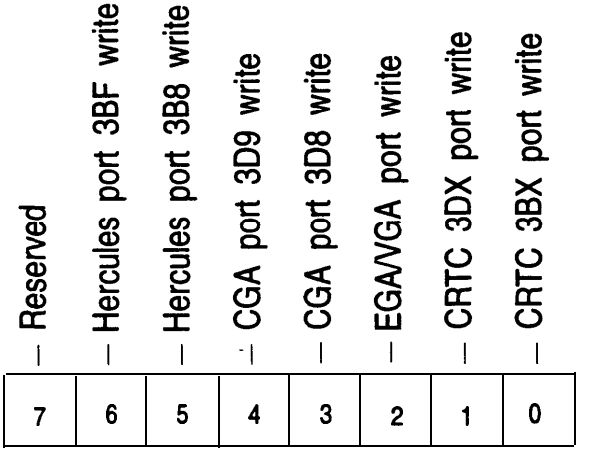
Test inputs are enabled when D2 is high and D7 of auxiliary register 1 is high. Bits DO and D1 are used to select which internal signals are to be driven:

Input Pin	*D1,D0=00*	*D1,D0=01*	*D1,D0=10*	*D1,D0=11*
MONSO	TMSYNC	*TMAMUX*	TMAMUX	TMDE
MONS 1	TMREFSH	TMBMUX	TMBMUX	TMBLANK
FEAT0	/TMDREN	/TMDREN	/TMDREN	TMCURSR
FEAT1	TMVDE	TMCRT	/TMCPUL	TMUNLIN
PANEL		TMCAL	/TMCRTL	TMPVRTC
LPENSW		TMCCLK	TMHRHLT (/TMDREN=1)	TMLCV
UP		/TMTOP		TMLCVBT
DOWN			TMDEBT	

Test outputs are enabled when D5 is high and D7 of auxiliary register 1 is high. Bits D3 and D4 are used to select which internal signals are available at the outputs:

Output Pin	*D4,D3=00*	*D4,D3=01*	*D4,D3=10*	*D4,D3=11*
FCO	/SQATLD	SQCRTLO	CR1SYNC	CRlSYNC
FC1	/SQCCLK	SQCRTL1	CR8RFSH	CR8RFSH
VDRIVE	SQAMUX	SQCRTL2	CR7CRSR	CR7BCRSR
ADRIVE	SQBMUX	/SQQRST	CR7UNLN	CR7BUNLN
ENABLE	SQCRT	/SQCPUL	CRlHDE	CR1HDE
IRQ	SQCAL	/SQGSL	CR4DE	CR4DE
TRAP	SQCRA2	/SQDREN	CR5LCV	CR5BLCV

Memory Address 1FDF **I/O Address** 3DF **Index** 0 5



The conditions which cause a trap interrupt (NMI) are described in detail in the section on Trap Interrupts.

D6 Hercules Port 3BFh Write: When Hercules trap conditions 2 or 5 are met then D6 is set. The trap conditions are described in another section.

D5 Hercules Port 3B8h Write: When Hercules trap conditions 1, 3, or 4 are met then D5 is set. The trap conditions are described in another section.

D4 CGA Port 3D9h Write: When CGA trap conditions 2 or 5 are met then D4 is set. The trap conditions are described in another section.

D3 CGA Port 3D8h Write: When CGA trap conditions 1, 3, 4, or 6 are met then D3 is set. The trap conditions are described in another section.

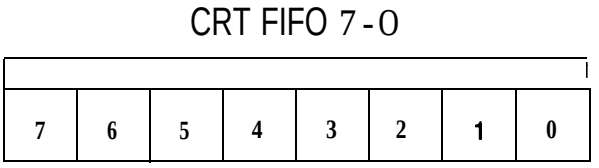
D2 VGA/EGA Port Write: This bit is set if VGA/EGA trap condition 1 occurred. The trap conditions are described in another section.

D1 CRTC 3DXh Port Write: This bit is set if a CRTC mode switch or CRTC emulation trap condition occurred at port addresses 3DOh to 3D7h.

DO CRTC 3BXh Port Write: This bit is set if a CRTC mode switch or CRTC emulation trap condition occurred at CRTC port addresses 3BOh to 3B7h.

CRTC FIFO Read (Auxiliary Registers)

Memory Address 1FDF **I/O Address** 3DF **Index** 0 6

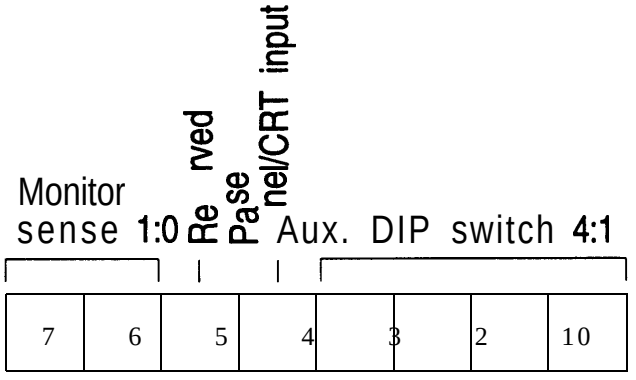


This register is used to read the CRTC emulation FIFO. When D6 of the auxiliary Index register is 1 then data is available in the FIFO. The FIFO is eight bytes in length.

The first read after a trap interrupt will return the data which was written to the CRTC and the second read returns the index in D4-D0 (D7-D5 are 0). Successive reads will alternately return data and then index. Up to four data/index pairs are available from the FIFO. When the FIFO is empty then the data returned will be random. Bit D6 of the auxiliary index register will become 0 when the FIFO is empty.

Auxiliary Input Register 1 (Auxiliary Registers)

Memory Address 1FDF **I/O Address** 3DF **Index** 0 7



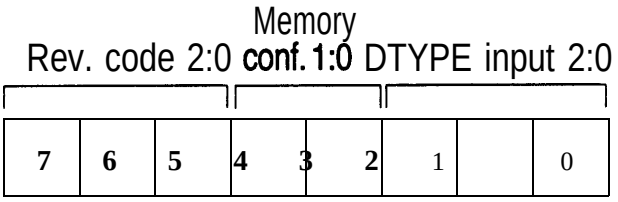
D7-D6 Monitor Sense Input 1-O: These bits are always read as 00.

D4 Panel/CRT Input: This bit is always read as 0.

D3-D0 Auxiliary Dip Switch l-4: These bits are always read as 0000.

(Auxiliary Registers) — Auxiliary Input Register 2

Memory Address 1FDF **I/O Address** 3DF **Index** 0 8



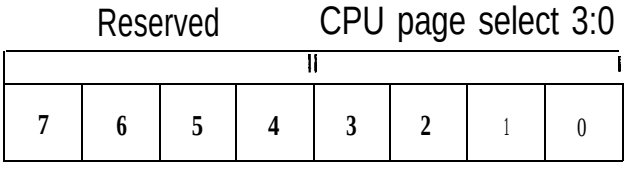
D7-D5 Revision Code 2-O: These bits are the chip revision code.

D4-D3 Memory Configuration: These bits are always read as 00.

D2-D0 Display Type Inputs 2-O: These bits are always read as 111.

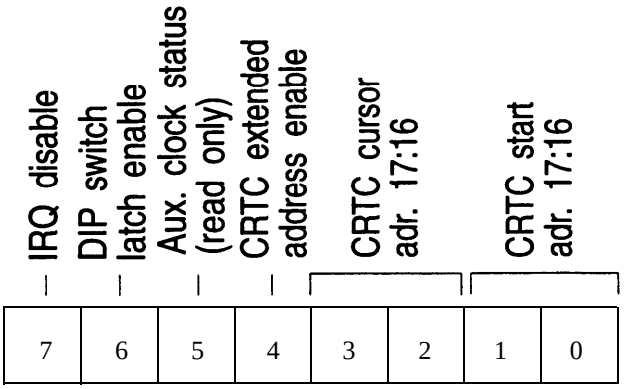
(Auxiliary Registers) — CPU Page Select

Memory Address 1FDF **I/O Address** 3DF **Index** 09



D3-D0 CPU Page Select 3-O: Up to 16 pages of memory are available in the 320 x 200 pixel, 256 color, graphics mode of the VGA. When in this mode these four bits select which 64K page the CPU can access. These bits take effect when one of either D3 of the extended function register 1, or D6 of graphics controller register 5 is high.

Memory Address 1FDF **I/O Address** 3DF **Index** 0A



D7 IRQ Disable: When D7=1 the IRQ output is prevented from going to the active state. This gives compatibility with the ISA bus version of the IBM VGA.

D6 DIP Switch Latch Enable: When D6 is high the DIP switch inputs (located in auxiliary register 07) are latched on the rising edge of the sequencer reset bit.

When D6 is low the DIP switch input values are not disturbed by subsequent sequencer resets.

D5 (R). Auxiliary Clock Status: This bit is always read as 1.

D4 CRTC Extended Address Enable: When D4 is low, the DRAM address bits 17 and 16 are low and only 256 KB of memory can be accessed. This is used to achieve full EGA and VGA compatibility when extended memory configurations are selected.

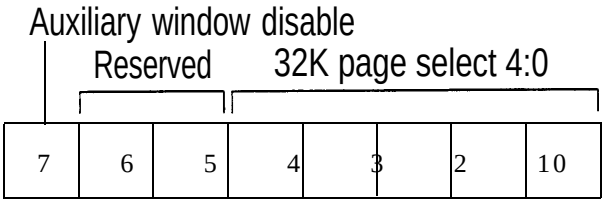
When D4 is high 18-bit addressing is enabled. Bits D2 and D3 of auxiliary register 9 form the high address bits on CPU accesses to DRAM. The CRTC address counter is extended to 18 bits to allow the display of any area of memory.

D3-D2 CRTC Cursor Address Bits 17,16: These are the most significant bits of the cursor address register when 18-bit CRTC addressing is used for expanded memory access.

D1-D0 CRTC Start Address Bits 17,16: These are the most significant bits of the start address register when 18-bit CRTC addressing is used for expanded memory access.

(Auxiliary Registers) **32K Video RAM Page Select**

Memory Address 1FDF **I/O Address** 3DF **Index** 0C



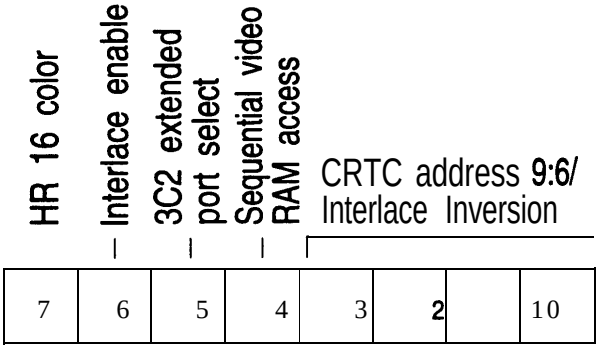
D7 Auxiliary Window Disable

- 0: Enables the second video RAM window.
- 1: Disables the second video RAM window.

D4-D0 32K Page Select Bits 4-O: Up to 16 pages of memory are available in the 320 x 200 pixel, 256 color, graphics mode of the VGA for the second video RAM window. When in this mode these four bits select which 64K page the CPU can access. These bits take effect when D7 of this register is low and one of either D3 of the extended function register 1, or D6 of graphics controller register 05 is high.

(Auxiliary Registers) **Interlace Support**

Memory Address 1FDF **I/O Address** 3DF **Index** O D



D7 HR16 Color: When this bit is high, and the HR256 mode is enabled, the sequencer runs in HR16 (high resolution, 16 color) mode while the attributes controller and the graphics controller run at twice the clock speed of the sequencer. Note that all horizontal values in the CRT controller are divided by two and that byte pan pans by 16 pixels instead of 8 in all VGA 16 color planer modes.

. When D7 is low this mode is disabled.

D6 Interlace Enable

. 0: The interlace mode is disabled.

. 1: This bit enables the interlace mode. In this mode CRTC counter address bits (6 to 9) are inverted every other vertical frame and the VRTC signal is delayed for one half of a horizontal line every other vertical frame. The VRTC signal is delayed on the opposite frame to the address being inverted. To use this mode select the CRTC address bits to be inverted and set the Interlace Enable bit. CRTC register 06, DO, inverts every other frame to give an odd total of lines for every two frames. The value in this register must be even in interlace mode and the logical horizontal line size must be double the display size.

D5 3C2 Extended Port Select

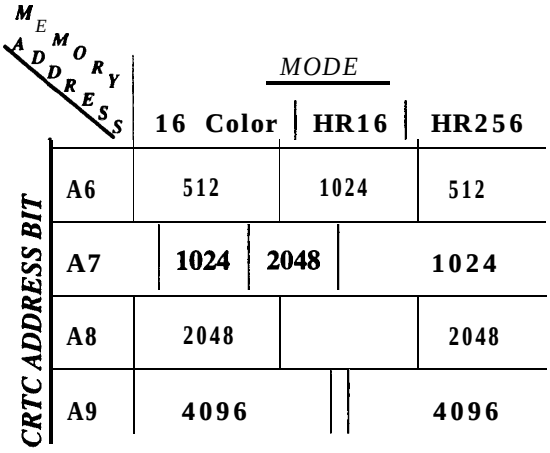
- 0: /EXPWR responds to I./O writes at address 3CBh as well as 3CDh.
- 1: Allows the /EXPWR signal to respond to I/O writes at address 3C2h

D4 Sequential Video RAM Access

- 0: Video data is stored one byte every four sequencer cycles.
- 1: This bit enables the HR256 sequencer cycles to store video data sequencially in video RAM. This supports a 16 color planer memory map.

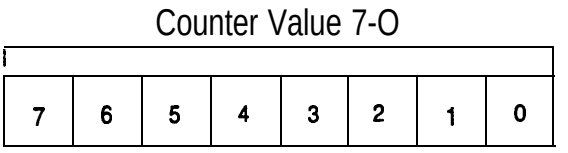
D3-D0 CRTC Address Bits 9 to 6/Interlace Inversion

These four bits are CRTC high address bits 9 through 6 and are only valid in interlace mode. Normally only one bit is selected. The following table shows the relationship between bit selected, address and mode selected.



(Auxiliary Registers) **Vertical Sync Adjust**

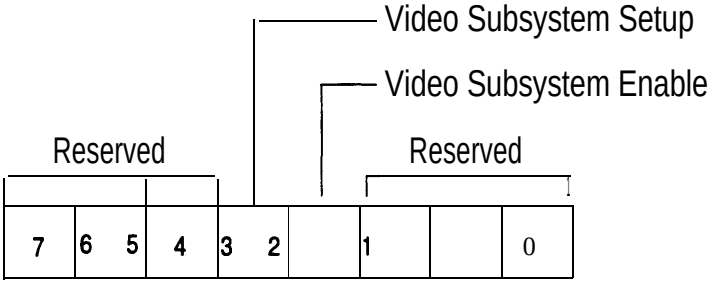
Memory Address 1FDF **I/O Address** 3DF **Index** O E



D7-D0 Counter Value Bits 7 to 0: This register provides a vertical sync timing adjustment for interlaced displays (interlace vertical retrace only). The value of these bits are compared to the horizontal count every other frame to provide a corrected vertical sync position. A value of zero in this register causes the horizontal total to be divided in half.

(Configuration) **Video Subsystem Access/Setup Enable**

Memory Address **I/O Address** 46E8



This register is only activated when ATLAS is reset with VGA enabled (refer to the vgaen strap description in Section 3.6.3 for more details).

D3 Video Subsystem Enable.

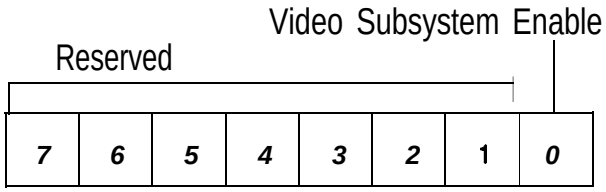
. 0: Disables the video subsystem

. 1: Enables the video subsystem

D4 Video Subsystem Setup.

- 0: Disables access to I/O address 102
- 1: Enables access to I/O address 102

Memory Address **I/O Address** 102



This register is only activated when ATLAS is reset with VGA enabled (refer to the VGAEN strap description in Section 3.6.3 for more details).

DO Video Subsystem Enable.

- 0: Disables the video subsystem
- 1: Enables the video subsystem

Chapter-6: Hardware Interface

This chapter explains the hardware interface to the ATLAS chip, both from the host PCI and ISA interfaces and to the video multiplexer (DUBIC if present), RAMDAC, and VRAM.

6.1 Introduction

The ATLAS chip has been designed in such a way as to minimize the amount of external logic required to implement a board. It includes:

. A direct interface to the ISA bus. In this case, the bus can be driven exclusively by means of buffers.

- A direct interface to the PCI bus, including a dedicated bus for external devices (this avoids the requirement for a buffer on the data bus).

. The PCI interface can be used to interface to any 32-bit bus, with glue logic.

. All necessary support for external devices, such as ROM, the Matrox DUBIC chip, RAMDACs, as well as an expansion decode strobe. All these devices can be interfaced without the need for glue logic.

. A 'No DUBIC' operation mode which eliminates the need for a DUBIC chip to drive the video data.

- A direct connection to the VRAM.

6.2 Host Interface

6.2.1 PCI Interface

The PCI Interface block diagram (Figure 6-l) shows how to connect ATLAS to the PCI bus, as well as to the local resources.

6.2.1 .1 PCI Bus Operation

Command Decoding

The following cycles on the PCI bus will perform the operations specified below on the ATLAS chip (when decoding recognizes the access):

C/BE<3:0># Command Type		*Operation*
0000	Interrupt acknowledge	None
0001	Special cycle	None
0010	I/O read	I/O read
0011	I/O write	I/O write
0100	Reserved	None
0101	Reserved	None
0110	Memory read	Memory read
0111	Memory write	Memory write
1000	Reserved	None
1001	Reserved	None
1010	Configuration read	Configuration register read
1011	Configuration write	Configuration register write
1100	Memory read multiple	Memory read
1101	Dual address cycle	None
1110	Memory read line	Memory read
1111	Memory write and invalidate	Memory write

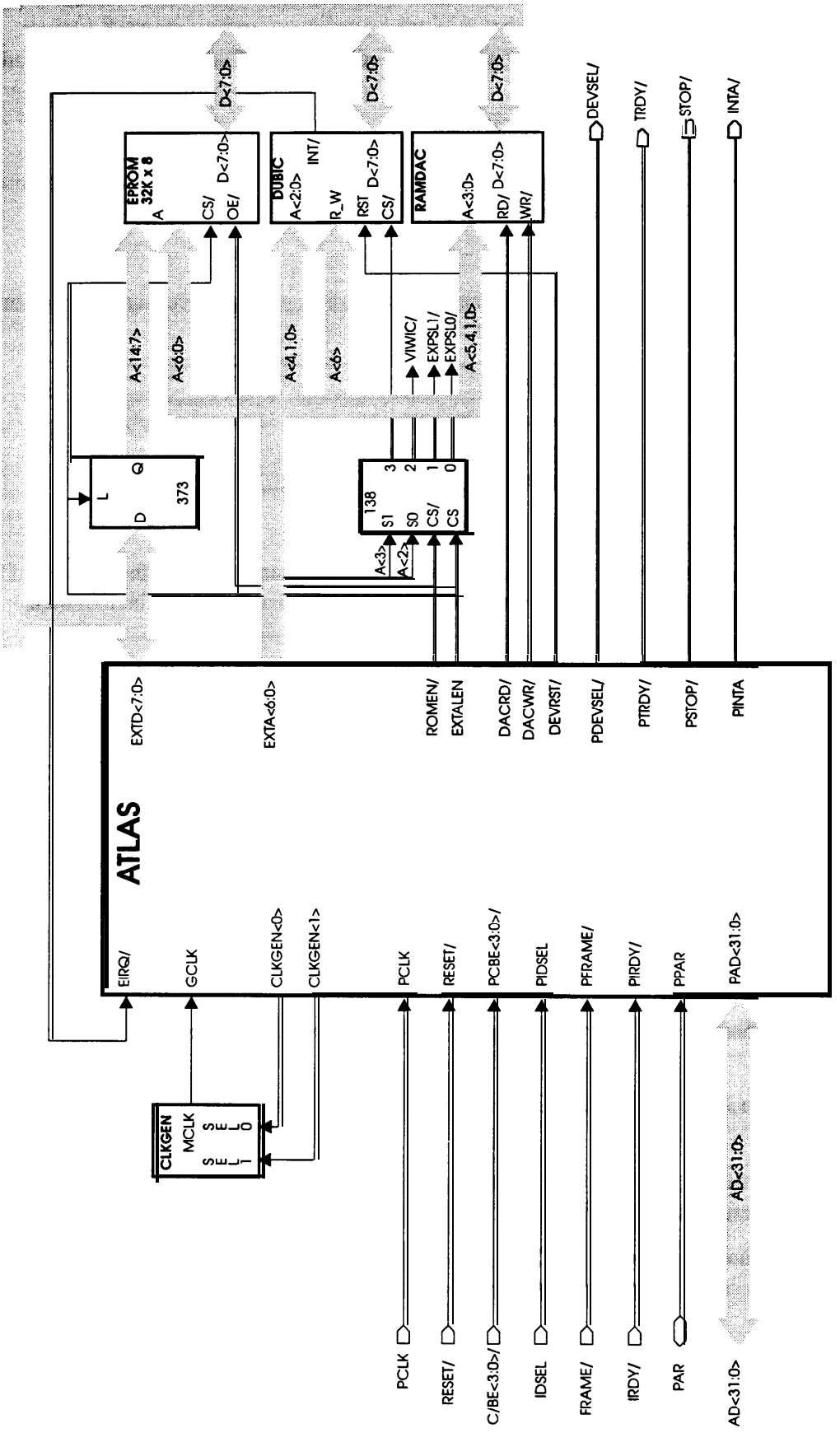


Figure 6-1: PCI Interface

DEVSEL

Because ATLAS is a medium-speed device, it will respond to DEVSEL in the second clock after FRAME/ is asserted.

Disconnect and Retry

Disconnect and retry are used in order to minimize the latency time on the bus. Refer to Section 6.2.1.2 for more information about when the disconnect and retry are used.

Burst Mode

Since ATLAS supports burst mode, address generation must be a counter. Because a 5-bit counter is employed, a disconnect will be generated every 32 dwords.

A1	A0	Burst Order
0	0	Linear incrementing (disconnect at every 32 dword boundary)
0	1	Disconnect after each transfer
1	X	Disconnect after each transfer

Configuration Access

During a configuration access, A<1:0> have a different function than normal - they indicate if the access is Type 0 or 1. ATLAS responds only to Type 0 accesses, since it is a device on the PCI bus.

A1	A0	Access Type
0	0	ATLAS access when idsel is asserted
0	1	Configuration access to another PCI bus (bridge)
1	X	Reserved

Snooping

ATLAS can perform snooping under the following two conditions:

1. When the VGA RAMDAC snooping bit is active.
2. When the 46E8 enabling feature is activated.

This cycle operates in two different ways:

- If there is no room in the input buffer then ATLAS takes control of the bus and a retry cycle is performed.
- If there is room in the input buffer then the data will be loaded when the data transfer occurs on the PCI bus.

Under normal conditions, only a subtractive agent will respond to the access. In this case, the snoop mechanism will function correctly. For other than normal conditions:

- If there is another device on the PCI bus that responds to this mapping, or if another device is performing the snoop mechanism with retry capabilities, then this will result in contention on the PCI bus.
- Burst mode is not supported in the snooping area. This is not supposed to append since bridges are not allowed to 'burst' consecutive I/O accesses, and CPUs do not perform burst on I/O accesses.
- If another device on the PCI bus performed the shortest cycle, then ATLAS will not be able to get the data, but the state machine will be able to recover.

6.2.1.2 PCI Cycles

The following resources are accessible to the PCI interface:

- Configuration register writing
- Input buffer writing to:
  - I/O
  - VGA frame buffer
  - Power Graphic mode memory space
- Configuration register reading
- Output buffer reading:
  - Power Grapic mode memory space (and pseudo DMA range when enabled)
- Direct reading from:
  - I/o
  - VGA frame buffer
  - Power Grapic mode memory space (except pseudo DMA range when enabled)
  - EPROM

Configuration Register Writing

These cycles will be of fixed length as far as ATLAS is concerned (no wait states are added by the master). To avoid burst, a disconnect cycle is performed when TRDYN is asserted.

Input Buffer Writing

This cycle operates under the following parameters:

- If there is room in the input buffer, the cycle is of fixed length.
- If there is no room in the input buffer, a retry cycle is performed.
- A retry cycle is performed when a 32 dword boundary is passed.
- A disconnect cycle is performed when TRDYN is asserted, to avoid burst during I/O access.

Configuration Register Reading

These cycles will be of fixed length as far as ATLAS is concerned (no wait states are added by the master). A disconnect cycle is performed when TRDY/ is asserted, to avoid burst.

Output Buffer Reading

This cycle operates under the following parameters:

- If there is data in the input buffer, then a retry cycle of fixed length is performed.
- If there is data in the output buffer, then the cycle is of fixed length.
- If there is no data in the output buffer, then a retry cycle of fixed length is performed.

Direct Read

This cycle operates under the following parameters:

. If there is data in the input buffer, then a retry cycle of fixed length is performed.

. If there is no data in the input buffer, then wait states are generated until ATLAS acknowledges the access. A disconnect cycle is performed when TRDY/ is asserted, to avoid burst.

6.2.1.3 Bus Sizing

The PCI bus does not support bus sizing. However, internal circuitry performs the bus sizing for the following devices: EPROM, I/O accesses, VGA register space in 16K windows (offset 1F00h - 1FFFh), and the VGA frame buffer.

When bus sizing is performed in the PCI interface, the access is performed in LSB/MSB order.

6.2.1.4 External Devices

The standard external devices can be connected to the ATLAS as shown in Figure 6-l.

When only the EPROM and RAMDAC are present, the decoder (138) is not required. If the DUBIC or another external device is required, then the decoder must be added to the design.

When accessing the 'external devices' memory space (offset 3C00h-3FFCh), all devices within this memory space are 8-bit, connected to byte 0 in the double-word address boundary. Byte, word and double-word accesses are allowed, but only byte0 is valid. Byte3, 2, and 1 are masked by ATLAS.

You can add other devices by using the EXPSL/ signal and external circuitry. Refer to Table 4-3 ('ATLAS Power Graphic Mode Memory Mapping') and the expdev bit of the CONFIG register description (which starts on page 5-43) for details about EXPSL/.

❖ Note: In the PCI configuration, the EXPSL/ signal is never activated with I/O commands.

The RAMDAC can be accessed by ATLAS in two distinct ways: in VGA mode by an I/O access, or in Power Graphic mode by a memory access. For I/O access to the RAMDAC, the ATLAS chip guarantees the recovery time between accesses to the palette that are required by some RAMDACs. This is guaranteed for pixel clocks that are greater than 10 MHz. For memory access to the RAMDAC, ATLAS does not guarantee the recovery time. In this case, the recovery time must be guaranteed by software.

6.2.2 ISA Interface

The ISA interface block diagram (Figure 6-2) shows how to connect ATLAS to the ISA bus, as well as to the local resources.

6.2.2.1 Bus Sizing

Since bus sizing is supported in ISA systems, there are only two limitations:

1. The first limitation occurs when accessing the 'vgareg' portion of the ATLAS memory space (offset 1F00h-1FFFh), with the ATLAS configured as a 16-bit device. Note that the 'vgareg' memory space can be accessed only in Power Graphic mode (vgaen = '0').

   Only byte accesses are allowed in this mapping. ATLAS will perform byte swapping from, or to, the byte0 of the internal data bus, since all 'vgareg' devices are connected to byte0. If an access is performed at an even address, the odd byte will be ignored, and if an access is performed at an odd address, the even byte will be ignored.

2. The second limitation occurs when accessing the 'external devices' memory space (offset 3C00h-3FFCh), in 8 or 16-bit mode. All devices in this memory space are 8-bit devices connected on AD<7:0>, and mapped into a double word address boundary. Byte, word and double word accesses are allowed, but only byte0 is valid. Byte3, byte2, and byte1 must be masked.

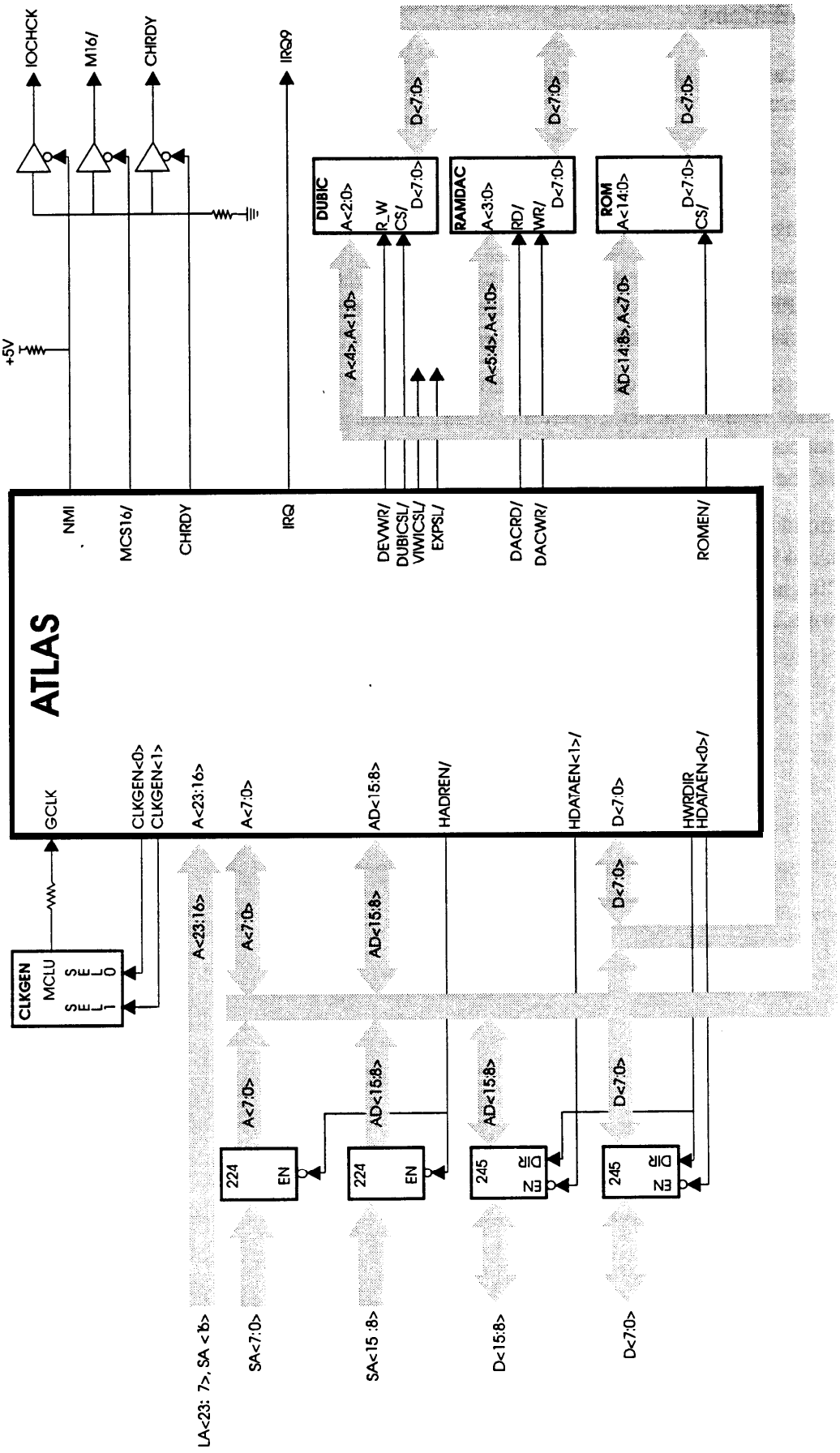


Figure 6-2: ISA Interface

6.2.2.2 External Devices

The standard external devices can be connected to the ATLAS as shown in Figure 6-2. Some timing restrictions for the external address and data buffers are assumed in order for the ATLAS chip to function properly. In addition to satisfying all ATLAS and system timings, the following constraints must also be respected.

1. The address buffers (244 type) must have a propagation delay of 10 ns or less, and an enable time of 11 ns or less.
2. The data transceivers must be able to drive the elevated capacitive load of the system data bus, and still guarantee a propagation delay of 10 ns or less and an enable time of 12 ns or less.

ATLAS provides the necessary control signals (HADREN/, HWRDIR, and HDATAEN<3:0>/) for the address and data buffers. When they are used as indicated, there is no contention on the multiplexed address and data bus. If these signals are modified or not used at all, extreme caution must be exercised, because the behavior of the multiplexed bus is not always obvious. During external device accesses in particular, the address is driven by ATLAS and not by the address buffer. Refer to Section A.2.3 for more information.

All external devices such as the RAMDAC, DUBIC, and ROM must be connected to byte 0 of the data bus. These devices are memory mapped to be double-word aligned. Only byte 0 accesses are allowed; accesses to other bytes will cause errors. Word and double-word accesses will cause unpredictable results.

You can add other devices by using the EXPSL/ signal and external circuitry. Refer to Table 4-3 ('ATLAS Power Graphic Mode Memory Mapping'), Table 4-5 ('I/O Mapping'), and the expdev bit of the CONFIG register description (which starts on page 5-43) for details about EXPSU. Since the EXPSL/ signal can be active in various memory and I/O ranges, you must take care to qualify the strobe to limit accesses to the desired range. Specifically, EXPSL/ may be active in the VGA I/O space, where only the 16 least significant address bits are decoded. Depending on how the strobe is used, it may be necessary to qualify EXPSL/ with the memory or I./O command strobe to eliminate any undesired effects.

The ATLAS chip doesn't provide any mechanism to guarantee the recovery time between accesses to the palette that some RAMDACs require. This constraint is often a function of the pixel clock, and can often become significant in length.

The RAMDAC can be accessed by ATLAS in two distinct ways: in VGA mode by an I/O access, or in Power Graphic mode by a memory access. In an ISA implementation, the I./O accesses are rarely a problem since the ISA specification for I/O accesses is usually sufficient to guarantee the RAMDAC constraint. In any other implementation, this parameter must be guaranteed by the hardware (through additional circuitry, if necessary) in order to guarantee VGA software compatibility. For memory accesses, since there is no software compatibility issue, the solution can be implemented in the software if it isn't guaranteed by the hardware.

6.3 VRAM Interface

ATLAS connects directly to the VRAM. All addresses and control signals of the random port are generated from ATLAS. Serial data and control lines are interfaced directly to the RAMDAC or to the DUBIC chip.

Different memory banks can be populated in order to achieve different resolutions. In every case, the fbm field of the OPMODE register selects a specific memory mapping. There are three major groups:

1. fbm = 00X. In this case no interleave is performed on the memory. In No DUBIC mode, the video data is generated using external multiplexers. In DUBIC mode, only one DUBIC is required to generate the video data. These modes can support 8, 16, or 32 bits/pixel formats. This group only supports 1MB VRAM.
2. fbm = 01X. In this case no interleave is performed on the memory. In No DUBIC mode, the video data is generated using external multiplexers. In DUBIC mode, only one DUBIC is required to generate the video data.. These modes can support 8, 16, or 32 bits/pixel formats. This group supports 2MB VRAMs.
3. fbm = 1XX. In these cases, interleave is performed on the memory, and two DUBICs are required to generate the video data. These mapping groups only support 24 or 32 bits/pixel. Refer to Section 3.2.1 for additional information on memory configuration.

❖ Tables 6- 1 and 6-2 show the possible configurations in No DUBIC mode and DUBIC mode, respectively. If a configuration is not listed, it is not supported, and can't be used. The columns under the resolutions represent the supported pixel depths.

Mapping Group I										*Resolution*					
Memory Bank											*768 x 576*				
0	*1*	*2*	*3*	*4*	*5*	-	*7*	*8*	*fbm*	*640 x 480*	*800 x 600*	*1024 x 768*	*1152 x 882*	*1280 x 1024*	*1600 x 1200*
X									000	16	16	8	8		
x	x								000	32	32	16	16	8	8

Mapping Group 2										*Resolution*					
Memory Bank											*768 x 576*				
0	*1*	*2*	*3*	*4*	*5*	-	*7*	*8*	*fbm*	*640 x 480*	*800 x 600*	*1024x 768*	*1152 x 882*	*1280 x 1024*	*1600 x 1200*
		X							010	32	32	16	16	8	8
		x	x						010	32	32	32	32	16	16

Table 6-1: Frame Buffer Config. (No DUBIC Mode)

Legend:

X Bank is fully populated

0 Bank is optionally populated

Mapping Group 1 Memory Bank										Resolution					
										768 x 576					
0	1	2	3	4	5	-	7	8	fbm	640 x 480	800 x 600	1024 x 768	1152 x 882	1280 x 1024	1600 x 1200
X					O				000	16	16	8	8		
X	X				O				000	32	32	16	16	8	8
									001	16	16				

Mapping Group 2 Memory Bank										Resolution					
										768 x 576					
0	1	2	3	4	5	-	7	8	fbm	640 x 480	800 x 600	1024 x 768	1152 x 882	1280 x 1024	1600 x 1200
		X			O				010	32	32	16	16	8	8
		xx			O				010	32	32	32	32	16	16

Mapping Group 3 Memory Bank										Resolution					
										768 x 576					
0	1	2	3	4	5	-	7	8	fbm	640 x 480	800 x 600	1024 x 768	1152 x 882	1280 x 1024	1600 x 1200
		P	P		O		X		100	24	24	24	24		
		X	X		O				100	32	32	32	32		
		P	P	P	O		X		101	24	24	24	24	24	
		X	X	X	O				101	32	32	32	32	32	

Mapping Group 4 Memory Bank										Resolution					
										768 x 576					
0	1	2	3	4	5	-	7	8	fbm	640 x 480	800 x 600	1024 x 768	1152 x 882	1280 x 1024	1600 x 1200
		P	P		O			O	110	24	24	24	24		
		X	X		O			O	110	32	32	32	32		
		P	P	P	O			O	111	24	24	24	24	24	
		X	X	X	O			O	111	32	32	32	32	32	

Table 6-2: Frame Buffer Config. (DUBIC Mode)

Legend:

X Bank is fully populated

P Bank is partially populated: VD<55:32> and VD<23:0>

0 Bank is optionally populated

Note that fbm=01 1 is not listed in these tables (refer to Section 3.2.1).

The eight memory banks are explained on the next page:

Bank 0: 8 x 128K x 8 VRAM. This memory is used as the frame buffer and is connected to VD<63:0>.

Bank 1: 8 x 128K x 8 VRAM. This memory is used as the frame buffer and is connected to VD<63:0>.

Bank 2: 8 or 6 x 256K x 8 VRAM. This memory is used as the frame buffer. In the fbm=2 configuration, eight chips are used, connected to VD<63:0>. In the fbm= 4, 5, 6, and 7 configurations, six or eight chips are used. The six-chip configuration is for 24 bits/pixel, and the chips are connected to VD<55:32> and VD<23:0>.

Bank 3: 8 or 6 x 256K x 8 VRAM. This memory is used as the frame buffer. In the fbm=2 configuration, eight chips are used, connected to VD<63:0>. In the fbm= 4, 5, 6, and 7 configurations, six or eight chips are used. The six-chip configuration is for 24 bits/pixel, and the chips are connected to VD<55:32> and VD<23:0>.

Bank 4: 8 or 6 x 256K x 8 VRAM. This memory is used as the frame buffer. The eight chip configuration is used for 32 bits/pixel, and the chips are connected to VD<63:0>. The six chip configuration is used for 24 bits/pixel, and the chips are connected to VD<55:32> and VD<23:0>.

Bank 5: 4 x 256K x 16 DRAM. This bank is used as off-screen memory. Bank 5 is connected to VD<63:0>.

Bank 6: Reserved.

Bank 7: 1 x 64K x 16 DRAM. This memory is used to fill up the VRAM Data bus to 64 bits for configurations where only 24 bits are supported. This allows some offscreen areas to be used for font storage. This bank is connected to VD<63:56> and VD<31:24>.

Bank 8: 4 x 256(64)K x 16 DRAM. This memory is used as off-screen memory. Bank 8 is connected to VD<63:0>.

6.3.1 Memory Interleave

In order to have enough bandwidth for 1280 x 1024 x 24 bits, some modes use interleave schemes to address the frame buffer. The memory interleave is selected when fbm = 1XX. Interleave is performed only in the VRAM (Banks 2, 3, and 4). The interleave is done on a four-slice basis, which means that four consecutive slices are put in one bank, then the next four slices are put in the other bank and so on. This four-slice scheme was chosen to make block mode operations easier.

For example, at the beginning of the frame buffer in 32 bits/pixel, the pixels are arranged as follows between the two banks:

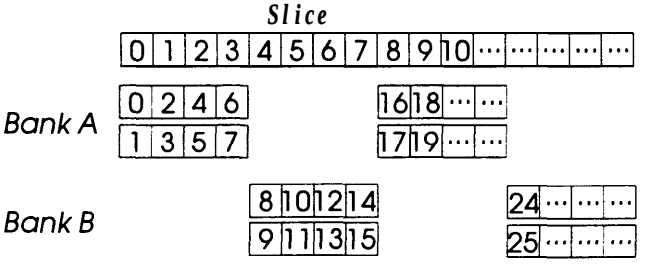


Figure 6-3: Pixel Arrangement

For fbm = 4 and 6, Banks A and B are assigned as follows:

Address	*Bank*	
(Bytes)	*A*	*B*
00000h-3FFFFFh	2	3

For fbm = 5 and 7, Banks A and B are assigned as follows:

Address	*Bank*	
(Bytes)	*A*	*B*
00000h-1FFFFFh	2	4
20000h-3FFFFFh	2	3
40000h-5FFFFFh	4	3

6.3.2 Patch RAM

The patch RAM is an optional device. Since for fbm = 1XX only 24(32) bits/pixel are supported, there's no need to populate the complete 64 bit data bus. However, offscreen memory can be used for font caching, patterns, and so on. Since the offscreen area accesses must be 64 bits, and the unused display bits are not contiguous, the patch RAM 'patches up the gaps' to support 64-bit data in the offscreen memory while the display area is only populated for 24 bits/pixel.

Since the patch RAM isn't used for video, normal DRAM can be used. Refer to Section 3.2.1 'Memory Configurations' for more information about where the patch RAM is mapped.

If Banks 2, 3 and 4 are fully populated, the patch RAM can't be used. Also, if DRAM is added to the system, the patch RAM may not be required, since some offscreen space will be available.

6.3.3 MCTLWTST Register Timings

The MCTLWTST (Memory Control Wait State) register is described in detail in Chapter 5. The following figures show the various cycles that are generated by the drawing engine. At the top of each timing diagram, the field of MCTLWTST that specifies the length of this state is shown.

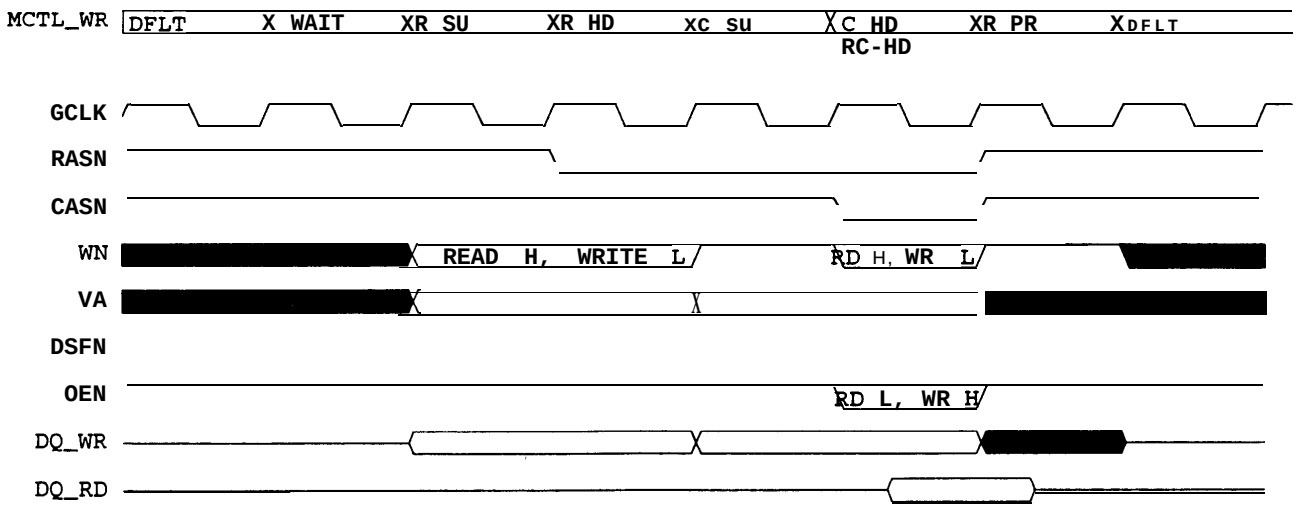


Figure 6-5: MCTLWTST for Direct Access Cycle

❖ During a direct read access, a state is added between RC-HD and R_PR, using the MCTLWTST wait field. This state has the same effect as the R_PR field on VRAM signals.

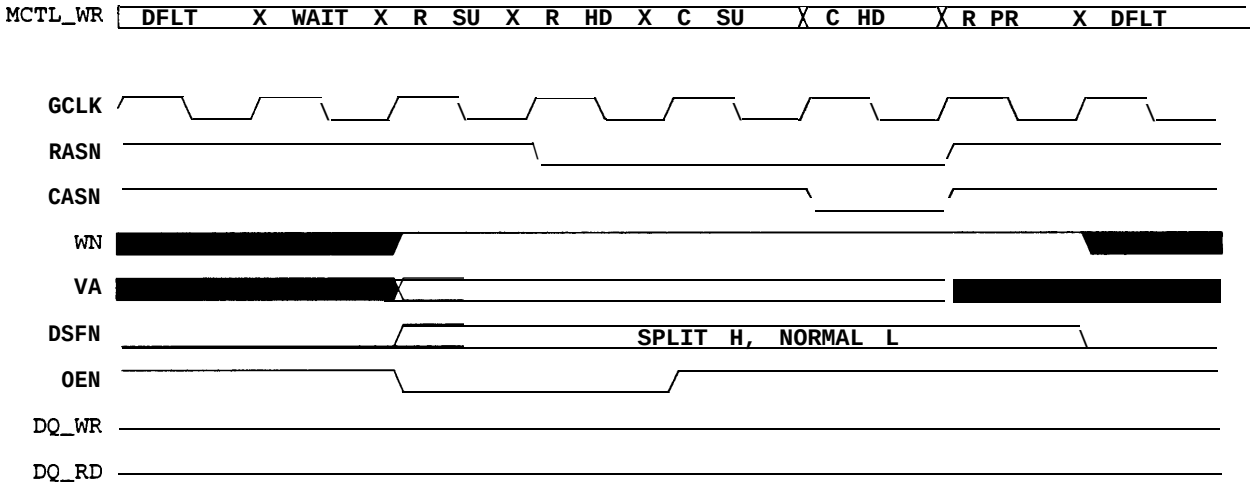


Figure 6-4: MCTLWTST for Data Transfer Cycle

OE<4:0>/ DT/OE strobe. Used for final bank selection during read cycles. There are five different DT/ strobes (two strobes in No DUBIC mode) generated by the ATLAS. This table shows how the DT/ signals generated by ATLAS are mapped to VRAM chips for each memory configuration.

	CAS/ or OE/								
fbm	*8*	*7*	*-*	*5*	*4*	*3*	*2*	*1*	*0*
000				2				1	0
001				2				1	0
010						0			
loo		4		2		0	1		
101		4		2	3	0	1		
110	4			2		0	1		
111	4			2	3	0	1		

Table 6-5: CAS and OE Assignment

WT<7:0>/ Write strobe. The Write strobes are used for pixel selection. Because the minimum pixel size is 8 bits/pixel, there is one strobe per byte.

DSF<1:0> Special function pin of the VRAM. This pin permits different types of data transfer (split – normal) simultaneously in different banks.

	DSF								
fbm	*8*	*7*	*-*	*5*	*4*	*3*	*2*	*1*	*0*
000								X	X
001								X	X
010						X	X		
100						X	X		
101					0	1	0		
110						X	X		
111					0	1	0		

X = ‘don’t care’

Table 6-6: DSF Assignment

6.3.5 Coprocessor Requests

Two pins permit sharing of the VRAM bus: BACK/ (generated by ATLAS) and BRQ/ (generated by the coprocessor).

When it releases the bus to the coprocessor, the ATLAS chip brings all VRAM control signals high before putting them in u-i-state. The coprocessor should do the same thing when releasing the bus. This procedure guarantees that no false access will be performed on the memory.

Figure 6-9 shows the normal sequence when the coprocessor requests and releases the bus.

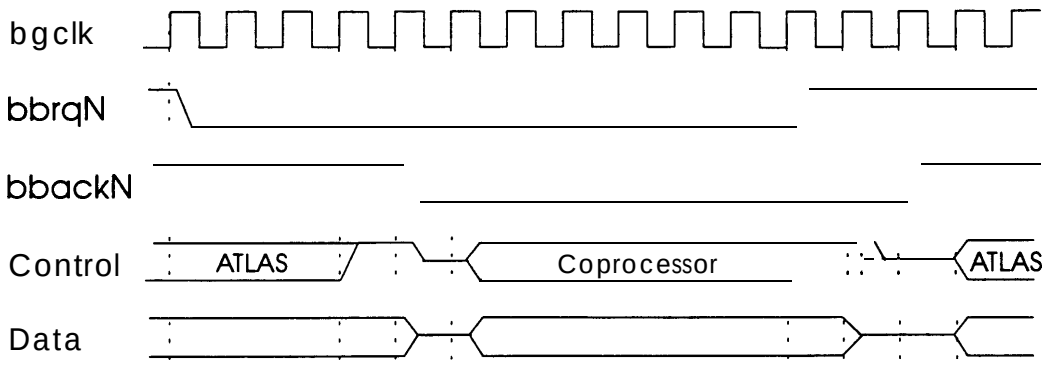


Figure 6-9: Normal Request and Release of the Bus

In order to allow the ATLAS chip to perform refresh cycles, the coprocessor must release the bus every 10 µS, for a minimum of one clock cycle. When the coprocessor releases the bus for only one clock cycle, ATLAS processes only the high priority refresh cycle. This is shown in Figure 6-10.

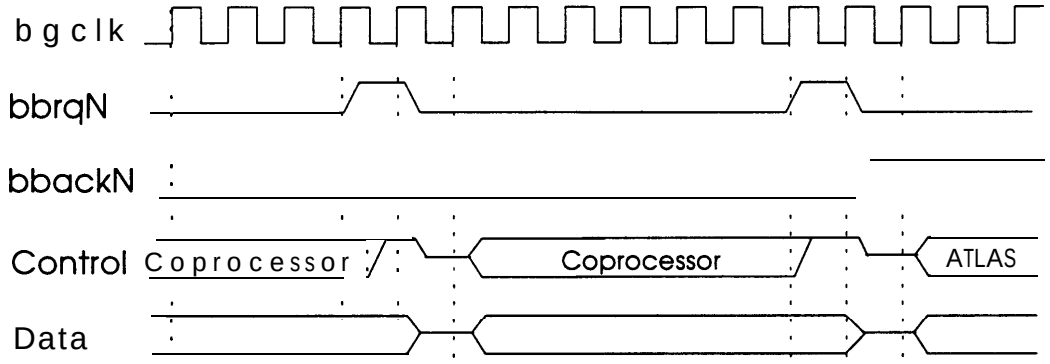


Figure 6-10: 1 gclk Release for Refresh

Finally, the ATLAS chip will notify the coprocessor that it requires the bus for a data transfer by removing the BACK/ signal. In this case, the coprocessor has a maximum of 20 clock cycles within which it must return the bus to the ATLAS. This is shown in Figure 6-l 1.

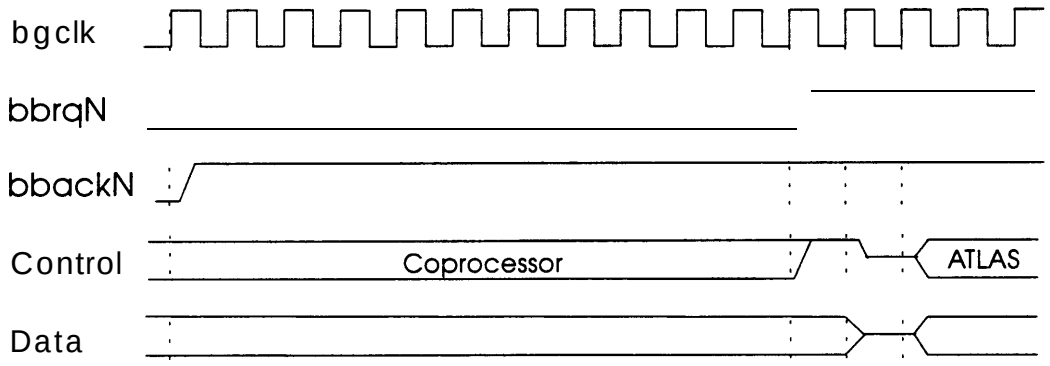


Figure 6-11: ATLAS Request for Data Transfer

6.4 VIDEO Interface

The video interface is different for Power Graphic mode and VGA mode. As well, Power Graphic mode supports the following two configurations: No DUBIC mode and DUBIC mode.

6.4.1 Power Graphic Mode (No DUBIC Mode)

In 'No DUBIC' mode, ATLAS itself is responsible for generating all the control signals for the VRAM serial port, the multiplexers and RAMDACs. Figure 6-12 shows the connection between ATLAS and a 32-bit RAMDAC (such as the BT-485). External multiplexers are required in a 32-bit interface, since the RAMDAC's pixel port is 32 bits, while the memory interface is 64 bits.

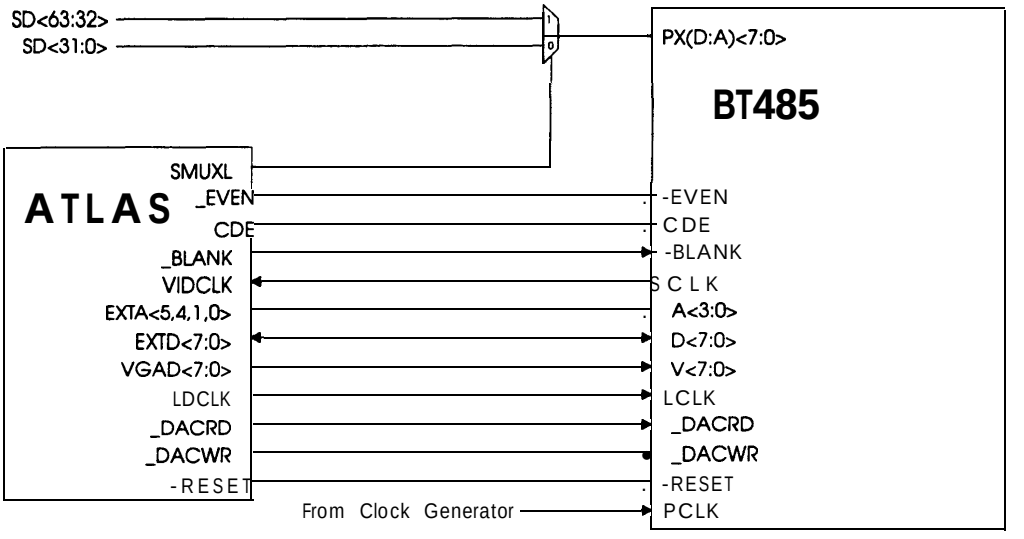


Figure 6-12: ATLAS/Memory Connection to 32 Bit RAMDAC

Figure 6-13 shows the connection between ATLAS and a 64-bit RAMDAC (such as the TI VIEWPOINT). No external multiplexing is required, since the RAMDAC's pixel port size matches that of the external memory interface.

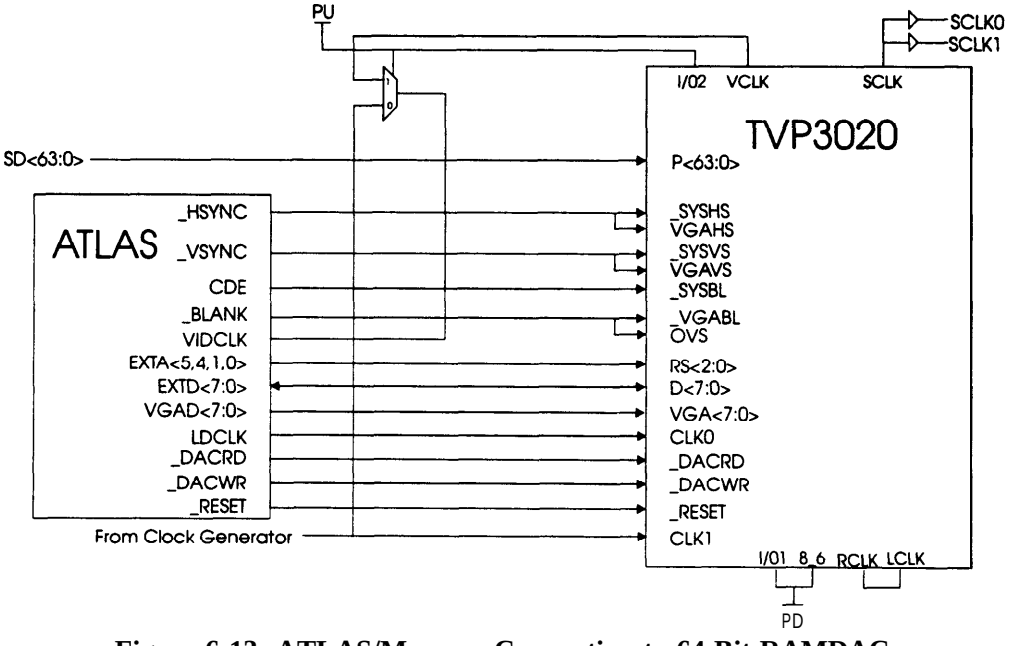


Figure 6-13: ATLAS/Memory Connection to 64 Bit RAMDAC

6.4.2 Power Graphic Mode (DUBIC Mode)

In Power Graphic mode when a DUBIC chip is present ('DUBIC mode'), controls are generated that cause the DUBIC chip to generate serial clocks to the VRAM as well as blank and sync signals for the video output.

In this mode, only the VIDINF pins are used for video generation.

VIDINF<3:0>	*Code Description*
0000	Horizontal and vertical sync and blank
0001	Horizontal sync and blank
0010	Vertical sync and blank
0011	Blank
0100	Display border color
0101	Active video
0110	Bank switching
0111	Vertical sync and blank (field 1)
1000	Data transfer in the current bank
1001	Bank switching and data transfer in the next bank
1110	Backward bank switch

Table 6-7: Power Graphic Mode Video Generation

Refer to the *DUBIC Specification* for more information on interconnecting the VRAM serial port, RAMDAC, DUBIC, and ATLAS.

6.4.3 VGA Mode

In VGA mode, ATLAS outputs different video signals, according to whether or not the system is operating in No DUBIC mode or in DUBIC mode. Refer to Table 6-8 for the signal assignment.

Signal Description	*No DUBIC Mode*	*DUBIC Mode*
, Pixel clock	LDCLK	VIDINF<3>
Blanking signal	BLANK/	VIDINF<2>
Horizontal sync signal	HSYNC/	VIDINF< 1 >
Vertical sync signal	VSYNC/	VIDINF<0>
VGA data <7>	VAA<11>	VAA<11>
VGA data <6>	VGAD<6>	OE<2>/
VGA data <5>	VGAD<5>	OE<4>/
VGA data <4>	VGAD<4>	OE<3>/

Table 6-8: VGA Signal Assignment

6.4.4 Slaving ATLAS

The VIDRSTN input pin of the chip is used to synchronize the MGA video with other external video sources.

Inside the CRTC circuitry, there are two 'total compare' signals (one for the horizontal counter, and one for the vertical counter). These signals reset the corresponding horizontal or vertical counter, based on the total values programmed in the registers.

Like the total compare signals, the VIDRSTN signal resets the horizontal and vertical counters. In other words, the VIDRSTN signal is responsible for initially synchronizing the video circuitry when it is necessary to get in phase with another video source. Two bits in the CRTC-CRTL register are used to enable the reset of either or both of the counters.

The VIDRSTN signal is periodic and must have exactly the same period as that obtained by the programmed video parameters. The period of VIDRSTN is either the same as the period of one line, or the same as the period of one frame (depending on the kind of synchronization that is necessary).

The first application of the signal will create a momentary instability in the video signals (blank, syncs, etc.). After this, the CRTC counters will be in phase with the VIDRSTN signal, and video signal generation will become stable.

When the vertical reset is used, the VIDRSTN signal is maintained internally until the next vertical clock (which is the horizontal retrace – this is also when the vertical counter is reset). It is necessary to send a VIDRSTN pulse of only one clock in length, once per frame (even in vertical reset).

In VGA mode, the VIDRST signal must be maintained active for a minimum of 8 VIDCLKs. In Power Graphic mode, VIDCLK is always divided by 8, so VIDRST can be maintained for only one VIDCLK.

The following figures illustrate the video signal waveforms and counters in relation to the video reset input signal once the CRTC is in phase with the video reset signal (VIDRSTN). The counter numbers are provided as sample values for a resolution of 1024 x 768.

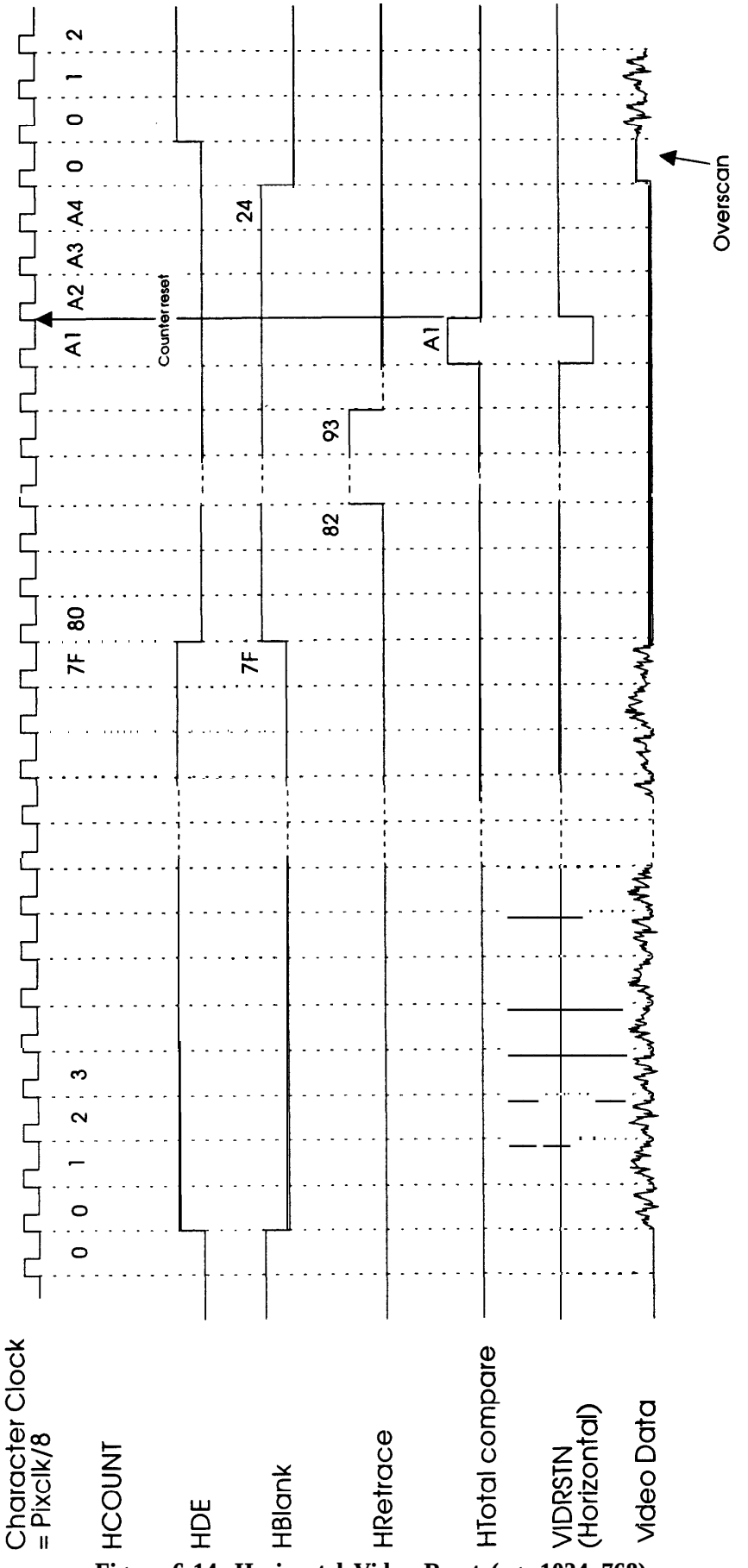


Figure 6-14: Horizontal Video Reset (eg. 1024x768)

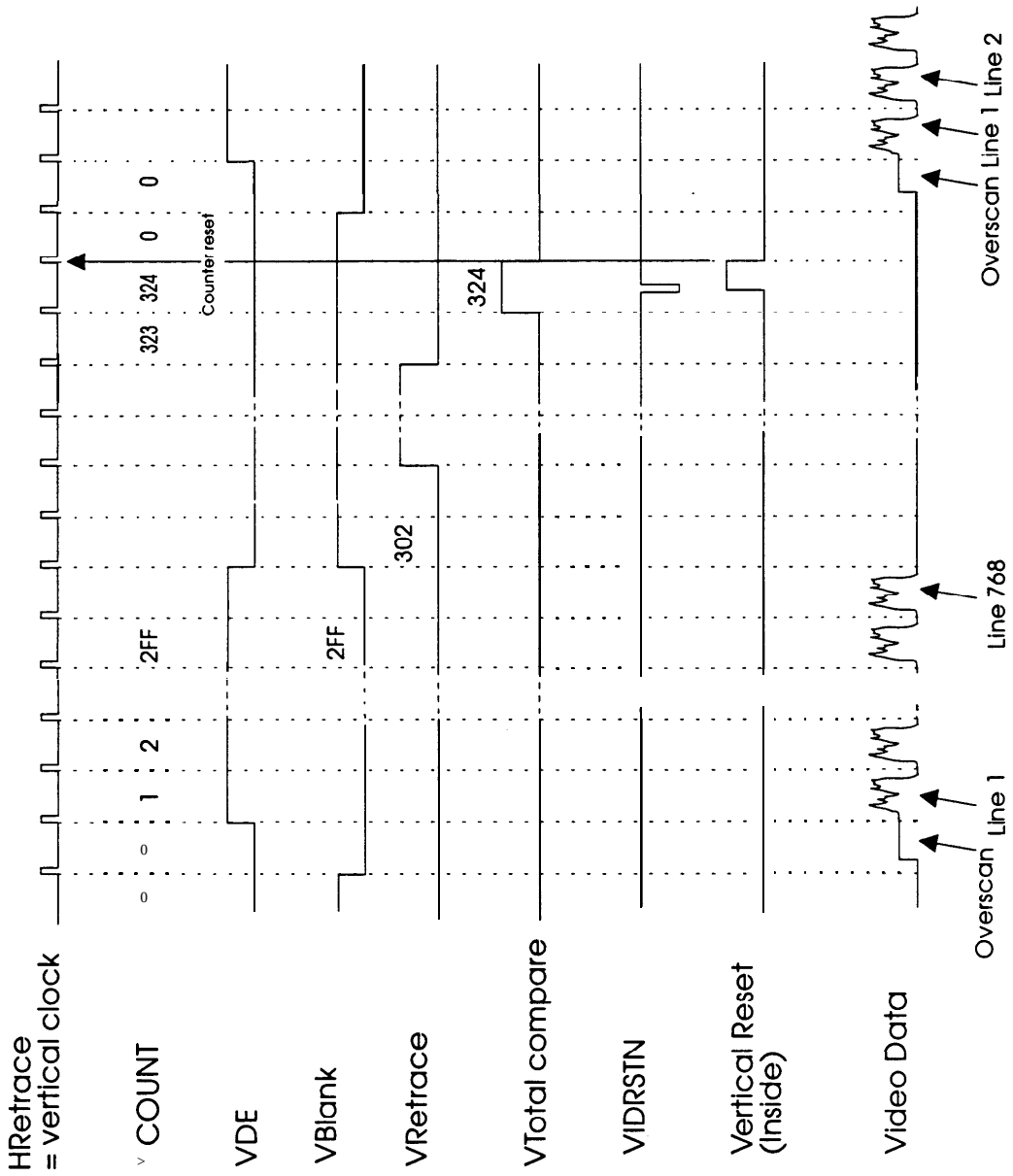


Figure 6-15: Vertical Video Reset (eg. 1024x768)

Appendix A: Technical Data

T

information.

A.1 Pin List

When groups of pins are listed together, they're presented in order from MSB to LSB.

A.1.1 Host Interface (ISA Configuration)

Name	*No. of pins*	*Type*	*Description*
A<23:16>	8	*I/O*	Partial Address bus. Not multiplexed. Pins: 10 17 29 48 97 143 144 175
A<7:0>	8	*I/O*	Partial Address bus. Not multiplexed. Pins: 162 153 127 126 125 124 123 113
AD<15:8>	8	*I/O*	Address and Data multiplexed bus. Pins: 152 134 133 112 111 103 102 98
D<7:0>	8	*I/O*	Partial Data bus. Not multiplexed. Pins: 74 58 57 49 38 30 19 18
HADREN/	1	*0*	Host ADdRess ENable. External address buffer enable. Pin: 96
HDATAEN<1:0>/	2	*0*	Host DATA byte ENable bus. External data buffer enable signals. Pins: 142 70
HWRDIR	1	*0*	Host WRite DIRection. External data buffer direction control signal. Pin: *158*
AEN	1	I	Address ENable signal. Prevents IO decodes during DMA cycles. Pin: 55
MCS16/	1	0	Memory Chip Select 16 signal. Pin: 90
CHRDY	1	0	ReaDY signal. Pin: 116
CHRDYEN/	1	0	This pin can be used to enable an external CHRDY buffer so that the bus ready signal is driven high before being disabled. Pin: 105
REFRESH/	1	I	REFRESH cycle signal. Prevents memory decodes during bus refresh cycles. Pin *86*
MRDC/	1	I	Memory ReaD Control strobe. Pin: 82
MWTC/	1	I	Memory WriTe Control strobe. Pin: 84

Name	*No. of pins*	*Type*	*Description*
IORC/	1	I	I/O Read Control strobe. Pin: 91
IOWC/	1	I	I/O Write Control strobe. Pin: 106
BALE	1	I	Bus Address Latch Enable signal. Pin: 69
SBI-W	1	I	System Bus High Enable signal. Pin: 99
IRQ	1	0	Interrupt ReQuest signal. - The same interrupt is used for ATLAS and VGA. - A shared interrupt protocol is used in Power Graphic mode, but not in VGA mode. - There is a rising edge trigger (ISA type) interrupt in VGA mode. - There is a negative level interrupt option in Power Graphic mode. - Open collector output. Pin: 171
NMI/	1	0	Generate an NMI to the host CPU for CGA-Hercules CRTC register emulation. This pin is connected to the IOCHW pin on ISA. It is useful only if the ATLAS VGA is used. Pin: 83
DECODE<1 :0>/	2	I	Optional high level DECODE pins which should be pulled down when not used. Refer to the map table in the CONFIG register description in Chapter 5 (page 5-43) for more information. Pins: 73 72
ISA	1	0	Indicates that the ATLAS is operating in the ISA configuration and not in the PCI configuration. Pin: 56
DRQ	1	0	DMA ReQuest signal. Refer to Section 3.2.4 for more information. Pin: 104
DAK/	1	I	DMA AcKnowledge signal. Refer to Section 3.2.4 for more information. Pin: 157
TC	1	I	Terminal Count signal. Refer to Section 3.2.4 for more information. Pin: 118
PU	2	I	Connected to a pull-up. Pins: 107 115
NC	2	0	No Connect signals. Pins: 114 156

A.I.2 Host Interface (PCI Configuration)

Name	*No of pins*	*Type*	*Description*
PCLK	1	I	This CLocK provides timing for all transactions on PCI. **Pin: 86**
PCBE<3:0>/	4	I	PCI Bus Command and Bytes Enables are multiplexed on the same PCI pins. During the address phase of a transaction, PCICBE<3:0> defines the bus command. During the data phase, the PCICBE<3:0> signals are used as byte enables. **Pins: 156 114 142 70**
PAD<31:0>	32	I/O	Address and Data multiplexed bus. During the first clock of a transaction PCIAD<31:0> contains a physical address; during subsequent clocks PCIAD<31:0> contains data. **Pins: 10 17 29 48 97 143 144 175** **162 153 127 126 125 124 123 113** **152 134 133 112 111 103 102 98** **74 58 57 49 38 30 19 18**
PPAR	1	0	PARity is even across PCIAD<31:0> and PCICBE<3:0>. Parity is generated during read data phases. **Pin: 83**
PFRAME/	1	I	Cycle FRAME indicates the beginning and duration of an access. **Pin: 96**
PTRDY/	1	0	Target ReaDY indicates the ATLAS chip's ability to complete the current data phase of the transaction. It is used in conjunction with IRDY/. Wait cycles are inserted until both IRDY/ and TRDY/ are asserted together. **Pin: 82**
PIRDY/	1	I	Initiator ReaDY indicates the initiating agent's ability to complete the current data phase of the transaction. It is used in conjunction with TRDY/. Wait cycles are inserted until both IRDY/ and TRDY/ are asserted together. **Pin: 116**
PDEVSEL/	1	0	DEVice SELect, when actively driven, indicates that the ATLAS chip has decoded its address as the target of the current access. **Pin: 84**
PSTOP/	1	0	STOP indicates that ATLAS is requesting that the master device halt the current transaction. **Pin: 91**

PINTA	1	0	INTerrupt ReQuest signal. - The same interrupt is used for ATLAS and VGA. - A shared interrupt protocol is used in Power Graphic mode, but not in VGA mode. - There is a rising edge trigger (ISA type) interrupt in VGA mode. - There is a negative level interrupt option in Power Graphic mode. - Open collector output. Pin: 171
PIDSEL	1	I	Initialization Device SELect is used as a chip select in lieu of the upper 24 address lines during configuration read and write transactions. Pin: 105

A.I.3 External Device Interface (ISA Configuration)

Name	*No. of pins*	*Type*	*Description*
DACRD/	1	0	ramDAC ReaD control strobe. Pin: 138
DACWR/	1	0	ramDAC WRite control strobe. Pin: 137
ROMEN/	1	0	BIOS ROM ENable strobe. Pin: 117
DEVWR/	1	0	external DEVice WRite. This pin indicates if the current external device cycle is a read (1) or a write (0). Pin: 109
DUBICSU	1	0	DUBIC SeLect strobe. This pin works in conjunction with the DEVWR/ signal. Pin: 154
VIWICSL/	1	0	VIWIC SeLect strobe. This pin works in conjunction with the DEVWR/ signal. Pin: 155
EXPSL/	1	0	EXPansion SeLect control strobe. This pin can be used as the VGA expansion write signal or for other expansion devices when EXPDEV/ is active. In this case, external decoding circuitry is required. Pin: 141
CLKGEN<1 :0>	2	0	Clock generator control bits. These bits come from the VGA Miscellaneous Output Register 3C2<3:2>. Pins: 129 128

A.I.4 External Device Interface (PCI Configuration)

Name	*No of pins*	*Type*	*Description*
EXTA<6:0>	7	0	EXTemal device Addresses. If external devices are enabled, the EXTA<3:2> bits are used as second and first decoder addresses, and EXTA<6> is used as a R/W signal. Pins: 158 157 118 69 154 155 141
EXTD<7:0>	8	I/O	EXTemal Device data bus. This bus is also used as EXTA<14:7> for EPROM accesses. Pins: 115 56 104 107 99 55 73 72
ROMEN/	1	0	BIOS ROM output ENable signal. This pin is also used as the chip select by the external decoder for other external devices. Pin: 117
EIRQ/	1	I	External device Interrupt ReQuest. Pin: 90
DACRD/	1	0	RAMDAC ReaD control signal. If external devices are enabled, this bit is used as the decoder enable strobe. Pin: 138
DACWR/	1	0	RAMDAC WRite control signal. If external devices are enabled, this bit is used as the third decoder address. Pin: 137
CLKGEN<1:0>	2	0	CLOCK GENerator control bits which emanate from the VGA Miscellaneous Output register (3C2<3:2>). Pins: 129 128
EXTALEN	1	0	EXTernal Address Latch. This pin is used to latch the MSB addresses in an external latch when an EPROM access is performed. This pin is also used as a chip select on the EPROM, and as a positive chip select by the external decoder for other external devices. Pin: 106
DEVRST/	1	0	DEVice ReSeT. Reset output generated for local devices. Pin: 109

A.1.5 Drawing Engine (No DUBIC Mode)

Name	*No of pins*	*Type*	*Description*
VD<63:0>	64	I/O	Video Data bus. These pins are connected to VRAM and DRAM. Pins: 131 136 147 148 149 165 166 167 168 176 177 178 182 183 184 185 195 196 197 203 204 205 206 212 213 214 215 216 224 225 226 232 233 234 235 236 237 8 9 14 15 16 25 26 27 28 34 35 36 37 42 43 44 53 54 62 63 64 65 75 76 77 87 93
VAA<13:0>	14	0	VRAM and DRAM multiplexed addresses. This bus includes all of the different addresses that must be generated for all banks of VRAM and DRAM. Refer to Table 6-3 for more information. Pins: 146 164 186 187 188 198 189 199 217 218 3 23 33 94
VAB<6:0>	7	0	VRAM and DRAM multiplexed addresses. This bus includes all the addresses that are the same for Power Graphic mode (duplicated for load distribution) but different in VGA mode (for character modes). Refer to Table 6-3 for more information. Pins: 207 208 227 231 22 32 78
RAS<1:0>/	*2*	*0*	RAS/ strobe, used for bank selection. Five different RAS/ strobes are generated by ATLAS. Refer to Table 6-4 for more information. Pins: 238 239
CAS<1:0>/	*2*	*0*	CAS/ strobe, used for final bank selection during write cycles. Five different CAS/ strobes are generated by ATLAS. Refer to Table 6-5 for more information. Pins: 12 39
OE<1:0>/	*2*	*0*	DT/OE strobe, used for final bank selection during read cycles. Five different DT/ strobes are generated by ATLAS. Refer to Table 6-5 for more information. Pins: 163 173
WT<7:0>/	*8*	*0*	WriTe strobes, used for pixel selection. Because the minimum pixel depth is 8 bits/pixel, there is one strobe per byte. The ninth strobe is unused. Pins: 174 209 219 13 45 46 51 52
DSF<1:0>	*2*	*0*	Special Function pin of the VRAM. This pin permits different types of data transfer (split/normal) simultaneously in different banks. Refer to Table 6-6 for more information. Pins: 68 135
BRQ/	1	I	Co-processor VRAM Bus ReQuest. Pin: 6
BACK/	1	0	ACKnowledge from ATLAS of the VRAM bus request. Pin: 7

A.I.6 Drawing Engine (DUBIC Mode)

Name	*No. of pins*	*Type*	*Description*
VD<63:0>	64	I/O	Video Data bus. These pins are connected to VRAM and DRAM. **Pins:** 131 136 147 148 149 165 166 167 168 176 177 178 182 183 184 185 195 196 197 203 204 205 206 212 213 214 215 216 224 225 226 232 233 234 235 236 237 8 9 14 15 16 25 26 27 28 34 35 36 37 42 43 44 53 54 62 63 64 65 75 76 77 87 93
VAA<13:0>	14	0	VRAM and DRAM multiplexed Addresses. This bus includes all the addresses that must be generated for all banks of VRAM and DRAM. Refer to Table 6-3 for more information. **Pins:** 146 164 186 187 188 198 189 199 217 218 3 23 33 94
VAB<6:0>	*7*	*0*	VRAM and DRAM multiplexed Addresses. This bus includes all the addresses that are the same for Power Graphic mode (duplicated for load distribution) but are different in VGA mode (for character mode). Refer to Table 6-3 for more information. **Pins:** 207 208 227 231 22 32 78
RAS<4:0>/	*5*	*0*	RAS/ strobe. Used for bank selection. There are five different RAS/ strobes generated by ATLAS. Refer to Table 6-4 for more details. **Pins:** 47 222 223 238 239
CAS<4:0>/	*5*	*0*	CAS/ strobe. Used for final bank selection during write cycles. There are five different CAS/ strobes generated by ATLAS. Refer to Table 6-5 for more information. **Pins:** 88 202 4 12 39
OE<4:0>/	*5*	*0*	DT/OE strobe. Used for final bank selection during read cycles. There are five different DT/ strobes generated by ATLAS. Refer to Table 6-5 for more information. **Pins:** 89 145 194 163 173
WT<7:0>/	*9*	*0*	WriTe strobe. Write strobes are used for pixel selection. Because the minimum pixel size is 8 bits/pixel, there is one strobe per byte. The ninth strobe is unused. **Pins:** 174 209 219 13 45 46 51 52
DSF< 1 :0>	*2*	*0*	Special Function pin of the VRAM. This pin permits different types of data transfer (split - normal) simultaneously in different banks. Refer to Table 6-6 for more information. **Pins:** 68 135

BRQ/	1	I	Co-processor VRAM Bus ReQuest. Pin: 6
BACK/	1	0	ACKnowledge from the ATLAS of the VRAM bus request. Pin: 7
NC	1	I/O	Not Connected. Pin: 67

A.I.7 Video Interface (No DUBIC Mode)

Name	*No of pins*	*Type*	*Description*
VIDCLK	1	I	Input CLOCK for the CRTC and the DT request module in Power Graphic mode. Pin: 229
VIDRST/	1	I	VIDeo ReSeT input. Pin: 159
HSYNC/	1	0	Horizontal SYNC. In VGA mode, sync polarity is selected from the VGA control register. In Power Graphic mode, the sync is always active low. Pin: 211
VSYNC/	1	0	Vertical SYNC. In VGA mode, sync polarity is selected from the VGA control register. In Power Graphic mode, the sync is always active low. Pin: 169
BLANK/	1	0	Video BLANK signal. Pin: 193
CDE	1	0	Video CDE signal. Pin: 223
LDCLK	1	0	Video CLOCK. Pin: 191
VGAD<6:0>	7	0	VGA Data output. VGAD<7> is multiplexed with VAA<11>. Pins: 194 89 145 24 66 79 95
SC<1:0>	2	0	Serial Clock. Each half-bank is connected to one of these serial clock pins. Pins: 88 202
SOE<1:0>/	2	0	Serial Output Enable control for each bank. Pins: 47 222
EVEN/	1	0	EVEN line signal (used for interlace operation only). The even field is defined as the field that starts with line two, while the odd field starts with line one. Pin: 67
SMUXSL	1	0	Serial MUX Low input select. This pin connects directly to the select pin of the muxes. Pin: 4

A.I.8 Video Interface (DUBIC Mode)

Name	*No. of pins*	*Type*	*Description*
VIDCLK	1	I	Input CLOCK for the CRTC and the DT request module in Power Graphic mode. Pin: 229
VIDRST/	1	I	VIDeo ReSeT input. Pin: 159
VIDINF<3:0>	4	0	VIDeo INFormation (to DUBIC). Refer to Table 6-7 for more information. Not available in No DUBIC mode. Pins: 191 193 211 169
VGAD<3:0>	4	0	VGA Data output. Pins: 24 66 79 95

A.1 .9 Miscellaneous

A.I.9.1 Fixed

Name	*No of pins*	*Type*	*Description*
GCLK	1	I	Graphic (and host interface) CLocK. Pin: 151
RESET/	1	I	This is an active low hard RESET pin. Pin: 119

A.7.9.2 Test

Name	*No of pins*	*Type*	*Description*
HIZ	1	I	This pin is used to put all bi-directional buffers in tri-state. This pin should be tied to a pull-down resistor on all products. Pin: 108
SCANEN	1	I	This is the SCAN chain ENable signal. A '1' on this pin will cause the scan chain to be active. This pin should be tied to a pull-down resistor on all products. Pin: 5
<SCANIN>	1	I	SCAN chain INput. This is a shared pin. Pin: 6
<SCANOUT>	1	0	SCAN chain OUTput. This is a shared pin. Pin: 7
<NANDTREE>	1	0	Output of the NAND TREE. This is a shared pin. Pin: 109
<RINGOSC>	1	0	Output of the RING OSCillator (the ring oscillator is enabled when the chip is in reset). This is a shared pin. Pin: 158

A.1.9.3 VCC/GND

Name	*No of pins*	*Type*	*Description*
PWR	16		Attached to +5 Volts.
			Pins: 21 40 61 81 100 120 132 140
			160 172 181 190 201 220 228 240
GND	29		Attached to GrouND.
			Pins: 1 2 11 20 31 41 50 59
			60 71 80 85 92 101 110 121
			122 130 139 150 161 170 179 180
			192 200 210 221 230

A.2 Electrical Specification

A.2.1 Maximum Ratings

. Storage Temperature: -40° C. to +125° C.

- DC Supply Voltage: -0.5 V to +7.0 V
- I/O pin voltage with respect to VSS: -0.5 V to VDD + 0.5 V

A.2.2 DC Specifications

. For VDD = 5.0 +- 5% , Ta = 0 to 70° C.

Symbol	*Parameter*	*Conditions*	*Min.*	*Typical*	*Maximum*	*Units*
VIL	Input low voltage				0.8	V
VIH	Input high voltage		2.2			V
VOL	Output low voltage I=IOL				0.4	V
		IOL=0			0.1	V
VOH	Output high voltage I=IOH		2.4			V
		IOH=0	V_{DD} -0.1			V
VT	Switching Threshold	Schmidt buffer (SC) Positive going	1.2		2.4	V
		Schmidt buffer (SC) Negative going	0.6		1.8	V
IIL	Input low current		-10			µA
		With pull up (PU)	-40	-100	-270	µA
IIH	Input high current				10	µA
		With pull down (PD)	40	100	270	µA
ICC	Power supply current				300	mA
IOL	Output low current	Applies to signals with 6 mA drivers			6	mA
		Applies to signals with 9 mA drivers			9	mA
		Applies to signals with 12 mA drivers			12	mA
		Applies to signals with 18 mA drivers			18	mA
		Applies to signals with PCI buffers			33	mA
IOH	Output high current	Applies to signals with 6 mA drivers			-3	mA
		Applies to signals with 9 mA drivers			-4.5	mA
		Applies to signals with 12 mA drivers			-6	mA
		Applies to signals with 18 mA drivers			-9	mA
		Applies to signals with PCI buffers			-12	mA
IOZ	Output tri-state current				10	µA
C	Pin capacitance			10	20	pF

Table A-l: DC Specification

Signal Name	*Drive Strength (mA)*	*Comment*	*Maximum Load (pF)*
A<23:16>	18	PU	70
AD<15:12>	18	PU	loo
AD<11:8>	18	PU	130
D<7:0>	18	PU	130
HADREN/	9	PU	60
HDATAEN<1:0>/	9	PU	40
HWRDIR	18	PU	70
AEN		PU	
MCS16/	18	PU	45
CHRDY	18	PU	45
CHRDYEN/	9	PU	30
RESET/		PU	
REFRESH/			
MRDC/			
MWTC/			
IORC/			
IOWC/		PU	
BALE		PU	
SBHE/		PU	
IRQ	12	Open Drain	120
NMI/	18	PU	240
DECODE<1:0>/	18	PU	70
ISA	18	PU	60
DRQ	18	PU	120
DAK/		PU	
TC		PU	

Table A-2: Host Interface (ISA) Signal Buffers

Signal Name	*Drive Strength (mA)*	*Comment*	*Maximum Load (pF)*
PCLK			
PCBE<3:0>		PU	
PAD<31:0>	18	PU	50
PPAR	18	PU	50
PFRAME/		PU	
PTRDY/	PCI		50
PIRDY/		PU	
PDEVSEL/	PCI		50
PSTOP/	PCI		50
PINTA	12	Open Drain	50
PIDSEL		PU	

Table A-3: Host Interface (PCI) Signal Buffers

Signal Name	*Drive Strength (mA)*	*Comment*	*Maximum Load (pF)*
DACRD/	18	PU	40
DACWR/	18	PU	40
ROMEN/	18	PU	40
DEVWR/	18		70
DUBICSL/	18	PU	40
VIWICSL/	18	PU	40
EXPSL/	18	PU	40
CLKGEN<1:0>	18	PU	25

Table A-4: External Device Signal Buffers (ISA)

Signal Name	*Drive Strength (mA)*	*Comment*	*Maximum Load (pF)*
EXTA<6:0>	18	PU	60
EXTD<7:0>	18	PU	70
ROMEN/	18	PU	40
EIRQ/		PU	
DACRD/	18	PU	40
DACWR/	18	PU	40
CLKGEN<1:0>	18	PU	25
EXTALEN	18	PU	50
DEVRST/	18	PU	50

Table A-5: External Device Signal Buffers (PCI)

Signal Name	*Drive Strength (mA)*	*Comment*	*Maximum Load (pF)*
VD<63:0>	18		58
VAA<13,12,8>	18	PU	108
VAA<11,10,7>	18	PU	94
VAA<9,6:0>	18	PU	130
VAB<6:0>	18	PU	122
RAS<1:0>/	18	PU	93
CAS<1:0>/	18	PU	93
OE<1:0>/	18	PU	93
WT<7:0>/	18	PU	58
DSF<1:0>	18	PU	100
BRQ/		PU	
BACK/	18		30

Table A-6: Drawing Engine Signal Buffers (No DUBIC)

Signal Name	*Drive Strength (mA)*	*Comment*	*Maximum Load (pF)*
GCLK			
VD<63:0>	18		58
VAA<13,12,8>	18	PU	108
VAA<11,10,7>	18	PU	94
VAA<9,6:0>	18	PU	130
VAB<6:0>	18	PU	122
RAS<4:0>/	18	PU	93
CAS<4:0>/	18	PU	93
OE<4:3>/	18	PU	44
OE<2>/	18	PU	79
OE<1:0>/	18	PU	93
WT<7:0>/	18	PU.	58
DSF<1:0>	18	PU	100
BRQ/		PU	
BACK/	18		30

Table A-7: Drawing Engine Signal Buffers (DUBIC)

Signal Name	*Drive Strength (mA)*	*Comment*	*Maximum Load (pF)*
VIDCLK/			
VIDRST/		PU	
HSYNC/	18	PU	40
VSYNC/	18	PU	40
BLANK/	18	PU	40
CDE	18	PU	40
LDCLK	9	PU	40
VGAD<6:0>	18	PU	51
SC< 1 :o>	18	PU	93
SOE< 1 :0>/	18	PU	93
EVEN/	9	PU	40
SMUXSL	18	PU	93

Table A-8: Video Interface Signal Buffers (No DUBIC)

Signal Name	*Drive Strength (mA)*	*Comment*	*Maximum Load (pF)*
VIDCLK			
VIDRST/		PU	
VIDINF<2:0>	18	PU	40
VIDINF<3>	9	PU	40

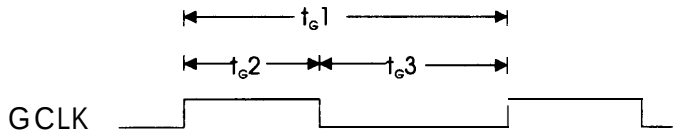
Table A-9: Video Interface Signal Buffers (DUBIC)

Signal Name	*Drive Strength (mA)*	*Comment*	*Maximum bad (pF)*
GCLK			
RESET/		PU	
HIZ		PD	
SCANEN		PD	
<SCANIN>		PU	
<SCANOUT>	18		30
<NANDTREE>	18		70
<RINGOSC>	18	PU	70
Power pins			
Ground pins			

Table A-10: Miscellaneous Signal Buffers

A.2.3 AC Specifications

A.2.3.1 GCLK



Signal	*Min*	*Max*	*Description*
t_G1	20 ns	28 ns	GCLK period
t_G2	8 ns		GCLK high
t_G3	8 ns		GCLK low

A.2.3.2 Host Interface Timing

The host interface waveforms and parameter lists are found on the pages which follow.

Figure A-l: ISA Host Interface Waveform

Ref.	Min (ns)	Max (ns)	Comments	Notes
Tsu1	20		aen → iorc/ iowc/ LOW	
Th2	15		aen (HOLD) → iorc/ iowc/ HIGH	
Tsu3	40		refreshN → mrdc/ LOW	
Th4	6		refreshN (HOLD) → mrdc/ HIGH	
Tsu5	15		decode< 1 :0>/ → mwtc/ mrdc/ iorc/ iowc/ LOW	
Th6	5		decode<1:0>/ (HOLD) → mwtc/ mrdc/ iorc/ iowc/ HIGH	(1) (4)
Tsu7	10		decode<1:0>/ → bale LOW	
Th7	3		decode<1:0>/ (HOLD) → bale LOW	
Tsu8	14		sbhe/ → mwtc/ mrdc/ iorc/ iowc/ LOW	(1)
Th9	10		sbhe/ (HOLD) → mwtc/ mrdc/ iorc/ iowc/ HIGH	(1)
Tsu14	19		ad<15:0> (ADDR) → mwtc/ mrdc/ iorc/ iowc/ LOW	(1)
Th14	10		ad<15:0> (ADDR) (HOLD) → mwtc/ mrdc/ iorc/ iowc/ LOW	(1)
Tsu15	6		ad<15:0> (ADDR) → bale LOW	(1)
Th15	5		ad<15:0> (ADDR) (HOLD) → bale LOW	(1)
Tsu16	19		adc23: 16> (ADDR) → mwtc/ mrdc/ iorc/ iowc/ LOW	(1)
Th17	10		ad<23:16> (ADDR) (HOLD) → mwtc/ mrdc/ iorc/ iowc/ HIGH	(1) (4)
Tsu18	6		ad<23:16> (ADDR) → bale LOW	(1)
Th18	5		ad<23:16> (ADDR) (HOLD) → bale LOW	(1)
Tsu19	20		bale HIGH → mwtc/ mrdc/ iorc/ iowc/ LOW	
Th20	15		bale LOW (HOLD) → mwtc/ mrdc/ iorc/ iowc/ HIGH	
Ta21	8		bale HIGH	
Tde122	55		mwtc/ mrdc/ iorc/ iowc/ HIGH → bale LOW	(15)
Ta24	85 3*gclk+13		mwtc/ mrdcl iorc/ iowc/ ACTIVE	(18)
	130		iowc/ ACTIVE	(2)
	215		iorc/ ACTIVE	(5)
Tr24	65 2*gclk+15		mwtc/ mrdc/ iorc/ iowc/ RECOVERY	(18)
	3*gclk+250		mwtc/ mrdc/ iorc/ iowc/ RECOVERY	(9)
Tsu25	20		ad<15:0> (DATA) → mwtc/ iowcl HIGH	
	10		ad<15:0> (DATA) → iowc/ HIGH	(2)
Th25	5		ad<15:0> (DATA) (HOLD) → mwtc/ iowc/ HIGH	
	5		ad<15:0> (DATA) (HOLD) → iowc/ HIGH	(2)
Tde126		51	mwtc/ LOW → ad<7:0> (DATA)	(8)
Tpd27		60	mrdcl iorc/ LOW → adc 15:0> (OUTPUT DATA)	
		120	iorcl LOW → ad<7:0> (OUTPUT DATA)	(5)
Tpa27	3	60	mrdc/ iorcl LOW → ad<15:0> (DATA) ACTIVE	(16)
	3	120	iorc/ mrdcl LOW → ad<7:0> (DATA) ACTIVE	(16) (5) (7)
Tpz28	3	20	mrdc/ iorc/ HIGH → ad<15:0> (DATA) TRISTATE	(16)
Tpi28	0		mrdcl iorc/ HIGH → ad<15:0> (DATA) invalid	
Tde129		0	chrdy → ad<15:0> (OUTPUT DATA)	
		60	chrdy → ad<7:0> (OUTPUT DATA)	(7)
Tpd30		29	mwtc/ mrdc/ iorc/ iowc/ LOW → chrdy LOW	(5) (6) (7) (8)
		21	mwtcl mrdcl iorc/ iowc/ LOW → chrdy LOW	
Th3 1	0		mwtc/ mrdc/ iorcl iowc/ LOW (HOLD) → chrdy HIGH	
Tpd32		25	mwtc/ mrdc/ iorc/ iowc/ LOW → chrdyen LOW	(1)
Tpd34		18	ad<16:0> (ADDR) → mcs 16/	(1) (10)

(continued on the next page)

Ref.	Min (ns)	Max (ns)	Comments	Notes
Tpd35		18	adc23: 17> (ADDR) → mcs16/	(1)
Tpd36		18	decode< 1 :0>/ → mcs 16/	
Tpd38		70	mwtc/ mrdc/ HIGH → mcs 16/ valid	
Tpd39	4		mwtc/ mrdc/ LOW → mcs 16/ HIGH	
Tsu45	0		hwrdir → hdataen<1:0>/ LOW	(15)
Th46	0		hwrdir (HOLD) → hdataen<1:0>/ HIGH	(15)
Tpd47	2*gclk+40		mwtc/ iowc/ LOW → hdataen<1:0>/ LOW	(15) (13) (2)
		30	mwtc/ LOW → hdataen<0>/ LOW	(15) (8)
		118	mrdc/ iorc/ LOW → hdataen<1:0>/ LOW	(15) (5) (7)
		50	mwtc/ mrdc/ iorc/ iowc/ LOW → hdataen<1:0>/ LOW	(15) (17) (14)
Tpd48		17	mwtc/ mrdc/ iorc/ iowc/ HIGH→ hdataen<1:0>/ HIGH	(15)
Tpd49	0	35	mwtc/ mrdc/ iorc/ iowc/ LOW → hadren/ HIGH	(15)
Tpd50		34	mwtc/ mrdc/ iorc/ iowc/ HIGH → hadren/ LOW	(15)
Tdel51	3		hadren/ HIGH → hdataen<1>/ LOW	(15)
Tdel52	1		hdataen<1>/ HIGH → hadren/ LOW	(15)
Tdel53	0		ad<15:8> (OUTPUT DATA) TRISTATE → hadren/ LOW	(15)
Tdel54	3		hadren/ HIGH → ad<15:8> (OUTPUT DATA) ACTIVE	(15)
Th55	0		ad<15:0> valid (DATA) (HOLD) → hdataen<1:0>/ HIGH	(15)
Th57	0		ad<15:8> valid (ADDR) (HOLD) → hadren/ HIGH	(15) (1)
Tsu58	2*gclk+70		tc → iowc/ HIGH	(2)
Th58	-41		tc (HOLD) → iowc/ HIGH	(2)
Tsu59	100		dak/ → iowc/ LOW	(2)
Th60	45		dak/ (HOLD) → iowc/ HIGH	(2)
Tpd61	2	50	iowc/ LOW → drq LOW	(2)
Tpd62		33	tc → drq LOW	(2)
Tdel63	10		drq LOW → drq TRISTATE	(2)
Tdel64	14*gclk		irq LOW → irq HIGH	(3) (11) (19)
Tpd65		3*gclk+35	mwtc/ HIGH → isa	(3) (19)
Ta66	1 µs		reset ACTIVE	(3) (12) (19)

Table A-11: Host Interface Parameter List

Notes:

(1) ISA timing
(2) DMA timing
(3) The timing appears only as a note, and isn't shown in the diagram.
(4) Necessary only for cycles in which there is no BALE.
(5) VGA I/O read.
(6) VGA I/O write.
(7) VGA frame buffer read.
(8) VGA frame buffer write.
(9) After a CONFIG or OPMODE register write.
(10) Narrow decode only.
(11) Edge-triggered interrupt mode.
(12) The timing is also a function of the pull-up or pull-down, and the load.
(13) Write cycle.
(14) Read cycle.
(15) Must be considered only when hadren/ and hdataen/ are used.

(16) Can be ignored if **hadren/** and **hdataen/** are used, since an equivalent timing is guaranteed (as long as external buffers respect the constraints mentioned in Section 6.2.1.4).

(17) Write cycles without wait states.

(18) Choose the greater of the two values listed.

(19) These timings are not shown in the corresponding waveform.

Timing Conditions

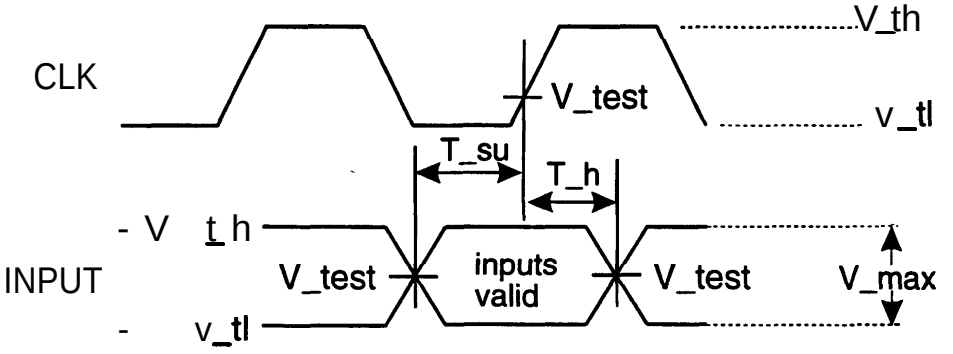


Figure A-2: Host PCI Input Waveform

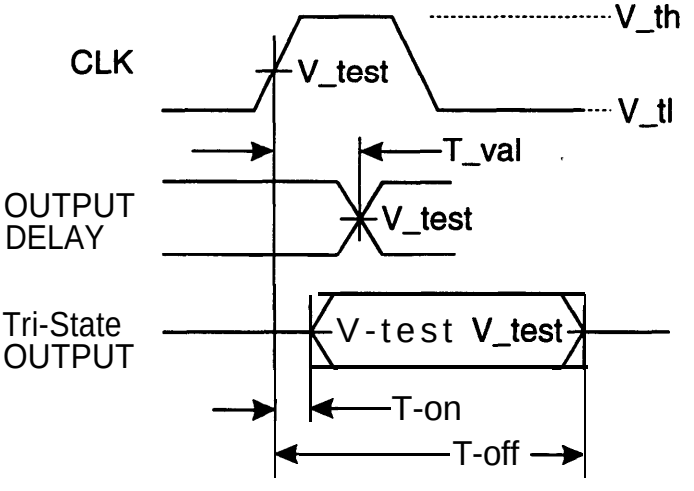


Figure A-3: Host PCI Output Waveform

Figures A-2 and A-3 define the conditions under which timing measurements are made. The component test guarantees that all timings are met with minimum clock slew rate (slowest edge) and voltage swing. The design guarantees that minimum timings are also met with maximum clock slew rate (fastest edge) and voltage swing. The design also guarantees proper input operation for input voltage swings and slew rates that exceed the specified timing conditions.

Symbol	*5 V Signalling*	*units*
V_{th}	2.4	V
V_{tl}	0.4	V
V_{test}	1.5	V
V_{max}	2 . 0	V
Input signal edge rate	1 V / ns	

V_{max} specifies the maximum peak-to-peak waveform allowed for testing input timing.

Symbol	*Parameter*	*Min*	*Max*	*Units*	*Notes*
t_{val}	CLK to Signal valid delay (bussed signals)	2	11	ns	(3) (2)
t_{on}	Float to Active delay	2		ns	(3)
t_{off}	Active to Float delay		28	ns	(3)
t_{su}	Input Setup time to CLK (bussed signals)	7		ns	(1)
t_h	Input Hold time from CLK	0		ns	(1)

Table A-12: Host PCI 5 V Timing Parameters

(1) Refer to Figure A-2.
(2) Minimum times measured with 0 **pF** equivalent load. Maximum times measured with 50 **pF** equivalent load. Actual test capacitance may vary. Correlate results to these specifications.
(3) Refer to Figure A-3.

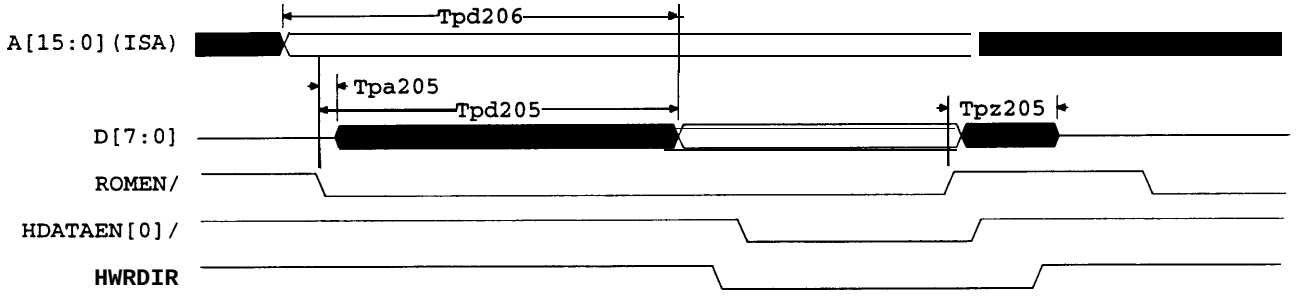


Figure A-4: ROM Host Interface Waveform

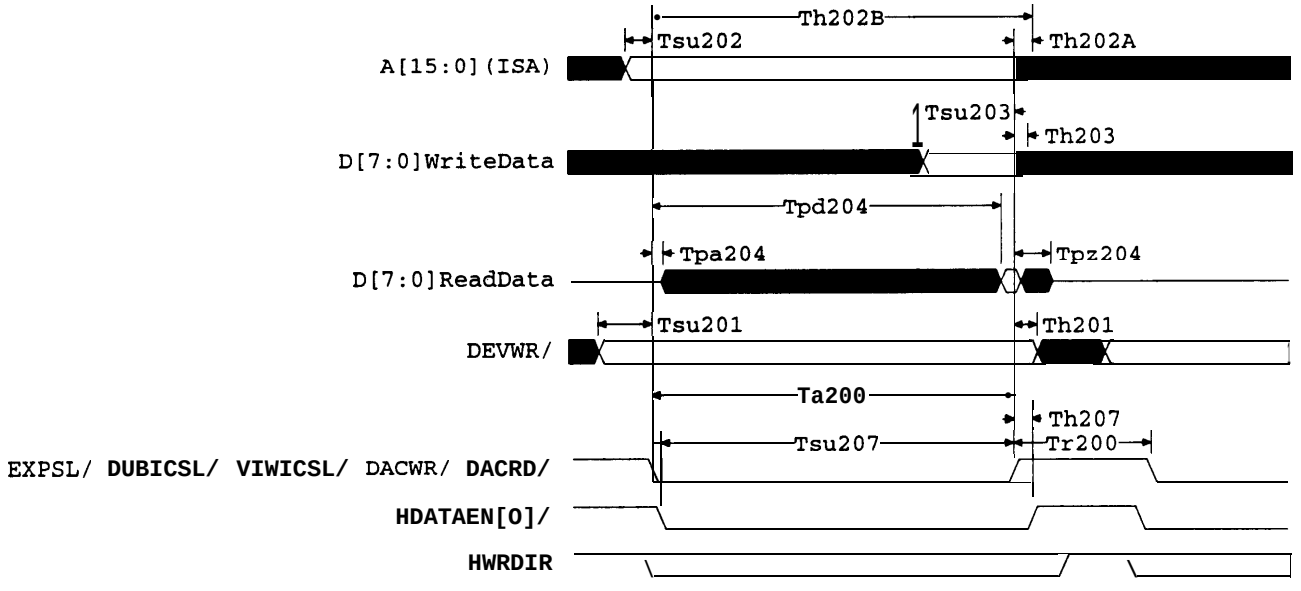


Figure A-5: External Device Interface Waveform (ISA)

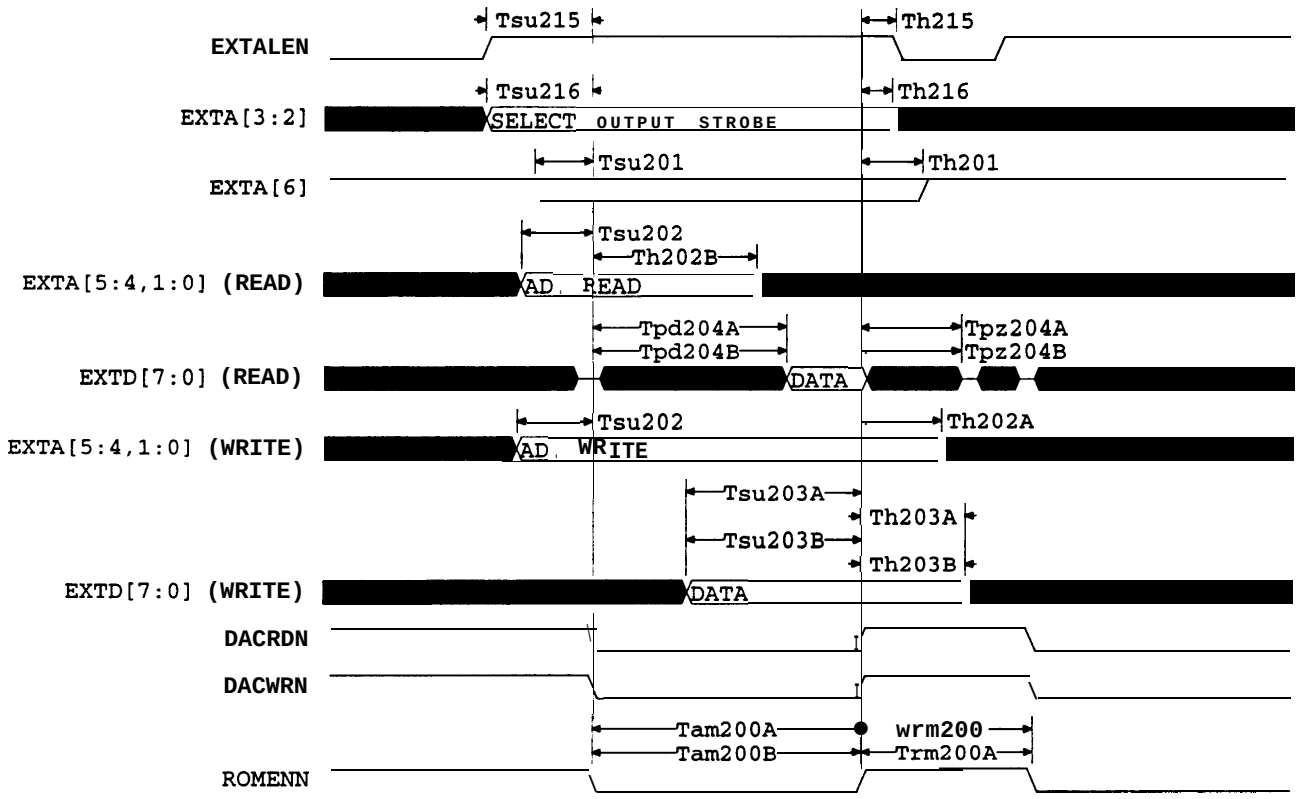


Figure A-6: External Device Interface Waveform (PCI)

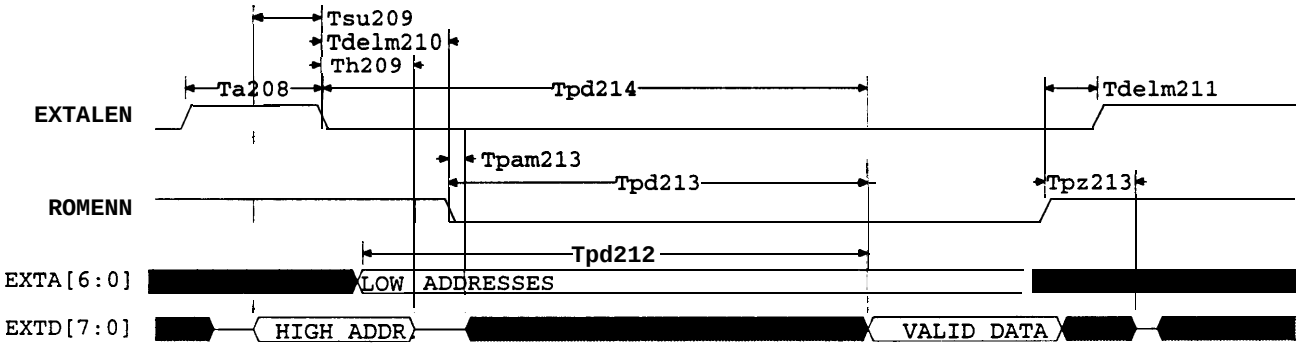


Figure A-7: BIOS ROM (PCI Configuration)

Ref.	Min (ns)	Max (ns)	Comments	Notes
Ta200	320		expsl/ ACTIVE (ISA) romenN (for expslN) (ACTIVE pulse) (PCI)	
	140		dacrd/ dacwr/ viwicsl/ dubicsl/ ACTIVE (ISA) dacrdN, dacwrN, romenN (for viwicslN, dubicslN) (ACTIVE pulse) (PCI)	
Tr200	60		expsl/ dacrd/ dacwr/ viwicsl/ dubicsl/ RECOVERY (ISA) dacrdN, dacwrN, romenN (RECOVERY pulse) (PCI)	
Tsu20 1	10		devwr/ → expsl/ viwicsl/ dubicsl/ LOW (ISA) exta<6> (devwrN) → romenN (LOW) (PCI)	
Th201	10		devwr/ (HOLD) → expsl/ viwicsl/ dubicsl/ HIGH (ISA) exta<6> (devwrN) (HOLD) → romenN (HIGH) (PCI)	
Tsu202	10		ad<15:0> (ADDR) → expsl/ viwicsl/ dubicsl/ dacrd/ dacwr/ LOW (ISA) exta<5:4,1:0> → dacrdN, dacwrN, romenN (LOW) (wr/rd) (PCI)	
Th202A	15		ad<15:0> (ADDR) (HOLD) → expsl/ viwicsl/ dubicsl/ dacwr/ HIGH (ISA) exta<5:4,1:0> (HOLD) → dacwrN, romenN (HIGH) (WRITE) (PCI)	(1)
Th202B	150		ad<15:0> (ADDR) (HOLD) → expsl/ viwicsl/ dubicsl/ dacrd/ LOW (ISA) exta<5:4,1:0> (HOLD) → dacrdN, romenN (LOW) (read) (PCI)	(2)
Tsu203	100		ad<7:0> (OUTPUT DATA) → expsl/ HIGH (ISA) exdt<7:0> → romenN (for expslN) (HIGH) (write) (PCI)	
	50		ad<7:0> (OUTPUT DATA) → viwicsl/ dubicsl/ dacwr/ HIGH (ISA) exdt<7:0> → dacwrN, romenN (for viwicslN, dubicslN) (HIGH) (write) (PCI)	
Th203	15		ad<7:0> (OUTPUT DATA) (HOLD) → expsl/ viwicsl/ dubicsl/ dacwr/ HIGH (ISA) extd<7:0> (HOLD) → dacwrN, romenN (HIGH) (write) (PCI)	
Tpa204	2		expsl/ viwicsl/ dubicsl/ dacrd/ LOW → ad<7:0> (INPUT DATA) ACTIVE	
Tpd204	2	300	expsl/ LOW → ad<7:0> (INPUT DATA) (ISA) romenN (for expslN) (LOW) → extd<7:0> (VALID) (read) (PCI)	
	2	90	viwicsl/ dubicsl/ dacrd/ LOW → ad<7:0> (INPUT DATA) (ISA) dacrdN, romenN (for viwicslN, dubicslN) (LOW) → extd<7:0> (VALID) (read) (PCI)	
Tpz204	2	40	expsl/ HIGH → ad<7:0> (INPUT DATA) TRISTATE (ISA) romenN (for expslN) (HIGH) → extd<7:0> (TRISTATE) (read) (PCI)	
	2	25	viwicsl/ dubicsl/ dacrd/ HIGH → ad<7:0> (INPUT DATA) TRISTATE (ISA) dacrdN, romenN (for viwicslN, dubislN) (HIGH) → extd<7:0> (TRISTATE) (read) (PCI)	
Tpd205		10*gclk-50 200	romen/ LOW → ad<7:0> (DATA)	(3)
Tpa205	2		romen/ LOW → ad<7:0> (DATA) ACTIVE	
Tpz205	2	60	romen/ HIGH → ad<7:0> (DATA) TRISTATE	
Tpd206	0	200 1 0*gcl k-50	ad<15:0> (OUTPUT ADDR) → ad<7:0> (DATA)	(3)
Tsu207	115		hdataen/ LOW → expsl/ HIGH	
	65		hdataen/ LOW → viwicsl/ dubicsl/ dacwr/ HIGH	
Th207	15		hdataen/ LOW (HOLD) → viwicsl/ dubicsl/ dacwr/ expsl/ HIGH	
Ta208	6		extalen(HIGH) ACTIVE	

Ref.	*Min (ns)*	*Max (ns)*	*Comments*	*Notes*
Tsu209	2		extd<7:0> → extalen (LOW)	
Th209	3		extd<7:0> (HOLD) → extalen (LOW)	
Tdelm2 10	6.30		extalen (LOW) → romenN (LOW)	
Tdelm2 11	4.80		romenN (HIGH) → extalen (HIGH)	
Tpd212	0	200	exta<6:0> → extd<7:0> (DATA)	
Tpd213	0	75	romenN (LOW) → extd<7:0> (DATA)	
Tpam213	0		romenN (LOW) → extd<7:0> (ACTIVE)	
Tpz213	0	60	romenN (LOW) → extd<7:0> (TRISTATE)	
Tpd214	0	200	extalen (LOW) → extd<7:0> (DATA)	
Tsu215	6.80		extalen (HIGH) → romenN (LOW) when NOT BIOSROM	
Th215	5.30		extalen (HIGH HOLD) → romenN (HIGH) when NOT BIOSROM	
Tsu216	6.80		exta<3:2> → romenN (LOW) when NOT BIOSROM	
Th216	5.30		exta<3:2> (HOLD) → romenN (HIGH) when NOT BIOSROM	

Table A-13: External Device Parameter List

Notes:

(1) Write cycle.
(2) Read cycle.
(3) Choose the lesser of the two values listed.

A.2.3.3 Power Graphic Mode VRAM Interface Timing

The MGA Power Graphic Mode VRAM interface timing diagrams and parameter lists are found on the pages which follow. This timing data is based on 80 ns VRAMs, with the MCTLWTST register programmed to C4001010h.

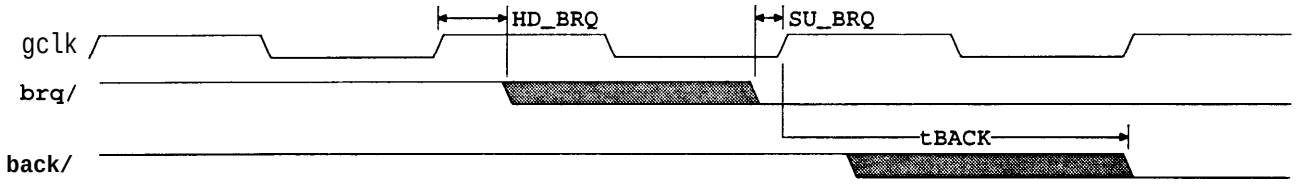


Figure A-8: BRQ Back Timing

Name	*Min. (ns)*	*Max.*
tBRQ	5	23
tBACK	5	25
SU_BRQ	0	
HD_BRQ	4	

Table A-14: BRQ Back Timing Parameter List

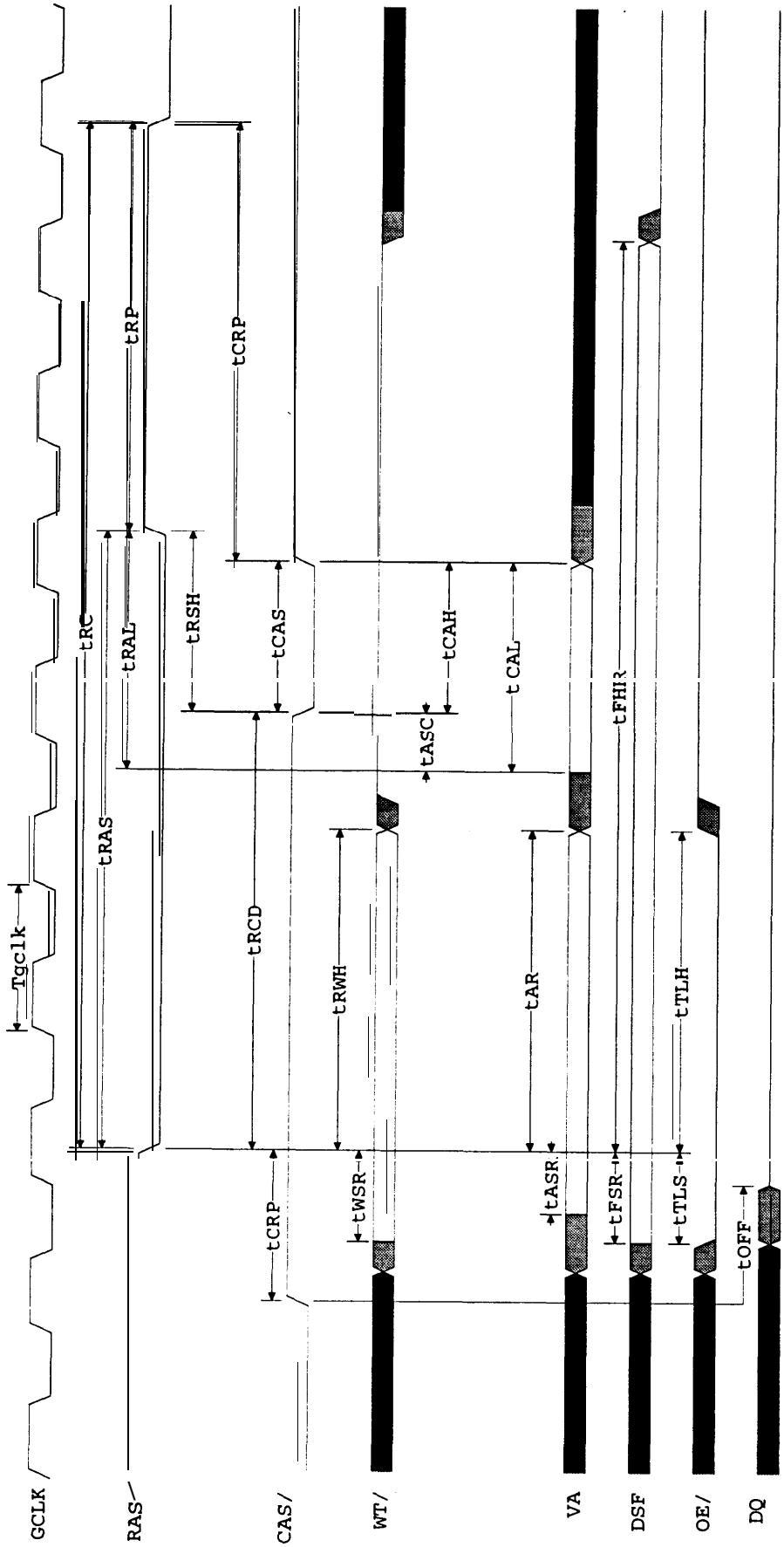


Figure A-9: Data Transfer Cycle Waveform

Name	*Min. (ns)*	*Max.*	*Comments*
Tgclk	20		GCLK period
tAR	50		Column address hold time after RAS/ low
tASC	10		Address setup time before CAS/ low
tASR	15		Address setup time before RAS/ low
tCAH	13		Address hold time after CAS/ low
tCAL	28		Column address to CAS/ high
tCAS	19		CAS/ pulse width
tCRP	19		CAS/ high before RAS/ low precharge time
tFHR	134		DSF hold time after RAS/ low (CAS/ one - block write)
tFSR	19		DSF setup time before RAS/ low
tOFF	0	120	Output buffer turn-off delay from CAS/
tRAL	40		Column address to RAS/ high
tRAS	94		RAS/ pulse width
tRC	156		Random read cycle time
tRCD	72		RAS/ low to CAS/ low delay time
tRP	55		RAS/ precharge time
tRSH	21		RAS/ hold time after CAS/
tRWH	49		Write hold after RAS/ low
tTLH	51		DT/ hold time after RAS/ low
tTLS	18		DT/ setup time before RAS/ low
tWSR	22		Write set up to RAS/ low

Table A-15: Data Transfer Cycle Parameter List

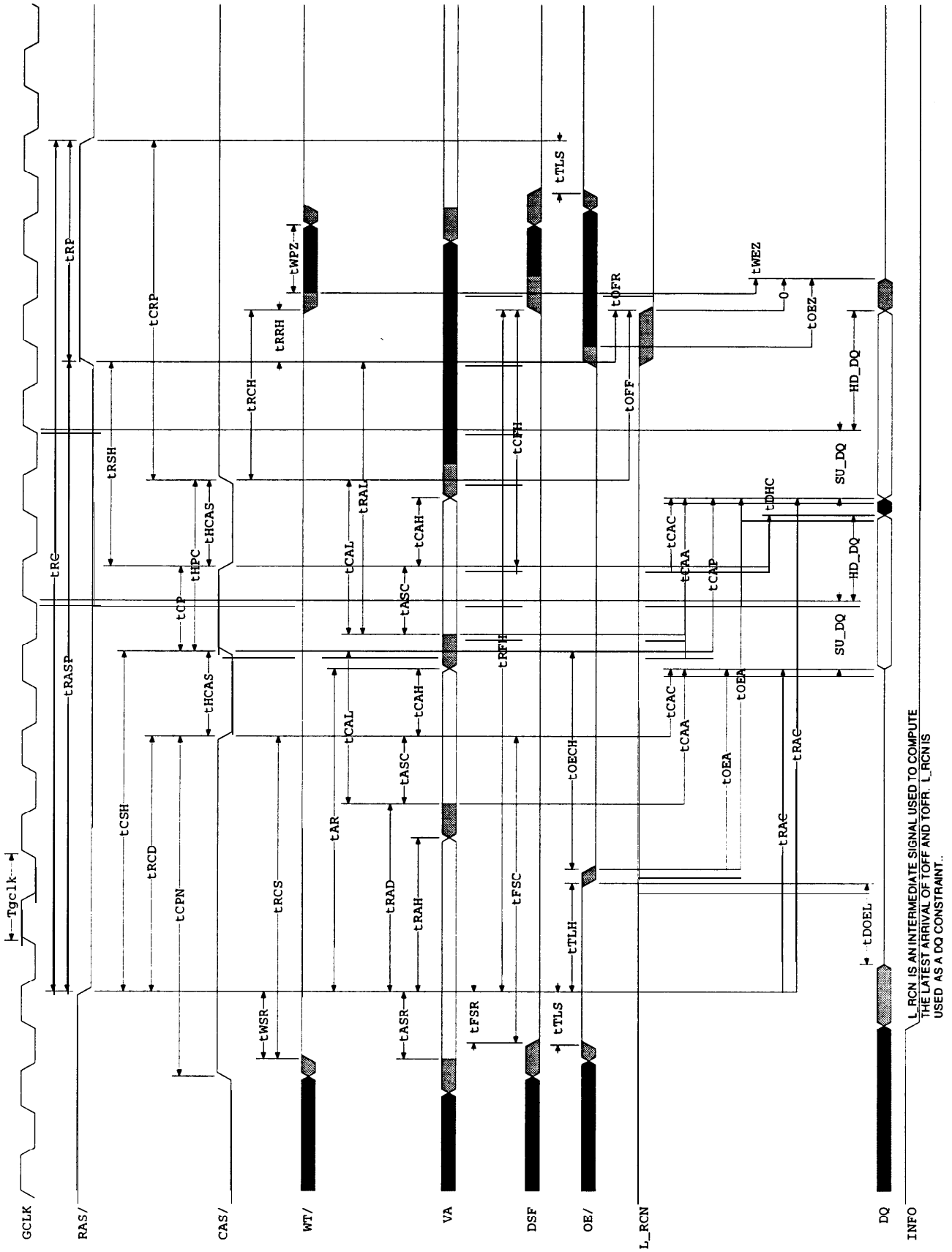


Figure A-10: Hyper Page Read Cycle Waveform

Name	*Min. (ns)*	*Max.*	*Comments*
Tgclk	20		GCLK period
HD_DQ	2		DQ hold after GCLK
SU_DQ	4		DQ setup time before GCLK
tAR	90		Column address hold time after RAS/ low
tASC	10		Address setup time before CAS/ low
tASR	15		Address setup time before RAS/ low
tCAA	0	31	Access time from column address
tCAC	0	16	Access time from CAS/
tCAH	13		Address hold time after CAS/ low
tCAL	28		Column address to CAS/ high
tCAP	0	35	Access time from CAS/ precharge
tCFH	56		DSF hold time after CAS/ low
tCP	14		CAS/ precharge time (fast page mode)
tCPN	94		CAS/ precharge time (not fast page mode)
tCRP	79		CAS/ high before RAS/ low precharge time
tCSH	90		CAS/ hold time after RAS/
tDHC	0	16	Data hold time (to CAS/)
tDOEL	18		Delay time data to OE/ low
tFSC	94		DSF setup time before CAS/ low
tFSR	19		DSF setup time before RAS/ low
tHCAS	19		Hyper Page mode CAS/ pulse width
tHPC	40		Hyper Page mode cycle time
tOEA	0	75	Access time from OE/
tOECH	72		CAS/ hold from OE/ low
tOEZ	0	20	Output buffer turn-off delay from OE/
tOFF	0	39	Output buffer turn-off delay from CAS/
tOFR	0	17	Output disable time from RAS/ high (Hyper Page mode)
tRAC	0	93	Access time from RAS/
tRAD	62		RAS/ low to column address delay time
tRAH	50		Address hold time after RAS/ low
tRAL	53		Column address to RAS/ high
tRASP	154		RAS/ pulse width (fast page mode)
tRC	216		Random read cycle time
tRCD	72		RAS/ low to CAS/ low delay time
tRCH	32		Read command hold time after CAS/ high
tRCS	93		Read command Setup time before CAS/ low
tRFH	174		DSF hold time after RAS/ low
tRP	60		RAS/ precharge time
tRRH	10		Read command hold time referenced to RAS/
tRSH	37		RAS/ hold time after CAS/
tTLH	13		DT/ hold time after RAS/ low
tTLS	20		DT/ Setup Time before RAS/ low
tWEZ	0	2	Output disable time from WT/ low (Hyper Page mode)
tWPZ	15		Write command pulse width (to turn 00-7 Z)
tWSR	18		Write set up to RAS/ low

Table A-16: Hyper Page Read Cycle Parameter List

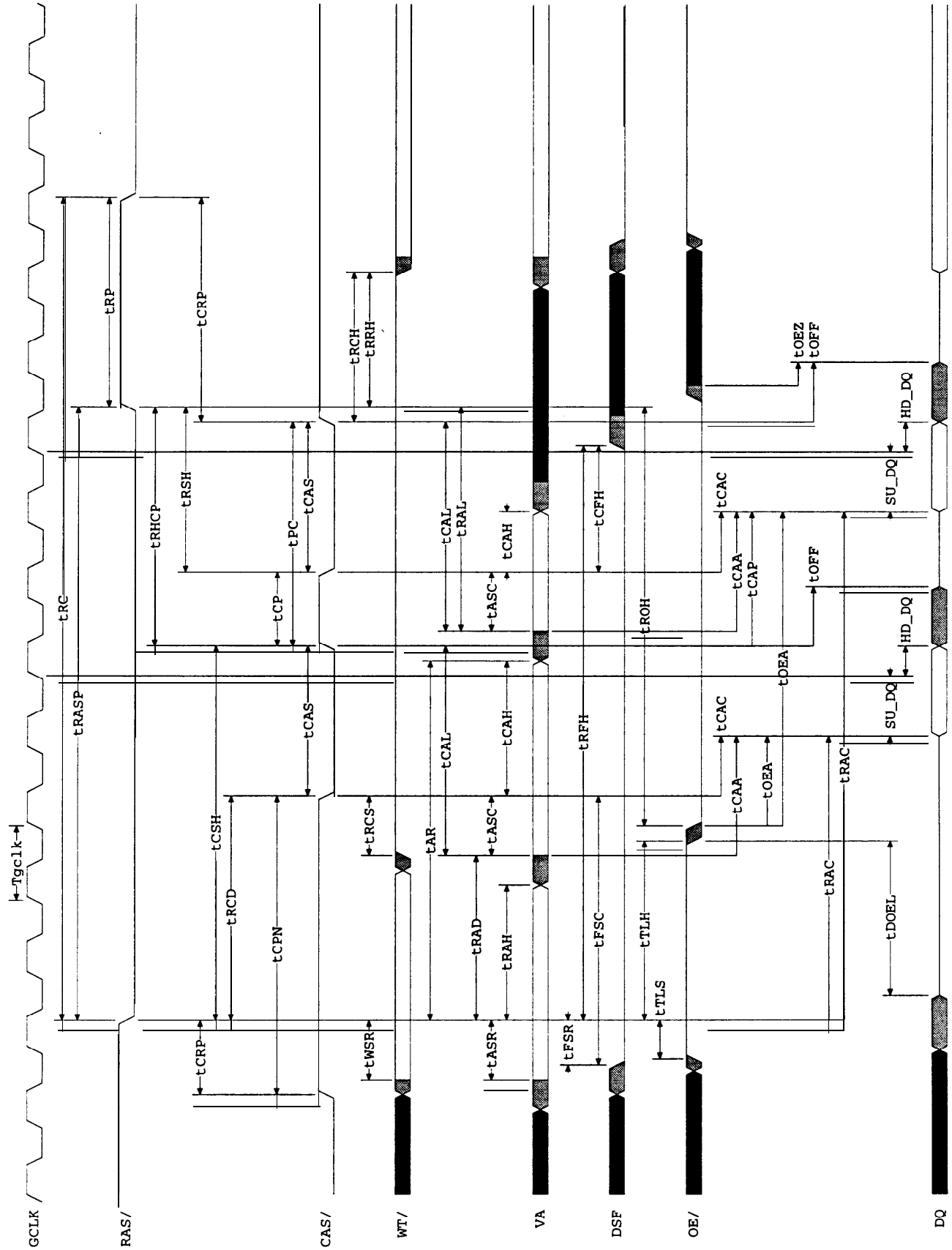


Figure A-11: Page Read Cycle waveform

Name	*Min (ns)*	*Max*	*Comments*
Tgclk	20		GCLK period
HD_DQ	2		DQ hold after GCLK
SU_DQ	4		DQ setup time before GCLK
tAR	110		Column address hold time after RAS/ low
tASC	10		Address setup time before CAS/ low
tASR	15		Address setup time before RAS/ low
tCAA	0	31	Access time from column address
tCAC	0	16	Access time from CAS/
tCAH	13		Address hold time after CAS/ low
tCAL	48		Column address to CAS/ high
tCAP	0	35	Access time from CAS/ precharge
tCAS	33		CAS/ pulse width
tCFH	36		DSF hold time after CAS/ low
tCP	14		CAS/ precharge time (fast page mode)
tCPN	94		CAS/ precharge time (not fast page mode)
tCRP	59		CAS/ high before RAS/ low precharge time
tCSH	110		CAS/ hold time after RAS/
tDOEL	41		Delay time data to OE/ low
tFHR	174		DSF hold time after RAS/ low (CAS/ one - Block Write)
tFSC	94		DSF setup time before CAS/ low
tFSR	19		DSF setup time before RAS/ low
tOEA	0	35	Access time from OE/
tOEZ	0	21	Output buffer turn-off delay from OE/
tOFF	0	14	Output buffer turn-off delay from CAS/
tPC	60		Fast page mode cycle time
tRAC	0	93	Access time from RAS/
tRAD	62		RAS/ low to column address delay time
tRAH	50		Address hold time after RAS/ low
tRAL	53		Column address to RAS/ high
tRASP	174		RAS/ pulse width (fast page mode)
tRC	236		Random read cycle time
tRCD	72		RAS/ low to CAS/ low delay time
tRCH	32		Read command hold time after CAS/ high
tRCS	13		Read command setup time before CAS/ low
tRFH	174		DSF hold time after RAS/ low
tRHCP	57		RAS/ hold time from CAS/ precharge (Fast Page Mode)
tROH	116		RAS/ hold time referenced to OE/
tRP	60		RAS/ precharge time
tRRH	30		Read command hold time referenced to RAS/
tRSH	37		RAS/ hold time after CAS/
tTLH	53		DT/ hold time after RAS/ low
tTLS	20		DT/ setup time before RAS/ low
tWSR	16		Write set up to RAS/ low

Table A-17: Page Read Cycle Parameter List

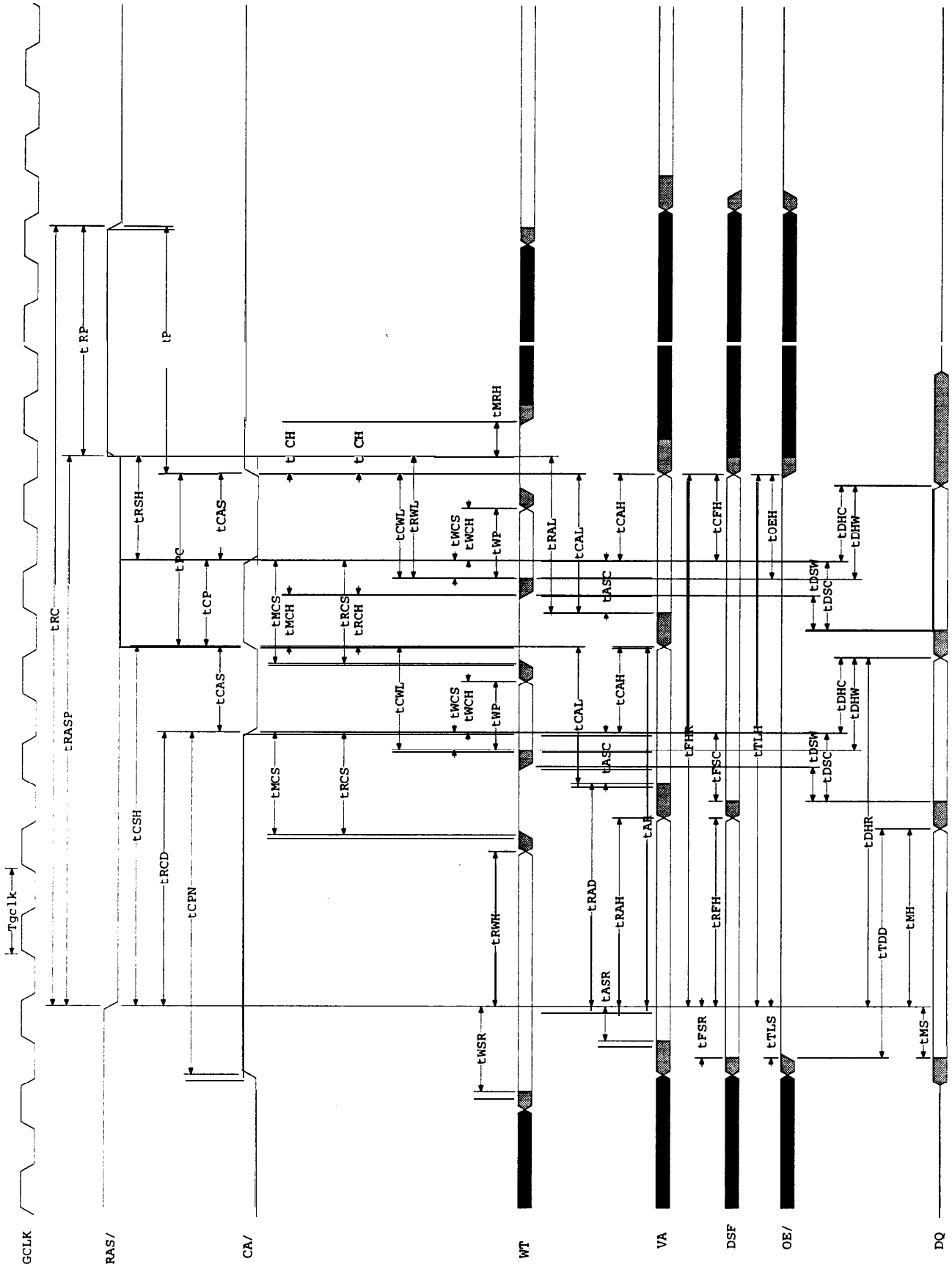


Figure A-12: Page Write Cycle Waveform

Name	*Min (ns)*	*Comments*
Tgclk	20	GCLK period
tAR	90	Column address hold time after RAS/ low
tASC	10	Address setup time before CAS/ low
tASR	15	Address setup time before RAS/ low
tCAH	13	Address hold time after CAS/ low
tCAL	28	Column address to CAS/ high
tCAS	19	CAS/ pulse width
tCFH	16	DSF hold time after CAS/ low
tCP	14	CAS/ precharge time (fast page mode)
tCPN	94	CAS/ precharge time (not fast page mode)
tCRP	59	CAS/ high before RAS/ low precharge time
tCSH	90	CAS/ hold time after RAS/
tCWL	17	Write command to CAS/ lead time
tDHC	15	Data hold time (to CAS/)
tDHR	89	Data hold time after RAS/ low
tDHW	15	Data hold time (to WT/)
tDSC	4	Data setup to CAS/
tDSW	2	Data setup to WT/
tFHR	134	DSF hold time after RAS/ low (CAS/ one - Block Write)
tFSC	15	DSF setup time before CAS/ low
tFSR	19	DSF setup time before RAS/ low
tMCH	10	Masked write hold time referenced to CAS/
tMCS	13	Masked write setup time
tMH	49	Write mask hold time after RAS/ low
tMRH	10	Masked write hold time referenced to RAS/
tMS	4	Write mask setup time before RAS/ low
tOEH	20	OE/ high hold time after WT/ low (OE/ controlled write)
tPC	40	Fast page mode cycle time
tRAD	62	RAS/ low to column address delay time
tRAH	50	Address hold time after RAS/ low
tRAL	38	Column address to RAS/ high
tRASP	134	RAS/ pulse width (fast page mode)
tRC	196	Random read cycle time
tRCD	72	RAS/ low to CAS/ low delay time
tRCH	12	Read command hold time after CAS/ high
tRCS	13	Read command setup time before CAS/ low
tRFH	54	DSF hold time after RAS/ low
tRP	60	RAS/ precharge time
tRSH	20	RAS/ hold time after CASI
tRWH	49	Write hold after RAS/ low
tRWL	20	Write command to RAS/ lead time
tTDD	72	OE/ high to data low impedance delay time
tTLH	133	DT/ hold time after RAS/ low
tTLS	20	DT/ setup time before RAS/ low
tWCH	15	Write command hold time after CAS/ low
tWCS	0	Write command setup time before CAS/ low
tWP	15	Write command pulse width
tWSR	22	Write set up to RAS/ low

Table A-18: Page Write Cycle Parameter List

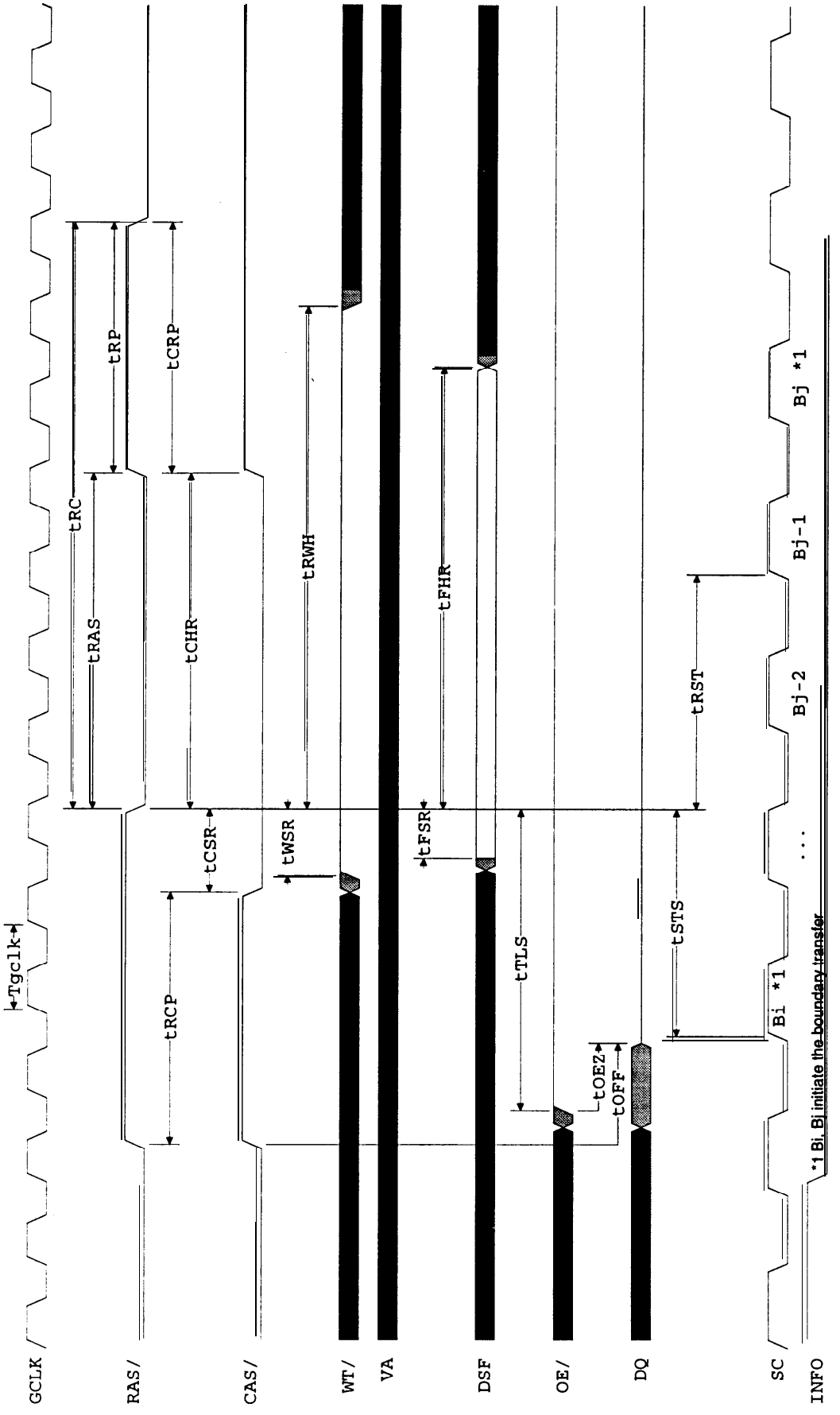


Figure A-13: Refresh Cycle Waveform

Name	*Min (ns)*	*Max*	*Comments*
Tgclk	20		GCLK period
tCHR	90		CAS/ low after RAS/ low hold time (C-R rfh)
tCRP	59		CAS/ high before RAS/ low precharge time
tCSR	19		CAS/ low to RAS/ low set up time (CAS/ before RAS/ refresh)
tFHR	114		DSF hold time after RAS/ low (CAS/ one - Block Write)
tFSR	19		DSF setup time before RAS/ low
tOEZ	0	160	Output buffer turn-off delay from OE/
tOFF	0	160	Output buffer turn-off delay from CAS/
tRAS	94		RAS/ pulse width
tRC	156		Random read cycle time
tRCP	52		RAS/ high to CAS/ low precharge (C-R rfh)
tRP	60		RAS/ precharge time
tRST	87		Split transfer hold time referenced to RAS/
tRWH	129		Write hold after RAS/ low
tSTS	47		QSF to RAS/ low delay time
tTLS	80		DT/ setup time before RAS/ low
tWSR	22		Write set up to RAS/ low

Table A-19: Refresh Cycle Parameter List

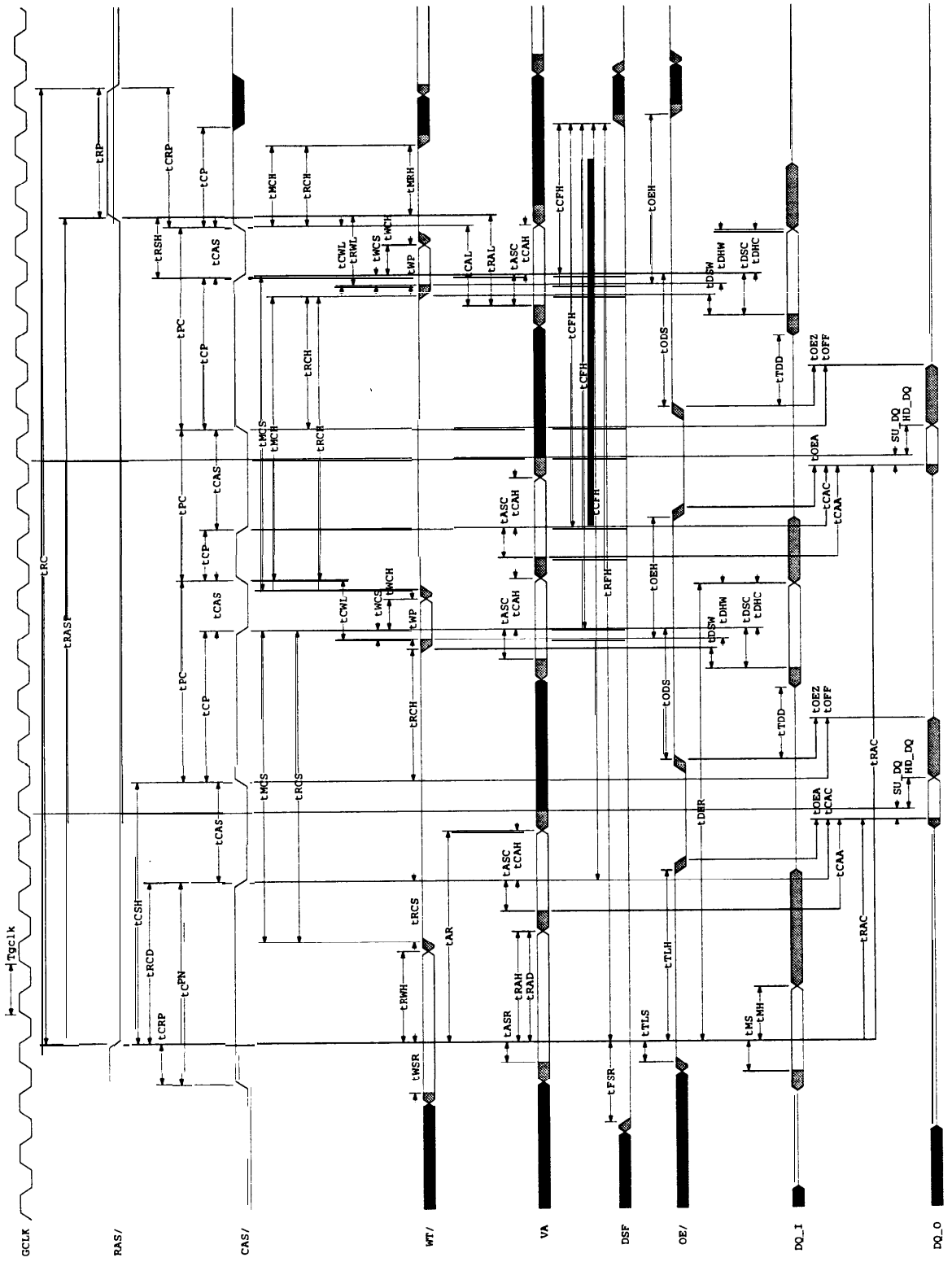


Figure A-14: Page Read-Modify-Write Cycle Waveform

Name	*Min (ns)*	*Max*	*Comments*
Tgclk	20		GCLK period
HD_DQ	2		DQ Hold after GCLK
SU_DQ	4		DQ Setup time before GCLK
tAR	90		Column Address Hold Time after RAS/ Low
tASC	10		Address Setup Time before CAS/ low

Name	*Min (ns)*	*Max*	*Comments*
tASR	15		Address setup time before RAS/ low
tCAA	0	31	Access time from column address
tCAC	0	16	Access time from CAS/
tCAH	13		Address hold time after CAS/ low
tCAL	28		Column Address to CAS/ high
tCAS	19		CAS/ pulse width
tCFH	56		DSF Hold Time after CAS/ low
tCP	14		CAS/ precharge time (fast page mode)
tCPN	94		CAS/ precharge time (not fast page mode)
tCRP	19		CAS/ high before RAS/ low precharge time
tCSH	110		CAS/ hold time after RAS/
tCWL	17		Write command to CAS/ lead time
tDHC	15		Data hold time (to CAS/)
tDHR	189		Data hold time after Ras/ Low
tDHW	15		Data hold time (to WT/)
tDSC	0		Data setup to CAS/
tDSW	0		Data setup to WT/
tFSR	39		DSF setup time before RAS/ low
tMCH	32		Masked write hold time referenced to CAS/
tMCS	113		Masked write setup time
tMH	10		Write mask hold time after RAS/ low
tMRH	30		Masked write hold time referenced to RAS/
tMS	4		Write mask setup time before RAS/ low
tODS	55		Output disable setup time
tOEA	0	15	Access time from OE/
tOEH	39		OE/ high hold time after WT/ low (OE/ contolled write)
tOEZ	0	20	Output buffertTurn-off delay from OE/
tOFF	0	19	Output buffer turn-off delay from CAS/
tPC	60		Fast page mode cycle time
tRAC	0	93	Access time from RAS/
tRAD	62		RAS/ low to column address delay time
tRAH	50		Address hold time after RAS/ low
tRAL	38		Column address to RAS/ high
tRASP	334		RAS/ pulse width (fast page mode)
tRC	396		Random read cycle time
tRCD	72		RAS/ low to CAS/ low delay time
tRCH	32		Read command hold time after CAS/ high
tRCS	13		Read command setup time before CAS/ low
tRFH	374		DSF hold time after RAS/ low
tRP	60		RAS/ precharge time
tRSH	20		RAS/ hold time after CAS/
tRWH	49		Write hold after RAS/ low
tRWL	20		Write command to RAS/ lead time
tTDD	20		OE/ high to data low impedance delay time
tTLH	73		DT/ hold time after RAS/ low
tTLS	20		DT/ setup time before RAS/ low
tWCH	15		Write command hold time after CAS/ low
tWCS	0		Write command setup time before CAS/ low
tWP	15		Write command pulse width
tWSR	18		Write set up to RAS/ low

Table A-20: Page Read-Modify-Write Cycle Parameter List

A.2.3.4 VGA Mode VRAM Interface Timing

Notes:

(1) In the tables which follow, t_s, t_h and t_l are the period of VIDCLK, VIDCLK high pulse width, and VIDCLK low pulse width, respectively.

(2)
A = Standard Modes (CPU Writes),
High-resolution 256-Color Modes (CPU Writes during Blank) (4)
B = High-Resolution 256-Color Modes (CPU Writes) (4)
C = Low Frequency Sequence (Display Reads),
High-resolution 256-Color Mode (CPU Reads during Blank) (4)
D = Low Frequency Sequence (Catch Up Display Reads)
E = Low Frequency Sequence (CPU Reads)
F = High Frequency Sequence (Display Reads)
G = High Frequency Sequence (Catch Up Display Reads)
H = High Frequency Sequence (CPU Reads)
I = High-resolution 256-Color Mode (CPU Reads during Video) (4)
J = High resolution 256-Color Mode (Display Reads) (4)

(3) The 'VRAM' column represents the timing that the VRAM must respect in order to support Super VGA modes.

(4) For 1024 x 768 x 16 NI at 65 MHz, the pixel clock is divided by two, so high-resolution 256-color mode cycles have twice the number of clocks.

(5) The WTN signals are high for at least one full cycle prior to the one indicated.

(6) The WTN signals are high for at least one full cycle after the one indicated.

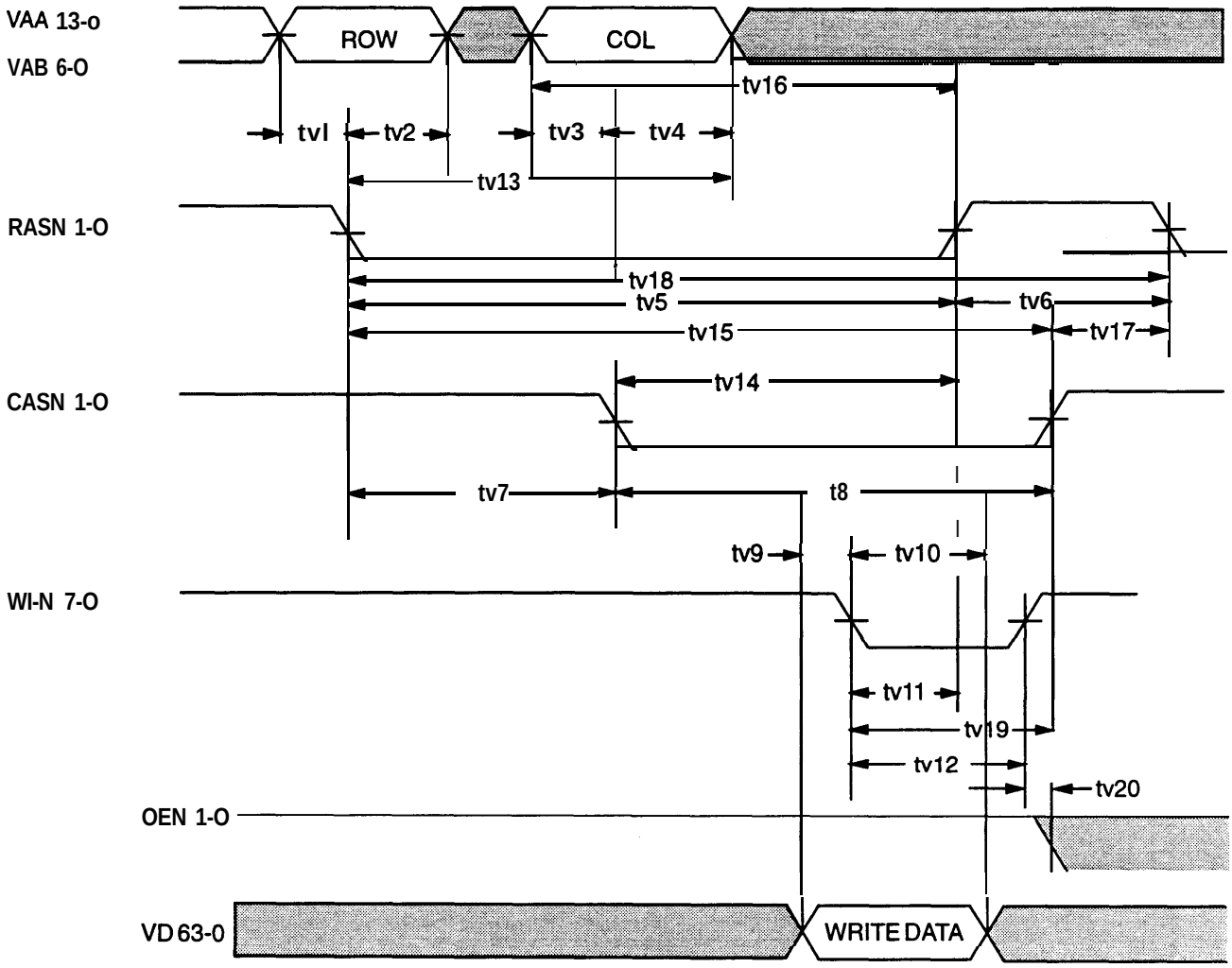


Figure A-15: Video Dynamic RAM Write Cycles

		Mode (1) (2)		VRAM (3)	
		A	B	Min	Max
tv1	Row address setup time to RASN low	$2t_s$	t_s+t_h	0	
tv2	Row address hold time from RASN low	t_s	tl	10	
tv3	Column address setup time to CASN low	t_h	th	0	
tv4	Column address hold time from CASN low	t_s	tl	15	
tv5	RASN low duration	$5t_s$	3ts	80	10000
tv6	RASN high duration	$3t_s$	t_l+2t_s	60	
tv7	RASN to CASN low delay	t_s+t_h	ts	20	
tv8	CASN low duration	$5t_s$	3ts	20	10000
tv9	Write data setup time to WTN low	t_l+4t_s	$4t_s+t_h$	0	
tv10	Write data hold time from WTN low	$3t_s+t_h$	$tl+5t_s$	20	
tv11	WTN to RASN high lead time	$2t_s$	ts	20	
tv12	WTN low duration	$4t_s$	2ts	20	
tv13	Column address hold, referenced to RASN	$2t_s+t_h$	$tl+t_s$	45	
tv14	RASN hold time	t_l+3t_s	2ts	20	
tv15	CASN hold time	$6t_s+t_h$	4ts	80	
tv16	Column address to RASN lead time	$4t_s$	$2ts+t_h$	40	
tv17	CASN to RASN precharge	t_l+t_s	t_l+t_s	10	
tv18	Random read/write cycle time	$8t_s$	$tl+5t_s$	150	
tv19	WTN to CASN lead time	$3t_s+t_h$	2ts	20	
tv20	OEN command hold time	$3t_s+t_h$	$tl+3t_s$	20	-

Table A-21: Video Dynamic RAM Write Cycles

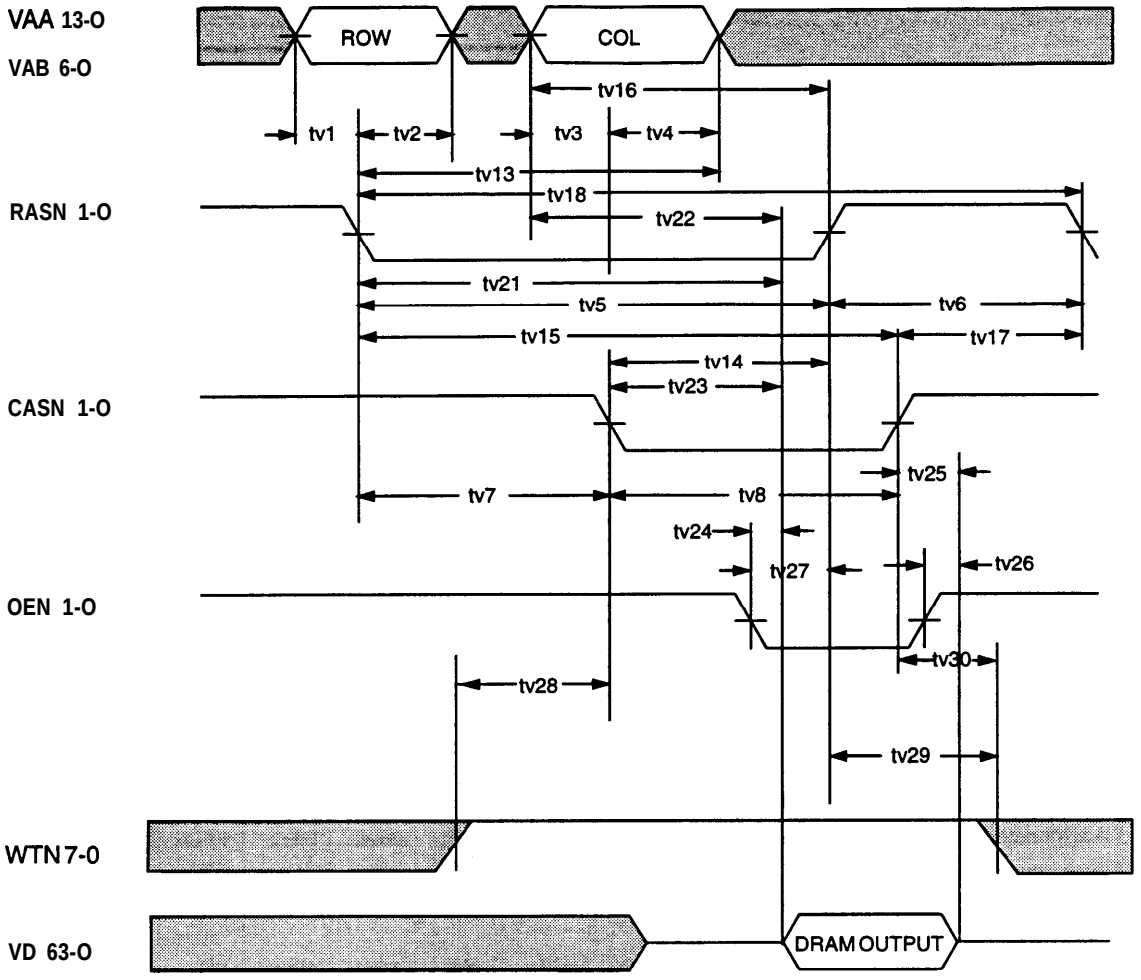


Figure A-16: Video Dynamic RAM Read Cycles

		Mode (1) (2)							VRAM (3)	
		C	D	E	F	G	H	I	Min	Max
tvl	Row address setup time to RASN low	$2t_s$	$2t_s$	2ts	ts	2ts	2ts	$ts+t_h$	0	
tv2	Row address hold time from RASN low	t_s	t_s	t_s	t_s	t_s	t_s	t_l	10	
tv3	CASN setup time to CASN low	t_h	t_h	t_h	t_h	t_h	t_h	t_h	0	
tv4	CASN hold time from CASN low	t_s	t_s	t_s	t_s	t_s	t_s	t_l	15	
tv5	RASN low duration	$3t_s$	$3t_s$	$5t_s$	$4t_s$	$4t_s$	$5t_s$	$3t_s$	80	loo00
tv6	RASN high duration	$5t_s$	$3t_s$	$3t_s$	$4t_s$	$3t_s$	$3t_s$	t_l+2t_s	60	
tv7	RASN to CASN low delay	t_s+t_h	t_s+t_h	t_s+t_h	t_s+t_h	t_s+t_h	t_s+t_h	t_s	20	
tv8	CASN low duration	$3t_s$	$3t_s$	$5t_s$	$4t_s$	$3t_s$	$5t_s$	$3t_s$	20	10000
tv13	Column address hold referenced to RASN	$2t_s+t_h$	$2t_s+t_h$	$2t_s+t_h$	$2t_s+t_h$	$2t_s+t_h$	$2t_s+t_h$	t_l+t_s	45	
tv14	RASN hold time	t_l+t_s	t_l+t_s	t_l+3t_s	t_l+2t_s	t_l+t_s	t_l+3t_s	$2t_s$	20	
tv15	CASN hold time	$4t_s+t_h$	$4t_s+t_h$	$6t_s+t_h$	$5t_s+t_h$	$5t_s+t_h$	$6t_s+t_h$	$4t_s$	80	
tv16	Column address to RASN lead time	$2t_s$	$2t_s$	$4t_s$	$3t_s$	$3t_s$	$4t_s$	$2t_s+t_h$	40	
tv17	CASN to RASN precharge	$3t_s+t_l$	$ts+t_l$	$tl+t_s$	$tl+2t_s$	$tl+t_s$	$tl+t_s$	$tl+t_s$	10	
tv18	Random read/write cycle time	$8t_s$	$6t_s$	$8t_s$	$8t_s$	$7t_s$	$8t_s$	t_l+5t_s	150	
tv21	Access time from RASN								80	
tv22	Access time from column address								40	
tv23	DRAM access time from CASN low									20
tv24	OEN to DRAM data output delay									20
tv25	Output buffer turn off time from CASN									20
tv26	Output buffer turn off time from OEN									20
tv27	RASN hold time referenced to OEN	t_l	t_l	t_l+2t_s	$tl+t_s$	$tl+t_s$	t_l+2t_s	t_s+t_h	20	
tv28	Row command setup	(5)	$2t_s+2t_h$	(5)	(5)	$3t_s+t_h$	(5)	(5)	0	
tv29	Read command hold time referenced to RASN	(6)	$6t_s$	(6)	$6t_s$	$6t_s$	(6)	(6)	10	
tv30	Read command hold time	(6)	t_l+4t_s	(6)	t_l+4t_s	$tl+4t_s$	(6)	(6)	0	

Table A-22: Video Dynamic RAM Read Cycles

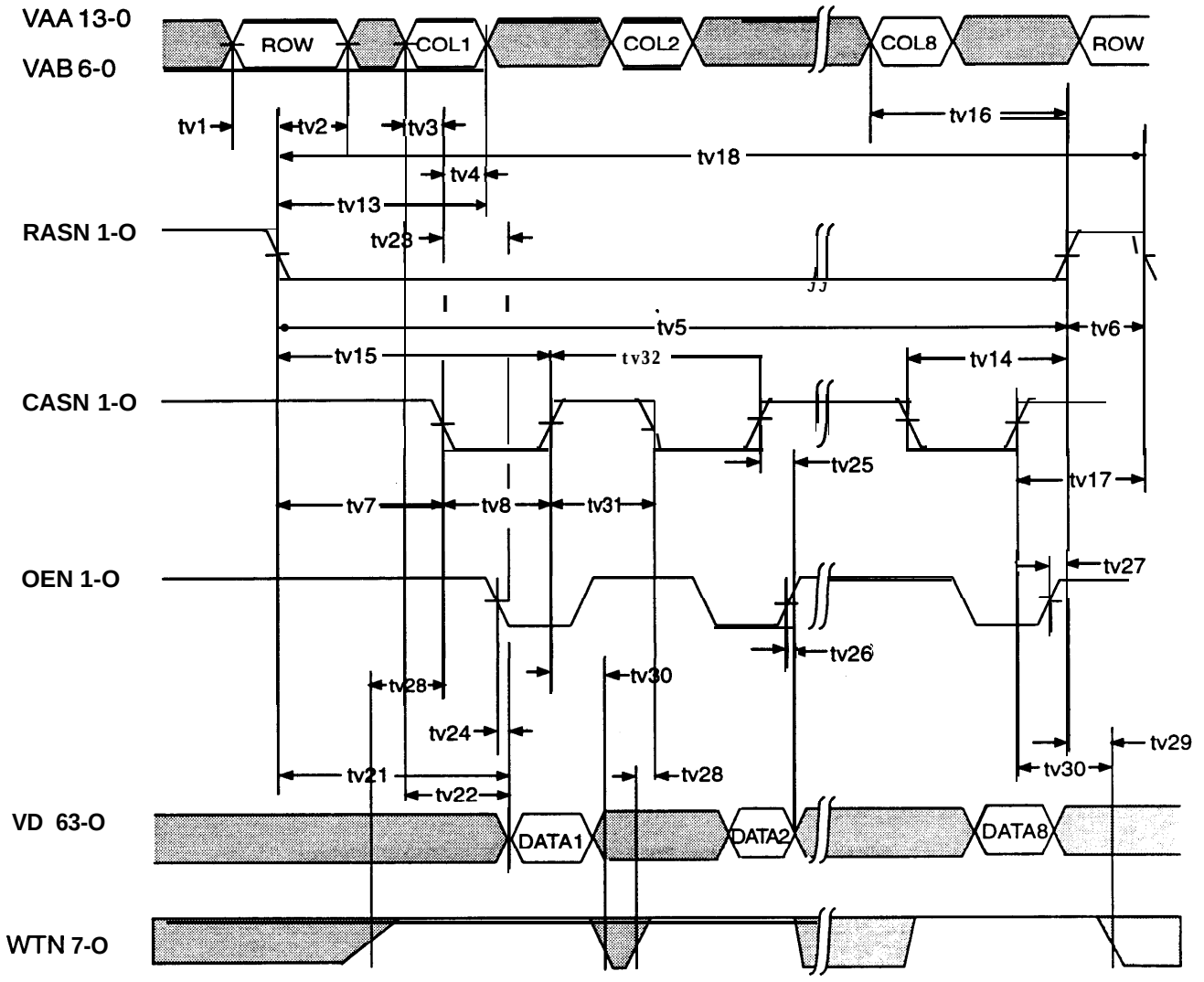


Figure A-17: Video Dynamic RAM Page Read Cycles

		Mode (1) (2)	VRAM (3)	
		J	Min	Max
tv1	Row address setup time to RASN low	$2t_s$	0	
tv2	Row address hold time from RASN low	t_h	10	
tv3	Column address setup time to CASN low	t_s	0	
tv4	Column address hold time from CASN low	t_l+t_s	15	
tv5	RASN low duration	$24t_s$	80	10000
tv6	RASN high duration	$2t_s+t_h$	60	
tv7	RASN to CASN low delay	t_s+t_h	20	
tv8	CASN low duration	t_l+t_s	20	10000
tv13	Column address hold referenced to RASN	$3t_s$	45	
tv14	RASN hold time	t_l+t_s	20	
tv15	CASN hold time	$3t_s$	80	
tv16	Column address to RASN lead time	$3t_s$	40	
tv17	CASN to RASN precharge	$2t_s+t_h$	10	
tv18	Random read/write cycle time	$26t_s+t_h$	150	
tv21	Access time from RASN		80	
tv22	Access time from column address		40	
tv23	DRAM access time from CASN low		20	
tv24	OEN to DRAM data output delay		20	
tv25	Output buffer turn off time from CASN			20
tv26	Output buffer turn off time from OEN			20
tv27	RASN hold time referenced to OEN	$0t_s$	20	
tv28	Row command setup	$3t_s$	0	
tv29	Read command hold time referenced to RASN	$4t_s+t_h$	10	
tv30	Read command hold time	$4t_s+t_h$	0	
tv31	CASN high duration	t_s+t_h	10	
tv32	Fast page mode cycle	$3t_s$	50	

Table A-23: Video Dynamic RAM Page Read Cycles

A.2.3.5 Video Interface Timing

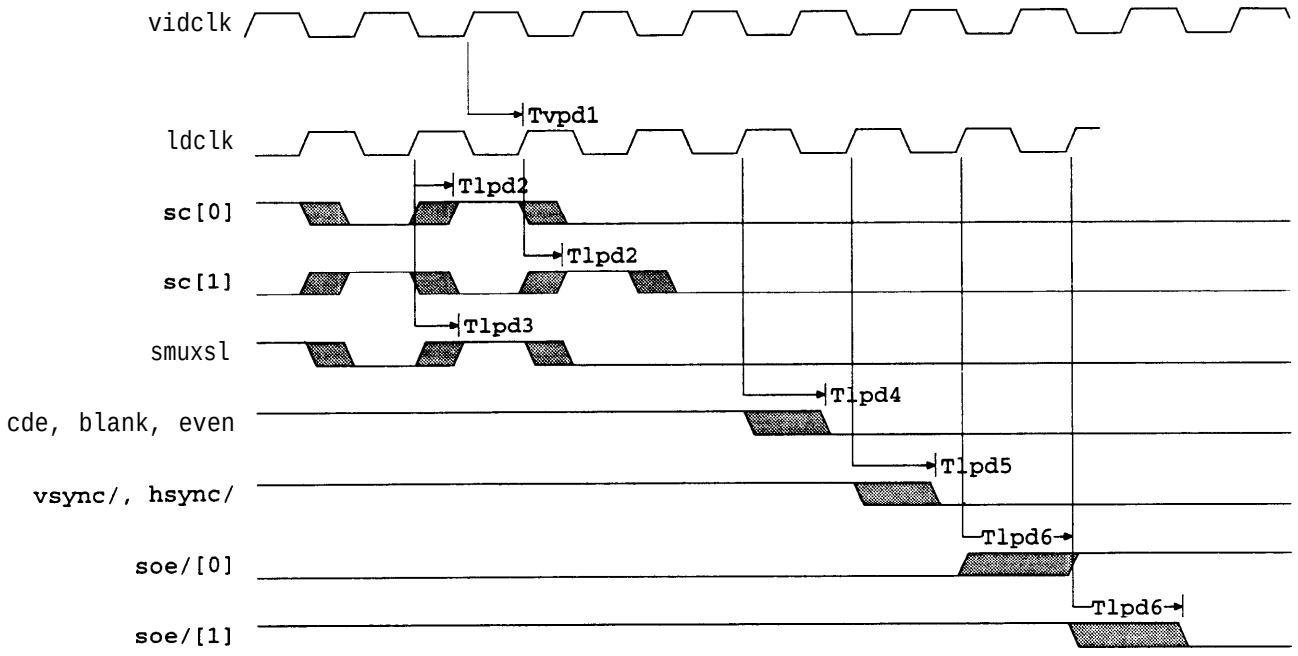


Figure A-18: Video Timing (No DUBIC Mode)

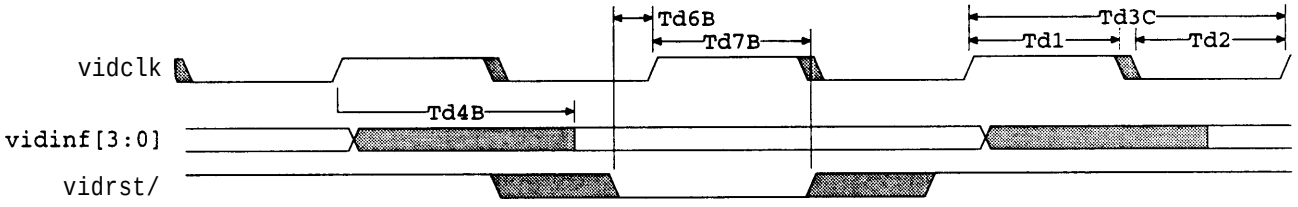


Figure A-19: Power Graphic Video Timing (DUBIC Mode)

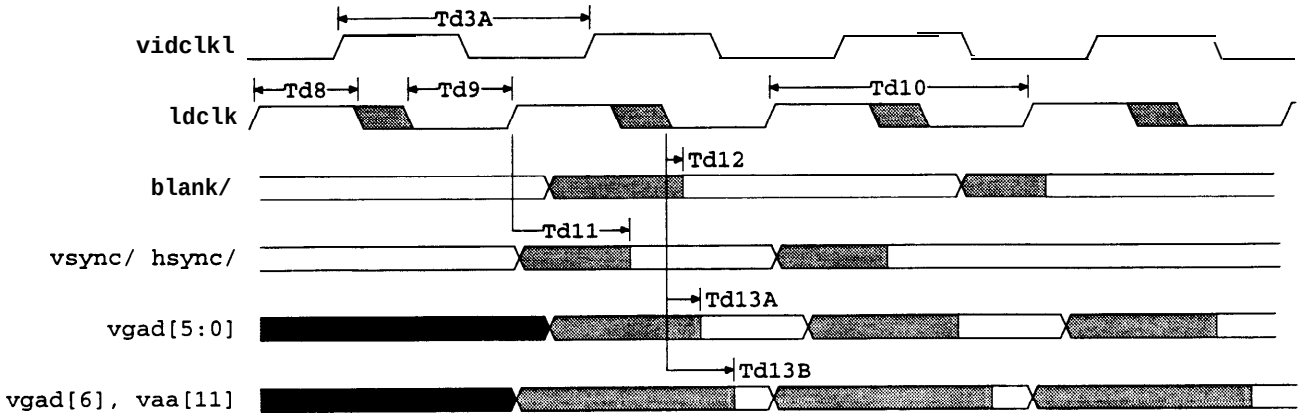


Figure A-20: VGA Mode (Normal) Video Timing

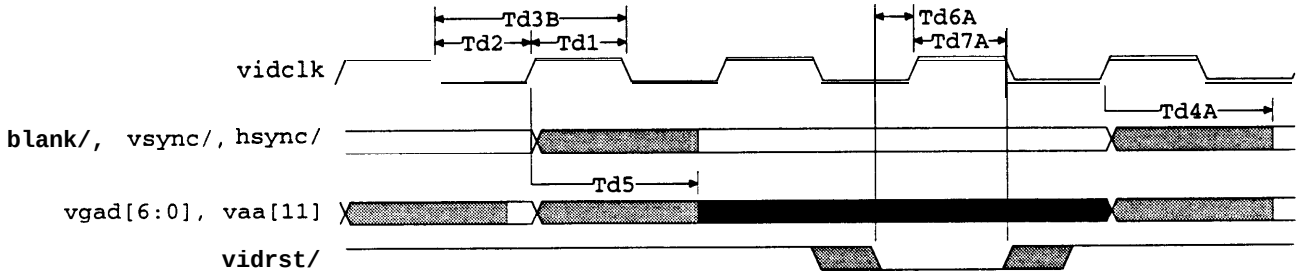


Figure A-21: VGA Mode (Slave) Video Timing

❖ Note: In Figures A-20 and A-21, the signal names correspond to the No DUBIC mode signals. See Table A-24 for the No DUBIC mode signal names.

Name	*Min. (ns)*	*Max.*	*Comment*
Td1	6		vidclk HIGH
Td2	6		vidclk LOW
Td3a	15		vidclk cycle (VGA Normal)
Td3b	66		vidclk cycle (VGA Slave)
Tp3c	40		vidclk cycle (Power Graphic mode)
Td4a	2	58	vidclk → blank/, vsync/, hsync/ (VGA Slave) (No DUBIC mode) vidclk → vidinf<2:0> (VGA Slave) (DUBIC mode)
Td4b	2	30	vidclk → vidinf<3:0> (Power Graphic mode)
Td5	2	58	vidclk → vgad<6:0>, va<11> (VGA Slave) (No DUBIC mode) vidclk → vgad<3:0>, oe<4:2>/, va<11> (VGA Slave) (DUBIC mode)
Td6a	5		vidrst/ → vidclk (VGA Slave)
Td6b	5		vidrst/ → vidclk (Power Graphic mode)
Td7a	30		vidrst/ HOLD → vidclk (VGA Slave)
Td7b	20		vidrst/ HOLD → vidclk (Power Graphic mode)
Td8	6		ldclk HIGH (No DUBIC mode) vidinf<3> HIGH (DUBIC mode)
Td9	6		ldclk LOW (No DUBIC mode) vidinf<3> LOW (DUBIC mode)
Td10	15		ldclk cycle (VGA) (No DUBIC mode) vidinf<3> cycle (VGA) (DUBIC mode)
Tdll	0.4	7	ldclk → vsync/, hsync/ (VGA) (No DUBIC mode) vidinf<3> → vidinf<1:0> (VGA) (DUBIC mode)
Td12	-4	1	ldclk → blank/ (VGA) (No DUBIC mode) vidinf<3> → vidinf<2> (VGA) (DUBIC mode)
Td13a	-4	2	ldclk → vgad<5:0> (VGA) (No DUBIC mode) vidinf<3> → vgad<3:0>, oe<4:3>/ (VGA) (DUBIC mode)
Td13b	-6	4	ldclk → vgad<6>, va<11> (VGA) (No DUBIC mode) vidinf<3> → oe<2>/, va<11> (VGA) (DUBIC mode)
Tvpd 1		10	vidclk → ldclk
Tlpd2	0	7	ldclk → sc<1:0>
Tlpd3	0.6	8	ldclk → smuxsl (1)
Tlpd4	1.2	7.5	ldclk → cde, blankN, even (1)
Tlpd5	1.2	7.5	Idclk → h[v]sync (1)
Tlpd6	0	20	ldclk ==> soeN<1:0>

Table A-24: Video Interface Timing Parameter List

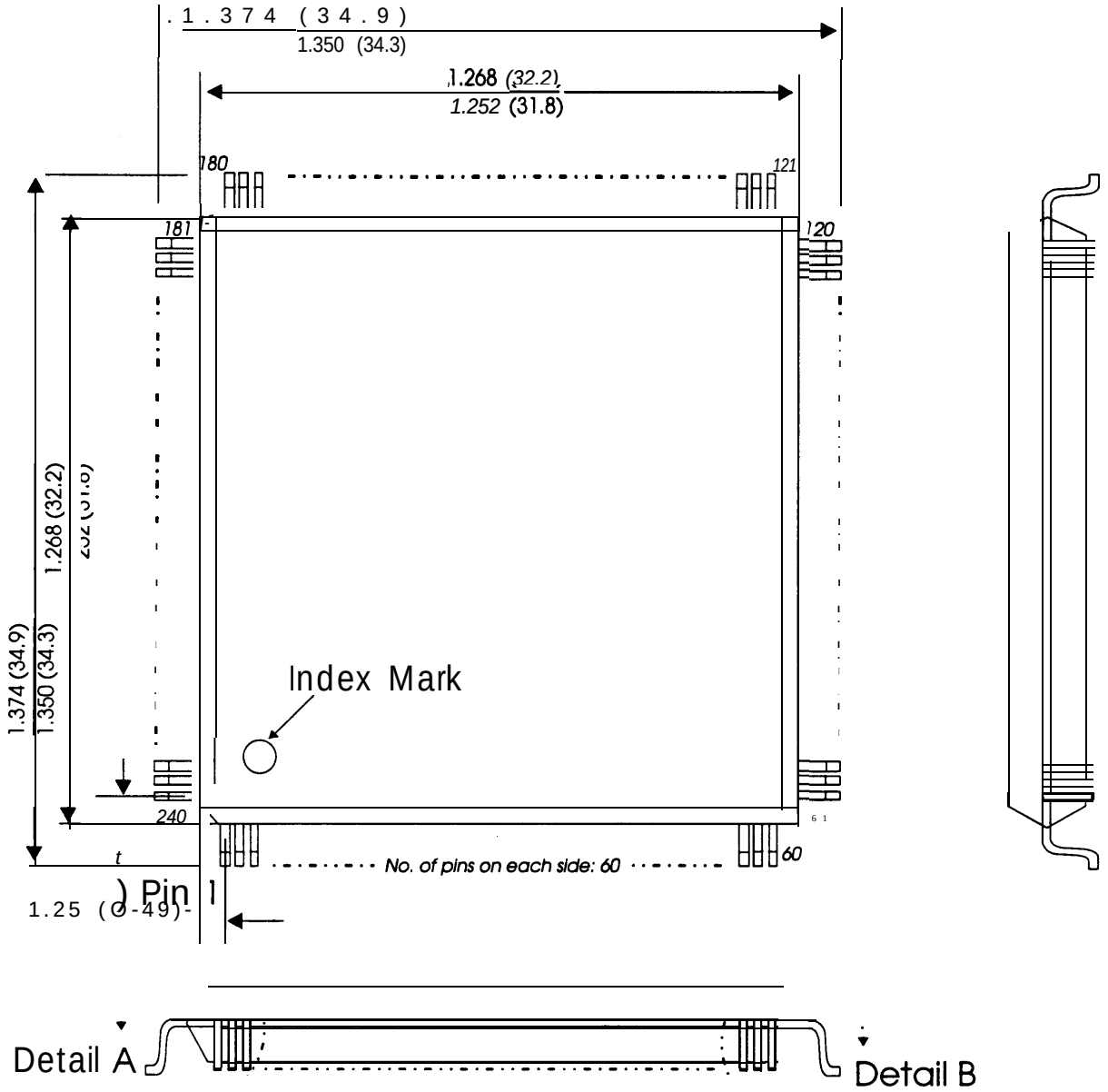
(1) External resistance capacitor (RC) network must be added to respect most RAMDAC hold time constraints (3 ns).

Note:

SOEN<0> and SOEN<1> are both inactive for at least 1 ldclk cycle when switching between banks.

A.3 Mechanical Specification

ATLAS PQFP 240-Pin (Plastic Quad Flat Pack) Square/Gull Wing



LEGEND: Maximum Inches (millimeters) / Minimum Inches (millimeters)

Figure A-22: ATLAS Mechanical Drawing

Appendix B: Customer Support

This appendix provides instructions on how to contact Matrox Customer support.

B.I Customer Support

. If you have a problem or question that isn't explained in this manual, you can contact the Customer Support Group at Matrox. Our phone numbers are:

. Outside the U.S. and Canada: (514) **685-2630**

. FAX: (514) **685-2853**

- You may address your technical support questions via electronic mail by posting a message to:

  GRAPH_TS@MATROX.COM

- You may also write to us at the following address:

  Matrox Electronic Systems Ltd.
  Customer Support
  1055 St. Regis Blvd.
  Dorval, Quebec
  Canada **H9P 2T4**

Power Graphic Mode Registers

Power Graphic Mode Register Fields

VGA Mode Registers, Part I

VGA Mode Registers, Part2

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