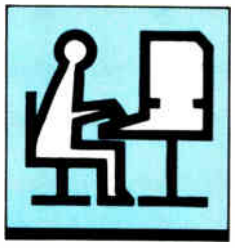
# WOULD YOU BELIEVE A 60-MIPS CLIPPER? ECL RISC CHIP IS EXPECTED NEXT YEAR

## Intergraph will also introduce a 20-mips CMOS version of the Fairchild-originated processor



Vendors like Sun Microsystems, MIPS Computer Systems, and Motorola have been loudly promoting reduced instruction-set chips—talking up versions of their processors that are not yet in production. And almost drowned out by the noise was another would-be contestant, the Clipper processor developed by Fairchild Semiconductor. But Intergraph Corp.'s Advanced Processor Division, the former Fairchild operation that passed through National Semiconductor Corp.'s hands and then to Intergraph of Huntsville, Ala., now looks to have a chance to beat the other guys at their own game and win support among system builders.

Intergraph has just formally introduced a new version of the Clipper, the C300, that cranks out 15 million instructions per second, and will be shipping a work station based on that chip set starting in December (see p. 105). And news has leaked out in a meeting of industry analysts of the imminent arrival of both a 20-mips CMOS version and an emitter-coupled-logic implementation said to be capable of 60 mips, all manufactured by Fujitsu Ltd., Tokyo. Intergraph declines to comment on future product plans, but sources close to the company confirm that it expects to have systems based on the two new Clipper versions on the market next year. First silicon on the ECL chips should be in hand during the first quarter of 1989, they say.

The high-end ECL version in particular would appear to be well ahead of other RISC chips that would to deliver comparable performance. For example, an ECL implementation of Motorola Inc.'s 88000 processor is not expected to reach silicon until sometime in 1991. In addition, sources close to Intergraph indicate that the ECL Clipper will offer higher performance than the planned ECL version of the 88000. The Sun camp hopes to get a faster version of the Sparc into production during 1989, but it will fall short of the ECL Clipper performance, if it can only do the projected 40 mips.

The RISC game is a serious one. The prize at stake is a market that by 1992 will be worth $505 million, says Robert N. Castellano, president of the Information Network, a market-research firm based in San Francisco. Castellano is predicting that the market for RISC chips will grow at a compound annual growth rate of 96.3% through 1992.

Howard Sacks, vice president and general manager of Intergraph's Advanced Processor Division in San Jose, Calif., believes that the RISC war is still wide open. Each major RISC combatant has a weakness in his battle plan, he says. For example, a weakness he sees in the MIPS and Sparc game plans is that neither has an integrated floating-point processor, cache, and MMU. All are found on the multichip RISC sets from Motorola and Intergraph.

> The ECL chip will beat the competition to market and it'll be downward compatible

What the Clipper offers is what others have been promising but not yet delivering, says Sacks. "Motorola cannot deliver the 88000 solution until 1990," he contends. "On the other hand, we can deliver in volume starting next month. If a designer started designing with the C300 Clipper chip now, he could have a 20-mips system in production by the middle of next year, a full year ahead of Motorola."

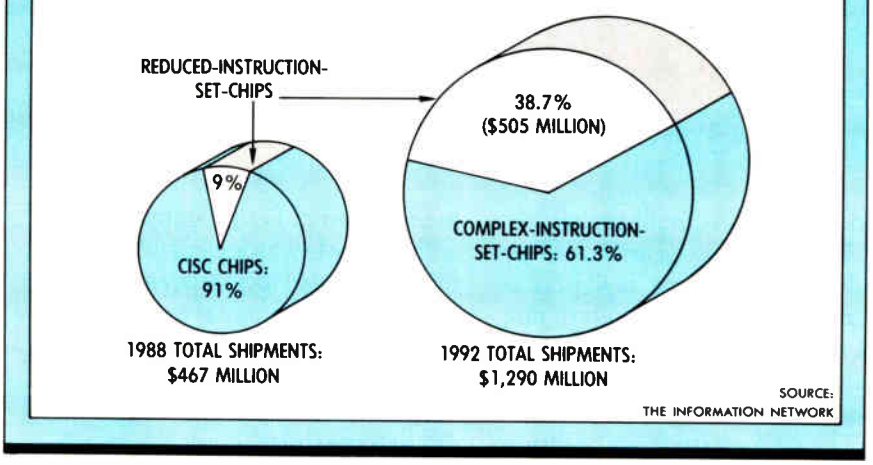
Sacks cautions that to achieve the full 20-mips performance with the C300, a system built with current Clipper parts would have to use non-Clipper cache chips. But sources say that the company is building a cache solution similar to what Motorola plans to have on the 88000 and will be demonstrating the new cache devices, possibly before the end of 1988.

One analyst who supports the belief that an ECL Clipper will arrive next year is Peter D. Schleider, a partner in the investment firm of Wessels, Arnold & Henderson in Minneapolis, Minn. "The processor, a board-level product called the E1, will be 100% software compatible with the existing Clipper," he says.

"Given this timetable, Intergraph has beaten both Sun and Apollo at the price-performance game," Schleider says. "Apollo would say that Intergraph has not beaten them because of the DN10000 [work station]. However, the ECL version of Clipper is completely software-compatible with the C100 and C300. Neither Sun nor Apollo can claim software compatibility with their earlier hardware."

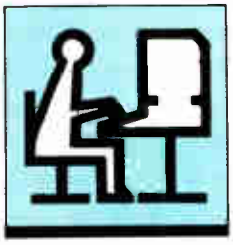
But Intergraph's weakness is credibility as a supplier. It "has to convince designers that the company has a strong production capability in Fujitsu, which will manufacture the chips in sufficient volume to meet demand; that it is still committed to developing new Clipper generations; and that it has a long life expectancy," Intergraph's Sacks says. One sign it is succeeding is the recent decision by DuPont's imaging division to buy up to 50,000 Clippers in the next few years. *–Jonah McLeod*

### RISC WILL CARVE A BIG SLICE



# A 10-MIPS WORK STATION IS HERE FOR UNDER $60,000

Intergraph's RISC-based system outperforms competitive work stations in its price range and offers engineers an extra-large CRT display



Today's competitive work-station marketing environment has systems houses playing a game of mips-manship. The trickiest part is that the game is based on next-generation reduced-instruction-set-computer chips not yet in production.

But one house, Intergraph Corp., plans to ship production versions of its next-generation RISC-based system next month. These work stations, called the 3000 Series, incorporate the Intergraph's new C300 Clipper chips, and are the first to achieve true, conservatively rated, 10-million-instruction/s performance in the class of work stations that cost less than $60,000, according to the Huntsville, Ala., company. The 3000 will easily outperform other current-generation RISC-based work stations in that price range, says Bruce Imsand, vice president of systems development at Intergraph.

In fact, the 40-MHz C300 Clipper chip allows the work stations to pump out up to 13 mips peak, a big increase over the 300 Series work stations, which run at 5 to 7.5 mips. And a 50-MHz version of the Clipper will boost performance to 15 mips next year during the summer.

Part of the performance boost comes from changes in the way load, store, and branch instructions are implemented, as well as changes in the floating-point processor—changes that do not affect software that was written for the earlier version of the Clipper, the C100. In addition, the 3000 Series work stations come with a 27-in. diagonal display, which allows designers to view much larger portions of their designs.

Intergraph's second-generation system is arriving ahead of the next-generation Sparc-based system from Sun Microsystems, Inc. of Mountain View, Calif., and ahead of the RISC-based stations from Digital Equipment Corp., Maynard, Mass., which will use processors developed by MIPS Computer Systems Inc. Only MIPS Computer, Sunnyvale, Calif., is currently shipping a system—the M/2000—with the new 20-mips versions of its chip, but it is priced at $100,000. Systems based on Motorola's 88000 RISC processor—a chip set with an architecture remarkably similar to the Clipper's—are still a long way off.

Intergraph's entry-level 3000 Series Model 3070, which will start shipping in December, will cost under $60,000, well below the $90,000 price of the 10-mips, Sparc-based Sun 4. The price difference results from the higher level of integration the C300 Clipper affords. "The C300 consists of four chips: an integer and floating-point processor on one chip, two cache and memory-management chips—one for instructions and one for data—and a clock chip. They all fit on a single card measuring 2.5 by 3 in.," says Eugene Grindstaff, senior manager of work-station sales and support at Intergraph.

"To achieve the equivalent of this [functionality] on other RISC-based systems requires a board of 13 by 15 in.," Grindstaff continues. "Besides using discrete-integer and floating-point processors, these designs use larger emitter-coupled-logic cache memories than the Clipper. They achieve a higher mips rating, but at a higher price, and without necessarily running benchmarks faster than our Clipper-based system."

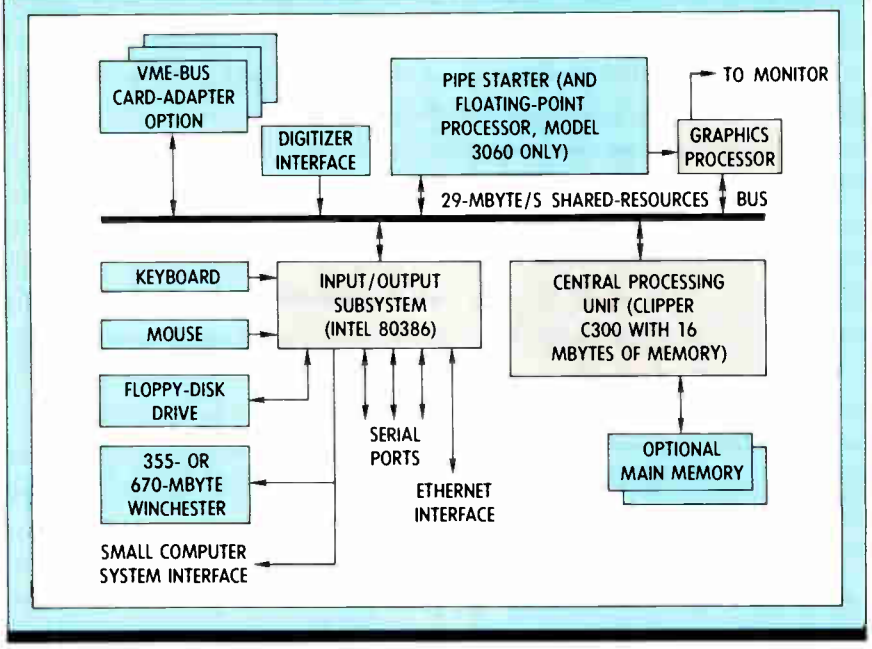
Intergraph's new system enters into a competitive market. One market research firm, Daratech Inc., based in Cambridge, Mass., predicts the market will grow 15%. In 1987, it was worth $4.56 billion and this year is expected to reach $5.2 billion. Daratech, specializing in computer-aided design, engineering, and manufacturing, breaks down that total market into three main segments: mechanical, electronic, and AEC (for architectural, electrical, and civil engineering). The lion's share of the 1987 market was held by the mechanical-design segment, at 59%, the electronics-design portion held 22%, AEC made up 17%, and others made up the rest.

Intergraph sells its work stations and the individual boards in them by themselves (see p. 109). It also sells software targeting the three design-automation market areas Daratech describes—mechanical, electronic, and AEC. Intergraph touts the standards they support—Unix System V, Ethernet networking, transmission-control protocol/internet protocol (TCP/IP), and the Network File System, just like the competitors based on Sparc and MIPS Computer chips.

**SAME LOOK.** Designing the 3000 Series work station was made much easier by the fact that the performance of the new C300 Clipper RISC-chip set looks the same as the C100, from the system's point of view, in all aspects but its clock frequency. But it is not the same. The new work station has a different memory system design, one that can accommodate the 40- and 50-MHz clock rates of the new and future versions of the Clipper chip.

"In addition, the new C300 can perform some functions in the burst mode to make better use of the memory bus than other

## A HIGH-THROUGHPUT THREE-PROCESSOR SYSTEM




**The Clipper CPU** in Intergraph's 3000-series work stations works faster with support from a graphics processor and a 386 handling input/output tasks concurrently.

RISC processors," says Grindstaff. This is apparent to the user. The cache and memory management units perform a four-word transfer in burst mode, a unique feature. With four-word transfer capability, the units prefetch more instructions into the cache at once to reduce the time penalty resulting from a cache miss.

"The critical characteristics [for a cache system] are how fast the cache operates and how quickly it can reload when there is a miss," says Gary Baum, director of marketing for Intergraph's Advanced Products Division in Palo Alto, Calif. This unit is the Fairchild Clipper group that National Semiconductor Inc. of Santa Clara, Calif., sold to Intergraph after acquiring Fairchild Semiconductor Corp. from its parent Schlumberger Ltd.

Grindstaff also contrasts the Intergraph system architecture, which has processors for computation, input/output tasks, and graphics processing, with the Sun 4, which saddles its Sparc processor with all three jobs. Besides the C300 Clipper, with its integrated integer and floating-point processor, there is a 3-mips Intel 80386 processor for I/O and a 40-mips proprietary graphics processor.

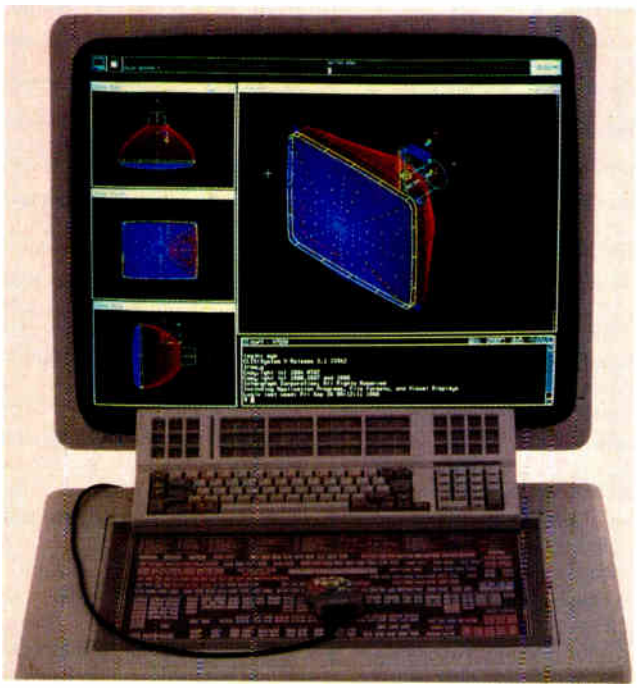
The Intergraph multiprocessor design leads to better performance than some machines with higher mips ratings, Grindstaff maintains. In a real-world application, computation, I/O, and graphics operations all occur concurrently. "The fact that the three processors distribute the load throughout the machine is the biggest reason for the performance advantage over competitive systems," he declares.

The C300 chip also has an advantage over other RISC processors available in that both integer and floating-point processors are on a single chip, so that the two processors can execute concurrently and communicate quickly. Furthermore, the floating-point unit in the C300 has been redesigned. "What we did was reduce the number of clock cycles needed for a floating-point operation significantly," Baum explains.

The C100 performs floating-point operations 2 bits at a time, while the C300 performs them 8 bits at a time. Thus the number of clock cycles needed to perform a double-precision multiply instruction, for example, is significantly reduced. The C300's floating-point performance is two to three times better than that of the C100, Intergraph says.

Another change that makes the C300 chip faster than the previous-generation C100 chip is the fact that the load, store, and branch instructions now execute in one less clock cycle. The academic approach to RISC-processor design holds that all instructions should execute in one clock cycle. So designers of central processing units must find their slowest instruction, typically a load, store, or branch instruction, and make that instruction execute in one clock cycle. Even though the computer could execute simpler operations. such as adds, in less time, they occupy the same amount of time as the slower instructions.

In designing the Clipper chip, which is patterned on the architecture of the Cray supercomputer, the fastest instructions, such as an add or register-to-register operation, are designed to execute in a single cycle. More time-consuming operations, such as loads, stores, or branch instructions, take up multiple clock cycles.



**A screen measuring 27 in.** on the diagonal, which displays 1,664 by 1,248 pixels, is available on Intergraph's model 3070 work station.

## Intergraph's next-generation system is arriving before rivals from Sun and DEC

"In the next generation of products, we may choose to keep the clock frequency fixed and reduce the [number of] clocks per instruction," says Baum. Running faster may not be desirable because of the problem of interfacing with TTL circuits outside the chip. "Imagine what would happen if we could achieve the same number of clocks per instruction that other RISC implementations achieve today, 1.5 to 2 clocks per instruction, with a 50 MHz clock—yet have a higher level of functionality per instruction than other RISC implementations running at 25 MHz," Baum says.

In addition to providing a faster computation engine, the 3000 Series work stations come with the first ever 27-in. workstation cathode-ray tube. In providing the big display, the company is responding to customer demand for a larger contiguous screen-display area in which to work. The new display offers a resolution of 1,664 by 1,248 pixels.

The reason it takes most companies a long time to implement new display technology is that the monitor circuit technology must catch up with the tube and yoke technology. "We have a close relationship with a number of Japanese manufacturers of tubes and yokes and they have been interested in working with us because we can help them develop their tube technology," Imsand explains.

"A year ago, we requested they build for us a 27-in. color tube for a data-display terminal," he says. "We felt that the timing and technology was right for this kind of product."

The implosion-protection and radiation-protection certifications required for data-display applications are major barriers to making these tubes generally available. Without some guarantee of sales, tube makers are not willing to make the investment needed to build and certify them. That guarantee is what Intergraph gave to these tube suppliers.

"After acquiring the 27-in. tube, we went about turning it into a data-display terminal," Imsand says. "We have had graphics-display controllers for two years that would drive 2 million pixels on a 19-in. tube." The display controller board comes with 2 to 8 Mbytes of CMOS RAM. It has bipolar digital-to-analog converters to produce the color drive for the three color guns and it has a number of CMOS application-specific integrated circuits developed by Intergraph.

The company's test marketing showed that there was no demand for a 2-million-pixel 19-in. display because people did not want to spend twice as much for a dot-resolution improvement of 41% over a conventional controller with 1-million-pixel capability. In addition, the light output of such a system decreases because it goes to a finer-pitch shadow mask to fit that many pixels into a 19-in. display. "We wanted to keep the number of dots per inch the same and take advantage of our 2-million-pixel resolution to drive a larger 27-in. screen display," Imsand says. *–Jonah McLeod*