82716/VSDD
VIDEO STORAGE AND DISPLAY DEVICE

- **Low Cost Graphics and Text Capability**
- **Minimum Chip Count Display Controller**
- **Displays Up to 16 Bit Map and Character Objects of Any Size**
- **On-Chip 16/4096 Color Palette**
- **On-Chip DRAM Controller**
- **On-Chip D/A Converters**
- **Arbitration of Processor RAM Requests**
- **NAPLPS and CEPT Compatible**
- **Objects Allow Windowing or Animation**
- **Resolution Up to 640 x 512 Pixels**
- **Up to 512K Bytes of Display Memory**
- **Compatible with 8 and 16 Bit Processors/Micro Controllers**
- **Twin Mode Operation for Higher Throughput**
- **Powerful External Sync and Overlay Capabilities**

82716/VSDD is a low cost, highly integrated video controller. It displays graphics and textual information using a minimum of chips. It allows the management of up to 16 display objects on the screen at any one time. These objects may be formatted as bit map or character arrays and can be used for windowing or animation.

An on-chip color palette allows the selection of up to 16 colors, from a range of 4096. The palette can be programmed to drive a set of on-chip D/A converters. The VSDD also provides DRAM controller functions.

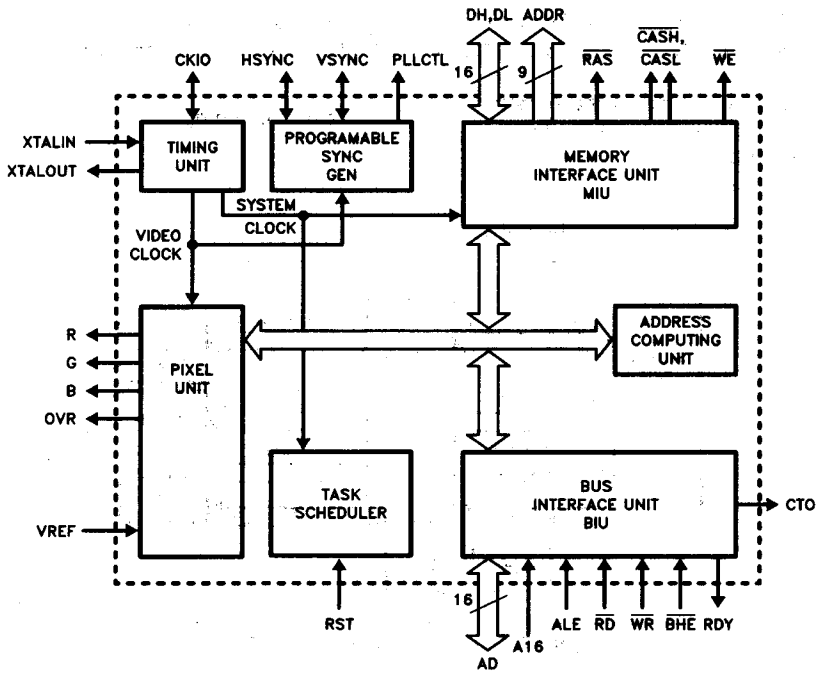

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Figure 1. VSDD Block Diagram

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GENERAL DESCRIPTION

The 82716/VSDD is a low cost, highly integrated VLSI CRT controller offering advanced display capabilities for Videotex and color graphics displays. Its internal architecture allows it to be connected to any Intel compatible processor. The screen image is constructed from various user-specified objects residing in the VSDD memory (mapped into the processor's address space). Pixels are taken directly from the memory for display on the screen. Characters are constructed employing user-defined RAM-based character generators. The VSDD takes the object data from its memory, buffers it, and runs it through a color palette and D/A converters to produce a video signal. The VSDD also supports overlapped objects and transparent pixels.

In conjunction with appropriate software, the VSDD can be compatible with such video standards as NAPLPS, CEPT or custom configurations. Its multi-window features and resolution make the VSDD ideal for:

- Home Information Systems, TV's, VCR's, Games and Home Computers
- Alphanumeric Color/Monochrome Terminals
- Real-Time Process Control Monitoring Equipment
- Videotex Terminals of the Alphageometric, Alphanumeric and Alphaphotographic Type
- Automotive Displays
- Medical Electronics

FUNCTIONAL DESCRIPTION

Bus Interface Unit (BIU): BIU is the interface between the CPU and the VSDD. CPU accesses the DRAM through the BIU.

Memory Interface Unit (MIU): It is the interface between the VSDD and the DRAM. MIU generates the control signals and the row and column addresses for DRAM.

Timing Unit: It consists of oscillator and clock generators. The Video and internal clocks are generated by timing unit.

Sync Generator: The sync generator controls the horizontal and vertical timings for raster generation (HSYNC and VSYNC).

Pixel Unit: The pixel unit contains pixel formatting unit as well as scan line buffers in which display information is placed for each scan line. It also contains the color lookup table (color palette) and D/A converters (DACs). DACs convert the digital color specifications to analog RGB signals for the monitor.

Task Scheduler: This unit is the control circuit of the VSDD. It provides the control signals for internal logic.

Address Computing Unit: It computes the DRAM addresses.

Figure 1 shows the block diagram of the VSDD.

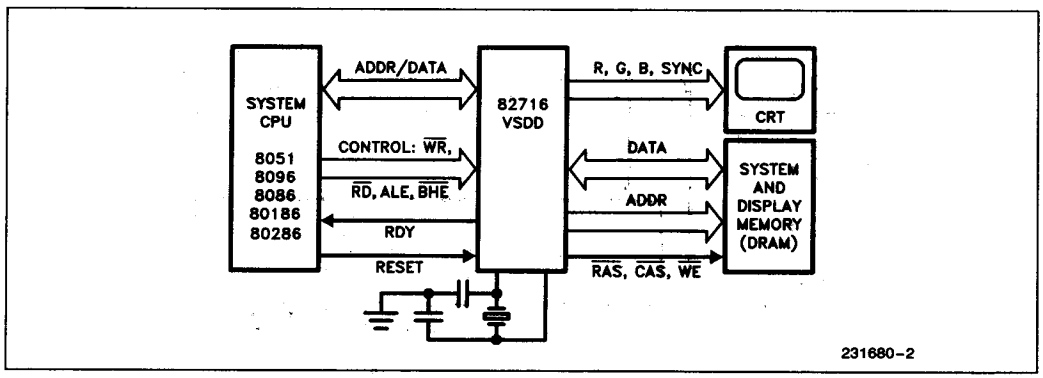


Figure 2. Simple System Configuration

SYSTEM OPERATION

The VSDD has 3 primary external interfaces: the CPU interface, the dynamic RAM display memory interface and the video pixel output.

The video subsystem looks like a memory to the CPU. All communication with the video subsystem occurs via that memory. The CPU develops display objects in memory and the VSDD constructs the actual video signal for the display from that memory. The CPU accesses the DRAM via the VSDD's BIU interface. The DRAM contains register segments and display information. CPU access of the dynamic RAM is controlled exclusively by the VSDD's DRAM controller.

The VSDD supports the simultaneous display of information from several sources. Each of these sources is an "object" and is assigned a display window within the VSDD screen. The VSDD can display up to 16 different objects. The size of each object can vary from a few pixels to larger than the full screen. The VSDD forms a scan line by gathering object information into one of the two internal line buffers. While one buffer is being updated with the next scan line, the other buffer is being read out to the color look-up table for display.

An object is defined as a list of pixels or string of characters within the VSDD DRAM memory. Each object is described by an entry, in the Object Descriptor Table (ODT) that contains positional information, color, size and various other attributes. The effective X-Y coordinates of an object can be changed at any time, without touching the object itself, thus allowing independent object animation as shown in Figure 3.

An object can be replaced by another object by changing the pointer in the ODT, allowing the possibility of many more objects in memory than on display at any one time.

Microprocessor Interface

The VSDD supports both 8 and 16 bit microprocessors and microcontrollers from all Intel compatible families. It uses a multiplexed data/address bus.

The VSDD accepts Read ($\overline{RD}$), Write ($\overline{WR}$), Address Latch Enable (ALE) and multiplexed Address and Data Bus (AD0–AD15) input signals as well as the Address 16 (A16) input. For 16 bit accesses the Byte High Enable ($\overline{BHE}$) input is also used. This allows the VSDD to distinguish between 16 and 8 bit ac-

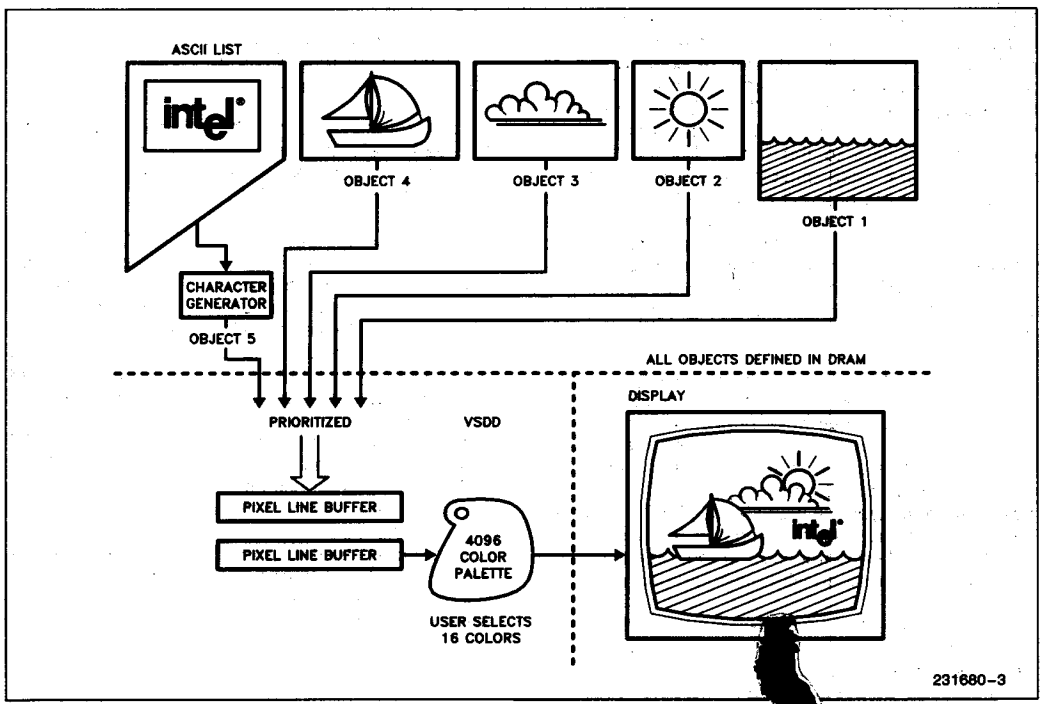


Figure 3. Building an Animation Scene

cesses. If the VSDD cannot service the processor request immediately, then it generates a ready signal (RDY) to extend the processor cycle. The VSDD allows the processor to access up to 512 Kbytes of display DRAM via memory mapping. CPU accesses DRAM with a 16 bit address plus a chip-select input A16 (maximum of 64 Kbytes of address space). A16 behaves like other address inputs. It should be active low.

During a bus access of the VSDD the RDY line is brought low to insert wait states. It is then driven high to indicate completion of the cycle. However after the CPU removes the $\overline{RD}$ and $\overline{WR}$ signal, the VSDD pulls the RDY line low again. It will remain low until the next address is latched into the 82716. If this address does not select the VSDD, the RDY line is driven high after the fall of ALE. If this address selects the VSDD, the RDY line remains low and begins the new data transfer cycle.

Arbitration of display memory access is carried out internally by the VSDD. The processor normally has priority over the VSDD Display Logic. Accesses made by the CPU through the VSDD to the display memory can impact VSDD's scan line building process.

When construction of a scan line is complete, the VSDD enters an idling state to wait till the previously constructed line is displayed. If display of the previously constructed line ends before construction of the new line is complete, the remainder of the line building algorithm is aborted. The VSDD's Construction Time Overflow (CTO) signal is activated to indicate this condition to the CPU. This can happen when there are more objects on the line than the VSDD has time to process or when CPU generated accesses to DRAM take up too much of the VSDD's time. To avoid this the VSDD can be programmed to allow only a certain (programmable) number of CPU accesses to the DRAM during line construction. The CTO signal is reset at the end of the Active Vertical Zone.

After each frame the user is able to specify the number of high priority accesses (n = 0 to 15) that the system processor may have during each line building process. Thus, n accesses from the system processor will be serviced with minimum delay concurrently with line buffer building. The (1 + n)th access will be delayed via wait-states (RDY) until completion of the line buffer. Whenever the VSDD isn't constructing a horizontal line, system processor accesses will be serviced with minimum delay.

For the MCS-51 family the interface is slightly different. This family has no RDY input and cannot be temporarily halted during a memory access. In this case the RDY output is programmed as a "Free Access" indicator. The 8051 can test this bit to see if the VSDD is using the memory and, if not, can gain access immediately. Because the 8051 has no RDY input, all read operations on the VSDD memory must be pipelined. In this mode a single read access to the DRAM requires two CPU read cycles. The first one is to address the desired DRAM location, but will not return data from that location. The second read cycle can be to any DRAM location, but will return the data that was addressed in the first cycle. Less overhead is required for a series of reads: The first read cycle returns random data, but after that each read cycle returns the data that was addressed in the previous cycle. In this configuration it should be noted that the $\overline{BHE}$ signal must be pulled high. The internal logic of the 82716 swaps data from the lower data pins onto the upper internal data lines during odd address accesses.

Video Section

The VSDD receives raw data from its display memory and performs all necessary conversions and manipulations to convert the display data to RGB signals. Two line buffers are implemented in on-chip dynamic RAM to store data from two complete scan lines. While one scan line is being displayed, the other buffer is being filled with the data for the next line.

The line buffer has the capacity to hold, at the user's selection, up to 640 pixels at 4 bits/pixel or up to 320 pixels at 8 bits/pixel.

4 bits/pixel are chosen if the display requires more than 320 pixels/line. This is called the High Resolution mode. This mode is selected by setting the HRS (High Resolution Screen) bit to 1.

The on-chip color look-up table [CLUT] contains 16 color entries defined by 12 bits (4-green, 4-red, 4-blue) for a possible palette of 4096 colors. The RGB signals are generated by 3 internal DACs (Digital-to-Analog Converter) whose inputs are the 12 bits (4/color) from the color look-up table. The actual data for color palette is stored in VSDD DRAM. The color palette in external DRAM consists of 16 entries. Each entry is 16 bits long with the lowest 4 bits specifying the address of the entry in the CLUT and the upper 12 bits specifying the color as shown in Figure 4. Four bit pixel codes are used to address the CLUT. The pixel code is matched with the lowest 4 bits of the CLUT entry and the pixel is given the color specified by the upper 12 bits. The color corresponding to the address 0010B is reserved for the background. At the end of every frame, VSDD accesses this data to load the on-chip color look-up table. The loading possibility at every frame allows the user to make real time changes in the color palette.

In some applications it is necessary to overlay external video signals. To support this the VSDD has an Overlay output pin "OVR" which can be used as a fast switch signal to allow display of external video instead of the VSDD output. The OVR pin is controlled by the outputs of the color look-up table. Whenever the color being displayed is RGB = 111H (0001 0001 0001B), the DAC driving the OVR pin goes to 'white' level [OFH or 1111B]. Any other color will cause the OVR pin to go to "black" level (00H or 0000B).

In a system where VSDD generated video will overlay video from an external video source, the "background" palette location 0010B would typically be programmed with 111H. Then, whenever the background color is displayed, user-supplied logic will switch in the external video source.

The overlay function is not available when the on-chip D/A converters are bypassed.

A digital mode is also available. In this mode the RGB and "OVR" pins provide direct digital outputs from the pixel buffer bypassing the internal color table and DACs. Up to 256 colors can be obtained in this mode using 8 bits/pixel with external color table and DACs. In 8 bits/pixel mode the data is available in two 4-bit nibbles. Low nibble always precedes the high nibble. The VSDD provides CKIO signal to latch low and high nibbles using off-chip decoders. Digital mode is also available with 4 bits/pixel.

The active high asynchronous Reset input is internally synchronized to both system clock and video clock. It must be held active for at least twenty (20) system clock AND video clock cycles. The reset active time should therefore be designed around the slowest of the two clocks. Care should be taken to keep noise off of the reset pin, since short duration spikes can start a "reset" sequence to begin, but not afford a proper length of time to complete.

Memory Mapping

The VSDD can support up to 512 Kbytes of DRAM. The DRAM is organized as 256K words of 16 bits by the VSDD for its own accesses. The VSDD allows CPU to access up to 512 Kbytes of DRAM via mem-

On Chip Color Look Up Table (CLUT)

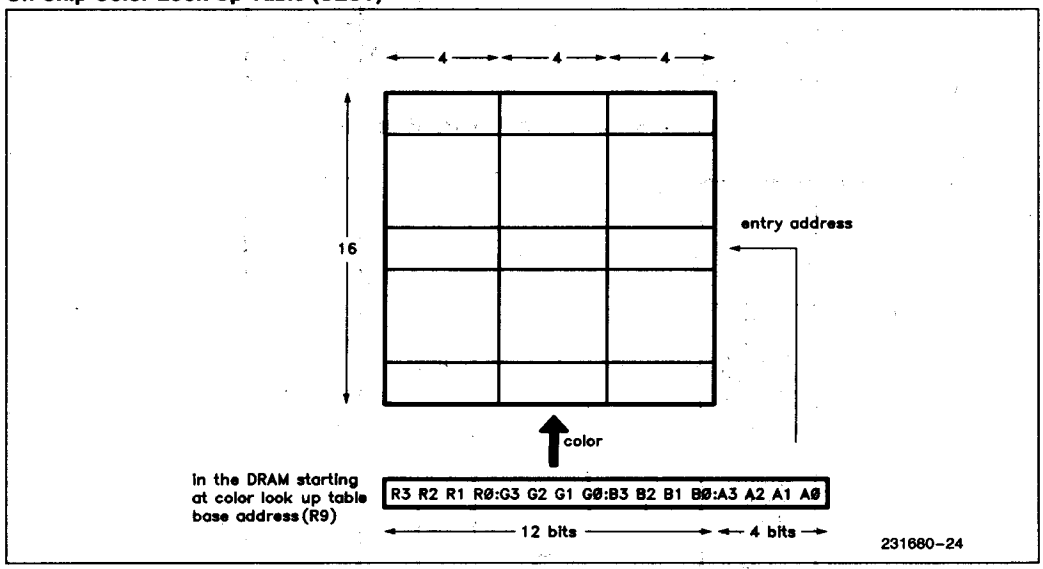


Figure 4. Filling the CLUT

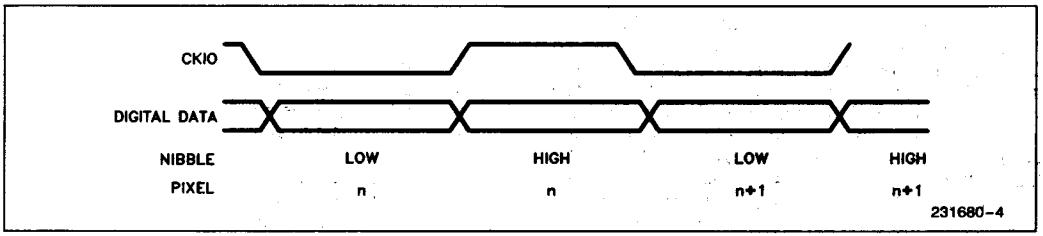
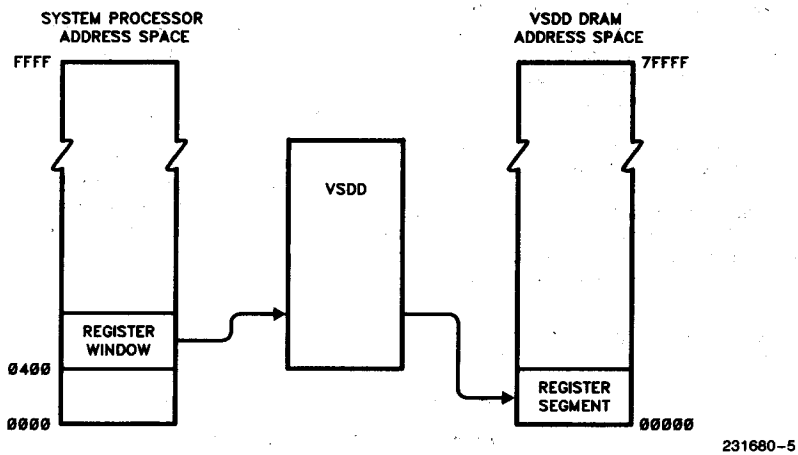
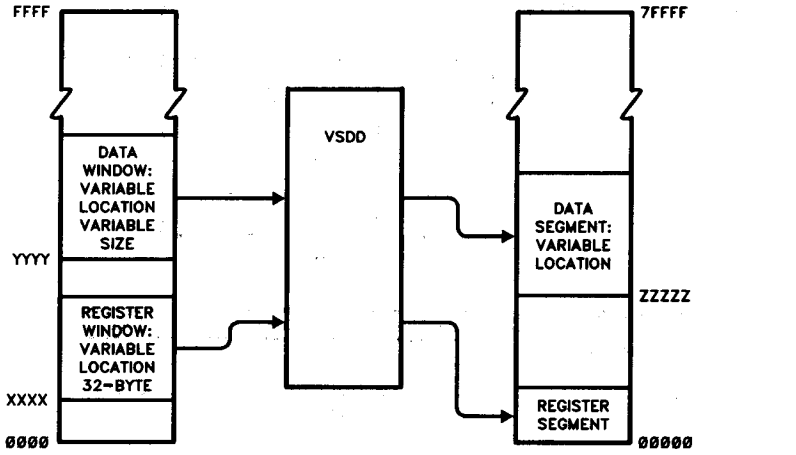


Figure 5. Digital Output Data, 8 Bits/Pixel (Hrs = 0)



(a) Pre-Initialization Memory Mapping



(b) Post-Initialization Memory Mapping

Figure 6. VSDD Memory Mapping

ory mapping. The DRAM is organized as 4 banks of 64K x 16 words. Even byte-addresses are in the lower half of a word and odd byte-addreses are in the upper half.

After the RST input to the VSDD goes inactive, the VSDD issues a single set of refreshes to DRAM. No further refreshes will occur until register R0 is initialized with DRAM configuration information. Once initialized, DRAM will be refreshed in a continuous loop.

The VSDD provides two logical windows to map portions of the processor address space into portions of the VSDD-DRAM address space. In the CPU address space, these windows are referred to as the Data Window and the Register Window. In the VSDD DRAM address space, they are referred to as the Data Segment and Register Segment. Thus the Data Window maps onto the Data Segment and the Register Window onto the Register Segment. The Windows are relocatable anywhere in the processor address space. While the Data Segment is relocatable within the VSDD DRAM address space, the Register Segment (32 bytes long) is fixed at VSDD DRAM starting location 00000H. The length of the Data Window/Segment can be specified from 4K to 64 Kbytes (Figure 6).

REGISTER SEGMENT

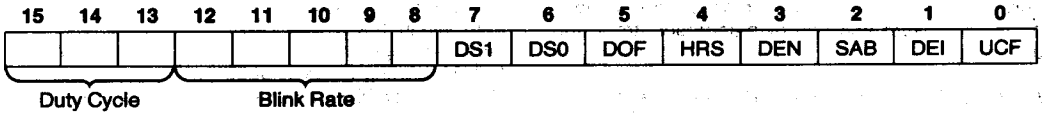
The register segment is the first 16 words (32 bytes) of VSDD DRAM. These registers contain the basic information for screen constants, DRAM organization, timing and base addresses. These registers have hardware counterparts on the VSDD. At the end of each frame, VSDD reads register R0 on to an internal register on the chip. If bit UCF (Update Control Flag) in R0 is set, the other registers will also be written on to the chip. These 16 registers are organized in DRAM as shown in Table 1.

Table 1. Register Window Organization

			VSDD Byte Loc
R15	Horiz. Constant 3	Vert. Constant 3	1EH
R14	Horiz. Constant 2	Vert. Constant 2	1CH
R13	Horiz. Constant 1	Vert. Constant 1	1AH
R12	Horiz. Constant 0	Vert. Constant 0	18H
R11	Access Table Base Address Counter (ATBAC)		16H
R10	Char Base Address 0 and 1		14H
R9	Color Table Base Address (CTBA)		12H
R8	Access Table Base Address (ATBA)		10H
R7	Object Descriptor Table Base Address (ODTBA)		0EH
R6	Priority Access Quantity (PAQ)		0CH
R5	Data Segment Base Address (DSBA)		0AH
R4	Data Window/Segment Length Mask (DWSLM)		08H
R3	Data Window Base Address (DWBA)		06H
R2	Register Window Base Address (RWBA)		04H
R1	Video Configuration Register 1 (VCR1)		02H
R0	Video Configuration Register 0 (VCR0)		00H

NOTE:
Where zeroes are shown in register locations, 0 must be written to those bits in order to ensure proper operation and upward compatibility with any future versions of this device.

R0: **Video Configuration Register 0**



Bit(s)	Description
UCF	Update Control Flag— If set (1), all the registers will be used to update the VSDD at the end of each frame. If not (0), only ATBA and VCR0 will be updated.
DEI	Digitally Encoded Color Information— If set (1), RGB and OVR outputs are digital. If not (0), RGB and OVR are analog.
SAB	Slow Access Bit— If set (1), then slow DRAM (page cycle time = 210 ns) can be used. If not (0), fast DRAM (page cycle time = 140 ns) can be used.
DEN	Display Enable Flag— If set (1), the VSDD display is enabled. If not (0), the VSDD display is disabled.
HRS	High Resolution Screen— If set (1), the maximum horizontal resolution is 640 pixels. If not (0), the resolution is 320 pixels.
Blink Rate	Blink rate of selected objects is set from 8 frames to 256 frames in multiples of 8 frames. For 50 Hz/60 Hz, this translates into blink rate increments of 160 ms/133 ms starting from 6.2 Hz/7.5 Hz (code 00000) down to 0.20 Hz/0.23 Hz (code 11111).
Duty Cycle	The duty cycle of the blink rate can be selected as below: 111 Always On 110 12.5% Off 87.5% On 101 25.0% Off 75.0% On 100 37.5% Off 62.5% On 011 50.0% Off 50.0% On 010 62.5% Off 37.5% On 001 75.0% Off 25.0% On 000 87.5% Off 12.5% On

DS1 and DS0 indicate the array size (16K, 64K or 256K) of the DRAM used to implement the display memory. DOF (DRAM organization flag) is used to indicate if the DRAM is bit-wide (DOF = 0) or nibble-wide (DOF = 1). See Table 2:

Table 2

DS1	DS0	DOF	Dram Configuration	Maximum Capacity	ADDR Pins Used		
					Row	Col	Bank Select
0	0	0	16K x 1	32 Kbytes	0–6	0–6	(None)
0	0	1	16K x 4	128 Kbytes	0–7	0–5	6, 7 at $\overline{CAS}$
0	1	0	64K x 1	128 Kbytes	0–7	0–7	(None)
0	1	1	64K x 4	512 Kbytes	0–7	0–7	8 at $\overline{RAS}$, $\overline{CAS}$
1	0	0	256K x 1	512 Kbytes	0–8	0–8	(None)

NOTE:
For 16K x 4, 2 bank select bits are emitted on address pin 6 and 7 when $\overline{CAS}$ goes low. By using external 2-to-4 decoders up to 4 banks can be selected. For 64K x 4, two bank select bits come out on address pin 8: one with the row address (MSB) and one with the column address (LSB).

R1: **Video Configuration Register 1**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				INL	MAS	SM	TMM	TMS	0	EVC	PCE	FAE	RE	PSA	PRE
Char Height															

Bit	Description
PRE	Pipeline Read Enable—If set (1), enables the pipeline read mode: CPU read cycles always return data from the previous read cycle. If not (0), then accesses are not pipelined.
PSA	Pre Scaler Active—This bit defines the relationship between the video clock frequency and the sync generator clock frequency. (Figure 7). GCLK is used for programming horizontal timings. If the video clock exceeds 16 MHz, the PSA bit should be set (1).
RE	This flag, when set (1), enables the CPU to read data from the display memory through 82716. If not (0), the output buffers of the VSDD are disabled, thus preventing CPU from reading the DRAM.
FAE	Free Access Enable—Enables the RDY pin to act as a free access indicator to the processor, if set (1).
PCE	Priority Counter Enable—If set (1), enables the VSDD to limit the number of CPU access to DRAM. Only valid with processors that have wait states.
EVC	External Video Clock—If set (1), it enables the CKIO pin to be used as input for a video clock up to 25 MHz. If not set, CKIO is a buffered clock output. (Figure 6)
TMS	Twin Mode Slave—Used for twin mode. If set (1), it specifies the VSDD as a slave, displaying only the even lines.
TMM	Twin Mode Master—In twin mode if set (1), it specifies the VSDD as a master, displaying only the odd lines and supplying sync to slave. The combination TMM = 0, TMS = 0 means twin mode operation is not in use. TMM = 1, TMS = 1 is illegal.
SM	Sync Mode—If set (1), enables the HSYNC pin to operate in composite sync mode. Otherwise HSYNC outputs horizontal sync.
MAS	Master—If set low, the VSDD accepts external synchronization signals and locks to it via an on-chip PLL circuit.*
INL	Interlace—If set (1), selects interlaced mode. If not (0), selects non-interlaced video.
Char Height	These 4 bits encode the number of scan lines per character. The number is encoded as a simple unsigned binary integer, except that 0000 means 16.

* If set high (1), HSYNC and VSYNC are outputs.

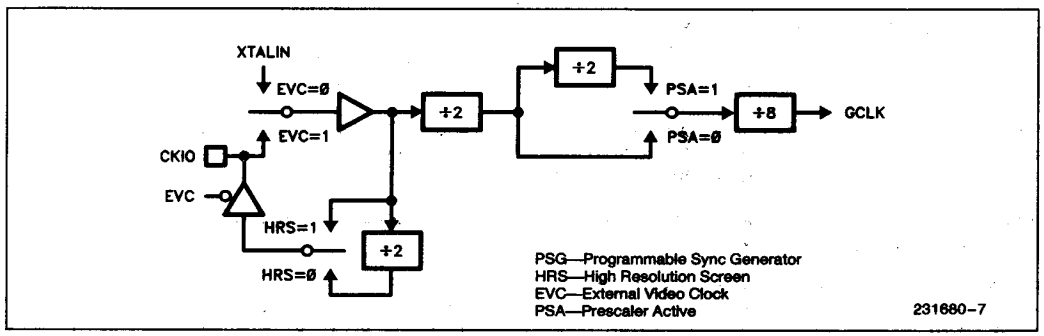


Figure 7. PSG Clock Generator

R2: **Register Window Base Address** (RWBA)

Register Window Base Address: R16–R5	0	TF2	TF1	ME

ME—Margin Enable: When set (1), a margin (in background color) can be added in a standard TV mode.

TF2,TF1 (Test Flags): If DEI = 1, then these flags determine what type of digital output is emitted. The output options are summarized in the table below:

DEI	TF2	TF1	Outputs	Signals
0	X	X	Analog	RGBO
1	0	0	Digital	Reds Only*
1	0	1	Digital	Greens Only*
1	1	0	Digital	Blues Only*
1	1	1	Digital	Pixel Code

NOTE:
*These three combinations can be used to test the on-chip color look-up table. The chosen combination selects one of the color components to be output via the DV3–DV0 outputs. The DEI bit has to be set to 1 to switch off the DACs.

R16–R5 specify the Register Window base address. This is the window (mapped into the CPU's address space) through which the CPU accesses the Register Segment of the DRAM. This register may be placed on 32 byte boundaries.

R3: **Data Window Base Address** (DWBA)

Data Window W16–W12	0	Screen Boundary SB9–SB3	0	0	0

SB9–SB3 Screen Boundary bits specify the upper 7 bits of the 10-bit x coordinate of the right edge of the screen. VSDD would process pixels up to x = to this number with lower 3 bits taken to be 1s. No pixels will be processed which are to the right of the screen boundary.

W16–W12 bits specify the Data Window Base Address. This is the window through which the CPU accesses the Data Segment of the DRAM.

R4: **Data Window/Segment Length Mask** (DWSLM)

L16	L15	L14	L13	L12	0	0	0	0	0	0	0	0	0	0	0

L16–L12 bits are the Data Window Length Mask, which specify the length of the Data Window in bytes, as follows:

L16	L15	L14	L13	L12	Data Window Length
1	1	1	1	1	4 Kbytes
1	1	1	1	0	8 Kbytes
1	1	1	0	0	16 Kbytes
1	1	0	0	0	32 Kbytes
1	0	0	0	0	64 Kbytes

R5: **Data Segment Base Address** (DSBA)

Data Segment S16–S12	0	0	BS0	BS1	0	0	0	0	0	0	0

BS1 BS0 divide the 512 Kbyte-address space into four banks of 128 Kbyte each. Note however that only bitmapped object data can reside in banks 1 through 3. All other display data such as character generators, register segment, access table etc. must be written to bank 0.

S16–S12 bits specify the Data Segment base address in the VSDD's address space. The display data is stored in the data segment. The data must be placed on the boundaries corresponding to the size specified in the data window length mask (see DWSLM).

R6: **Priority Access Quantity** (PAQ)

0	0	0	0	0	0	0	0	0	0	0	0	← P A Quantity →

PAQ 4 bits indicate the maximum number of CPU accesses to the DRAM that are allowed during building of each scan line, if PCE bit (in R1) is 1.

R7: **Object Descriptor Table Base Address** (ODTBA)

Object Descriptor Table Base: A15–A6	0	0	0	0	0	0

This register contains the word base address of the object descriptor table in the VSDD's address space. It is accessed by the VSDD at the end of each frame. This table must reside in bank 0.

R8: **Access Table Base Address** (ATBA)

Access Table Base Address: B15–B0

B15–B0 bits specify the Access Table base address. This table resides in the bank 0 of the VSDD's address space. This is a word-address. In a 256K word-address space, which requires 18-bit addresses, the two highest bits, corresponding to B16 and B17, are 0. It is accessed by the VSDD on each frame.

R9: **Color Table Base Address** (CTBA)

Color Table Base Address: D15–D0

D15–D0 bits specify the Color-Table base address. Color table is located in bank 0 in VSDD memory. This is a word-address. In a word-address space, which requires 18-bit addresses, the two highest bits, corresponding to D16 and D17, are 0. It is accessed by the VSDD on each frame.

R10: **Character Generator Base Address** (CGBA)

0	0	0	0	0	0	0	0	Char Gen 0	Char Gen 1

Char Gen 0, Char Gen 1 bits specify bits 15 through 12 of the base address of the two character generators. Bits 16 and 17 are 0 implying that both the character generators must be in bank 0. Refer to Character Generator section on how to access the generators.

R11: **Access Table Address Counter** (ATBAC)

Access Table Address Counter: C15–C0

C15–C0 bits point to the next Access Table entry to be used. It's maintained by the VSDD. The CPU can read this value but should not write to it. C16 and C17 are 0 as access table must be in bank 0. It is incremented after each scan line.

R12–R15: **Horizontal and Vertical Constants**

R15	HC3	VC3
R14	HC2	VC2
R13	HC1	VC1
R12	HC0	VC0

These registers hold data for screen timings. Four constants are defined for both horizontal and vertical timings as follows:

Screen Constant	What It Programs
HC0	Width of HSYNC
HC1	AHZ Start Time
HC2	AHZ Stop Time
HC3	Horizontal Sweep Time
VC0	Width of VSYNC
VC1	AVZ Start Time
VC2	AVZ Stop Time
VC3	Vertical Sweep Time

The horizontal screen constants are programmed in units of GCLK periods, offset by 1 (see Figure 7). If the programmed constant is 5, the actual time is 6 GCLK periods.

The vertical screen constants VC0 through VC3 are programmed in units of horizontal lines offset by 1. If the programmed constant is 5, the actual time is 6 horizontal lines.

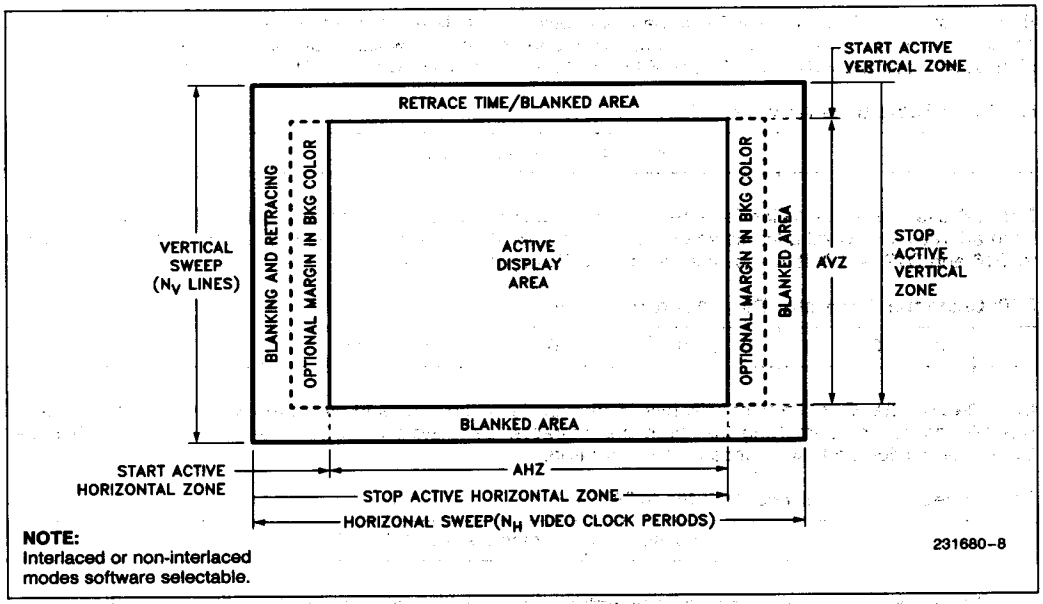


Figure 8. Programmable Raster Parameters

ACCESS TABLE

The Access Table contains the vertical positioning information for each object. The Table begins at the location designated by the Access Table Base Address register, R8 in the Register Bank. The Table contains one word in DRAM for each scan line in the Active Vertical Zone of the display.

The first line (at the top of the display) is associated with the word at the Table's base address. Within each word, bit number I is the Access Flag associated with object number I in the display and has the priority I. Object number 4 has a lower priority than object number 5 (see Figure 9).

b0 is the access flag for object 0, b1 for object 1, etc.

The Access Flags indicate to the VSDD which objects are to be present on which lines of the display. If an Access Flag is set (1), then there is to be no change in the object's display status; that is, if the object did not appear on the previous line, it will also not appear on this line. If the object's Access Flag is clear (0), the object's display status is reversed from what it was in the previous line. All objects are disabled at the end of the Active Vertical Zone.

An object is activated by putting a zero in the word corresponding to the scan line on which the object is first displayed. This turns on the object for all following scan lines. The object is toggled off by putting a zero in the scan line following the last line of the object.

At the beginning of each frame, the VSDD writes the contents of Access Table base address, R8, into Access Table Counter, R11. At the end of each line this counter is read into the Access Table Entry Address Register (on the VSDD). This entry address is then used to read the access flags for the line that is to be constructed. Access Table Entry Address is then incremented and written back into R11 preparing it for the next line.

Then the Access Flag Register is examined bit by bit to determine if there is a change in any object's display status. If object number I is to be displayed, then its Object Descriptor field is read. The base address for the Object Descriptor field for object number I is constructed from the Object Descriptor Table Base Address register, R7, by concatenating bits A15 through A6 from R7 with 4 bits representing the number I (i = 0 to 15).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

Figure 9. Access Flag Register

Then the Object Descriptor field base Address is:

0	0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	i3	i2	i1	i0	0	0

An Object Descriptor field is 4 words long, and all 4 words are read, so the last two bits in the above address are incremented to get all 4 words. Access Table and Object Descriptor Table must reside in bank 0.

Different Access Tables may be defined at the same time but only one is activated during any one frame. The Access Table allows easy vertical scrolling of an object. If the object scrolls down, truncating takes place by simply moving the window down and truncating the object when it moves off the screen. Moving up the screen is similar except when the object moves past the top of the screen, the object base address must be incremented to point to the start of the next displayed line.

OBJECT DESCRIPTOR TABLE

The Object Descriptor Table (ODT) contains a 4-word Object Descriptor field for each object in the display. This field describes the base address, attributes, and X-position of each object. This information is initialized as well as updated by the system processor. The 16 available object descriptors (128 bytes) are located contiguously in the ODT, starting at the location specified by the ODTBA register. The ODT is located in the VSDD DRAM.

There are two types of objects: bitmapped and character. Their descriptor fields are as shown below.

Bitmap Descriptor Field:

N: Current Object Entry Address is the address of the pixel data for the next scan line for the object. At the beginning of each frame, the VSDD copies Object Base Address into this field. This is maintained by the VSDD and should not be altered by the CPU.

O: Object Base Address points to the beginning of the object's data base. This is a 18 bit address. Only low 16 bits are specified here. O17 and O16 are specified elsewhere in the descriptor field.

W: Object Width indicates how wide the object is in "64 bit words". The width of the object must be a multiple of four 16-bit words. 000001 specifies a width of 1 "64 bit word", 111111 a width of 63 "64 bit words".

X: X0 coordinate is a 10-bit signed number (2's complement) encoding the horizontal position of the leftmost pixel in the object. X0 can be −512 to +511.

C/B: Character/Bitmap Object Specifier. C/B = 1 indicates a character object. C/B = 0 indicates a bitmap object.

Bitmap Descriptor Field:

HI	N: Current Object Entry Address N15–N0															
	O: Object Base Address O15–O0															
	W: Object Width						X: X0 Coordinate									
LO	0	0	0	0	C/B	R1	R0	0	O17	O16	OBL	BLA	0	TDE	C1	C0

R1, R0: Resolution: For a bitmap object, these 2 bits specify how many bits each pixel takes up in VSDD DRAM, as shown in the table below. HRS is a bit in R0.

Bitmapped Objects (C/B = 0)

HRS	R1	R0	Bits/Pixel
0	0	0	Do Not Use
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Do Not Use
1	0	1	Do Not Use
1	1	0	2
1	1	1	4

O17, O16: Two highest bits of the object base address.

OBL: Object Blinker = 1 causes the object to blink between foreground and background color. The blink rate and duty cycle are specified in R0 in the Register Segment.

BLA: Blanker = 1 turns the object off i.e. the object is not displayed.

TDE: Transparency Detect Enable. If TDE = 1, then pixels that are encoded as all 0's are not written into the Line Buffers. The buffers will retain the previous pixel data. Thus a low priority object will be visible through the transparent pixels of a higher priority object. When TDE = 0, then pixels that are encoded as all 0's are written into the line buffer. "0000B" is then one of 16 color codes.

C1 C0: Default Color Specification. For bitmapped objects that are stored in external VSDD memory in the 2 bits/pixel mode, these two bits extend the pixel specification to 4 bits.

Character Descriptor Field:

Z: Slice Number contains a character object's slice number for the next scan line. It is reloaded by the VSDD once per frame with the slice number (YS3–YS0).

N: For character object, it's the beginning address of the current line of text. The entry address is formed of O15–O12 and N11–N0. Hence, a character object may not extend across a 4K word boundary. Two highest bits—O17, O16—are zero for character objects. Between each frame, lowest 12 bits of object base address are written into N.

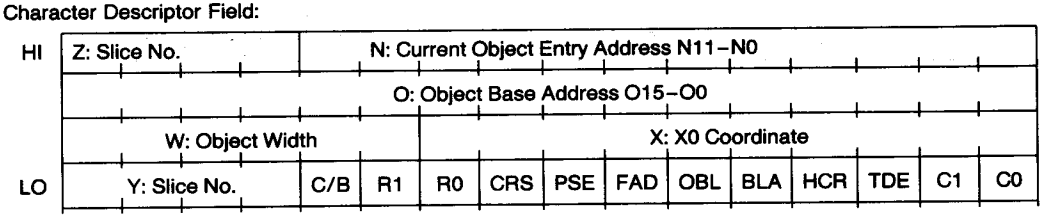
Y: Start Slice Number is the first (topmost) character slice of this object. The CPU can modify this field to produce a scrolling effect in the display of the text. Y = 0 is the bottom of the character and Y = Character height (defined in R1) is the top.

R1 R0: Resolution: For character objects, R1 and R0 specify the width of the character, as shown in the table below.

Character Objects (C/B = 1)

HRS	R1	R0	Pixels/Char
0	0	0	6
0	0	1	8
0	1	0	12
0	1	1	16
1	0	0	16
1	0	1	6
1	1	0	8
1	1	1	12

Character Descriptor Field:



FAD: Full Attribute Definition = 1 means character descriptions are 3 bytes long. Each character is encoded as an ASCII byte plus a 2-byte attribute word. FAD = 0 means character descriptions are 1 byte long.

CRS: Conceal/Reveal/Select. If FAD = 1, then CRS = 1 enables the MSK bit in the character's attribute word to cause the character to be concealed. If FAD = 0, then CRS selects one of two character generators. CRS = 0 selects CGBA0 as specified in the register segment. CRS = 1 selects CGBA1.

PSE: Proportional Spacing = 1 enables proportional spacing of characters.

HCR: High Color Resolution. If FAD = 1, then HCR = 1 means use 16-color palette for characters and their backgrounds. If FAD = 1, then HCR = 0 means use 8-color palette (see Attribute definition). If FAD = 0, then HCR should be 0.

C1 C0: For character objects that are stored in external memory in the 1 byte/character mode, these two bits become the MSBs of the foreground/background colors of the characters as shown below.

Foreground color = C1 C0 0 1
Background color = C1 C0 0 0

OBJECT DATA

Objects are rectangular windows on the screen. Object data begins at the Object Base Address specified in the "O" field of the Descriptor table. The length of the data file depends on the object's height, width and resolution. The width of the object is specified in 4-word units by the 'W' field in the Object Descriptor. For example, if the 'W' field contains 001010 then the object is ten 4-word units wide.

The VSDD will read in 10 × 4 = 40 words of object data for each scan line in which the object appears. For bit-mapped objects, the beginning address of each block of 40 words is constructed from the 'N' field in the Object Descriptor. The 'N' field is updated for the next scan line after each block of data is read.

For character objects, 'N' field is used to construct the beginning address of a line of ASCII text. The object itself may consist of many lines of text. Each line of text consists of individual scan lines—each scan line presenting one "slice" of the text character. When the final slice of a line of text has been constructed the 'N' field is updated to the next line of text.

The Table 3 shows minimum and maximum width of character and bit-mapped objects.

Table 3

Object Type		Min. Width	Max. Width
Bitmap	2 Bit/Pixel	32 Pixels	2016 Pixels
Bitmap	4 Bit/Pixel	16 Pixels	1008 Pixels
Bitmap	8 Bit/Pixel	8 Pixels	504 Pixels
Character	1 Byte/Char	8 Chars	504 Chars
Character	3 Byte/Char	1 Char(2)	168 Chars(1)

NOTES:
1. The last 16 bit-word of the object will not be used.
2. The minimum memory required is actually 4 x 16-bit words. The second character can be eliminated by setting its transparent attribute bit.
3. For 3 bytes/character objects, full memory utilization can be obtained if the width of the object is a multiple of 12 words.

For character objects, two formats are defined. The first is a 1 byte/character mode. In this mode 2 ASCII character codes are stored in each DRAM word. The second format uses 3 bytes/character. They are formed as follows:

1 Byte/Character

X15	X0
2nd Character	1st Character
A7:A6:A5:A4:A3:A2:A1:A0	A7:A6:A5:A4:A3:A2:A1:A0

- A7–A0 = Character ASCII Code

3 Bytes/Character

	X15	X0
HI	2nd Character Attribute Field	
	1st Character Attribute Field	
LO	A7:A6:A5:A4:A3:A2:A1:A0	A7:A6:A5:A4:A3:A2:A1:A0
	2nd Character	1st Character

The attribute field is formatted as follows:

CG	TFG	TBG	DW	MSK	INV	BLI	UND	FC3	FC2	FC1	FC0	BC3	BC2	BC1	BC0

WHERE:

- A7–A0 — 8 bit ASCII code or any other 8 bit character code.
- BC2–BC0 — Background color.
- BC3 (U/L) — When HCR = 0, it specifies the upper or lower half of the character in double height mode. When set (1), it specifies the upper half. If not (0), lower half is specified. When HCR = 1, it is used as the MSB of the background color.
- FC2–FC0 — Foreground color.
- FC3 (DH) — When HCR = 0, it specifies the character to be double its normal height when set (1). When HCR = 1, it is the MSB of the foreground color. When HCR = 0, and DH = 0, then U/L must be set to 0.
- UND — If set (1), the character is underlined.
- BLI — Enables the character to alternate between foreground and background color when set (1).
- INV — If set (1), the foreground and background colors are reversed.
- MSK — If set (1), the character disappears from the screen (when CRS = 1) i.e. foreground color is same as background color. When CRS = 0, MSK attribute is ignored.
- DW — If set (1), the character is expanded to double width.
- TBG — Sets background transparent, when TBG = 1.
- TFG — Sets background transparent, when TFG = 1.
- CG — Selects one of two character generators.

Character Generators

The VSDD allows the simultaneous use of two independent character generators of 256 characters each. Bits 15–12 of their base addresses are specified in R10 in the Register Segment. Each character generator must begin on a 4K word-address boundary in memory bank 0.

The address for a character generator consists of four fields: See Figure 10

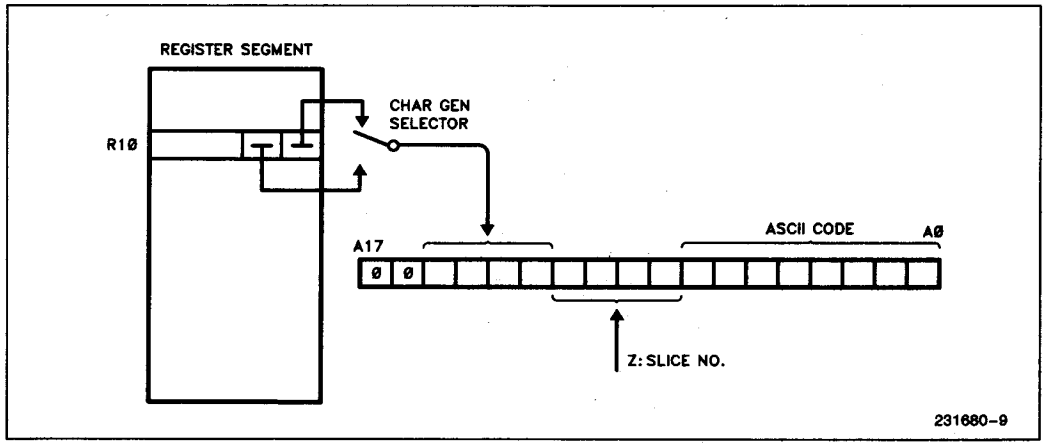


Figure 10

A character set consists of H blocks of 256 words, where H is the character height in scan lines. Each character is divided into H slices with slice zero defined as the bottom of the character and slice H-1 is the top scan line of the character. Character height, globally defined for the whole frame in register R1 can be up to 16.

Each slice occupies one word in DRAM. Within the word, the slice is encoded as a sequence of pixel bits, the leftmost pixel being the LSB in the word. If a pixel bit is 1, then the pixel is to be given foreground color. If a pixel bit is 0, the pixel is given background color.

If the characters are encoded in plain ASCII (FAD = 0), then the character generator is selected by the CRS bit in the Object Descriptor. If the characters are encoded with full attributes (FAD = 0), then the character generator is selected by attribute bit CG.

As the characters are defined in DRAM, a new version of the character generator can be obtained by either:

— modifying the character generator directly or

— updating one set while the other set is being displayed. The set can then be changed by updating the CGBA pointer in the register segment. This method results in an instantaneous change on the screen.

PICTURE CONSTRUCTION

VSDD supports, 2, 4 or 8 bits pixels. Up to 640 x 512 pixels can be supported using 2 or 4 bits/pixel. In the 8 bits/pixel mode, a picture size of 320 x 512 can be supported. In this mode only the lower 4 bits of the byte are used by the color look-up table, the upper four are ignored. In digital mode, using 8 bits/pixel 256 colors can be obtained with external color palette and DACs.

The VSDD starts picture construction at the beginning of the frame using the logic flow shown in Figure 11.

At the beginning of each frame, the contents of Access Table Base Address, R8 is copied into R11, Access Table Counter. Simultaneously, the VSDD also loads the color look-up table from the DRAM into the on-chip color look-up table. This feature enables the user to select a different set of 16 colors at every frame.

After each scan line, R11 is loaded into an on-chip register, Access Table Entry Address Register by the VSDD. The on-chip register (Access Table Entry Address) points to an access table entry for the line that is to be constructed. The VSDD reads this entry into an on-chip register called the Access Flag register. (R11 is then incremented by 1 to point to the access table entry for the next scan line.) (Simultaneous to this operation, the VSDD fills the line buffer with the specified background color.) Each access table word contains 16 flag bits—one for each object. Access flags determine which objects are present on the line. Object priorities are fixed with object 15 being the highest and object 0 being the lowest.

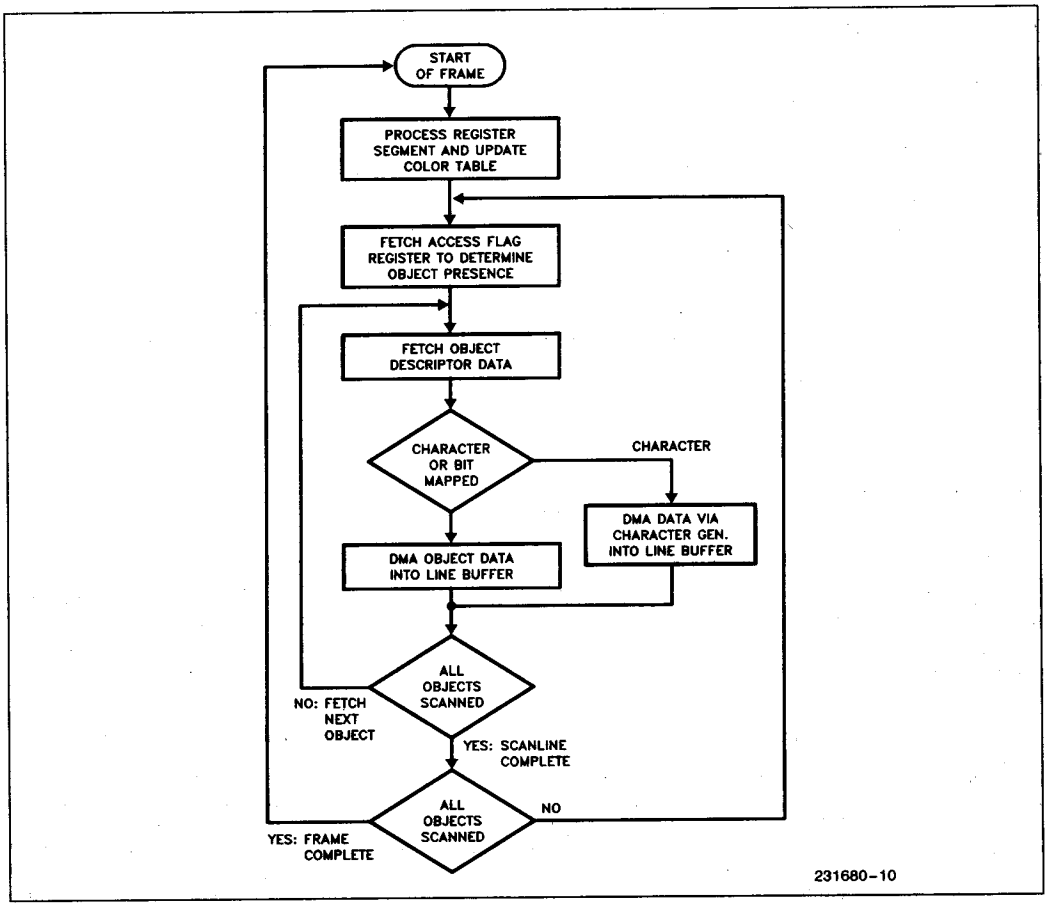


Figure 11. Scan Line Building Process

If an object is present, then its object descriptor data is read from the VSDD DRAM. This determines the object's width, horizontal position, type and where to find the display data for this line of the object. For bit-mapped objects the display data passes directly from the VSDD DRAM into the line buffer.

For character objects, the data passes via a character generator into the line buffer. The appropriate slice of character pixel information is written in the appropriate horizontal position in the line buffer. Both character and bit-mapped data overwrites the background pixels that were previously written into the buffer.

This procedure is repeated for each object that is present on the line. For overlapped objects, the high priority data overwrites the low priority data. Low priority object will be hidden behind the high priority object. The priority of objects are determined by the order in which they are written into the line buffer. For example, the object number 5 has higher priority than the object number 4. Object number 1 is described in the first Object Descriptor Table entry, object number 2 in the second entry, etc. Transparent Pixels (0000B, when TDE bit is set) are not written into the line buffer. Previous pixel data is retained at the location where transparent pixels are present. Thus a lower priority object can still be visible behind the transparent parts of a higher priority object.

The construction process may result in more pixels being read from the DRAM than are actually displayed on the line. Since only a finite time exists for line construction, it is important that the number of objects and the amount of overlap between the objects be considered when examining display performance.

When construction of each line is complete the VSDD enters an idling state to wait till the previously constructed line finishes being displayed. If display of the previously constructed line ends before construction of the new line is complete, the remainder of the line construction algorithm is aborted, and the VSDD's Construction Time Overflow signal is activated to indicate this condition to the CPU.

Construction time overflow can result when there are more objects on the line than the VSDD has time to process or when CPU-generated accesses to DRAM takes up too much of the VSDD's time.

Figure 12 shows the VSDD and DRAM operation during line building process.

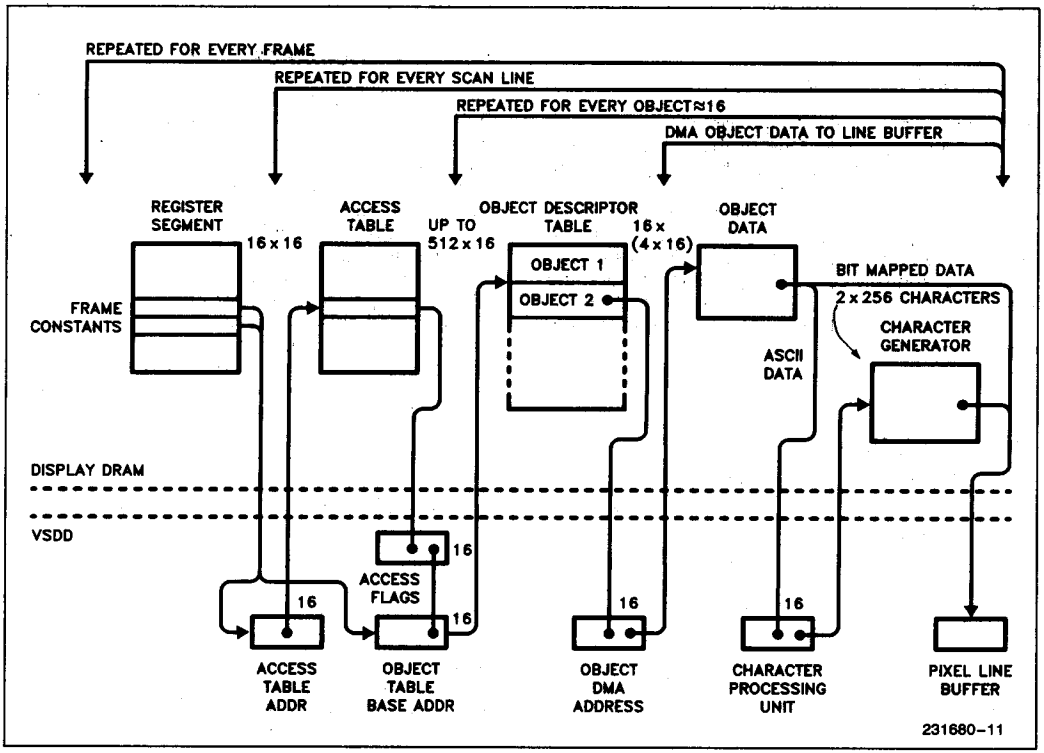


Figure 12. VSDD and DRAM Operation

Movement of objects is accomplished easily in the x direction by changing the value in the object descriptor. Movement in the y direction is accomplished by moving the bits which turn the object on and off within the access table. If the "off" bit falls below the bottom of the access table, the object will automatically be truncated at the bottom of the screen. Moving in an upwards direction requires that the object base address in the desciptor table be changed to truncate the top of the object.

TWIN-MODE OPERATION

For higher performance, it is possible to connect two VSDD chips in parallel. One of them is designated as the master and the other as the slave. The master generates information for the even lines of the display together with all the system timing. The slave accepts the synchronization pulses as inputs and displays the odd lines of the picture. Because each VSDD is essentially constructing half the picture, the scan line construction time is twice as great, allowing higher throughput in terms of information processed and objects displayed.

PERFORMANCE

The number of objects that a VSDD can support on a scan line is dependent upon the screen resolution, refresh rate, DRAM type, and resolution per object. In addition, the percent overlap of each object can affect the performance. Usually the amount of overlap can be kept to a minimum by keeping the object window only as large as necessary.

VIDEOTEX STANDARDS

The VSDD has been designed for these types of application. It can support several Videotex standards from Europe, North America and Japan. Although it has been optimized for alpha-geometric applications such as NAPLPS, GKS, and VDI, it is capable of supporting the existing alpha-mosaic standards and the higher resolution alpha-photographic standards. It supports most of the European CEPT standard that includes PRESTEL and TELETEL by using static character objects. In addition it offers bit-map objects and movement. Alpha-photographic standards such as Picture PRESTEL and Picture TELETEL can be supported in 8 bit pixel mode with the addition of external color translation and higher resolution hardware.

Pin Description

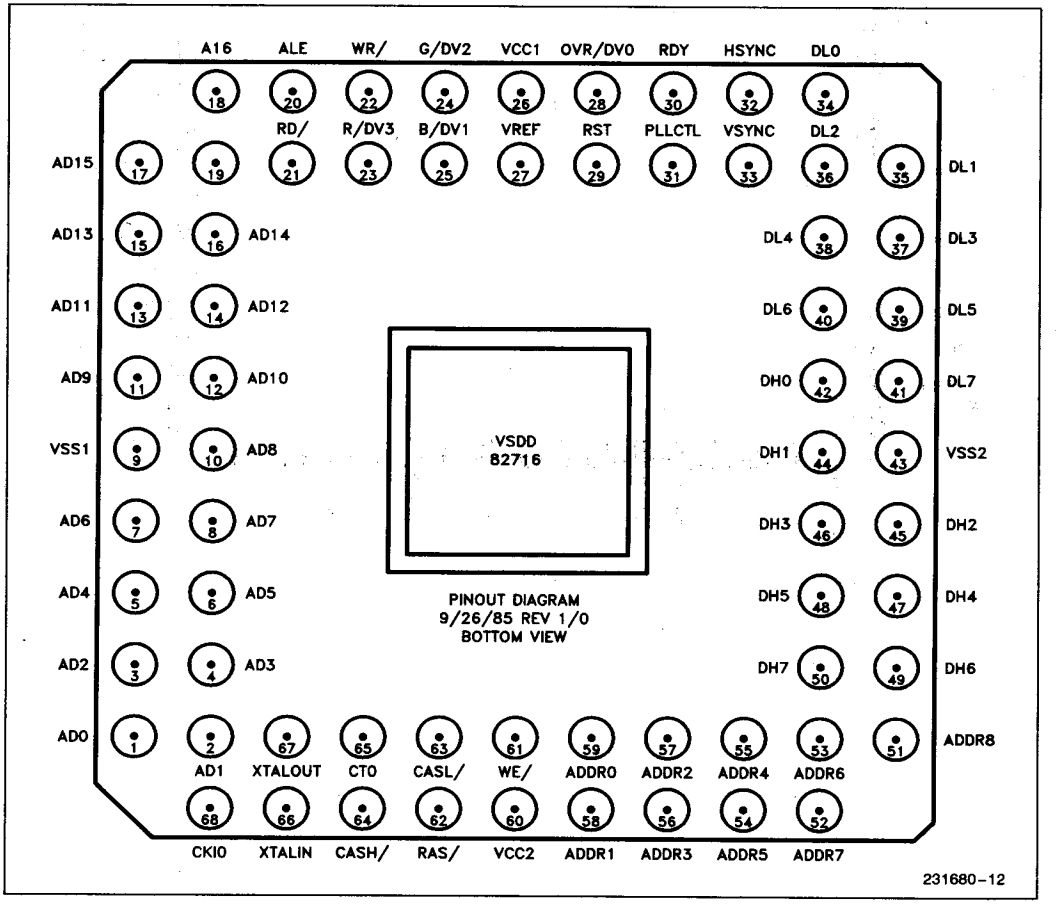
Symbol	Pin	Type	Function
AD0–AD7 AD8–AD15	1–8 10–17	I/O	Processor system bus multiplexed address/data.
A16	18	I	Programmable chip select.
$\overline{BHE}$	19	I	Byte high enable.
ALE	20	I	Address latch enable.
$\overline{RD}$	21	I	Read strobe from processor.
$\overline{WR}$	22	I	Write strobe from processor.
RESET	29	I	Places the VSDD in initialization mode.
RDY	30	O	Ready-wait state for 86/88/96 and free access indicator for MCS-51.
R/DV3, G/DV2 B/DV1	23,24 25	O	Red, green, and blue analog outputs or 3 bits of digital output.
OVR/DV0	28	O	Output signal or fourth digital output.
V_{REF}	27	I	Analog voltage reference.
HSYNC	32	I/O	As an output it supplied horizontal or composite sync. As an input it synchronizes the VSDD with an external video signal.
VSYNC	33	I/O	As an output it provides vertical sync. As an input it synchronizes the VSDD to external video.
DL0–DL7	34–41	I/O	Data input/output to DRAM low order byte.
DH0–DH7	42–50	I/O	Data input/output to DRAM high order byte.
ADDR0–ADDR8	59–51	O	DRAM row and column addresses.
$\overline{RAS}$	62	O	Row address strobe.
CTO	65	O	Construction time overflow.
$\overline{CASL}$	63	O	Column address strobe low.
$\overline{CASH}$	64	O	Column address strobe high.

Pin Description (Continued)

Symbol	Pin	Type	Function
$\overline{WE}$	61	O	Write enable.
XTALIN	66	I	Oscillator input or crystal terminal.
XTALOUT	67	O	Oscillator output or crystal terminal.
CKIO	68	I/O	As output it serves as a buffered dot clock. As an input it is used to receive external dot clock.
PLLCTL	31	O	PLL control used to fine tune oscillator
V_{CC}	26, 60		5 volt main supply.
V_{SS}	9, 43		Digital ground.

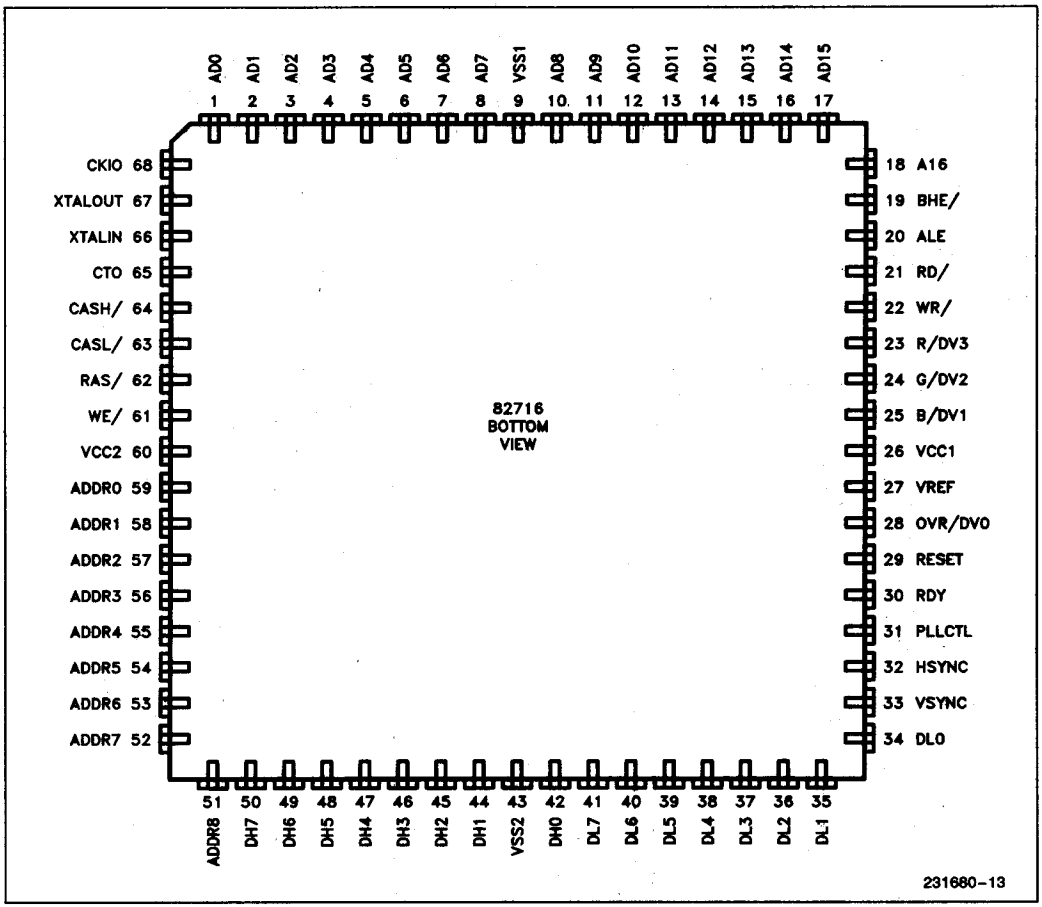
PACKAGING

Pinout for a 68-pin Pin Grid Array Package is shown below.



PLCC PACKAGE

Pinout for a 68-pin plastic leaded chip carrier is as below:



ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0 to 70°C
Storage Temperature .....−65°C to +150°C
Voltage from any Pin with Respect to V_{SS} .....−1.0 to +7.0V
Power Dissipation 3W
V_{REF} 2V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS T_A = 0 to 70°C, V_{CC1}/V_{CC2} = +5V ±10%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 µA
V_{OL}	Output Low Voltage		0.4	V	I_{OH} = 2.0 mA
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5V	V	
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IHC}(1)	Input High Voltage Clock	3.5	V_{CC}+0.5V	V	
V_{ILC}(1)	Input Low Voltage Clock	−0.5	0.8	V	
I_{LI}	Input Leakage Current		±10	µA	0V < V_{IN} < V_{CC}
I_{LO}	Output Leakage Current		±10	µA	0.45V < V_{OUT} < V_{CC}
I_{CC}	Power Supply Current		300	mA	
C_{IN}	Capacitance of Inputs		10	pF	f_c = 1 MHz
C_{IO}	Capacitance of I/O's		15	pF	f_c = 1 MHz
C_{OUT}	Capacitance of Outputs RAS, CASL, CASH, WE, OE		15	pF	f_c = 1 MHz
C_{OUT}	Capacitance of Outputs		10	pF	f_c = 1 MHz
C_{OUT}	Capacitance of Outputs (R/DV3, G/DV2, B/DV1, I/DV)		7	pF	f_c = 1 MHz
C_{RAS}	RAS Load		200	pF	
C_{CAS}	CACSn Load		100	pF	
C_{WE}	WE Load		200	pF	
C_{Dij}	DL0–DL7 DH0–DH7 Load		100	pF	
C_{ADD}	ADD0–ADD8 Load		150	pF	

NOTE:
1. For XTALIN, CKIO and RESET pins only.

A.C. CHARACTERISTICS T_A = 0 to 70°C, V_{CC1}/V_{CC2} = +5V ±10%

TIMING REQUIREMENTS

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{CLCL}	CLOCK Cycle Period	70	200	ns	
DCCK	Duty Cycle	40	60	%	
t_{CLCH}	CLK Low Time	0.4 t_{CLCL}		ns	
t_{CHCL}	CLK High Time	0.4 t_{CLCL}		ns	
t_{VCLCL}	VIDEO CLOCK Cycle Period	40	200	ns	
DCVCK	Duty Cycle	40	60	%	
t_{VCILIH}	Video Clock Rise Time(1)		10	ns	From 1.0V to 3.5V
t_{VCIHIL}	Video Clock Fall Time(1)		10	ns	From 3.5V to 1.0V
t_{ILIH}	Input Rise Time		20	ns	From 0.8V to 2.0V
t_{IHIL}	Input Fall Time		20	ns	From 2.0V to 0.8V

NOTE:
1. Timings defined for CKIO in input mode.

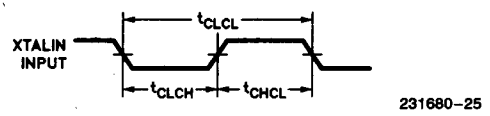


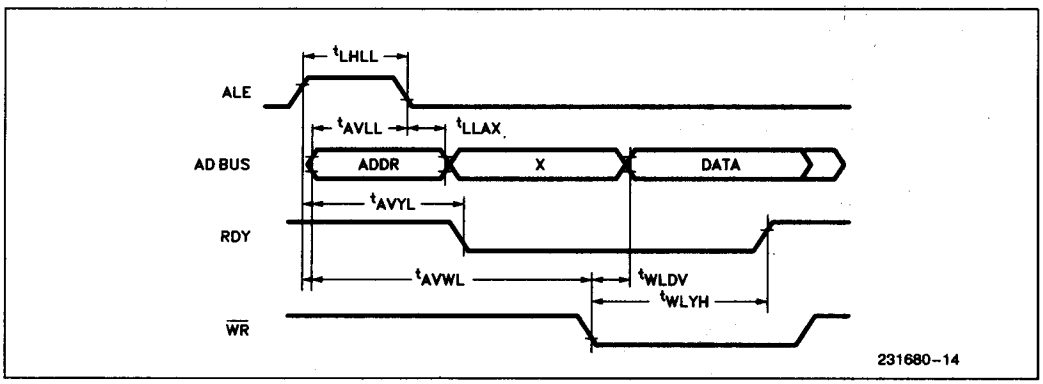
Diagram 1

BUS INTERFACE UNIT

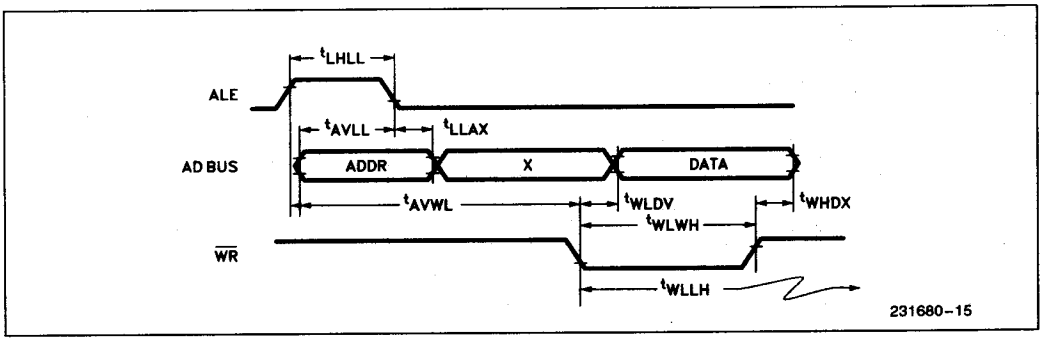
CPU WRITE CYCLE TIMINGS

Symbol	Parameter	Min	Max	Units	Note
t_{LHLL}	ALE Pulse Width	35		ns	
t_{AVLL}(1)	Address Set-Up Time	15		ns	
t_{LLAX}	Address Hold Time	20		ns	
t_{AVWL}	Address Valid or ALE HIGH (whichever is later) to $\overline{WR}$ LOW	75		ns	
t_{AVYL}	Address Valid or ALE HIGH (whichever is later) to RDY LOW		120	ns	
t_{WLDV}	Data Valid after $\overline{WR}$ LOW		$8t_{CLCL}$ −100	ns	
t_{WLYH}	$\overline{WR}$ LOW to RDY High		$14t_{CLCL}$ +100	ns	
t_{WLWH}	$\overline{WR}$ Pulse Width	$2t_{CLCL}$ +20		ns	
t_{WHDX}	Data Hold Time After $\overline{WR}$ High	20		ns	
t_{WLLH}	$\overline{WR}$ Low to ALE High of Next $\overline{RD}/\overline{WR}$ Cycle	$18t_{CLCL}$ +100		ns	

NOTE:
1. Chip select input, A16, has the same timing spec as the other address inputs.



CPU Write Cycle Using Ready to Generate WAIT States

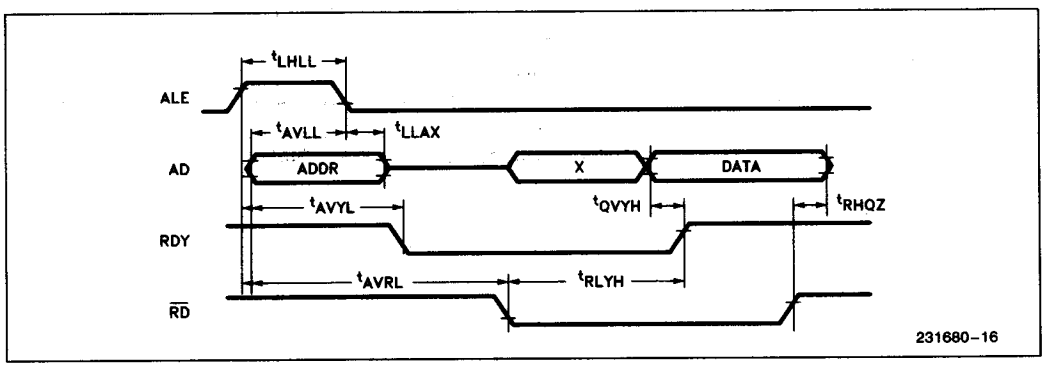


CPU Write Cycle Not Using Ready

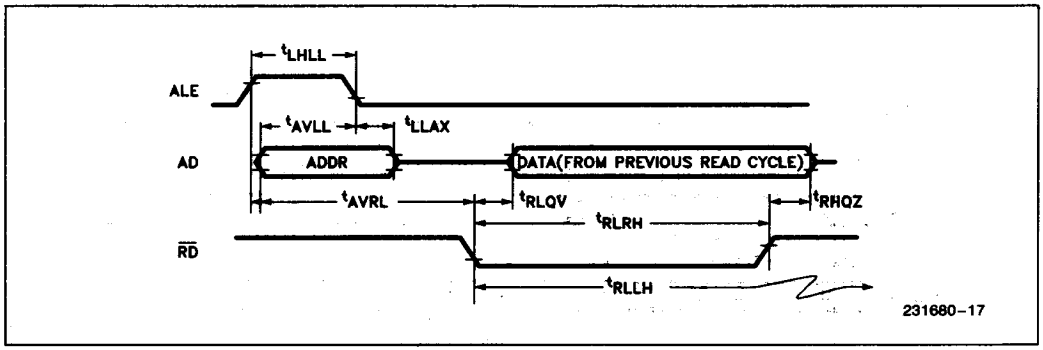
CPU READ CYCLE TIMINGS

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{RLYH}	$\overline{RD}$ LOW to RDY High		$19t_{CLCL}$ +100	ns	
t_{QVYH}	Data Valid to RDY High	0		ns	
t_{RHQZ}	Data Float Time after $\overline{RD}$	10	60	ns	(Note 1)
t_{RLQV}	$\overline{RD}$ LOW to Data Valid (PRE = 1)		75	ns	
t_{RLRH}	$\overline{RD}$ Pulse Width (PRE = 1)	$2t_{CLCL}$ +20		ns	
t_{RLLH}	$\overline{RD}$ LOW to ALE High of Next $\overline{RD}/\overline{WR}$ Cycle	$18t_{CLCL}$ +100		ns	
t_{AVRL}	Address Valid or ALE High (whichever is later) to $\overline{RD}$ LOW	75		ns	

NOTE:
1. I_{OL}, I_{OH} = 10 mA, C_L = 100 pF.



CPU Read Cycle Using Ready to Generate WAIT States (PRE = 0)



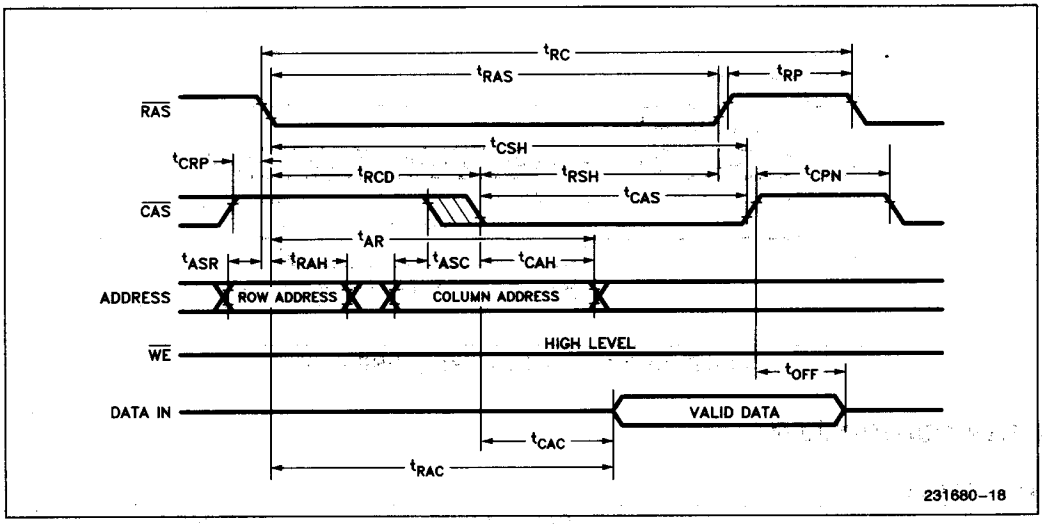
CPU Read Cycle Not Using Ready (PRE = 1)

DRAM CONTROLLER

READ CYCLE

Symbol	Parameter	SAB = 1		SAB = 0		Units
		Min	Max	Min	Max	
t_{RC}	Random Read Cycle Time	5 tclcl − 40		4 tclcl − 40		ns
t_{REF}	Refresh Time 128 Cycles 256 Cycles	 Note 1 Note 2		 Note 1 Note 2		ms
t_{RP}	$\overline{RAS}$ Precharge Time	2 tclcl − 20		2 tclcl − 20		ns
t_{CPN}	$\overline{CAS}$ Precharge Time (Non-Page Mode)	3 tclcl − 40		3 tclcl − 40		ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tclcl − 10		tclcl − 10		ns
t_{RSH}	$\overline{RAS}$ Hold Time	2 tclcl − 35		tclcl − 35		ns
t_{CSH}	$\overline{CAS}$ Hold Time	3 tclcl − 20		2 tclcl − 20		ns
t_{ASR}	Row Address Set-Up Time	5		5		ns
t_{RAH}	Row Address Hold Time	tchcl − 65		tchcl − 65		ns
t_{ASC}	Column Address Set-Up Time	5		5		ns
t_{CAH}	Column Address Hold Time	tclcl		tclcl		ns
t_{AR}	Column Address Hold to $\overline{RAS}$	3 tclcl + tchcl − 20		2 tclcl + tchcl − 20		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	3 tclcl − 30		2 tclcl − 30		ns
t_{CAS}	$\overline{CAS}$ Pulse Width	2 tclcl − 40		tclcl − 40		ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	2 tclcl − 50		2 tclcl − 50		ns
t_{CAC}	Access Time from $\overline{CAS}$		2 tclcl − 70		tclcl − 70	ns
t_{RAC}	Access Time from $\overline{RAS}$		3 tclcl − 45		2 tclcl − 45	ns
t_{OFF}	Data-In Hold Time	35		35		ns

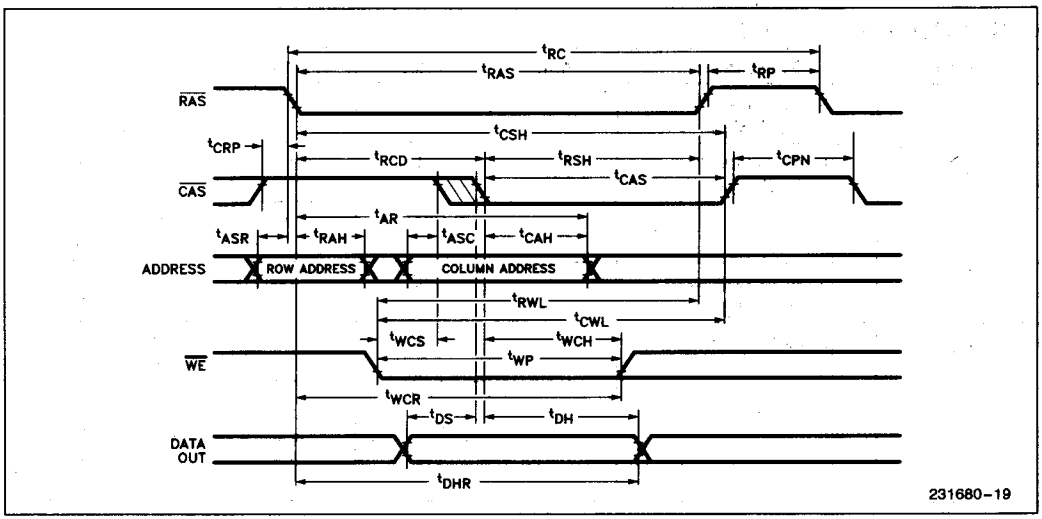
NOTES:
1. (128/(12 * scan line time)) + 10,000 tclcl
2. (256/(12 * scan line time)) + 10,000 tclcl



Read Cycle

WRITE CYCLE

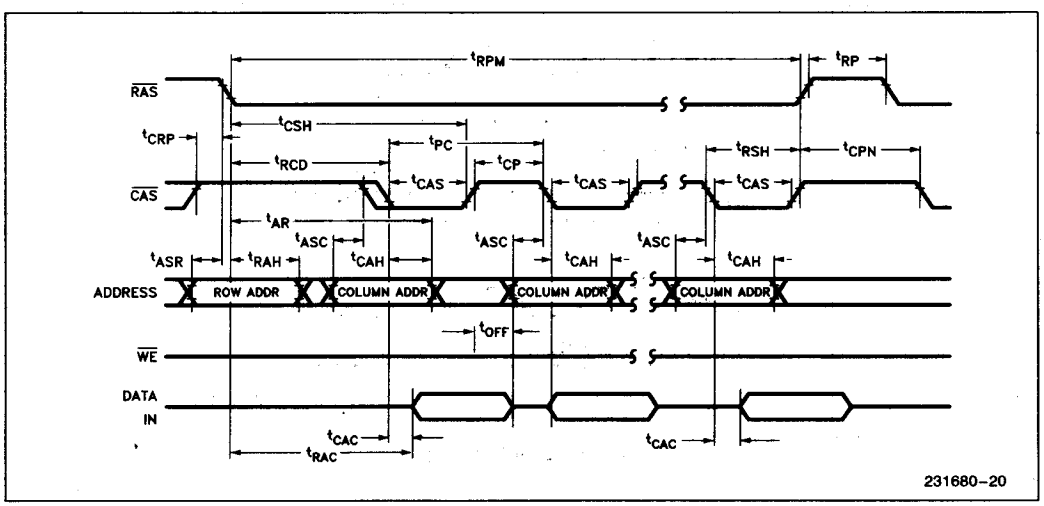
Symbol	Parameter	SAB = 1		SAB = 0		Units
		Min	Max	Min	Max	
t_{RC}	Random Write Cycle Time	5 tclcl − 40		4 tclcl − 40		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	3 tclcl − 30		2 tclcl − 30		ns
t_{CAS}	$\overline{CAS}$ Pulse Width	2 tclcl − 40		tclcl − 40		ns
t_{WP}	Write Command Pulse Width	3 tclcl − 20		2 tclcl − 20		ns
t_{WCS}	Write Command Set-Up Time	tclch − 10		tclch − 10		ns
t_{WCH}	Write Command Hold Time to $\overline{CAS}$	2 tclcl + tchcl − 40		tclcl + tchcl − 40		ns
t_{WCR}	Write Command Hold Time to $\overline{RAS}$	3 tclcl + tchcl − 40		2 tclcl + tchcl − 40		ns
t_{RWL}	Write to $\overline{RAS}$ Lead Time	2 tclcl + tclch −40		tclcl + tclch − 40		ns
t_{CWL}	Write to $\overline{CAS}$ Lead Time	2 tclcl + tclch − 50		tclcl + tclch − 50		ns
t_{DS}	Data-Out Set-Up Time	tclcl + tclch − 50		tclcl + tclch − 50		ns
t_{DH}	Data-Out Hold Time	2 tclcl + tchcl − 20		tclcl + tchcl − 20		ns
t_{DHR}	Data-Out Hold Time to $\overline{RAS}$	3 tclcl + tchcl − 20		2 tclcl + tchcl − 20		ns
t_R, t_F	Rise, Fall Time $\overline{RAS}$, $\overline{CAS}$	5	40	5	40	ns



Write Cycle

PAGE MODE

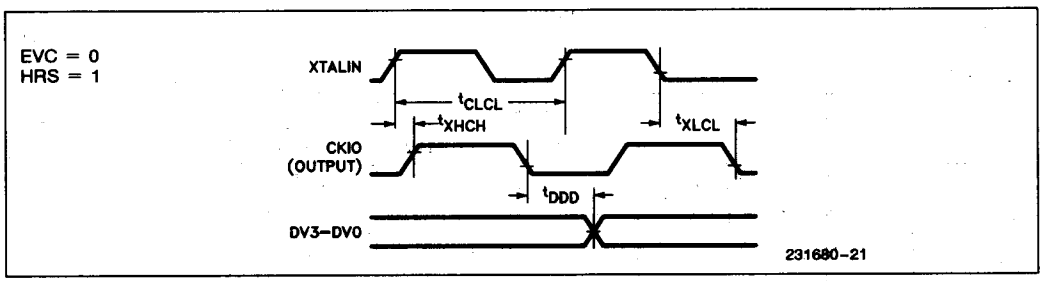
Symbol	Parameter	SAB = 1		SAB = 0		Units
		Min	Max	Min	Max	
t_{PC}	Page Mode Read Cycle	3 tclcl − 20		2 tclcl − 20		ns
t_{CP}	$\overline{CAS}$ Precharge Time	tclcl − 20		tclcl − 20		ns
t_{CAS}	$\overline{CAS}$ Pulse Width	2 tclcl − 40		tclcl − 40		ns
t_{RPM}	$\overline{RAS}$ Pulse Width	96 tclcl − 5		65 tclcl − 5		ns



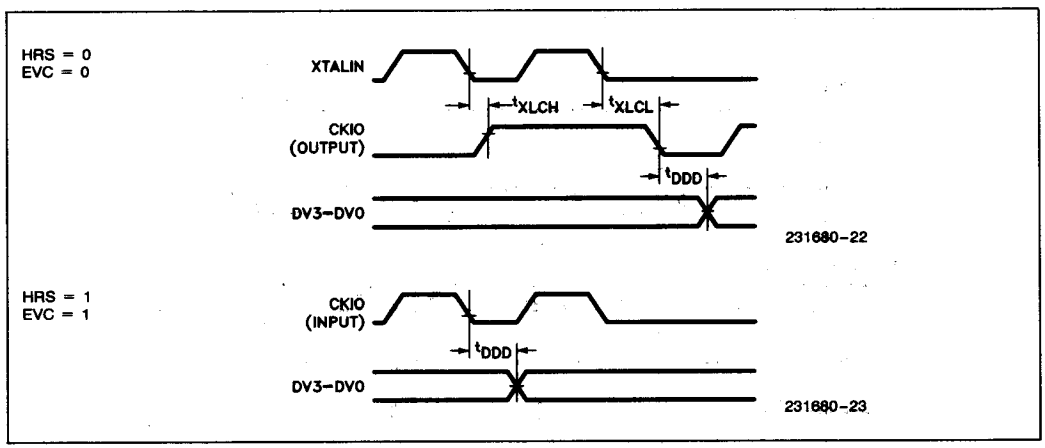
Page Mode Read Cycle

VIDEO OUTPUT TIMINGS

Symbol	Parameter	Min	Max	Units	Comments
tx_{HCH}	XTALIN High to CKIO High		60	ns	EVC = 0 HRS = 1
tx_{LCL}	XTALIN Low to CKIO Low		70	ns	EVC = 0 HRS = 1
			75	ns	EVC = 0 HRS = 0
tx_{LCH}	XTALIN Low to CKIO High		80	ns	EVC = 0 HRS = 0
tx_{DDD}	Digital Data Delay		30	ns	EVC = 0 HRS = 1
			35	ns	EVC = 0 HRS = 0
			70	ns	EVC = 1 HRS = 1



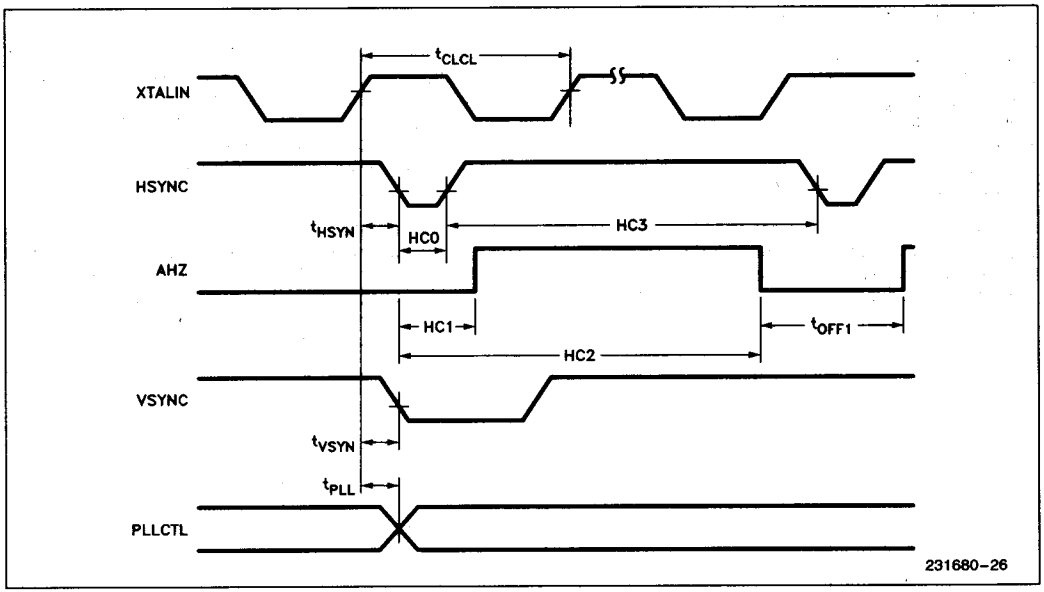
Video Output Timings



Video Output Timings

DAC SPEC

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{REF}	Reference Voltage		1.6	V	typ = 1.6V
$R_{V_{REF}}$	Source Impedance of V_{REF}		200	Ω	
	Linearity		½ LSB		V_{REF} = 1.6V ±5%
t_s	Settling Time		20	ns	Max Load = 10 pF
SYNC SPEC					
t_{HSYN}	HSYNC Delay from XTALIN		150	ns	
t_{VSYN}	VSYNC Delay from XTALIN		150	ns	
t_{OFF1}	Dead Zone between Two Active Horizontal Zones	120 tclcl		ns	
t_{PLL}	PLLCTL Valid Delay from HSYNC		100	ns	



Sync Specs

DATA SHEET REVISION REVIEW

The following lists key differences between this and the July 1986 (Order no. 231680-001) data sheet:

1. Test conditions for t_{RHQZ} (data float time after $\overline{RD}$) are clarified in Note 1. CPU Read Cycle Timings.
2. DRAM controller READ and WRITE cycle timings changed to reflect current testing.
3. Microprocessor and Memory Interface text modified to clarify RDY and REFRESH operations, respectively.