Electronics

INTEL'S ISSCC BOMBSHELL: A SUPERCOMPUTER ON A CHIP

The 80860 may revolutionize the way work stations are built

SAN JOSE, CALIF.

Intel Corp. has dropped a bomb on the work-station market: a reduced-instruction-set-computer chip that is no less than the silicon equivalent of a Cray 1 supercomputer. It could mean that designers laboring on the next generation of RISC work stations based on Sparc, MIPS, Clipper, or 88000 central-processing units are going to have to start over.

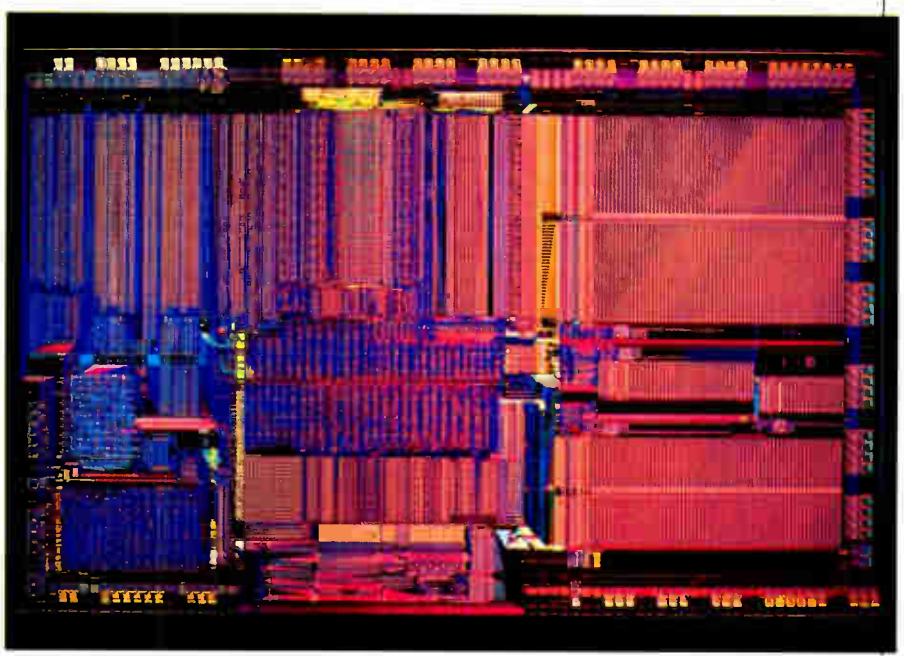
The reason: Intel's chip, the 80860, does right now what the others had hoped to do by year's end. It integrates integer processor, 64-bit floating-point unit, data and instruction caches, and memory-management unit on one chip. It then adds a powerful three-dimensional graphics processor to boot.

The 80860, up to now known as the N10, sets a new benchmark in supercomputer applications. Running at a 40-MHz clock speed, the chip delivers 33 million VAX instructions/s running the Stanford test suites, 10 million floating-point operations/s on the Linpack benchmark, 90,000 Dhrystones, and 500,000 4-by-4 vector transforms/s performing a graphics operation. In addition, it has been designed for multiprocessor operation, so the company has multiprocessor Unix development under way to support it. If all that weren't enough, Intel will start selling the 80860 before the year is up for $750 in 1,000-unit lots—a supercomputer on a chip at an affordable price.

The chip's commercial debut is bound to light a fire under developers of RISC-based systems, because the 80860 will permit them to build supercomputer work stations that will sell for less than $10,000. To help this effort along, Intel is providing a compiler in addition to starting the Unix development. Meanwhile, original-equipment manufacturers—IBM Corp. is probably among them—are already designing systems with the chip. Computer makers find the 80860 appealing because its individual processors—integer, floating-point, memory-management and cache, and graphics—can all compute simultaneously.

On the marketing side, shipments of RISC microprocessors in work stations have so far been far from breathtaking compared with those of complex-instruction-set chips such as Intel's 80386. Alice Leeper, senior analyst at Dataquest Inc., a market-research firm in San Jose, Calif., predicts that 600,000 RISC processors will sell this year, with the total growing to 6 million units in 1992. By contrast, she says, 8.3 million CISC processors will ship in 1989, growing to 26.3 million in 1992.

What is needed to narrow the gap is a high-performance, low-cost RISC chip that will spur work-station unit shipments, and that can be used in embedded-control applications. That's the 80860.



Intel's blockbuster 80860 is likely to goose the work-station market, because it will permit system houses to build $10,000 supercomputer desktop machines.

"With the floating-point and graphics capability, the chip is ideal for high-end 3-d graphics work stations," says Bill Rash, advanced 32-bit microprocessor-marketing manager at Intel in San Jose. "It's also ideal for high-end engineering work stations performing simulations for solids and fluids as well as electrical-circuits modeling, and board and chip layout."

In either case, the chip threatens to leave work-station marketplace competitors in the dust. Semiconductor vendors such as Intergraph, MIPS, Motorola, and those making Sparc CPUs have been making do with multiple-chip solutions using 32-bit-wide architectures. Work-station vendors using other chips will also be at a cost and size disadvantage compared with those using the 80860. "With this chip, a designer can build a Cray 1 supercomputer in a small-footprint desktop system for under $10,000," says Rash.

Rash cites the example of work-station manufacturers already offering diskless machines for less than $10,000 complete with high-resolution color graphics, a 1,000-by-1,000-pixel color monitor, and 8 Mbytes of random-access memory. "It's possible to build such a system with the 80860, which provides the graphics capability as well as the high-performance vector- and scalar-computing capability, and offer the system at the same price," he says.

The CPU cost with the 80860 will be considerably less than with the other RISC alternatives. A comparison made by Michael Slater, editor and publisher of the industry newsletter *Microprocessor*

Report, puts the single-unit cost of a minimum system using the Motorola Inc. three-chip 88000 RISC implementation at $1,732 with a 32-Kbyte cache. The Cypress Semiconductor Corp. implementation with six chips and a 64-Kbyte cache costs $2,500 in multiple quantities. And the MIPS Computer Systems Inc. implementation comes in at about $1,515 in multiple quantities, with 128 Kbytes of cache.

However, the 80860 does have one disadvantage: a smaller cache than any of the others, though it does come with the integral graphics-processing capability that the others do not offer.

While the cost of the chip makes a persuasive argument for designers to switch from other RISC chips, Slater does not believe other RISC suppliers are going to be too worried yet. "The saving grace for all of them is that they have their own next-generation processors in the works," he says, "and they all have been out there establishing relationships with software developers, starting to build a binary base of software, and selling the user community on adopting a new binary standard."

Intel has recognized the importance of providing software for the 80860. In introducing the chip in late February, the company announced a complete set of development tools including C and Fortran compilers and Fortran vectorizers. Intel also has an early prototype of a multiprocessing version of Unix on the 80860, now being upgraded to System V, Release 4.0.

"We were concerned about the number of designers willing to recompile applications to take advantage of the capability of the 80860," says Rash. "But the level of performance improvement the chip offers, in some cases a 50-times boost in floating-point capability, motivates software developers to recompile." However, software developers port software to work stations, not to chips. And in recent months, major work-station vendors have already chosen the chip they will use in their next-generation product.

Yu tuned the design to the chip process.

Kohn's team used supercomputer methods.

Digital Equipment Corp. is using the MIPS chip, Motorola has signed up a number of major OEMs for the 88000, and an impressive number of companies are building equipment around the Sparc architecture. So far no one has said it has enlisted the biggest OEM of all, IBM. But given Intel's close relationship with Big Blue on the 80386, which is used in IBM's Personal System/2, it's a safe bet that the giant computer maker has had a peek at the new chip—and IBM certainly can use it. Its work-station strategy with the IBM PC RT has been uninspiring at best, and the company is certainly looking to become a greater force.

Toward that end, IBM has licensed a set of tools from Next Inc. of Palo Alto, Calif. Coincidentally, the applications tool kit that Next developed is for a multiprocessor Unix operating system much like the one being developed by Intel and an independent group of companies for the 80860 chip.

But editor Slater thinks IBM has other plans for the 80860. "I think IBM is committed to the RT architecture and I would be surprised to see it change the

CPU in its RISC-based computer away from its own proprietary architecture," he says. "I could see IBM building a high-performance graphics subsystem using the [80860] as a graphics accelerator. That way IBM retains the main CPU but gets much higher graphics performance at the same time."

Slater believes that Intel's original intent was to bundle the upcoming 80486 with the 80860. "If the [80860] is used as only a graphics accelerator, it is easier to incorporate into a system," he points out. "A graphics kernel can be written for it and then applications software can take advantage of its performance without making the investment in applications-software development that would otherwise be required."

The chip comes with a RISC integer CPU, single- and double-precision pipelined vector floating-point processors (a separate adder and multiplier), 3-d graphics, 4-Kbyte instruction and 8-Kbyte data caches, and paged memory-management unit. It uses a 64-bit data and instruction bus to execute more operations per second. With such a wide data path, the computer can load a 32-bit integer and 32-bit floating-point instruction, which execute concurrently in a single clock cycle.

Moreover, because the unit has separate multiplier and adder, a multiply-and-accumulate operation can occur in a single clock cycle as well.

At one company that has seen the 80860, Stellar Computer Inc. of Newton, Mass., vice president Michael Sporer says the idea of fetching a 32-bit integer instruction and a 32-bit floating-point instruction at once "is a fundamentally good idea. We implement that in our machine and I see more and more people doing it."

It's a safe bet that IBM is one of the OEMs that has had a peek at the 80860

In addition, the graphics processor can operate on bytes of data, a powerful feature for handling color. In one instruction cycle, the unit can individually process the values to drive the red, green, and blue guns of a color monitor and still have a byte operation to spare. But raw processing power is useless unless processors can rapidly acquire data to feed these units.

The 80860 has a system of buses that could not be implemented easily on a printed-circuit board with discrete processor chips. "A 64-bit bus feeds instructions to both integer and floating-point processors," explains Intel's Rash. It transfers 320 Mbytes/s of data. Another bus running between the data cache and the floating-point unit is 128 bits wide and can move 640 Mbytes/s. The external bus to the DRAMs is 64 bits wide and can transfer data at 160 Mbytes/s. "Altogether about a gigabyte of data can flow around the chip at any one time," he says.

While the chip uses a split instruction and data bus internally, externally it uses a standard 64-bit-wide bus for connecting to standard DRAMs. The bus transfers a data item every other clock, but with interleaved banks of DRAMs, all three banks can access data at once.

In addition to wide buses, the chip comes with architectural features to improve performance of its various processors. Leslie Kohn, chief architect, says his team applied some of the techniques that were developed for supercomputers to handle large data structures that did not completely fit inside the cache. Large data structures require many random accesses to memory. In a system with three banks of memory, for example, a structure could span all three.

"We have special instructions for performing pipeline accesses of large data structures, called pipelined floating-point load, in which the data is brought directly into the floating-point hardware without going through the on-chip cache," Kohn explains. The pipeline floating-point load

instruction of a large data structure implies a one-time use of the data coming into the floating-point unit; so it is not desirable to flush the cache and load it with information that will only have to be flushed afterward anyway. This feature—preventing a cache flush and loading data directly from RAM at full speed by overlapping memory accesses from the three banks of memory—provides a factor-of-three speed increase.

Three-dimensional graphics capability was added after the initial chip-architecture definition. "We found that once we had developed the hardware to feed the floating-point unit sufficiently to keep it busy," says Kohn, "we could add another unit that required only 3% more silicon area, and could piggyback onto existing hardware to give us about a 10-times performance improvement in 3-d graphics."

Just how did Intel come up with this impressive chip? "In a design as complex as the 80860, there are a number of intricate relationships between circuit design, architecture, and the manufacturing process," says Albert Yu, vice president and general manager of the component technology and development group. "What we have that others do not is a design that is tuned to the semiconductor process, and we believe we are ahead in 1-μm CMOS process technology."

Also, other companies building RISC processors have either had to contract out some of the design or the fabrication

PROCESSORS REV UP AT THE ISSCC

Designers of microprocessors are like builders of drag-racing cars: they squeeze every ounce of power possible out of their finely tuned engines. And at this year's International Solid State Circuits Conference in New York, Intel Corp. of Santa Clara, Calif., took the checkered flag. Intel's vehicle was the 80860, a 40-MHz chip that packs more processing power per square micron than anything in its class this year (see p. 25).

But others were in the race with chips that, although not as loaded as the 80860, posted some impressive compute times as well. Among them was Hewlett-Packard Co.'s entry. The Palo Alto, Calif., firm offered a 32-bit VLSI central-processing unit rated at 30 million instructions/s that proves there's still life left in n-MOS. And Digital Equipment Corp. of Marlboro, Mass., showed off two reduced-instruction-set computing machines, one monster that can peak at 50 mips and another that can run 20 mips sustained.

Though Intel's 80860 is the winner, others also have pedal to the metal

Outside the ISSCC, Cypress Semiconductor Corp. has rolled out its Sparc-compatible RISC engine, redesigned by Roger Ross. Ross's redesign cut the chip count from nine to six. In addition, the San Jose, Calif., company intends to introduce this year a complete chip set able to run at 40 MHz, says Dane Elliot, director of applications engineering. It also hopes to have a 50-MHz part by next January that offers 36 mips of integer performance. A floating-point unit running at 50 MHz should give about 9 million floating-point operations/s of double-precision floating-point computational power. Finally, Cypress has a cache-controller/memory-management chip that is the first to bring multiprocessing to the Sparc architecture.

Then there are the complex-instruction-set CPUs, which promise to pack the magical million transistors under their lids, but will be slower rolling off the assembly line than expected. Michael Slater, who publishes the newsletter *Microprocessor Report*, says that Motorola Inc.'s 68040 and Intel's 80486 will be million-transistor chips, and that both will be out this year.

Slater says that the 68040 from Motorola will house a floating-point engine as well as a the memory-management unit. It will sport more pipelining, too, to boost performance by cutting the average number of clocks per instruction. Intel engineers, meanwhile, are making the same moves on their 80486.

Slater thinks that Intel will announce the 80846 in April; Intel confirms this. Motorola, however, will hold off until later in the year when it has a few circuits off the assembly line.

Nor were gleaming engines from Japan in short supply at the ISSCC, though they were aimed at floating-point rather than integer crunching.

A 64-bit chip from Matsushita Electric Industrial Co. of Osaka gets some of its extra horsepower by doubling the word size. The number cruncher can run a 64-bit floating-point add, subtract, and multiply operation every 50 ns and a divide operation every 350 ns. That converts to 20 megaflops of peak performance. Measuring 14.4 by 13.5 mm, the chip crams 440,000 transistors under its lid.

A 32-bit machine, this one from Mitsubishi Electric Corp. of Hyogo, achieves an astonishing 40 megaflops of peak performance. The key lies in the use of an elastic pipeline structure, which minimizes the effects of clock skew on pipeline performance. Fabricated using a 1.3-μm double-metal CMOS process, the chip holds a relatively modest 85,000 transistors in 13.3 by 12.6 mm. —*Jonah McLeod*

of their chips. By contrast, Intel does it all, and the 80860 was the result of a long-range view. To predict future-generation microprocessors, says Yu, one has only to look at developments in large-computer architectures. Then, as process technology allows greater integration, simply implement mainframe architectural features in silicon.

As Kohn and project manager Sai-Wai Fu began designing the chip in 1986, the Cray architecture was well known, but no one imagined it could be implemented on a chip. "With Intel's next-generation process technology, we recognized that we could build a million-transistor chip," says Kohn. "Without being constrained to be compatible with an existing chip architecture, we felt we could achieve significant improvements."

"Intel is good at taking risks when they think it is the right thing to do," Yu says. "When Les and Fu came up with the idea of the chip, it was not all that difficult to embark on the project." But it is one thing to propose an idea and another to produce chips three years later. "It takes a certain amount of faith and vision to believe that you can build a chip with 1 million transistors and that you're going to get good yields on it," Kohn says. "We had that and we were able to do it."

–Jonah McLeod, with additional reporting by Lawrence Curran

SEMICONDUCTORS

ISSCC CHIPS HERALD SWEEPING CHANGES IN SYSTEM DESIGN

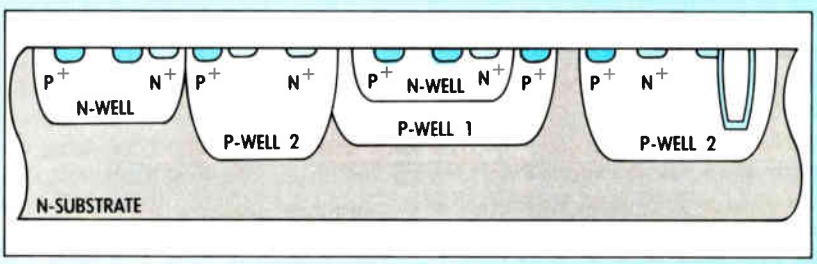
SAN JOSE, CALIF.

If last month's International Solid State Circuits Conference in New York can be said to have had a theme, it might be "Rethink Your Options, System Designers."

Across the board—in processors, dynamic and static random-access memories, nonvolatile memory, logic, and gate arrays—new circuit developments and combinations unveiled at the ISSCC promise to open possibilities for drastic changes in how systems are implemented. Not only are processor designers looking to 64-bit-wide architectures to boost system speed while facilitating the use of lower-cost main memory, but the density and speed of the memory devices that are emerging will show the way to system configurations never possible before.

Take DRAMs, for instance. Scarcely

HOW TOSHIBA GETS A 45-NS DRAM



Toshiba's 16-Mbit DRAM is designed around 64 subarrays, each 256 Kbits in size; a single chip could replace up to 16 commodity parts in a PC.