WORKSTATION GRAPHICS WITH A PC PRICE TAG

RISC-BASED CHIP SUPPORTING 8514/A AND VGA BRINGS A SIGNIFICANT DROP IN GRAPHICS-BOARD COSTS

BY SAMUEL WEBER

GRAPHICS

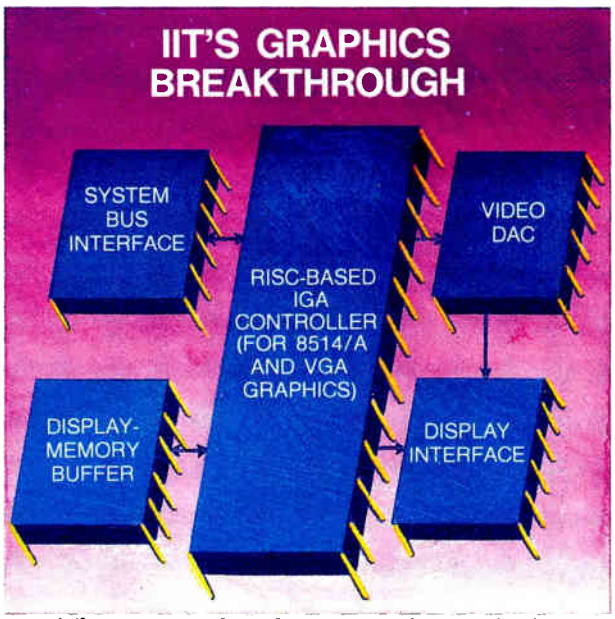
FOR THE FIRST TIME, A RISC engine has been applied to high-resolution personal computer graphics, and the result is a low-cost, high-performance graphics controller that implements all the popular IBM Corp. graphics modes, including the Personal System/2's 8514/A high-resolution standard. What's more, performance tests running under Microsoft Windows indicate that a high-resolution graphics board based on the new chip will run significantly faster than equivalent products offered by other vendors.

The new Integrated Graphics Array (IGA) from Integrated Information Technologies in Santa Clara, Calif., should find avid acceptance among original-equipment manufacturers and makers of add-in boards. Because the chip works with low-cost dynamic random-access memories instead of expensive video RAMs, board manufacturers have an easy upgrade path. The controller can be initially installed as VGA only, but by adding DRAMs, it can be upgraded easily to 8514/A.

Up to now, graphics boards that include 8514/A capability have been quite expensive, running more than $1,000. With the new low-cost IGA chip, the manufacturing cost of a 0.5-Mbyte board would be substantially less than that, says Y. W. Sing, IIT's vice president and cofounder. For the user, the chip will bring workstation-level graphics to the PC at modest cost.

"To provide a successful next-generation graphics solution in the PC market," says Sing, "you have to meet four criteria: you have to provide a high-performance graphics engine, you have to have 1,024-by-768-pixel resolution with 256 colors, it has to be low in cost, and you must be fully compatible with VGA. And we meet all four points in any card built with our chip."

It wasn't long ago that VGA—the Video Graphics Array standard—was the sine qua non for PC graphics, at



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640 by 480 pixels for standard VGA and 800 by 600 for so-called "Super VGA." But then came 8514/A, with its 1,024 by 768 pixels. With the advent of 8514/A support of such applications as Microsoft Windows, Presentation Manager, and AutoCAD, serious users find that VGA is lacking, Sing says.

But all those pixels don't come cheap: in April 1987, when 8514/A was introduced, an 8514/A card for the PS/2 and 512 Kbits of video RAM weighed in at $1,290, plus $1,560 for an 8514/A monitor. Although monitor prices have declined in the interim, 8514/A cards from several vendors, including IBM, still top the $1,000 mark.

Another approach to high-performance graphics is Texas Instruments Inc.'s TMS34010 and 34020 graphics controllers [*Electronics*, May 1990, p. 103]. But although fast, the TI approach, too, is relatively expensive. Vendors with 8514/A-compatible offerings include Chips & Technologies Inc. with its 82C480 single-chip device and Western Digital Corp. with a two-chip set, the PWGA1. Neither directly supports VGA.

The IIT chip, by contrast, supports VGA, CGA, MDA, EGA, and Hercules in addition to 8514/A—no easy task considering the standards' differing technical needs. In the pixel-oriented CGA, EGA, and VGA, the central processing unit on the PC motherboard directs the graphics board's frame-buffer logic on a pixel-by-pixel basis. But 8514/A directs the CPU to send high-level graphics commands to a graphics engine for drawing lines and rectangles, making bit-block transfers (Bitblts), scissoring and other graphics operations, and moving objects around on the screen.

Most graphics adapters capable of implementing both VGA and 8514/A require what amounts to two separate subsystems, one for each standard. Because most available software is designed to support the VGA modes, high-end PCs that implement 8514/A must still provide a VGA board. Thus most 8514/A boards provide some sort of VGA pass-through

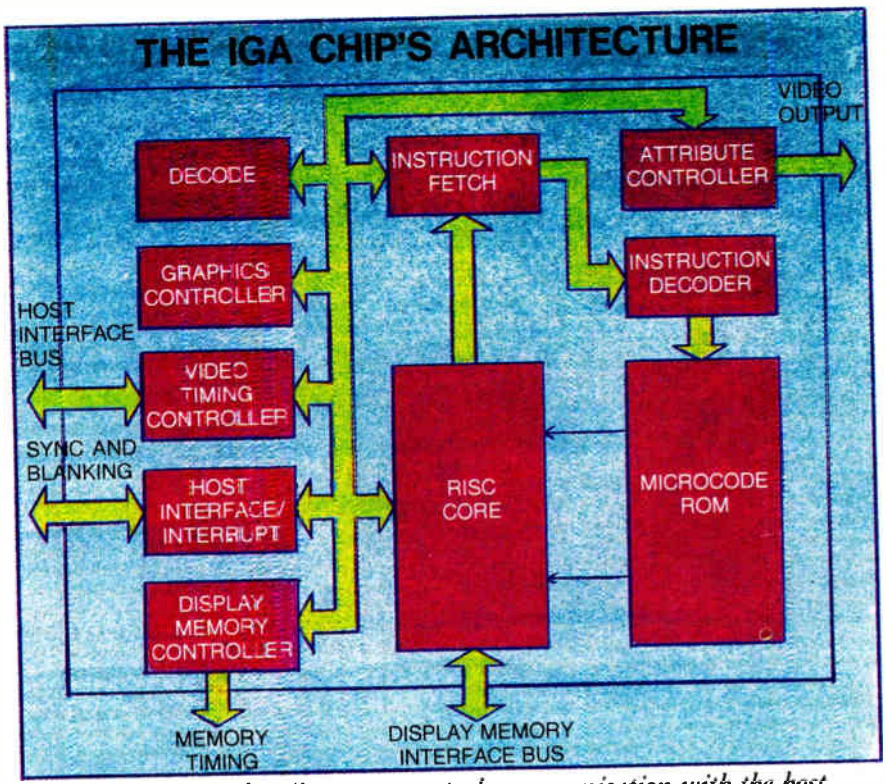
capability without full VGA functionality. To provide both means two processors, two frame buffers, two sets of TTL interface chips, two digital-to-analog converters—and concomitant high cost. But the IIT chip handles both standards with only one set of RAM buffers, video DACs, and TTL interface chips. The result is lower cost and reduced board area. In fact, it is possible to consider putting the IGA on the motherboard, since the chip will automatically switch to the appropriate mode.

IIT is a three-year-old company founded by Sing and Chi-Shin Wang, both formerly with Weitek Corp. of Sunnyvale, Calif. Its current sales level of $20 million is expected to quadruple this year, according to Sing. The company's first products were floating-point coprocessors compatible with Intel Corp.'s 287/387 but twice as fast. IIT's strategy, Sing says, is twofold: to provide a total solution for the PC motherboard and also to provide high-performance applications. Currently in the works are designs for a 386/486-compatible CPU [*Electronics*, May 1990, p. 78] and an image compression/decompression chip for multimedia, both targeted for next year.

Essentially, what IIT designers have done with the IGA is to combine two diverse architectures on a single chip. According to Sing, the VGA architecture has five basic components: a bus interface unit that talks to the AT or MicroChannel bus; a CRT controller that controls all the cathode-ray-tube signals; what IBM calls a sequencer, which generates all the internal signal timing and controls the frame-buffer video-RAM timing; a graphics controller that handles all the graphics data; and an attribute controller that handles text and screen manipulation.

The 8514/A architecture is less well-defined, says Sing, but basically it partitions into four components: bus interface unit, CRT controller, timing generator for the frame buffer, and graphics engine. "To put the two together," Sing says, "you have to share a lot of the logic. Right now we share the logic of the bus unit, the CRT controller, and the DRAM controller. That's how we are able to put all this on a single chip."

To accomplish this feat means mastering three tasks, adds Gene Parrott, vice president of sales and marketing. "First you need to design a RISC machine that will solve the problems of both diverse architectures. The VGA part is a pixel painter, and the 8514/A is a graphics engine—two very dissimilar animals—and you need to have full knowledge of the register-level architectures of both of them." Next, says Parrott, "your RISC engine must be designed to share a lot of the functions between those two parts." And finally, "implementation must be by a full custom design—not a gate array. There are just too many gates."



The host interface/interrupt controls communication with the host interface bus and passes data to all the other units on the board.

IIT IS THE ONLY VENDOR to use a reduced-instruction-set type of graphics engine; most solutions now available rely on state machines. But "a state machine is fixed, designed for a specific application, and can't be changed," Sing says. "Our design is much more flexible because changing the microcode can change the function or features."

The IGA is a 1.2-μm, custom-designed CMOS VLSI chip with a RISC processor running at 25 million instructions/s. This single chip is the equivalent of the three large gate arrays used by IBM and other vendors as a hard-wired graphics engine.

The RISC engine takes commands from the CPU, decodes and executes them. The drawing engine provides the hardware support for all major graphic functions—line draw, Bitblts, rectangle and polygon fill, patterns, vector fonts, and so on. The display processor configures itself using the control registers, reads video memory, and outputs an image to the screen. It also provides all the hardware necessary to emulate VGA, EGA, CGA, Hercules, and MDA.

The CPU sends drawing instructions to the graphics controller via the host bus interface. The graphics controller performs drawing computations and sends the pixel coordinates to the display-memory interface bus.

The decode function interprets instructions sent by the system CPU. The attribute controller receives data from the display memory via the graphics controller and the RISC core, then formats it for display. The instruction-fetch section maintains the flow of instructions from the CPU to the IGA. The instruction decoder provides primary-level decoding of the instructions fetched from the CPU, which in turn drive the microcode ROM.

The latter provides a second level of instruction decoding that produces the microinstructions needed to drive the RISC core computer. The display-memory controller generates basic timing for the display-memory RAMs while the video timing controller generates horizontal and vertical synchronous timing and refresh addressing.