CyberPro2010

Software Programmer's Guide to Register Definitions

"The Internet Multimedia Company!"

Revision 1.1E

NOTICE

This *Software Programmer's Guide to Register Definitions* is intended to be utilized with the materials contained in the *CyberPro2010 Software Developer's Kit* (SDK). Contact your IGS representative or contact the IGS home office for an SDK.

CyberPro2010

Software Programmer's Guide to Register Definitions

August, 1997

Printed in the United States of America

IGS Technologies, Inc.
4001 Burton Drive
Santa Clara, CA 95054
Phone (408) 982-8588
FAX (408) 982-8591
http://www.igst.com

Table of Contents

Table of Contents

Table of Contents

Table of Contents

Table of Contents

Table of Contents

Table of Contents

Table of Contents

THIS PAGE IS INTENTIONALLY LEFT BLANK

1 IGA Register Definitions

Name	Port	Index	Type	Reset; Remarks
CRTC Index	3?4	—	R/W	
CRT Shadow Control	3?5	1F	R/W	YES; CRT
Graphics Latched Data Readback n	3?5	22	RO	NO; CRT TO GC
Attribute Toggle Readback	3?5	24	RO	NO; CRT TO AC
Attribute Index Readback	3?5	26	RO	NO; CRT TO AC

Name	Port	Index	Type	Reset; Remarks
TV First Skip Line Address Low	3?5	40	R/W	
TV First Skip Line Address High	3?5	41	R/W	
TV Address Overflow	3?5	42	R/W	
TV Line Fetch Counter	3?5	43	R/W	
TV Max And Skip Lines	3?5	44	R/W	
TV Interpolation Miscellaneous Control	3?5	45	R/W	
TV Skip Delta Lines Address Low	3?5	46	R/W	
TV Skip Delta Lines Address High	3?5	47	R/W	

Name	Port	Index	Type	Reset; Remarks
Graphics Index	3CE	—	R/W	
Extended (EXT) Start Address	3CF	10	R/W	YES; CRT
EXT CRT Vertical Overflow	3CF	11	R/W	YES
EXT CRT IRQ Control	3CF	12	R/W	YES
EXT CRT Testing - Internal Test Only	3CF	13	R/W	YES
EXT Number Of Fetch 0	3CF	14	R/W	YES
EXT Number Of Fetch 1	3CF	15	R/W	YES
EXT HSYNC/VSYNC Control	3CF	16	R/W	YES
EXT CRT Vertical Counter 0	3CF	18	RO	
EXT CRT Vertical Counter 1	3CF	19	RO	

Name	Port	Index	Type	Reset; Remarks
EXT Bus Control	3CF	30	R/W	YES; BIU
EXT Segment Write Pointer	3CF	31	R/W	YES; BIU
EXT Segment Read Pointer	3CF	32	R/W	YES; BIU
EXT BIU Miscellaneous Control	3CF	33	R/W	YES; BIU
EXT Linear Address	3CF	35	R/W	YES; BIU
Function Control	3CF	3C	R/W	YES; BIU
PCI Bus Master Control	3CF	3E	R/W	YES; BIU
Big Endian Control	3CF	3F	R/W	YES; BIU
Bus Master Program Big Endian Swap	3CF	X3E	R/W	YES; BIU

Name	Port	Index	Type	Remarks
EXT V2 Video Memory Starting Address Low	3CF	X40	R/W	
EXT V2 Video Memory Starting Address Middle	3CF	X41	R/W	
EXT V2 Video Memory Starting Address High	3CF	X42	R/W	
EXT V2 Video Source Map Width Low	3CF	X43	R/W	
EXT V2 Video Source Map Width High	3CF	X44	R/W	
EXT V2 Video Display Horizontal Starting Pixel Low	3CF	X45	R/W	
EXT V2 Video Display Horizontal Starting Pixel High	3CF	X46	R/W	
EXT V2 Video Display Horizontal Ending Pixel Low	3CF	X47	R/W	
EXT V2 Video Display Horizontal Ending Pixel High	3CF	X48	R/W	
EXT V2 Video Display Vertical Starting Line Low	3CF	X49	R/W	
EXT V2 Video Display Vertical Starting Line High	3CF	X4A	R/W	
EXT V2 Video Display Vertical Ending Line Low	3CF	X4B	R/W	
EXT V2 Video Display Vertical Ending Line High	3CF	X4C	R/W	
EXT V2 Video Display Memory Offset Phase	3CF	X4D	R/W	
EXT Double Buffer Starting Address A Low	3CF	Y41	R/W	
EXT Double Buffer Starting Address A Middle	3CF	Y42	R/W	
EXT V2 Video Horizontal DDA Increment Value Low	3CF	Y43	R/W	
EXT V2 Video Horizontal DDA Increment Value High	3CF	Y44	R/W	
EXT Double Buffer Starting Address B Low	3CF	Y45	R/W	
EXT Double Buffer Starting Address B Middle	3CF	Y46	R/W	
EXT V2 Video Vertical DDA Increment Value Low	3CF	Y47	R/W	
EXT V2 Video Vertical DDA Increment Value High	3CF	Y48	R/W	

Name	Port	Index	Type	Remarks
EXT V2 Video FIFO Low Control	3CF	Y49	R/W	
EXT V2 Video FIFO High Control	3CF	Y4A	R/W	
EXT V2 Video Format Control	3CF	Y4B	R/W	
EXT V2 Video Display Control I	3CF	Y4C	R/W	
EXT V2 Video FIFO Control I	3CF	Y4D	R/W	
EXT V2 Video Miscellaneous Control I	3CF	Y4E	R/W	
EXT Steeling Cycle D	3CF	Y4F	R/W	
EXT X2 Video Memory Starting Address Low	3CF	J40	R/W	
EXT X2 Video Memory Starting Address Middle	3CF	J41	R/W	
EXT X2 Video Memory Starting Address High	3CF	J42	R/W	
EXT X2 Video Source Map Width	3CF	J43	R/W	
EXT X2 Video Memory SRC Map & SRC Window Width High	3CF	J44	R/W	
EXT X2 Video Display Horizontal Pipe Starting Pixel Low	3CF	J45	R/W	
EXT X2 Video Display Horizontal Pipe Starting Pixel High	3CF	J46	R/W	
EXT X2 Video Display Horizontal Starting Pixel Low	3CF	J47	R/W	
EXT X2 Video Display Horizontal Starting Pixel High	3CF	J48	R/W	
EXT X2 Video Display Horizontal Ending Pixel Low	3CF	J49	R/W	
EXT X2 Video Display Horizontal Ending Pixel High	3CF	J4A	R/W	
EXT X2 Video Display Vertical Starting Line Low	3CF	J4B	R/W	
EXT X2 Video Display Vertical Starting Line High	3CF	J4C	R/W	
EXT X2 Video Display Vertical Ending Line Low	3CF	J4D	R/W	
EXT X2 Video Display Vertical Ending Line High	3CF	J4E	R/W	
EXT X2 Video Source Window Width	3CF	J4F	R/W	
EXT X2 Video Horizontal DDA Initial Value Low	3CF	K40	R/W	
EXT X2 Video Horizontal DDA Initial Value High	3CF	K41	R/W	
EXT X2 Video Horizontal DDA Increment Value Low	3CF	K42	R/W	
EXT X2 Video Horizontal DDA Increment Value High	3CF	K43	R/W	
EXT X2 Video Vertical DDA Initial Value Low	3CF	K44	R/W	
EXT X2 Video Vertical DDA Initial Value High	3CF	K45	R/W	
EXT X2 Video Vertical DDA Increment Value Low	3CF	K46	R/W	
EXT X2 Video Vertical DDA Increment Value High	3CF	K47	R/W	
EXT X2 Video Format Control	3CF	K48	R/W	
EXT X2 Video display Control I	3CF	K49	R/W	
EXT X2 Window Double Buffer Address Low	3CF	K4A	R/W	
EXT X2 Window Double Buffer Address Middle.	3CF	K4B	R/W	
EXT X2 Window Double Buffer Address High	3CF	K4C	R/W	
EXT X2 Window Control I	3CF	K4D	R/W	

Name	Port	Index	Type	Reset; Remarks
SPRITE HORIZONTAL START LO	3CF	50	R/W	NO; AC
SPRITE HORIZONTAL START HI	3CF	51	R/W	NO; AC
SPRITE HORIZONTAL PRESET	3CF	52	R/W	NO; AC
SPRITE VERTICAL START LO	3CF	53	R/W	NO; AC
SPRITE VERTICAL START HI	3CF	54	R/W	NO; AC
SPRITE VERTICAL PRESET	3CF	55	R/W	NO; AC
SPRITE CONTROL	3CF	56	R/W	YES; AC
EXT Attribute Control	3CF	57	R/W	YES; AC
EXT Overscan Red	3CF	58	R/W	YES; AC
EXT Overscan Green	3CF	59	R/W	YES; AC
EXT Overscan Blue	3CF	5A	R/W	YES; AC
EXT COP Back Door	3CF	5B	R/W	; COP
EXT RAMDAC	3CF	5C	R/W	YES; Reserved

Name	Port	Index	Type	Remarks
EXT Capture Horizontal Starting Low	3CF	60	R/W	
EXT Capture Horizontal Starting High	3CF	61	R/W	
EXT Capture Horizontal Ending Low	3CF	62	R/W	
EXT Capture Horizontal Ending High	3CF	63	R/W	
EXT Capture Vertical Starting Low	3CF	64	R/W	
EXT Capture Vertical Starting High	3CF	65	R/W	
EXT Capture Vertical Ending Low	3CF	66	R/W	
EXT Capture Vertical Ending High	3CF	67	R/W	
EXT Capture Horizontal DDA Initial Value Low	3CF	68	R/W	
EXT Capture Horizontal DDA Initial Value High	3CF	69	R/W	
EXT Capture Horizontal DDA Increment Value Low	3CF	6A	R/W	
EXT Capture Horizontal DDA Increment Value High	3CF	6B	R/W	
EXT Capture Vertical DDA Initial Value Low	3CF	6C	R/W	
EXT Capture Vertical DDA Initial Value High	3CF	6D	R/W	
EXT Capture Vertical DDA Increment Value Low	3CF	6E	R/W	
EXT Capture Vertical DDA Increment Value High	3CF	6F	R/W	

Name	Port	Index	Type	Remarks
EXT Memory Controller 0	3CF	70	R/W	YES; SEQ
EXT Memory Controller 1	3CF	71	R/W	YES; SEQ
EXT Memory Controller 2	3CF	72	R/W	YES; SEQ
EXT Hidden Control 1	3CF	73	R/W	YES; SEQ
EXT FIFO Control 0	3CF	74	R/W	YES; SEQ
EXT FIFO Control 1	3CF	75	R/W	YES; SEQ
EXT SEQ Miscellaneous	3CF	77	R/W	YES; SEQ
EXT Hidden Control 3	3CF	79	R/W	YES; SEQ
EXT Hidden Control 4	3CF	7A	R/W	YES; SEQ
EXT Scratch Control	3CF	7B	R/W	YES; SEQ
Sprite Data Location Low	3CF	7E	R/W	YES; SEQ
Sprite Data Location High	3CF	7F	R/W	YES; SEQ

Name	Port	Index	Type	Remarks
EXT Capture PIP Horizontal Starting Low	3CF	80	R/W	
EXT Capture PIP Horizontal Starting High	3CF	81	R/W	
EXT Capture PIP Horizontal Ending Low	3CF	82	R/W	
EXT Capture PIP Horizontal Ending High	3CF	83	R/W	
EXT Capture PIP Vertical Starting Low	3CF	84	R/W	
EXT Capture PIP Vertical Starting High	3CF	85	R/W	
EXT Capture PIP Vertical Ending Low	3CF	86	R/W	
EXT Capture PIP Vertical Ending High	3CF	87	R/W	
EXT Capture New Control I	3CF	88	R/W	
EXT Capture New Control II	3CF	89	R/W	
EXT Video Chroma Compare Red High	3CF	8A	R/W	
EXT Video Chroma Compare Red Low	3CF	8B	R/W	
EXT Video Chroma Compare Green High	3CF	8C	R/W	
EXT Video Chroma Compare Green Low	3CF	8D	R/W	
EXT Video Chroma Compare Blue High	3CF	8E	R/W	
EXT Video Chroma Compare Blue Low	3CF	8F	R/W	

Name	Port	Index	Type	Remarks
EXT Graphics Control	3CF	90	R/W	YES; GC
EXT Chip ID 0 (data=A1)	3CF	91	R/W	YES; GC
EXT Chip ID 1 (data=03)	3CF	92	R/W	YES; GC
EXT Chip ID 2 (data=00)	3CF	93	R/W	YES; GC
EXT Scratch 0	3CF	94	R/W	YES; GC
EXT Scratch 1	3CF	95	R/W	YES; GC
EXT Scratch 2	3CF	96	R/W	YES; GC
EXT Scratch 3	3CF	97	R/W	YES; GC
PCI Bus Master Control 0	3CF	9C	R/W	YES; GC
PCI Bus Master Control 1	3CF	9D	R/W	YES; GC
EXT Write FIFO Miscellaneous	3CF	9E	R/W	YES; GC

Name	Port	Index	Type	Remarks
EXT CCIR656 Capture Mode I	3CF	A4	R/W	
EXT CCIR656 Capture Mode II	3CF	A5	R/W	
EXT Video Bus Master I	3CF	A6	R/W	
EXT Video Bus Master Address High	3CF	A9	R/W	
EXT Double Buffer Control I	3CF	AC	R/W	
EXT Double Buffer Starting Address AB High	3CF	AD	R/W	
EXT TV Control	3CF	AE	R/W	
EXT Test Control	3CF	AF	R/W	

Name	Port	Index	Type	Remarks
EXT VCLK Parameter 0	3CF	B0	R/W	DEFAULT ;VCG
EXT VCLK Parameter 1	3CF	B1	R/W	DEFAULT ;VCG
EXT MCLK Numerator 0	3CF	B2	R/W	DEFAULT ;VCG
EXT MCLK Numerator 1	3CF	B3	R/W	DEFAULT ;VCG
EXT Jumper Latch 0	3CF	B4	R/W	LATCH ;VCG
EXT Jumper Latch 1	3CF	B5	R/W	LATCH ;VCG
EXT Jumper Latch 2	3CF	B6	R/W	LATCH ;VCG
EXT Feature Connector	3CF	B7	R/W	DEFAULT ;VCG
EXT Jumper Latch 3	3CF	B8	R/W	LATCH ;VCG
EXT MISC CLK	3CF	B9	R/W	LATCH ;VCG
EXT VCLK Parameter 2	3CF	BA	R/W	DEFAULT ;VCG
EXT MCLK Numerator 2	3CF	BB	R/W	DEFAULT ;VCG
EXT VCLK Control	3CF	BC	R/W	;VCG
EXT MCLK Control	3CF	BD	R/W	;VCG
EXT XT Control	3CF	BE	R/W	;VCG
EXT XB Control	3CF	BF	R/W	;VCG

Name	Port	Index	Type	Remarks
EXT Programmable Bit 0	3CF	XB0	R/W	;VCG
EXT Programmable Bit 1	3CF	XB1	R/W	;VCG
EXT Programmable Bit 2	3CF	XB2	R/W	;VCG
EXT Video Memory Starting Address Low	3CF	C0	R/W	
EXT Video Memory Starting Address Middle	3CF	C1	R/W	
EXT Video Memory Starting Address High	3CF	C2	R/W	
EXT Video Memory Fetch Pitch Low	3CF	C3	R/W	
EXT Video Memory Fetch Pitch High	3CF	C4	R/W	(64-bit)
EXT Video Display Horizontal Starting Pixel Low	3CF	C5	R/W	
EXT Video Display Horizontal Starting Pixel High	3CF	C6	R/W	
EXT Video Display Horizontal Ending Pixel Low	3CF	C7	R/W	
EXT Video Display Horizontal Ending Pixel High	3CF	C8	R/W	
EXT Video Display Vertical Starting Line Low	3CF	C9	R/W	
EXT Video Display Vertical Starting Line High	3CF	CA	R/W	
EXT Video Display Vertical Ending Line Low	3CF	CB	R/W	
EXT Video Display Vertical Ending Line High	3CF	CC	R/W	
EXT Video Display Memory Offset Phase	3CF	CD	R/W	
EXT Video Color Compare Red	3CF	CE	R/W	
EXT Video Color Compare Green	3CF	CF	R/W	
EXT Video Color Compare Blue	3CF	D0	R/W	
EXT Video Horizontal DDA Initial Value Low	3CF	D1	R/W	
EXT Video Horizontal DDA Initial Value High	3CF	D2	R/W	
EXT Video Horizontal DDA Increment Value Low	3CF	D3	R/W	
EXT Video Horizontal DDA Increment Value High	3CF	D4	R/W	
EXT Video Vertical DDA Initial Value Low	3CF	D5	R/W	
EXT Video Vertical DDA Initial Value High	3CF	D6	R/W	
EXT Video Vertical DDA Increment Value Low	3CF	D7	R/W	
EXT Video Vertical DDA Increment Value High	3CF	D8	R/W	
EXT Video FIFO Low Control	3CF	D9	R/W	
EXT Video FIFO High Control	3CF	DA	R/W	
EXT Video Format Control	3CF	DB	R/W	
EXT Video display Control I	3CF	DC	R/W	
EXT Video FIFO Control I	3CF	DD	R/W	
EXT Video Miscellaneous Control I	3CF	DE	R/W	
EXT Video ROM Test Address	3CF	DF	R/W	

Name	Port	Index	Type	Remarks
EXT Video ROM VCR4R Low	3CF	E0	R	
EXT Video ROM VCR4R High	3CF	E1	R	
EXT Video ROM VCR4G Low	3CF	E2	R	
EXT Video ROM VCR4G High	3CF	E3	R	
EXT Video ROM UCB4G Low	3CF	E4	R	
EXT Video ROM UCB4G High	3CF	E5	R	
EXT Video ROM UCB4B Low	3CF	E6	R	
EXT Video ROM UCB4B High	3CF	E7	R	
EXT VFAC Control And Capture Mode I	3CF	E8	R/W	
EXT VFAC Control And Capture Mode II	3CF	E9	R/W	
EXT VFAC Control And Capture Mode III	3CF	EA	R/W	
EXT Capture Memory Starting Address Low	3CF	EB	R/W	
EXT Capture Memory Starting Address Middle	3CF	EC	R/W	
EXT Capture Memory Starting Address High	3CF	ED	R/W	
EXT Capture Memory Fetch Pitch Low	3CF	EE	R/W	
EXT Capture Control Miscellaneous	3CF	EF	R/W	

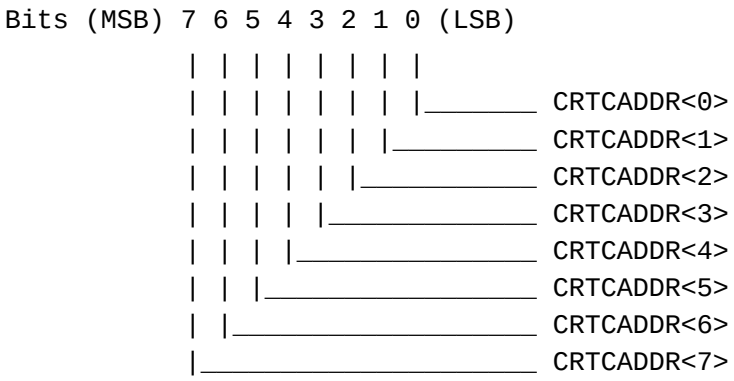
Name	Port	Index	Type	Remarks
EXT MISC0	3CF	F0	R/W	
EXT MISC1	3CF	F1	R/W	
EXT MISC2	3CF	F2	R/W	
EXT MISC3	3CF	F3	R/W	
EXT MISC4	3CF	F4	R/W	
EXT VUMA Configuration	3CF	F5	R/W	
EXT VUMA Extended Address	3CF	F6	R/W	
EXT VUMA Arbitration Value	3CF	F7	R/W	
EXT EDO Memory	3CF	F8	R/W	
EXT Video Planar Mode	3CF	F9	R/W	
EXT Indirect Index For 4X	3CF	FA	R/W	
Not Used	3CF	FB	R/W	
EXT YUV Value Offset Low	3CF	FC	R/W	
EXT YUV Value Offset High	3CF	FD	R/W	

NOTE: The port addresses are (03B4 and 03CF) or (03D4 and 03CF). This decision is controlled by Bit 0 of the register located at port 03C2H. A logical 1 selects 03D4 and 03CF; a logical 0 selects 03B4 and 03CF.

2 CRT Controller Register Definitions

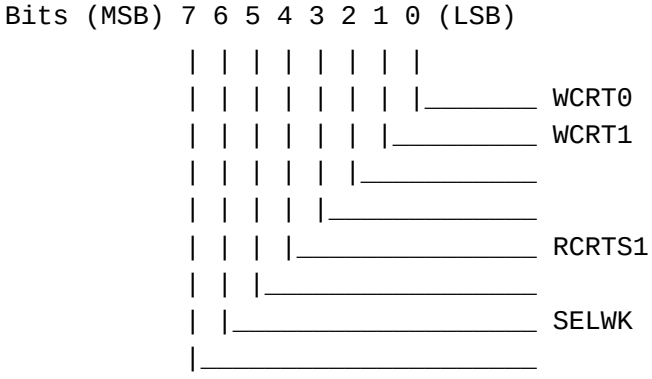
Note: In the bit maps displayed in this section, bits that are read during power-up and reset, but have another designation during operation, are listed adjacent to the operational bit name with the power-up/reset designation name inside parentheses, preceded by an asterisk: BIOS64K (*MOD27).

2.1 CRTC Index (3?4, R/W)



CRTCADDR(7:0): These six bits determine the index of the register pointed to in the next register R/W operation.

2.2 CRT Shadow Control (3?5/1F, R/W)



WCRT0: Write CRT Set 0: When this bit is 1, the standard VGA CRT registers is allowed to be updated. This bit defaults to logic 1 at power-up.

WCRT1: Write CRT Set 1: When this bit is 1, the extended CRT register set is allowed to be updated. This bit defaults to logic 0 at power-up. When this bit is 0, the standard VGA CRT register is allowed to be read.

RCRTS1: Read CRT Set 1: When this bit is 1, the extended CRT register set is allowed to be read. When this bit is 0, the standard VGA CRT registers are allowed to be read. This bit defaults to logic 0.

SELWK: Select Working (Refer to Figure 2-1): When this bit is 1, the extended CRT register set is operated as the CRT controller. When this bit is 0, the standard CRT register set is operated as the CRT controller. This bit defaults to logic 0.

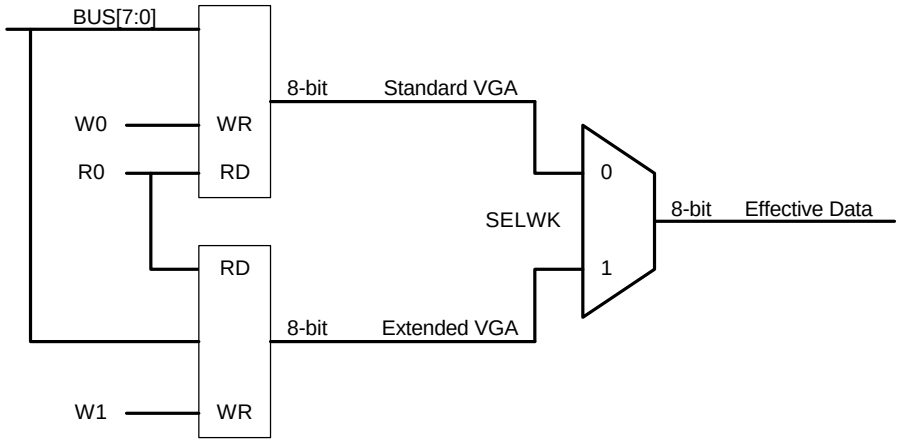


Figure 2-1: SELWK Logic Diagram

2.3 Graphics Latched Data Readback n (3?5/22, RO)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ LATCHD0
           | | | | | | |_________ LATCHD1
           | | | | | |___________ LATCHD2
           | | | | |_____________ LATCHD3
           | | | |_______________ LATCHD4
           | | |_________________ LATCHD5
           | |___________________ LATCHD6
           |_____________________ LATCHD7
```

This register is used to readback one of the four Graphics Controller Latched Data. The latch data is selected from the Standard Graphics Controller Register 4, bits[1:0].

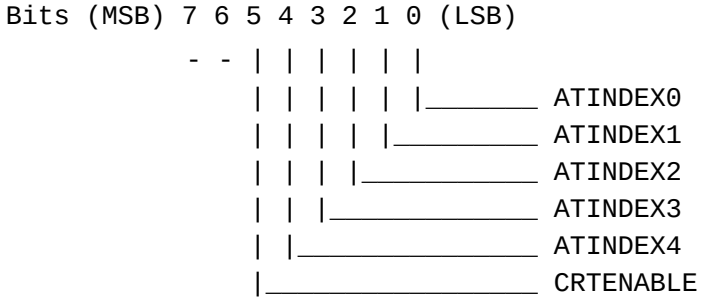
2.4 Attribute Toggle Readback (3?5/24, RO)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | - - - - - - -
           |_____________________ ATOGGLE
```

ATGGLE: Attribute Toggle Bit: When this bit reads back zero, then the Attribute Controller will read or write an index value on the next access. If this bit read back is logic 1, then the Attribute Controller will read or write an data value on the next access.

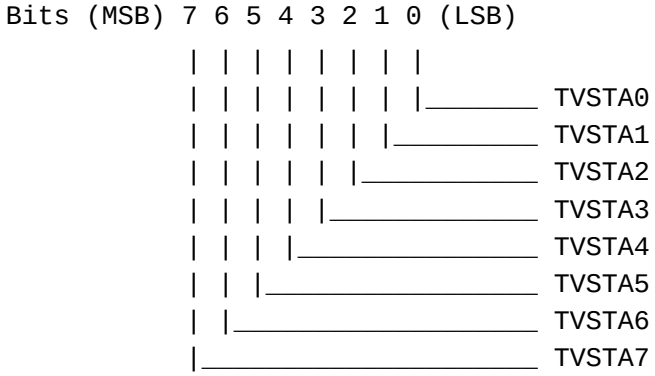
2.5 Attribute Index Readback (3?5/26, RO)

This register reads the Attribute index register.

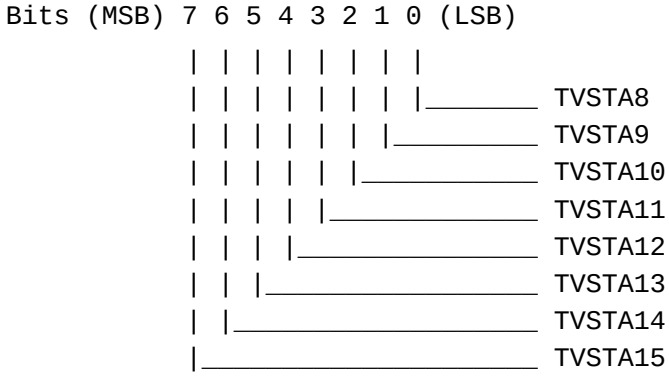


2.6 TV First Skip Line Address Low (3?5,40 R/W)

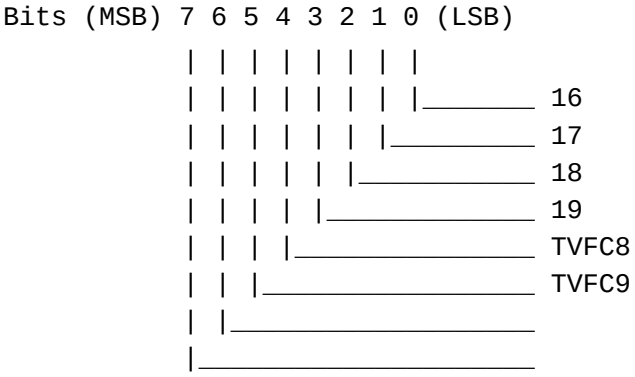
The following two registers (TVSTA[15:0]) form a starting address of the first scan line to skip.



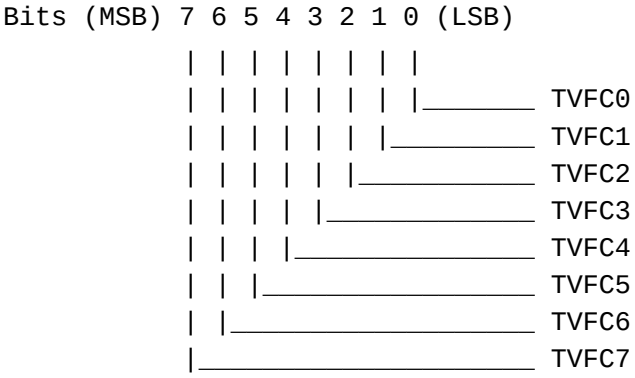
2.7 TV First Skip Line Address High (3?5,41 R/W)



2.8 TV Address Overflow (3?5,42 R/W)

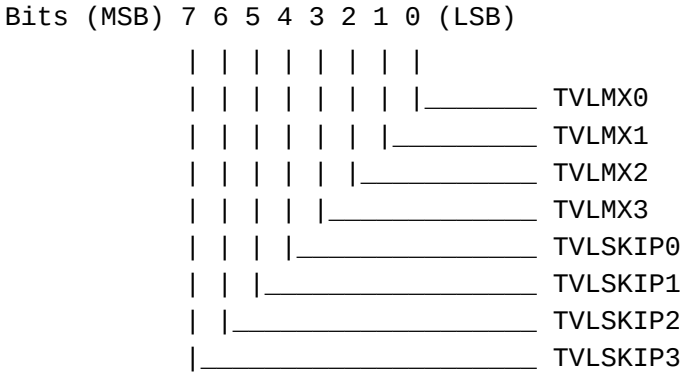


2.9 TV Line Fetch Counter (3?5,43 R/W)



TVFC[7:0]: This is a fetched counter register. It contains a number of 32-bit skip line data to be fetched and store in a temporary buffer.

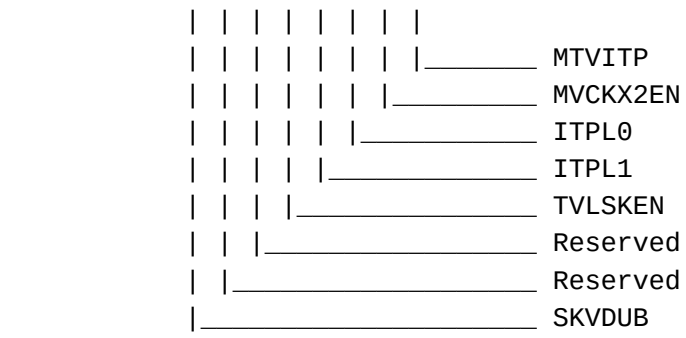
2.10 TV Max And Skip Lines (3?5,44 R/W)



TVLMX[3:0]: This is a set of lines to be operated for TV interpolation. For example, if a line needs to be skipped in every 6 original lines, a value of 6 needs to be programmed.

TVLSKIP[3:0]: Indicates which line is to be skipped in the set defined by TVLMX[3:0]. For example, in a set of 6 original lines to be operated for TV interpolation, if the original line #5 needs to be skipped, then the value of (5-1)4 needs to be programmed into this register.

2.11 TV Interpolation Miscellaneous Control (3?5,45 R/W)



MTVITP: TV Interpolation: When equal to 1, the TV interpolation function will be enabled.

MVCKX2EN: VCLK X 2 is Enable: This bit is used to enable 2 times VCLK for the interpolation circuit.

ITPL0: Interpolate Line 0: This is the upper of skipped line to operator interpolation.

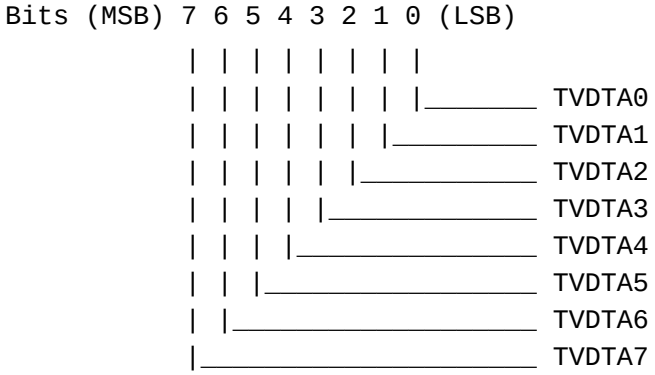
ITPL1: Interpolate Line 1: This is the lower of skipped line to operator interpolation.

TVLSKEN: When equal to 1, skip the line when line counter at skip line value.

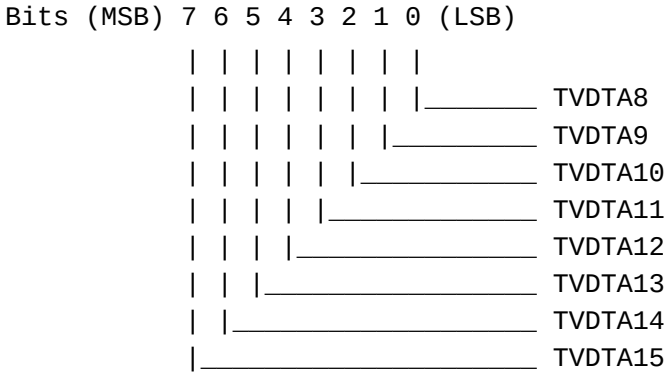
SKVDUB: Skip Vertical Double: When equal to 1, at the skip line, the next horizontal display value is next 2 scan lines.

2.12 TV Skip Delta Lines Address Low (3?5,46 R/W)

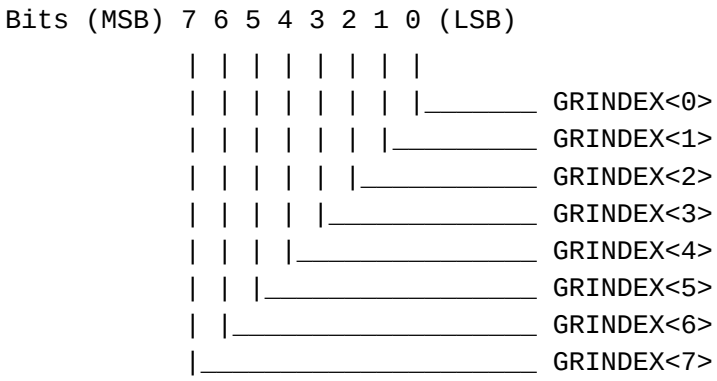
The following two registers (TVDTA[15:0]) form a delta lines different address for TV skip lines.



2.13 TV Skip Delta Lines Address High (3?5,47 R/W)

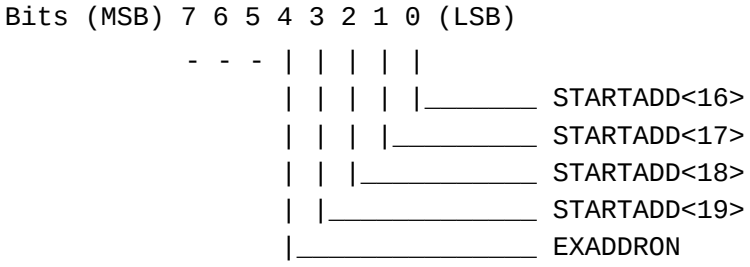


2.14 Graphics Index (3CE, R/W)



GRINDEX(7:0): These eight bits determine the index of the register pointed to in the next register R/W operation.

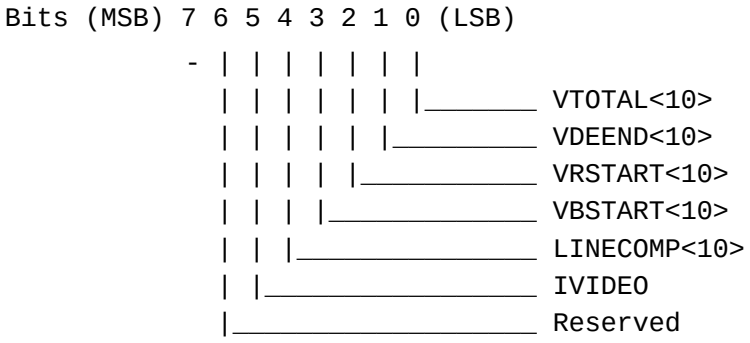
2.15 Extended Start Address (3CF/10, R/W)



STARTADD[19:16]: These are the extended high order bits of the starting memory address. This 20-bit value is the first address to use after the vertical retrace period. This value is preset into the memory address counter at the top of the screen. This height address is enabled only if bit 4 (EXADDRON) is set to logic 1.

EXADDRON: Extended Address On: This is to enable the high starting address bits STARTADD[19:16].

2.16 Extended CRT Vertical Overflow (3CF/11, R/W)



VTOTAL[10]: This is bit 10 of the vertical total value. Bit 9 is in register 3?5/7 bit 5. Bit 8 is in register 3?5/7 bit 0. The low order 8 bits are in register 3?5/6.

VDEEND[10]: This is bit 10 of the vertical display enable end value. Bit 9 is in register 3?5/7 bit 6. Bit 8 is in register 3?5/7 bit 1. The low order 8 bits are in register 3?5/12.

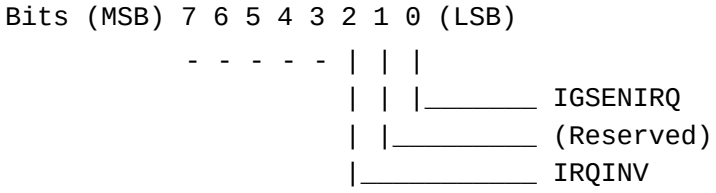
VRSTART[10]: This is bit 10 of the vertical retrace start value. Bit 9 is in register 3?5/7 bit 7. Bit 8 is in register 3?5/7 bit 2. The low order 8 bits are in register 3?5/10.

VBSTART[10]: This is bit 10 of the vertical blanking start value. Bit 9 is in register 3?5/9 bit 5. Bit 8 is in register 3?5/7 bit 3. Bits 0:7 are in register 3?5/15.

LINECOMP[10]: This is bit 10 of the line compare value. Bit 9 is in register 3?5/9 bit 6. Bit 8 is in register 3?5/7 bit 4. Bits 0:7 are in register 3?5/18.

IVIDEO: Interlace Video mode, set this bit to enable the interlace display mode. This bit is also to control a hardware cursor at interlace mode.

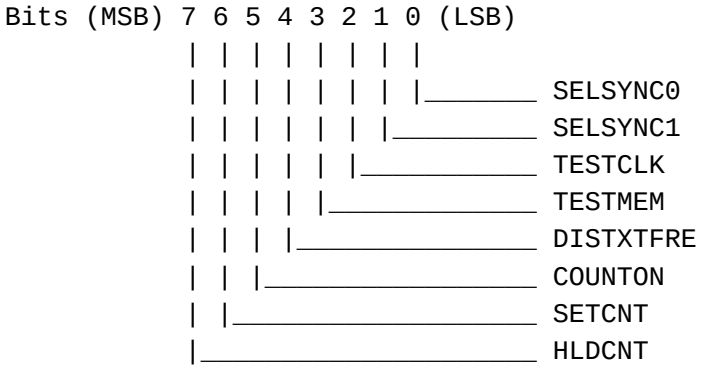
2.17 Extended CRT IRQ Control (3CF/12, R/W)



IGSENIRQ: IGS Enable IRQ: This bit has default logic 0 to disable IRQ; set this bit to logic 1 to enable the IRQ.

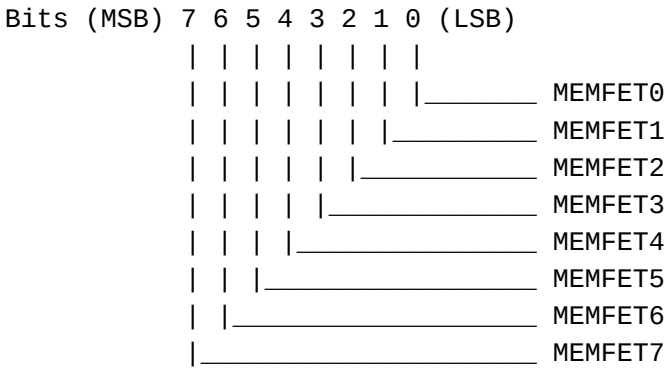
IRQINV: IRQ Invert: This bit has default logic 0 for IRQ active low; set this bit to logic 1 to change to IRQ active high.

2.18 Extended CRT Testing – Internal Test Only (3CF/13, R/W)



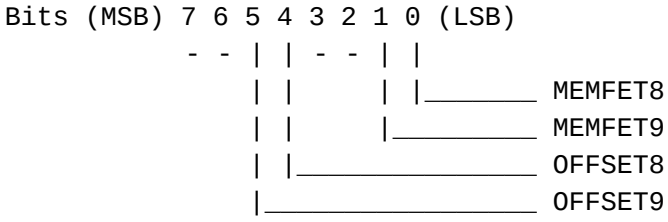
Bit[7:0]: These bits are reserved for testing. All of these bits must be cleared to logic 0 for normal operation.

2.19 Extended Number Of Fetch 0 (3CF/14, R/W)



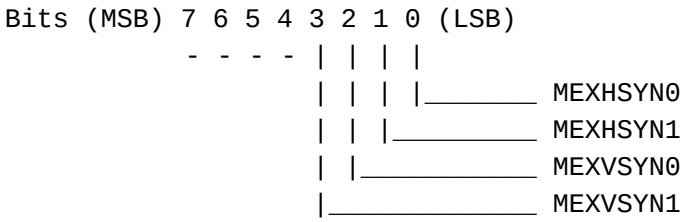
MEMFET[9:0]: Number Of Memory Fetch: These 10 register bits are used for all extended modes. The value in these 10 bits are used to define the number of fetches per scan line. For a 32-bit memory bus, the total memory fetch data is twice this value. For a 64-bit memory bus, the total memory fetch data per scan line is 4 times this value

2.20 Extended Number Of Fetch 1 (3CF/15, R/W)



OFFSET[9:8]: Offset overflow bit [9:8]: These two bits are the overflow bits for Standard CRT Register 13.

2.21 Extended HSYNC/VSYNC Control (3CF/16, R/W)



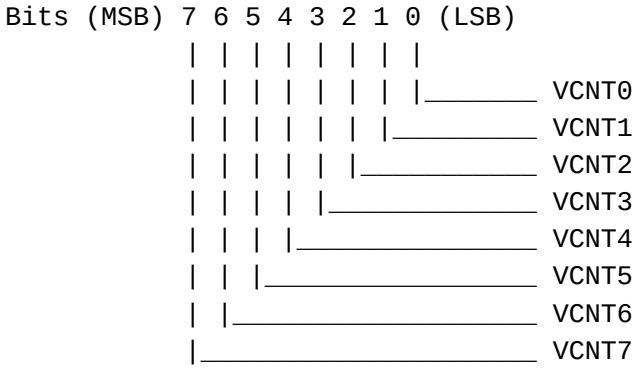
MEXHSYN[1:0]: Controls the horizontal sync signal:

MEXHSYN1	MEXHSYN0	Horizontal sync signal
0	0	Normal operation
0	1	force logic 0
1	0	force logic 1
1	1	combine HSYNC and VSYNC (for MAC monitor)

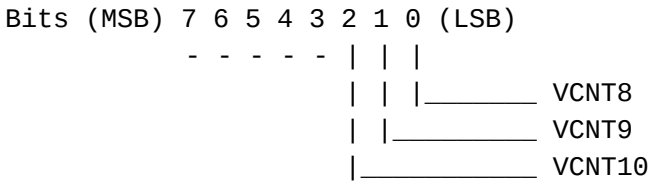
MEXVSYN[1:0]: Controls the vertical sync signal:

MEXVSYN1	MEXVSYN0	Vertical sync signal
0	0	Normal operation
0	1	force logic 0
1	0	force logic 1
1	1	TV composite sync

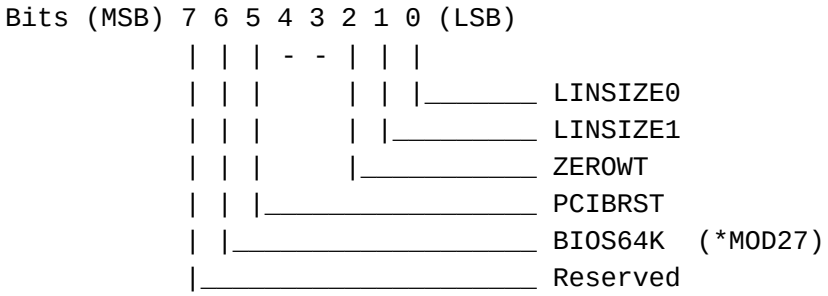
2.22 Extended CRT Vertical Counter 0 (3CF/18, RO)



2.23 Extended CRT Vertical Counter 1 (3CF/19, RO)



2.24 Extended Bus Control (3CF/30, R/W)



ZEROWT: Zero Wait: When this bit equals 1, a zero wait state CPU write cycle is enabled.

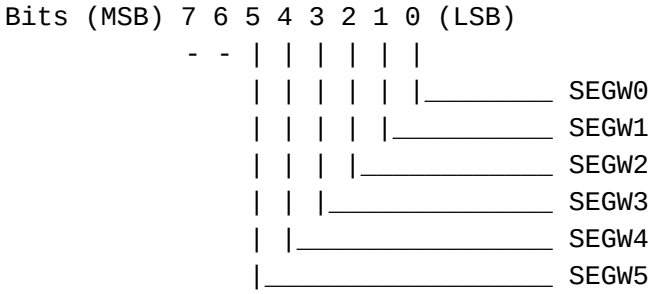
PCIBRST: PCI BURST MODE: This bit is used in PCI mode only. When this bit is set, the graphics chip internally accepts Burst mode. This bit defaults logic low to disable Burst mode.

BIOS64K = 1: Sets the VGA BIOS to 64KB memory.

LINSIZE[1:0]: Defines the linear opened address:

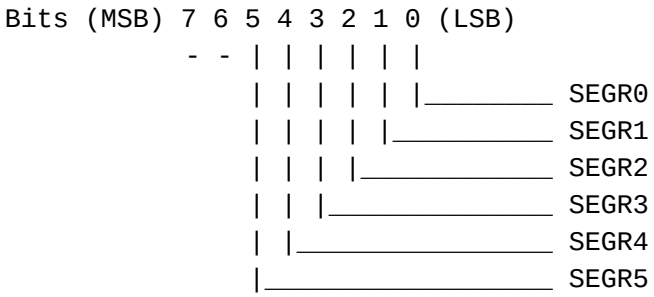
LINSIZE1	LINSIZE0	Linear address size
0	0	1MB
0	1	2MB
1	X	4MB

2.25 Extended Segment Write Pointer (3CF/31, R/W)



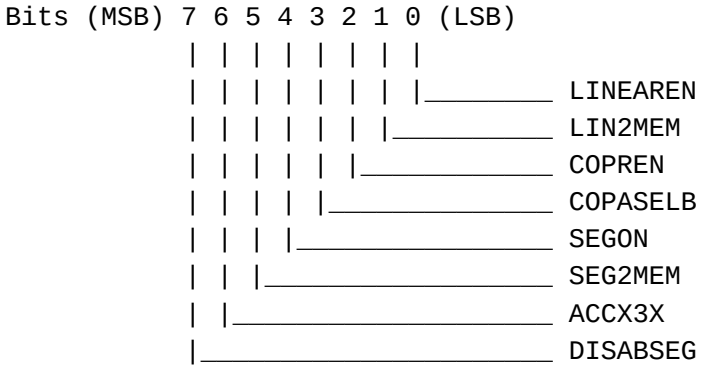
SEGW[5:0]: Segment Write pointer, each value of this register can access 64k of system memory at location A0000:AFFFF.

2.26 Extended Segment Read Pointer (3CF/32, R/W)



SEGR[5:0]: Segment Read pointer, each value of this register can access 64k of system memory at location A0000:AFFFF.

2.27 Extended BIU Miscellaneous Control (3CF/33, R/W)



LINEAREN: Linear Enable: When this bit equals 1, the linear address is enabled.

LIN2MEM: Linear To Memory: When this bit equals 0, the CPU cycle access through linear address may be the HOST BLT (COP) or the memory cycle, depending upon the coprocessor control signal. If this bit equals 1, the CPU cycle is forced to be memory cycle.

COPREN: Coprocessor Registers Enable: This bit has a default value of 0. When this bit equals 1, CPU can direct access to the Coprocessor 256 byte area.

COPASELB: COP Address Select A/B Segment: When this bit equals 0, the graphics engine address is set to AFC00 - AFFFF. When this bit equals 1, the graphics engine address is set to BFC00 - BFFFF (1KB) access.

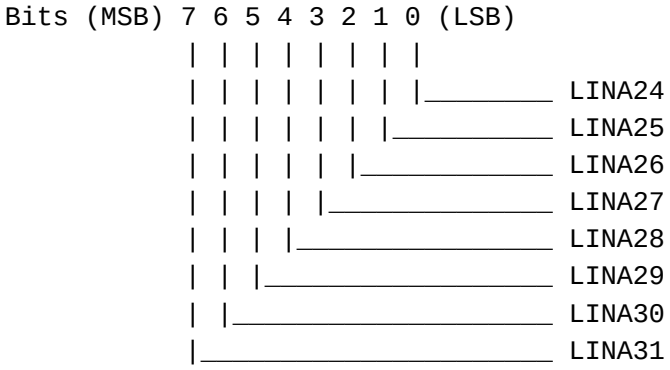
SEGON: Segment On: When this bit equals 1, the 64K segment address at A is enabled.

SEG2MEM: Segment To Memory: When this bit equals 0, the CPU's segment cycle may be the HOST BLT (COP) or the memory cycle, depending upon the graphics engine control signal. If this bit equals 1, the CPU cycle is forced to the memory cycle.

DISABSEG: Disables A/B segment: When this bit equals 1, and the graphics engine is in real mode, the A/B segment access is disabled. The bit default is 0.

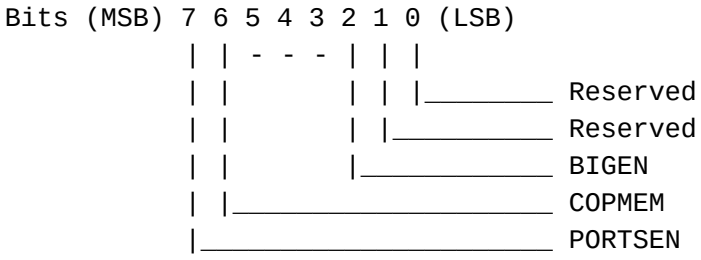
ACCX3X: Access Address X3X: When this bit equals 0, the normal 3CF/3X registers are used. When this bit equals 1, the extended 3CF/X3X registers are used.

2.28 Extended Linear Address (3CF/35, RO)



The Configuration R/W Cycle for the Base Address Register at location h10-h13 is used to allocate an address on the PCI bus. The most significant byte (h13) is the byte in this register. There is a total of 16MB reserved for the linear address A0-A23.

2.29 Function Control (3CF/3C, R/W)

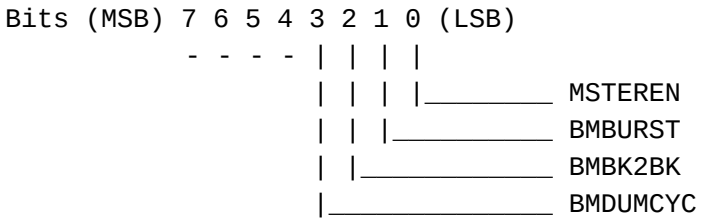


BIGEN: Big Endian Enable: When this bit is equal to 1, the data transfer between the system bus and the graphics controller is changed to the big endian format. The big endian format is based on program resister 3CF/3F.

COPMEM: Co-processor Memory Map: When equal to 1, the linear memory-map access data to co-processor is enabled. The linear address LL90PPPP(hex) is used to map to co-processor. When equal to 0, this range of address is used for EPROM access.

PORTSEN: Ports Enable: When equal to 1, the TV, and PORTS[7:0] registers allow to access.

2.30 PCI Bus Master Control (3CF/3E, R/W)



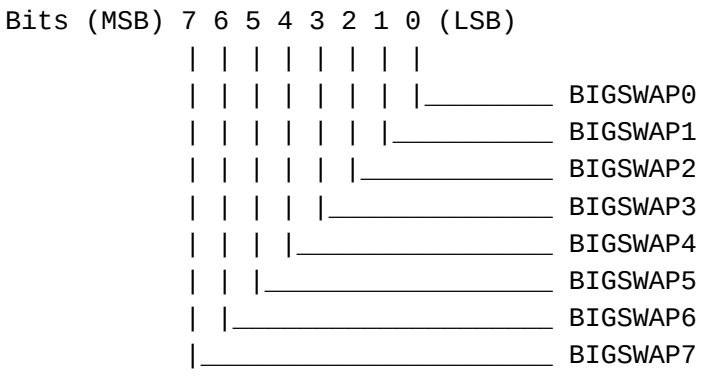
MSTEREN: Bus Master Enable: When equal to 1, the Bus Master mode is enabled.

BMBURST: Bus Master Burst: When equal to 1, allows the burst on Bus Master.

BMBK2BK: Bus Master Back-To-Back: When equal to 1, allows burst cycle running at back-to-back mode.

BMDUMCYC: Bus Master Dummy Cycle: When equal to 1, inserts dummy cycle during burst cycle.

2.31 Big Endian Control (3CF/3F, R/W)



BIGSWAP[7:0]: This register is used only if bit 3 in 3CF/3C is set to logic 1. Then the data path between the system and the graphics chip will perform any combination of byte swapping. The following table lists the byte swap paths, which applies to all system memory read or write cycles.

Byte Swap Table

If BIGSWAP[1:0]=00, then system data byte0 to/from chip data path byte0.

If BIGSWAP[1:0]=01, then system data byte1 to/from chip data path byte0.

If BIGSWAP[1:0]=10, then system data byte2 to/from chip data path byte0.

If BIGSWAP[1:0]=11, then system data byte3 to/from chip data path byte0.

If BIGSWAP[3:2]=00, then system data byte1 to/from chip data path byte1.

If BIGSWAP[3:2]=01, then system data byte0 to/from chip data path byte1.

If BIGSWAP[3:2]=10, then system data byte3 to/from chip data path byte1.

If BIGSWAP[3:2]=11, then system data byte2 to/from chip data path byte1.

If BIGSWAP[5:4]=00, then system data byte2 to/from chip data path byte2.

If BIGSWAP[5:4]=01, then system data byte3 to/from chip data path byte2.

If BIGSWAP[5:4]=10, then system data byte0 to/from chip data path byte2.

If BIGSWAP[5:4]=11, then system data byte1 to/from chip data path byte2.

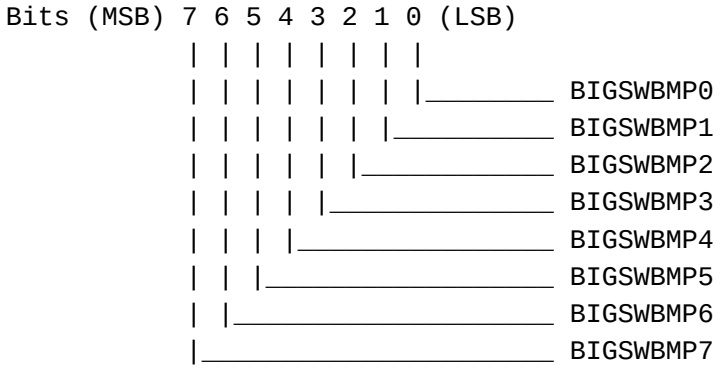
If BIGSWAP[7:6]=00, then system data byte3 to/from chip data path byte3.

If BIGSWAP[7:6]=01, then system data byte2 to/from chip data path byte3.

If BIGSWAP[7:6]=10, then system data byte1 to/from chip data path byte3.

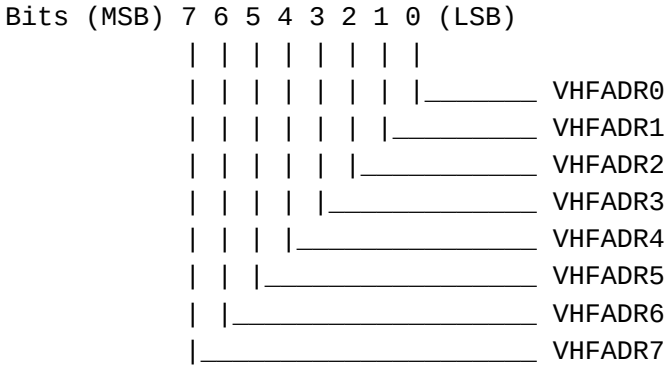
If BIGSWAP[7:6]=11, then system data byte0 to/from chip data path byte3.

2.32 Bus Master Program Big Endian Swap (3CF,X3E R/W)



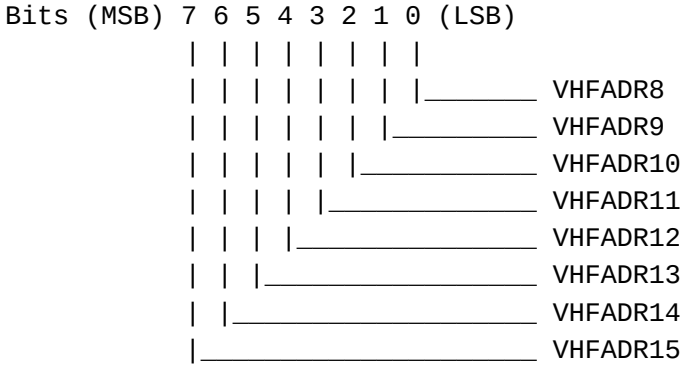
BIGSWBMP[7:0]: This register is to swap bytes during Bus Master program mode. If no Big Endianess, this register must be all zero. For Big Endian Bus Master program mode, the value in this register follows the same manner in register 3cf/3f BYTE SWAP TABLE.

2.33 Extended V2 Video Memory Starting Address Low (3CF/X40, R/W)



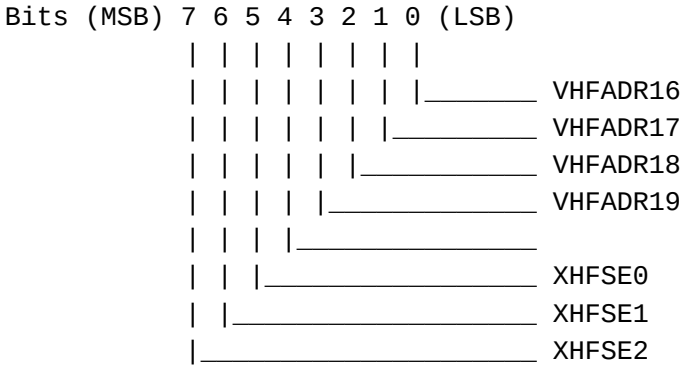
VHFADR[7:0]: Video starting address low: This address field will be defined as video display starting address.

2.34 Extended V2 Video Memory Starting Address Middle (3CF/X41, R/W)



VHFADR[15:8]: Video starting address middle: This address field will be defined as video display starting address. (which is 32 bits address field.)

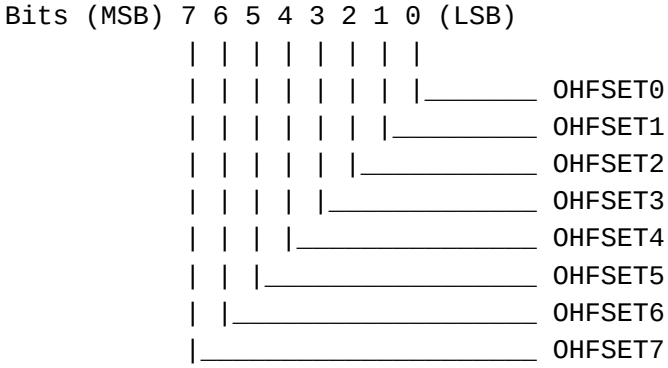
2.35 Extended V2 Video Memory Starting Address High (3CF/X42, R/W)



VHFADR[19:16]: Video starting address HIGH: This address field will be defined as video display starting address.

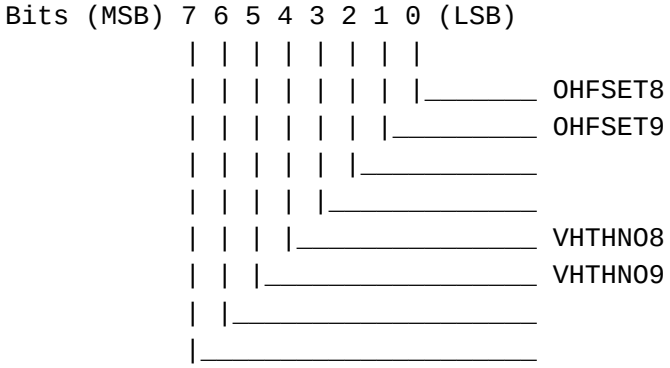
XHFSE[2:0]: Horizontal phase offset: These three bits will control horizontal video "pixel" offset value from 0 to 7.

2.36 Extended V2 Video Source Map Width Low (3CF/X43, R/W) (V2 Video Memory Fetch Pitch Low)



OHFSET[7:0]: Video map width low: This offset value will control video display next line starting address.

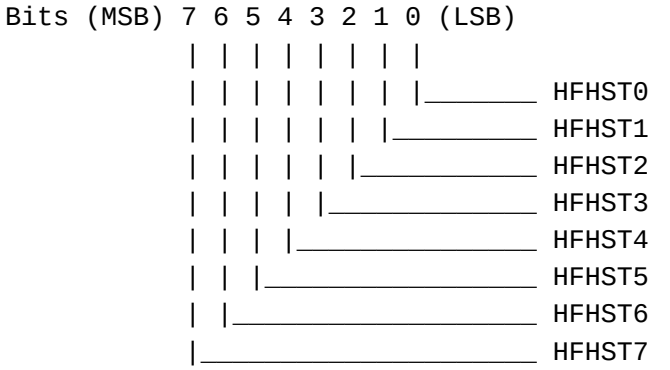
2.37 Extended V2 Video Source Map Width High (3CF/X44, R/W) (64-bit) (V2 Video Memory Fetch Pitch High)



OHFSET[9:8]: Video map width high: This offset value will control video display next line starting address.

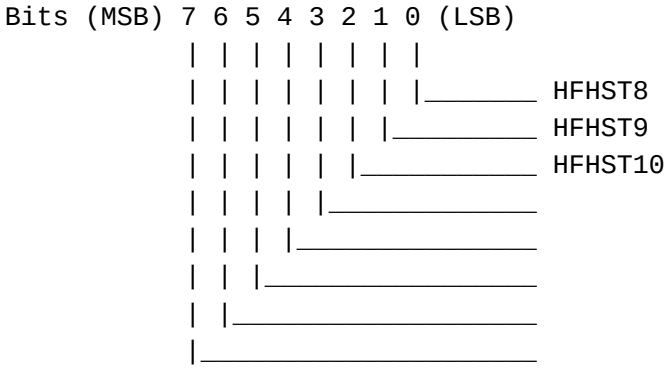
VHTHNO[9:8]: Video display fetch number high: This fetch number will determine the number of pixels which will be fetched from video memory. This field is always programmed same as OFFSET register.

2.38 Extended V2 Video Display Horizontal Starting Pixel Low (3CF/X45, R/W)



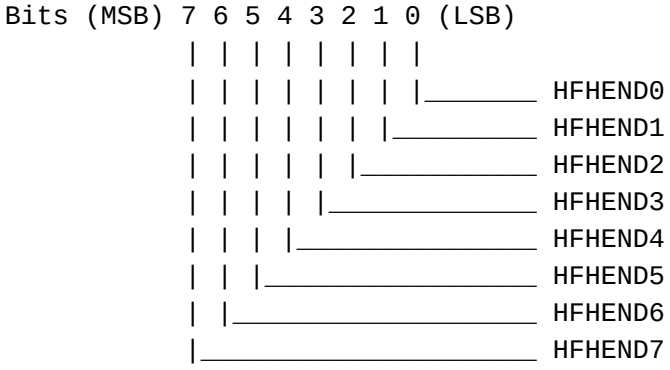
HFHST[7:0]: Video display horizontal start low: This field will be used to determine the starting pixel of a horizontal display line and the first pixel should be programmed to 0.

2.39 Extended V2 Video Display Horizontal Starting Pixel High (3CF/X46, R/W)



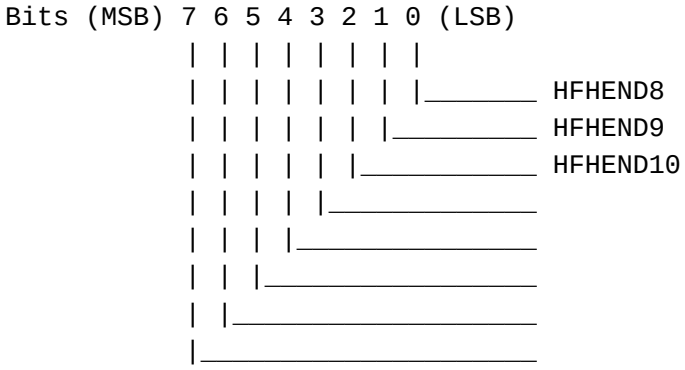
HFHST[10:8]: Video display horizontal start high: This field will be used to determine the starting pixel of a horizontal display line and the first pixel should be programmed 0.

2.40 Extended V2 Video Display Horizontal Ending Pixel Low (3CF/X47, R/W)



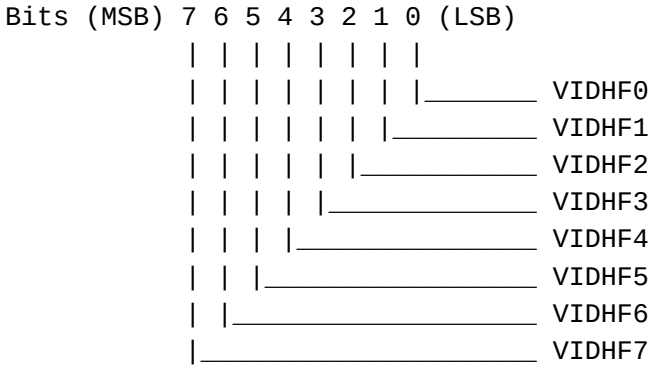
HFHEND[7:0]: Video display horizontal end low: This field will be used to determine the ending pixel of a horizontal display line and this register should be programmed of the starting pixel plus the desired display pixel width. For example, if the starting pixel = 0Ah and the display pixel width = 10h, then this field should be 0Ah+10h = 1Ah.

2.41 Extended V2 Video Display Horizontal Ending Pixel High (3CF/X48, R/W)



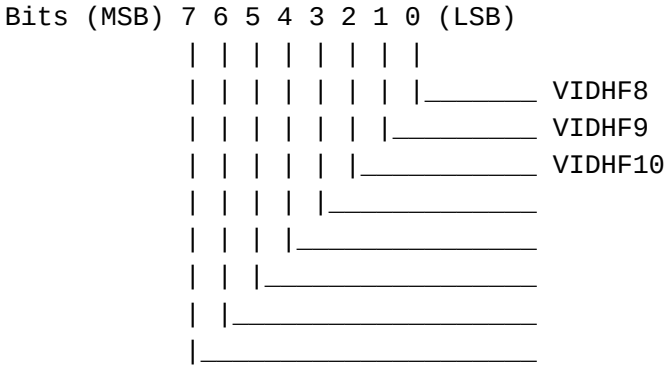
HFHEND[10:8]: Video display horizontal end high: This field will be used to determine the ending pixel of a horizontal display line and this register should be programmed of the starting pixel plus the desired display pixel width. For example, if the starting pixel = 0Ah and the display pixel width = 10h, then this field should be 0Ah+10h = 1Ah.

2.42 Extended V2 Video Display Vertical Starting Line Low (3CF/X49, R/W)



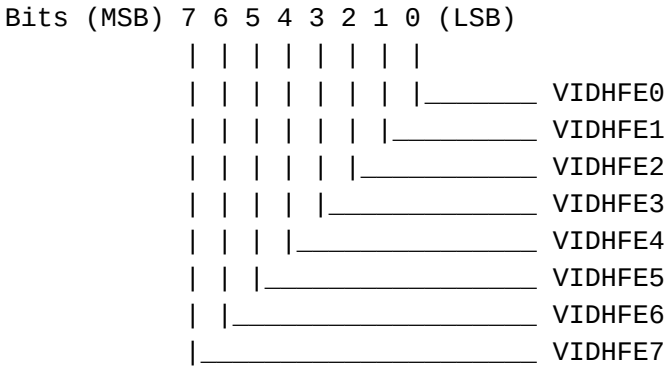
VIDHF[7:0]: Video display vertical start low: This field will be used to determine the starting line of the vertical display line and the first display line should be programmed to 0.

2.43 Extended V2 Video Display Vertical Starting Line High (3CF/X4A, R/W)



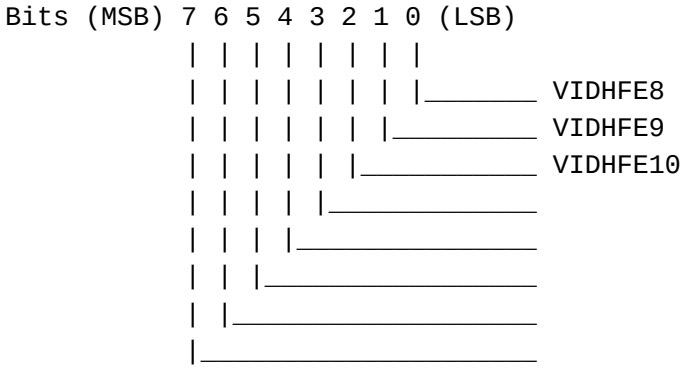
VIDHF[10:8]: Video display vertical start high: This field will be used to determine the starting line of the vertical display line and the first display line should be programmed to 0.

2.44 Extended V2 Video Display Vertical Ending Line Low (3CF/X4B, R/W)



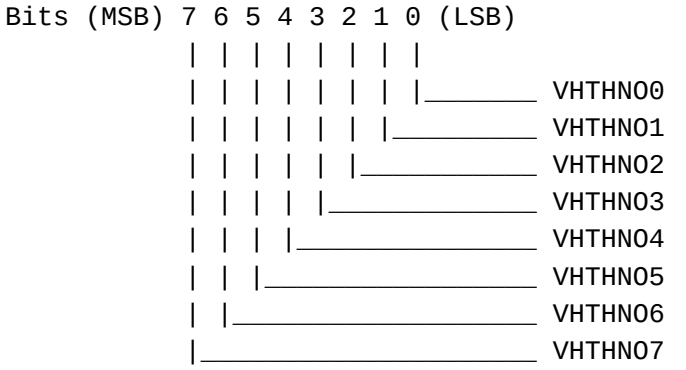
VIDHFE[7:0]: Video display vertical end low: This field will be used to determine the ending line of the vertical display line and this register should be programmed of the starting display line plus the desired display line width. For example, if the starting display line = 0Ah and the display line width = 10h, then this field should be 0Ah+10h = 1Ah.

2.45 Extended V2 Video Display Vertical Ending Line High (3CF/X4C, R/W)



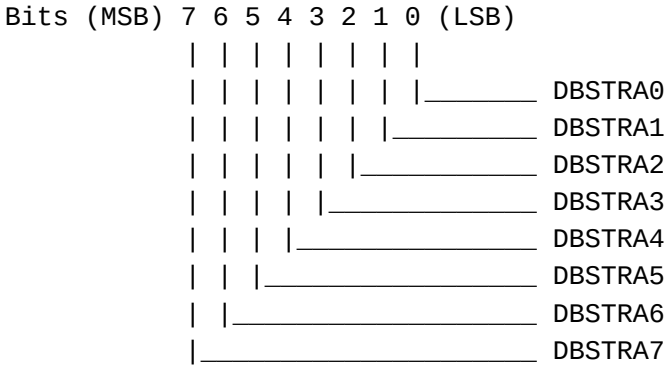
VIDHFE[10:8]: Video display vertical end high: This field will be used to determine the ending line of the vertical display line and this register should be programmed of the starting display line plus the desired display line width. For example, if the starting display line = 0Ah and the display line width = 10h, then this field should be 0Ah+10h = 1Ah.

2.46 Extended V2 Video Display Memory Offset Phase (3CF/X4D, R/W)



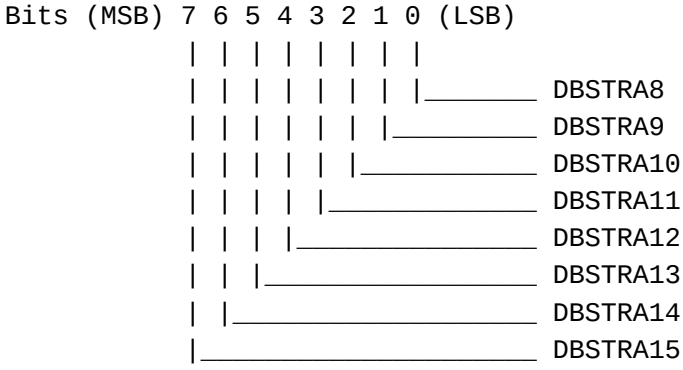
VHTHNO[7:0]: Video display fetch number low: This fetch number will determine the number of pixels which will be fetched from video memory. This field is always programmed the same as the OFFSET register. If the register bits XHFSE[2:0] are not equal to 0, then the proper value should be added to this field.

2.47 Extended Double Buffer Starting Address A Low (3CF/Y41, R/W)



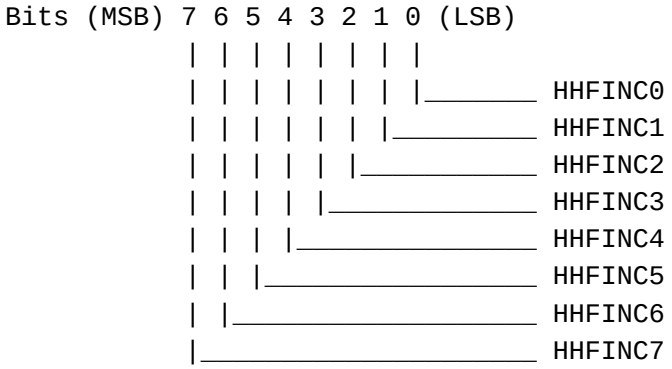
DBSTRA[7:0]: Video double buffer A starting address low: This field is the starting address of video double buffer A.

2.48 Extended Double Buffer Starting Address A Middle (3CF/Y42, R/W)



DBSTRA[15:8]: Video double buffer A starting address middle : This field is the starting address of video double buffer A.

2.49 Extended V2 Video Horizontal DDA Increment Value Low (3CF/Y43, R/W)

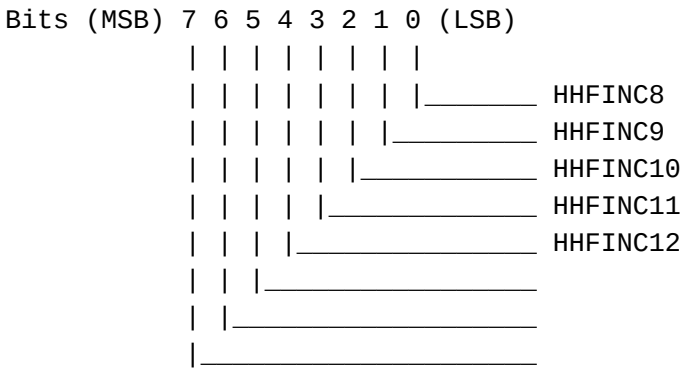


HHFINC[7:0]: Horizontal DDA (digital differential algorithm) increment value low: The formula to calculate this field is shown below :

$$HHFINC = \frac{(video\_pixel\_width\_in\_memory - 2) * 1000h + 800h - HDDAINI}{video\_pixel\_width\_on\_screen}$$

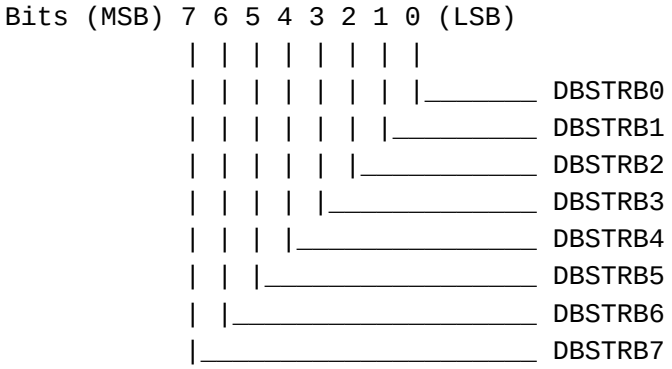
If no horizontal interpolation will be used, then this field should be programmed to 1000h.

2.50 Extended V2 Video Horizontal DDA Increment Value High (3CF/Y44, R/W)



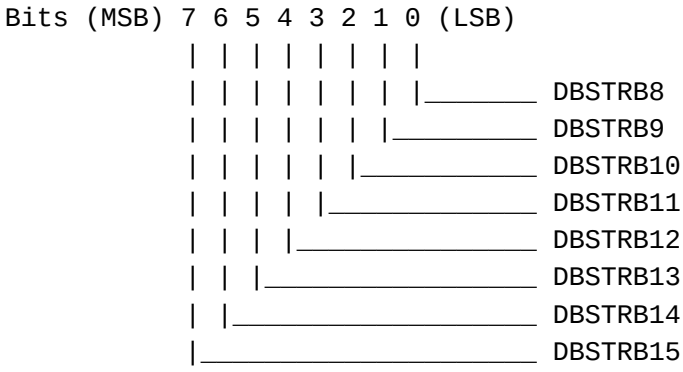
HHFINC[12:8]: Horizontal DDA (digital differential algorithm) increment value high.

2.51 Extended Double Buffer Starting Address B Low (3CF/Y45, R/W)



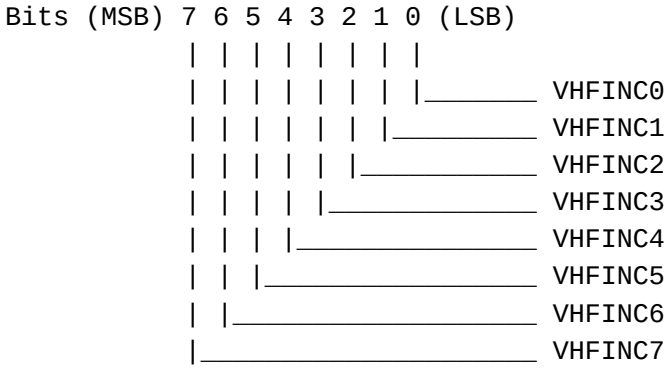
DBSTRB[7:0]: Video double buffer B starting address low: This field is the starting address of video double buffer B.

2.52 Extended Double Buffer Starting Address B Middle (3CF/Y46, R/W)



DBSTRB[7:0]: Video double buffer B starting address middle: This field is the starting address of video double buffer B.

2.53 Extended V2 Video Vertical DDA Increment Value Low (3CF/Y47, R/W)

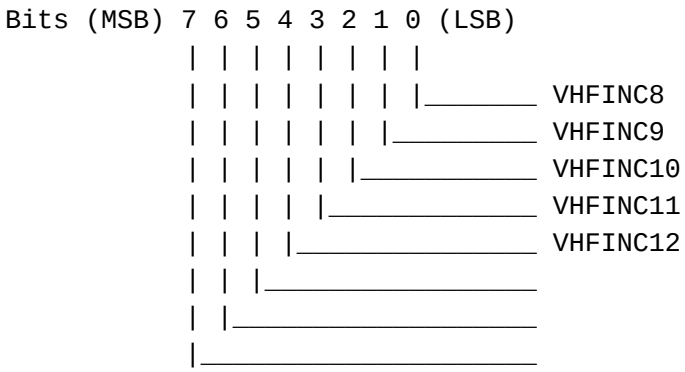


VHFINC[7:0]: Vertical DDA (digital differential algorithm) increment value low: The formula to calculate this field is shown below :

$$VHFINC = \frac{(video\_line\_height\_in\_memory - 2) * 1000h + 800h - VDDAINI}{video\_pixel\_line\_on\_screen}$$

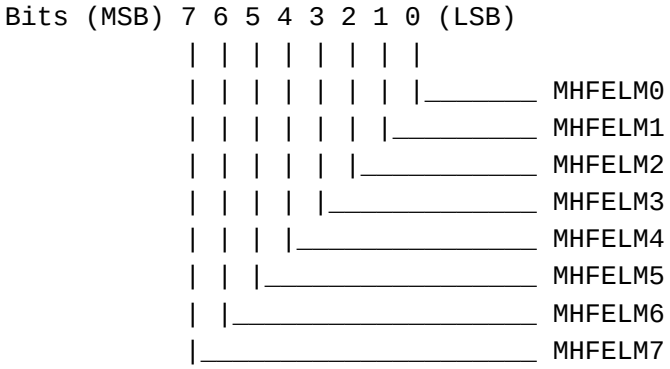
If no vertical interpolation will be used, then this field should be programmed to 1000h.

2.54 Extended V2 Video Vertical DDA Increment Value High (3CF/Y48, R/W)



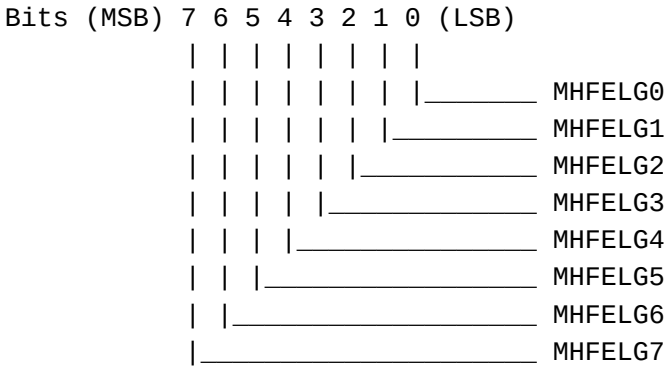
VHFINC[12:8]: Vertical DDA (digital differential algorithm) increment value high.

2.55 Extended V2 Video FIFO Low Control (3CF/Y49, R/W)



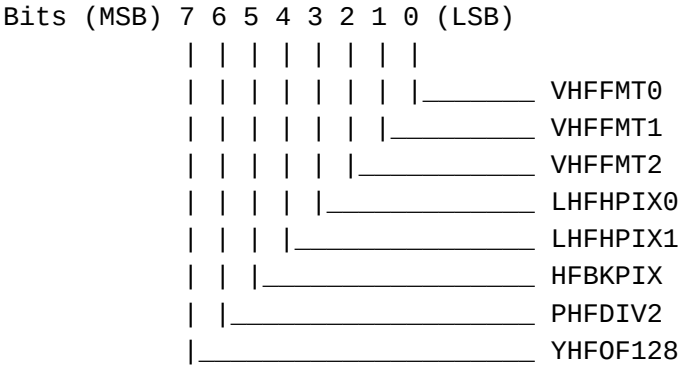
MHFELM[7:0]: Video FIFO policy must value: This field will defined the video high request timing.

2.56 Extended V2 Video FIFO High Control (3CF/Y4A, R/W)



MHFELG[7:0]: Video FIFO policy general value: This field will defined the video low request timing.

2.57 Extended V2 Video Format Control (3CF/Y4B, R/W)



VHFFMT[2:0]: Video Pixel Display Format:

VHFFMT2	VHFFMT11	VHFFMT0	# Video Input Format	
0	0	0	4 2 2 YUV	(YUVPIX)
0	0	1	5 5 5 RGB	(RG5BPIX)
0	1	0	5 6 5 RGB	(RG6BPIX)
0	1	1	24 Bits RGB	(RGB24PIX)
1	0	0	32 Bits RGB	(RGB32PIX)
1	0	1	8 Bits RGB	(RGB8PIX)
1	1	0	4 4 4 4 RGB	(RGB4PIX)
1	1	1	8T Bit RGB	(RGB8TPIX)

LHFHPIX[1:0]: Video Pixel Display Zoom Out Format:

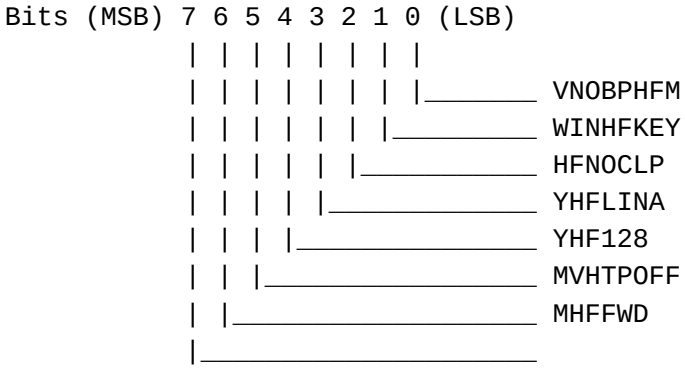
LHFHPIX1	LHFHPIX0	# Video Pixel Zoom Out Format	
0	0	0.5 Linearity approach	(LINHPIX)
0	1	Duplicate Previous Pixel	(DUPPIX)
1	x	Reserved	

HFBKPIX: Third pixel jump back: When this bit is set to 1 and LINHPIX[1:0] is equal to 00, the third duplicated pixel will jump back one-half value. When this bit is set to 0, no action will take place.

PHFDIV2: Double horizontal display pixel: When this bit is set to 1, horizontal pixel will be duplicated.

YHFOF128: YUV Data Offset 128: When this bit is equal to 1, YUV pixel data will be added 128 before any process.

2.58 Extended V2 Video display Control I (3CF/Y4C, R/W)



VNOBPHFM: Video pixel not by passed internal ram: When this bit is equal to 0, pixel data will totally bypass internal RAM.

WINHFKEY: Video display use window key: When this bit is equal to 1, video display will ignore color compare register.

HFNOCLP: Data process no clipping: When this bit is set to 1, video FIFO data will not be clipped to (16, 235) (16, 240).

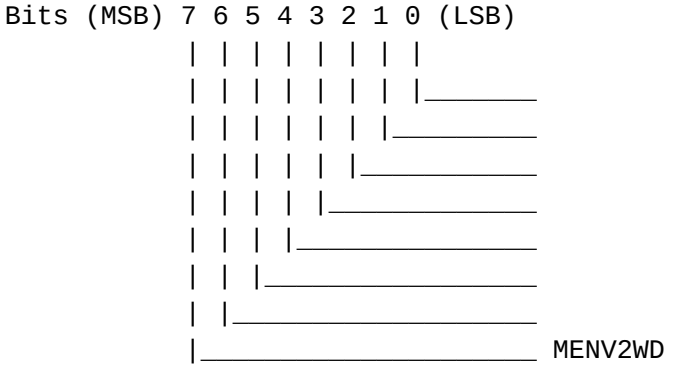
YHFLINA: U and V data process linearly: When this bit is equal to 1, U and V data will be averaged by previous U(V) and the U(V) pixel after.

YHF128: Y Color Offset 128 enable: When this bit and YUVOF128 both are set to 1, then Y color will offset by 128.

MVHTPOFF: Vertical interpolation off: When this bit is equal to 1, then the vertical interpolation will be turned off

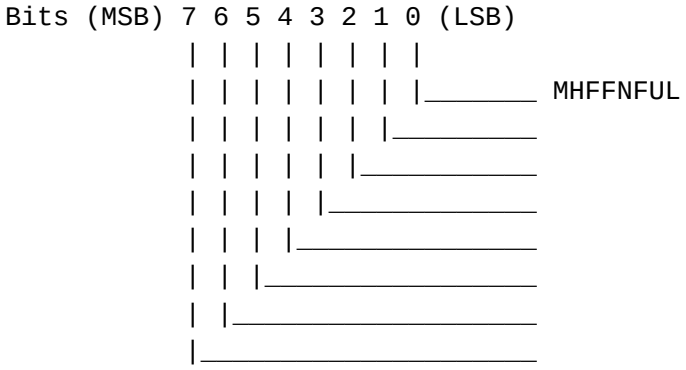
MHFFWD: Video on full window: When this bit is equal to 1, no CRT data will be fetched and only video data will be displayed.

2.59 Extended V2 Video FIFO Control I (3CF/Y4D, R/W)



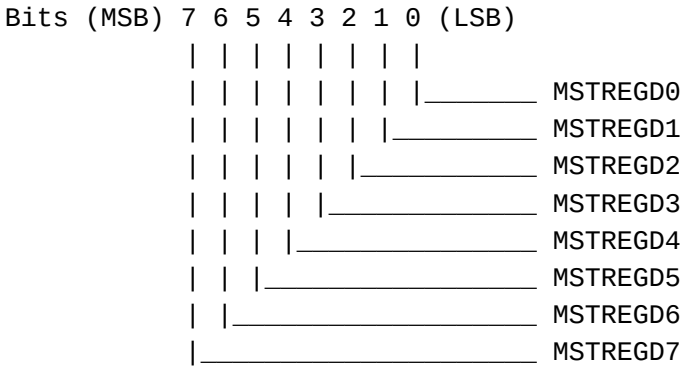
MENV2WD: Enables V2 Video: When this bit is equal to 1, then V2 video will be enabled

2.60 Extended V2 Video Miscellaneous Control I (3CF/Y4E, R/W)



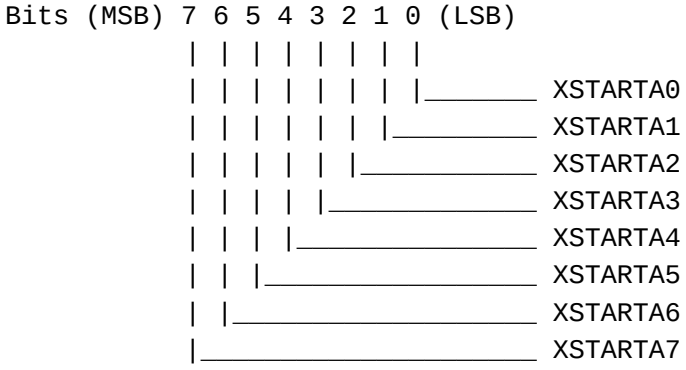
MHFFNFUL: CF FIFO not full: When this bit and MOFFDLY(SQ) are both at 1, CF FIFO will only has high request and not fill out the FIFO.

2.61 Extended Steeling Cycle D (3CF/Y4F, R/W)



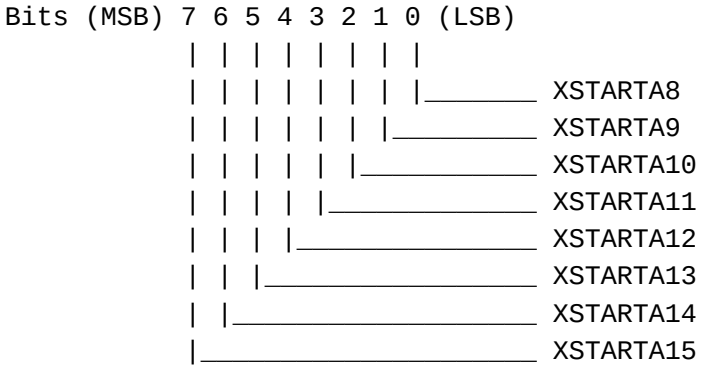
MSTREGD[7:0]: Cycle steeling data D: This is byte 3 for the period of cycle steeling.

2.62 Extended X2 Video Memory Starting Address Low (3CF/J40, R/W)



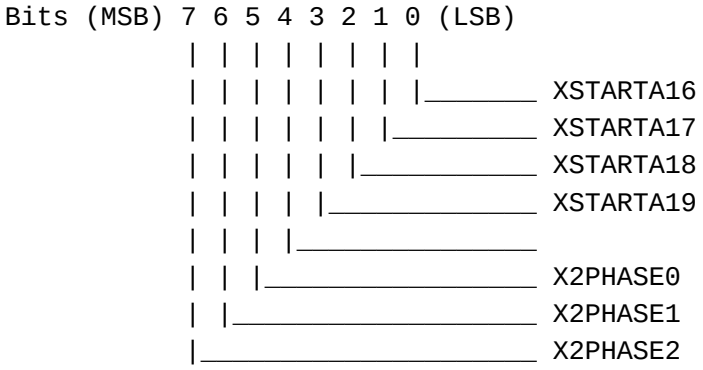
XSTARTA[7:0]: Video starting address low: This address field will be defined as video display starting address.

2.63 Extended X2 Video Memory Starting Address Middle (3CF/J41, R/W)



XSTARTA[15:8]: Video starting address middle: This address field will be defined as the video display starting address.

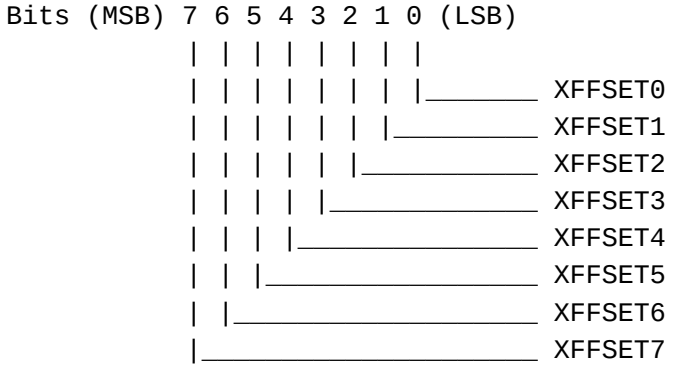
2.64 Extended X2 Video Memory Starting Address High (3CF/J42, R/W)



XSTARTA[19:16]: Video starting address HIGH: This address field will be defined as the video display starting address.

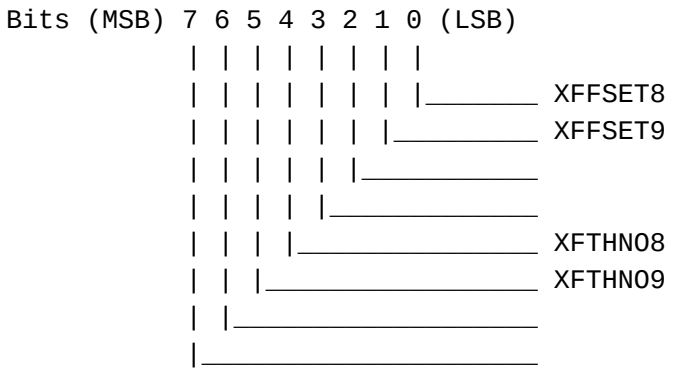
X2PHASE[2:0]: Horizontal phase offset: These three bits will control the horizontal video "pixel" offset value from 0 to 7.

2.65 Extended X2 Video Source Map Width (3CF/J43, R/W) (X2 Video Memory Fetch Pitch Low)



XFFSET[7:0]: Video map width low: This offset value will control video display next line starting address.

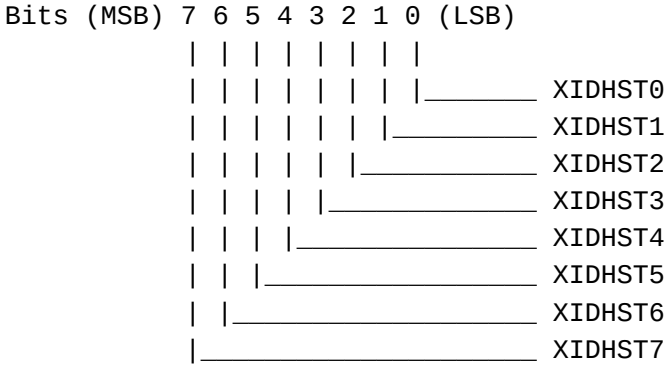
2.66 Extended X2 Video Memory SRC Map and SRC Window Width High (3CF/J44, R/W) (X 2Video Memory Fetch Pitch High)



XFFSET[9:8]: Video map width high: This offset value will control video display next line starting address.

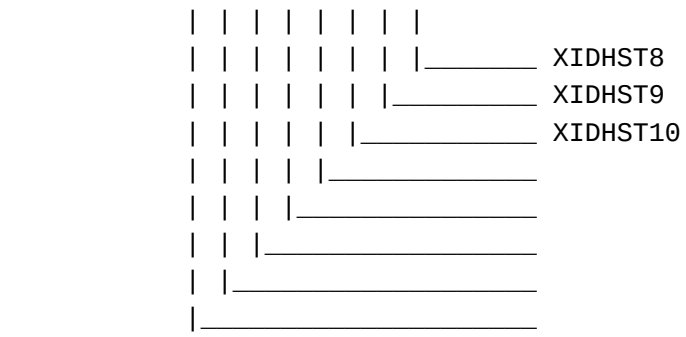
XFTHNO[9:8]: Video display fetch number high: This fetch number will determine the number of pixels which will be fetched from video memory. This field is always programmed same as OFFSET register.

2.67 Extended X2 Video Display Horizontal Pipe Starting Pixel Low (3CF/J45, R/W)



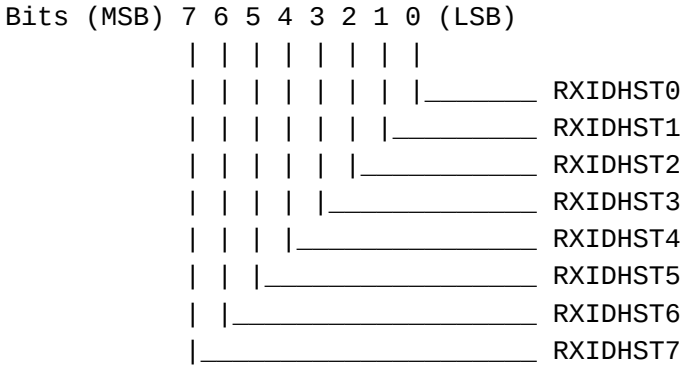
XIDHST[7:0]: Video display horizontal pipe start low: This field will be used to determine the pipe starting pixel of a horizontal display line.

2.68 Extended X2 Video Display Horizontal Pipe Starting Pixel High (3CF/J46, R/W)



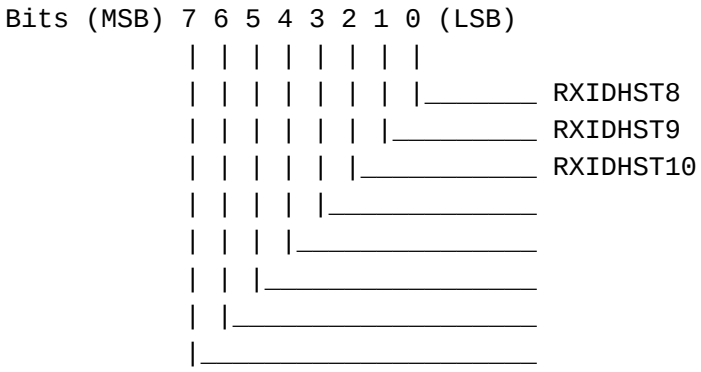
XIDHST[10:8]: Video display horizontal pipe start low: This field will be used to determine the pipe starting pixel of a horizontal display line.

2.69 Extended X2 Video Display Horizontal Starting Pixel Low (3CF/J47, R/W)



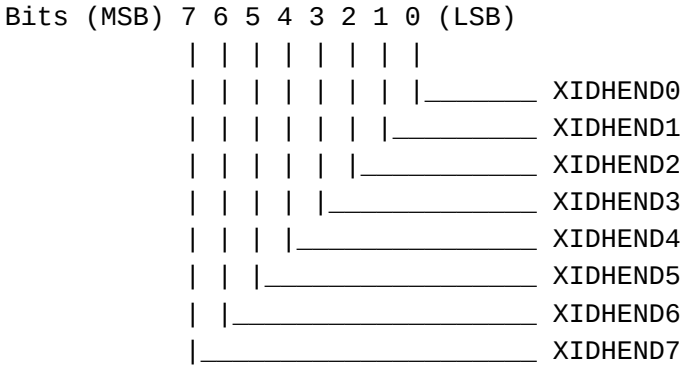
RXIDHST[7:0]: Video display horizontal start low: This field will be used to determine the starting pixel of a horizontal display line and the first pixel should be programmed to 0.

2.70 Extended X2 Video Display Horizontal Starting Pixel High (3CF/J48, R/W)



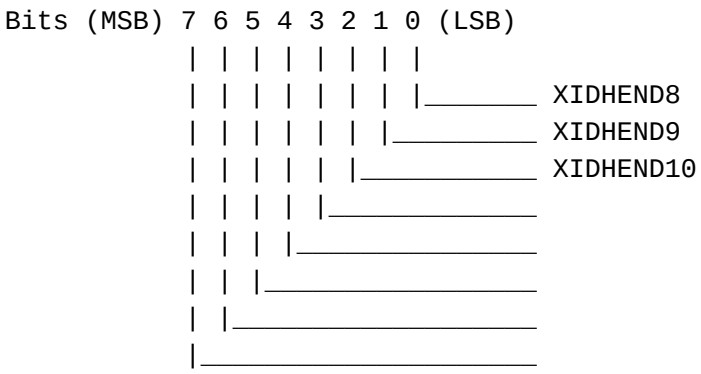
RXIDHST[10:8]: Video display horizontal start high: This field will be used to determine the starting pixel of a horizontal display line and the first pixel should be programmed 0.

2.71 Extended X2 Video Display Horizontal Ending Pixel Low (3CF/J49, R/W)



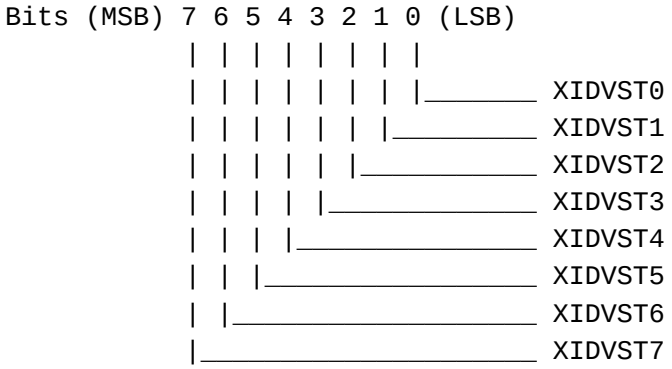
XIDHEND[7:0]: Video display horizontal end low: This field will be used to determine the ending pixel of a horizontal display line and this register should be programmed of the starting pixel plus the desired display pixel width.

2.72 Extended X2 Video Display Horizontal Ending Pixel High (3CF/J4A, R/W)



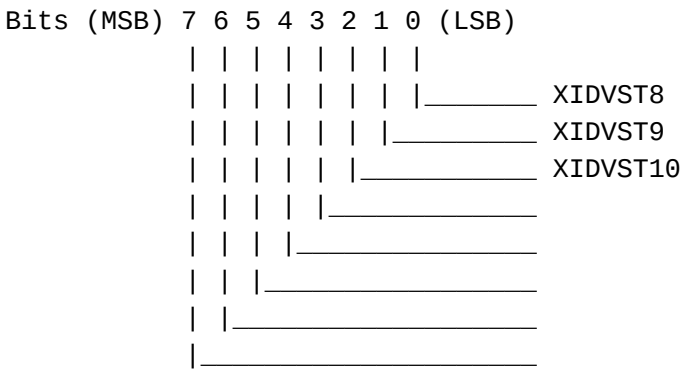
XIDHEND[10:8]: Video display horizontal end high: This field will be used to determine the ending pixel of a horizontal display line and this register should be programmed of the starting pixel plus the desired display pixel width.

2.73 Extended X2 Video Display Vertical Starting Line Low (3CF/J4B, R/W)



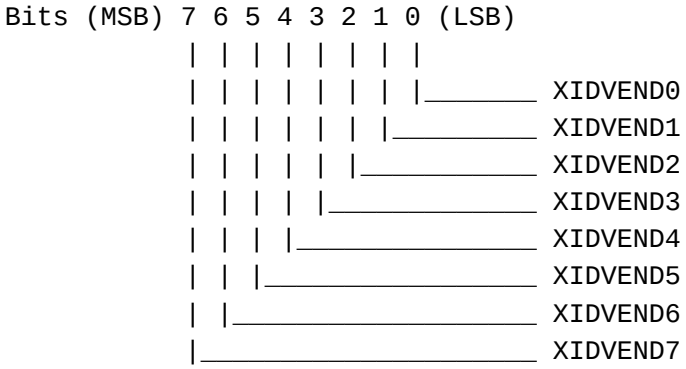
XIDVST[7:0]: Video display vertical start low: This field will be used to determine the starting line of the vertical display line and the first display line should be programmed to 0.

2.74 Extended X2 Video Display Vertical Starting Line High (3CF/J4C, R/W)



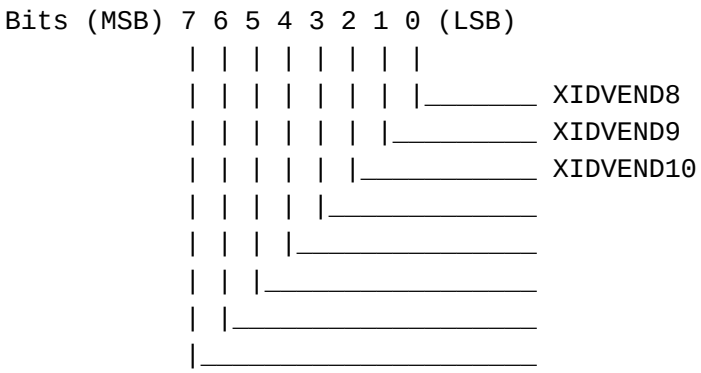
XIDVST[10:8]: Video display vertical start high: This field will be used to determine the starting line of the vertical display line and the first display line should be programmed to 0.

2.75 Extended X2 Video Display Vertical Ending Line Low (3CF/J4D, R/W)



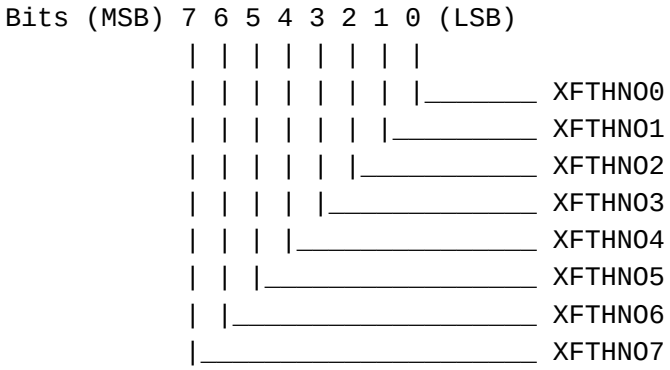
XIDVEND[7:0]: Video display vertical end low: This field will be used to determine the ending line of the vertical display line and this register should be programmed of the starting display line plus the desired display line width.

2.76 Extended X2 Video Display Vertical Ending Line High (3CF/J4E, R/W)



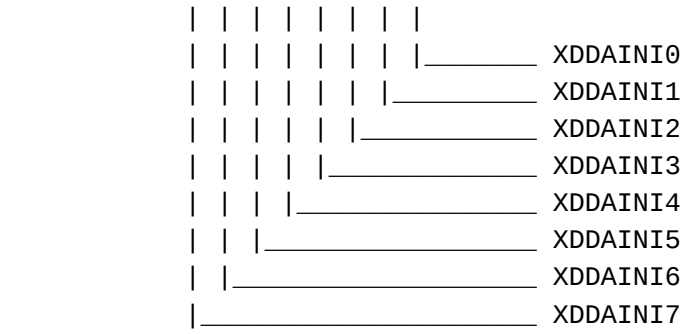
XIDVEND[10:8]: Video display vertical end high: This field will be used to determine the ending line of the vertical display line and this register should be programmed of the starting display line plus the desired display line width.

2.77 Extended X2 Video Source Window Width (3CF/J4F, R/W) (X2 Video Display Memory Offset Fetch)



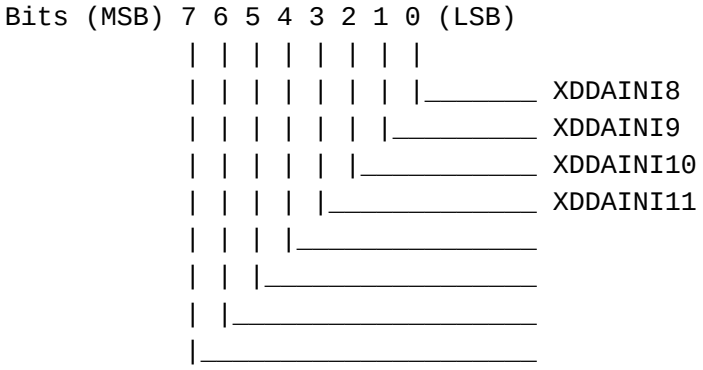
XFTHNO[7:0]: Video display fetch number low: This fetch number will determine the number of pixels which will be fetched from video memory. This field is always programmed same as OFFSET register. If register bits XPHASE[2:0] is not equal to 0, then proper value should be added to this field.

2.78 Extended X2 Video Horizontal DDA Initial Value Low (3CF/K40, R/W)



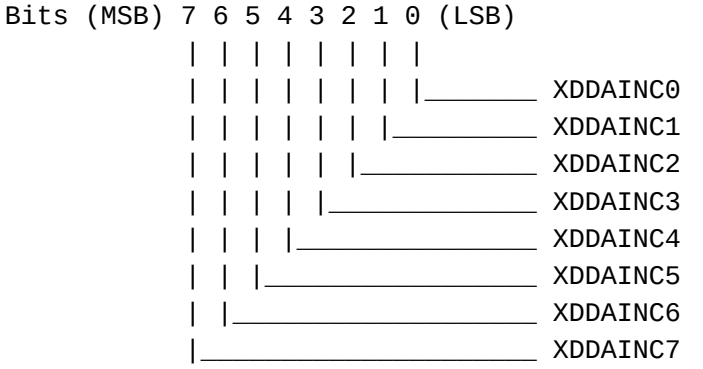
XDDAINI[7:0]: Horizontal DDA (digital differential algorithm) initial value low. (This field should be set to 0800h)

2.79 Extended X2 Video Horizontal DDA Initial Value High (3CF/K41, R/W)



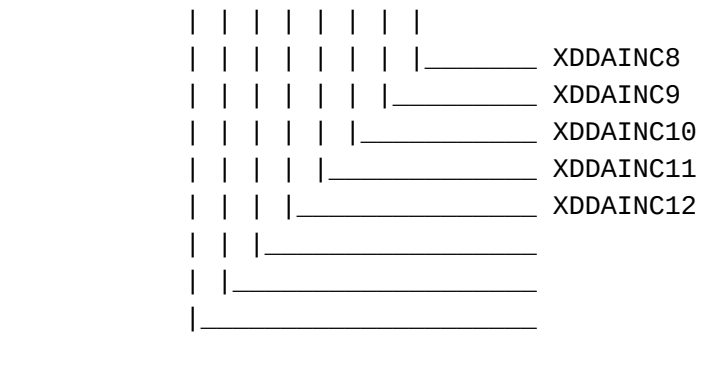
XDDAINI[11:8]: Horizontal DDA (digital differential algorithm) initial value high. (This field should be set to 0800h)

2.80 Extended X2 Video Horizontal DDA Increment Value Low (3CF/K42, R/W)



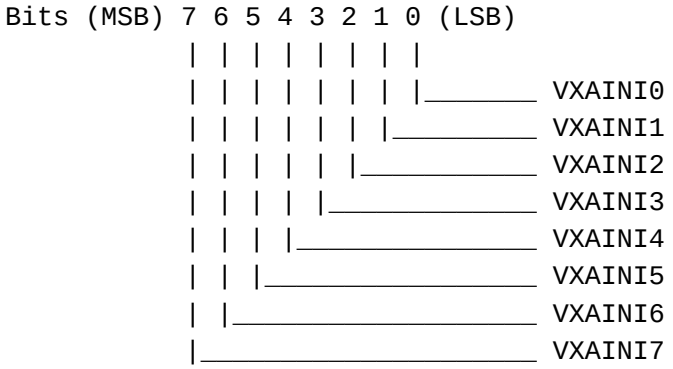
XDDAINC[7:0]: Horizontal DDA (digital differential algorithm) increment value low.

2.81 Extended X2 Video Horizontal DDA Increment Value High (3CF/K43, R/W)



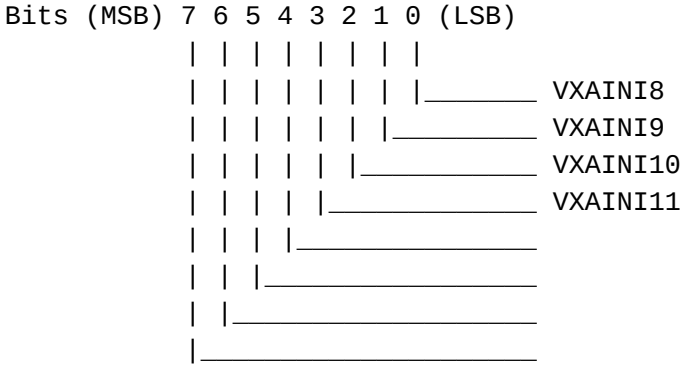
XDDAINC[12:8]: Horizontal DDA (digital differential algorithm) increment value high.

2.82 Extended X2 Video Vertical DDA Initial Value Low (3CF/K44, R/W)



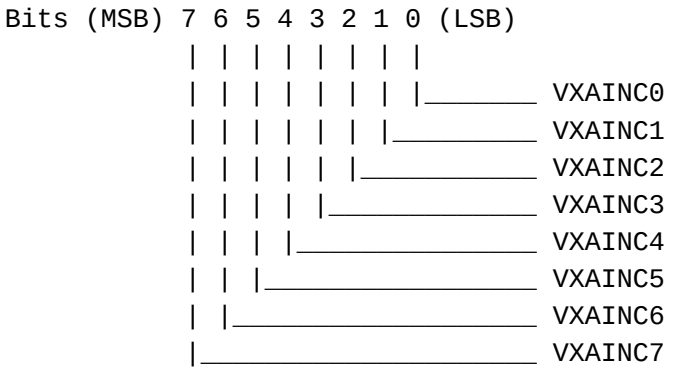
VXAINI[7:0]: Vertical DDA (digital differential algorithm) initial value low. (This field should be set to 0800h)

2.83 Extended X2 Video Vertical DDA Initial Value High (3CF/K45, R/W)



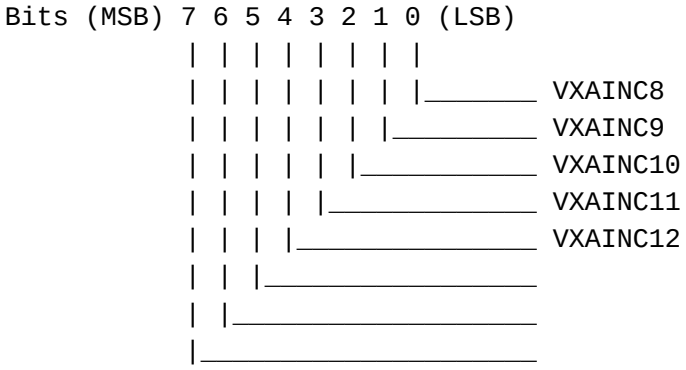
VXAINI[11:8]: Horizontal DDA (digital differential algorithm) initial value high. (This field should be set to 0800h)

2.84 Extended X2 Video Vertical DDA Increment Value Low (3CF/K46, R/W)



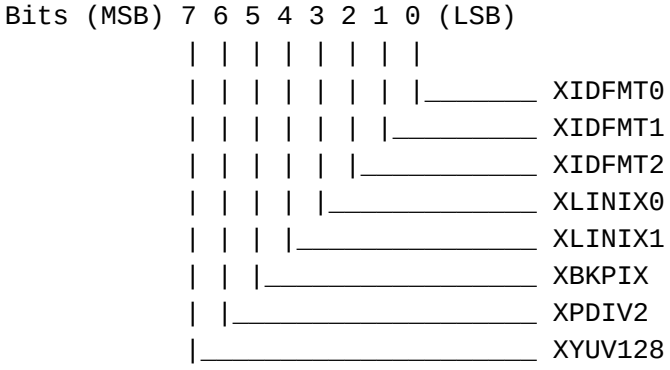
VXAINC[7:0]: Vertical DDA (digital differential algorithm) increment value low.

2.85 Extended X2 Video Vertical DDA Increment Value High (3CF/K47, R/W)



VXAINC[12:8]: Vertical DDA (digital differential algorithm) increment value high.

2.86 Extended X2 Video Format Control (3CF/K48, R/W)



XIDFMT[2:0]: Video Pixel Display Format:

XIDFMT2	XIDFMT11	XIDFMT0	# Video Input Format	
0	0	0	4 2 2 YUV	(YUVPIX)
0	0	1	5 5 5 RGB	(RG5BPIX)
0	1	0	5 6 5 RGB	(RG6BPIX)
0	1	1	24 Bits RGB	(RGB24PIX)
1	0	0	32 Bits RGB	(RGB32PIX)
1	0	1	8 Bits RGB	(RGB8PIX)
1	1	0	4 4 4 4 RGB	(RGB4PIX)
1	1	1	8T Bit RGB	(RGB8TPIX)

XLINIX[1:0]: Video Pixel Display Zoom Out Format:

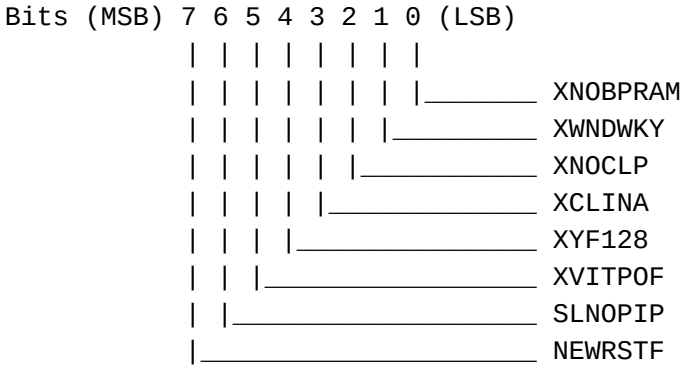
XLINIX1	XLINIX0	# Video Pixel Zoom Out Format
0	0	0.5 Linearity approach (LINHPIX)
0	1	Duplicate Previous Pixel (DUPPIX)
1	x	Reserved

XBKPIX: Third pixel go back: When this bit is set to 1 and XLINIX[1:0] is equal to 00, then the third duplicated pixel will jump back half value. When this bit is equal to 0, no effect will happened.

XPDIV2: Double horizontal display pixel: When this bit is set to 1, horizontal pixel will be duplicated.

XYUV128: YUV Data Offset 128: When this bit is equal to 1, YUV pixel data will be added 128 before any process.

2.87 Extended X2 Video Display Control I (3CF/K49, R/W)



XNOBPRAM: Video pixel not by passed internal ram : When this bit is equal to 0, pixel data will totally bypass internal RAM.

XWNDWKY: Video display use window key: When this bit is equal to 1, video display will ignore color compare register.

XNOCLP: Data process no clipping: When this bit is set to 1, video FIFO data will not be clipped to (16, 235) (16, 240).

XCLINA: U and V data process linearly: When this bit is equal to 1, U and V data will be averaged by previous U(V) and the U(V) pixel after.

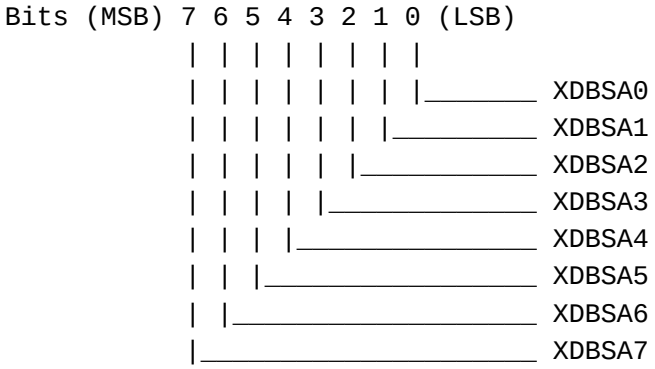
XYF128: Y Color Offset 128 enable: When this bit and XYUV128 both are set to 1, then Y color will offset by 128.

XVITPOF: Vertical interpolation off: When this bit is equal to 1, then the vertical interpolation will be turned off.

SLNOPIP: Select no pipe: When this bit is equal to 1, then capture will become one channel only.

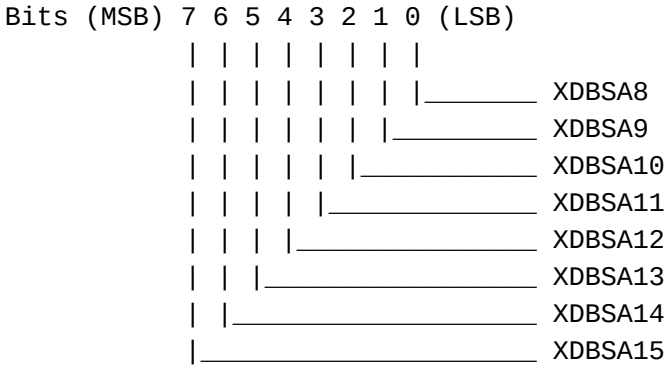
NEWRSTF: New reset for channel: When this bit is equal to 1, then the new reset signal will be VGT1RPZ.

2.88 Extended X2 Window Double Buffer Address Low (3CF/K4A, R/W)



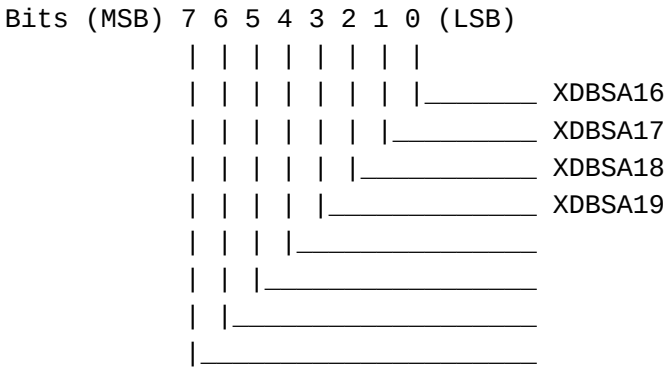
XDBSA[7:0]: Video X2 double buffer A starting address low: This field is the starting address of X2 video double buffer A.

2.89 Extended X2 Window Double Buffer Address Middle. (3CF/K4B, R/W)



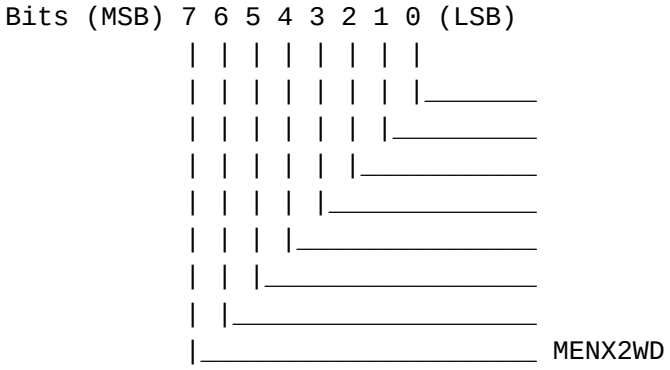
XDBSA[15:8]: Video X2 double buffer A starting address middle: This field is the starting address of X2 video double buffer A.

2.90 Extended X2 Window Double Buffer Address High (3CF/K4C, R/W)



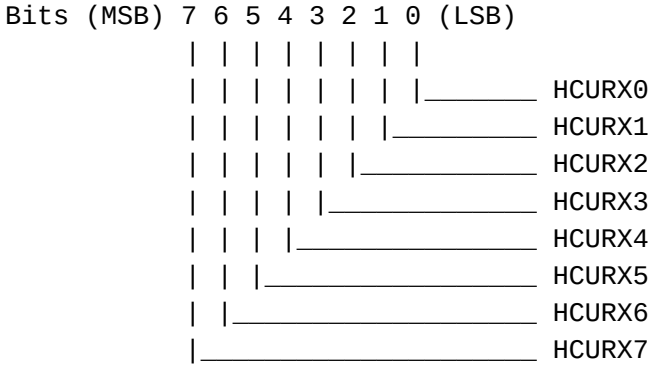
XDBSA[19:15]: Video X2 double buffer A starting address high: This field is the starting address of X2 video double buffer A.

2.91 Extended X2 Window Control I (3CF/K4D, R/W)



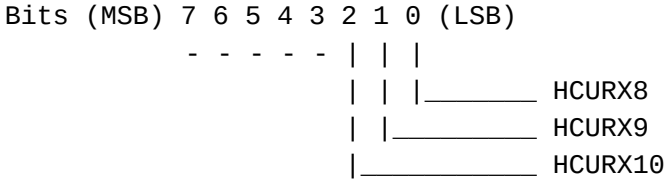
MENX2WD: Enables X2 video: When this bit is set to 1, the X2 video window will be displayed on the screen.

2.92 SPRITE HORIZONTAL START LO (3CF/50, R/W)



HCURX7-HCURX0: This register defines the low byte of the Sprite Horizontal Start value in units of pixel.

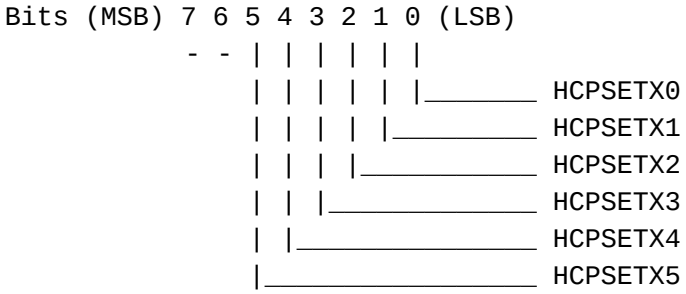
2.93 SPRITE HORIZONTAL START HI (3CF/51, R/W)



HCURX10-HCURX8: This register defines the high byte of the Sprite Horizontal Start value in units of pixel.

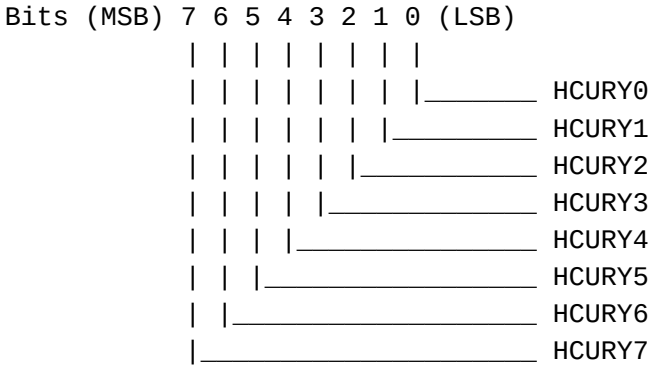
HCURX10-HCURX0: MUST be loaded as a 11 bit value in the range 000H to 07FFH.

2.94 SPRITE HORIZONTAL PRESET (3CF/52, R/W)



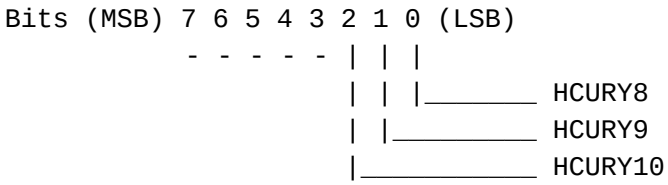
HCPSETX5-HCPSETX0: These bits define the horizontal position within the 64X64 sprite bitmap area in units of pixel at which the sprite starts. The sprite always ends at position 63 (that is, it does not wrap). If sprite is programmed to 32X32, HCPSETX5 always set to logic 1.

2.95 SPRITE VERTICAL START LO (3CF/53, R/W)



HCURY7-HCURY0: This register defines the low byte of the Sprite Vertical Start value in units of one scan line.

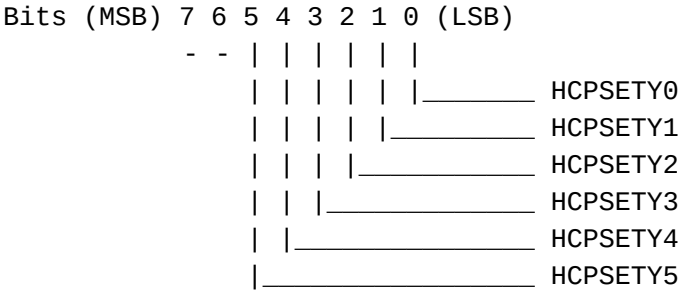
2.96 SPRITE VERTICAL START HI (3CF/54, R/W)



HCURY10-HCURY8: This register defines the high byte of the Sprite Vertical Start value in units of one scan lines.

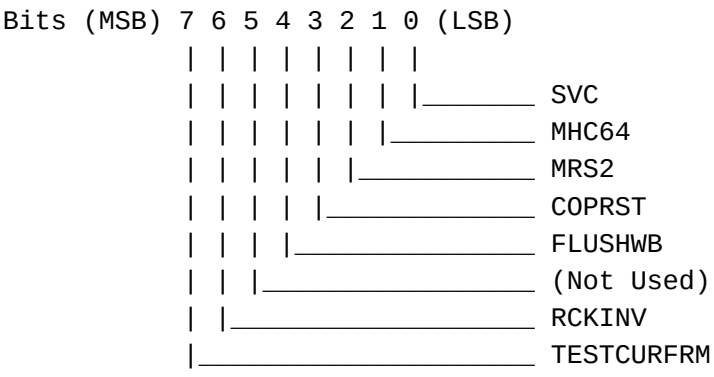
HCURY10-HCURY0: MUST be loaded as a 11 bit value in the range 000H to 7FFH.

2.97 SPRITE VERTICAL PRESET (3CF/55, R/W)



HCPSETY5-HCPSETY0: These bits define the vertical position within the 64X64 sprite bitmap area in units of one scan line at which the sprite starts. The sprite always ends at position 63 (that is, it does not wrap). If a sprite is 32X32, then bit HCPSETY5 is always set to logic 1. The 32x32 uses 256 bytes of last 1KB memory.

2.98 SPRITE CONTROL (3CF/56, R/W)



SVC: This bit defines the Sprite Visible Control. A '1' enables the sprite display on the screen at the location controlled by the sprite position control registers. A '0' disables the sprite display.

The sprite is a 64X64 pixels bitmap image, each pixel is a 2 bits and stores in sprite buffer in packeted format with Intel format. Offset address 0 is at the top left corner of the Sprite bitmap. The sprite color mapping is defined as follows:

Bit 1 0	Sprite Pixel Color Effect
0 0	Sprite Color 0
0 1	Sprite Color 1
1 0	Transparent (The underlying pixel is displayed)
1 1	Complement (1's complement of the underlying pixel is displayed)

MHC64:	Hardware Cursor 64: When this bit is equal to 1, the hardware cursor is set to 64x64 size. When this bit is equal to 0, the hardware cursor is set to 32x32 size. This bit default is to be logic 0. The hardware cursor memory map is always located at last 1KB of physical memory. For 32x32 cursor size, the hardware cursor only take the last 256 bytes of memory.
MRS2:	RAMDAC address 2 select bit.
COPRST:	Coprocessor Reset: When this bit equals 1, the coprocessor is forced to reset.
FLUSHWB:	Flush Write Buffer: When this bit equals 1, all the write buffers are clear to empty stage.
RCKINV:	When equal to 0, the pixel clock to RAMDAC is invert with VCLKSTD. When equal to 1, the pixel clock to RAMDAC is the same phase with VCLKSTD. The RAMDAC pixel clock is always operated in different phases with VIDCLK.
TESTCURFRM:	Test Cursor/Frame: When this bit set to logic 1, the VGA cursor and frame blind will toggle every other frame. For normal operation, this bit clear to logic 0.

2.99 Extended Attribute Control (3CF/57, R/W)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
                        | | |
                        | | |_______ MGREXT
                        | |_________ MTXT132
                        |___________ MPGFONT
```

MGREXT:	Graphics Extended Mode, logic 0 means the chip operates in an IBM standard mode. Logic 1, the chip works in an extended graphics mode.
MTXT132:	Text 132 Column Mode, set logic 1 to operate in 132 column text mode.
MPGFONT:	Page Font: When this bit is set, the font RAS address will locate at the low address of memory so that CRT will fetch font in page mode.

2.100 Extended Overscan Red (3CF/58 R/W)

These 8 bits are used to generate a red color border in the extended (non-IBM) mode.

2.101 Extended Overscan Green (3CF/59 R/W)

These 8 bits are used to generate a green color border in the extended (non-IBM) mode.

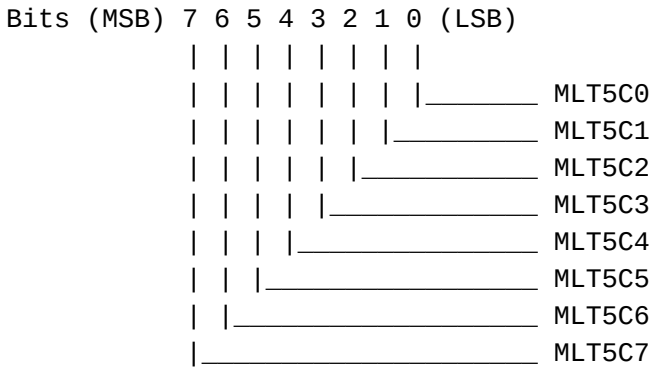
2.102 Extended Overscan Blue (3CF/5A R/W)

These 8 bits are used to generate a blue color border in the extended (non-IBM) mode.

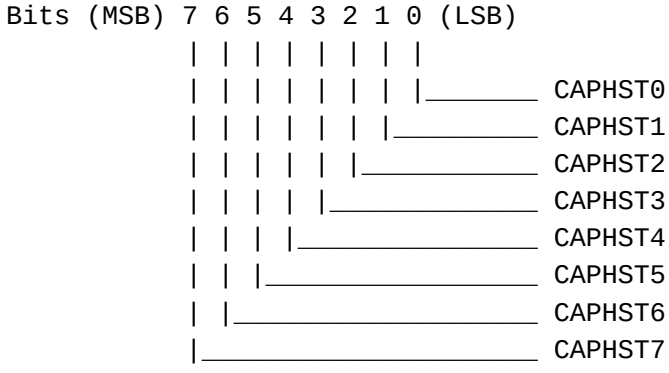
2.103 Extended COP Back Door (3CF/5B RO)

These 8 bits are reserved.

2.104 Extended RAMDAC (3CF/5C, R/W) (Reserved)

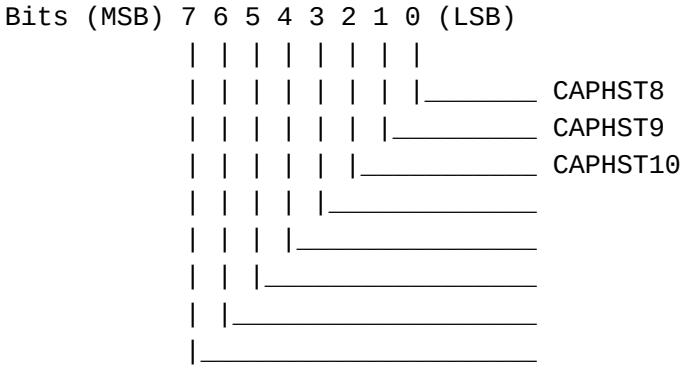


2.105 Extended Capture Horizontal Starting Low (3CF/60, R/W)



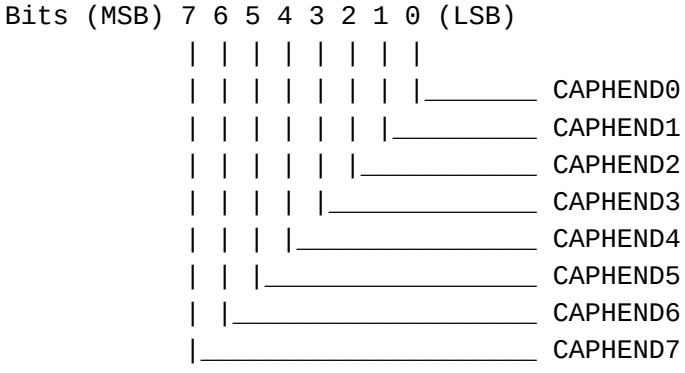
CAPHST[7:0]: Video Capture Horizontal Starting Low: This field will be used to determine the starting pixel of a horizontal capture line (16-bit capture port when using pixel boundary; 8-bit capture port when using byte boundary).

2.106 Extended Capture Horizontal Starting High (3CF/61, R/W)



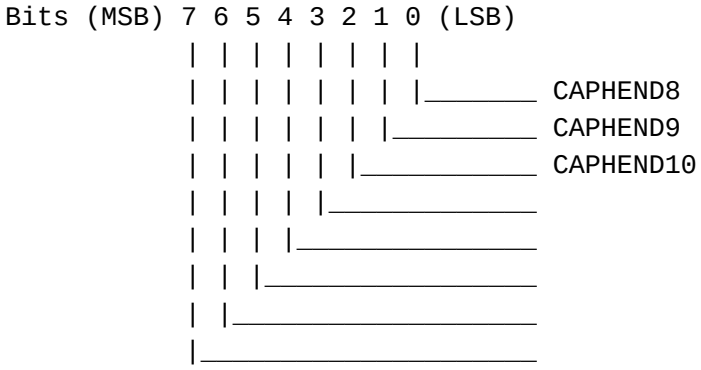
CAPHST[10:8]: Video Capture Horizontal Starting High: This field will be used to determine the starting pixel of a horizontal capture line (16-bit capture port when using pixel boundary; 8-bit capture port when using byte boundary).

2.107 Extended Capture Horizontal Ending Low (3CF/62, R/W)



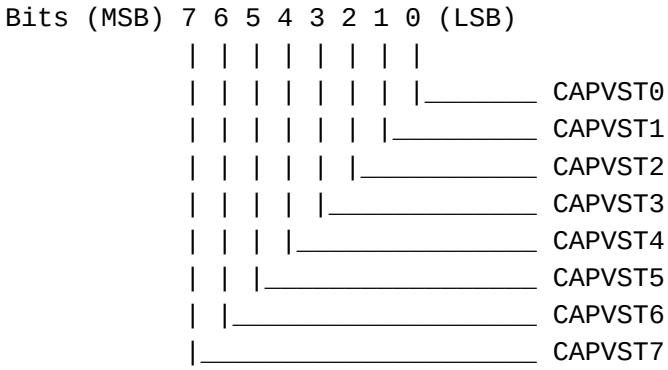
CAPHEND[7:0]: Video Capture Horizontal Ending Low: This field will be used to determine the ending pixel of a horizontal capture line (16-bit capture port when using pixel boundary; 8-bit capture port when using byte boundary).

2.108 Extended Capture Horizontal Ending High (3CF/63, R/W)



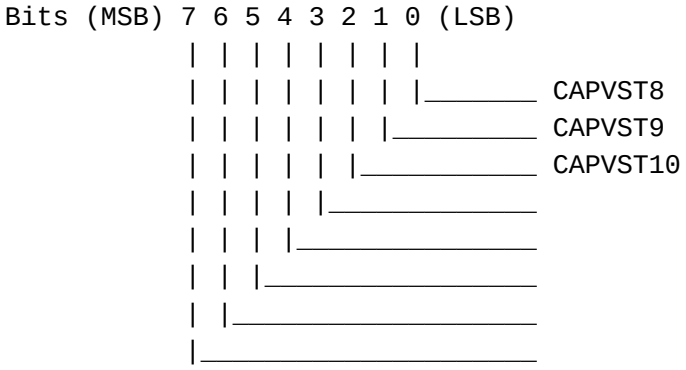
CAPHEND[10:8]: Video Capture Horizontal Ending High: This field will be used to determine the ending pixel of a horizontal capture line (16-bit capture port when using pixel boundary; 8-bit capture port when using byte boundary).

2.109 Extended Capture Vertical Starting Low (3CF/64, R/W)



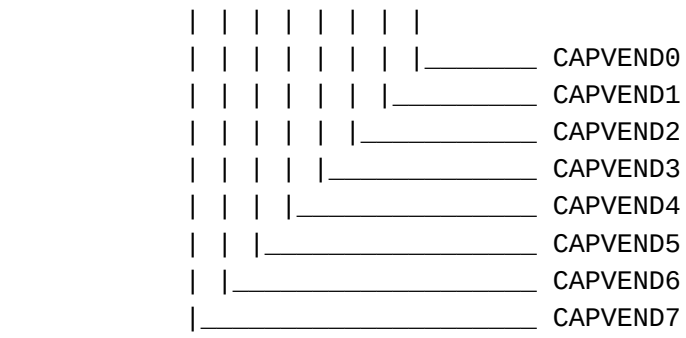
CAPVST[7:0]: Video Capture Vertical Starting Low: This field will be used to determine the starting line of a vertical capture field.

2.110 Extended Capture Vertical Starting High (3CF/65, R/W)



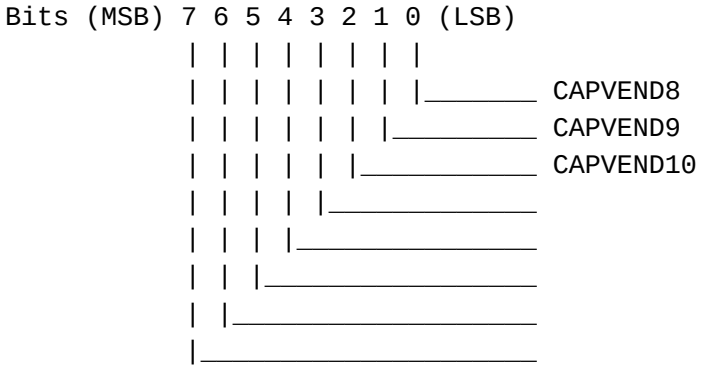
CAPVST[10:8]: Video Capture Vertical Starting High: This field will be used to determine the starting line of a vertical capture field.

2.111 Extended Capture Vertical Ending Low (3CF/66, R/W)



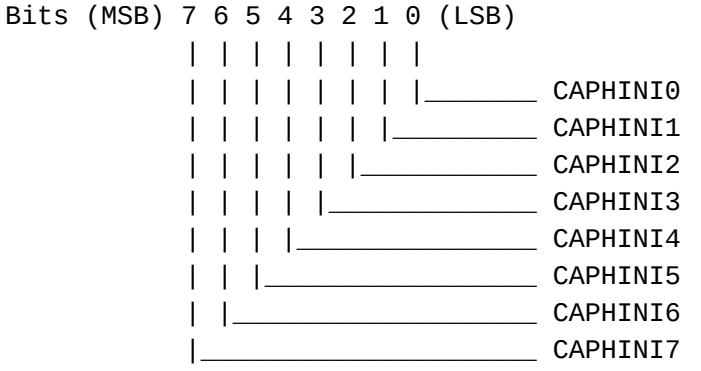
CAPVEND[7:0]: Video Capture Vertical Ending Low: This field will be used to determine the ending line of a vertical capture field.

2.112 Extended Capture Vertical Ending High (3CF/67, R/W)



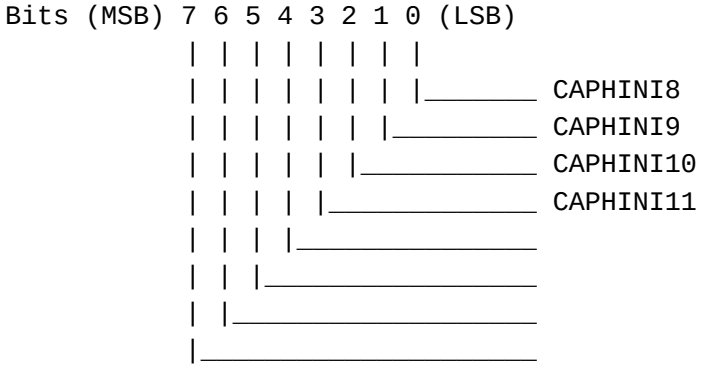
CAPVEND[10:8]: Video Capture Vertical End High: This field will be used to determine the ending line of a vertical capture field.

2.113 Extended Capture Horizontal DDA Initial Value Low (3CF/68, R/W)



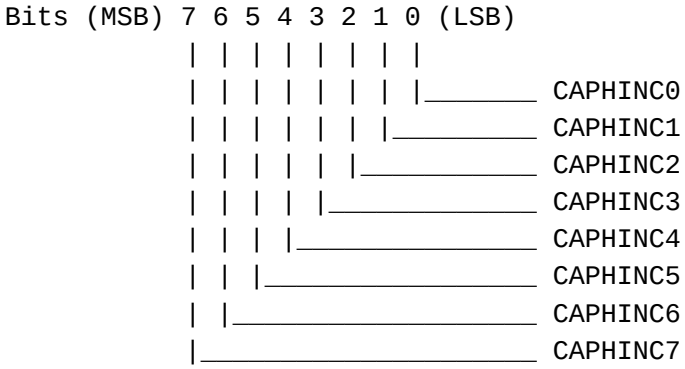
CAPHINI[7:0]: Horizontal DDA (digital differential algorithm) initial value low: This field will be set to 0800h during reset period.

2.114 Extended Capture Horizontal DDA Initial Value High (3CF/69, R/W)



CAPHINI[11:8]: Horizontal DDA (digital differential algorithm) initial value high: This field will be set to 0800h during reset period.

2.115 Extended Capture Horizontal DDA Increment Value Low (3CF/6A, R/W)

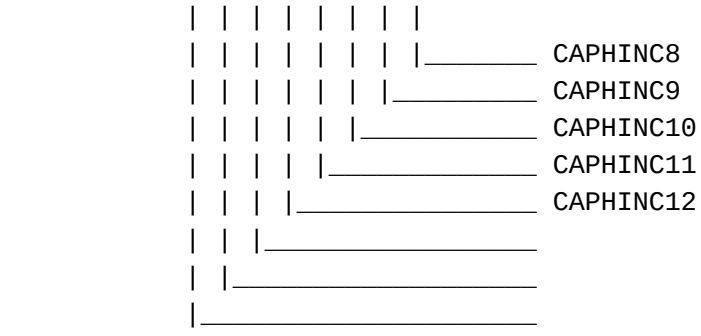


CAPHINC[7:0]: Horizontal DDA (digital differential algorithm) increment value low: The formula to calculate this field is shown below :

$$CAPHINC = \frac{(video\_pixel\_capture\_in\_memory) * 1000h + 800h - CAPHINI}{capture\_pixel\_from\_vafc}$$

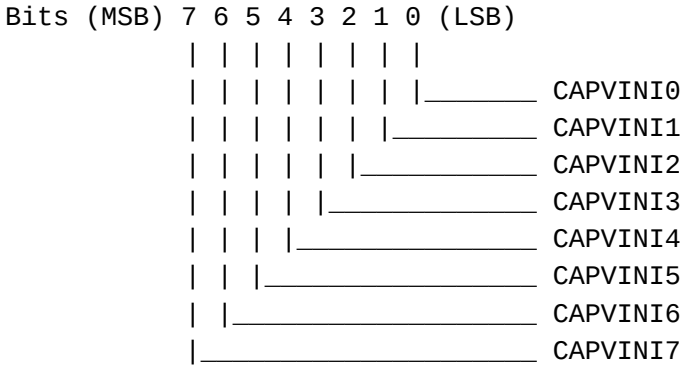
If no horizontal interpolation will be used, then this field should be programmed to 1000h.

2.116 Extended Capture Horizontal DDA Increment Value High (3CF/6B, R/W)



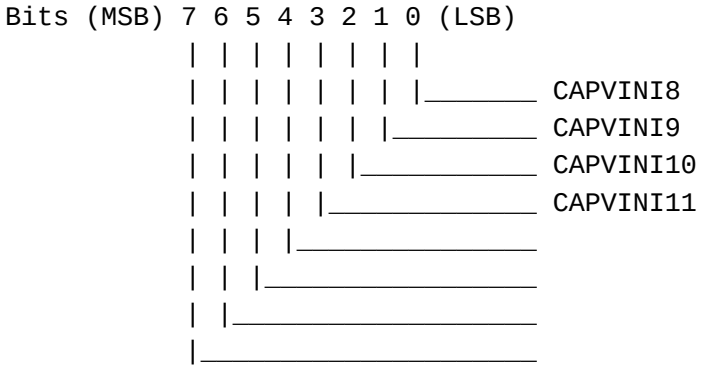
CAPHINC[12:8]: Horizontal DDA (digital differential algorithm) increment value high.

2.117 Extended Capture Vertical DDA Initial Value Low (3CF/6C, R/W)



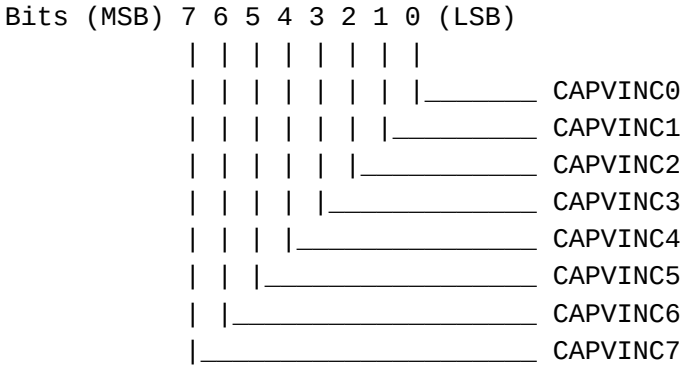
CAPVINI[7:0]: Vertical DDA (digital differential algorithm) initial value low: This field will be set to 0800h during reset period.

2.118 Extended Capture Vertical DDA Initial Value High (3CF/6D, R/W)



CAPVINI[11:8]: Horizontal DDA (digital differential algorithm) initial value high: This field will be set to 0800h during reset period.

2.119 Extended Capture Vertical DDA Increment Value Low (3CF/6E, R/W)

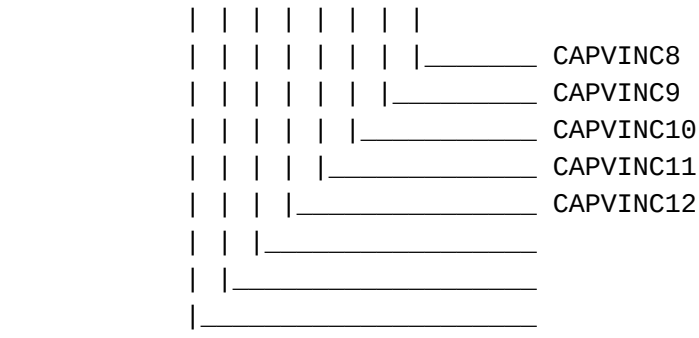


CAPVINC[7:0]: Vertical DDA (digital differential algorithm) increment value low: The formula to calculate this field is shown below :

$$CAPVINC = \frac{(video\_line\_capture\_in\_memory\ ) * 1000h + 800h - CAPVINI}{capture\_line\_from\_vafc}$$

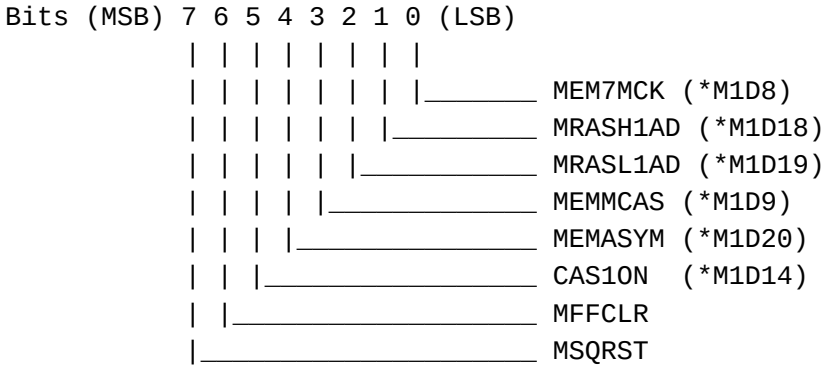
If no vertical interpolation will be used, then this field should be programmed to 1000h.

2.120 Extended Capture Vertical DDA Increment Value High (3CF/6F, R/W)



CAPVINC[12:8]: Vertical DDA (digital differential algorithm) increment value high.

2.121 Extended Memory Controller 0 (3CF/70, R/W)



MEM7KCK(*M1D8): Memory 7 MCLK: When this bit equal to 0, the Memory cycle is operated at 6 MCLK, and a memory cycle works at 7 MCLK when this signal equal to 1.

MRASH1AD: RAS Precharge Insert One Clock: When this bit is equal to logic 1, the RAS precharge time will extend one MCLK.

MRASL1AD: RAS Low To CAS Low Insert One Clock: When this bit is equal to logic 1, the RAS access time before CAS low will extend one MCLK.

MEMMCAS(*M1D9): Multiple CAS, logic 0 will set the Memory cycle in multiple WE, logic 1 lets the memory cycle executing in multiple CAS mode.

MEMASYM(*M1D13): Asymmetrical Memory Address, logic 0 arranges the Memory address in symmetrical mode, that is number of RAS and CAS addresses are equal. Logic 1 sets the Memory address in asymmetrical mode.

CAS1ON(*M1D14): CAS1 On, logic 1 means CAS1 and CAS0 have the same timing in multiple write enable configuration.

MFFCLR: FIFO Flush, set logic 1 to clear both R/W FIFO to zeroes.

This bit is clear to logic 0 for normal operation. MEMR2WPG, Memory Read To Memory Write Insert Dummy Cycle, a dummy cycle is inserted during memory read cycle to memory write cycle if this bit is set.

MSQRST: Sequencer Reset, set to logic 1 to reset Sequencer state machine asynchronously.

2.122 Extended Memory Controller 1 (3CF/71, R/W)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ MEMSP0   (*M1D15)
           | | | | | | |_________ MEMSP1   (*M1D16)
           | | | | | |___________ MEMSYNC  (*M1D17)
           | | | | |_____________ SGRAM    (*M1D23)
           | | | |_______________ MEMASYMT (*M0D19)
           | | |_________________ MEMSTY0  (*M0D16)
           | |___________________ MEMSTY1  (*M0D17)
           |_____________________ MEMSTY2  (*M0D18)
```

MEMSP[1:0](*M1D[16:15]): Memory Structure Serial/Parallel Arrangement:

MEMSP1	MEMSP0	memory chips layout structure
0	0	parallel
0	1	serial-parallel
1	0	reserved
1	1	serial

MEMSYNC(*M1D17): Synchronized Memory: When this bit is set to logic 1, a synchronized memory chips are installed. Logic 0 means normal Memory chips are in operation.

MEMTYPE(*M1D23): Memory Type, logic 0 means DRAM's are installed. Logic 1 uses VRAM's as display Memory.

MEMASYMT(*M0D19): Asymmetrical Memory Refresh Rate, logic 0 makes the asymmetrical memory refresh at 2k address range. Logic 1 uses 4k address refresh range.

MEMSTY[2:0](*M0D[18:16]): Memory Styles:

MEMSTY2	MEMSTY1	MEMSTY0	memory chip type used
0	0	X	256Kx4
0	0	X	256kx16
0	1	0	512kx8
0	1	1	1Mx16

Note * : the signal is pull-up or pull-down by the Memory data pin during system reset.

2.123 Extended Memory Controller 2 (3CF/72, R/W)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ MEMSZ0   (*M1D21)
           | | | | | | |_________ MEMSZ1   (*M1D22)
           | | | | | |___________ MEMBUSW  (*M0D23)
           | | | | |_____________ MSELADD0
           | | | |_______________ INLVCRT0
           | | |_________________ INLVCOP0
           | |___________________ MEMREFN0
           |_____________________ MEMREFN1
```

MEMSZ[1:0],(*M1D[23:22]): Memory Size:

MEMSZ1	MEMSZ0	memory size set for operation
0	0	1MB
0	1	2MB
1	0	4MB
1	1	reserved

Note * : the signal is pull-up or pull-down by the Memory data pin during system reset.

MEMBUSW(*M0D23): Memory Bus Width, logic 0 means 32-bits memory bandwidth is used. The chips works in 64-bits memory bandwidth if this bit is set to logic 1.

MSELADD0: Select Adder: When this bit is equal to 0, it uses as select adder to synchronize shift and load read pointer. Logic 1 is to select counter as synchronized shift and load read pointer.

INLVCRT0: Interleave CRT Cycle, logic 1 means interleave CRT cycle for extended mode only.

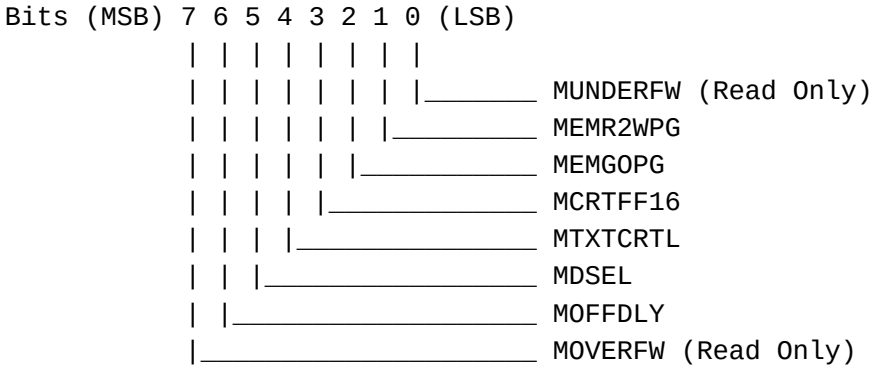
INLVCOP0: Interleave COP Cycle, logic 1 means interleave COP write cycle for extended mode only.

MEMREFN[1:0]: Memory Refresh Rate:

MEMREFN1	MEMREFN0	# of refresh cycles per scan line
0	0	3/5 default, (depend on VGA refresh bit)
0	1	1
1	0	2
1	1	4

Note * : the signal is pull-up or pull-down by the Memory data pin during system reset.

2.124 Extended Hidden Control 1 (3CF/73, R/W) (Internal Use Only)



MUNDERFW: FIFO Underflow Status Bit: When equal to 0, the FIFO operates normally. When this bit is equal to 1, an error underflow has occurred in the FIFO. This status bit is cleared at each I/O read to this register.

MEMGOPG: Memory Cycles Stay in Page: When this bit is equal to 1, the contiguous memory cycles stay in page mode.

MCRTFF16: CRT FIFO 16: When this bit is equal to 1, the 32 depth CRT FIFO becomes only 16 deep.

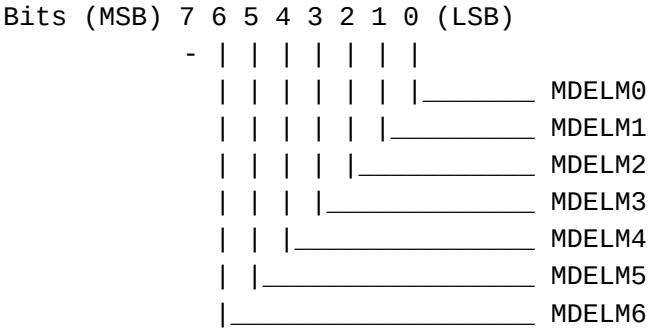
MTXTCRTL: Memory CRT/VRT Request Swap: This bit is used during video playback mode. When this bit is equal to 1, the CRT request priority will be higher than a VRT request.

MDSEL: Memory Write Data Buffer Control: When this bit is equal to 1, then the memory write data buffer will be opened a half-clock later.

MOFFDLY: FIFO Not Full: When this bit and MCFFNFUL (CF) are both equal to 1, CV FIFO will only have a high request.

MOVERFW: FIFO Overflow Status Bit: When this bit is equal to 0, the FIFO operates normally. When this bit is equal to 1, an error overflow has occurred in the FIFO. This status bit is cleared at each I/O read to this register.

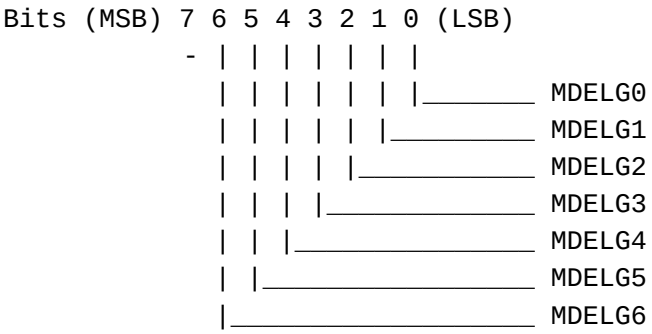
2.125 Extended FIFO Control 0 (3CF/74, R/W)



MDELM[6:0]: Delta M Value, if FIFO depth is less than or equal to delta M value, the CRT fetch has highest priority.

This register default is to be 0Bh.

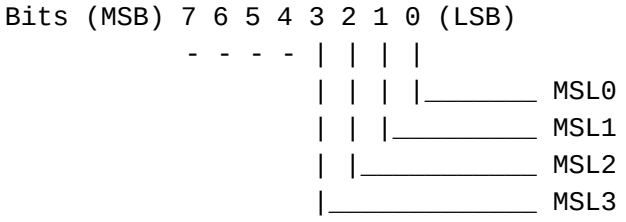
2.126 Extended FIFO Control 1 (3CF/75, R/W)



MDELG[6:0]: Delta G Value, if FIFO depth is equal to or greater than delta G value, the CRT fetch has the lowest priority.

This register default is to be 17h.

2.127 Extended SEQ Miscellaneous (3CF/77, R/W)



MSL[3:0]: These three bits control number of SL signals happen between two CCLK.

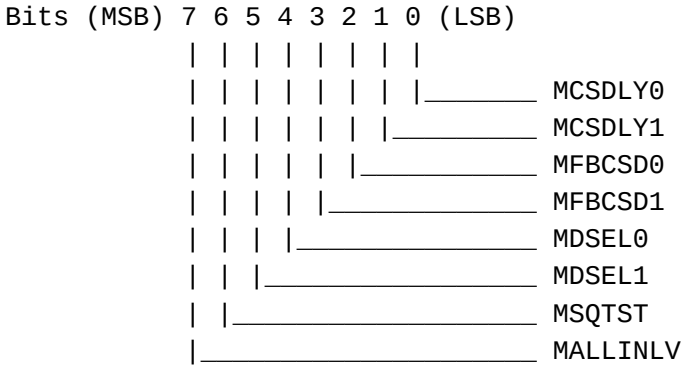
MSL3	MSL2	MSL1	MSL0	number of SL between CCLK
0	0	0	0	1 (default IBM STD)
0	0	0	1	2 8-bit/pixel
0	0	1	0	4 16-bit/pixel (5-6-5)
0	1	1	0	4 16-bit/pixel (5-5-5)
0	0	1	1	8 32-bit/pixel
0	1	0	0	6 24-bit/pixel
1	0	0	1	2 8-bit/pixel (3-3-2)
1	0	1	0	4 16-bit/pixel (4-4-4)

The following table shows the MSL[2:0] signals combines with MODE256 and SRMODE signals.

MSL3	MSL2	MSL1	MSL0	MODE256	SRMODE	Display Mode
0	0	0	0	0	0	IBM Seq mode
0	0	0	0	0	1	IBM mode 4 and 5 (CGA)
0	0	0	0	1	0	IBM 256 color mode
0	0	0	1	1	1	Extended 256 color mode
0	0	0	0	1	0 *	Extended 4bits/pixel pack mode
0	0	1	0	1	1	HiColor 16bits/pixel 5-6-5
0	1	1	0	1	1	HiColor 16bits/pixel 5-5-5
0	0	1	1	1	1	True color 32bits/pixel
0	1	0	0	1	1	True color 24bits/pixel
1	0	0	1	1	1	Extended 256 color mode 3-3-2
1	0	1	0	1	1	HiColor 16bits/pixel 4-4-4

Note * : This mode set the PELWIDTH=0 (3C0/10 BIT 6).

2.128 Extended Hidden Control 3 (3CF/79, R/W)



MCSDLY[1:0]: Controls CAS waveform to memory.

MCSDLY1	MCSDLY0	# period of delay (ns)
0	0	4 (default)
0	1	2
1	0	6
1	1	0

MFBCSD[1:0]: Controls CAS waveform feedback from memory.

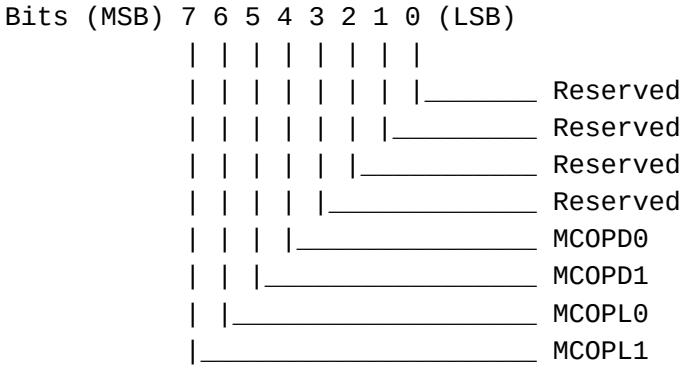
MFBCSD1	MFBCSD0	# period of delay (ns)
0	0	0 (default)
0	1	2
1	0	6
1	1	4

MDSEL[1:0]: Controls memory data latch position.

MDSEL1	MDSEL0	# latching position
0	0	tracking CAS
0	1	early to CAS
1	0	medium to CAS
1	1	late to CAS

MALLINLV: When equal to 1, coprocessor write cycle will be ALWAYS interleave operation only valid when MEMMCAS=0 and INLVCOP=1.

2.129 Extended Hidden Control 4 (3CF/7A, R/W)



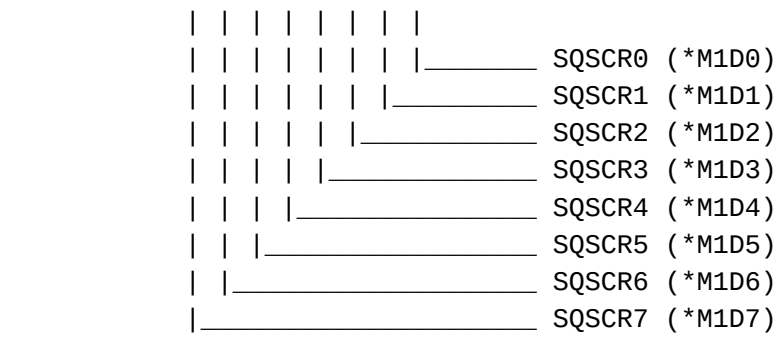
MCOPD[1:0]: Controls latch signal delay for COP cycles.

MCOPD1	MCOPD0	# period of delay (ns)
0	0	0 (default)
0	1	2
1	0	6
1	1	4

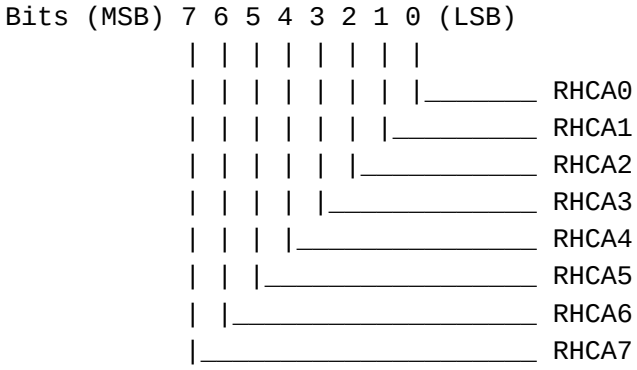
MCOPL[1:0]: COP latch signal control.

MCOPL1	MCOPL0	# latching position
0	0	tracking CAS
0	1	early to CAS
1	0	medium to CAS
1	1	late to CAS

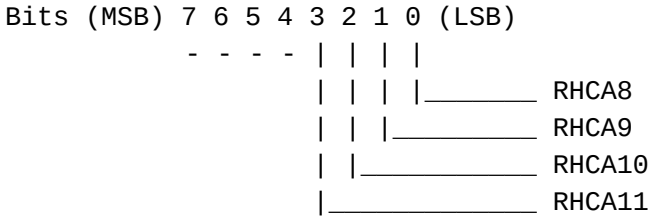
2.130 Extended Scratch Control (3CF/7B, R/W)



2.131 Sprite Data Location Low (3CF/7E R/W)

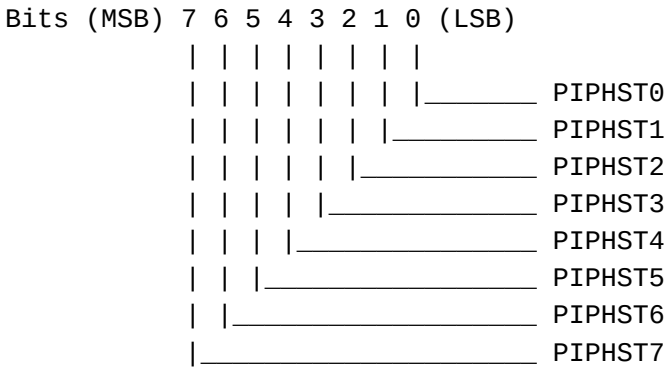


2.132 Sprite Data Location High (3CF/7F R/W)



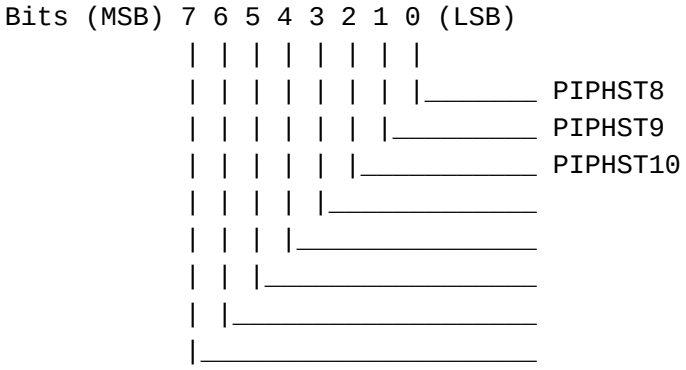
RHCA[11:0]: Hardware Cursor Data Pointer: These 12 bits are the high address bits for Hardware Cursor data location. The low 10 bits address (1KB) is the range of hardware cursor data size. The hardware cursor data can be stored anywhere in the display memory, up to 4MB, with 1KB contiguous address ranges and starting with the low 10 address bits at 0.

2.133 Extended Capture PIP Horizontal Starting Low (3CF/80, R/W)



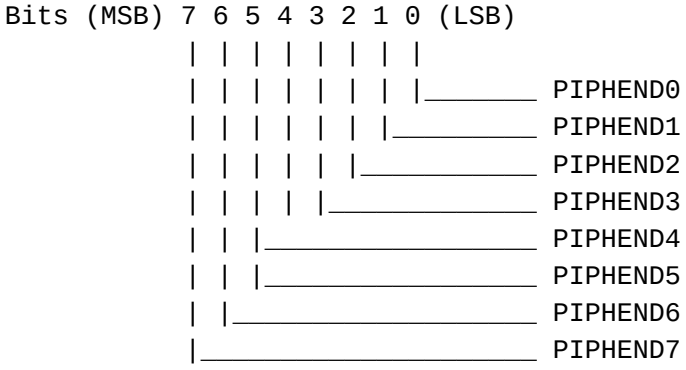
PIPHST[7:0]: Video capture horizontal pip start low: This field will be used to determine the pip starting pixel of a horizontal capture line.

2.134 Extended Capture PIP Horizontal Starting High (3CF/81, R/W)



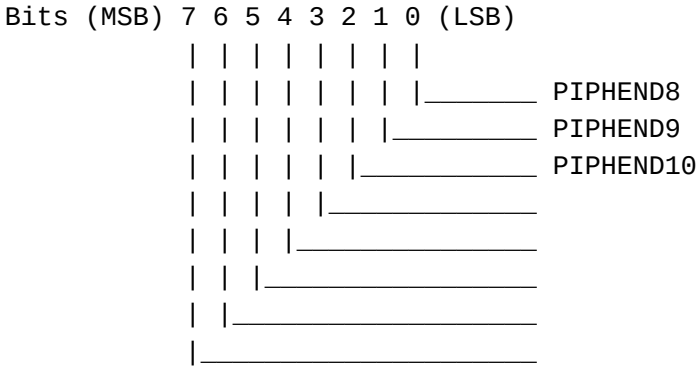
PIPHST[10:8]: Video capture horizontal pip start high: This field will be used to determine the pip starting pixel of a horizontal capture line.

2.135 Extended Capture PIP Horizontal Ending Low (3CF/82, R/W)



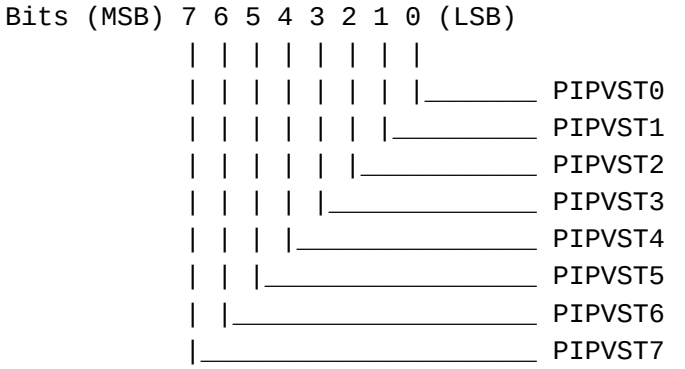
PIPHEND[7:0]: Video capture horizontal pip end low: This field will be used to determine the pip ending pixel of a horizontal capture line.

2.136 Extended Capture PIP Horizontal Ending High (3CF/83, R/W)



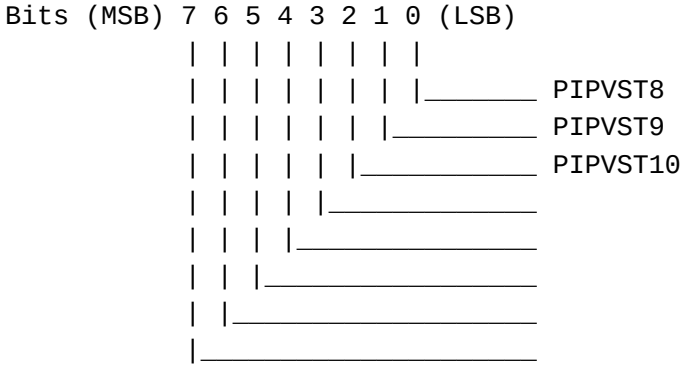
PIPHEND[10:8]: Video capture horizontal pip end high: This field will be used to determine the pip ending pixel of a horizontal capture line.

2.137 Extended Capture PIP Vertical Starting Low (3CF/84, R/W)



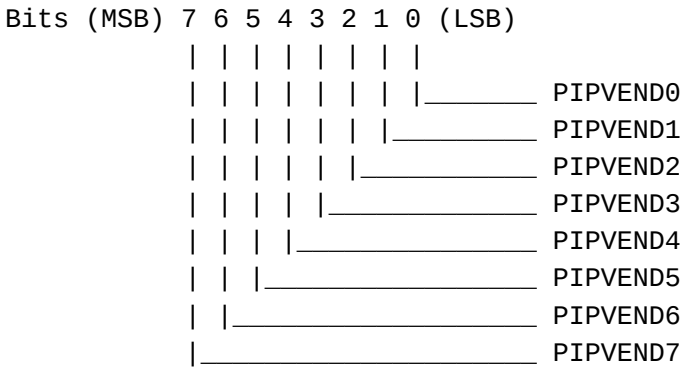
PIPVST[7:0]: Video capture vertical pip start low: This field will be used to determine the pip starting pixel of a vertical capture line.

2.138 Extended Capture PIP Vertical Starting High (3CF/85, R/W)



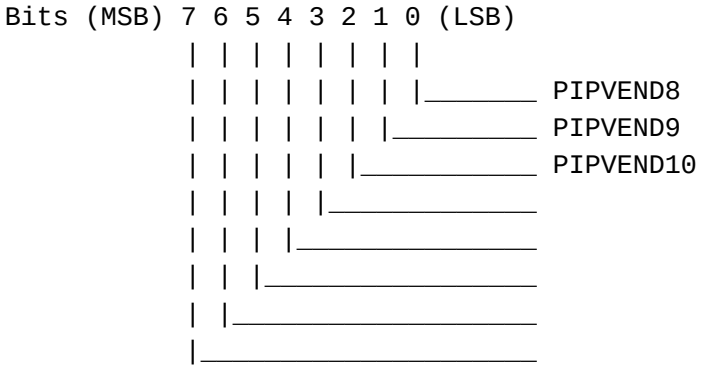
PIPVST[10:8]: Video capture vertical pip start high: This field will be used to determine the pip starting pixel of a vertical capture line.

2.139 Extended Capture PIP Vertical Ending Low (3CF/86, R/W)



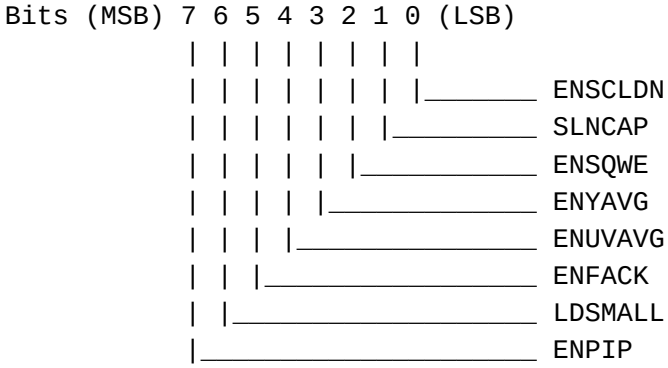
PIPVEND[7:0]: Video capture vertical pip end low: This field will be used to determine the pip ending pixel of a vertical capture line.

2.140 Extended Capture PIP Vertical Ending High (3CF/87, R/W)



PIPVEND[10:8]: Video capture vertical pip end high: This field will be used to determine the pip ending pixel of a vertical capture line.

2.141 Extended Capture New Control I (3CF/88, R/W)



ENSCLDN: When this bit is equal to 1, a new scale down logic will be used on FIFO input.

SLNCAP: When this bit is equal to 1, a new FIFO logic will be used to make an SQ request.

ENSQWE: When this bit is equal to 1, WE from FIFO will been used.

ENYAVG: When this bit is equal to 1, Y value will do color averaging.

ENUVAVG: When this bit is equal to 1, U,V values will do color averaging.

ENFACK: When this bit is equal to 1, the self-ACK will be generated during PIP and a capture freeze period.

LDSMALL: When this bit is equal to 1, each capture HDDA carry period will load a new pixel value from VAFC.

ENPIP: When this bit is equal to 1, PIP will be enables.

2.142 Extended Capture New Control II (3CF/89, R/W)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ SLODDIRQ
           | | | | | | |_________ SLOTHER
           | | | | | |___________ REQPGON
           | | | | |_____________ SLYDE1P
           | | | |_______________ NINPTD0
           | | |_________________ NINPTD1
           | |___________________ ENLOST
           |_____________________ MCAPSWPT
```

SLODDIRQ: When this bit is equal to 1, odd frame capture interrupt will be sent to system.

SLOTHER: When this bit is equal to1, "another" frame capture interrupt will be sent to system.

REQPGON: When this bit is equal to1, capture request will be in page mode.

SLYDE1P: When this bit is equal to1, YDE1FP will be used rather than VDNE1P.

NINPTD[1:0]: Delay Input Capture Data: When this bit is equal to1, then the capture data and input waveform will de delayed.

NINPTD1	NINPTD0	# delay time
0	0	4 NS
0	1	2 NS
1	0	6 NS
1	1	0 NS

ENLOST: When this bit is equal to1, video data will be read out from FIFO, regardless of SQ status when one more level of FIFO is full.

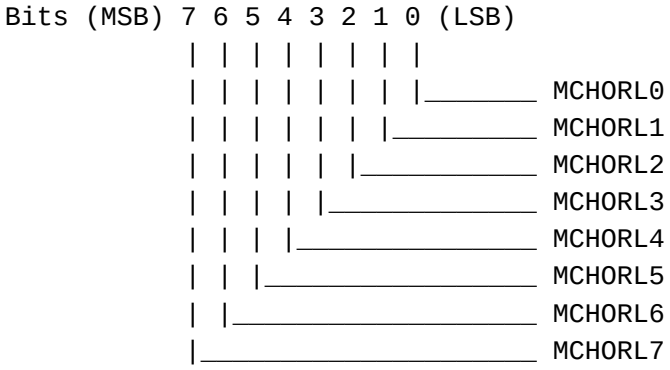
MCAPSWPT: When this bit is equal to1, CPU and CAPTURE priority is switched.

2.143 Extended Video Chroma Compare Red High (3CF/8A, R/W)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ MCHORH0
           | | | | | | |_________ MCHORH1
           | | | | | |___________ MCHORH2
           | | | | |_____________ MCHORH3
           | | | |_______________ MCHORH4
           | | |_________________ MCHORH5
           | |___________________ MCHORH6
           |_____________________ MCHORH7
```

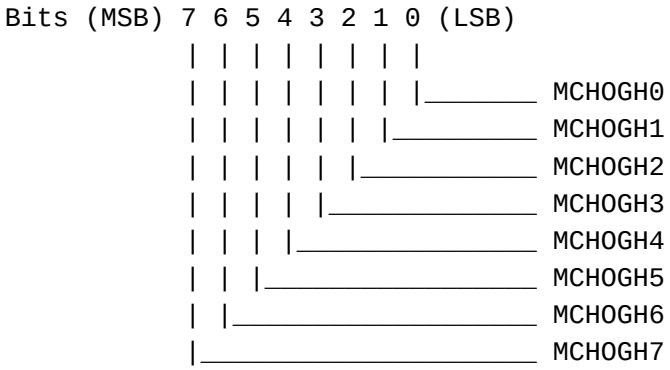
MCHORHR[7:0]: Chroma key compare red value high: When chroma key has been used, then red color index will be compared with this field.

2.144 Extended Video Chroma Compare Red Low (3CF/8B, R/W)



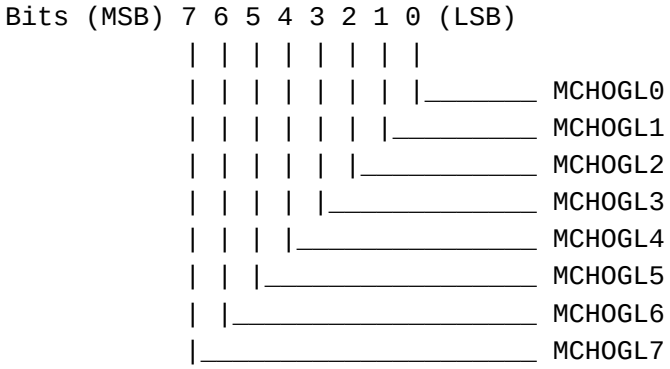
MCHORL[7:0]: Chroma key compare red value low: When chroma key has been used, then red color index will be compared with this field.

2.145 Extended Video Chroma Compare Green High (3CF/8C, R/W)



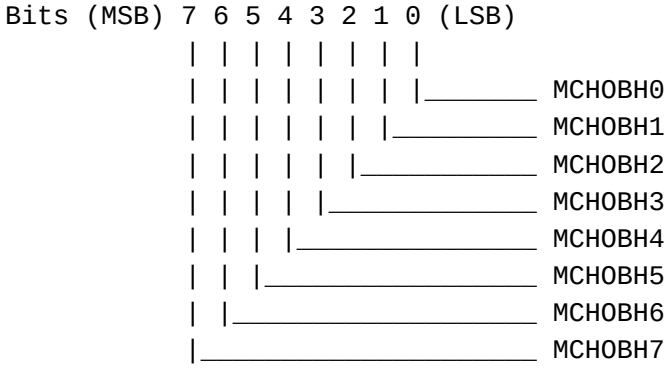
MCHOGH[7:0]: Chroma key compare green value high: When chroma key has been used, then green color index will be compared with this field.

2.146 Extended Video Chroma Compare Green Low (3CF/8D, R/W)



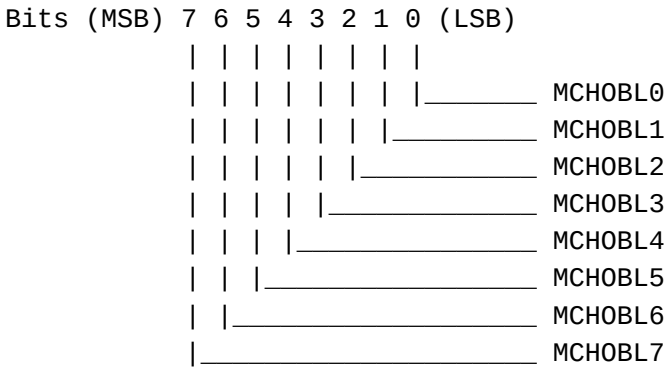
CMPG[7:0]: Chroma key compare green value low: When chroma key has been used, then green color index will be compared with this field.

2.147 Extended Video Chroma Compare Blue High (3CF/8E, R/W)



MCHOBH[7:0]: Chroma key compare blue value high: When chroma key has been used, then blue color index will be compared with this field.

2.148 Extended Video Chroma Compare Blue Low (3CF/8F, R/W)



MCHOBL[7:0]: Chroma key compare blue value low: When chroma key has been used, then blue color index will be compared with this field.

2.149 Extended Graphics Control (3CF/90, R/W)

GCEXTPATH: GC Extended Path: When this bit is zero, the GC operates in an IBM standard mode. That is all the CPU data pass through GC before write to display memory. When set this bit to logic one, the CPU data will be directly written to display memory.

WFALLFULL: This status bit is set when all write FIFO is full. This is a latched signal, and will be cleared to logic 0 when this register is read.

ALLWBEPTZ: All Write Buffer Empty: This is a read only bit. When read this bit contains logic one, some data is still in the write buffers.

2.150 Extended Chip ID 0 (3CF/91, RO)

In the CyberPro2010, this ID is A4.

2.151 Extended Chip ID 1 (3CF/92, RO)

In the CyberPro2010, this ID is 08.

2.152 Extended Chip ID 2 (3CF/93, RO)

For chip revision A, this ID is 00. For chip revision B, this ID is 01.

2.153 Extended Scratch 0 (3CF/94, R/W)

This register is reserved for software scratch pad usage.

2.154 Extended Scratch 1 (3CF/95, R/W)

This register is reserved for software scratch pad usage.

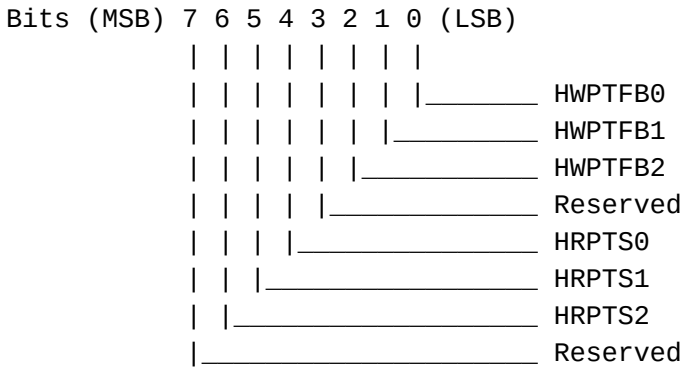
2.155 Extended Scratch 2 (3CF/96, R/W)

This register is reserved for software scratch pad usage.

2.156 Extended Scratch 3 (3CF/97, R/W)

This register is reserved for software scratch pad usage.

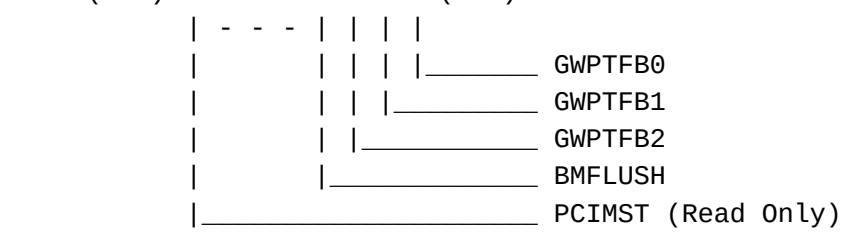
2.157 PCI Bus Master Control 0 (3CF/9C, R/W)



HWPTFB[2:0]: Host Write Pointer Full: These bits are reserved for internal use. When these bits = 000, the write pointer full signal is set when 8 rows of FIFO contain data; when these bits = 001, the write pointer full signal is set when 7 rows of FIFO contain data; etc.

HRPTS[2:0]: Host Read Pointer Start: These bits control the number of data in FIFO before starting to service the Bus Master.

2.158 PCI Bus Master Control 1 (3CF/9D, R/W)

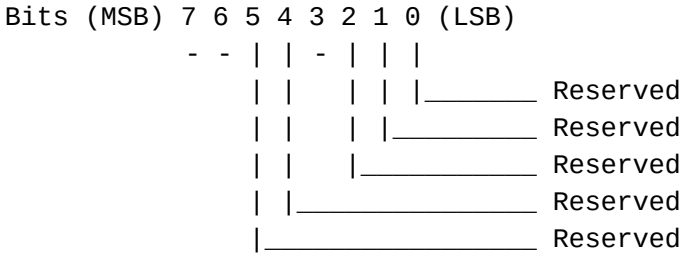


GWPTFB[2:0]: These bits are for internal use. These three bits define the Write Pointer Full signal. When equal to 0, indicates that the Write Pointer Full signal is set when 8 deep FIFO contains all data. When equal to 1, indicates that the Write Pointer Full signal is set when 7 deep of FIFO contains valid data, and so on.

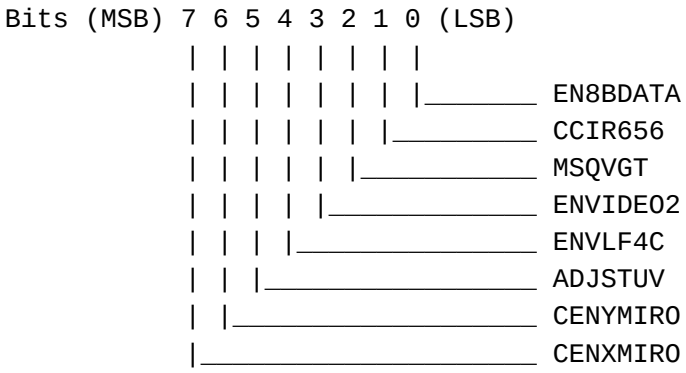
BMFLUSH: Bus Master Flush: When equal to 1, all the FIFO for Bus Master are clear to logic zero.

PCIMST: PCI MASTER is a read only bit. This bit is the same bit in PCI configuration register address 04 bit-2. When equal to 1, the PCI accepts Bus Master cycles.

2.159 Extended Write FIFO MISC (3CF/9E, R/W) (Reserved for Internal Use)



2.160 Extended CCIR656 Capture Mode I (3CF/A4, R/W)



EN8BDATA: Enables 8-bit capture mode: When this bit is equal to 1, then 8 bits video capture will be used, otherwise 16 bits capture will be used.

CCIR656: CCIR656 capture mode: When this bit is equal to 1, then video capture will use capture clock and capture data signals only. This bit should be used with 8 bit capture (EN8BDATA) together.

MSQVGT: Qualified VGT for HGT signal: When this bit is equal to 1, then VGT signal will not be used

ENVIDEO2: Enables second video source for capture: When this bit is equal to 1, then the eighth bit of incoming capture will allocated the source address which will be written into memory and the second video source address will use 3CE.A7, 3CE.A8, and 3CE.A9.

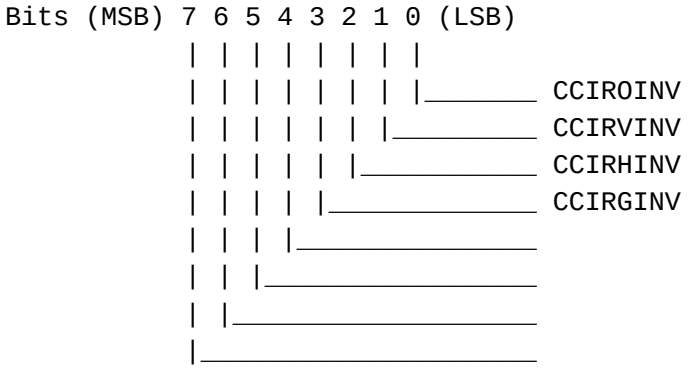
ENVLF4C: Enables new FIFO VLF for capture: When this bit is equal to 1, then the capture will use VLF FIFO instead of VSF or VLF and vertical interpolation can be used during play back period.

ADJSTUV: Adjust U,V sequence: When this bit is equal to 1, then incoming U,V sequence will be exchanged for color matching purpose.

CENYMIRO: Enables Y mirror: When this bit is equal to 1, then capture will be captured up side down for Y direction.

CENXMIRO: Enables X mirror: When this bit is equal to 1, then capture will be captured reversed in left to right direction for X axes.

2.161 Extended CCIR656 Capture Mode II (3CF/A5, R/W)



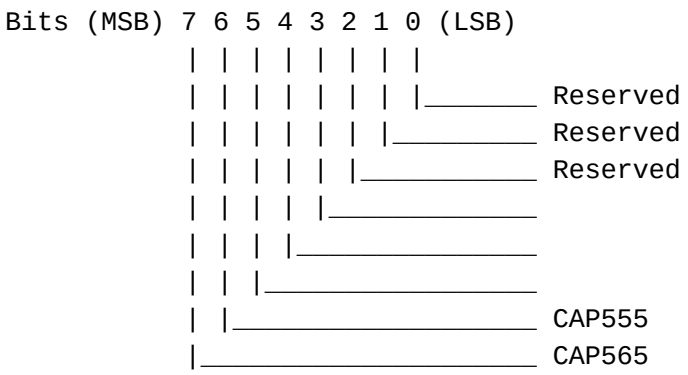
CCIROINV: Invert odd/even signal: When this bit is equal to 1, then the odd/even signal will be inverted in CCIR656 mode.

CCIRVINV: Invert VGT signal: When this bit is equal to 1, then the VGT signal will be inverted in CCIR656 mode.

CCIRHINV: Invert VGT signal: When this bit is equal to 1, then the VGT signal will be inverted in CCIR656 mode.

CCIRGINV: Invert DATAGOOD signal: When this bit is equal to 1, then the DATAGOOD signal will be inverted in CCIR656 mode.

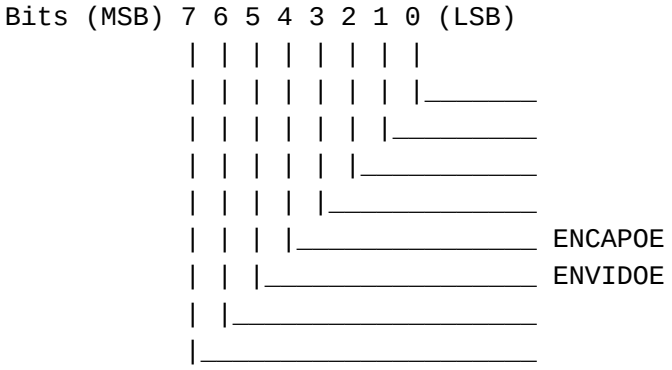
2.162 Extended Video Bus Master I (3CF/A6, R/W)



CAP555: Capture Philip RGB555 mode: When this bit is equal to 1, then 16 bits RGB555 mode will be used and only available in capture 16 bits hardware mode. i.e. 3CE.A4[0]=0

CAP565: Capture Philip RGB565 mode: When this bit is equal to 1, then 16 bits RGB565 mode will be used and only available in capture 16 bits hardware mode. i.e. 3CE.A4[0]=0

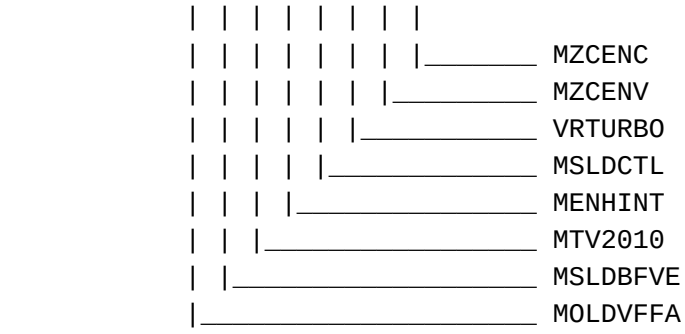
2.163 Extended Video Bus Master Address High (3CF/A9, R/W)



ENCAPOE: Capture odd/even field in two area: When this bit is equal to 1, then capture data can be put in two different space and the second area will be controlled by 3CE.A7, 3CE.A8, and 3CE.A9.

ENVIDOE: Display capture odd/Eden field double buffer: When this bit is equal to 1, then play back mode can display double buffer for capture video data.

2.164 Extended Display ZRGB Control I (3CF/AB, R/W)



MZCENC: CRT ZRGB Format Display: When this bit equals 1, then the CRT display will be set for the ZRGB 16Z-16RGB format.

MZCENV: Video ZRGB Format Display: When this bit equals 1, then the video display will be set for the ZRGB 16Z-16RGB format.

VRTURBO: Video Display in Turbo Mode: When this bit equals 1, then the video display will be set for the turbo mode.

MSLDCTL: Select Data Delay Control: When this bit equals 1, then the MUX control will match the delay for the data path.

MENHINT: Enable Horizontal Interrupt: When this bit equals 1, then every horizontal line will generate an interrupt request for each capture horizontal line.

MTV2010: Select TV2010: When this bit equals 1, then the new TV control for video FIFO will be used to handle high and true color modes.

MSLDBFVE: Select Double Buffer Control: When this bit equals 1, then the double buffer flip control will be at the vertical display end. When this bit equals 0, video display timing will be used.

MOLDVFFA: Video Fetch "Old" Method: When this bit equals 0, then the new VFFACT method will be used. When this bit equals 0, the 1682 method will be used.

2.165 Extended Double Buffer Control I (3CF/AC, R/W)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ FLIPBF
           | | | | | | |_________ ENDBUF
           | | | | | |___________ FRCESBF
           | | | | |_____________ MLOSTAT  (Read Only)
           | | | |_______________ FLIPSTAT (Read Only)
           | | |_________________ CLRFST
           | |___________________ FLIPIRQ  (Read Only)
           |_____________________ MFLPRQEN
```

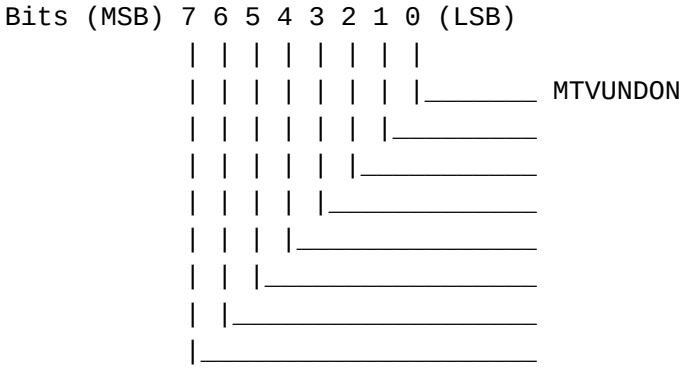
FLIPBF:	Flip Display Double Buffer: This bit is programmed by the CPU to indicate that the video path can flip the double buffer.
ENDBUF:	Enable Double Buffer: When this bit is equal to 1, then play back double buffer has been turned on.
FRCESBF:	Force Single Buffer: When this bit is equal to 1, then flip double function will always be in single buffer mode.
MLOSTAT:	Lost Status: This read only bit indicates that capture FIFO has lost data during the capture period.
FLIPSTAT:	Flip Status: When this bit is equal to 1, it indicates that hardware has flipped the double buffer already.
CLRFST:	Clear Flip Status: When this bit is equal to 1, FLIPSTAT will be cleared to zero.
FLIPIRQ:	Flip Status: When this bit is equal to 1, which indicates that hardware has flipped the double buffer already.
MFLPRQEN:	Flip Request Enable: When this bit is equal to 0, FLIPIRQ will be cleared to zero.

2.166 Extended Double Buffer Starting Address AB High (3CF/AD, R/W)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ DBSTRA16
           | | | | | | |_________ DBSTRA17
           | | | | | |___________ DBSTRA18
           | | | | |_____________ DBSTRA19
           | | | |_______________ DBSTRB16
           | | |_________________ DBSTRB17
           | |___________________ DBSTRB18
           |_____________________ DBSTRB19
```

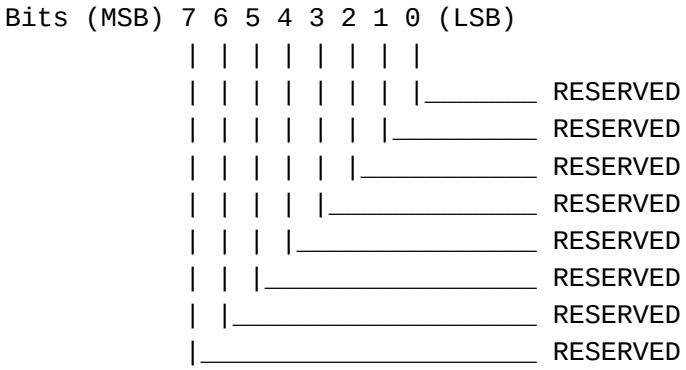
DBSTRA[19:16]:	Video Double Buffer A Starting Address High: This field is the starting address of video double buffer A.
DBSTRB[19:16]:	Video Double Buffer B Starting Address High: This field is the starting address of video double buffer B.

2.167 Extended TV Control (3CF/AE, R/W)



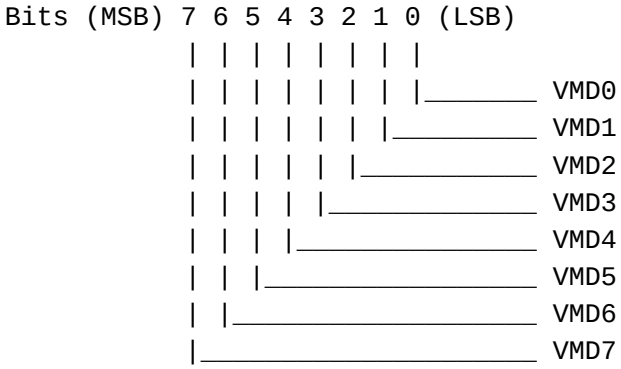
MTVUNDON: TV underscan enable: When this bit is equal to 1, then video FIFO will be used for TV underscan usage.

2.168 Extended Test Control (3CF/AF, R/W)



2.169 Extended VCLK Parameter 0 (3CF/B0, R/W)

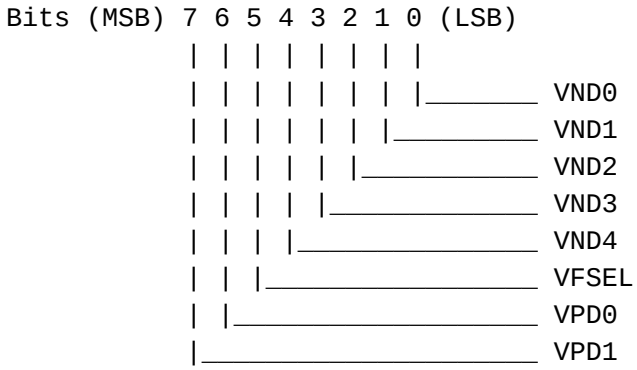
This register, along with B1 and BA, are used for VCLK.



VMD[7:0]: 8-bit Counter.

2.170 Extended VCLK Parameter 1 (3CF/B1, R/W)

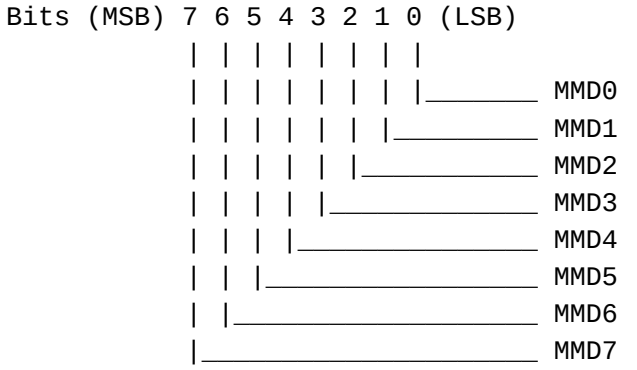
This register, along with B0 and BA, are used for VCLK.



VND[5:0]:	5-bit Counter.
VFSEL:	Video Frequency PLL Select: This bit has a default of zero.. Set to logic 1 to select different set of PLL.
VPD[1:0]:	2-bit Divider.

2.171 Extended MCLK Parameter 0 (3CF/B2, R/W)

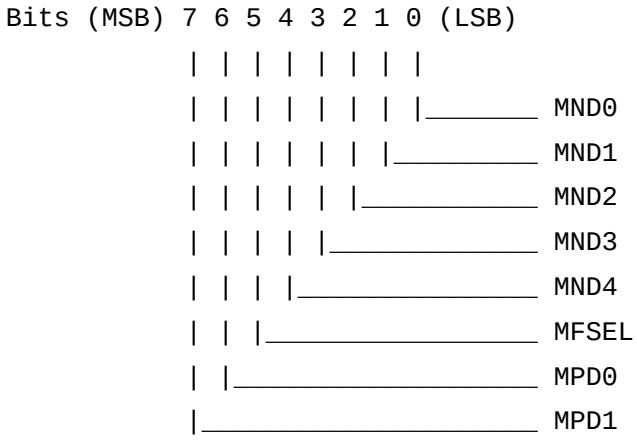
This register, along with B3 and BB, are used for MCLK.



MMD[7:0]:	8-bit Counter.

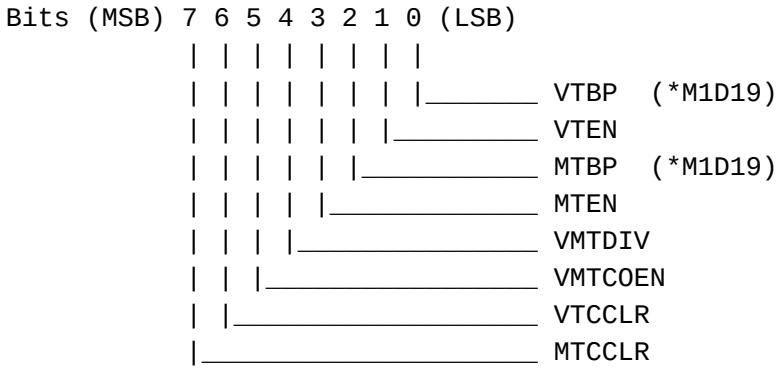
2.172 Extended MCLK Parameter 1 (3CF/B3, R/W)

This register, along with B2 and BB, are used for MCLK.



MND[4:0]:	5-bit Counter.
MFSEL:	Memory Frequency PLL Select: This bit has a default of zero. Set to logic 1 to select different set of PLL.
MPD[1:0]:	2-bit Divider.

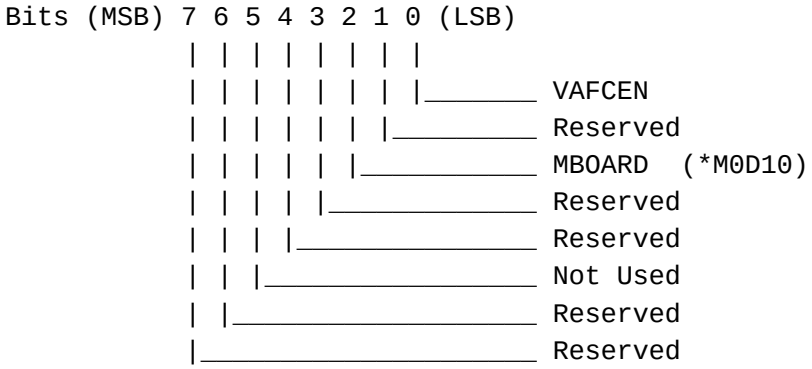
2.173 Extended Jumper Latch 0 (3CF/B4, R/W)



Bits [7:0] in this register are reserved for PLL testing.

Note * : the signal is pull-up or pull-down by the Memory data pin during system reset.

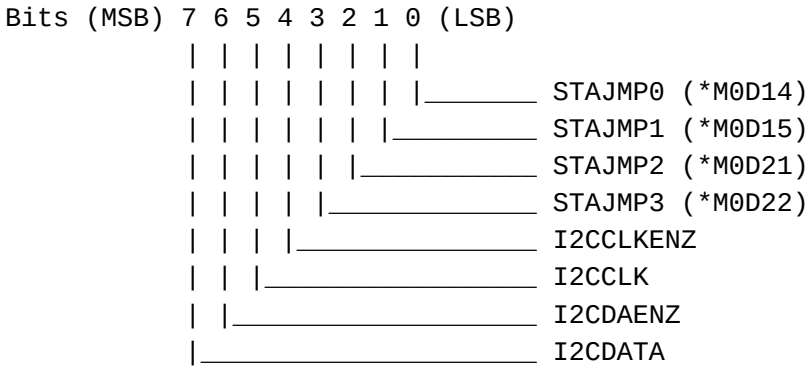
2.174 Extended Jumper Latch 1 (3CF/B5, R/W)



VAFCEN: VAFC Enable: When equal to 1, the VAFC feature is enabled.

MBOARD: Mother Board: When equal to 1, the chip is installed in a motherboard.

2.175 Extended Jumper Latch 2 (3CF/B6, R/W)



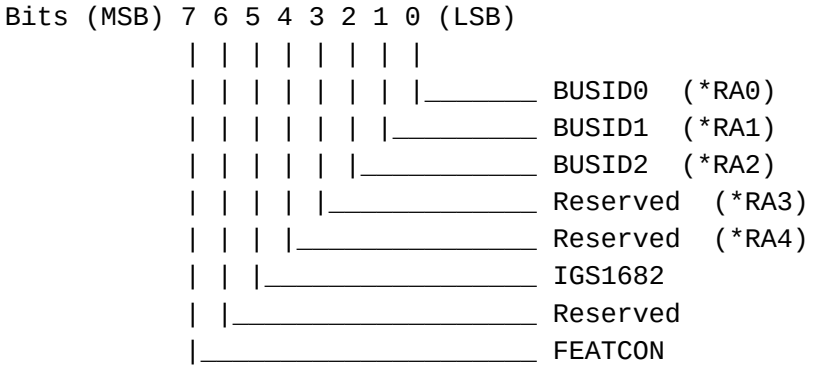
STAJMP[3:0]: These four bits readback the jumper status by software.

I2CCLKENZ, I2CCLK: I2C CLOCK: Uses I/O to control I^2C bus clock signal.

I2CDAENZ, I2CDATA: I2C DATA: Uses I/O to control I^2C bus data signal.

Note: I2CCLKENZ and I2CDAENZ are active low signals which default to logic 1 at power-up.

2.176 Extended Feature Connector (3CF/B7, R/W)



BUSID[2:0]: Bus ID: These three bits indicate the processor bus interface type. These bits are automatically set during power-up. Although these bits are R/W bits, the users are not supposed to write into these three bits. If a wrong bus type is written into these three bits, the result will be a hung bus.

BUSID2	BUSID1	BUSID0	BUSID1
0	0	0	PCI
0	0	1	NEC
0	1	0	Hitachi
0	1	1	Motorola
1	0	0	VL Standard
1	0	1	VL Linear
1	1	0	ESST
1	1	1	(Not Used)

IGS1682: IGS1682 compatibility: When this bit is equal to one, it specifies compatibility. If this bit is equal to zero, it specifies non-compatibility.

FEATCON: Feature Connector: When this is set, the feature connector is enabled on the board. This bit has a default of 1.

2.177 Extended Jumper Latch 3 (3CF/B8, R/W)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ MTYPEX    (*M1D29)
           | | | | | | |_________ SUBIDZ    (*M1D8)
           | | | | | |___________ Reserved
           | | | | |_____________ Reserved
           | | | |_______________ 9X8Y/8X9Y (*M1D12)
           | | |_________________ SPAREJ1   (*M1D13)
           | |___________________ SPAREJ2   (*M1D10)
           |_____________________ SPAREJ3   (*M1D24)
```

MTYPEX: Memory Table Select: When this bit equals 1, selects the upper table. When this bit equals 0, selects the lower table.

SUBIDZ: PCI Configuration Address (2Fh-2Ch), Subsystem ID and Subsystem Vendor ID: When pin M1D8 is pulled up with an external resistor at power-up (bit equals 1), the Subsystem ID and Subsystem Vendor ID are equal to 0. When pin M1D8 is not pulled up (internal pull-down, bit equals 0), the Subsystem ID and the Subsystem Vendor ID are stored in the second last four bytes in EPROM. This means that vendors can program their own Subsystem ID in the EPROM.

9X8Y/8X9Y: DRAM Select (For 128Kx16 Only): When this bit equals 1, indicates 9X8Y. When this bit equals 0, indicates 8X9Y.

SPAREJ1: HW/SW Monitor Detection: When this bit equals 1, indicates HW detection. When this bit equals 0, indicates SW detection.

SPAREJ2 & J3: Not Used.

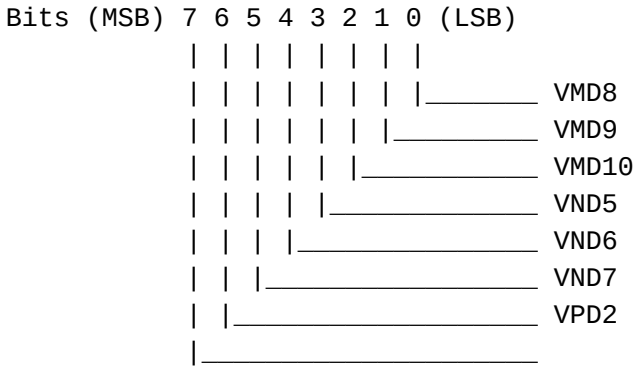
2.178 Extended MISC CLK (3CF/B9, R/W)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______
           | | | | | | |_________
           | | | | | |___________
           | | | | |_____________
           | | | |_______________
           | | |_________________
           | |___________________
           |_____________________ FRQLAT
```

MSCK2MCK: System Clock to Memory Clock, if this bit is set to logic 1, then the internal memory clock uses bus system clock frequency. This signal is used only if the bus is set to VL or PCI.

2.179 Extended VCLK Parameter 2 (3CF/BA, R/W)

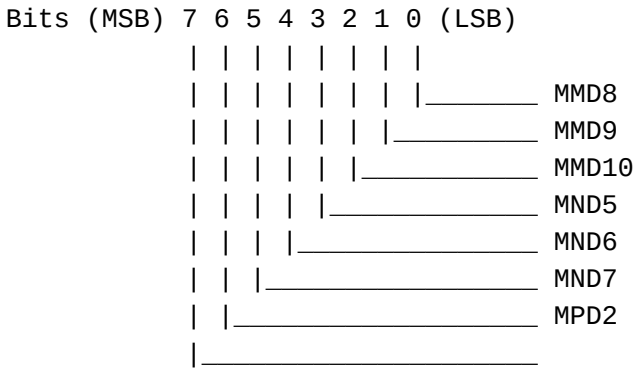
This register, along with B0 and B1, are used for VCLK.



VMD[10:8]:	3-bit Counter.
VND[7:5]:	3-bit Counter.
VPD2:	1-bit Divider.

2.180 Extended MCLK Parameter 2 (3CF/BB, R/W)

This register, along with B2 and B3, are used for MCLK.



MMD[10:8]:	3-bit Counter.
MND[7:5]:	3-bit Counter.
MPD2:	1-bit Divider.

2.181 Extended VCLK Control (3CF/BC, R/W)

This register is reserved for programming the VCLK frequency.

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ VPRST
           | | | | | | |_________
           | | | | | |_____________ SCK2VCK (*M1D19)
           | | | | |_______________ BVCKEN (*M1D19)
           | | | |_________________ 2VCKDIV2 (*M1D19)
           | | |___________________
           | |___________________
           |_____________________ CLKEXT (*M0D13)
```

2.182 Extended MCLK Control (3CF/BD, R/W)

This register is reserved for programming the MCLK frequency.

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ MPRST
           | | | | | | |_________
           | | | | | |_____________ SCK2MCK (*M1D19)
           | | | | |_______________ BMCKEN  (*M1D19)
           | | | |_________________ 2MCKP0
           | | |___________________ 2MCKP1  (*M1D19)
           | |___________________ 2MCKP2
           |_____________________ MCKLONG
```

2.183 Extended XT Control (3CF/BE, R/W)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ Reserved
           | | | | | | |_________ Reserved
           | | | | | |_____________ VIDEO16   (*M0D24)
           | | | | |_______________           (*M0D25)
           | | | |_________________ MACCHIP   (*M0D26)
           | | |___________________ Reserved
           | |___________________ Reserved
           |_____________________ Reserved
```

VIDEO16: When this bit is equal to 1, it indicates a 16-bit capture port. When this bit is equal to 0, it indicates an 8-bit capture port.

MACCHIP: When this bit is equal to 1, it indicates a Macintosh PCI bus interface.

2.184 Extended XB Control (3CF/BF, R/W)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | - - - - |
           | | |         |_______ XCKREG
           | | |_____________________
           | |_____________________ Reserved
           |_____________________ MEMTRI  (csm)
```

XCKREG: Extended Clock Generator Register: When equal to 0, the first set of the index register 3CE from B0 to B7 is accessible. When equal to 1, the second set of the index register 3CE from B0 (XB0) to B7 (XB7) is accessible.

MEMTRI: Memory Tri-state: At power-up, this bit has a default value of logic 1 if the Flexibus® is being used. After power-up, in order to start the DRAM cycle, this bit needs to be programmed to a value of logic 0.

2.185 Extended Programmable Bit 0 (3CF/XB0, R/W)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ P24EN (Refer to Figure 2-2)
           | | | | | | |_________ P24DU (Refer to Figure 2-2)
           | | | | | |___________ P24DI (Refer to Figure 2-2)
           | | | | |_____________ (Not Used)
           | | | |_______________ P31EN
           | | |_____________________ P31DU
           | |_____________________ P31DI
           |_____________________ (Not Used)
```

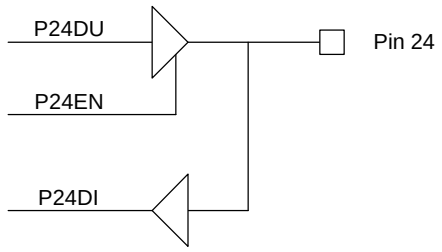


Figure 2-2: Pin 24 Logic Diagram

2.186 Extended Programmable Bit 1 (3CF/XB1, R/W)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ P41EN
           | | | | | | |_________ P41DU
           | | | | | |___________ P41DI
           | | | | |_____________ VSTEREO
           | | | |_______________ P43EN
           | | |_________________ P43DU
           | |___________________ P43DI
           |_____________________ (Not Used)
```

VSTEREO: Vertical Sync Stereo, in order to get the vertical sync stereo output at pin_41 (EPA10), both P41EN(bit_0) and VSTEREO (bit_3) must be set to logic 1, and P41DU(bit_1) must be cleared to logic 0. Then the pin_41 will be toggled at every raising edge of vertical sync.

2.187 Extended Programmable Bit 2 (3CF/B2, R/W)

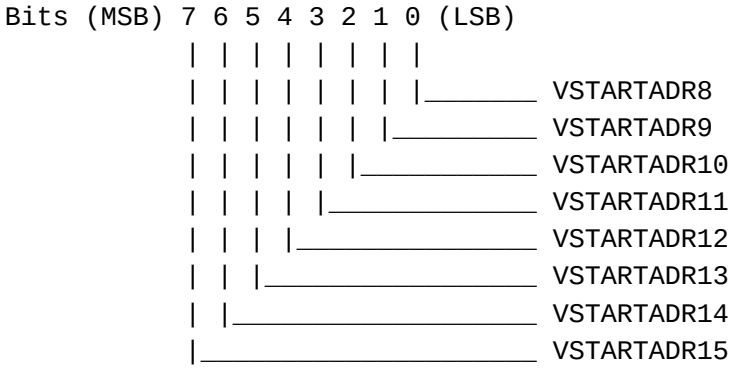
```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ P44EN
           | | | | | | |_________ P44DU
           | | | | | |___________ P44DI
           | | | | |_____________ (Not Used)
           | | | |_______________ P46EN
           | | |_________________ P46DU
           | |___________________ P46DI
           |_____________________ (Not Used)
```

2.188 Extended Video Memory Starting Address Low (3CF/C0, R/W)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ VSTARTADR0
           | | | | | | |_________ VSTARTADR1
           | | | | | |___________ VSTARTADR2
           | | | | |_____________ VSTARTADR3
           | | | |_______________ VSTARTADR4
           | | |_________________ VSTARTADR5
           | |___________________ VSTARTADR6
           |_____________________ VSTARTADR7
```

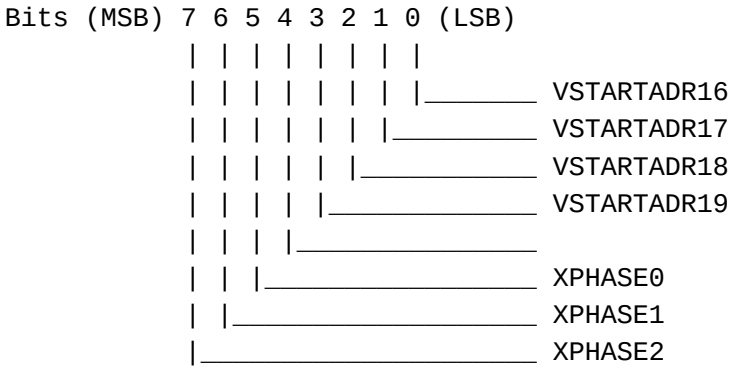
VSTARTADR[7:0]: Video starting address low: This address field will be defined as video display starting address.

2.189 Extended Video Memory Starting Address Middle (3CF/C1, R/W)



VSTARTADR[15:8]: Video starting address middle: This address field will be defined as video display starting address.

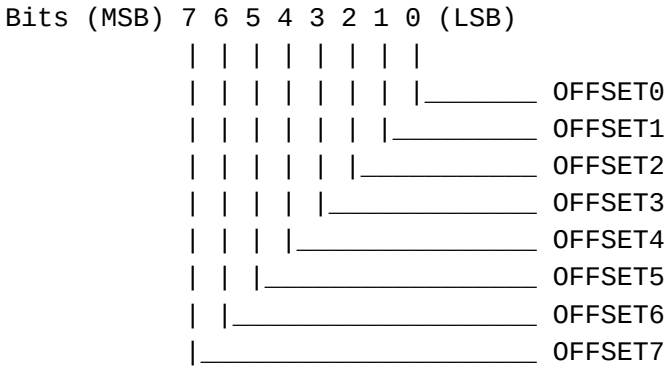
2.190 Extended Video Memory Starting Address High (3CF/C2, R/W)



VSTARTADR[19:16]: Video starting address HIGH: This address field will be defined as video display starting address.

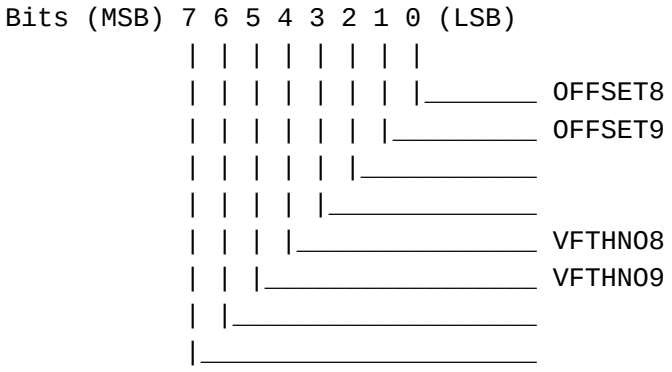
XPHASE[2:0]: Horizontal phase offset: These three bits will control horizontal video "pixel" offset value from 0 to 7.

2.191 Extended Video Source Map Width Low (3CF/C3, R/W) (Video Memory Fetch Pitch Low)



OFFSET[7:0]: Video map width low: This offset value will control video display next line starting address.

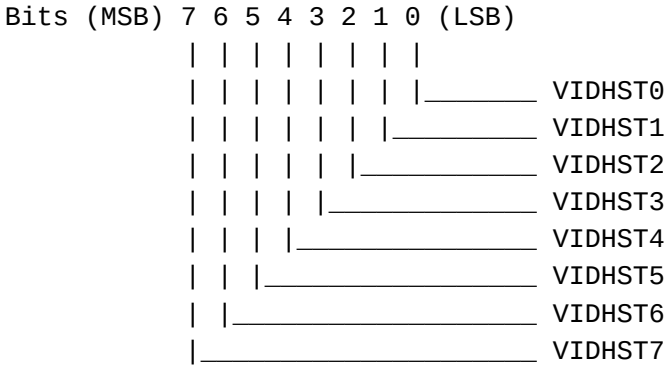
2.192 Extended Video Memory SRC Map and SRC Window Width High (3CF/C4, R/W) (Video Memory Fetch Pitch High)



OFFSET[9:8]: Video map width high: This offset value will control video display next line starting address.

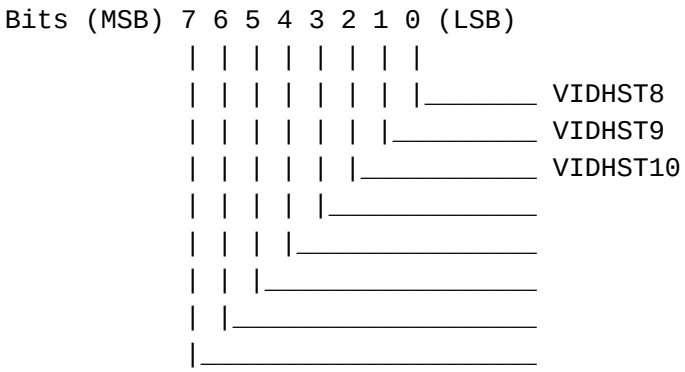
VFTHNO[9:8]: Video display fetch number high: This fetch number will determine the number of pixels which will be fetched from video memory. This field is always programmed same as OFFSET register.

2.193 Extended Video Display Horizontal Starting Pixel Low (3CF/C5, R/W)



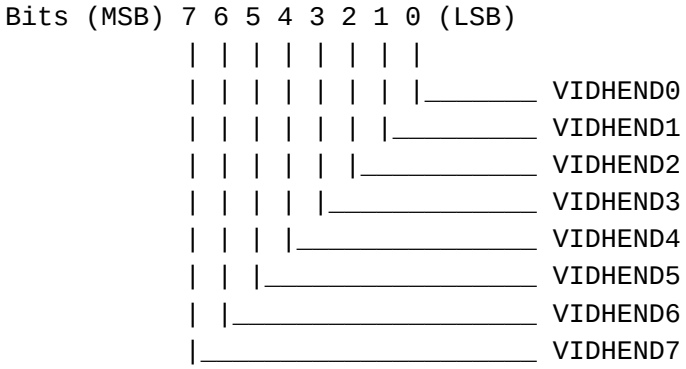
VIDHST[7:0]: Video display horizontal start low: This field will be used to determine the starting pixel of a horizontal display line and the first pixel should be programmed to 0.

2.194 Extended Video Display Horizontal Starting Pixel High (3CF/C6, R/W)



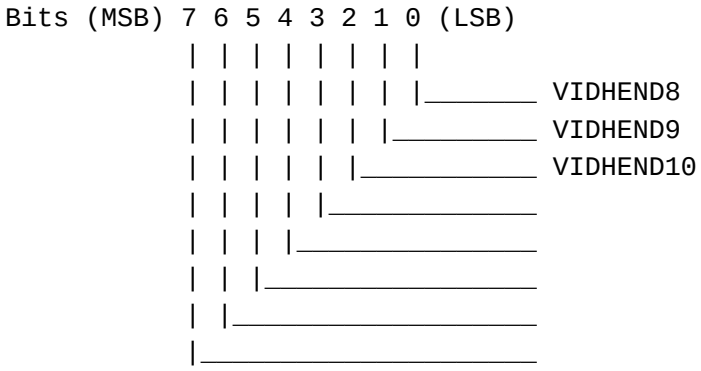
VIDHST[10:8]: Video display horizontal start high: This field will be used to determine the starting pixel of a horizontal display line and the first pixel should be programmed 0.

2.195 Extended Video Display Horizontal Ending Pixel Low (3CF/C7, R/W)



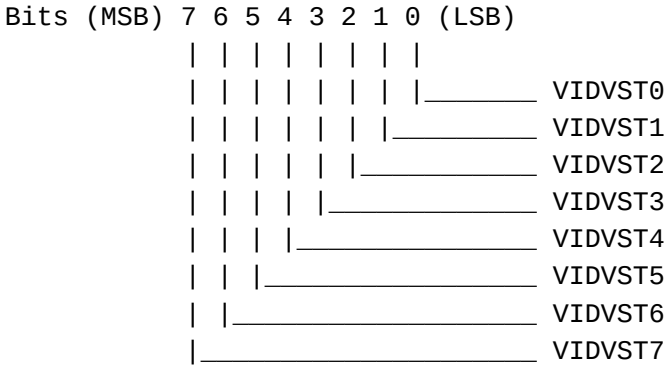
VIDHEND[7:0]: Video display horizontal end low: This field will be used to determine the ending pixel of a horizontal display line and this register should be programmed of the starting pixel plus the desired display pixel width. For example, if the starting pixel = 0Ah and the display pixel width = 10h, then this field should be 0Ah+10h = 1Ah.

2.196 Extended Video Display Horizontal Ending Pixel High (3CF/C8, R/W)



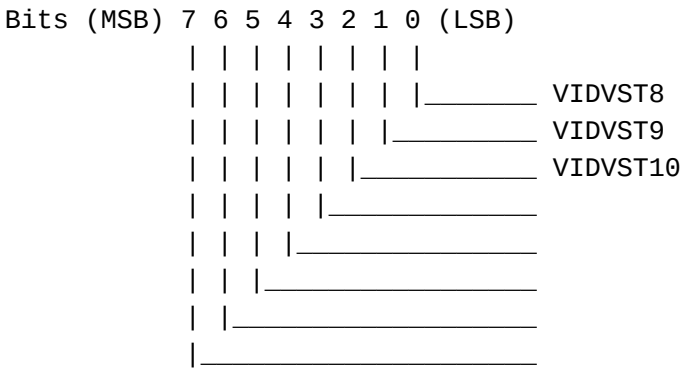
VIDHEND[10:8]: Video display horizontal end high: This field will be used to determine the ending pixel of a horizontal display line and this register should be programmed of the starting pixel plus the desired display pixel width. For example, if the starting pixel = 0Ah and the display pixel width = 10h, then this field should be 0Ah+10h = 1Ah.

2.197 Extended Video Display Vertical Starting Line Low (3CF/C9, R/W)



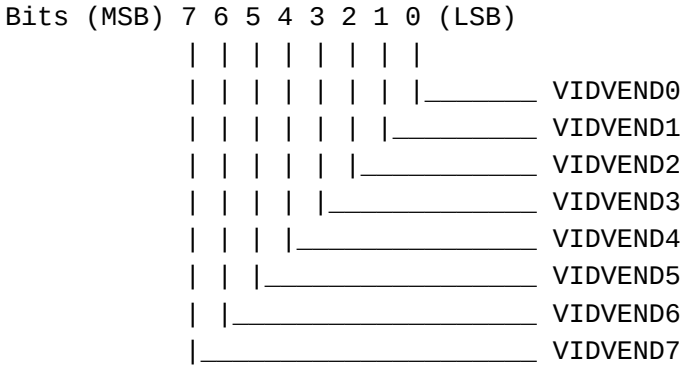
VIDVST[7:0]: Video display vertical start low: This field will be used to determine the starting line of the vertical display line and the first display line should be programmed to 0.

2.198 Extended Video Display Vertical Starting Line High (3CF/CA, R/W)



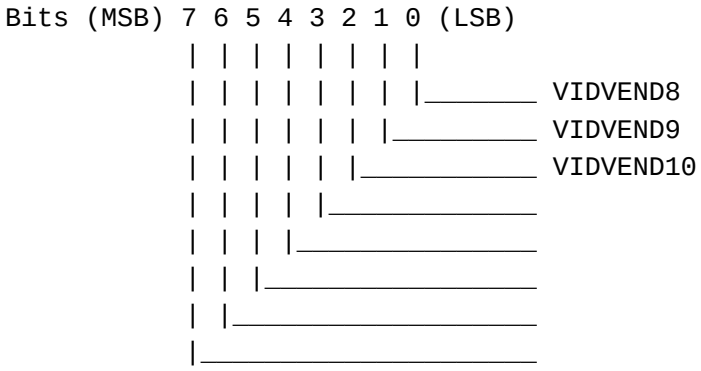
VIDVST[10:8]: Video display vertical start high: This field will be used to determine the starting line of the vertical display line and the first display line should be programmed to 0.

2.199 Extended Video Display Vertical Ending Line Low (3CF/CB, R/W)



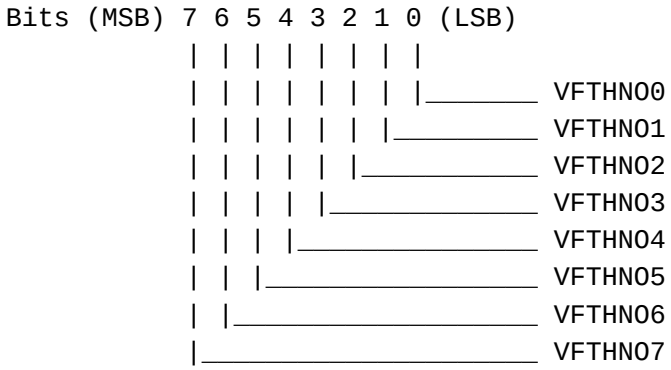
VIDVEND[7:0]: Video display vertical end low: This field will be used to determine the ending line of the vertical display line and this register should be programmed of the starting display line plus the desired display line width.
For example, if the starting pixel = 0Ah and the display pixel width = 10h, then this field should be 0Ah+10h = 1Ah.

2.200 Extended Video Display Vertical Ending Line High (3CF/CC, R/W)



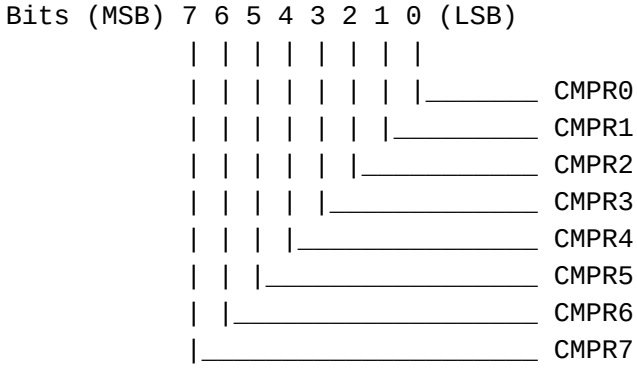
VIDVEND[10:8]: Video display vertical end high: This field will be used to determine the ending line of the vertical display line and this register should be programmed of the starting display line plus the desired display line width.
For example, if the starting pixel = 0Ah and the display pixel width = 10h, then this field should be 0Ah+10h = 1Ah.

2.201 Extended Video Source Window Width (3CF/CD, R/W) (Video Display Memory Offset Fetch)



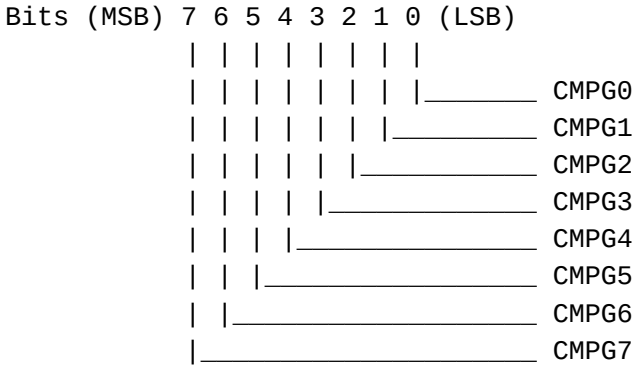
VFTHNO[7:0]: Video display fetch number low: This fetch number will determine the number of pixels which will be fetched from video memory. This field is always programmed the same as the OFFSET register. If the register bits XPHASE[2:0] are not equal to 0, then the proper value should be added to this field.

2.202 Extended Video Color Compare Red (3CF/CE, R/W)



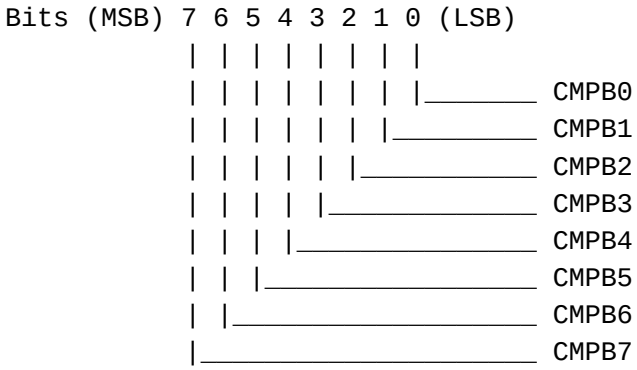
CMPR[7:0]: Color key compare red value: When color key has been used, then red color index will be compared with this field.

2.203 Extended Video Color Compare Green (3CF/CF, R/W)



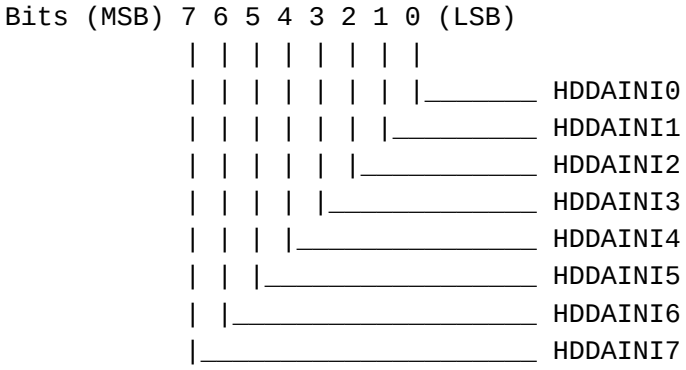
CMPG[7:0]: Color key compare green value: When color key has been used, then green color index will be compared with this field.

2.204 Extended Video Color Compare Blue (3CF/D0, R/W)



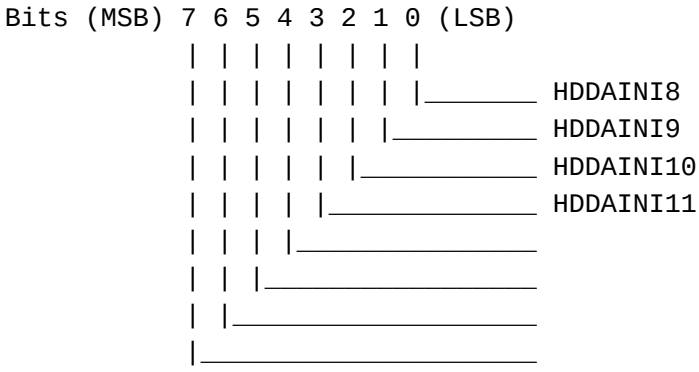
CMPB[7:0]: Color key compare blue value: When color key has been used, then blue color index will be compared with this field.

2.205 Extended Video Horizontal DDA Initial Value Low (3CF/D1, R/W)



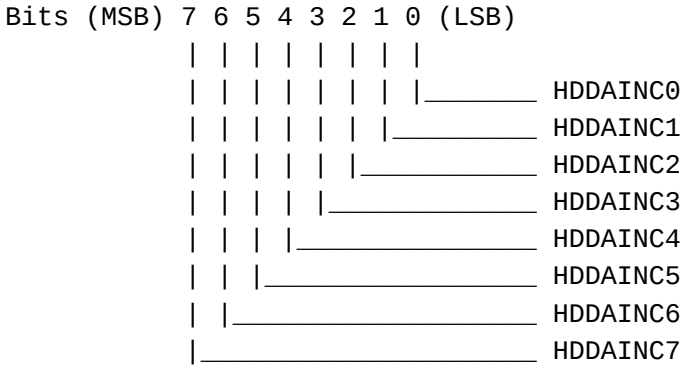
HDDAINI[7:0]: Horizontal DDA (digital differential algorithm) initial value low: This field will be set to 0800h during reset period.

2.206 Extended Video Horizontal DDA Initial Value High (3CF/D2, R/W)



HDDAINI[11:8]: Horizontal DDA (digital differential algorithm) initial value high: This field will be set to 0800h during reset period.

2.207 Extended Video Horizontal DDA Increment Value Low (3CF/D3, R/W)

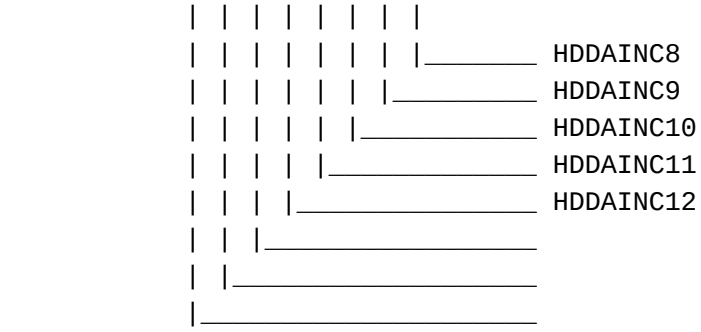


HDDAINC[7:0]: Horizontal DDA (digital differential algorithm) increment value low: The formula to calculate this field is shown below :

$$HDDAINC = \frac{(video\_pixel\_width\_in\_memory - 2) * 1000h + 800h - HDDAINI}{video\_pixel\_width\_on\_screen}$$

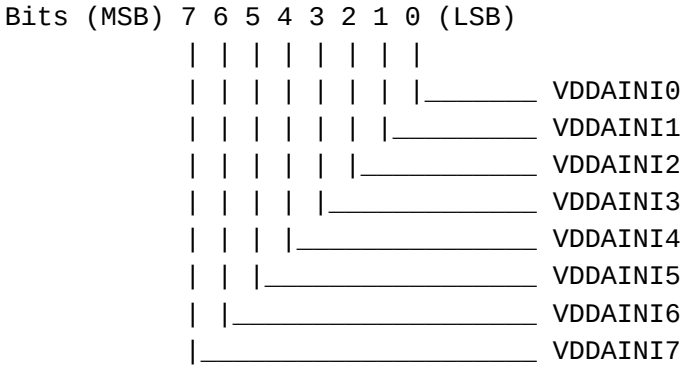
If no horizontal interpolation will be used, then this field should be programmed to 1000h.

2.208 Extended Video Horizontal DDA Increment Value High (3CF/D4, R/W)



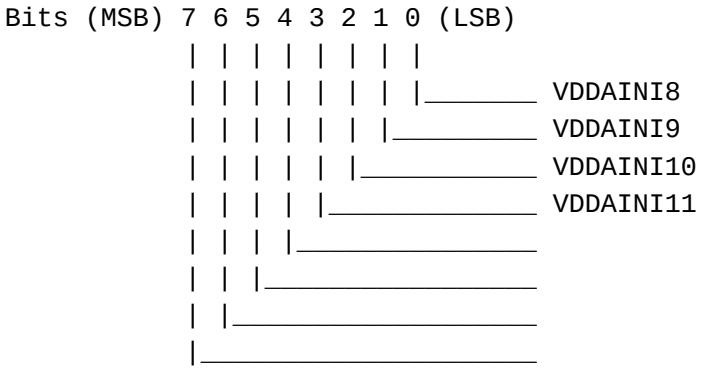
HDDAINC[12:8]: Horizontal DDA (digital differential algorithm) increment value high.

2.209 Extended Video Vertical DDA Initial Value Low (3CF/D5, R/W)



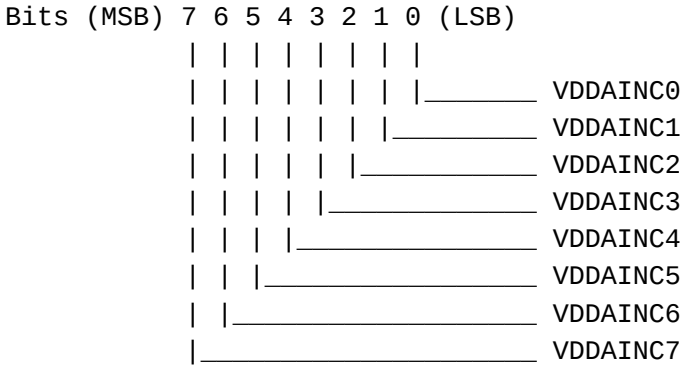
VDDAINI[7:0]: Vertical DDA (digital differential algorithm) initial value low: This field will be set to 0800h during reset period.

2.210 Extended Video Vertical DDA Initial Value High (3CF/D6, R/W)



VDDAINI[11:8]: Horizontal DDA (digital differential algorithm) initial value high: This field will be set to 0800h during reset period.

2.211 Extended Video Vertical DDA Increment Value Low (3CF/D7, R/W)

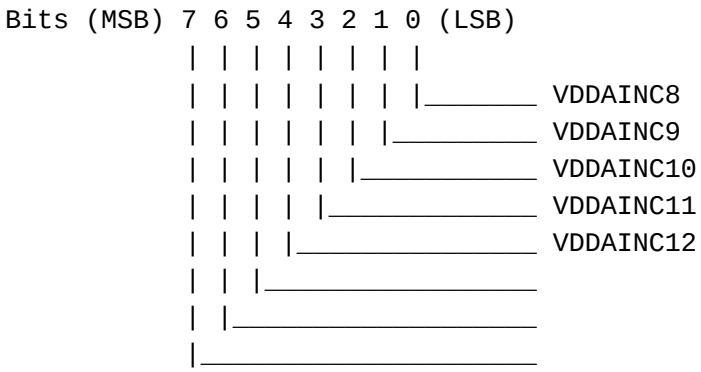


VDDAINC[7:0]: Vertical DDA (digital differential algorithm) increment value low: The formula to calculate this field is shown below :

$$VDDAINC = \frac{(video\_line\_height\_in\_memory - 2) * 1000h + 800h - VDDAINI}{video\_pixel\_line\_on\_screen}$$

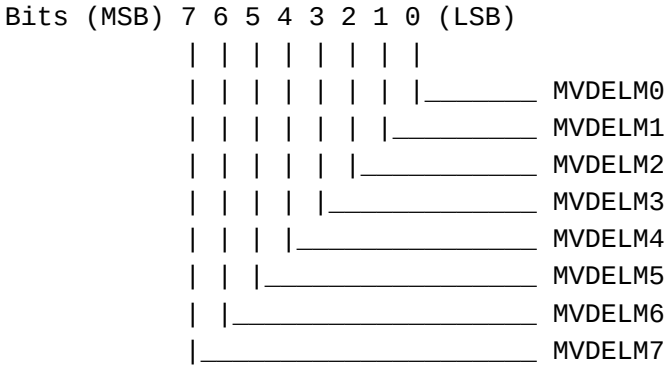
If no vertical interpolation will be used, then this field should be programmed to 1000h.

2.212 Extended Video Vertical DDA Increment Value High (3CF/D8, R/W)



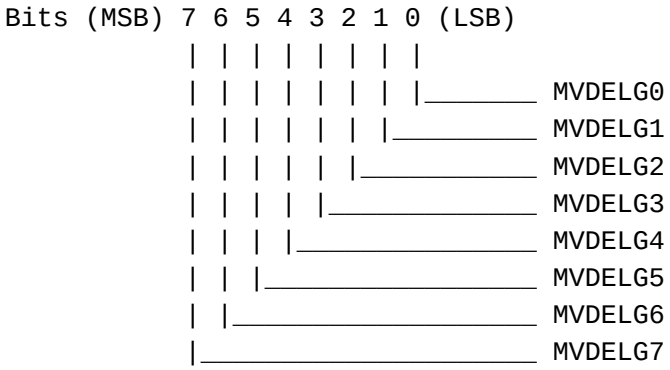
VDDAINC[12:8]: Vertical DDA (digital differential algorithm) increment value high.

2.213 Extended Video FIFO Low Control (3CF/D9, R/W)



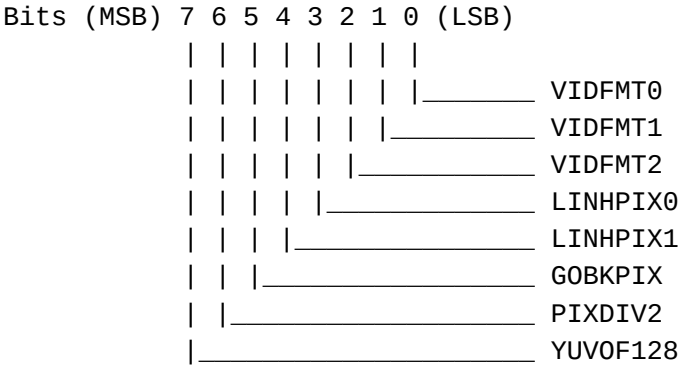
MVDELM[7:0]: Video FIFO policy must value: This field will defined the video high request timing. (reset default is 0F)

2.214 Extended Video FIFO High Control (3CF/DA, R/W)



MVDELG[7:0]: Video FIFO policy general value: This field will defined the video low request timing. (reset default is 1B)

2.215 Extended Video Format Control (3CF/DB, R/W)



VIDFMT[2:0]: Video Pixel Display Format:

VIDFMT2	VIDFMT11	VIDFMT0	# Video Input Format	
0	0	0	4 2 2 YUV	(YUVPIX)
0	0	1	5 5 5 RGB	(RG5BPIX)
0	1	0	5 6 5 RGB	(RG6BPIX)
0	1	1	24 Bits RGB	(RGB24PIX)
1	0	0	32 Bits RGB	(RGB32PIX)
1	0	1	8 Bits RGB	(RGB8PIX)
1	1	0	4 4 4 4 RGB	(RGB4PIX) (CONCERTO)
1	1	1	8T Bit RGB	(RGB8TPIX) (CONCERTO)

LINHPIX[1:0]: Video Pixel Display Zoom Out Format:

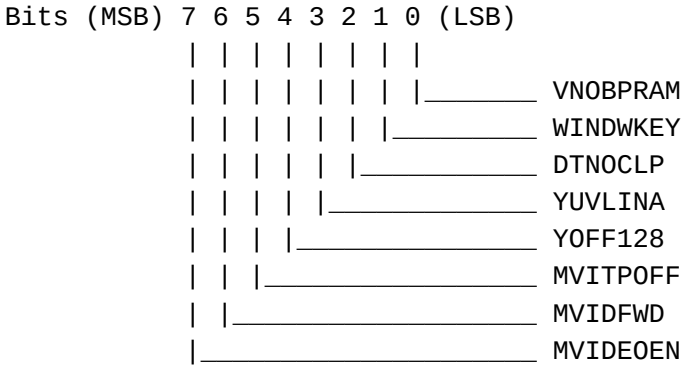
LINHPIX1	LINHPIX0	# Video Pixel Zoom Out Format	
0	0	0.5 Linearity approach	(LINHPIX)
0	1	Duplicate Previous Pixel	(DUPPIX)
1	x	Reserved	

GOBKPIX: Third pixel go back: When this bit is set to 1 and LINHPIX[1:0] is equal to 00, then the third duplicated pixel will jump back half value. When this bit is equal to 0, no effect will happened.

PIXDIV2: Double horizontal display pixel: When this bit is set to 1, horizontal pixel will be duplicated.

YUVOF128: YUV Data Offset 128: When this bit is equal to 1, YUV pixel data will be added 128 before any process.

2.216 Extended Video display Control I (3CF/DC, R/W)



VNOBPRAM: Video pixel not by passed internal ram : When this bit is equal to 0, pixel data will totally bypass internal RAM.

WINDWKEY: Video display use window key: When this bit is equal to 1, video display will ignore color compare register.

DTNOCLP: Data process no clipping: When this bit is set to 1, video FIFO data will not be clipped to (16, 235) (16, 240).

YUVLINA: U and V data process linearly: When this bit is equal to 1, U and V data will be averaged by previous U(V) and the U(V) pixel after.

YOFF128: Y Color Offset 128 enable: When this bit and YUVOF128 both are set to 1, then Y color will offset by 128.

MVITPOFF: Vertical interpolation off: When this bit is equal to 1, then the vertical interpolation will be turned off.

MVIDFWD: Video on full window: When this bit is equal to 1, no CRT data will be fetched and only video data will be displayed.

MVIDEOEN: Enables video: When this bit is set to 1, video window will be displayed on screen. If this bit is equal to 0, no video pixel will be fetched from video memory.

2.217 Extended Video Reserved Control I (3CF/DD, R/W)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ MVFFHLY
           | | | | | | |_________ CFLIKEZ
           | | | | | |___________ MGOFETH
           | | | | |_____________ MVRTCNTR
           | | | |_______________ MVRTFBD0
           | | |_________________ MVRTFBD1
           | |___________________ MVRTSEL0
           |_____________________ MVRTSEL1
```

MVFFHLY: Video FIFO High Policy Only: When this bit is equal to 1, video FIFO will be at high request only.

CFLIKEZ: CRT FIFO Like: When this bit is equal to 0, video FIFO policy will operate the same as 32 deep CRT FIFO.

MGOFETH: Video FIFO Always Fetch: When this bit is equal to 1, each horizontal line will fetch video data without looking at the vertical DDA algorithm.

MVRTCNTR: Video Counter Will Be Used: When this bit is equal to 1, a video adder will be used.

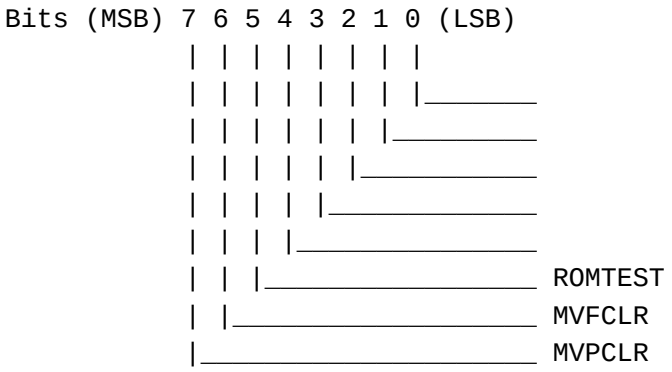
MVRTFBD[1:0]: Control CAS waveform feedback from memory:

MVRTFBD1	MVRTFBD0	# period of delay (ns)
0	0	0 (default)
0	1	2
1	0	6
1	1	4

MVRTSEL[1:0]: Control video memory data latch position:

MVRTSEL1	MVRTSEL0	# latching position
0	0	tracking CAS
0	1	early to CAS
1	0	medium to CAS
1	1	late to CAS

2.218 Extended Video Miscellaneous Control I (3CF/DE, R/W)

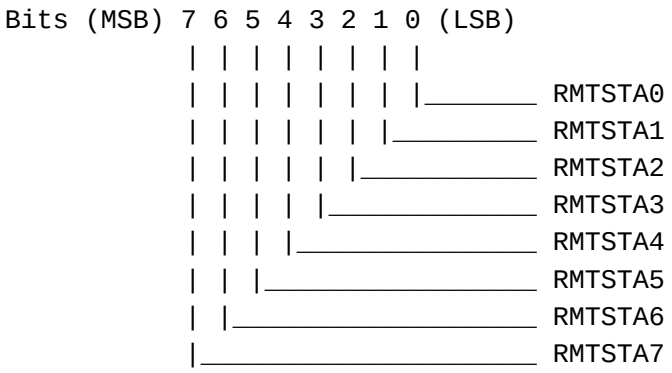


ROMTEST: ROM data test: When this bit is equal to 1, ROM data can be read out from register.

MVFCLR: Video FIFO clear: When this bit is set to 1, video FIFO module will be cleared.

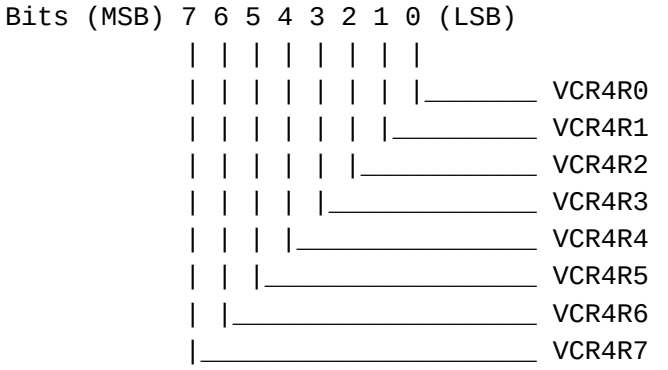
MVPCLR: Video pixel processor: When this bit is set equal to 1, video pixel processor module will be cleared.

2.219 Extended Video ROM Test Address (3CF/DF, R/W)



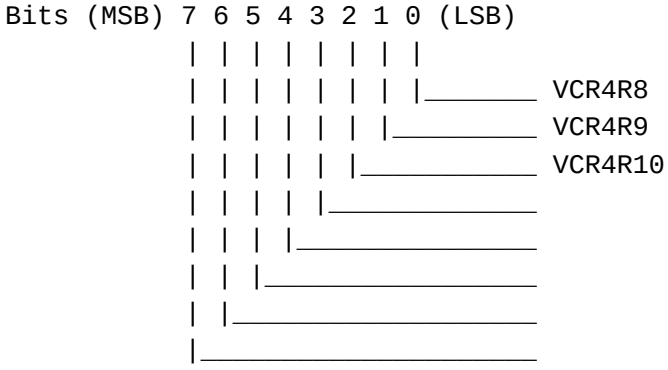
RMTSTA[7:0]: Video ROM test address: This field will be used as video ROM content test address.

2.220 Extended Video ROM VCR4R Low (3CF/E0, R) (Read Only)



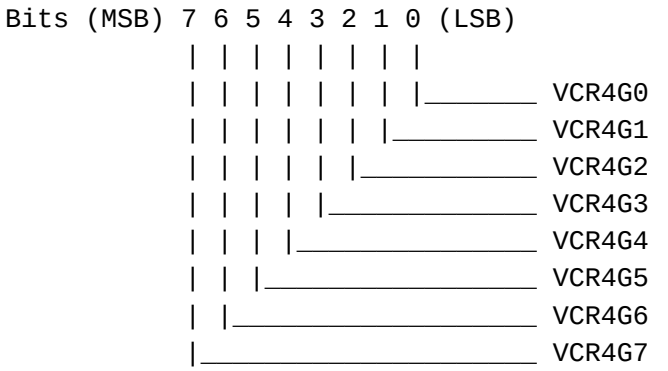
VCR4R[7:0]: Video convert for red value: This field will show the V color convert to red value.

2.221 Extended Video ROM VCR4R High (3CF/E1, R) (Read Only)



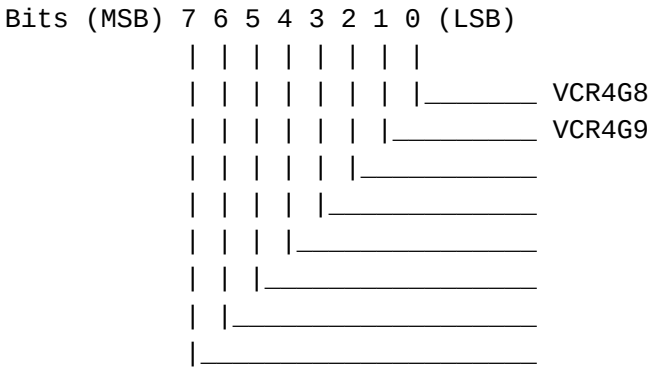
VCR4R[10:8]: Video convert for red value: This field will show the V color convert to red value.

2.222 Extended Video ROM VCR4G Low (3CF/E2, R) (Read Only)



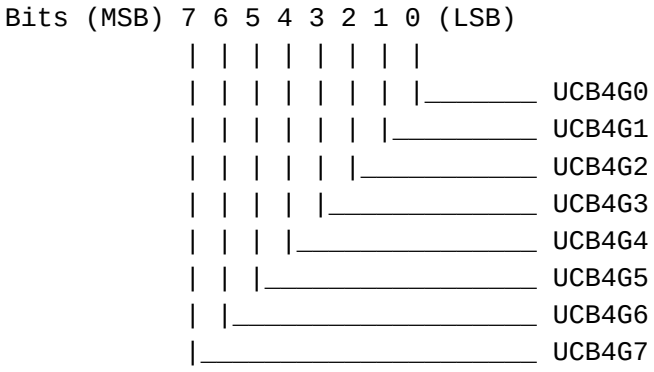
VCR4G[7:0]: Video convert for green value: This field will show the V color convert to green value.

2.223 Extended Video ROM VCR4G High (3CF/E3, R) (Read Only)



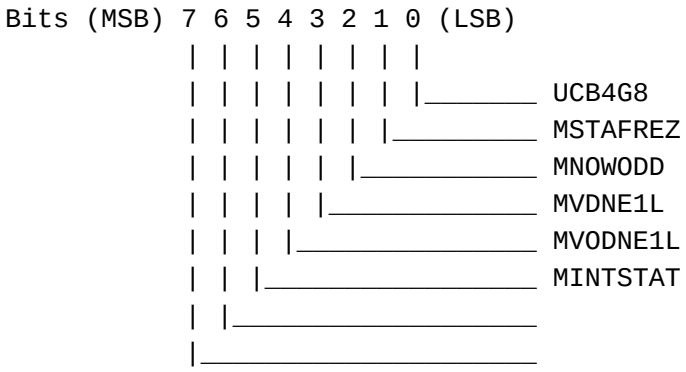
VCR4G[9:8]: Video convert for green value: This field will show the V color convert to green value.

2.224 Extended Video ROM UCB4G Low (3CF/E4, R) (Read Only)



UCB4G[7:0]: Video convert for green value: This field will show the U color convert to green value.

2.225 Extended Video ROM UCB4G High (3CF/E5, R) (Read Only)



UCB4G[8]: Video Convert for Green Value: This field will show the U color conversion to green value.

MSTAFREZ: Freeze Status: When this bit is equal to 1, the capture circuit is in the freeze state.

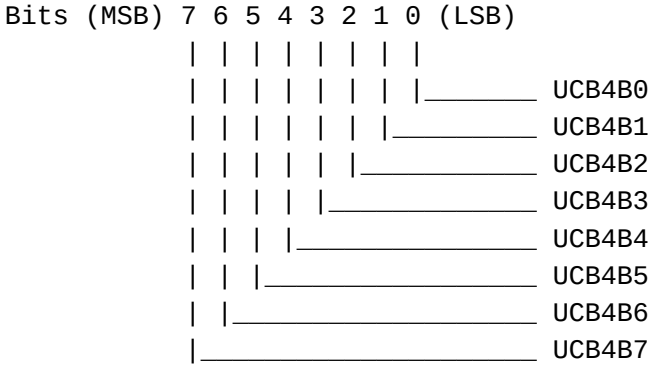
MNOWODD: Odd Frame: When this bit is equal to 1, then odd frame data will be captured into memory.

MVDNE1L: One Horizontal Period: When this bit is equal to 1, it indicates that the first horizontal line period comes after VGT falling edge.

MVODNE1L: Odd Frame Indicator: When this bit is equal to 1, it indicates that the odd frame data will be captured into memory. This signal will last for only one horizontal period.

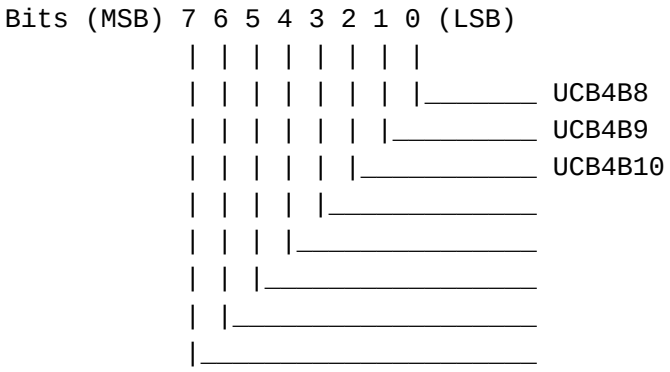
MINTSTAT: Video Interrupt Status: When this bit is equal to 1, it means that current interrupt belongs to video interrupt.

2.226 Extended Video ROM UCB4B Low (3CF/E6, R) (Read Only)



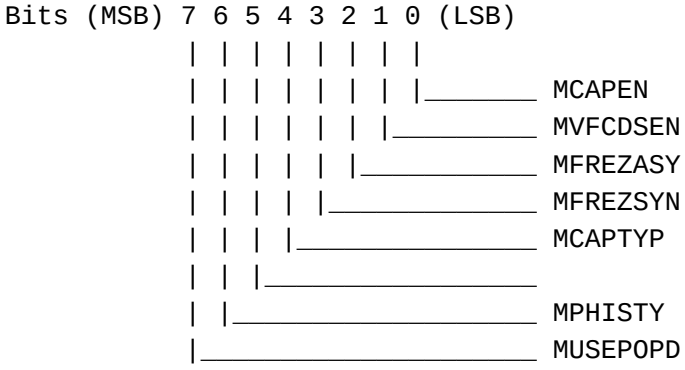
UCB4B[7:0]: Video convert for blue value: This field will show the U color convert to blue value.

2.227 Extended Video ROM UCB4B High (3CF/E7, R) (Read Only)



UCB4B[10:8]: Video convert for blue value: This field will show the U color convert to blue value.

2.228 Extended VFAC Control And Capture Mode I (3CF/E8, R/W)



MCAPEN: Capture Enable: When this bit is equal to 1, then 16 bits data from VFAC connector will be written into memory for capture usage. (This bit should be programmed during VSYNC high period.)

MVFCDSEN: VFAC display enable: When this bit is set to 1, then VFAC pixel video data will be overlaid on the CRT display.

MFREZASY: Freeze capture data: When this bit is equal to 1, then no more captured data will be written into memory and ready for CPU to read back the captured data from memory.

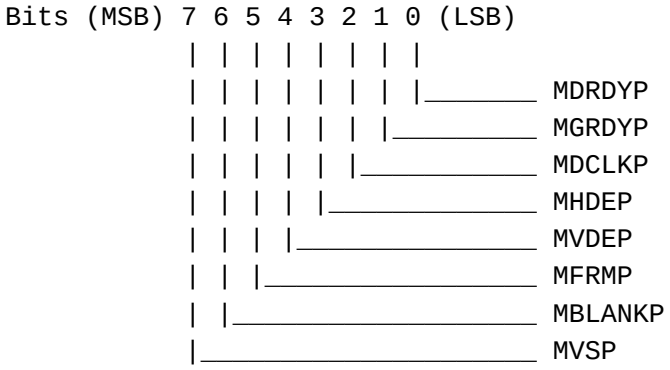
MFREZSYN: Same as MFREZASY, but it will take effect synchronously with vertical sync.

MCAPTYP: Capture Type: When this bit is set to 1, then GRDY (graphic ready), which is sent by the graphic chip, will be used for a valid video window. If this bit equals 0, then a valid video window will be defined by an external video chip.

MPHISTY: Philips style: When this bit is set to 1, then VSYNC (VDE), HSYNC (HDE) & BLANK signal will be in the input mode.

MUSEPOPD: Use pop delay for feedback latch signal: When this bit is set to 1, then write enable signal for vertical interpolation will not qualify with half dot clock.

2.229 Extended VFAC Control And Capture Mode II (3CF/E9, R/W)



MDRDYP: Video valid data ready (in): When this bit is set to 1, then signal into chip will be inverted. (internal active high signal will be used)

MGRDYP: Graphic ready signal (out): When this bit is equal to 1, then this signal will be inverted (negative polarity) and sent out.

MDCLKP: Dot clock (in): When this bit is set to 1, then DOTCLK from outside chip will be inverted and used by internal circuit.

MHDEP: HDE(in) or HSYNC(out) polarity: When this bit is equal to 1, then HDE(in) or HSYNC(out) will be inverted. (internal active high signal will be used)

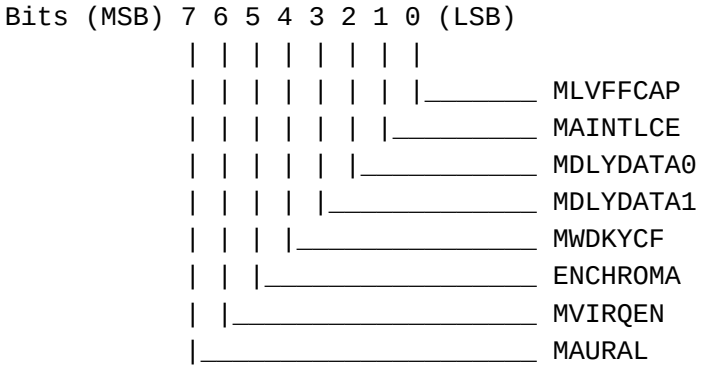
MVDEP: VDE(in) or VSYNC(out) polarity: When this bit is equal to 1, then VDE(in) or VSYNC(out) will be inverted. (internal active high signal will be used)

MFRMP: Frame odd/even (in) polarity: When this bit is equal to 1, then odd/even signal will be inverted. (internal 1=odd frame & 0=even frame)

MBLANKP: BLANK signal (out) polarity: When this bit is set to 1, then Blank will be inverted before set to outside.

MVSP: VSYNC signal (IN) polarity: When this bit is set to 1, then VSYNC will NOT be inverted before set to inside.

2.230 Extended VFAC Control And Capture Mode III (3CF/EA, R/W)



MLVFFCAP: Large FIFO Used for Capture: When this bit is equal to 1, then large FIFO will be used for captured data. Otherwise, the small video FIFO will be used, and no vertical interpolation will be handled.

MAINTLCE: Capture Data Interlace: When this bit is equal to 1, then capture will be in the interlaced mode.

MDLYDATA[1:0]: Delay Input Capture Data: When this bit is equal to 1, then the capture data will de delayed 4ns for more hold time for latching.

MDLYDATA1	MDLYDATA0	# delay time
0	0	4 NS
0	1	2 NS
1	0	6 NS
1	1	0 NS

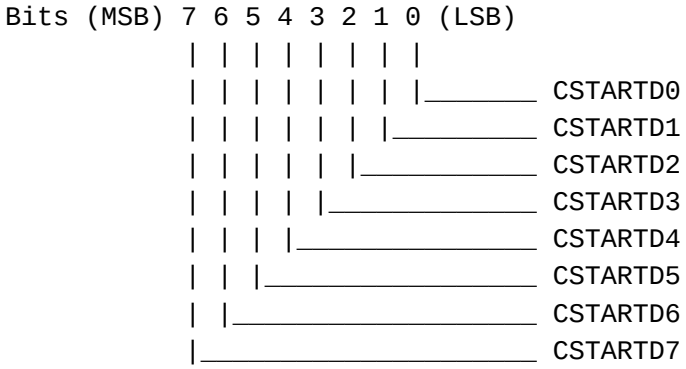
MWDKYCF: Window Keys for CF: When this bit is equal to 1, then video will be in window key and no CRT request will be generated during the video period.

ENCHROMA: Video Chroma Key Enable: When this bit is equal to 1, then video string will be in chroma key position.

MVIRQEN: Video Interrupt Enable: When this bit is equal to 1, then video interrupt will be set at every video non-display period.

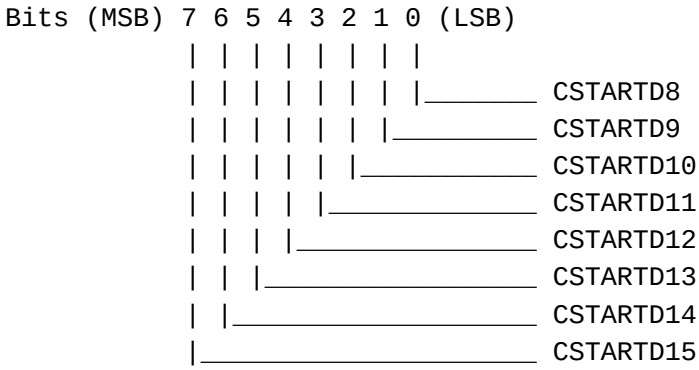
MAURAL: Aural Vision Data Format: When this bit is equal to 1, then capture data from outside will be in Aural Vision data format.

2.231 Extended Capture Memory Starting Address Low (3CF/EB, R/W)



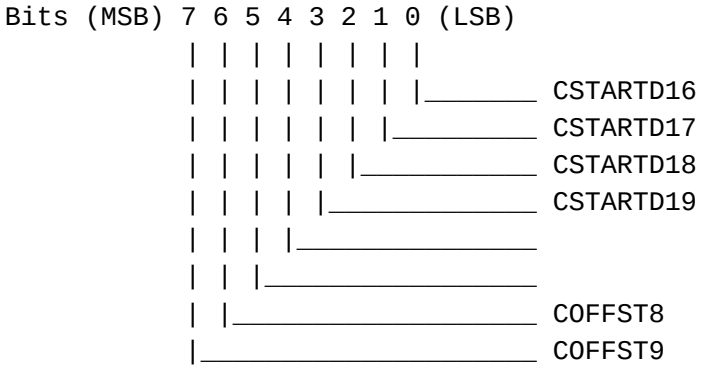
CSTARTD[7:0]: Video capture starting address low: This address field will be defined as video display starting address.

2.232 Extended Capture Memory Starting Address Middle (3CF/EC, R/W)



CSTARTD[15:8]: Video capture starting address middle: This address field will be defined as video display starting address.

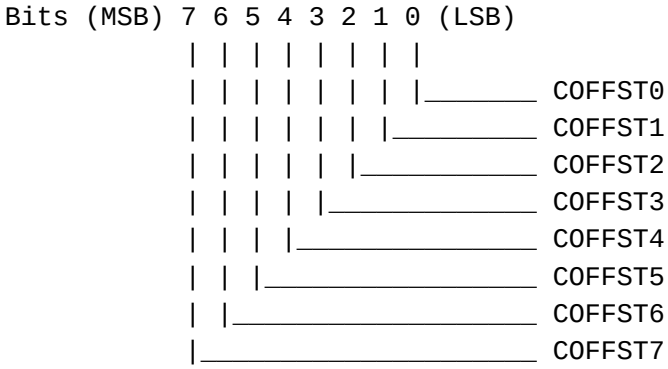
2.233 Extended Capture Memory Starting Address High (3CF/ED, R/W)



CSTARTD[19:16]: Video capture starting address high: This address field will be defined as video display starting address.

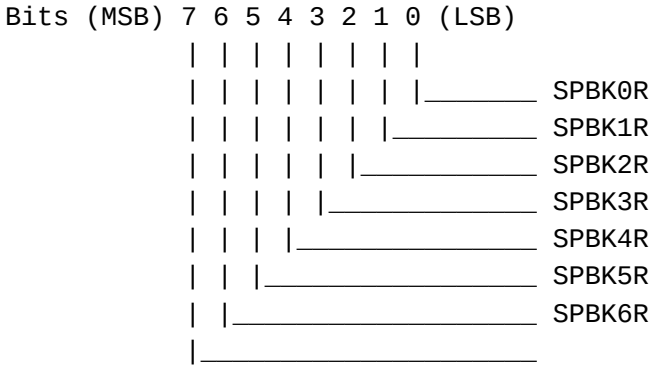
COFFST[9:8]: Video capture map width high: This offset value will control video capture display next line starting address.

2.234 Extended Capture Source Map Width Low (3CF/EE, R/W) (Capture Memory Fetch Pitch Low)



COFFST[7:0]: Video capture map width low: This offset value will control video capture display next line starting address.

2.235 Extended Capture Control Miscellaneous (3CF/EF, R/W)



SPBK0R: When this bit is equal to 1, a new control will be used for the horizontal divided factor, otherwise no divided factor will be used.

SPBK1R: When this bit is equal to 1, the horizontal divided by 4 will be used for data good signal; otherwise divided by 2 will be used. This bit is valid only when SPBK0R is equal to 1.

SPBK2R: When this bit is equal to 1, an odd/even frame signal will be used as the data good signal input; otherwise the original data good input from pad will be used.

SPBK3R: When this bit is equal to 1, the HGT signal will be divided by 2; otherwise the original HGT from pad will be used.

SPBK4R: When this bit is equal to 1, SYNCTZ will be always set to VDD; otherwise SYNCTZ will depend upon SPKBK5R.

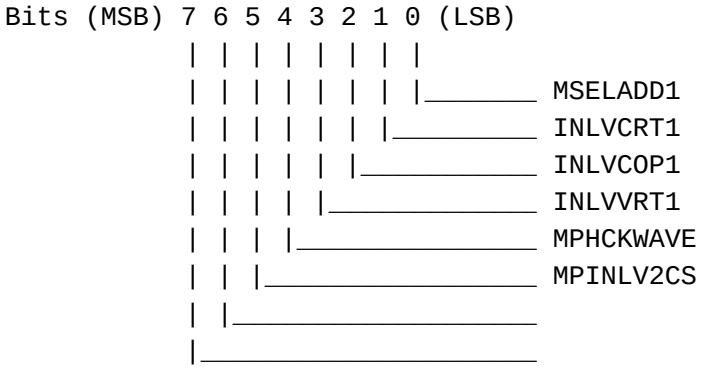
SPBK5R: When this bit is equal to 1, an OR function will be used for SYNCTZ; otherwise NSYNCZ will be used.

SPBK6R(Cheta2): When this bit is equal to 1, YDE1FP will be entered into FIFO; otherwise MCAPEN will be used for control.

SPBK6R(Genesis): When this bit is equal to 1, a SONY workstation problem will be fixed; and, after genesis, this bit should always be set to 1.

SPBK7R: When this bit is equal to 1, it indicates to software the video display has been used.

2.236 Extended MISC0 (3CF/F0 R/W)



MSELADD1: Same as MSELADD.

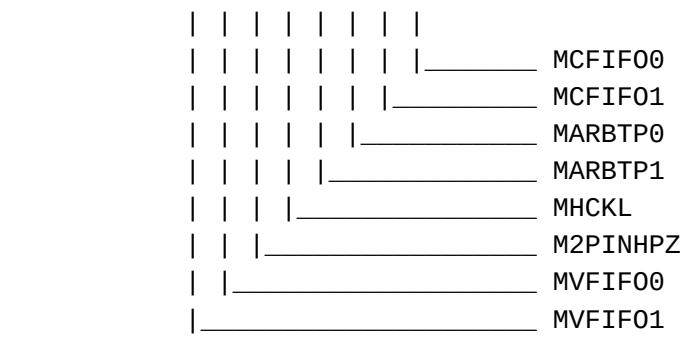
INLVCRT1: Same as INLVCRT.

INLVVRT1: Same as INLVVRT.

MPHCKWAVE: Half CLK mode select: When this bit is equal to 1 then CAS signal will be in half clock mode.

MPINLV2CS: Two CAS mode select: When this bit is equal to 1 then two CAS will be inserted. This bit and (INLVCRT, INLVVRT) can NOT be on the same time. This bit should be used with MPHCKWAVE.

2.237 Extended MISC1 (3CF/F1 R/W)



MCFIFO[1:0]: CRT FIFO depth control.

MCFIFO1	MCFIFO0	# of depth used
0	0	32 levels
0	1	64 levels
1	0	128 levels

MARBTP[1:0]: Arbitration for graphic to give up bus for CPU.

MARBTP1	MARBTP0	# of clk to give up bus
0	0	16
0	1	32
1	0	48
1	1	56

MHCKL: Half CLK select left side: When this bit is equal to 1, then the left part of CAS will be used if single clock mode is on.

M2PINHPZ: Not used.

MVFIFO[1:0]: Video FIFO depth control.

MVFIFO1	MVFIFO0	# of depth used
0	0	32 levels
0	1	64 levels
1	0	128 levels

Note: Use this bits has some constrained.

2.238 Extended MISC2 (3CF/F2 R/W)

```
Bits (MSB) 7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |
           | | | | | | | |_______ MUMBON (*M0D7)
           | | | | | | |_________ PIN2AR (*M0D8)
           | | | | | |___________ PRI2CPU
           | | | | |_____________ ALL2CPU
           | | | |_______________ MABORT
           | | |_________________ MZEROWT
           | |___________________ MCPUCKON
           |_____________________ MUBUSON
```

MUMBON: UMA bus on: When this bit is equal to 1, graphic chip in UMA bus condition.

PIN2ARB: Two pin arbitration: When this bit is equal to 1, graphic chip and chip set in two pin arbitration, otherwise three pins will be used.

PRI2CPU: Priority for CPU: When this bit is set to 1, priority high will be asserted to chip set only when high priority request from graphic chip.

ALL2CPU: All for CPU: When this bit is set to 1, graphic chip will not send request to chip set until it is necessary.

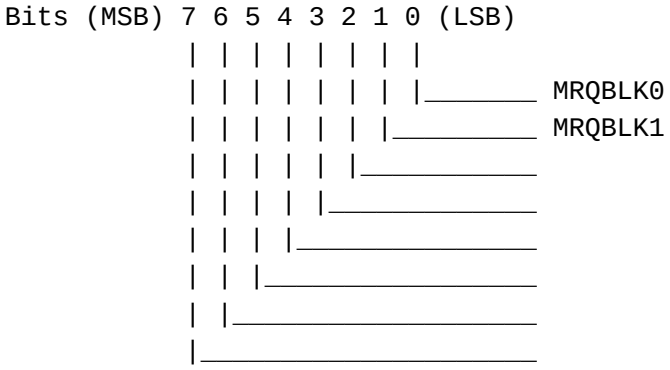
MABORT: Do not use.

MZEROWT: Do not use.

MCPUCKON: CPU clock on: When this bit is set to 1, graphic chip will use CPU 66Mhz for memory clock.

MUBUSON: UMA bus on: When this bit is set to 0, graphic chip memory side will be in tri-state condition.

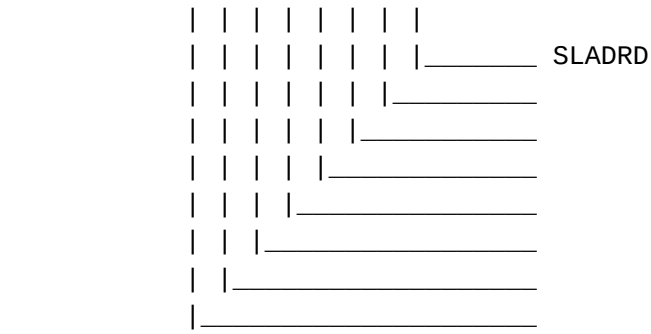
2.239 Extended MISC3 (3CF/F3 R/W)



MRQBLK[1:0]: Request block cycle after preempt by chip set.

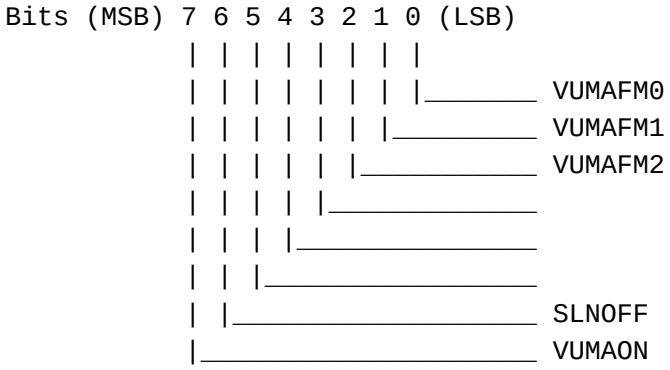
MRQBLK1	MRQBLK0	# of clk to block
0	0	6
0	1	4
1	0	3
1	1	2

2.240 Extended MISC4 (3CF/F4 R/W)



SLADRD: Address position select: When this bit is set to 1, DRAM address will be sent out on falling edge of memory clock.

2.241 Extended VUMA Configuration (3CF/F5 R/W)



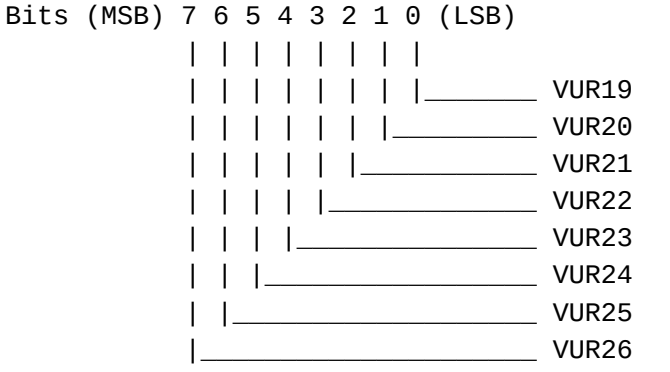
VUMAFM[2:0]: VESA UMA memory format.

VUMAF2	VUMAFMM1	VUMAFM0	# of clk to block
0	0	0	SYM & ASYx11
0	0	1	ASYx8
0	1	0	ASYx9 & UMCx8
0	1	1	ASYx10
1	X	X	Reserved

SLNOFF: Select number of arbitration: When this bit is set to 1, the register value of ROFFARB(3CE_F7) will be used.

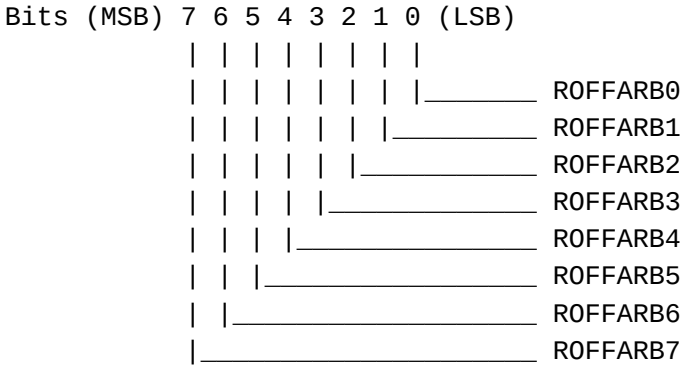
VUMBON: VUMA bus on: When this bit is equal to 1, graphic chip in VUMA bus condition.

2.242 Extended VUMA Extended Address (3CF/F6 R/W)



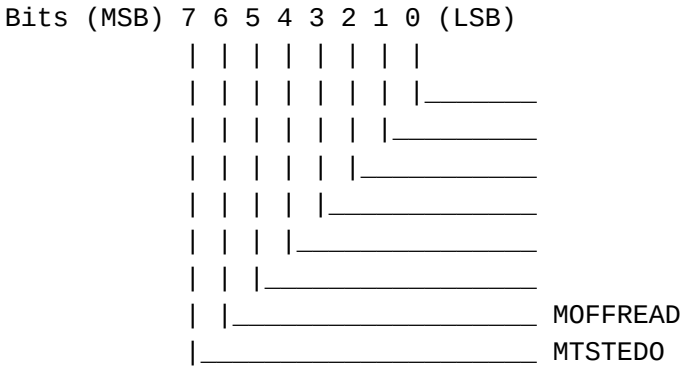
VUR[26:19]: VUMA high address, In VUMA mode the high address will be driven by this register.

2.243 Extended VUMA Arbitration Value (3CF/F7 R/W)



ROFFARB[7:0]: Arbitration for graphic to give up bus for CPU: This register will be used to terminated the memory bus for CPU.

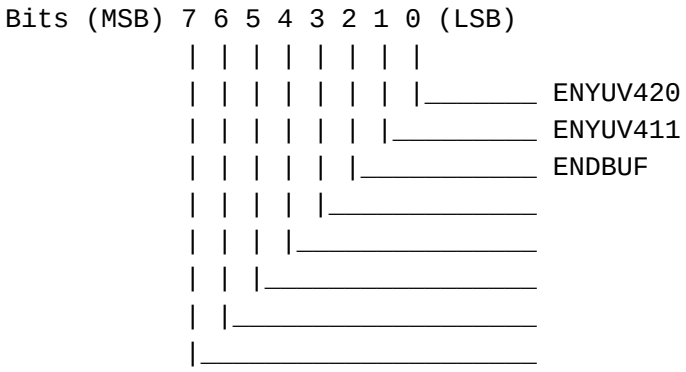
2.244 Extended EDO Memory (3CF/F8 R/W)



MOFFREAD: Turn all read cycle off: When this bit is equal to 1, all read cycle (CRT, REFRESH) will be turned off.

MTSTEDO: Test EDO memory: When this bit is equal to 1, all read cycle from CPU will not send CAS signal out to memory.

2.245 Extended Video Planar Mode (3CF/F9 R/W)

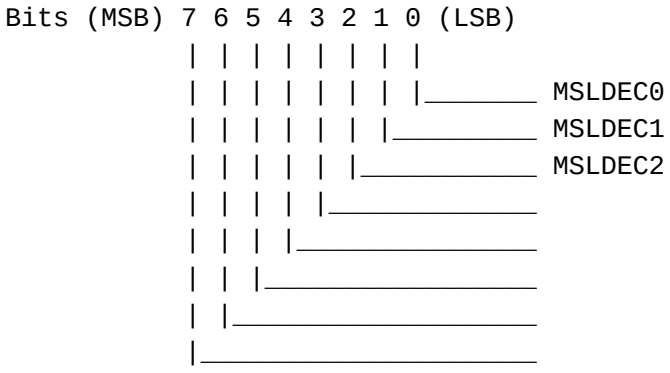


ENYUV420: Enables YUV420 mode: When this bit is equal to 1, CPU will enable YUV420 mode.

ENYUV411: Enables YUV411 mode: When this bit is equal to 1, CPU will enable YUV411 mode.

ENDBUF: Enables double buffer: When this bit is equal to 1, YUV420 or YUV411 will be in double buffer mode.

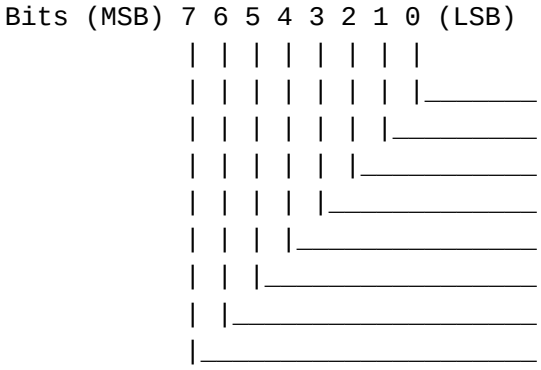
2.246 Extended Indirect Index For 4X (3CF/FA R/W)



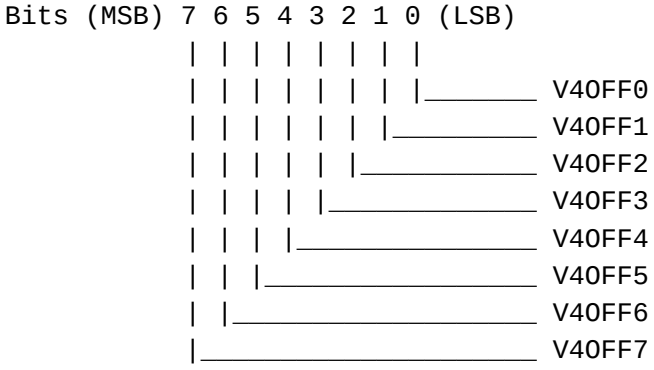
MSLDEC[2:0]: Indirect index registers decode select.

MSLDEC2	MSLDEC1	MSLDEC0	# of clk to block
0	0	0	0 (Hex 0)
0	0	1	1 (Hex 1)
0	1	0	2 (Hex 2)
0	1	1	3 (Hex 3)
1	0	0	4 (Hex 4)
1	0	1	5 (Hex 5)

2.247 Extended Not Used (3CF/FB R/W)

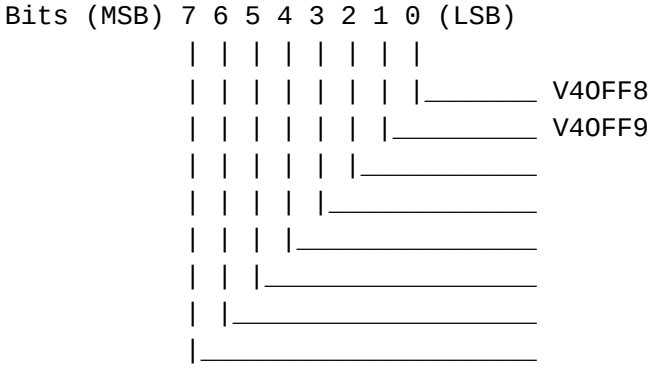


2.248 Extended YUV Value Offset Low (3CF/FC R/W)



V4OFF[7:0]: YUV offset register low: This low field contains the offset width value for YUV420 and YUV411 modes. (64-bit field)

2.249 Extended YUV Value Offset High (3CF/FD R/W)

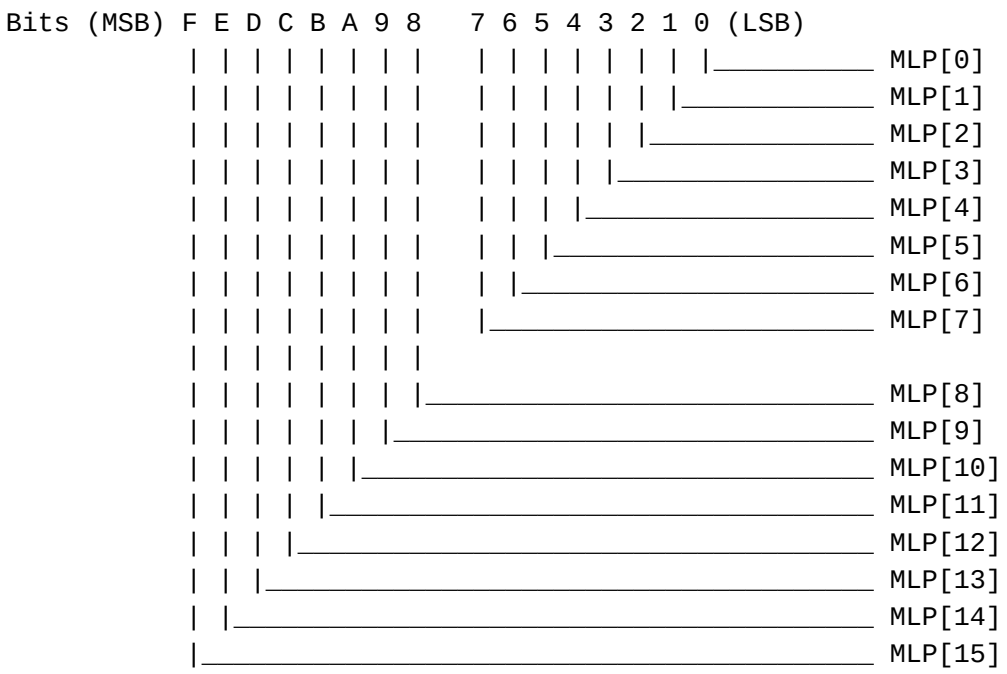


V4OFF[9:8]: YUV offset register low: This high field contains the offset width value for YUV420 and YUV411 modes. (64-bit field)

THIS PAGE INTENTIONALLY LEFT BLANK

3 TV Register Set

3.1 Port Address - BE428\H



MLP[15:0]: Multiplier Test Data: This is the test data results of the following 3 individual multipliers : C_MOD, SPBINS, UVBBINS.

To test the individual multiplier:

A. Turn on the individual test bit in index 269

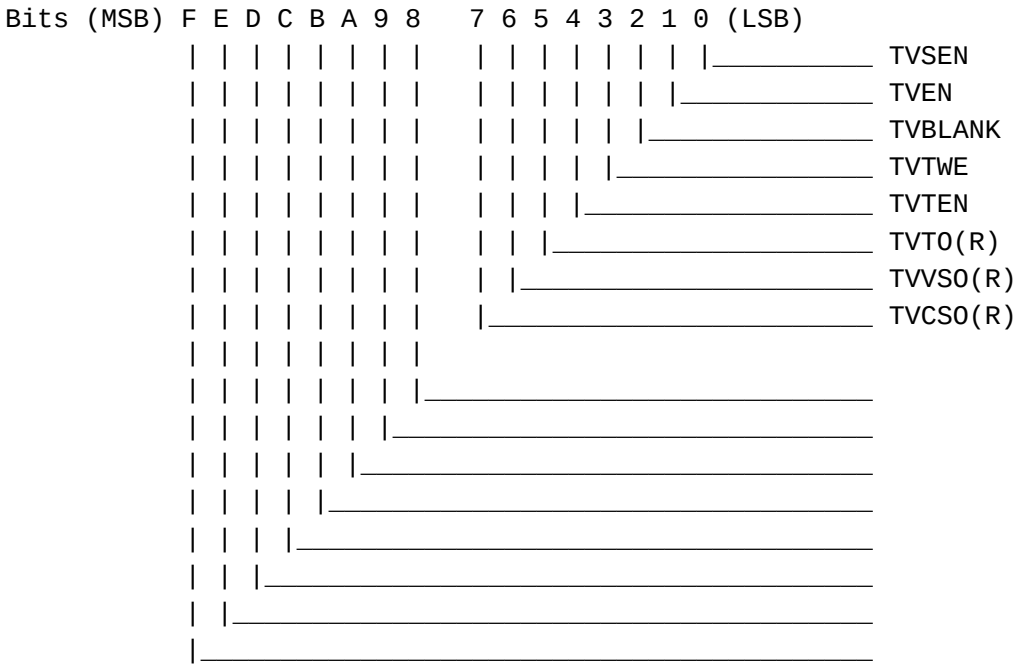
B. Memory write to index 266, and memory read from index 266

3.2 Port Address - BE42C\H

This register is reserved.

3.3 Port Address - BE430\H

TV DAC Related Test - This register is used for holding TVDAC test signals.

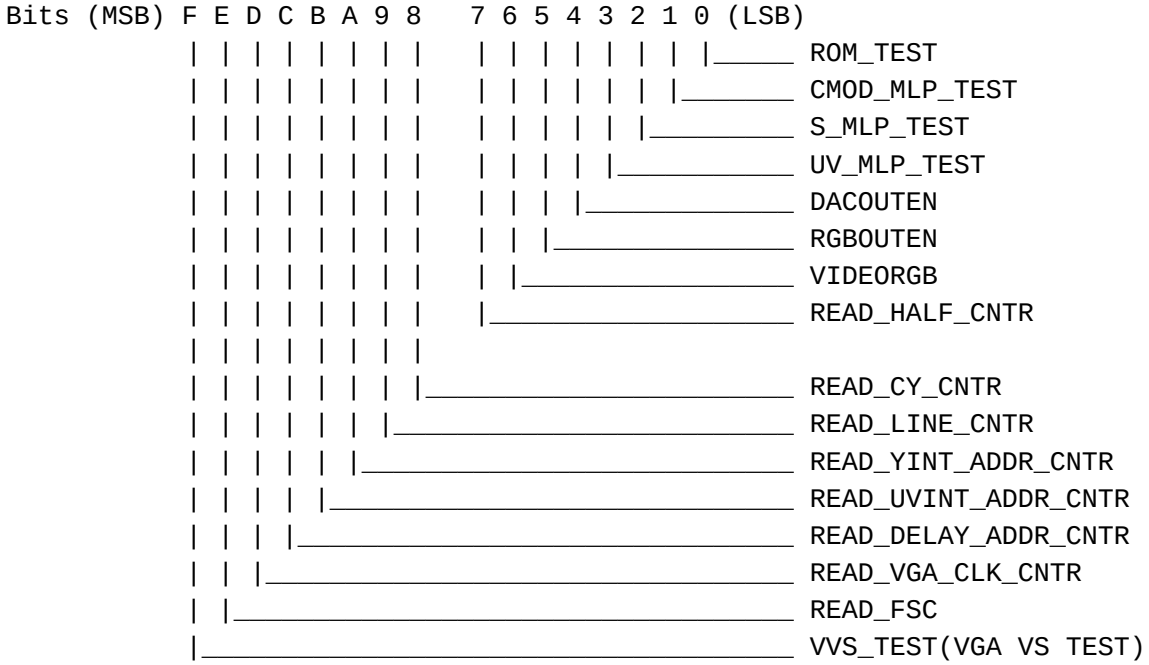


TVSEN:	Used to turn on TV detection circuitry.
TVEN:	TV enable.
TVBLANK:	Used to change the TV blank level.
TVTWE, TVTEN:	These two bits are used for TVDAC test signals
TVTO, TVVSO, TVCSO:	These three bits are used for TVDAC detection inputs, and cannot be written to.

Note: TVYSO -> TVVSO in 2010.

3.4 Port Address - BE434\H

ROM ,Multiplier, and TVDAC Output Related Test.



ROM_TEST: Used for SRO128x8 ROM test.

CMOD_MLP_TEST, S_MLP_TEST, UV_MLP_TEST: Used for testing respective multipliers.

DACOUTEN: to enable CDAC[7:0],YDAC[7:0] to MTST[15:0]

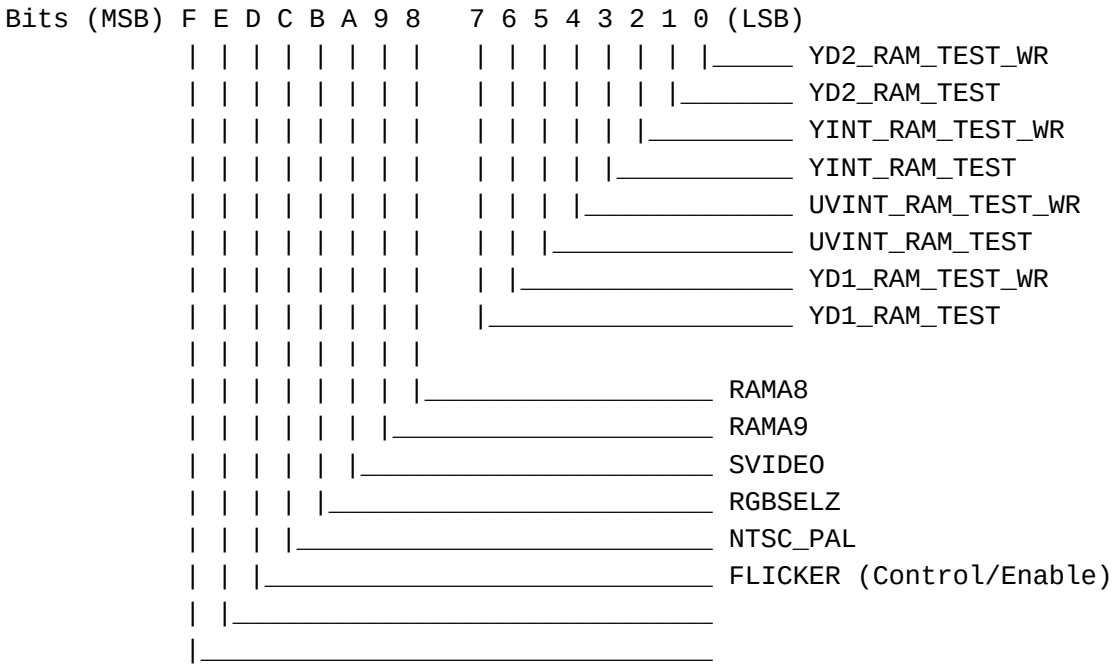
RGBOUTEN: Used to enable B[7:0], G_Y[7:0], TVYSO, TVTO, TVEN, CLK8, CLK4, CLK2, CLK, V2CLK, and R_UV[7:0] to MTST[31:0]

VIDEORGB: Used to select VIDEORGB data to TVOUT module instead of CRT RGB data to TVOUT

Note: READ_HALF_COUNTER takes precedence if multiple read's are on.

3.5 Port Address - BE438\H

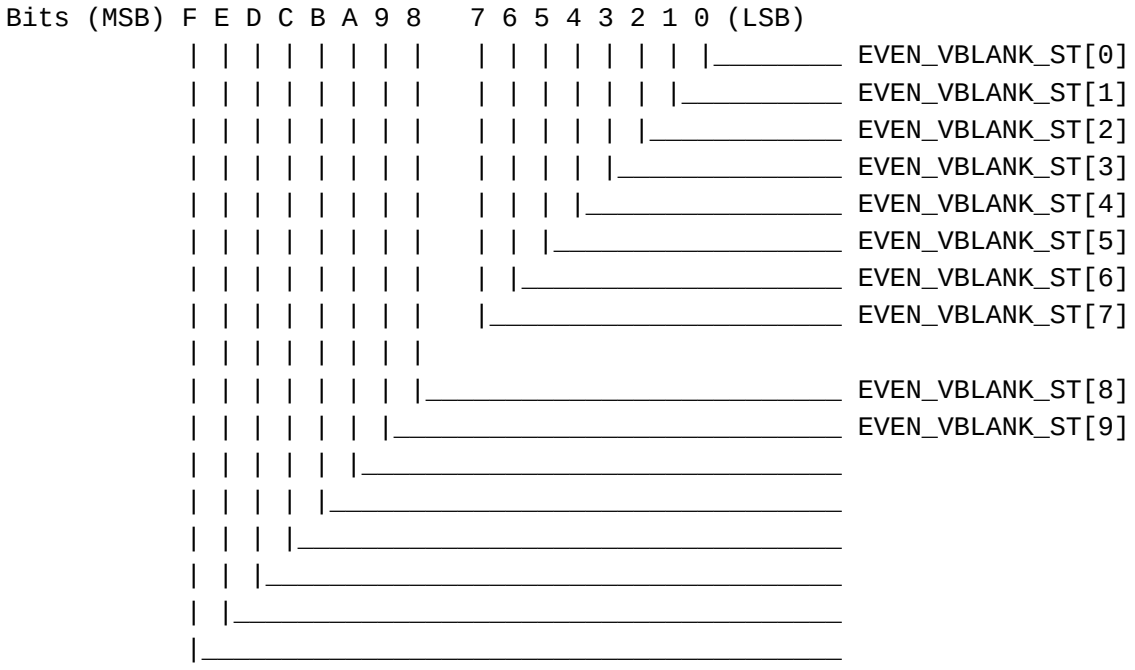
RAM Test enable, R/W control and miscellaneous control.



SVIDEO:	Must be 1 for CyberPro2000 mode. Must always be 0 for CyberPro2010 mode.
NTSC_PAL:	NTSC when this bit is 1; PAL when this bit is 0.
FLICKER:	Enabled when this bit is 1; disabled when this bit is 0.

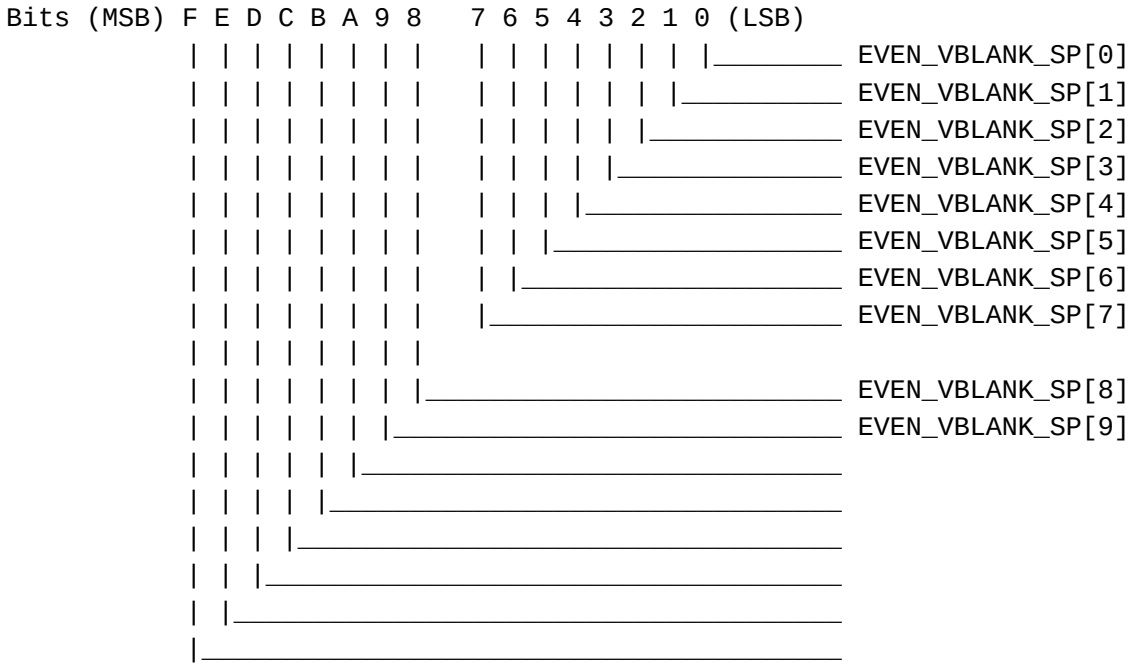
Note: RGBSELZ is normally LOW, which implies RGBSEL is normally HIGH, and RGB is used for input to encoder not YUV.

3.6 Port Address - BE43C\H



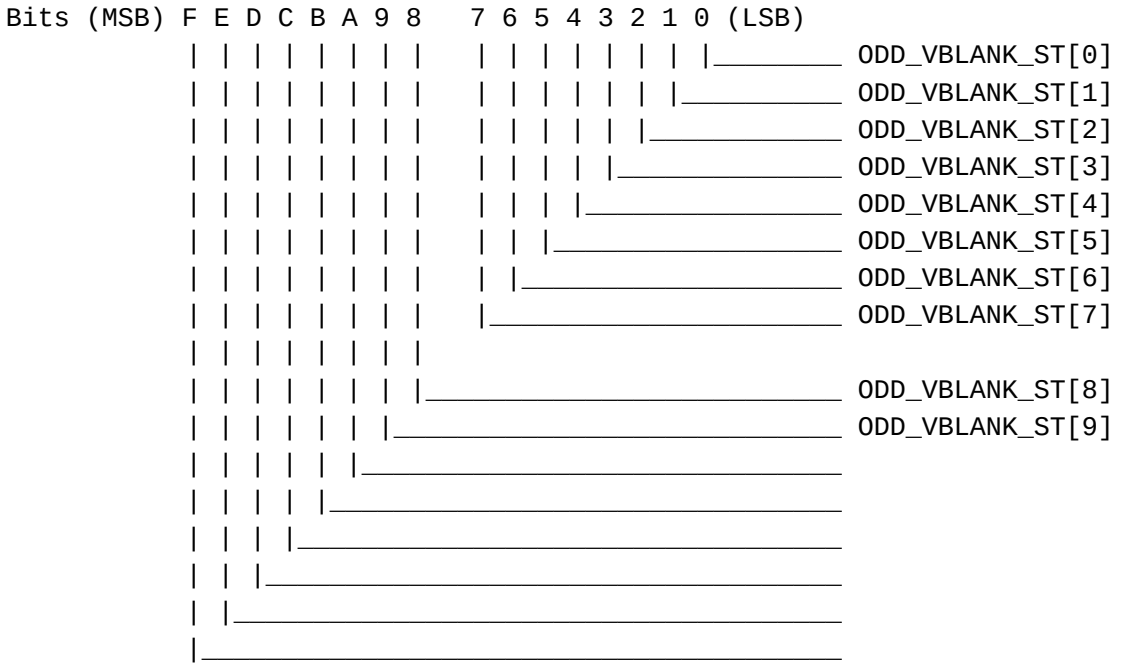
EVEN_VBLANK_ST[9:0]: Even field VBLANK start position control.

3.7 Port Address - BE440\H



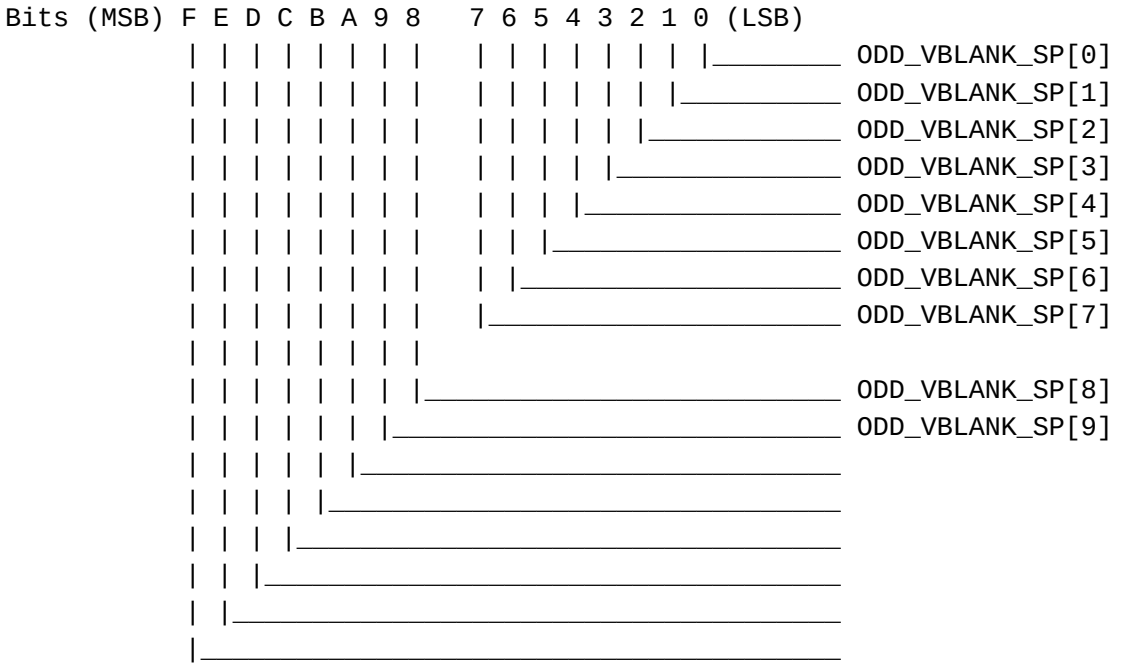
EVEN_VBLANK_SP[9:0]: Even field VBLANK stop position control.

3.8 Port Address - BE444\H



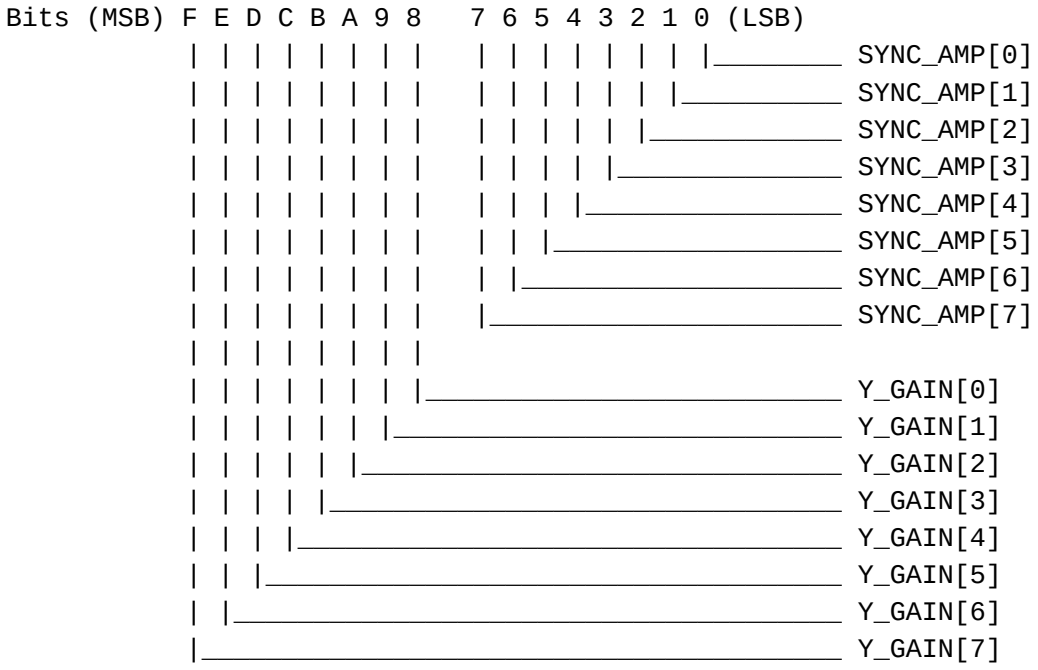
ODD_VBLANK_ST[9:0]: Odd field VBLANK stop position control.

3.9 Port Address - BE448\H



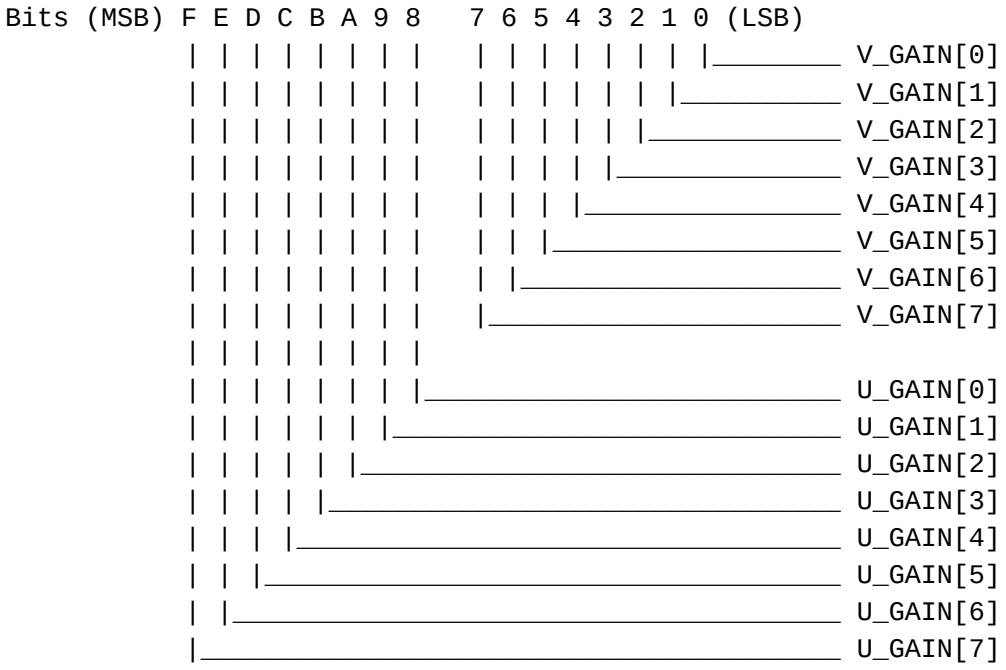
ODD_VBLANK_SP[9:0]: Odd field VBLANK stop position control.

3.10 Port Address - BE44C\H



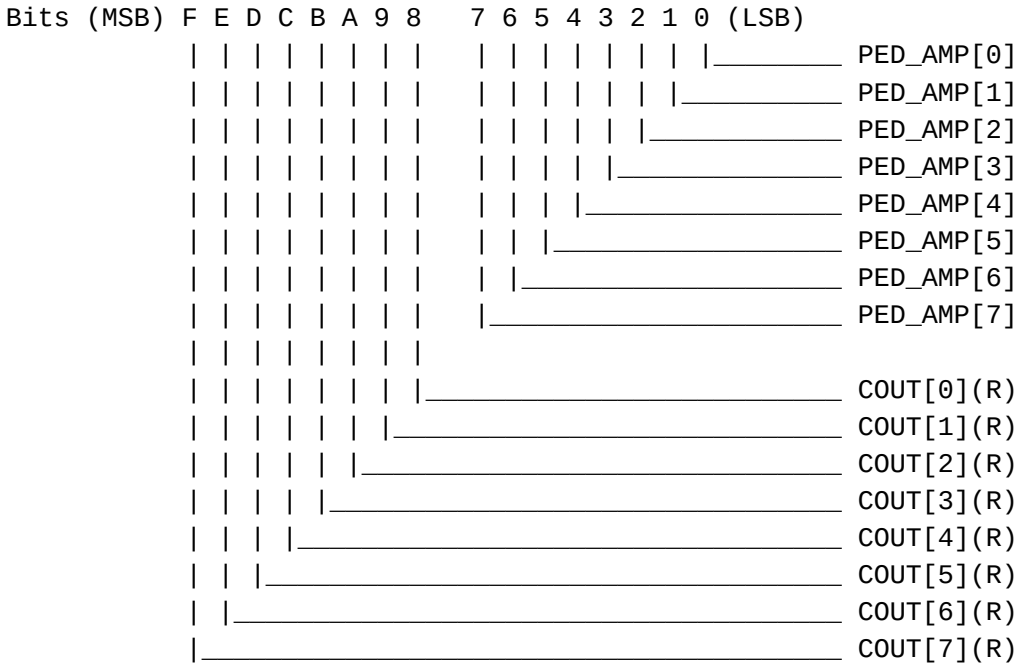
SYNC_AMP[7:0]: Sync Amplitude; amplitude of the sync level.
Y_GAIN[7:0]: Luminance Blanking Level Amplitude.

3.11 Port Address - BE450\H



V_GAIN: Gain control for V of chroma.
U_GAIN: Gain control for U of chroma.

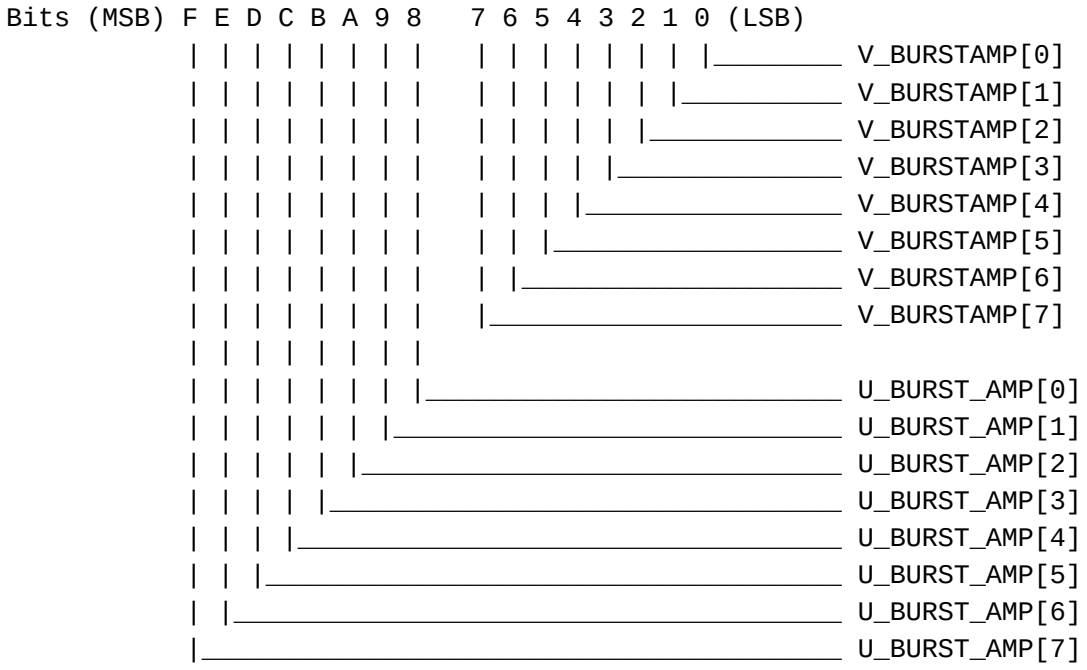
3.12 Port Address - BE454\H



PED_AMP[7:0]: This number determines the amplitude of pedestal or setup level.

COUT[7:0]: Color U,V detection value.

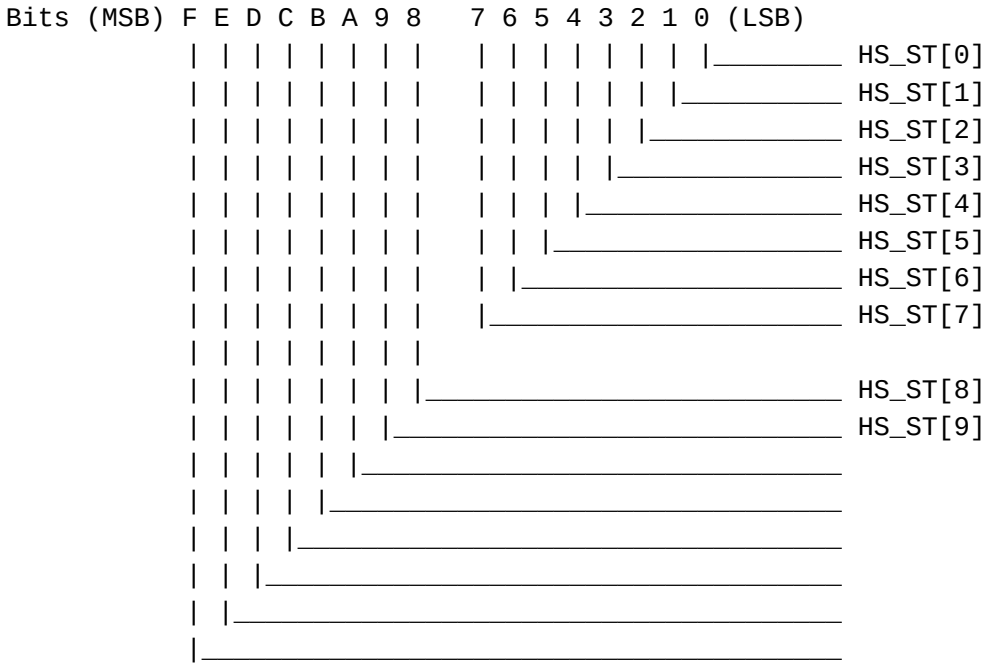
3.13 Port Address - BE458\H



U_BURST_AMP[7:0]: The amplitude of the burst in the U domain.

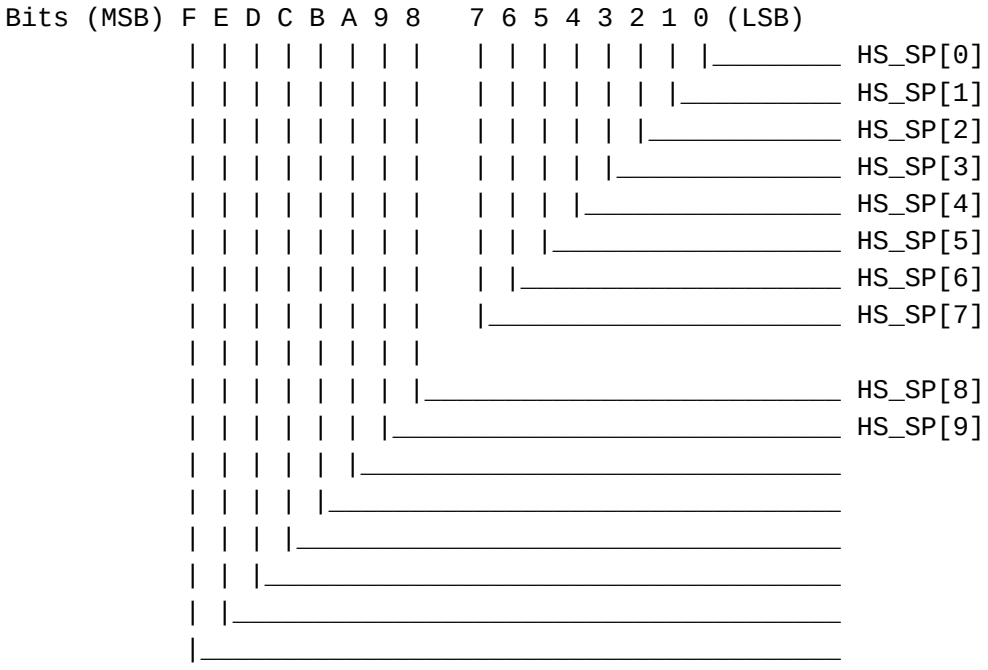
V_BURST_AMP[7:0]: The amplitude of the burst in the V domain.

3.14 Port Address - BE45C\H



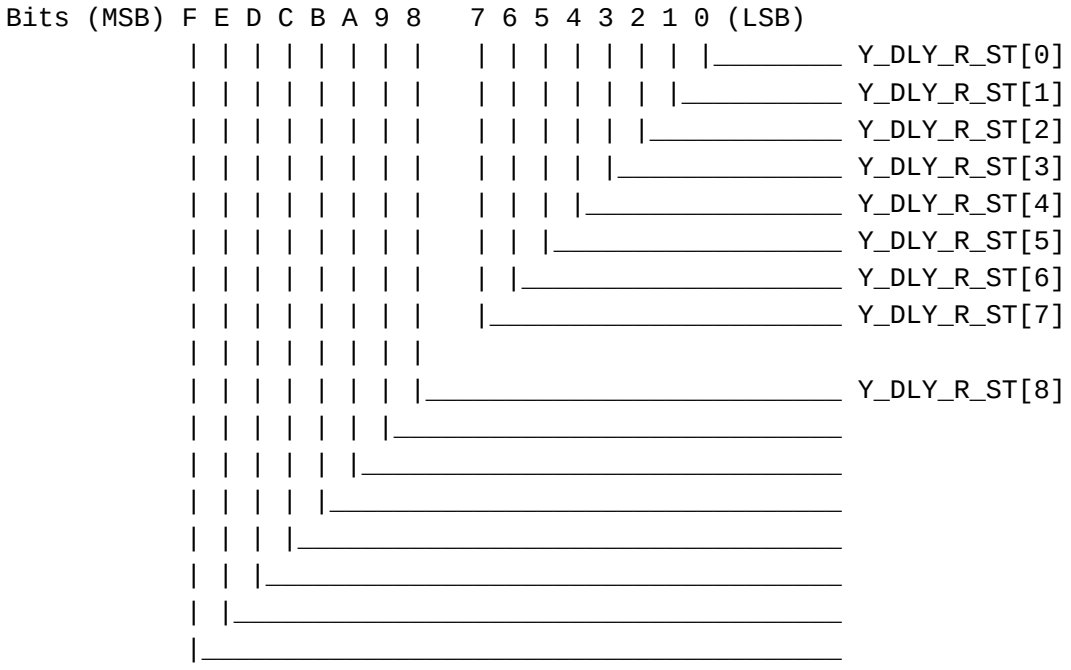
HS_ST[9:0]: Horizontal Sync. Start Position.

3.15 Port Address - BE460\H



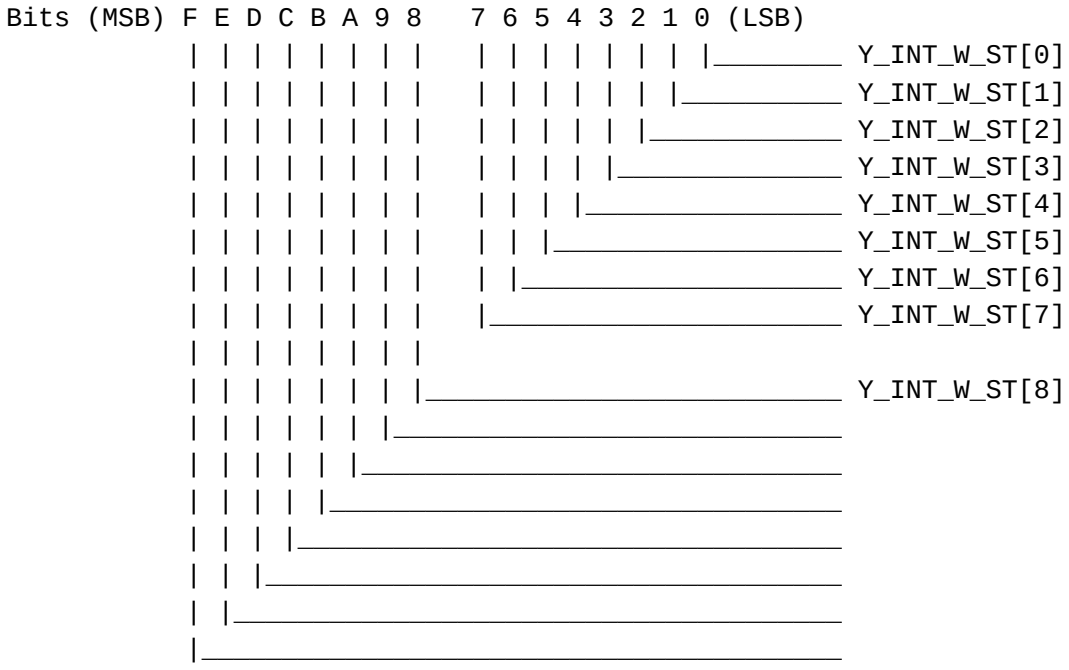
HS_SP[9:0]: Horizontal Sync. Stop Position.

3.16 Port Address - BE464\H



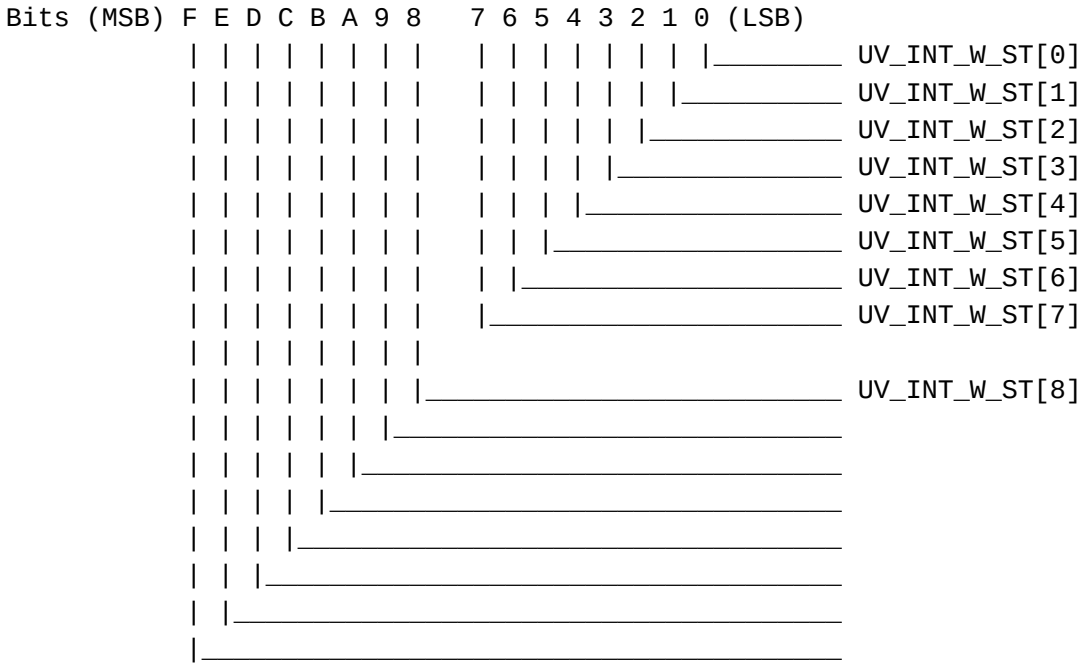
Y_DLY_R_ST[8:0]: VGA Active Data Delayed Read Start - Luminance Channel: This delays the luminance read to make up for the internal delay from chrominance processing (delay read address reset position).

3.17 Port Address - BE468\H



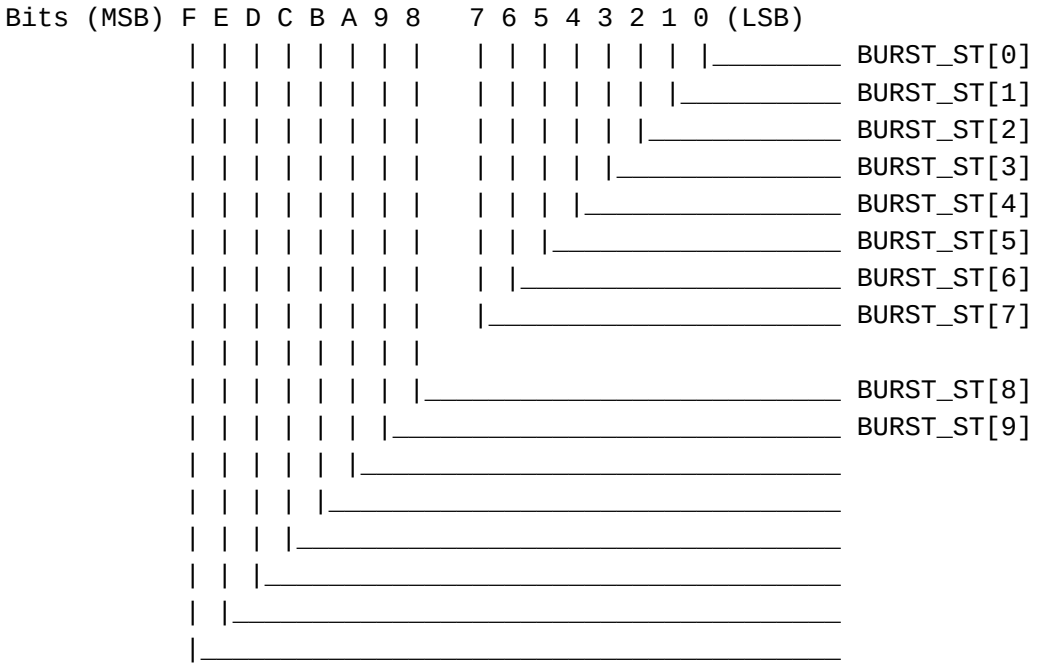
Y_INT_W_ST[8:0]: VGA Active Data Start - Luminance Channel: This selects the beginning of active VGA data compensated for the internal luminance delay of the encoder (Y_INT_RAM write reset position).

3.18 Port Address - BE46C\H



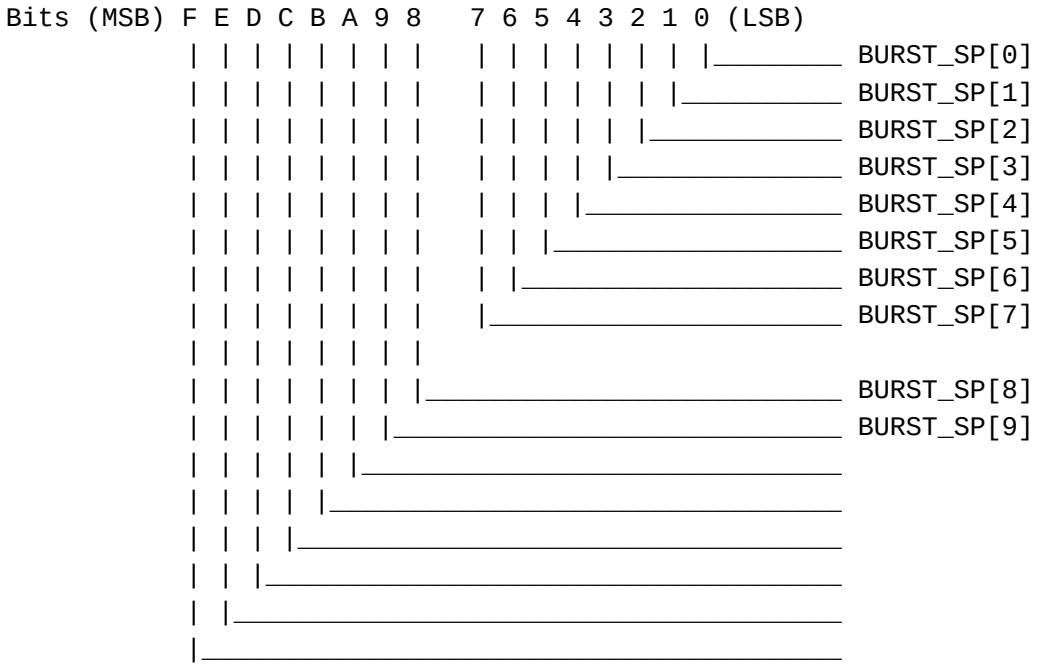
UV_INT_W_ST[8:0]: VGA Active Data Delayed Start - Chrominance Channel: This selects the beginning of active VGA data compensated for the internal chrominance delay of the encoder (UV_INT_RAM write reset position).

3.19 Port Address - BE470\H



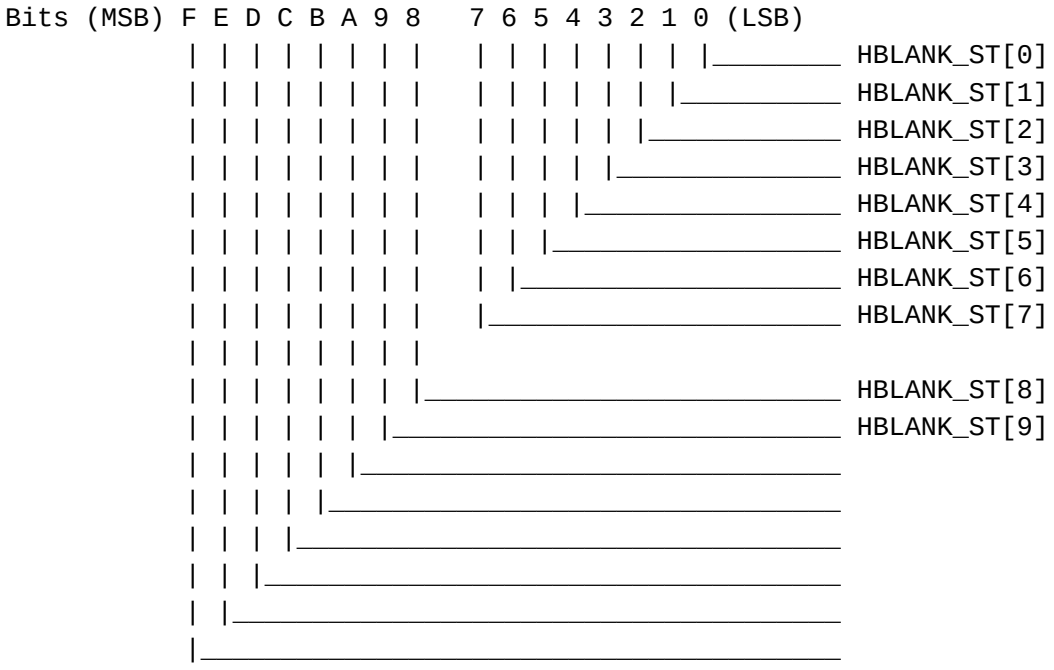
BURST_ST[9:0]: Start position of burstgate window.

3.20 Port Address - BE474\H



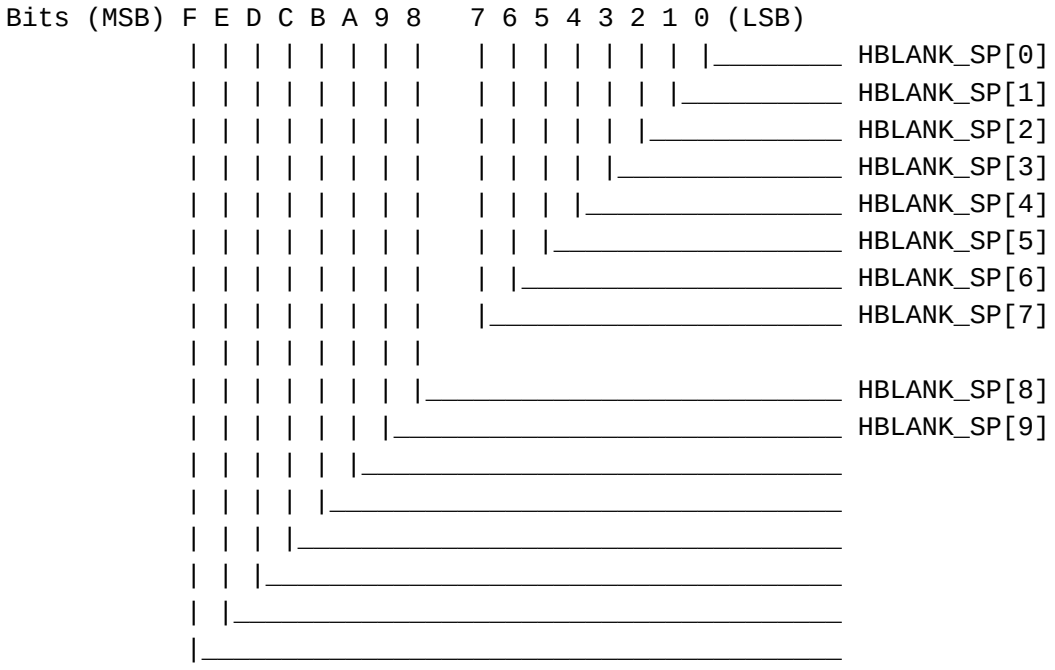
BURST_SP[9:0]: Stop position of burstgate window.

3.21 Port Address - BE478\H



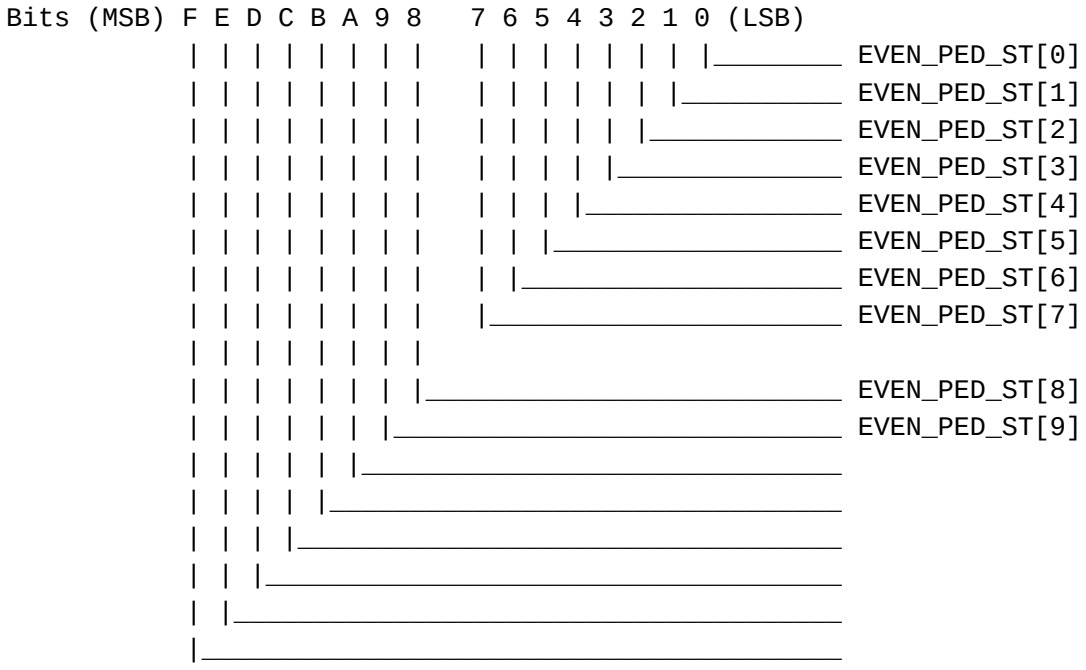
HBLANK_ST[9:0]: Horizontal Blanking Start Position.

3.22 Port Address - BE47C\H



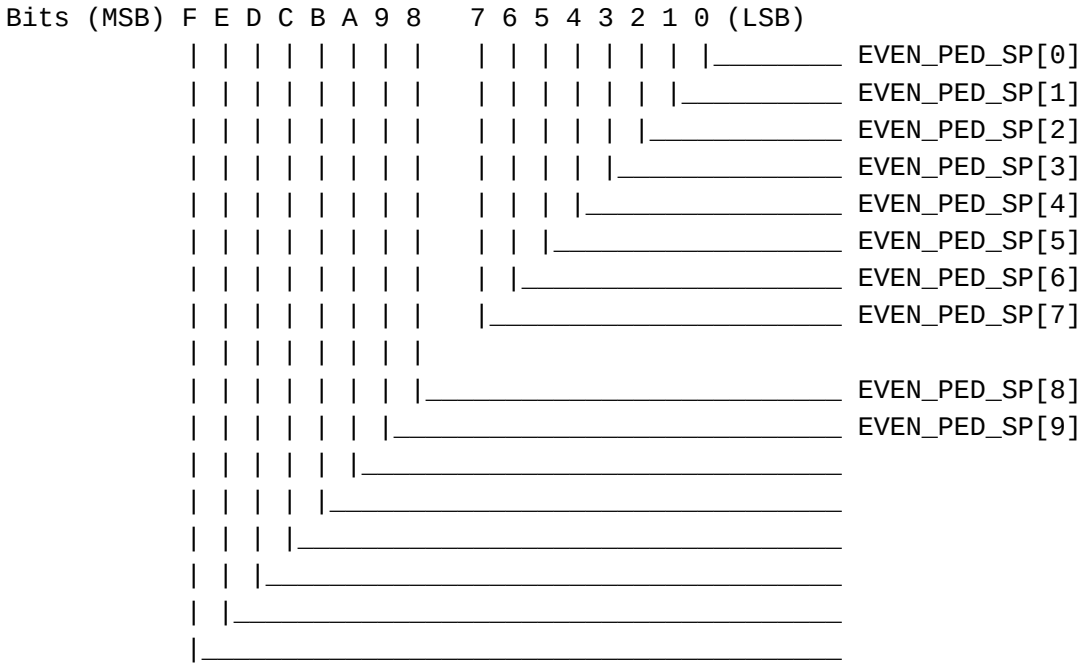
HBLANK_SP[8:0]: Horizontal Blanking Stop Position.

3.23 Port Address - BE480\H



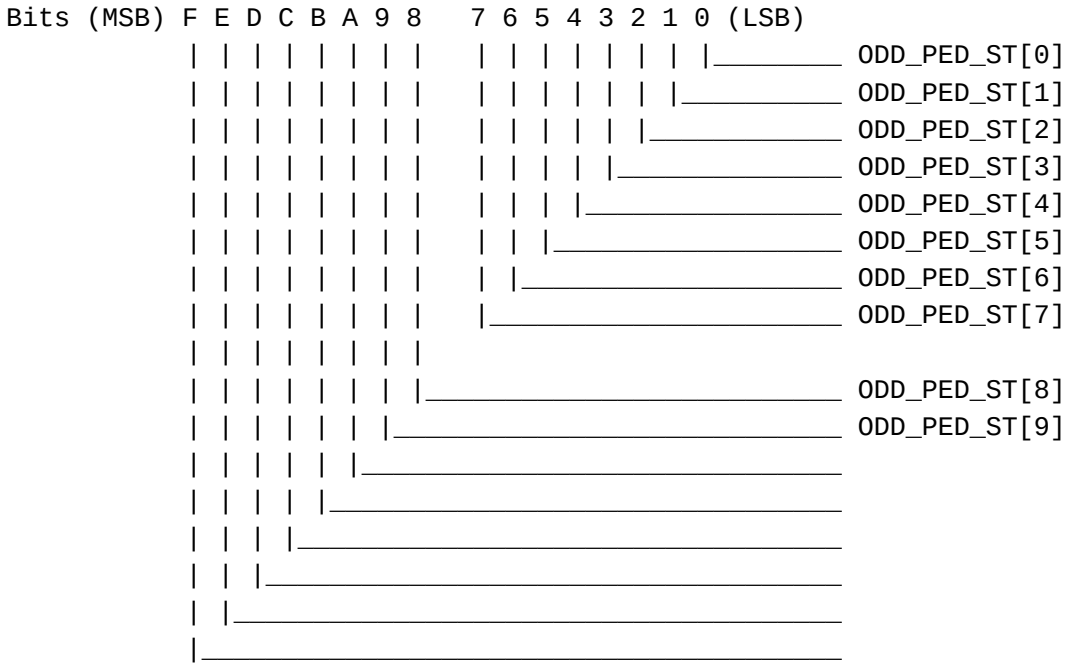
EVEN_PED_ST[9:0]: Start Position Of Pedestal Window On The Even Field.

3.24 Port Address - BE484\H



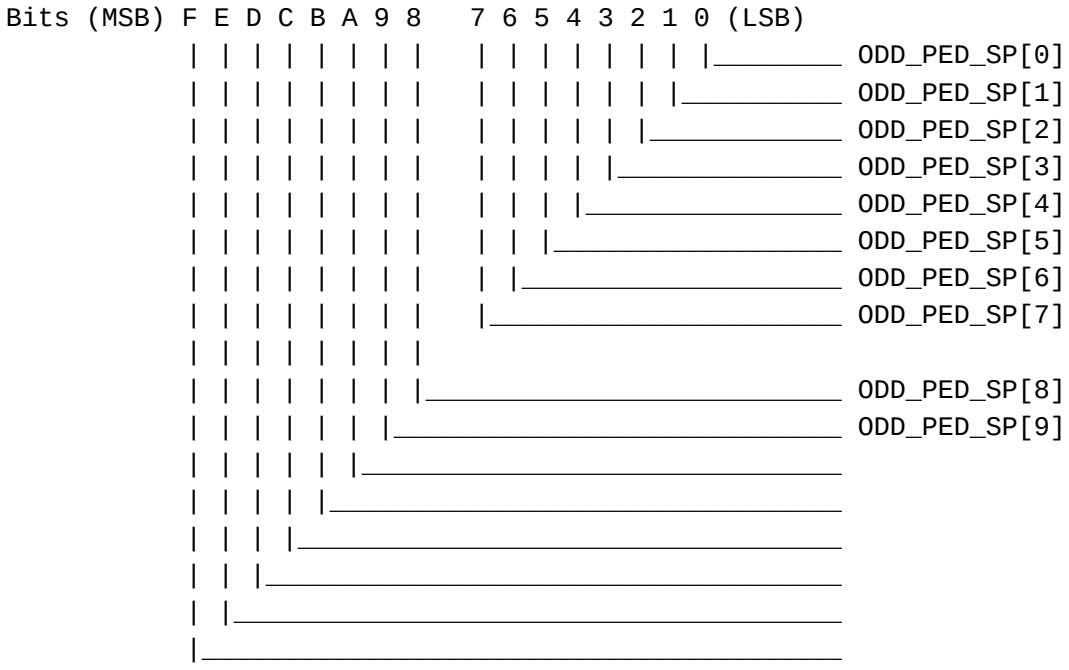
EVEN_PED_SP[8:0]: Stop Position Of Pedestal Window On The Even Field.

3.25 Port Address - BE488\H



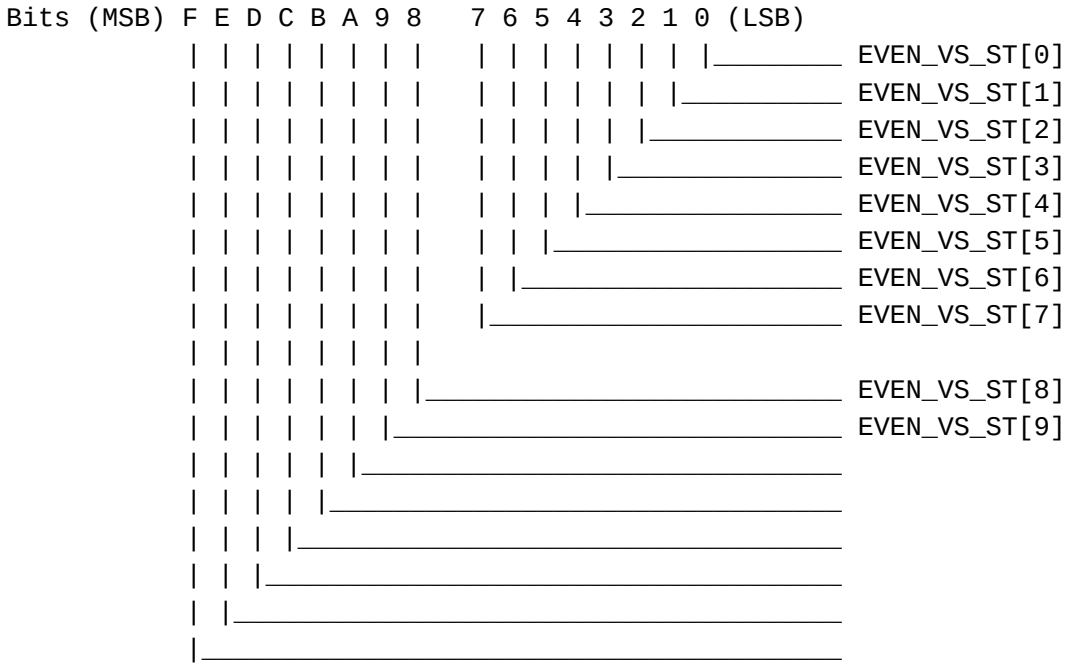
ODD_PED_ST[9:0]: Start Position Of Pedestal Window On The Odd Field.

3.26 Port Address - BE48C\H



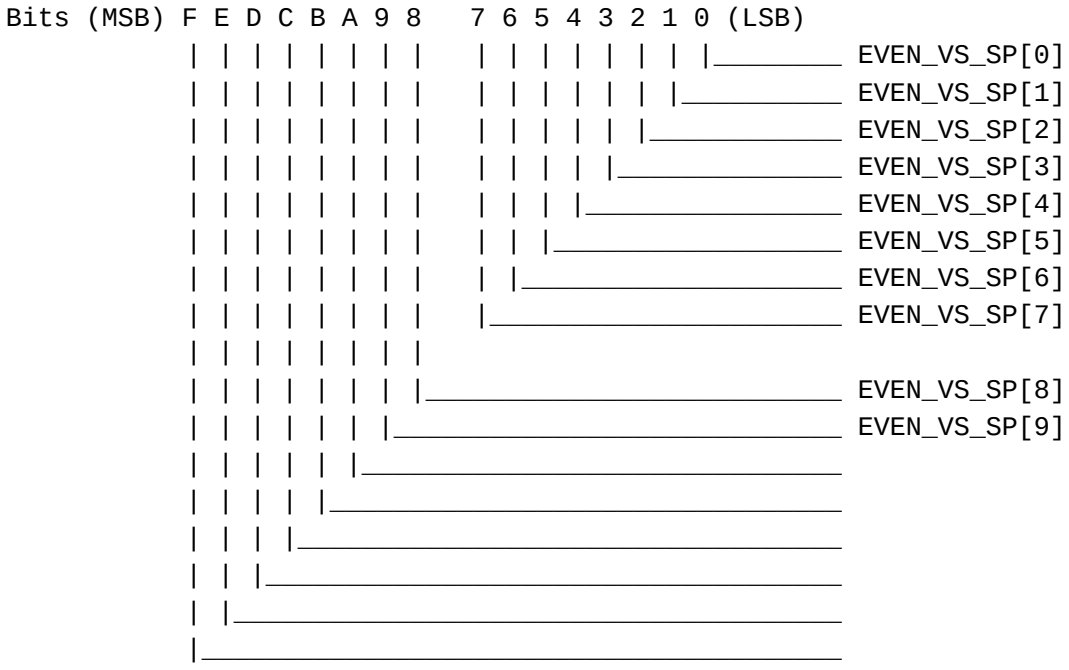
ODD_PED_SP[8:0]: Stop Position Of Pedestal Window On The Odd Field.

3.27 Port Address - BE490\H



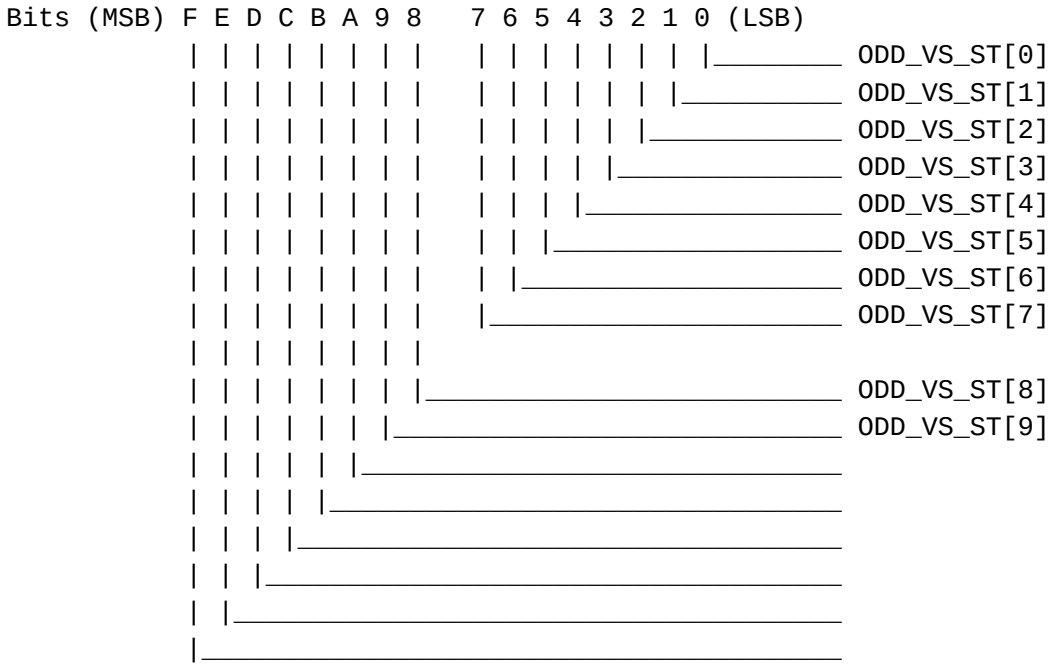
EVEN_VS_ST[9:0]: Start Position Of Vertical Sync On The Even Field.

3.28 Port Address - BE494\H



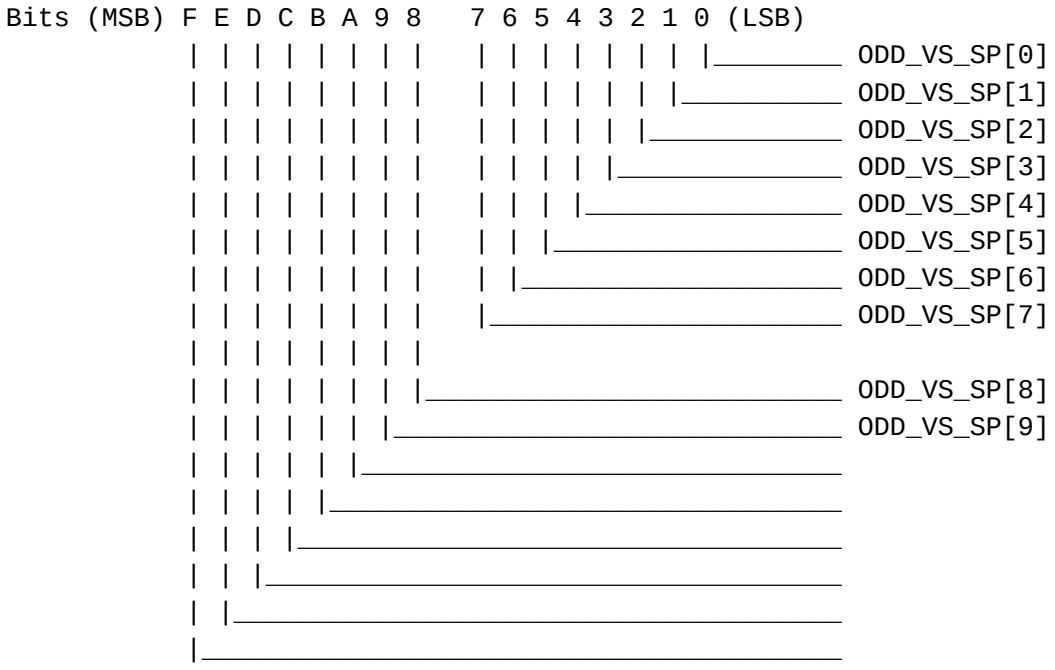
EVEN_VS_SP[8:0]: Stop Position Of Vertical Sync On The Even Field.

3.29 Port Address - BE498\H



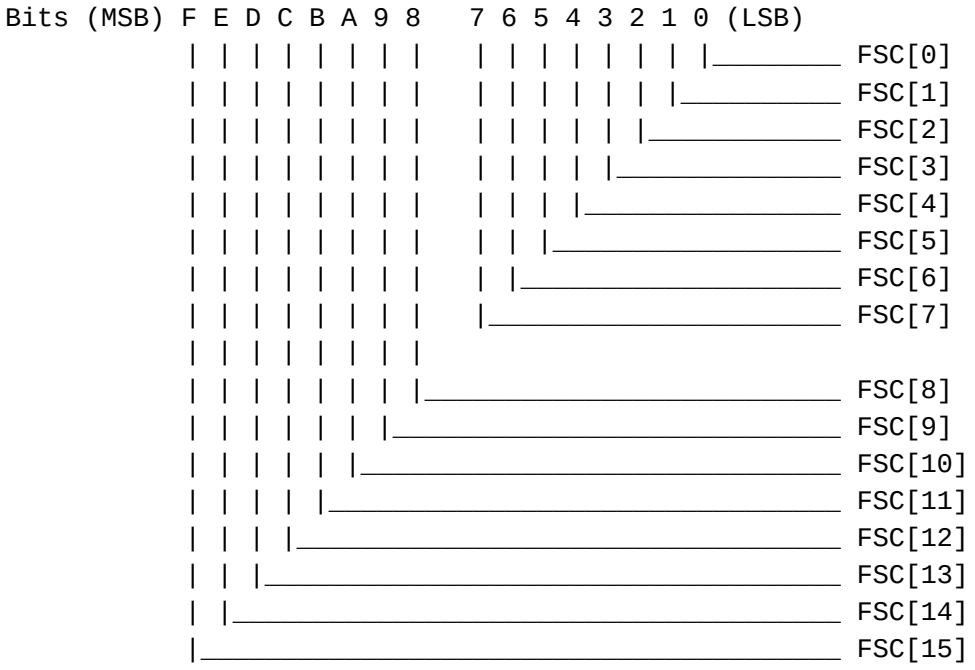
ODD_VS_ST[9:0]: Start Position Of Vertical Sync On The Odd Field.

3.30 Port Address - BE49C\H



ODD_VS_SP[8:0]: Stop Position Of Vertical Sync On The Odd Field.

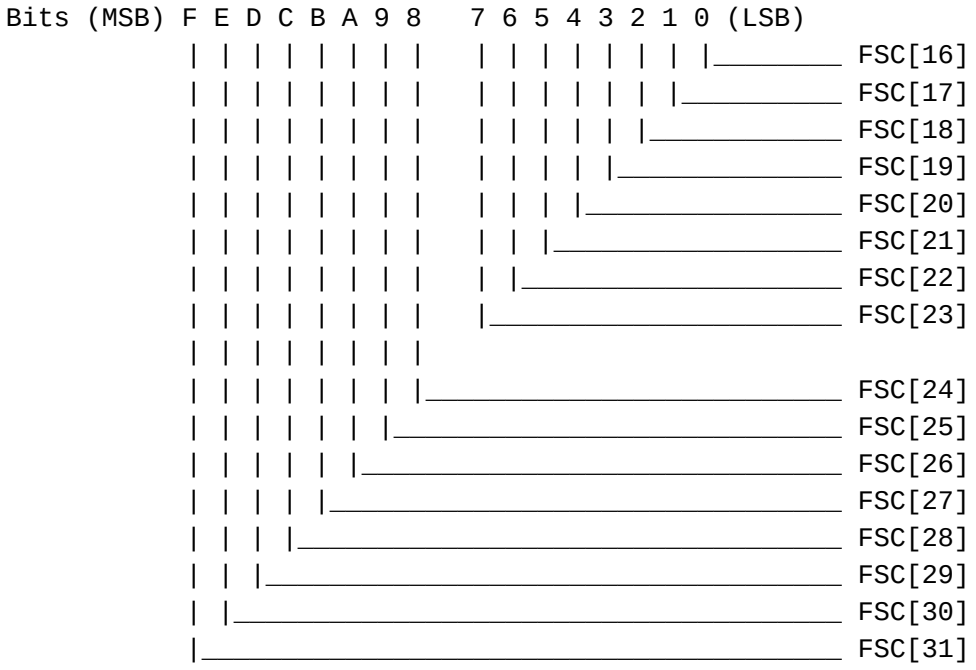
3.31 Port Address - BE4A0\H



FSC[15:0]: Subcarrier Frequency.

Note: If READFSC(bit 14 of index269\d(CPUA BE434\H)) is set to '1', then reading this register will read out ACC[15:0]

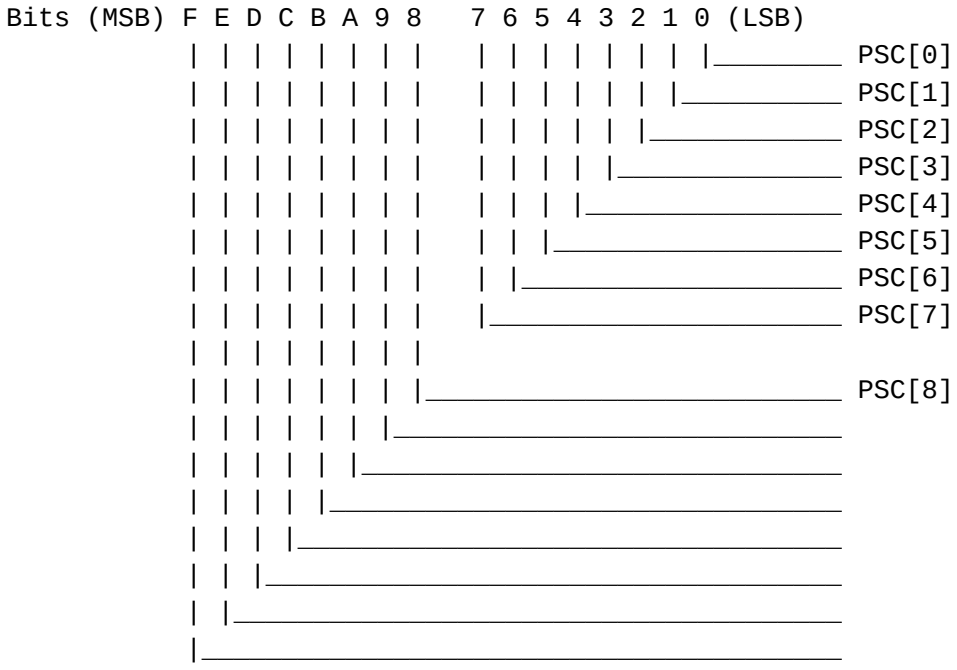
3.32 Port Address - BE4A4\H



FSC[31:16]: Subcarrier Frequency.

Note: If READFSC (bit 14 of index269\d(CPUA BE434\H)) is set to '1', then reading this register will read out ACC[31:16].

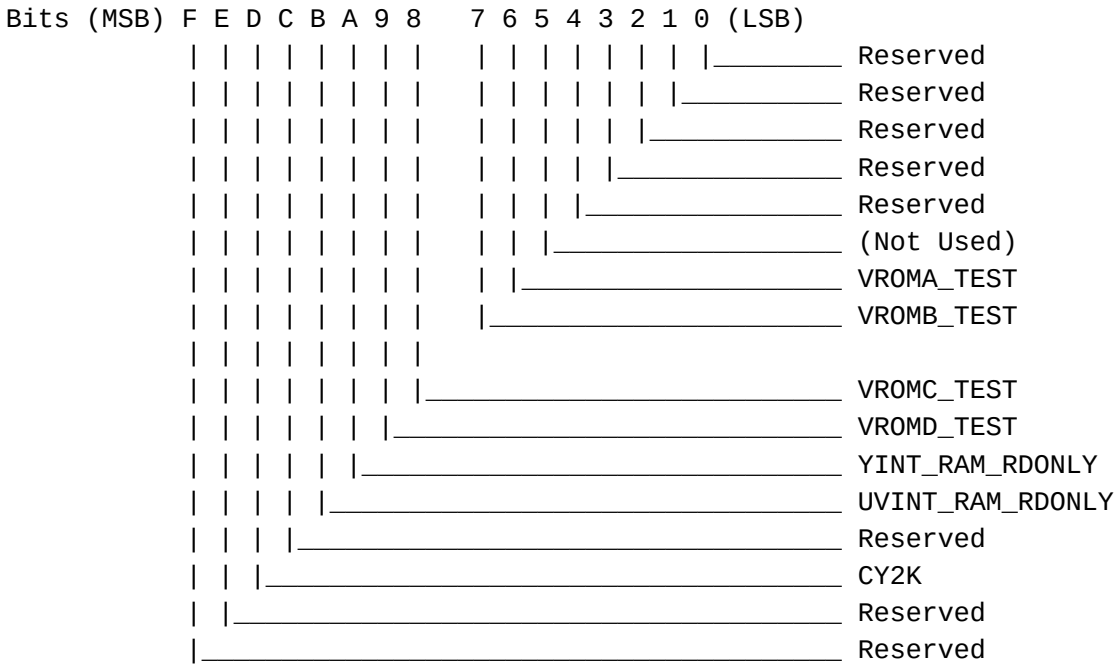
3.33 Port Address - BE4A8\H



PSC[8:0]: Subcarrier Phase.

3.34 Port Address - BE4AC\H

Miscellaneous debugging signals.

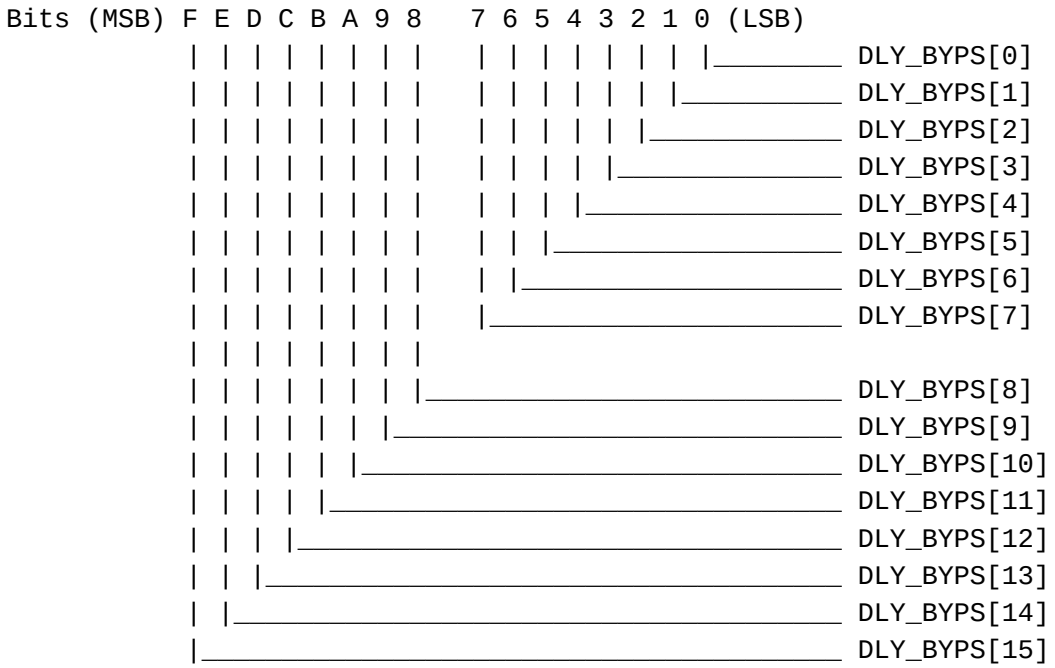


VROM[A,B,C,D]_TEST:	Used to test respective VROM.
YINT_RAM_RDONLY:	No address advancement for write address.
UVINT_RAM_RDONLY:	No address advancement for write address, except for UV_INT_RAM.
CY2K:	CyberPro2000 mode for Y,C,V.

3.35 Port Address - BE4B0\H

This register is reserved.

3.36 Port Address - BE4B4\H

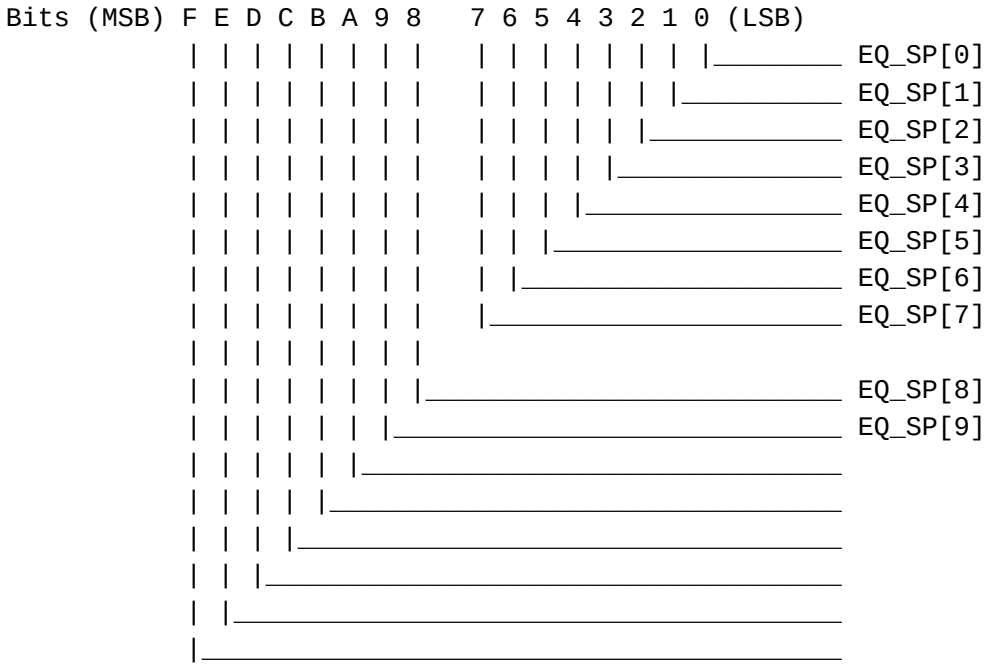


DLY_BYPS[15:0]: Used to control which y signals need to be brought out.

3.37 Port Address - BE4B8\H

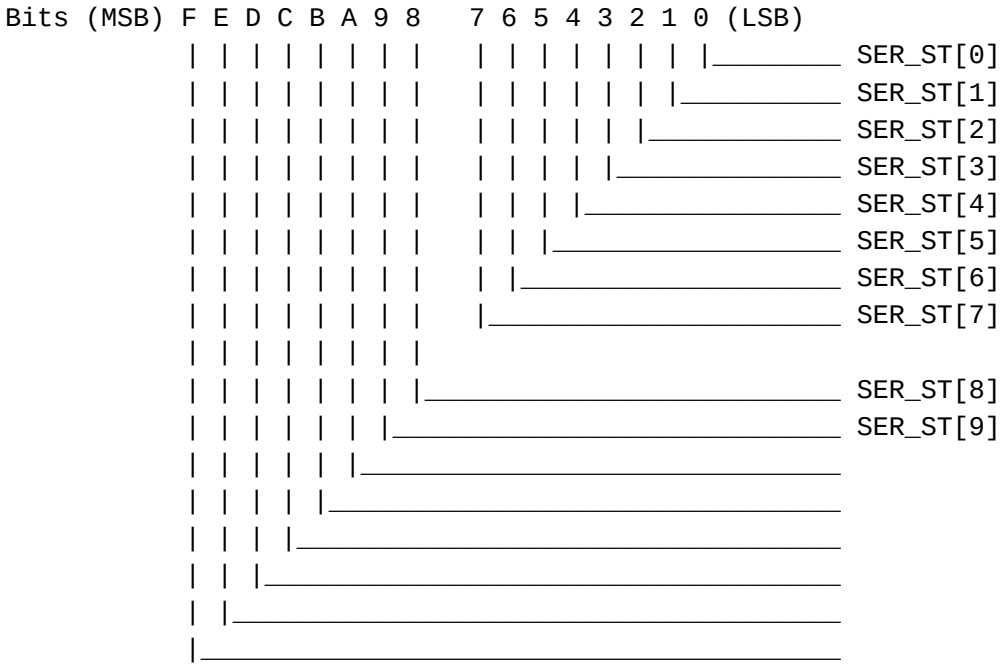
This register is reserved.

3.38 Port Address - BE4BC\H



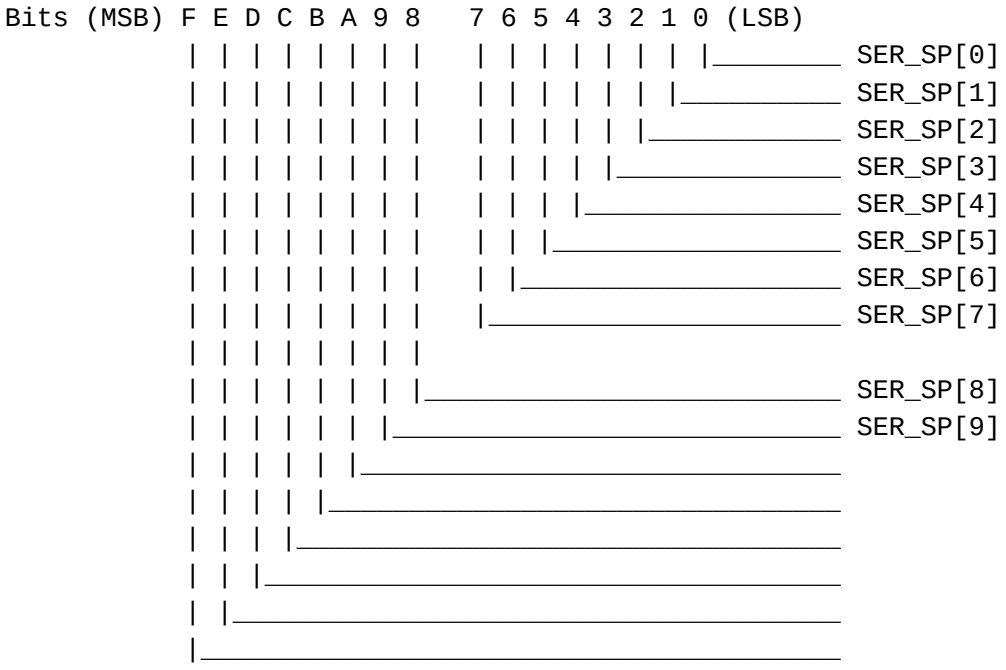
EQ_SP[9:0]: Used as stop position of equalization pulse.

3.39 Port Address - BE4C0\H



SER_ST[9:0]: Used as start position of serration pulse.

3.40 Port Address - BE4C4\H



SER_SP[9:0]: Used as stop position of serration pulse.

3.41 Port Address - BE4C8\H

This register is reserved.

3.42 Port Address - BE4CC\H

This register is reserved.

3.43 Port Address - BE4D0\H

This register is reserved.

3.44 Port Address - BE4D4\H

This register is reserved.

3.45 Port Address - BE4D8\H

This register is reserved.

3.46 Port Address - BE4DC\H

This register is reserved.

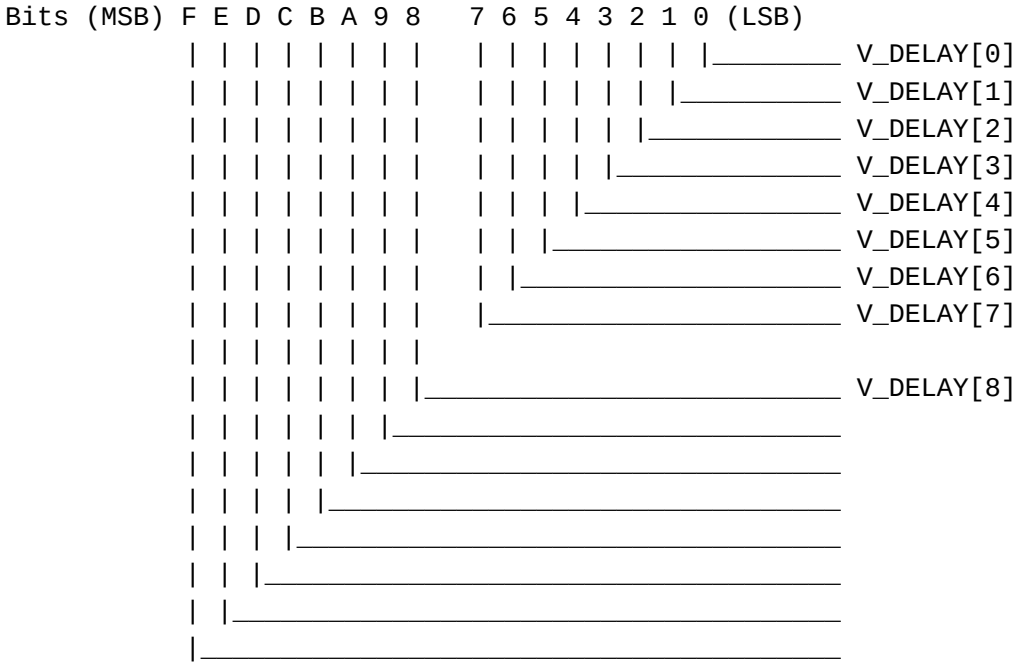
3.47 Port Address - BE4E0\H

This register is reserved.

3.48 Port Address - BE4E4\H

This register is reserved.

3.49 Port Address - BE4E8\H



V_DELAY[8:0]: TV Vertical position relative to VGA horizontal sync.

3.50 Port Address - BE4EC\H

This register is reserved.

3.51 Port Address - BE4F0\H

This register is reserved.

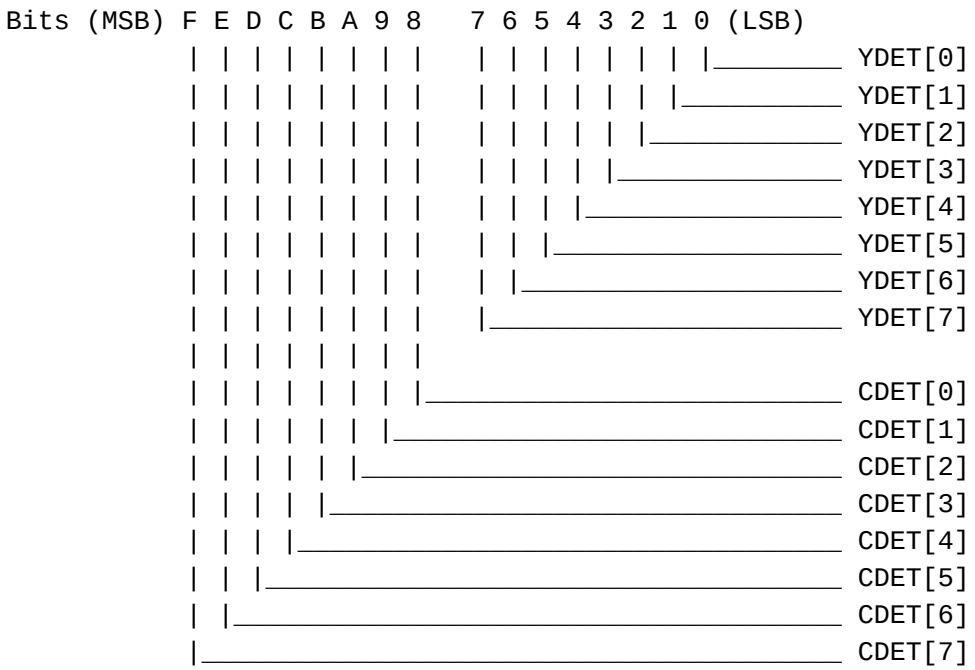
3.52 Port Address - BE4F4\H

This register is reserved.

3.53 Port Address - BE4F8\H

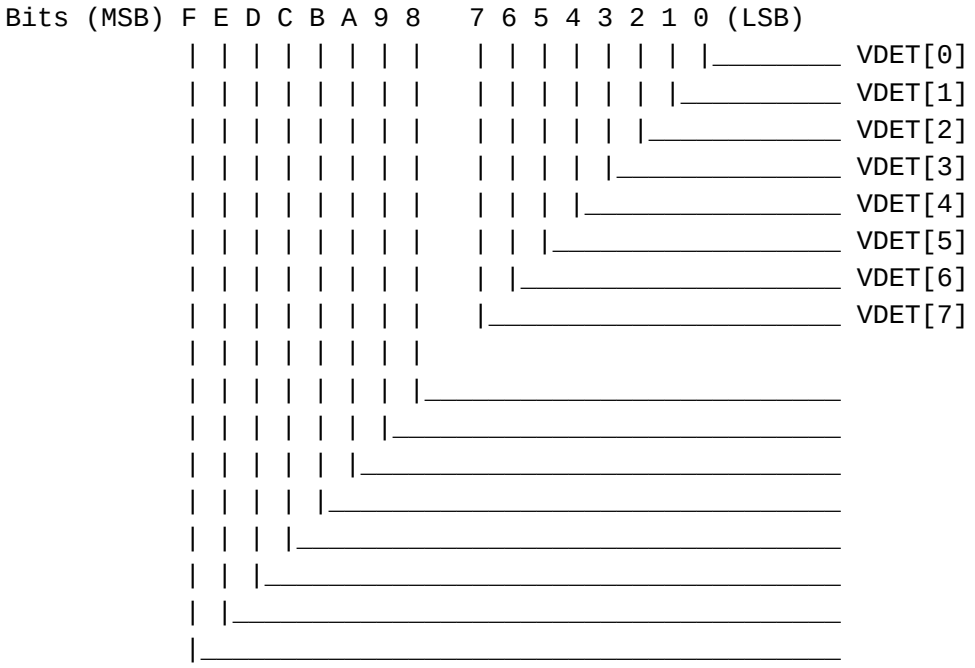
This register is reserved.

3.54 Port Address - BE4FC\H



YDET[7:0], CDET[7:0]: Registers for TV Sense Detection: The values in this register replace the normal data values for C,Y when TVSEN is ON.

3.55 Port Address - BE500\H

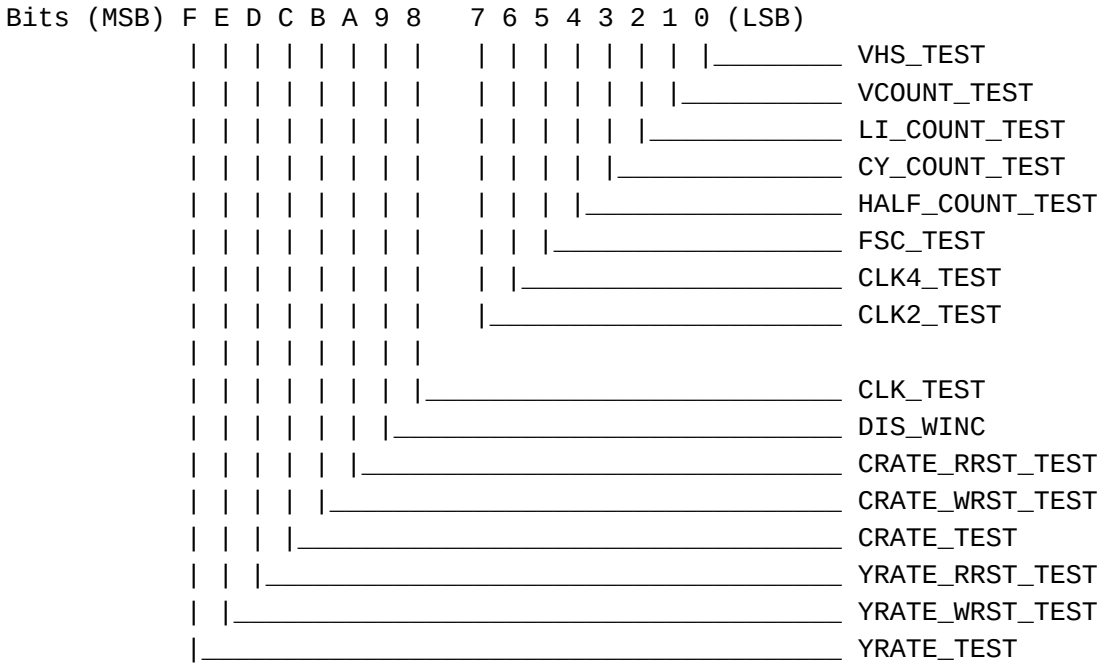


VDET[7:0]: Registers for TV Sense Detection: The values in this register replace the normal data values for V(composite) when TVSEN is ON.

3.56 Port Address - BE504\H

This register is reserved.

3.57 Port Address - BE508\H



ADR_CNTR_TEST[15:0]: Registers for testing the miscellaneous RAM address counter.

3.57.1 Examples for Testing Various Counters

1. To test the FSC counter:

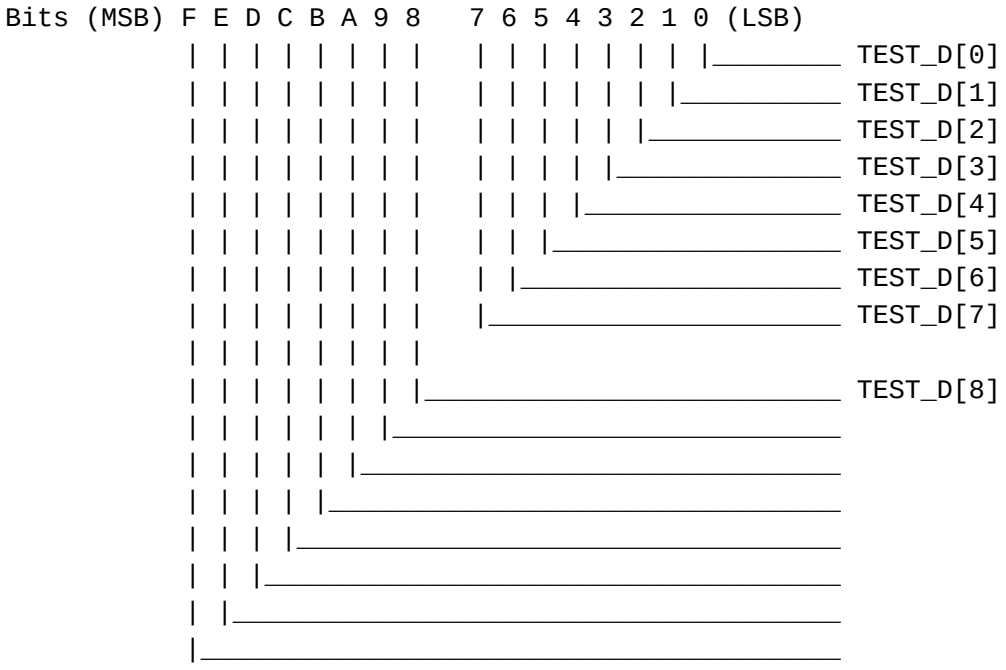
```
test_fsc()
{
        /* turn on fsc_test */
        memw(322,"0020");
        /* write fscl, fsch now */
        memw(296,"1234");
        memw(297,"5678");
        /* make clk2_test go from low->high */
        memw(322,"00A0");
        /* set read_fsc */
        memw(269,"4000");
        /* read fscl, fsch now*/
        memr(296);
        memr(297);

        /* let's turn off fsc_test */ /* since test means load */
        memw(322,"0000");
        /* make clk2_test go from low->high */
        memw(322,"0080");
        /* ACF02468 <- 56781234 + 56781234  */
        memr(296);
        memr(297);
        /* reset the toggle pointer */
        memw(322,"0000");
}
```

2. To test the crate counter:

```
/* only test write address */
/* NOTE: the highest count is 447\d 1BF\h for crate */
test_crate()  /* uvinta */
{
        /* turn on uvinta_test */
        memw(322,"1000");
        /* load up test_d, with A168 */
        memw(323,"A168");
        /* make clk2_test go from low->high */
        memw(322,"1080");
        /* set read_uvinta - bit11 of index269 */
        memw(269,"0800");
        /* read test_d now*/
        memr(323); /* should be A168\h */
        /* make clk2_test go from low->high */
        memw(322,"0000");
        memw(322,"0080");
        /* read test_d now*/
        memr(323); /* should be 169\h now */
        memw(322,"0000");
}
```

3.58 Port Address - BE50C\H



TEST_D[8:0]: Registers for loading/reading values of miscellaneous counters (CY_COUNT[9:0], HALF_COUNT[8:0], LI_COUNT[9:0], YINTADDR[9:0], UVADDR[8:0], Y_DLY_ADDR[9:0]) during test mode.

Note: Since this index is also used for reading out different counters during test mode, be sure to turn off all the 'read bits' in index 269 for testing this particular register. Otherwise, corresponding counter values are read out.

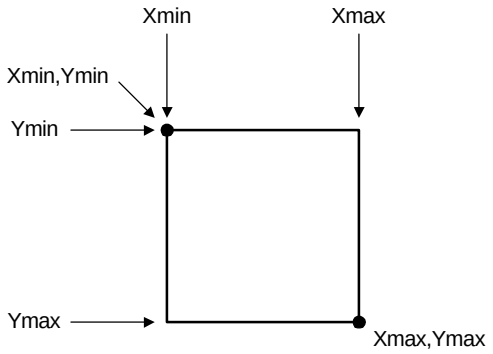
3.59 Port Address - BE510\H

This register is reserved.

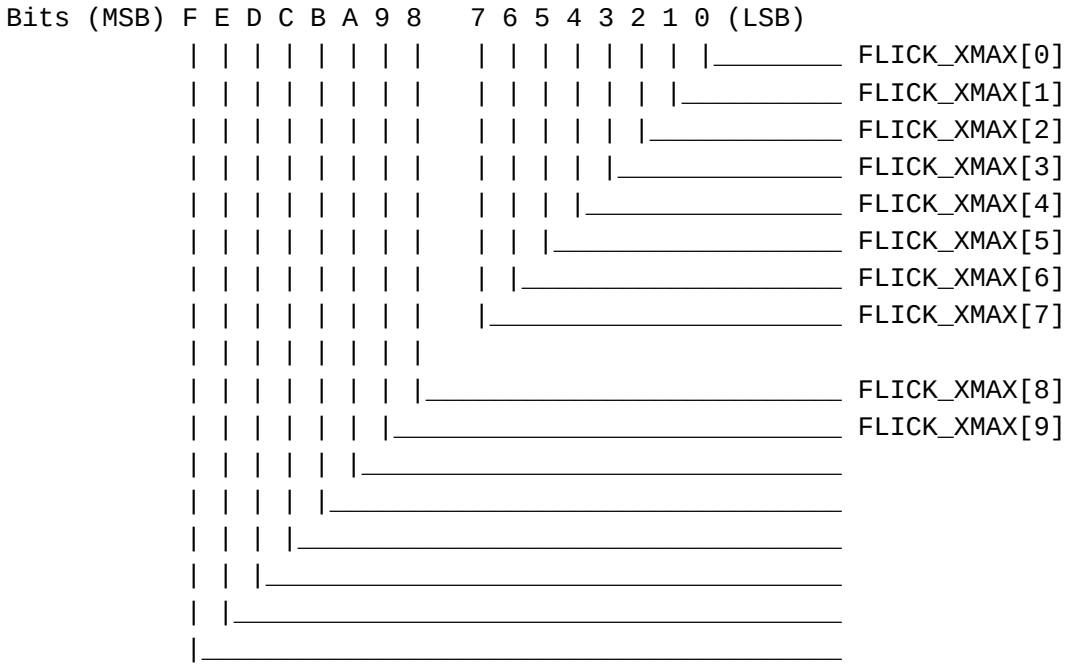
3.60 Port Address - BE514\H

```
Bits (MSB) F E D C B A 9 8   7 6 5 4 3 2 1 0 (LSB)
           | | | | | | | |   | | | | | | | |_________ FLICK_XMIN[0]
           | | | | | | | |   | | | | | | |___________ FLICK_XMIN[1]
           | | | | | | | |   | | | | | |_____________ FLICK_XMIN[2]
           | | | | | | | |   | | | | |_______________ FLICK_XMIN[3]
           | | | | | | | |   | | | |_________________ FLICK_XMIN[4]
           | | | | | | | |   | | |___________________ FLICK_XMIN[5]
           | | | | | | | |   | |_____________________ FLICK_XMIN[6]
           | | | | | | | |   |_______________________ FLICK_XMIN[7]
           | | | | | | | |
           | | | | | | | |_________________________ FLICK_XMIN[8]
           | | | | | | |___________________________ FLICK_XMIN[9]
           | | | | | |_____________________________
           | | | | |_______________________________
           | | | |_________________________________
           | | |___________________________________
           | |_____________________________________
           |_______________________________________
```

FLICK_XMIN[9:0]: Video window flicker control Xmin.

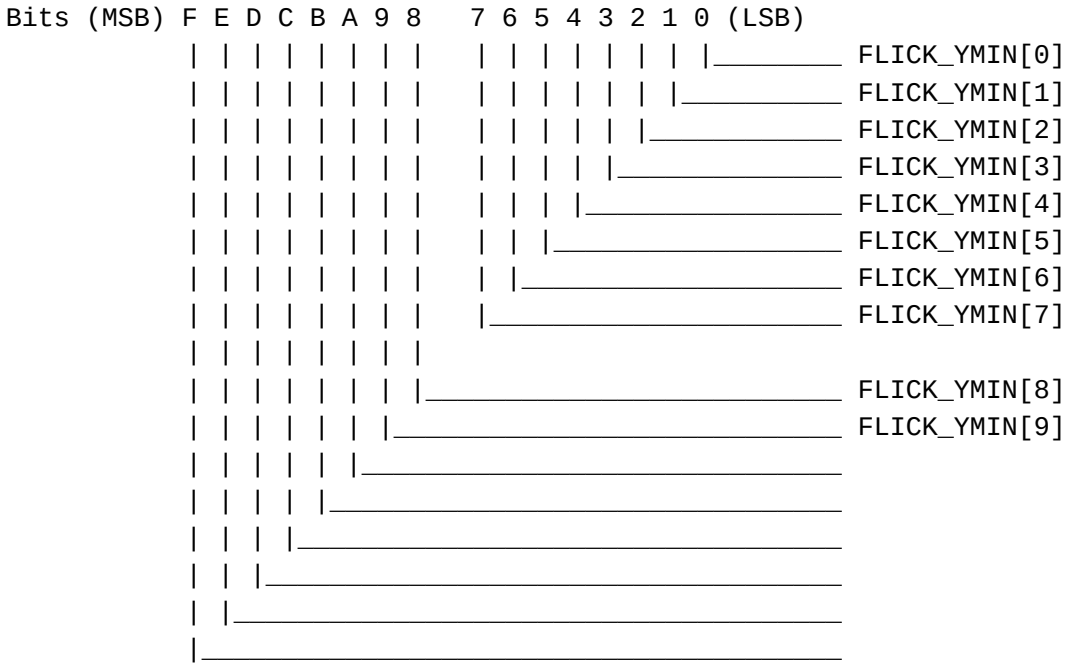


3.61 Port Address - BE518\H



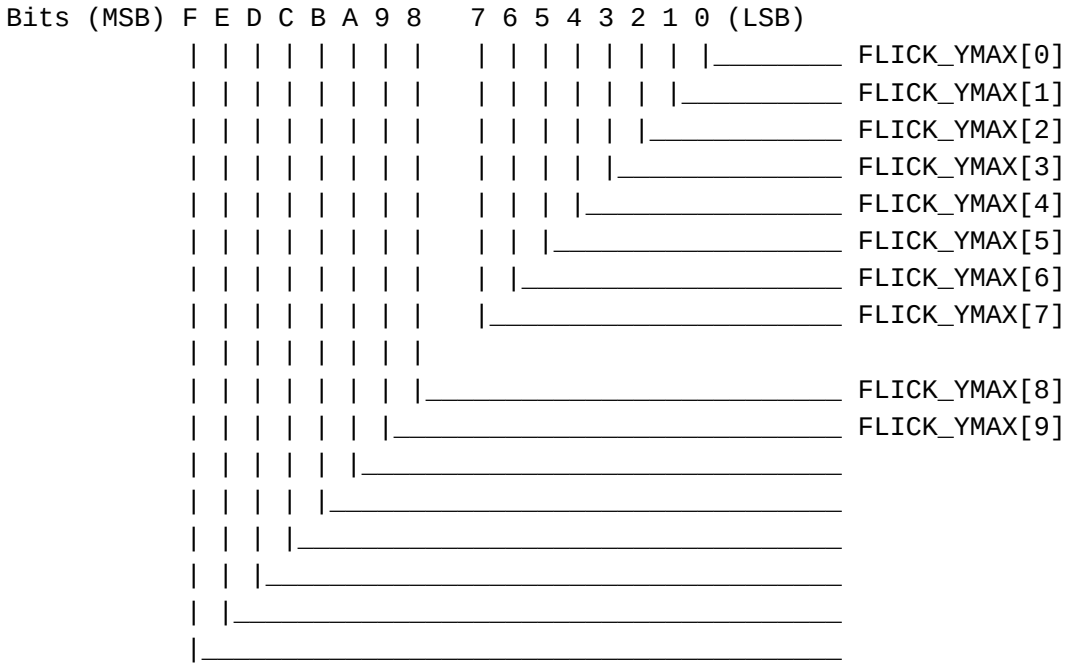
FLICK_XMAX[9:0]: Video window flicker control XMAX.

3.62 Port Address - BE51C\H



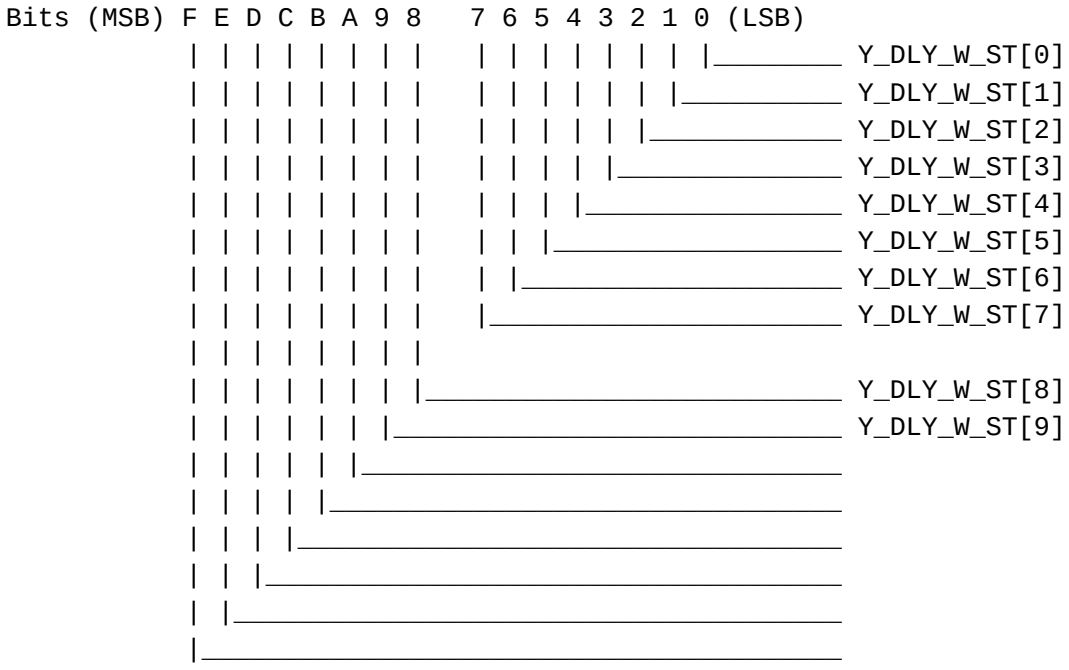
FLICK_YMIN[9:0]: Video window flicker control Ymin.

3.63 Port Address - BE520\H



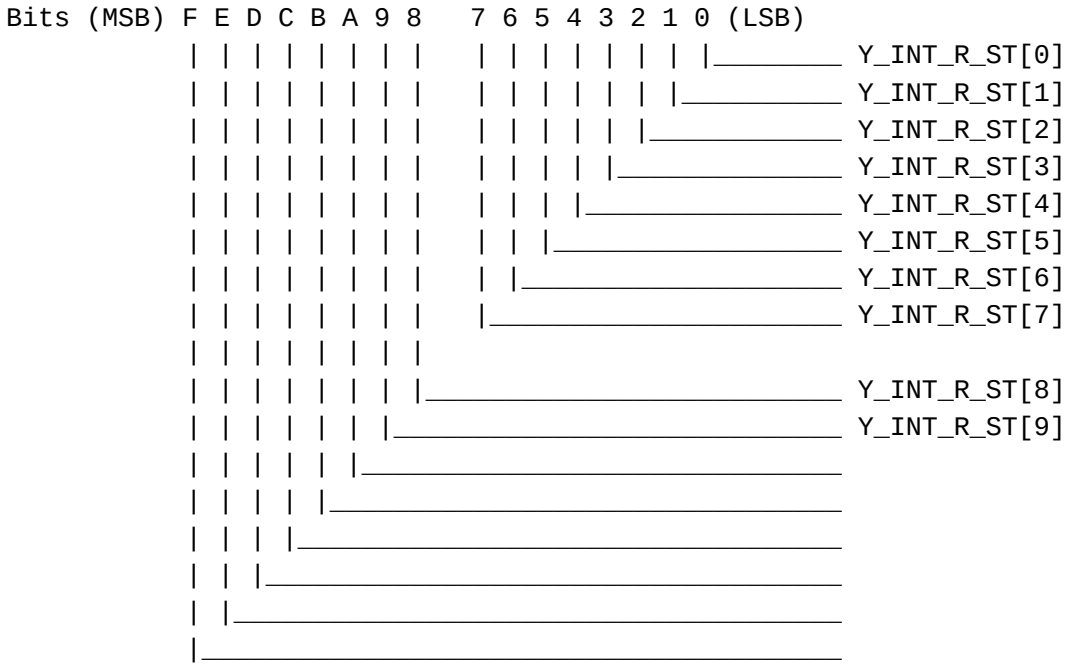
FLICK_YMAX[9:0]: Video window flicker control YMAX.

3.64 Port Address - BE524\H



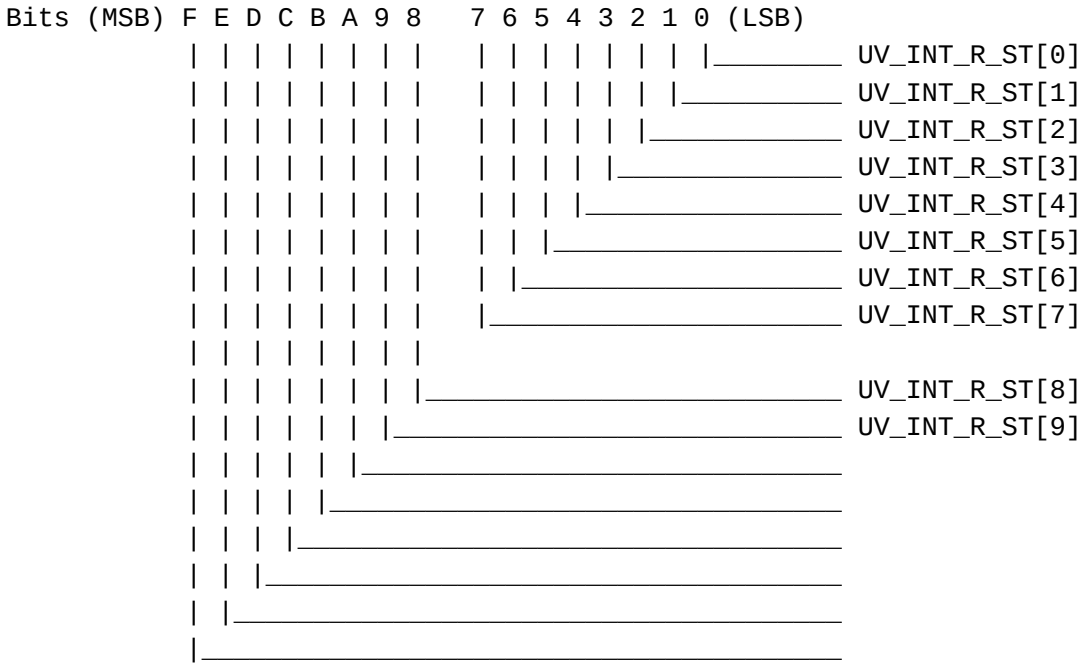
Y_DLY_W_ST[9:0]: Y delay RAM write reset position.

3.65 Port Address - BE528\H



Y_INT_R_ST[9:0]: Y interlace RAM read reset position.

3.66 Port Address - BE52C\H



UV_INT_R_ST[9:0]: UV interlace RAM read reset position.