IGS Technologies

CyberPro™ 2010

CyberPro2010 Multimedia Graphics Accelerator and Enhanced Digital TV Encoder

The CyberPro2010 merges the functions of a digital NTSC/PAL TV encoder, high-resolution graphics accelerator and a flexible CPU Bus interface into a single IC. These three functions combine to make the CyberPro2010 the ideal solution for Internet Web Browser and other applications. The CyberPro2010 also features an ITU-BT656/601 digital video input port which interfaces to standard video and MPEG decoders for enhanced TV and the Internet Web Browser combinations or video phone applications.

In PC applications the CyberPro2010 supports resolutions up to 1600 x 1200 and color depths up to 16.8 million colors.

Key Features

Graphics

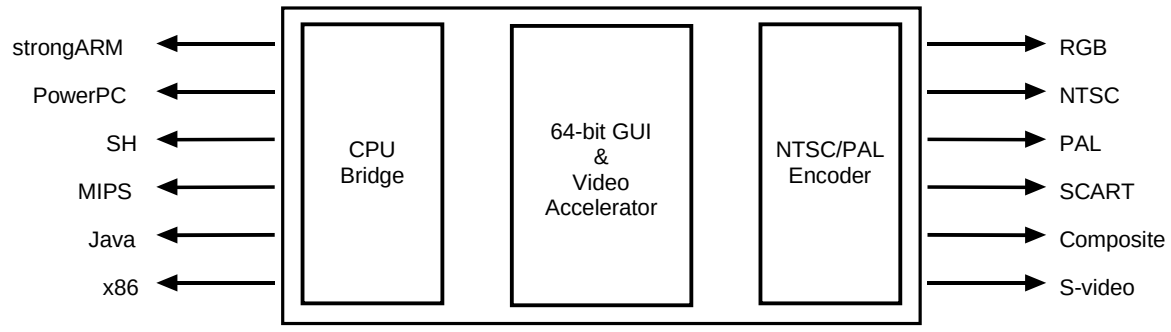
- 64-bit GUI
- 200 MHz RAMDAC
- Shadow register compatibility for popular video games

TV Encoder

- 6 on-chip DACS provide simultaneous S-video, composite (CVBS) and RGB/SCART outputs or simultaneous VGA and TV outputs (S-video and composite or RGB/SCART)
- Fully programmable field, line, and subcarrier frequencies to suit worldwide TV standards

Flexibus™

- Direct interface to 486 embedded processors via VL bus, including AMD Elan 400/410, Intel 486
- Direct interface to Pentium/RISC CPU via PCI bus/ bridge including Sparc/Java
- Direct interface to other RISC CPU including NEC, SH, Motorola PowerPC™



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Features

Graphics

- 64-bit GUI
- 200 MHz RAMDAC
- Dual clock
- Supports EDO DRAM from 1MB up to 4MB
- Shadow registers for complete compatibility with DOS™, Windows™, and TV video games
- Color expansion for all graphics modes
- Large data buffers for fast screen-to-screen BitBLTs
- Accelerated 8/16/24/32 BPP Packed modes
- 64-bit BitBLT engine
- Relocatable memory and memory-mapped I/O registers, supporting Java™, RISC, and open firmware
- Independent memory apertures allow BitBLT and CPU/video concurrent operation for optimized video playback.
- Big Endian / Little Endian support

TV Encoder

- One crystal for NTSC, PAL and VGA outputs
- NTSC (640x480@60Hz), PAL (800x600/720x540/ 640x480@50Hz)
- 6 on-chip DACS provide simultaneous S-video, composite (CVBS) and RGB/SCART outputs or simultaneous VGA and TV outputs (S-video and composite or RGB/SCART)
- Programmable field, line, and subcarrier frequencies to meet worldwide TV standards
- Display graphics on monitor while displaying graphics or video on a TV DuoVision™ Dual Display.
- 3 line flicker filter
- 8-bit DAC's (9-bit on composite output)
- Programmable flicker filter bypass on interlaced video
- 11-bit high precision PLL for subcarrier and clock generation

Flexibus™

- Direct interface to 486 embedded processors via VL bus, including AMD Elan 400/410, Intel 486
- Direct interface to Pentium/RISC CPU via PCI bus/ bridge including Sparc/Java
- Direct interface to other RISC CPU including NEC, SH, Motorola PowerPC™
- High-throughput CPU bus interface
- Large write buffer allows sustained zero-wait-state bursts
- PCI v2.1-compliant

Video Input

- VBI data passthrough for Intercast, Teletext, closed caption support
- ITU-BT656, ITU-BT601 8-bit video input interface
- High quality horizontal and vertical interpolation with jagged edge smoothing
- High quality multi-tap filtering
- X and/or Y mirror support for video conferencing
- Double buffering
- YUV 4:2:2, YUV 4:2:0 or RGB16

Video Window and Video Display

- 3 video windows plus PIP
- Color key
- Chroma key
- DirectDraw MPEG-1 playback with software using hardware assistance
- X and Y linear interpolated scaling and zooming

Frame Buffer

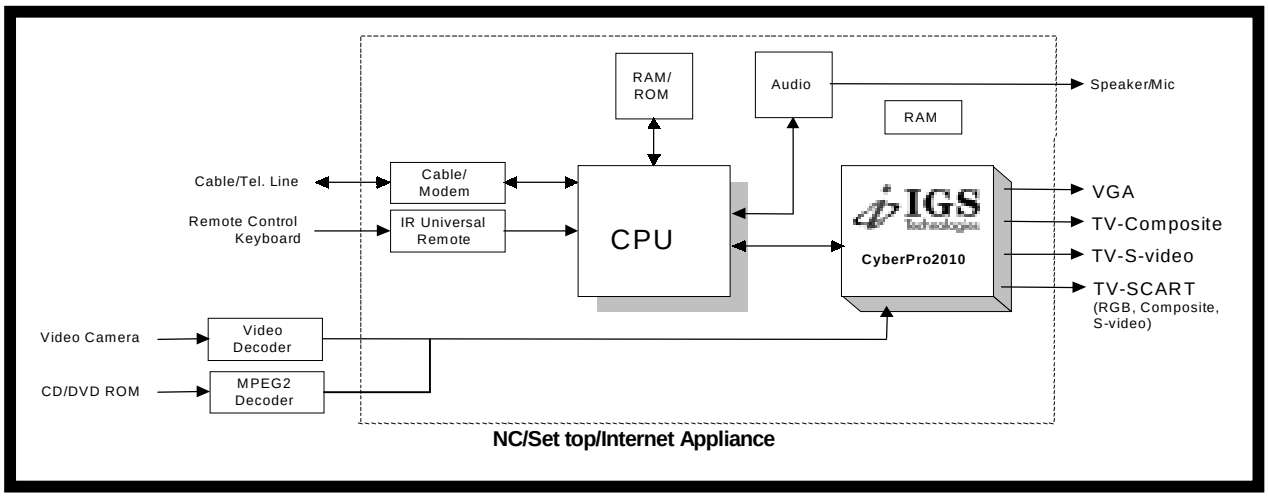
- Multiformat Frame Buffer:YUV-16 true color video with 8/16/24/32-bit graphics
- 64-bit DRAM interface optimized for EDO DRAM
- 100 MHz MCLK offers up to 320 Mbytes/sec. peak bandwidth
- 256 x 16, 128 x 16, 128 x 32-bit DRAM options

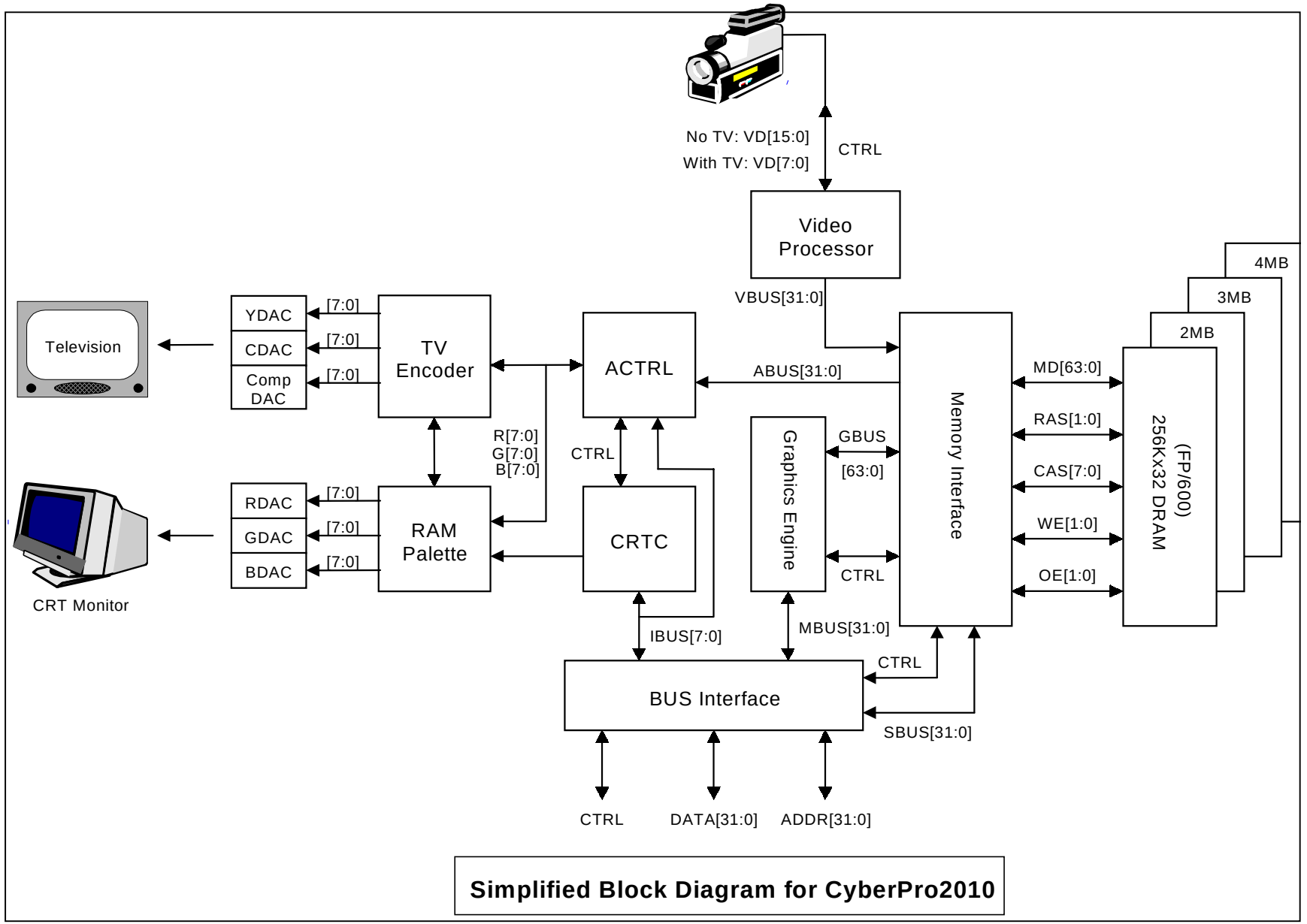
Software Compatibility

- VGA/SVGA/VBE 2.0/DPMS BIOS
- Windows 98™, Windows 95™, Windows™ 3.X, NT 3.X/4.0
- Direct Draw™, DCI and Video Capture
- OS/2 2.X/3.X
- AutoCAD™, PCAD™, WordPerfect™ and Lotus 123™

Applications

- Internet Web Browsers
- TV and Internet Browser combinations
- Video Phone/Video Conferencing on TV
- PC TV
- Video capture
- Home video editing
- Digital Camera display on TV





Simplified Block Diagram for CyberPro2010

Functional Description

The CyberPro2010 integrates three major components of NC/SetTop/Internet Appliance/TV design; a CPU bridge (Flexibus™ interface), GUI/Video Accelerator and a NTSC/PAL TV Encoder. In addition, the CyberPro2010 integrates a high speed 200 MHz RAMDAC and clock.

The CyberPro2010 has a 64-bit GUI multimedia accelerator that interfaces to EDO DRAM frame buffer with sizes from 1MB to 4MB. It provides VGA output resolution up to 1600x1200.

Graphics Engine

The graphics engine is a 64-bit DRAM based XVGA controller with hardware accelerated BitBLT, video playback, and video capture to the frame buffer.

It includes a BitBLT engine for block transfers within display memory at full memory bandwidth. System to display transfers can also be accomplished with the BitBLT engine.

The BitBLT control registers are double-buffered and memory mapped. Double-buffered registers allow concurrent operation of the host and the BitBLT engine. The host can prepare and load the parameters for operation n+1 while the BitBLT engine is executing operation n. When the current operation completes, the BitBLT engine automatically loads and begins with the parameters for the next operation.

All 16 two-operand ROPS (raster operations) are implemented in hardware. Color expansion leverages host bandwidth by a factor of up to 32 times .

Memory Interface

The memory sequencer controls access to the display memory. It ensures that the necessary screen refresh and dynamic memory refresh cycles are executed, and that the remaining memory cycles are made available for CPU read/write operations, BitBLT read/write operations, and video port write operations.

The interface consists of a memory arbiter and memory controller. It accepts requests from the CRT controller. It uses the display FIFO to deliver data to the display pipeline, and the write buffer to transfer data to the graphics controller.

The memory controller generates the signals and addresses necessary for accessing display memory. The memory controller is driven by MCLK (memory clock) which can be optimized for the speed of the DRAM used, independent of the VCLK (video clock). The memory controller can generate optimized timing for EDO DRAMs and operate with an MCLK of up to 100 MHz. The memory arbiter and host bus interface are also driven by the MCLK.

The memory arbiter allocates bandwidth to the five functions that compete for the frame buffer bandwidth: DRAM refresh, screen refresh, video port read/writes, and CPU and BitBLT access.

DRAM refresh is handled invisibly by allocating a selectable number of CAS#-before-RAS# refresh cycles at the beginning of each scan line. Screen refresh, video port writes, and CPU and BitBLT accesses are allocated cycles according to the FIFO control parameters. Priority is given to screen refresh and Video port writes.

Video Processor

The CyberPro2010 combines a video port with a multi-format frame buffer for cost effective video playback. The video port captures real-time video into the frame buffer with optional data reduction. The video can be displayed in a hardware video window with optional interpolated zooming.
Video can be of a different format (for example, (16 bit YUV 4:2:2) than the graphic format (for example, 8, 16 or 24 bits). The graphics controller provides access from the CPU to memory. It performs text manipulation, data rotation, color mapping, and other operations. These operations are typically performed in the graphics controller for VGA-compatible applications. Other applications can take advantage of the BitBLT engine.

CRTC

The CRT controller generates programmable horizontal and vertical synchronization signals for the CRT display. The CyberPro2010 supports all standard VGA modes, as well as extended resolutions and is software-compatible with the IBM VGA specification.

ACTRL

The attribute controller controls font, color, blinking, and underline in alphanumeric modes.

Programmable Dual-Frequency Synthesizer

The CyberPro2010 includes an integrated dual-frequency synthesizer that can be programmed to generate VCLK for all supported screen formats, and MCLK used by the sequencer. The VCLK synthesizer supports a pixel clock of up to 160 MHz. The MCLK synthesizer can be programmed up to 100 MHz. The dual-frequency synthesizer includes an on-chip oscillator that requires an inexpensive two-pin 14.31818 MHz crystal. However, a crystal oscillator is recommended if the TV encoder subcarrier frequency is required to stay within specified limits from system to system.

RAM Palette

The RAM Palette contains an 8-bit per color look up table and three 8-bit digital-to-analog converters. It is programable for 256 simultaneous colors from a palette of 256K, or the look up table can be bypassed in direct-color modes. In direct-color modes each 16 or 24-bits define one pixel giving 64k or 16.8M colors.

TV Encoder

The TV encoder encodes the digital data stored in the frame buffer and converts it to analog composite (CVBS) and simultaneously S-video signals. NTSC-M and Pal B/G standards plus other sub standards are supported in both interlaced and non-interlaced modes. Three separate analog RGB outputs are available.

The encoder incorporates a proprietary flicker free filter with a 3-line buffer. The flicker filter can be selectively turned off if the video source is interlaced insuring that the display will maintain the highest quality.

The encoder generates the subcarrier, modulates the color and inserts the synchronization signals. Included in the process the luminance and chrominance signals are filtered in accordance with normal standards.

DuoVision™Dual Display Support

The DuoVision feature allows video coming from the video port or through the Flexibus interface to be displayed directly on the TV while the monitor is being used to display normal graphics. In a PC application for example, this feature enables a user to work on an application while watching a full screen movie from the hard disk or CDROM without having to play it in a window on the PC monitor.

The CyberPro2010 provides high quality video capture and playback output on TV, by using its multi-tap filters, interpolation techniques and multiple hardware windows capability.

Flexibus Interface

The Flexibus feature incorporates the CPU bridge functions for most of the embedded CPU's which are designed into NC's, SetTops and Internet appliances. The CyberPro2010 has a glueless CPU bus interface to all PCI, VL bus and RISC CPU's, such as PowerPC, NEC V83X, and Hitachi SHX.

The CyberPro2010 decodes entire 32-bit address and executes 32-bit I/O and memory accesses at speeds up to 33 MHz. The CyberPro2010 also supports memory burst cycles and can also support an additional peripheral device through the I2C Bus.

The CyberPro2010 has a multi-level 32-bit CPU write buffer that increases GUI acceleration and enhances CPU performance. The CPU write buffer contains a queue of CPU write accesses to display memory or the BitBLT engine.

CPU Interfaces

PCI	VL	IBM	MOTOROLA	HITACHI	NEC
Sparc, MIPS, Pentium	**AMD Elan4XX StrongARM 110**	**PowerPC 4XX**	**PowerPC 8XX**	**SuperH SHX**	**V 8XX**
	ADR[31:2]	A[10:29]	ADDR[0:31]	ADDR[25:2]	ADDR[23:2]
		CSX#			
AD[31:0]	DAT[31:0]	D[0:31]	DATA[0:31]	DATA[31:0]	DATA[31:0]
BE[3:0]#	BE[3:0]#	WBE[0:3]	TSIZE[0:1]	WE[3:0]	WE[3:0]#
FRAME#	ADS#		TS#	BS#	BCYST#
DEVSEL#	LDEV#				
CLK	LCLK	SYSCLK	CLKOUT	CKIO	BCLK
IDSEL	W/R#		RD/WR#	RD/WR#	
IRDY#	RDYTRN#				
PAR	MIO#	OE#		RD#	MRD#
TRDY#	LRDY#	READY	TA#	WAIT#	READY#
IRQ#	INTR		IRQ#	IRL	INTP#
RST#	RESET#	RESET#	HRESET#	RESET#	RESET#

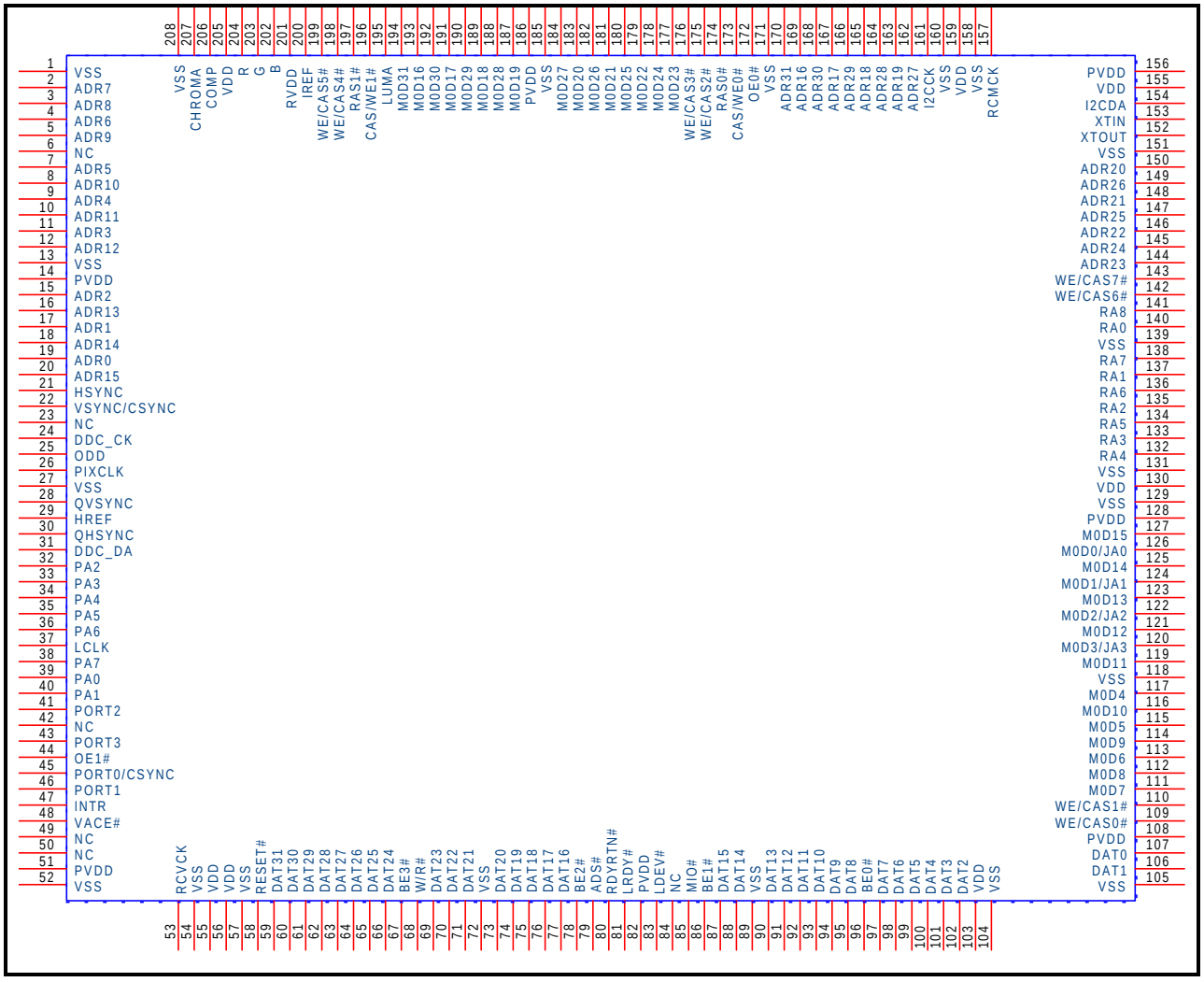
Power-up Bus Type Configuration

All memory addresses from RA8 to RA0 have an internal power-down.

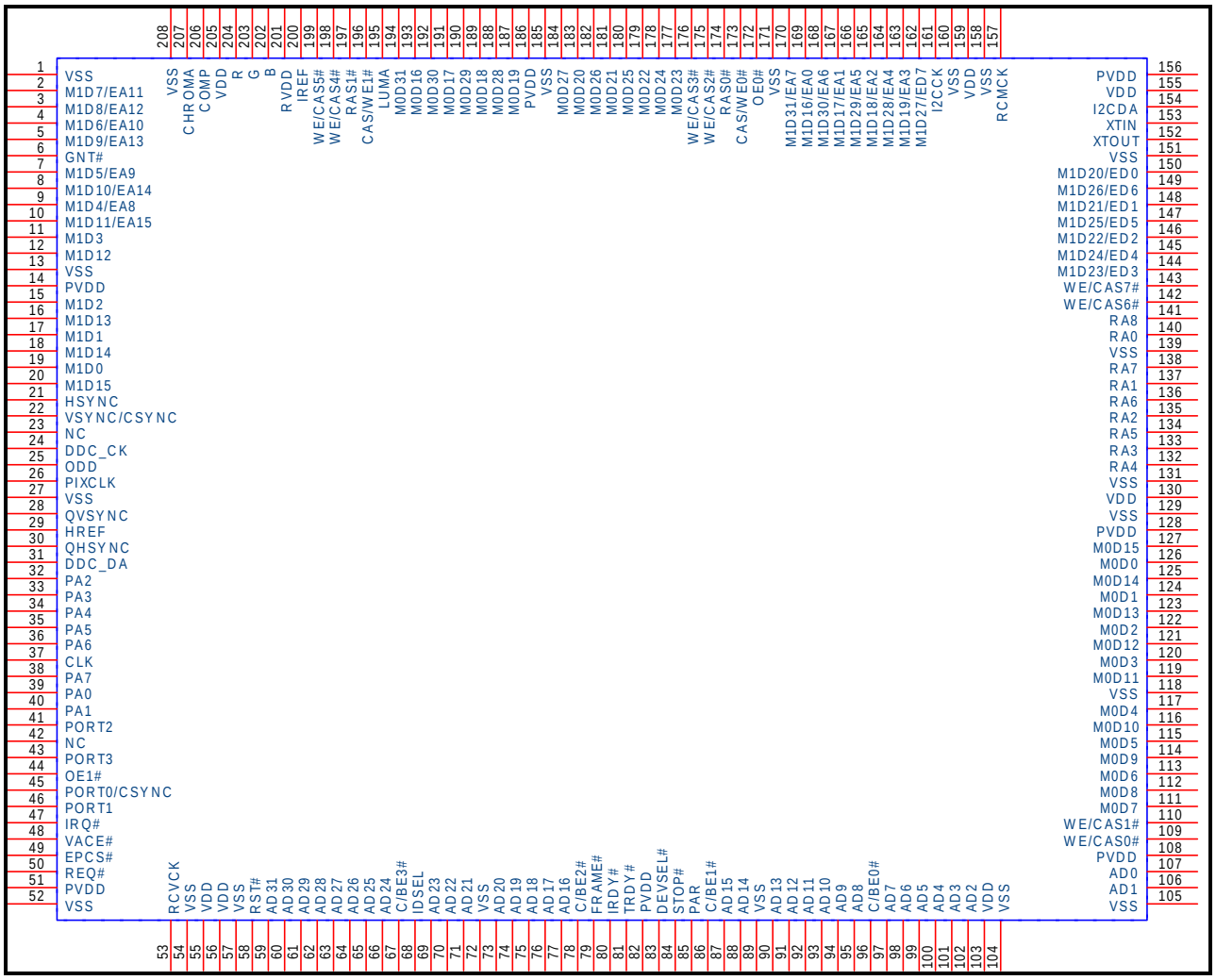
RA2	RA1	RA0	Bus Type
0	0	0	PCI (Default) for no pull-up resistors.
0	0	1	NEC 831
0	1	0	Hitachi (SHX)
0	1	1	Motorola
1	0	0	VL Standard
1	0	1	VL Linear Address
1	1	0	IBM

Flexibus Interfaces

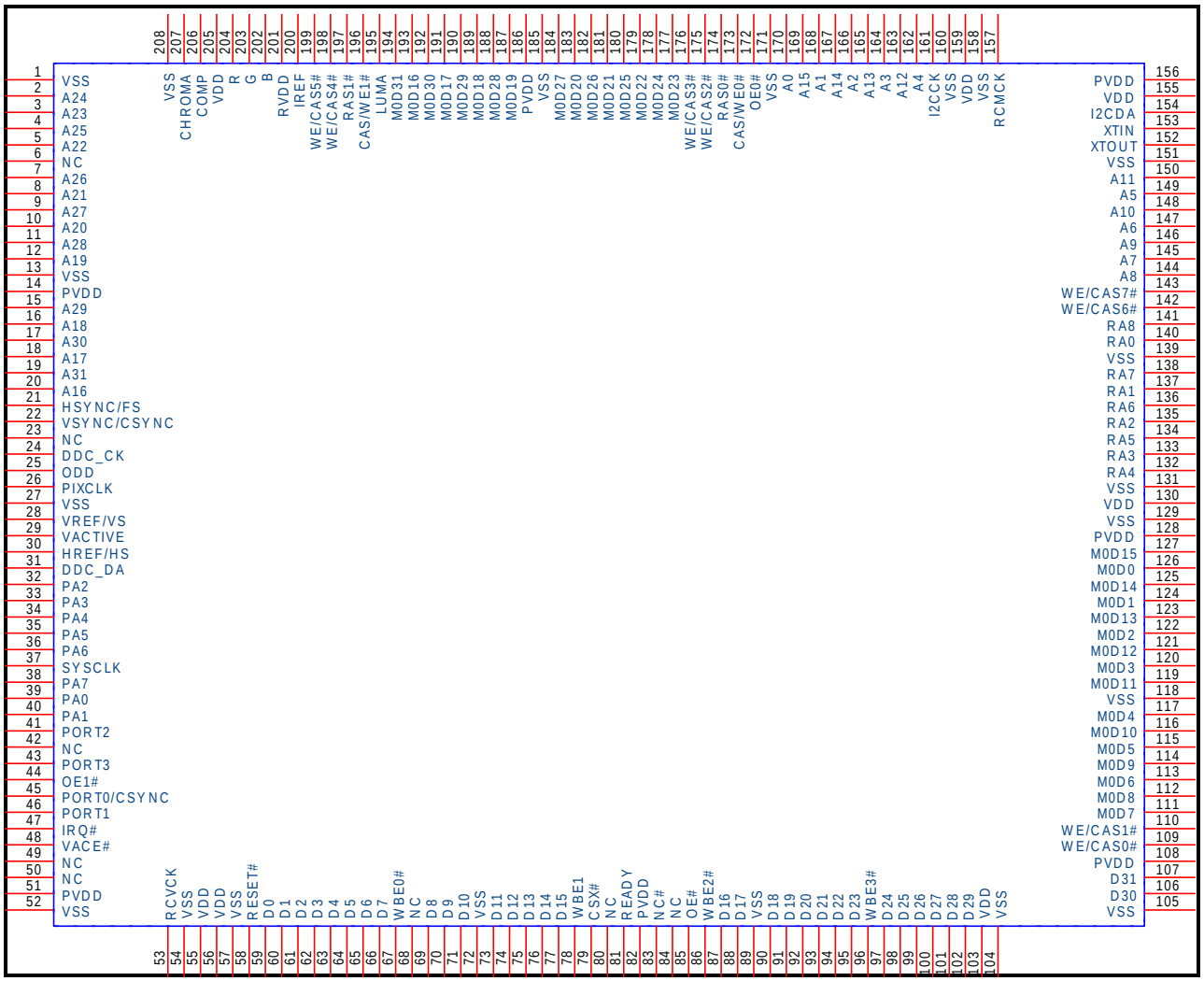
VL Bus Pin Diagram



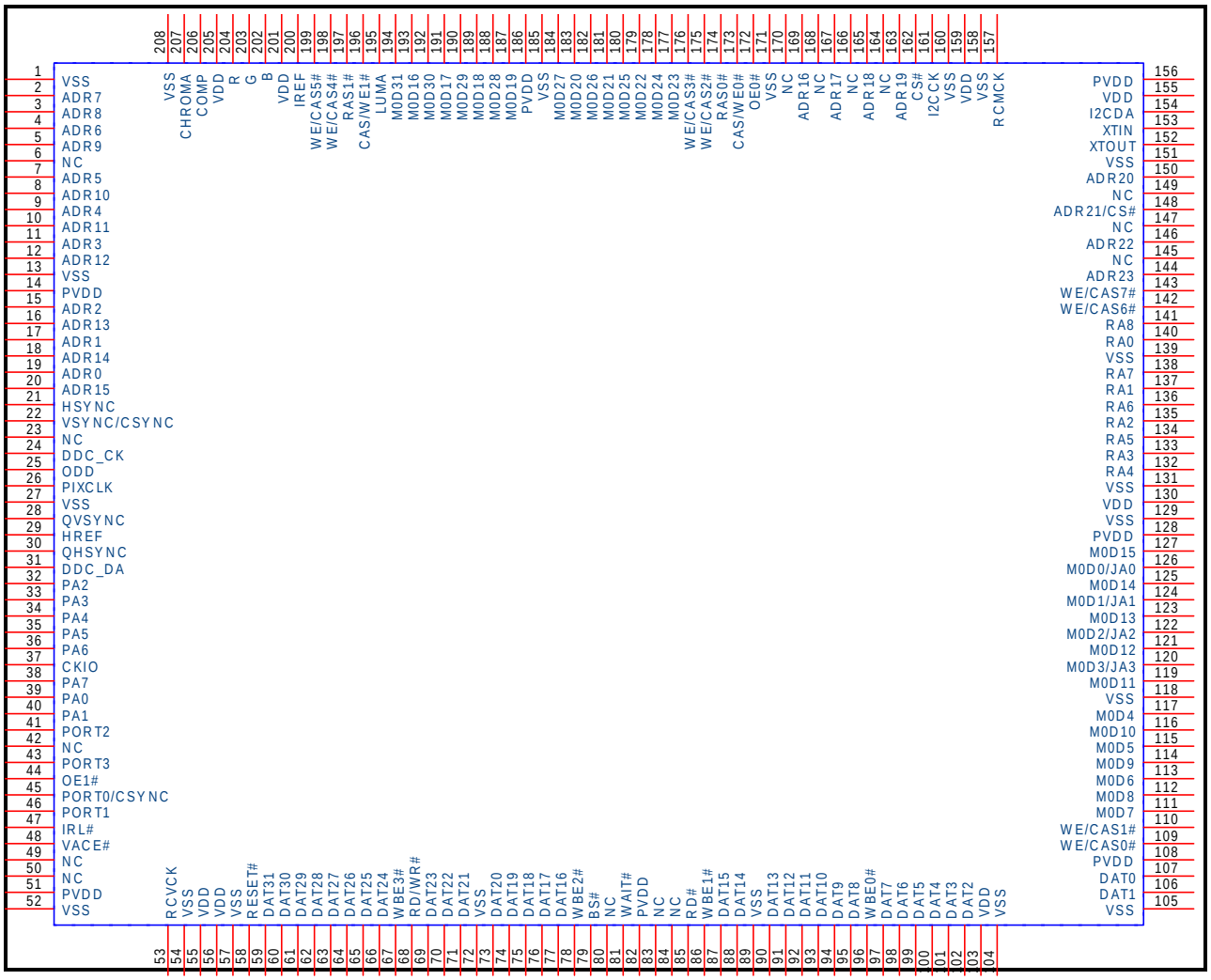
PCI Bus Pin Diagram



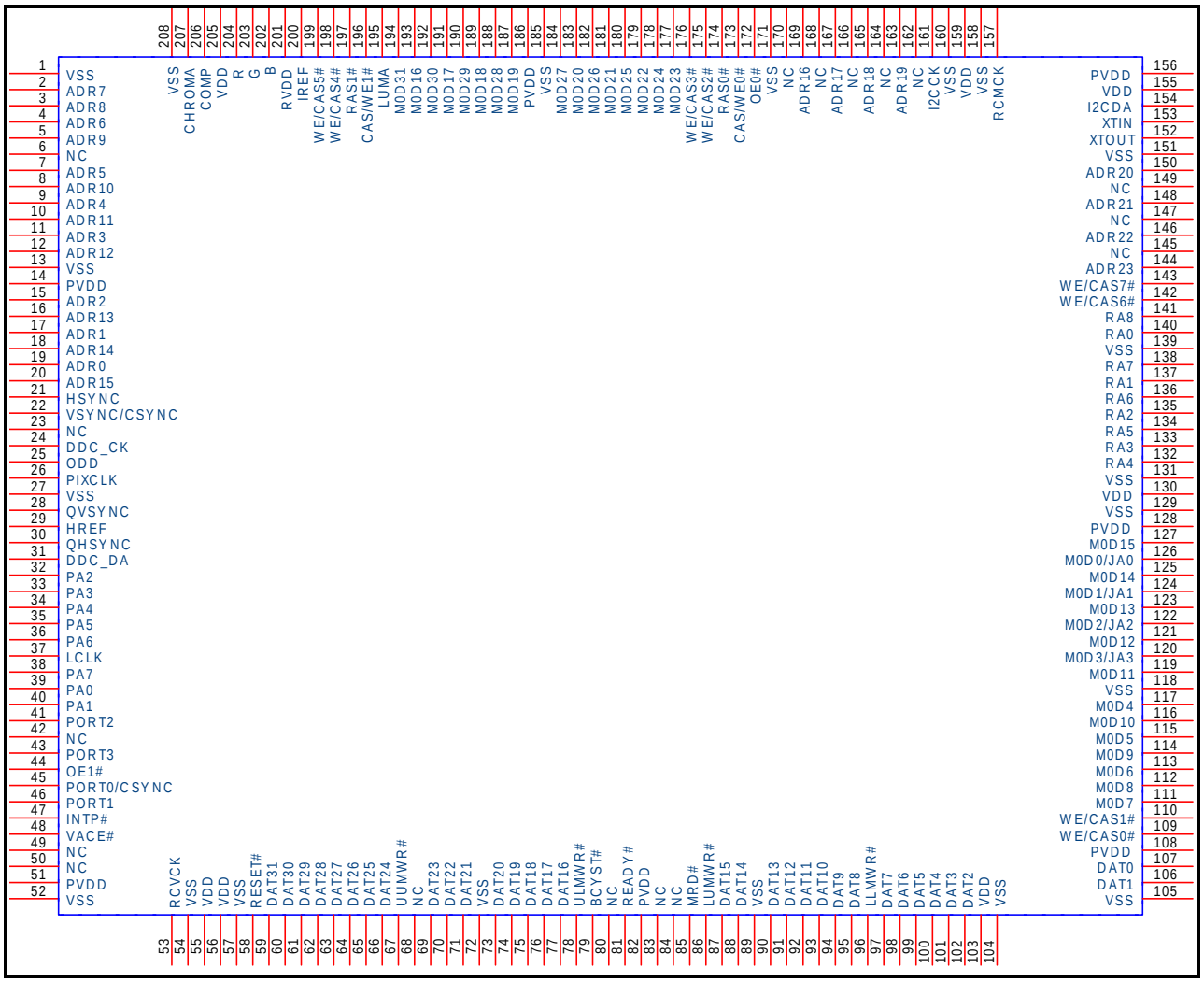
IBM40X Bus Pin Diagram



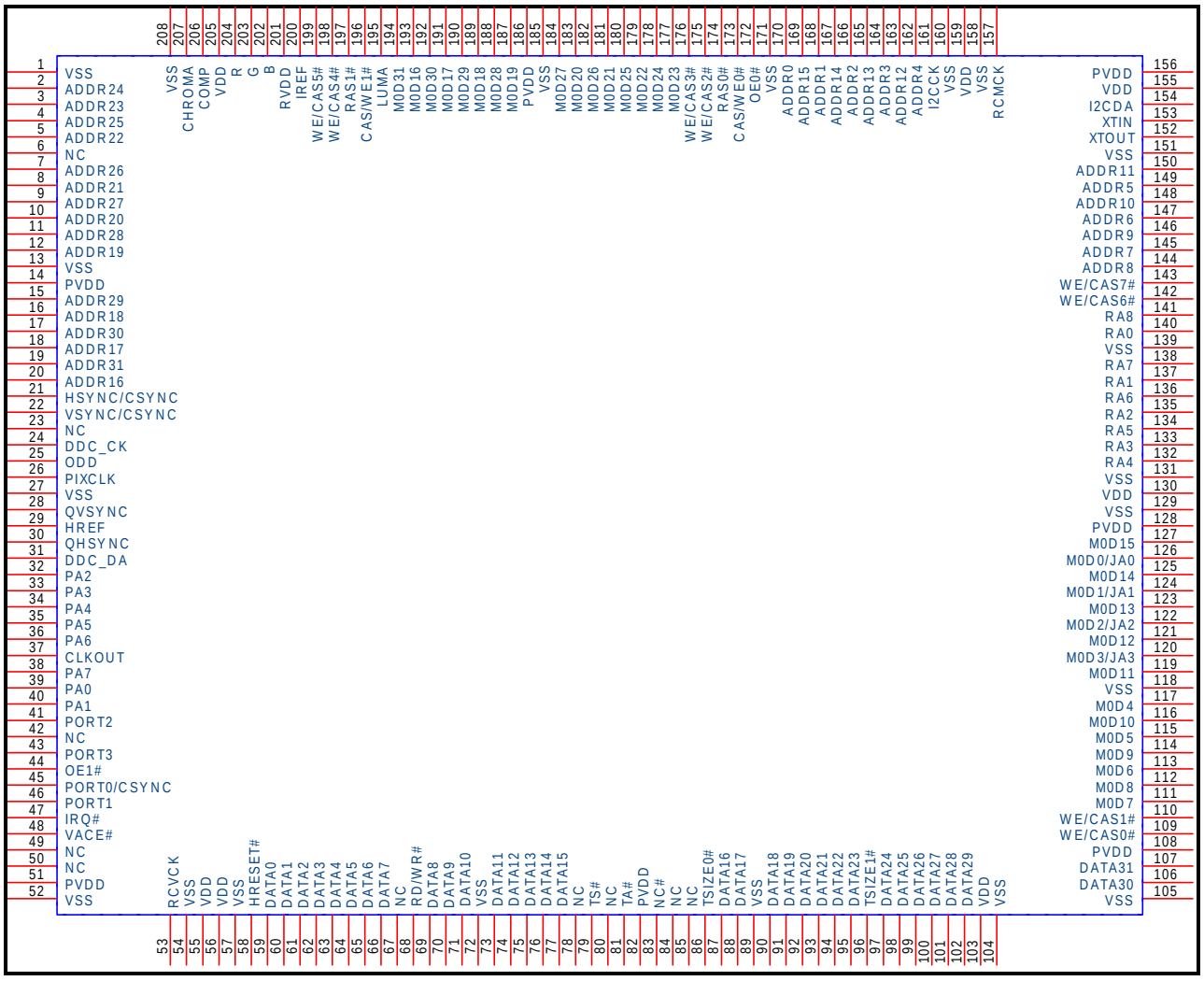
SHx Bus Pin Description



NEC V831 Bus Pin Diagram



MPC8XXPin Diagram



Host Interfaces

Host Interface (IBM40X)

Name	Type	Pin No.	Description
A[29:8]	I/O	15,11,9,7,4,2,3,5,8, 10,12,16,18,20,169, 167,165,163,150, 148,146,144, 170,168,166,164, 162,149,147,145	When the IBM40X is bus master, these bits are output addresses. When the IBM40X is not bus master, these bits are input addresses from the external bus master to determine bank register usage.
SYSCLK	I	37	Processor system clock input.
RESET#	I/O	58	System reset. A logic 0 input placed on this pin for SYSCLK cycle causes a system reset to begin. When a system reset in invoked, this pin becomes a logic 0 output for SYSCLK cycles.
D[0:31]	I/O	59,60,61,62,63, 64,65,66,69,70, 71,73,74,75,76, 77,87,88,90,91, 92,93,94,95,97, 98,99,100,101, 102,106,107	Data bus bits. This is a bi-directional data path between IMB40X bus devices and the CPU.
WBE[3:0]#	I/O	96,86,78,67	Byte enable. The byte enables indicate which byte lanes of the 32-bit data bus are involved with the current IMB40X bus transfer.
GND	—	79	Ground. Connect to VSS.
READY	I	81	Ready is used to insert externally generated (device paced) wait states into bus transactions.
OE#	I/O	85	Output Enable. When the IBM40X is bus master, this bit enables the SRAM's to drive the data bus.

Host Interface (MPC8XX)

Name	Type	Pin No.	Description
ADDR[0..31]	I	170,168,166,164, 162,149,147,145, 144,146,148,150, 163,165,167,169, 20,18,16,12, 10,8,5,3 2,4,7,9, 11,15,17,19	Address bus
DATA[0:31]	I/O	59,60,61,62, 63,64,65,66, 69,70,71,73, 74,75,76,77, 87,88,90,91, 92,93,94,95, 97,98,99,100, 101,102,106,107	Data bus.
CLKOUT	I	37	Processor system clock input.
IRQ#	O	47	Interrupt request to the CPU
HRESET#	I	58	System Reset.
TSIZE[0.1]	I/O	86,96	Transfer Size. Used to signal the number of bytes to be transferred
TS#	I	79	Transfer Start. Indicates the start of a bus cycle.
TA#	O	81	Transfer Acknowledge. Used to indicate the Cyberpro2010 has accepted the data.
RD/WR#	I	68	Used to indicate a read from or write to the CyberPro2010.

Host Interface (NEC V831)

Name	Type	Pin No.	Description
A[31:2]	I/O	170,168,166,164, 162,149,147,145, 144,146,148,150, 163,165,167,169, 20,18,16,12,10,8, 5,3,2,4,7,9,11,15	The address bus furnishes the physical memory or I/O port addresses to the VL bus target.
BCLK	I	37	The system input clock signal.
INTP#	O	47	Used to request an interrupt to the system.
RESET#	I	58	System reset. During power-up or a hardware reset, this signal must be at a logic low for at least 1ms. When this signal is low, the CyberPro2010 is in a reset state, all the pins are inactive, and the memory data bus is tri-state.
D[31:0]	I/O	59,60,61,62,63, 64,65,66,69,70, 71,73,74,75,76, 77,87,88,90,91, 92,93,94,95,97, 98,99,100,101, 102,106,107	Data bus. This is a bi-directional data path between VL bus devices and the CPU.
WE[3:0]#	I/O	67,78,86,96	Byte enable. The byte enables indicate which byte lanes of the 32-bit data bus are involved with the current VL bus transfer.

Host Interface (NEC V831 continued)

BCYST#	I/O	79	Address data strobe. ADS# indicates the start of the VL bus cycle.
READY#	I/O	81	Local ready. LRDY# begins the handshake that terminates the current active bus cycle when the target is not bursting.
MRD#	I/O	85	Memory or I/O status. This CPU output indicates the type of access currently executing on the VL bus.
RAS[1:0]#	O	197,174	ROW ADDRESS STROBE[1:0]# is used to control the DRAM RAS# signal.

Host Interface (PCI)

Name	Type	Pin No.	Description
GNT#	O	6	GRANT indicates to the agent that access to the bus has been granted.
SCLK	I	37	The system input clock signal.
IRQ	O	47	Used to request an interrupt to the system.
REQ#	O	50	Bus master request.
RST#	I	58	System reset. During power-up or a hardware reset, this signal must be at a logic low for at least 1ms. When this signal is low, the CyberPro2010 is in a reset state, all the pins are inactive, and the memory data bus is tri-state.
AD[31:0]	I/O	59,60,61,62,63, 64,65,66,69,70, 71,73,74,75,76, 77,87,88,90,91, 92,93,94,95,97, 98,99,100,101, 102,106,107	Data bus. This is a bi-directional data path between PCI bus devices and the CPU.
C/BE[3:0]#	I/O	67,78,86,96	Byte enable. The byte enables indicate which byte lanes of the 32-bit data bus are involved with the current PCI bus transfer.
IDSEL	I/O	68	DEVICE SELECT# is an active low output signal that responds to the current access, which means it is a valid cycle for the CyberPro2010.
FRAME#	I/O	79	Used to indicate the beginning of any cycle. At the rising edge of system clock when this signal is active low, all address and command codes are latched internally.
IRDY#	I/O	80	INITIATOR READY# is an active low input, used to indicate a handshake between the PCI and target. When this signal is low, the PCI data is ready and will wait for TRDY# to complete the current cycle.
TRDY#	I/O	81	TARGET READY# is an active low output signal, used to terminate a current bus cycle.
DEVSEL#	I/O	83	DEVICE SELECT# is an active low output signal that responds to the current access, which means it is a valid cycle for the CyberPro2010.
STOP#	I	84	STOP# is an active low output signal, used to indicate a bus master has stopped the current transaction.
PAR	I/O	85	PARITY - an I/O signal, used to generate even parity between AD[31:0] and C/BE[3:0]#. During a system read cycle, an even parity will be generated from the CyberPro2010. During system write operation, parity is read from this signal.

Host Interface (VL)

Name	Type	Pin No.	Description
ADR[31:2]	I/O	170,168,166,164, 162,149,147,145, 144,146,148,150, 163,165,167,169, 20,18,16,12,10,8, 5,3,2,4,7,9,11,15	Address bus.
LCLK	I	37	The system input clock signal.
INTR	O	47	Used to request an interrupt to the system.
RESET#	I	58	System reset. During power-up or hardware reset, this signal must be at a logic low for at least 1ms. When this signal is low, the CyberPro2010 is in a reset state, all the pins are inactive, and the memory data bus is tri-state.
DAT[31:0]	I/O	59,60,61,62,63, 64,65,66,69,70, 71,73,74,75,76, 77,87,88,90,91, 92,93,94,95,97, 98,99,100,101, 102,106,107	Data bus. This is a bi-directional data path between VL bus devices and the CPU.
BE[3:0]#	I/O	67,78,86,96	Byte enable. The byte enables indicate which byte lanes of the 32-bit data bus are involved with the current VL bus transfer.
W/R#	I/O	68	Writer or read status. This CPU output indicates the type of access currently executing on the VL bus.
ADS#	I/O	79	Address data strobe. ADS# indicates the start of the VL bus cycle.
RDYRTN#	I/O	80	Ready return. RDYRTN# establishes a handshake so the VL bus target knows when the cycle has ended.
LRDY#	I/O	81	Local ready. LRDY# begins the handshake that terminates the current active bus cycle when the target is not bursting.
LDEV#	I/O	83	Device select. LDEV# is an active low output signal that responds to the current access, which means it is a valid cycle for the CyberPro2010.
MIO#	I/O	85	Memory or I/O status. This CPU output indicates the type of access currently executing on the VL bus.

Host Interface (SHX)

Name	Type	Pin No.	Description
ADR[0=23]	I	19,17,15,11,9,7,4 2,3,5,8,10,12,16, 18,20,169,167,165, 163,150,148,146, 144	Address bus format for SHX.
WBE[0:3]	I/O	96,86,78,67,	32 byte enable.
CKIO	I	37	Processor system clock input.
RESET#	I	58	System reset. during power up or hardware reset. This signal must be at a logic low for at least 1ms.
DAT[0=31]	I/O	107,106,102,101, 100,99,98,97,95,94, 93,92,91,90,88,87, 77,76,75,74,73,71, 70.69.66.65.64.63, 62,61,60,59	Data bus format for SH2.
BS#	I	79	Bus cycle start.
IRL#	O	47	Used to request an interrupt to the system.
R/W#	I	68	Bus Read/Write status.
WAIT#	O	81	Wait# begins the handshake that terminates the current bus cycle when the target is not bursting.
RD#	I	85	The read pulse signal.
CS#	I	164	Chip select

Memory Interfaces

Memory Interface (IBM40X)

Name	Type	Pin No.	Description
OE1#	O	44	Output enable. Output address pins to DRAM.
WE/CAS[7:0]	O	143,142,199,198, 176,175,110,109	Used to control different banks of memory.
M0D[31:0]	I/O	194,192,190,188, 184,182,180,178, 177,179,181,183, 187,189,191,193, 127,125,123,121, 119,116,114,112, 111,113,115,117, 120,122,124,126	Used to transfer data between DRAM and the CyberPro2010.
RA[8:0]	O	141,138,136, 134,132,133, 135,137,140,	Output address pins to DRAM.
OE0#	O	172	Output enable. Used to control output enable to the DRAM.
CAS/WE[1:0]#	O	196,173	Each of these signals is used to control one bank of DRAM.
RAS[1:0]#	O	197,174	ROW ADDRESS STROBE[1:0]# is used to control the DRAM RAS# signal.

Memory Interface (MPC8XX)

Name	Type	Pin No.	Description
OE1#	O	44	Output enable. Output address pins to DRAM.
WE/CAS[7:0]	O	143,142,199,198, 176,175,110,109	Used to control different banks of memory.
M0D[31:0]	I/O	194,192,190,188, 184,182,180,178, 177,179,181,183, 187,189,191,193, 127,125,123,121, 119,116,114,112, 111,113,115,117, 120,122,124,126	Used to transfer data between DRAM and the CyberPro2010.
RA[8:0]	O	141,138,136, 134,132,133, 135,137,140,	Output address pins to DRAM.
OE0#	O	172	Output enable. Used to control output enable to the DRAM.
CAS/WE[1:0]#	O	196,173	Each of these signals is used to control one bank of DRAM.
RAS[1:0]#	O	197,174	ROW ADDRESS STROBE[1:0]# is used to control the DRAM RAS# signal.

Memory Interface (NEC V831)

Name	Type	Pin No.	Description
OE1#	O	44	Output enable. Output address pins to DRAM.
WE/CAS[7:0]#	O	143,142,199,198, 176,175,110,109	Used to control different banks of memory.
M0D[31:0]	I/O	194,192,190,188, 184,182,180,178, 177,179,181,183, 187,189,191,193, 127,125,123,121, 119,116,114,112, 111,113,115,117, 120,122,124,126	Used to transfer data between DRAM and the CyberPro2010.
RA[8:0]	O	141,138,136, 134,132,133, 135,137,140,	Output address pins to DRAM.
OE0#	O	172	Output enable. Used to control output enable to the DRAM.
CAS/WE[1:0]#	O	196,173	Each of these signals is used to control one bank of DRAM.

Memory Interface (PCI)

Name	Type	Pin No.	Description
OE1#	O	44	Output enable. Output address pins to DRAM.
WE/CAS[7:0]	O	143,142,199,198, 176,175,110,109	Used to control different banks of memory.
M0D[31:0]	I/O	194,192,190,188, 184,182,180,178, 177,179,181,183, 187,189,191,193, 127,125,123,121, 119,116,114,112, 111,113,115,117, 120,122,124,126	Used to transfer data between DRAM and the CyberPro2010.
M1D[31:0]	I/O	170,168,166,164, 162,149,147,145, 144,146,148,150, 163,165,167,169, 20,18,16,12,10,8,5, 3,2,4,7,9,11,15,17, 19	The address bus furnishes the physical memory or I/O port addresses to the PCI bus target.
RA[8:0]	O	141,138,136, 134,132,133, 135,137,140,	Output address pins to DRAM.
OE0#	O	172	Output enable. Used to control output enable to the DRAM.
CAS/WE[1:0]#	O	196,173	Each of these signals is used to control one bank of DRAM.
RAS[1:0]#	O	197,174	ROW ADDRESS STROBE[1:0]# is used to control the DRAM RAS# signal.

Memory Interface (VL)

Name	Type	Pin No.	Description
OE1#	O	44	Output enable. Output address pins to DRAM.
WE/CAS[7:0]#	O	143,142,199,198, 176,175,110,109	Used to control different banks of memory.
M0D[31:0]	I/O	194,192,190,188, 184,182,180,178, 177,179,181,183, 187,189,191,193, 127,125,123,121, 119,116,114,112, 111,113,115,117, 120,122,124,126	Used to transfer data between DRAM and the CyberPro2010.
RA[8:0]	O	141,138,136, 134,132,133, 135,137,140,	Output address pins to DRAM.
OE0#	O	172	Output enable. Used to control output enable to the DRAM.
CAS/WE[1:0]#	O	196,173	Each of these signals is used to control one bank of DRAM.
RAS[1:0]#	O	197,174	ROW ADDRESS STROBE[1:0]# is used to control the DRAM RAS# signal.

Memory Interface (SHX)

Name	Type	Pin No.	Description
OE1#	O	44	Output enable. Output address pins to DRAM.
WE/CAS[7:0]	O	143,142,199,198, 176,175,110,109	Used to control different banks of memory.
M0D[31:0]	I/O	194,192,190,188, 184,182,180,178, 177,179,181,183, 187,189,191,193, 127,125,123,121, 119,116,114,112, 111,113,115,117, 120,122,124,126	Used to transfer data between DRAM and the CyberPro2010.
RA[8:0]	O	141,138,136, 134,132,133, 135,137,140,	Output address pins to DRAM.
OE0#	O	172	Output enable. Used to control output enable to the DRAM.
CAS/WE[1:0]#	O	196,173	Each of these signals is used to control one bank of DRAM.
RAS[1:0]#	O	197,174	ROW ADDRESS STROBE[1:0]# is used to control the DRAM RAS# signal.

Common Interfaces

BIOS EPROM Interface

Name	Type	Pin No.	Description
EA[15:0]	I/O	10,8,5,3,2,4,7,9, 170,168,166,164, 163,165,167,169	The address bus furnishes the physical memory or I/O port addresses to the PCI bus target.
ED[7:0]	I/O	162,149,147,145, 144,146,148,150	The address bus furnishes the physical memory or I/O port addresses to the PCI bus target.
EPCS#	O	49	EPROM CHIP SELECT# is used to enable an external ROM.

CRT & TV Interface

Name	Type	Pin No.	Description
HSYNC/FS	O	21	HSYNC to CRT/fast switch (SCART).
VSYNC/ CSYNC	O	22	VSYNC to CRT; composite sync to TV.
DDC_CK	I/O	24	DDC2B clock.
DDC_DA	I/O	31	DDC2B data.
LUMA	O	195	Luminance output/TV blue.
B	O	202	Blue analog output connected to the monitor/TV blue.
G	O	203	Green analog output connected to the monitor/TV green.
R	O	204	Red analog output connected to the monitor/TV red.
COMP	O	206	Composite video output/TV red.
CHROMA	O	207	Chrominance output/TV green.

Miscellaneous

Name	Type	Pin No.	Description
NC	—	23,42	No connection.
PORT2	I/O	41	Port I/O programmable pin.
PORT3	I/O	43	Port I/O programmable pin.
PORT0/ CSYNC	I/O	45	Port I/O programmable pin/composite sync for TV.
PORT1	I/O	46	Port I/O programmable pin.
RCVCK	I	53	RC filter for internal DOT clock.
XTOUT	O	152	An output loop back pin for a crystal.
XTIN	I	153	An input pin for a crystal.
I2CDA	I/O	154	I^2C bus serial data input/output.
RCMCK	I	157	RC memory clock. Input from the memory clock RC network controls memory frequency.
I2CCK	I/O	161	I^2C bus serial clock input/output.
IREF	O	200	DAC reference current.

Power

Name	Type	Pin No.	Description
VSS	I	1,13,27,52,54,57,72, 89,104,105,118, 129,131,139,151, 158,160,171,185, 208,	0.0V
PVDD	I	14,51,82,108,128, 156,186	I/O pad power, 3.3/5.0V.
VDD	I	55,56,103,130,155, 159,201,205	+5.0V.

Video Port Interface

Name	Type	Pin No.	Description
ODD	I/O	25	Odd/even field ID.
PIXCLK	I/O	26	Video port clock.
QVSYNC	I/O	28	Vertical sync for video port.
QHSYNC	I/O	30	Video port horizontal reference or sync.
HREF	I/O	29	Horizontal Reference.
PA[7:0]	I/O	38,36-32,40,39	Video port data.
VACE#	O	48	Video port enable.

Addressing Modes

Linear Address Decodes for MPC8XX Bus

ADDR[8:31]	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
1st 1MB Memory	0	0	0	0	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	x	x
2nd 1MB Memory	0	0	0	1	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Write	1	0	0	0	0	0	0	0	#	#	x	x	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Read BE0	1	0	0	0	0	0	0	0	#	#	0	0	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Read BE1	1	0	0	0	0	0	0	0	#	#	0	1	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Read BE2	1	0	0	0	0	0	0	0	#	#	1	0	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Read BE3	1	0	0	0	0	0	0	0	#	#	1	1	#	#	#	#	#	#	#	#	#	#	x	x
R/W Port [7:0]	1	0	0	0	1	0	1	%	1	1	0	$	$	$	#	#	#	#	#	#	#	#	0	0
R/W TV 2K Byte	1	0	0	0	1	0	1	%	1	1	1	0	x	#	#	#	#	#	#	#	#	#	0	0
COPREG R/W	1	0	0	0	1	0	1	%	1	1	1	1	#	#	#	#	#	#	#	#	#	#	0	0

Example:
At power-up, M0D[3:0] = 0101; then, linear address will be 0001,0100 or 14H.

Motorola Highest 8 Bit Address Map

M0D[3:0] has internal pull-down.

At power-up, decodes the linear address.

MPC8XX Highest 8 Bits [0:7] = ADDR [0:7]

= 00JJJJ00

JJJJ is the jumper setting on Mod[3:0]

Mapped to linear address ADDR [2:5].

Process addresses ADDR [0:1] and ADDR [6:7] are always zero.

Legend for Decode Tables

#	0 or one range
x	Don't Care
C	RISC processor chip select (active low)
$	Binary range ($$$: from 0 to 7)

Linear Address Decodes for VL Bus

ADR[23:0]	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st 1MB Memory	0	0	0	0	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	x	x
2nd 1MB Memory	0	0	0	1	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Write	1	0	0	0	0	0	0	0	#	#	x	x	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Read BE0	1	0	0	0	0	0	0	0	#	#	0	0	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Read BE1	1	0	0	0	0	0	0	0	#	#	0	1	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Read BE2	1	0	0	0	0	0	0	0	#	#	1	0	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Read BE3	1	0	0	0	0	0	0	0	#	#	1	1	#	#	#	#	#	#	#	#	#	#	x	x
R/W Port [7:0]	1	0	0	0	1	0	1	%	1	1	0	$	$	$	#	#	#	#	#	#	#	#	0	0
R/W TV 2K Byte	1	0	0	0	1	0	1	%	1	1	1	0	x	#	#	#	#	#	#	#	#	#	0	0
COPREG R/W	1	0	0	0	1	0	1	%	1	1	1	1	#	#	#	#	#	#	#	#	#	#	0	0

VL Linear Highest 8 Bit Address Map

M0D[3:0] has internal pull-down.

At power-up, M0D[3:0] to decode the linear address.

M0D[3:0] is mapped to linear address A[29:26].

Process addresses A[31:30] and A[25:24] are always zero.

Example:
At power-up, M0D[3:0] = 0101; then, linear address will be 0001,0100 or 14H.

Legend for Decode Tables

#	0 or one range
x	Don't Care
C	RISC processor chip select (active low)
$	Binary range ($$$: from 0 to 7)

Linear Address Decodes for NEC, MPC8X and SHx

ADR[23:0]	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st 1MB Memory	0	0	C	0	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	x	x
2nd 1MB Memory	0	0	C	1	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Write	1	0	C	0	0	0	0	0	#	#	x	x	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Read BE0	1	0	C	0	0	0	0	0	#	#	0	0	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Read BE1	1	0	C	0	0	0	0	0	#	#	0	1	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Read BE2	1	0	C	0	0	0	0	0	#	#	1	0	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Read BE3	1	0	C	0	0	0	0	0	#	#	1	1	#	#	#	#	#	#	#	#	#	#	x	x
R/W Port [7:0]	1	0	C	0	1	0	1	%	1	1	0	$	$	$	#	#	#	#	#	#	#	#	0	0
R/W TV 2K Byte	1	0	C	0	1	0	1	%	1	1	1	0	x	#	#	#	#	#	#	#	#	#	0	0
COPREG R/W	1	0	C	0	1	0	1	%	1	1	1	1	#	#	#	#	#	#	#	#	#	#	0	0

Chip selects:

Connect the CPU CS# signal to Address 21.

The original A21 from the CPU is don't care.

SHx addresses A24 and A25 are don't care.

Legend for Decode Tables

#	0 or one range
x	Don't Care
C	RISC processor chip select (active low)
$	Binary range ($$$: from 0 to 7)

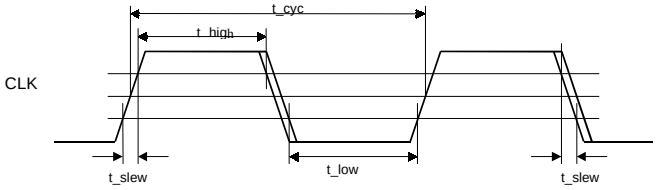
AC Specifications

Symbol	Parameter	MIN	MAX	Units	Note
t_cyc	CLK Cycle Time	30	-	ns	33 MHz max
t_high	CLK High Time	11	-	ns	
t_low	CLK Low Time	11	-	ns	
t_slew	CLK Slew Rate	1	4	v/ns	
t_is	Input Set Time	7	-	ns	
t_ih	Input Hod Time	0	-	ns	
t_od	Output Delay	5	13	ns	
t_ofd	Output Float Delay	8	13	ns	

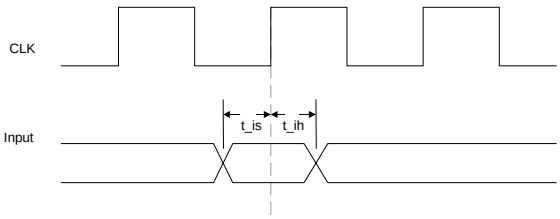
CyberPro2010 AC Timing

Important Note: The CLK, Input and Output AC timing apply to all busses and timing diagrams

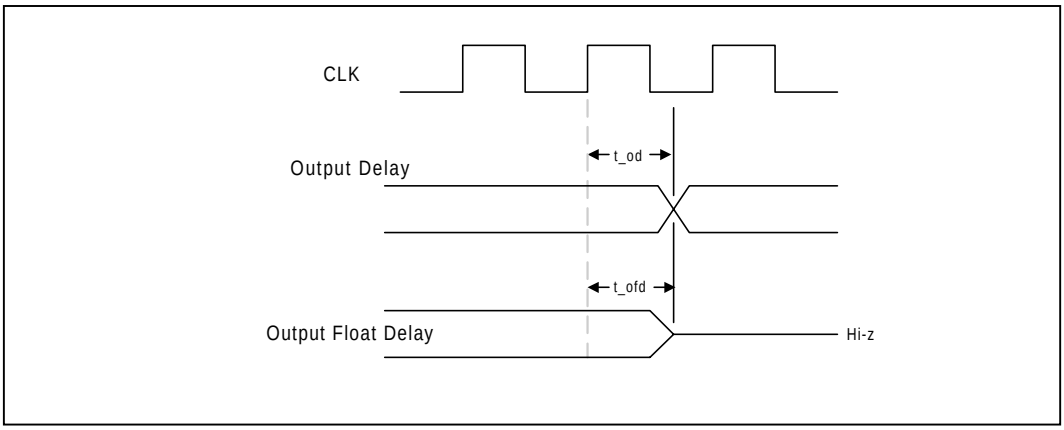
Bus CLK Timing



CyberPro 2010 Input Timing

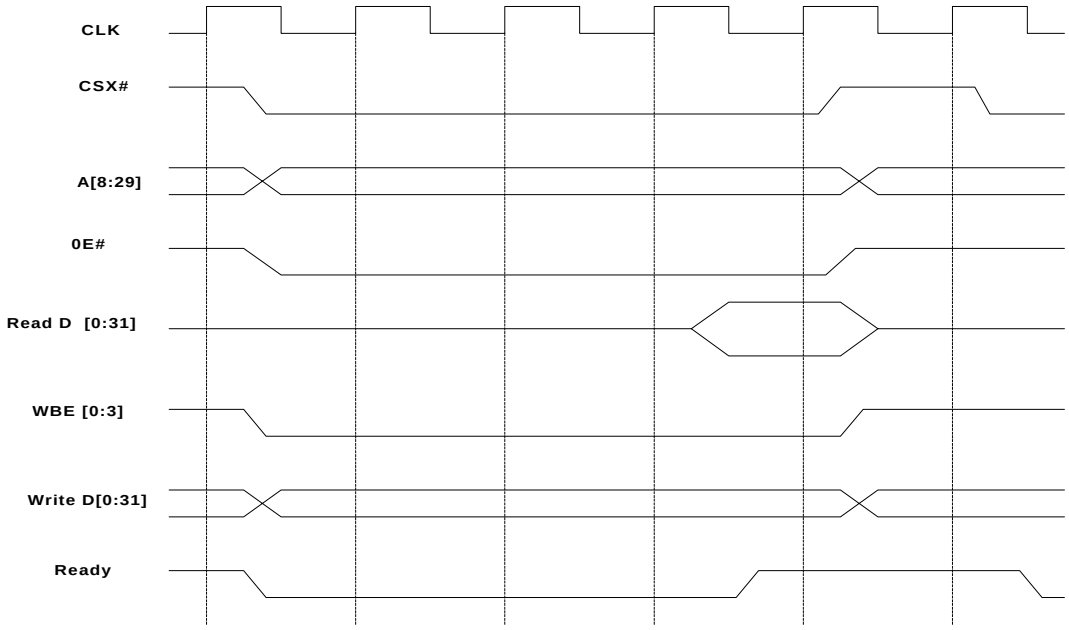


CyberPro 2010 Output Timing



IBM40X Timing Diagrams

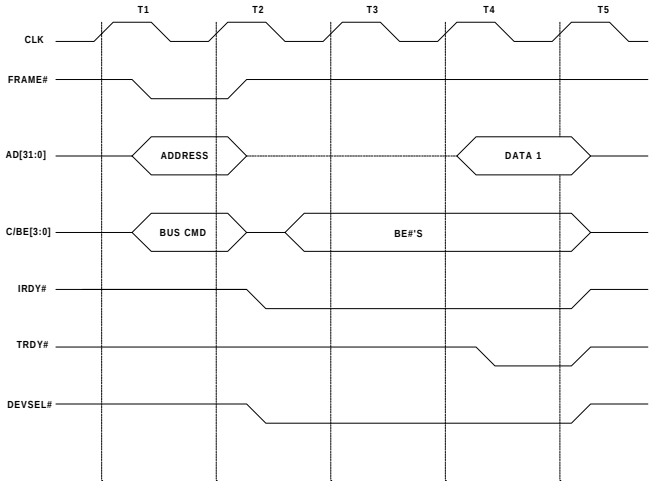
Basic IBM40X Write Cycle



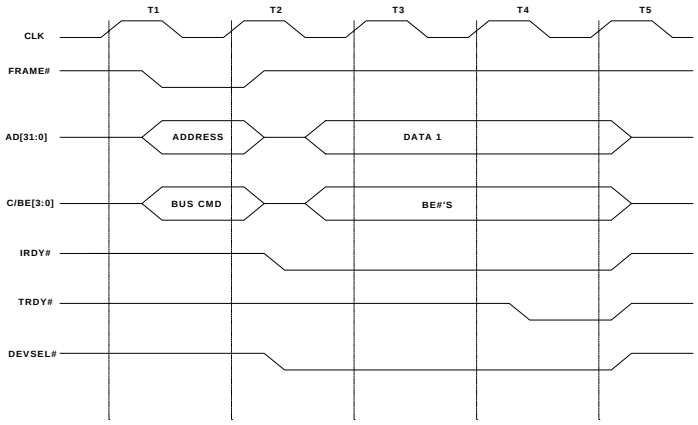
Basic IBM40X Read Cycle

PCI Bus Timing Diagrams

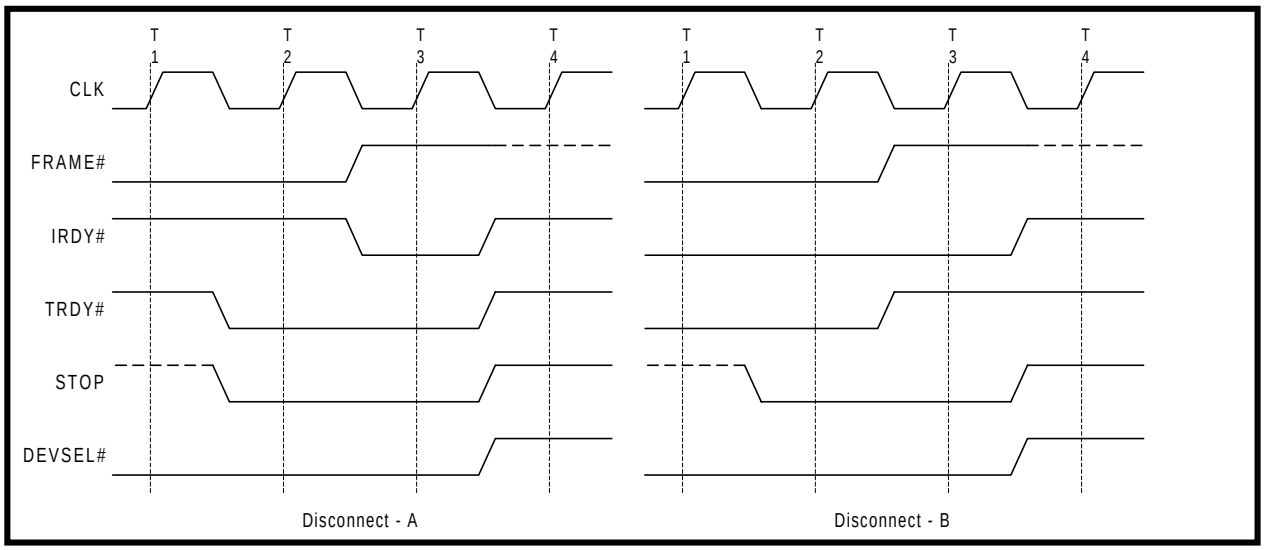
Basic PCI Read Cycle



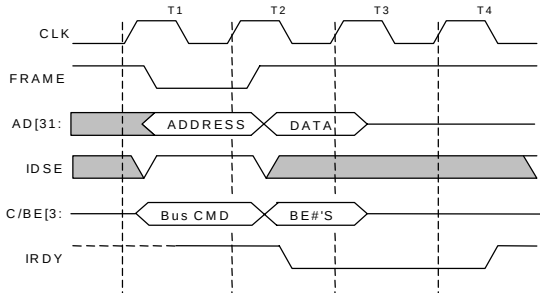
Basic PCI Write Cycle



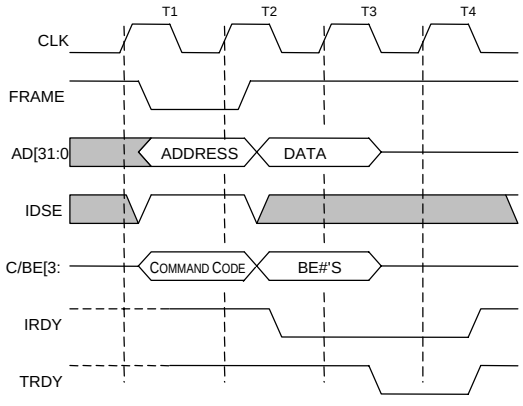
PCI Disconnect Cycle With last transfered Data



PCI Configuration Read Cycle

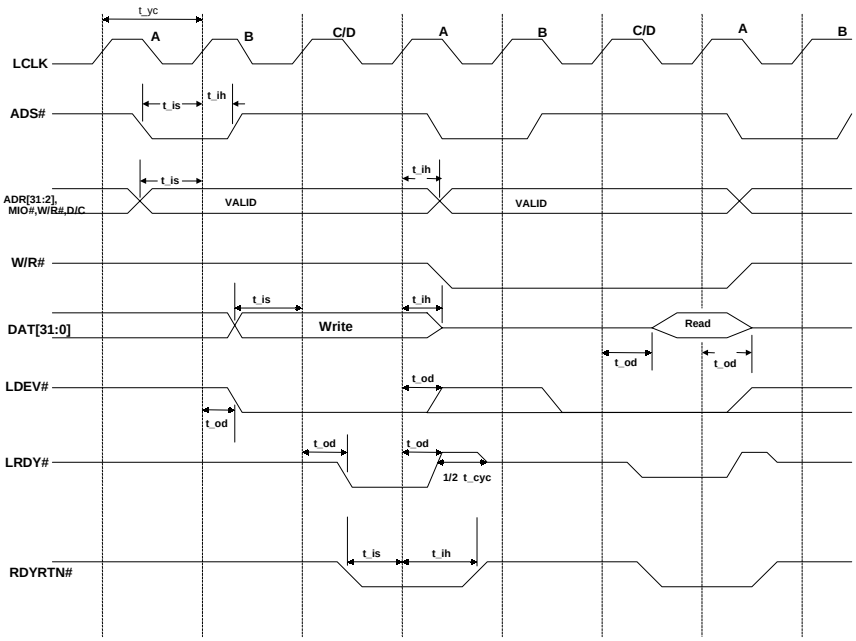


PCI Configuration Write Cycle



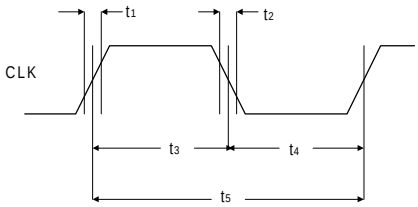
VL Bus Timing Diagram

VL Bus Write and Read Cycle



CLK Timing (PCI Bus)

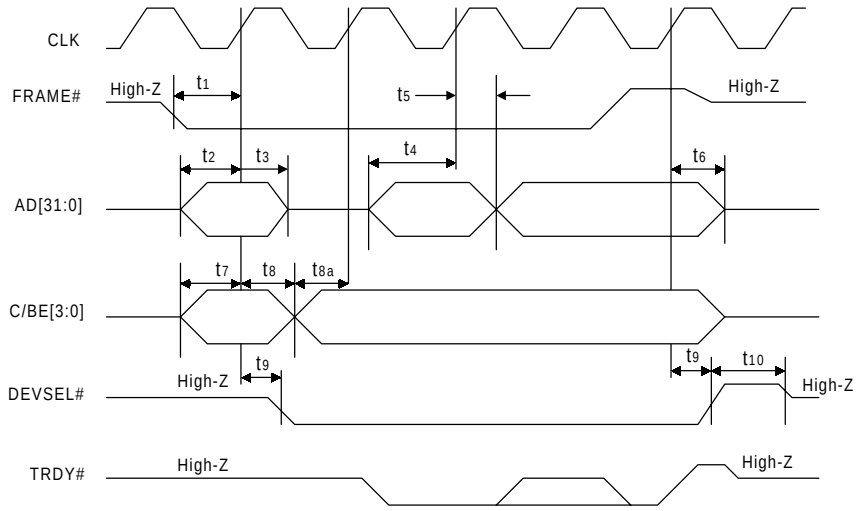
Symbol	Parameter	MIN	MAX	Units
t1	Rise time (CLK) PCI bus	-	4	ns
t2	Fall time (CLK) PCI bus	-	4	ns
t3	High period (CLK) PCI bus	40	60	% t
t4	Low period (CLK) PCI bus	40	60	% t
t5	Period (CLK) PCI bus	30	-	ns



CLK Timing (PCI Bus)

FRAME#, DEVSEL#, AD[31:0], and C/BE[3:0]# (PCI Bus)

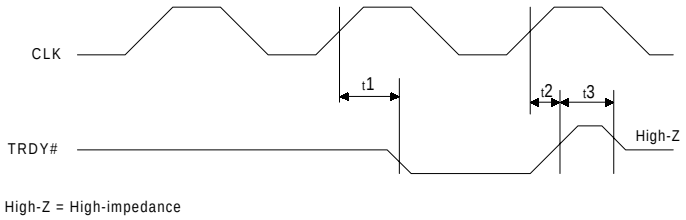
Symbol	Parameter	MIN	MAX	Units
t1	FRAME# setup to CLK	7	-	ns
t2	AD[31:0] (Address) setup to CLK	7	-	ns
t3	AD[31:0] (Address) hold from CLK	0	-	ns
t4	AD[31:0] (Data) setup to CLK	7	-	ns
t5	AD[31:0] (Data) hold from CLK	0	-	ns
t6	AD[31:0], C/BE[3:0]# high-impedance from CLK	0	28	ns
t7	C/BE[3:0]# (bus CMD) setup to CLK	7	-	ns
t8	C/BE[3:0]# (bus CMD) hold from CLK	0	-	ns
t8a	C/BE[3:0]# (byte enable) setup to CLK	7	-	ns
t9	DEVSEL# delay from CLK	2	11	ns
t10	DEVSEL# high before high-impedance	1	-	CLK



FRAME#, DEVSEL#, AD[31:0], and C/BE[3:0]# (PCI Bus)

TRDY# Delay (PCI Bus)

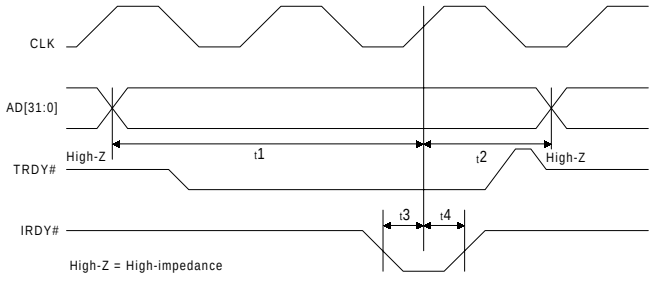
Symbol	Parameter	MIN	MAX	Units
t1	TRDY# active delay from CLK	2	11	ns
t2	TRDY# inactive delay from CLK	2	11	ns
t3	TRDY# high before high-impedance	1	-	CLK



TRDY# Delay (PCI)

Ready Data / TRDY# (PCI Bus)

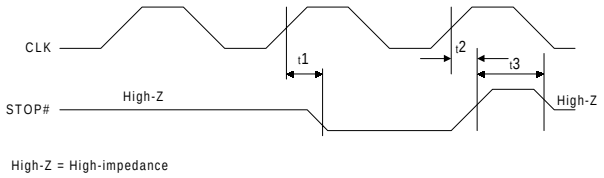
Symbol	Parameter	MIN	MAX	Units
t1	Read data setup to CLK while TRDY# active	7	-	ns
t2	Read data hold from CLK while TRDY# active	0	-	ns
t3	IRDY# setup to CLK	7	-	ns
t4	IRDY# hold from CLK	0	-	ns



Ready Data / TRDY# (PCI Bus)

STOP# Delay (PCI Bus)

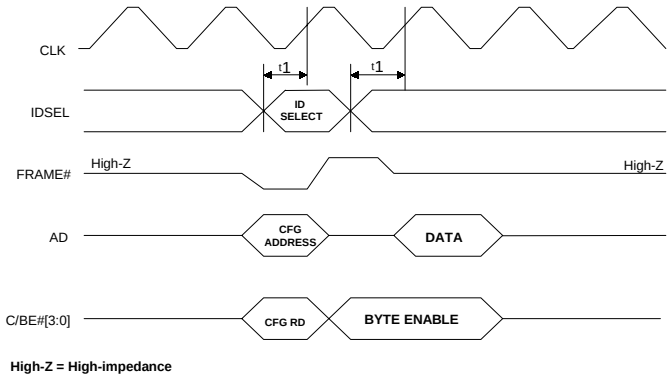
Symbol	Parameter	MIN	MAX	Units
t1	STOP# active delay from CLK	2	11	ns
t2	STOP# inactive delay from CLK	2	11	ns
t3	STOP# high before high-impedance	1	-	CLK



Stop# Delay (PCI Bus)

IDSEL Timing (PCI Bus)

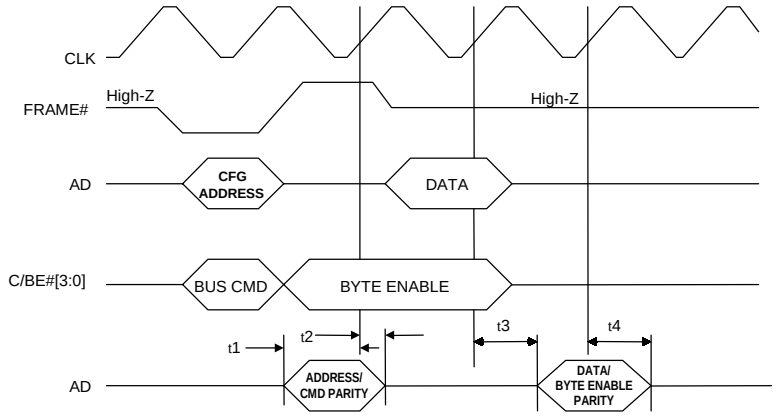
Symbol	Parameter	MIN	MAX	Units
t1	IDSEL setup to CLK	--	15	ns



IDSEL Timing (PCI Bus)

PART Timing (PCI Bus)

Symbol	Parameter	MIN	MAX	Units
t1	PAR setup from CLK (input to CyberPro2010)	7	-	ns
t2	PAR hold from CLK (input to CyberPro2010)	0	-	ns
t3	PAR delay from CLK (output from CyberPro2010) 2	11	-	ns
t4	PAR hold from CLK (output from CyberPro2010)	0	-	ns

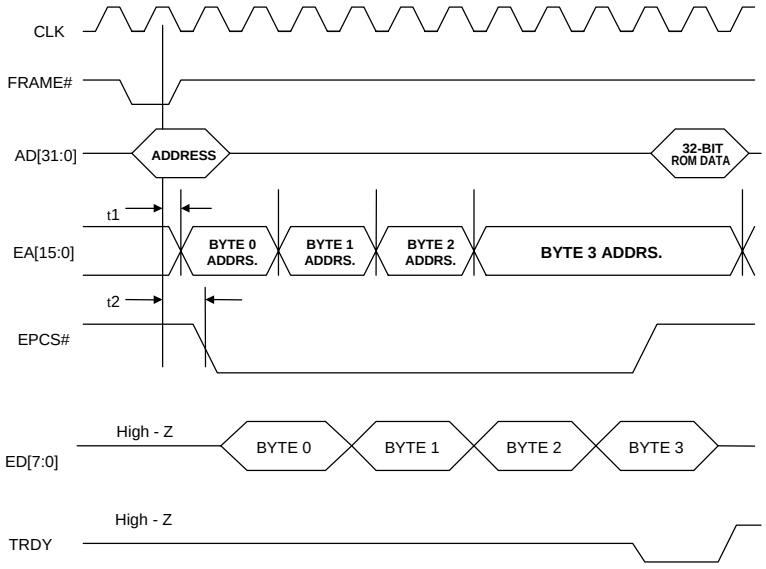


High-Z = High-impedance

PAR Timing (PCI Bus)

EPCS#, EA [15:0] Timing (PCI Bus)

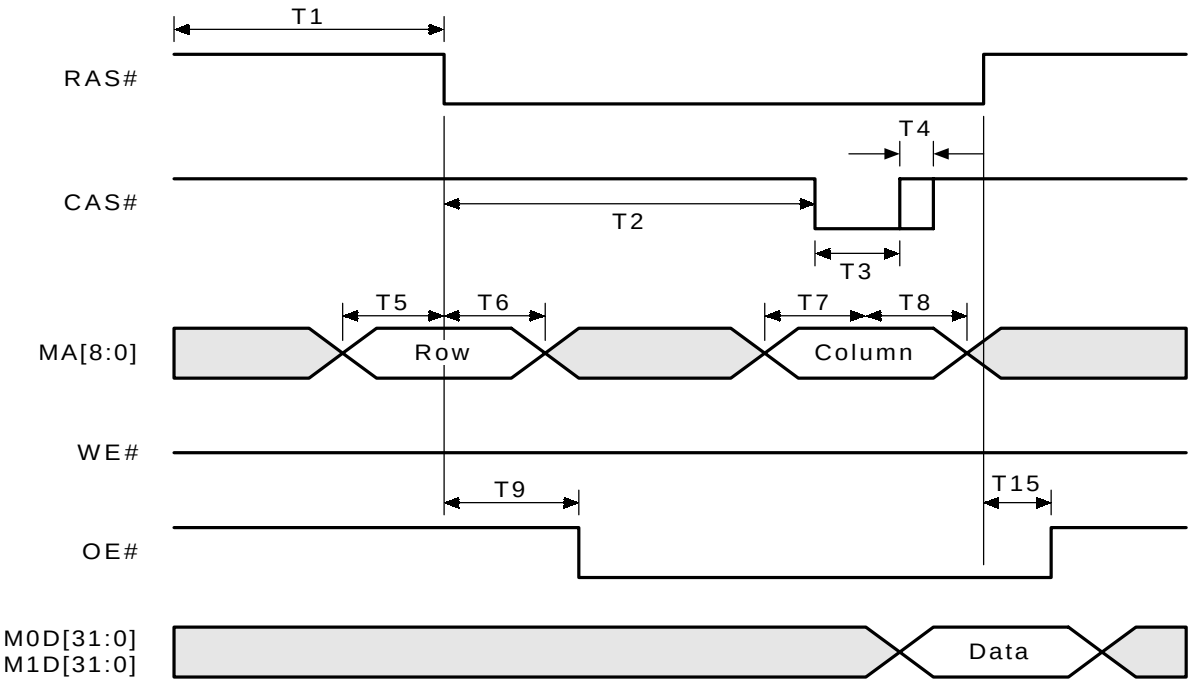
Symbol	Parameter	MIN	MAX	Units
t1	EA [15:0] delay from CLK	-	15	ns
t2	EPCS# delay from CLK	-	15	ns



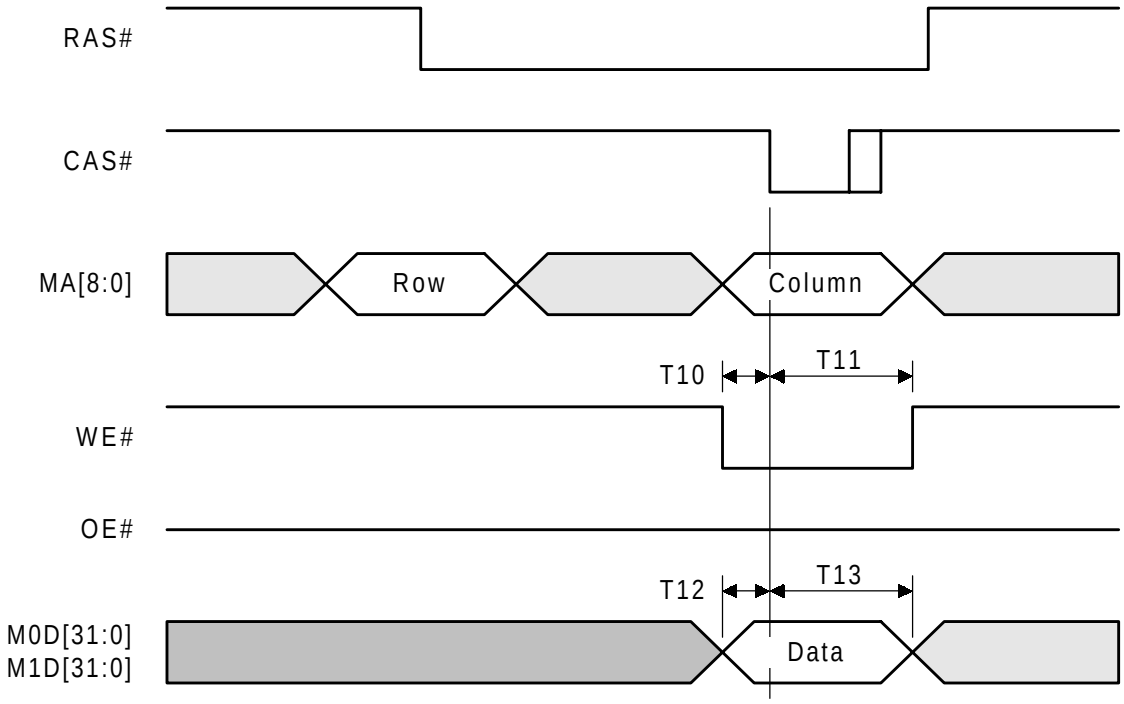
High = High-Impedance

EPCS#, EA [15:0] Timing (PCI Bus)

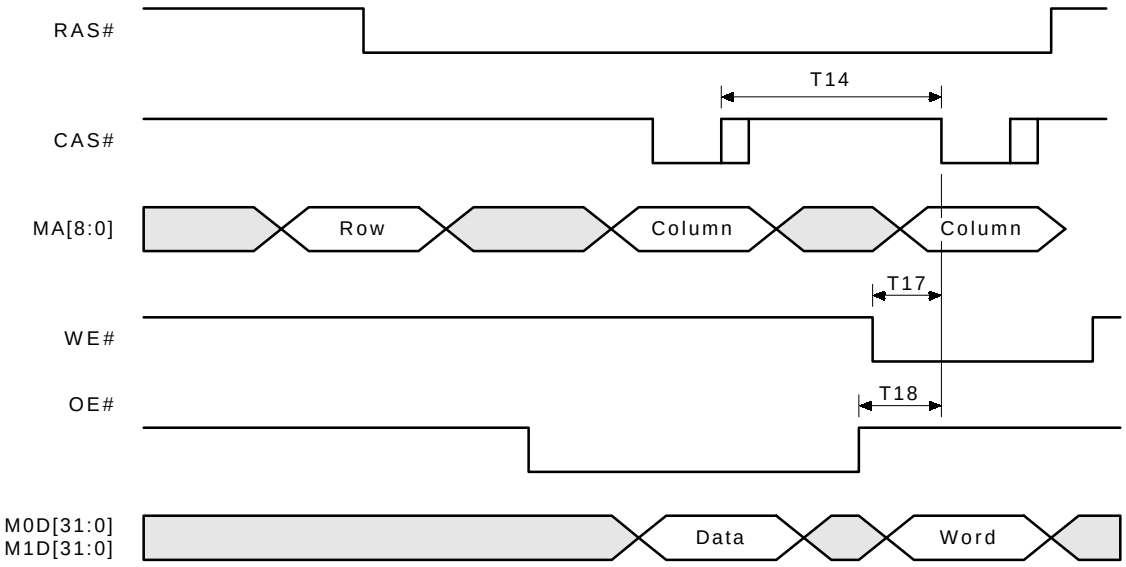
Read Cycle



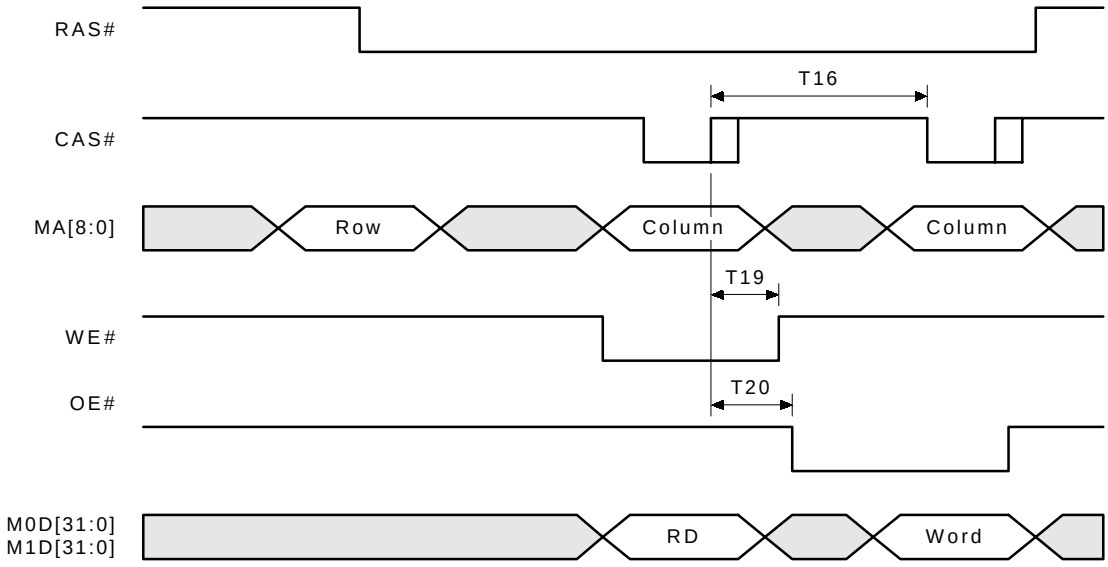
Write Cycle



Read-to-Write Cycle



Write-to-Read Cycle



Timing Parameters

Symbol	T Periods (T = 1xMCLK)	Register[Bits]
T1	2.5-4T	3CE.70[0]; 3CE.70[1]
T2	2.5-4T	3CE.70[0]; 3CE.70[2]
T3	1T	Fixed
T4	0,2,4,6 ns	3CE.79[1:0]
T5	2.5-3T	3CE.70[0]
T6	2T	Fixed
T7	0.5-1T	3CE.F4[0]
T8	1-1.5T	3CE.F4[0]
T9	2-2.5T	3CE.70[0]
T10	0.5T	Fixed
T11	1.5T	Fixed
T12	0.5-1T	3CE.73[5]
T13	1-1.5T	Fixed
T14	1-3T	3CE.73[1]; 3CE.7A[0]
T15	1T	Fixed
T16	1-2T	3CE.7A[1]
T17	0.5-2.5T	3CE.F8[1:0]
T18	1-3T	3CE.F8[3:2]
T19	0.5T	Fixed
T20	1T	Fixed

Electrical Characteristics

Absolute Maximum Ratings

Ambient temperature	0°C to 70°C
Storage temperature	65°C to 150°C
Voltage on any digital pin	-0.5V to Vcc + 0.5V
Power supply voltage	-0.5V to 7.0V
Injection current (latch-up testing)	100mA
DC Specifications (Digital)	(Vcc = 5V ± 5%, TA = 0° to 70°C, unless otherwise specified.

Note:

Stresses above those listed may cause permanent damage to the device. These are absolute stress ratings only. Functional operation at these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Symbol	Parameter	MIN	MAX	Units	Test Conditions
IVcc	Internal Power Supply Voltage	4.75	5.25	V	5.0V Operation
BVcc	I/O Bus Interface Power Supply Voltage	4.75 3.0	5.25 3.6	V V	5.0V Bus Interface 3.3V Bus Interface
ICC	Power Supply Current		480	mA	MCLK = 50 MHz VCLK = 80MHZ
VIL	Input Low Voltage	0	0.8	V	
VIH	Input High Voltage	2.0	Vcc + 0.5	V	
VOL	Output Low Voltage		0.5	V	IOL = 8mA
VOH	Output High Voltage	2.4		V	IOH = -400*uA*
IOH	Output High Current	-400		µA	VOH = 2.4V
IOL	Output Low Current	8		mA	VOL = 0.5V
IOZ	Input Leakage	-10	10	µA	0 < VIN < VCC
CIN	Input Capacitance		7	pF	
COUT	Output Capacitance		10	pF	

DAC Characteristics

(Vcc = 5V ± 5%, TA = 0° to 70° C)

Parameter	MAX	Units	Test	Note
Resolution (each DAC)	8	Bits		
Output Current (White Level)	20	mA	VO <1V	1,2
Analog Output Rise/Fall Time	8	ns		4
Analog Output Settling Time	15	ns		5
Analog Output Skew	TBD	ns		
DAC-to-DAC Matching	5	%		
Glitch Impulse Typical	TBD	pV-Sec		
Integral Linearity Error	±1	LSB		
Differential Linearity Error	±1	LSB		

Notes:

IREF = 8.39mA.

Load is 37.5Ω and 10 pF per analog output.

TD is measured from the 50% point of VCLK to 50% point of full-scale transition.

Rise time is measured from 10% to 90% full-scale; fall time is measured from 90% to 10% full-scale.

Settling time is measured from 50% of full-scale transition to output remaining within 2% of final value.

Clock Synthesis

The CyberPro2010 contains two phase-locked loop (PLL) frequency synthesizers. These generate the VCLK (video clock) and MCLK (memory clock) signals.

Each PLL uses a single reference frequency input on the XIN pin. By placing a parallel-resonant crystal between the XOUT output pin and the XIN pin the reference frequency is generated by the 2010's internal oscillator. Alternately, a CMOS-compatible clock input from a crystal oscillator can be connected to XIN to provide the reference frequency. (See Application Note IGS002)The frequency synthesized by each PLL is determined by the following equation:

$$f\,OUT = f\,REF \times \frac{(M+1)}{(N+1) \times Q}$$

Where Q = 1,2,4,6

The PLL M value can be programmed with any integer value from 1 to 255 for MCLK and VLCK. The binary equivalent of this value is programmed in bits 7-0 of B2 for the MCLK and in bits 7-0 of B0 for the VLCK. The PLL feedback loop frequency from the voltage controlled oscillator stage is scaled by dividing that frequency by (M+1).

The PLL N value can be programmed with any integer value from 1-31 for MCLK and VLCK. The binary equivalent of this value is programmed in bits 4-0 of B3 for the MCLK and in bits 4-0 of B1 for the VCLK. The reference frequency is divided by (N+1) before being fed to the phase detector stage of the PLL.

The PLL P value is a 2-bit range value that can be programmed with any integer value from 0 to 3. The P value is programmed in bits 7-6 of B3 for MCLK and bits 7-6 of B1 for VCLK. This value codes the selection of a frequency divider for the PLL output. Bit 5 for B1 and B3 set to 0.

Q = 1, if P= 0 Q = 2, if P= 1 Q = 4, if P= 2 Q = 6, if P= 3

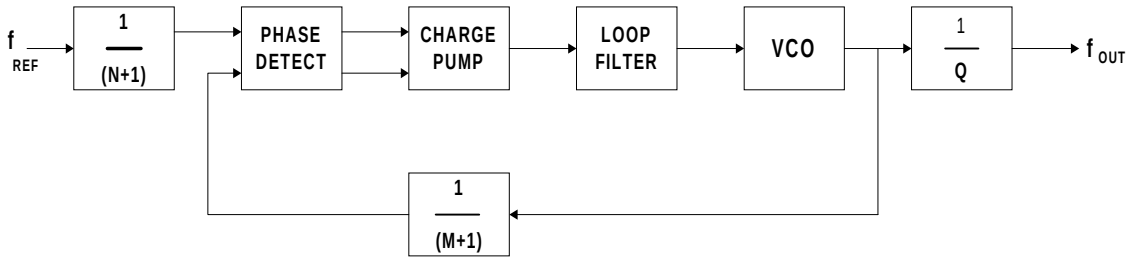


Figure 12-1. PLL Block Diagram

The following sequence may be followed to arrive at M and N values for any mode.

$$M = \frac{f\ OUT \times (N+1) \times Q}{f\ REF} - 1 \qquad \textbf{Notes}: N \leq 31,\ M \leq 255$$

1. Calculate a Q which does not violate the following constraints: 115 MHz $\leq f\ OUT * Q \leq$ 260 MHz

2. Start with N=1 and calculate:

3. Determine if the following constraint is met:

$$0.995\ f\ OUT < \frac{(M+1)\ f\ REF}{(N+1)\ Q} < 1.005\ f\ OUT$$

4. If the constraint in step 3 is met, the M and N values used will generate the desired frequency (within the specified tolerance). If the constraint is not met, repeat steps 2 and 3 with N increased by 1 each time until the constraint in step 3 is met. Note that multiple combinations of M and N are possible for a given output frequency. In this case choose the minimum M or N combination.

Clock Reprograming

If 3C2<3,2 >=1,1 = 00b, the VCLK PLL parameters are using the default values to generate a frequency of 25.175 MHz. This is the VCLK frequency generated at power on to support standard VGA operation.

If 3C2<3-2 = 01b, the VCLK PLL parameters are using the default values to generate a frequency of 28.322MHz.

For Enhanced mode operation, 3C2<3-2 are programmed to 11b and the VCLK PLL values are taken from B0 and B1. No default values are defined for these registers.

New VCLK PLL parameter values can be programmed at any time.

To load the new VCLK frequency toggle bit 7 of B9 by programming it to a 1 and then a 0. This immediately loads the VCLK (and MCLK) frequencies (no variable delay). For example, pseudo code to change VCLK to the frequency specified by PLL parameter values of B0=E2H and B1= 58H is:

3C2<3,2>=1,1

3CE_B0=E2h

3CE_B1=58h

3CE_B9<7>=1

3CE_B9<7>=0

After power-up, all MCLK frequency changes must be made by re-programming B2 and B3. If bit 7 of B9 is cleared to 0, the new frequency does not take effect until a 1 has been written to bit 7 of B9. This bit must then be cleared to 0 to prevent repeated loading. Actual loading will be delayed for a short but variable period of time.

Video Clock Programmable Frequencies
The following table lists the parameters for the programmable frequencies.

Notes: This is a example of M, N, B0, B1 of VCLK with fref = 14.31818 MHz

VCO: 115 MHz to 260 MHz

V*out* = 14.31818 MHz x (M+1)/((N+1)Q); M = 8-bit counter (From register B0)
N = 5-bit counter (From register B1)

VCO = V*out* x Q, where Q=1 if P=0; Q=2 if P=1; Q=4 if P=2; Q=6 if P=3;
P = 2-bit divider (From register B1)

After programming registers B0 and B1, register B9[7] must be toggled from 0 to 1 and then back to 0 in order to enable the video PLL.

Video Clock Programmable Frequencies

Frequencies (MHz)		Parameters					
Video Output	VCLK VCO	(P) 7-6	(B1) 5	(N) 4-0	(B0) (8-bit) VM	(B1)	Error Rate
25.175	151.05	3	0	19	210/D2h	D3h	.000046
28.322	169.932	3	0	14	177/B1h	CEh	.00014
31.500	189	3	0	04	65/41h	C4h	.0000001
32.000	192	3	0	16	227/E3h	D0h	.00017
36.000	144	2	0	17	180/B4h	91h	.00016
40.000	160	2	0	16	189/BDh	90h	.00017
44.900	179.6	2	0	12	162/A2h	8Ch	.00041
49.500	198	2	0	05	82/52h	85h	.00035
50.000	200	2	0	17	250/FAh	91h	.0018
50.350	201.4	2	0	14	210/D2h	8Eh	.000046
52.000	208	2	0	16	246/F6h	90h	.00017
56.644	226.576	2	0	10	173/ADh	8Ah	.0004
63.000	126	1	0	04	43/2Bh	44h	.0000001
65.000	130	1	0	24	226/E2h	58h	.00007
72.000	144	1	0	17	180/B4h	51h	.00016
75.000	150	1	0	20	219/DBh	54h	.0000001
78.800	157.6	1	0	01	21/15h	41h	.00064
80.000	160	1	0	16	189/BDh	50h	.00017
89.800	179.6	1	0	12	162/A2h	4Ch	.00041
95.000	190	1	0	14	198/C6h	4Eh	.00022
100.000	200	1	0	17	250/FAh	51h	.0018
105.000	210	1	0	02	43/2Bh	42h	.0000002
108.000	216	1	0	11	180/B4h	4Bh	.00016
110.000	220	1	0	10	168/A8h	4Ah	.000095
115.000	230	1	0	14	240/F0h	4Eh	.0002
120.000	240	1	0	12	217/D9h	4Ch	.00044
125.000	250	1	0	12	226/E2h	4Ch	.00007
130.000	130	0	0	24	226/E2h	18h	.00007
135.000	135	0	0	06	65/41h	06h	.0000001
140.000	140	0	0	08	87/57h	08h	.0000001

Video Clock Programmable Frequencies (continued)

Frequencies (MHz)		Parameters					
Video Output	VCLK VCO	(P) 7-6	(B1) 5	(N) 4-0	(B0) (8-bit) VM	(B1)	Error Rate
145.000	145	0	0	07	80/50h	07H	.0002
150.000	150	0	0	20	219/DBh	14h	.0000001
155.000	155	0	0	22	248/F8h	16h	.000064
160.000	160	0	0	16	189/BDh	10h	.000167
182.000	182	0	0	06	88/58h	06h	.00025
206.000	206	0	0	12	186/BAh	0Ch	.00019

Package Dimensions

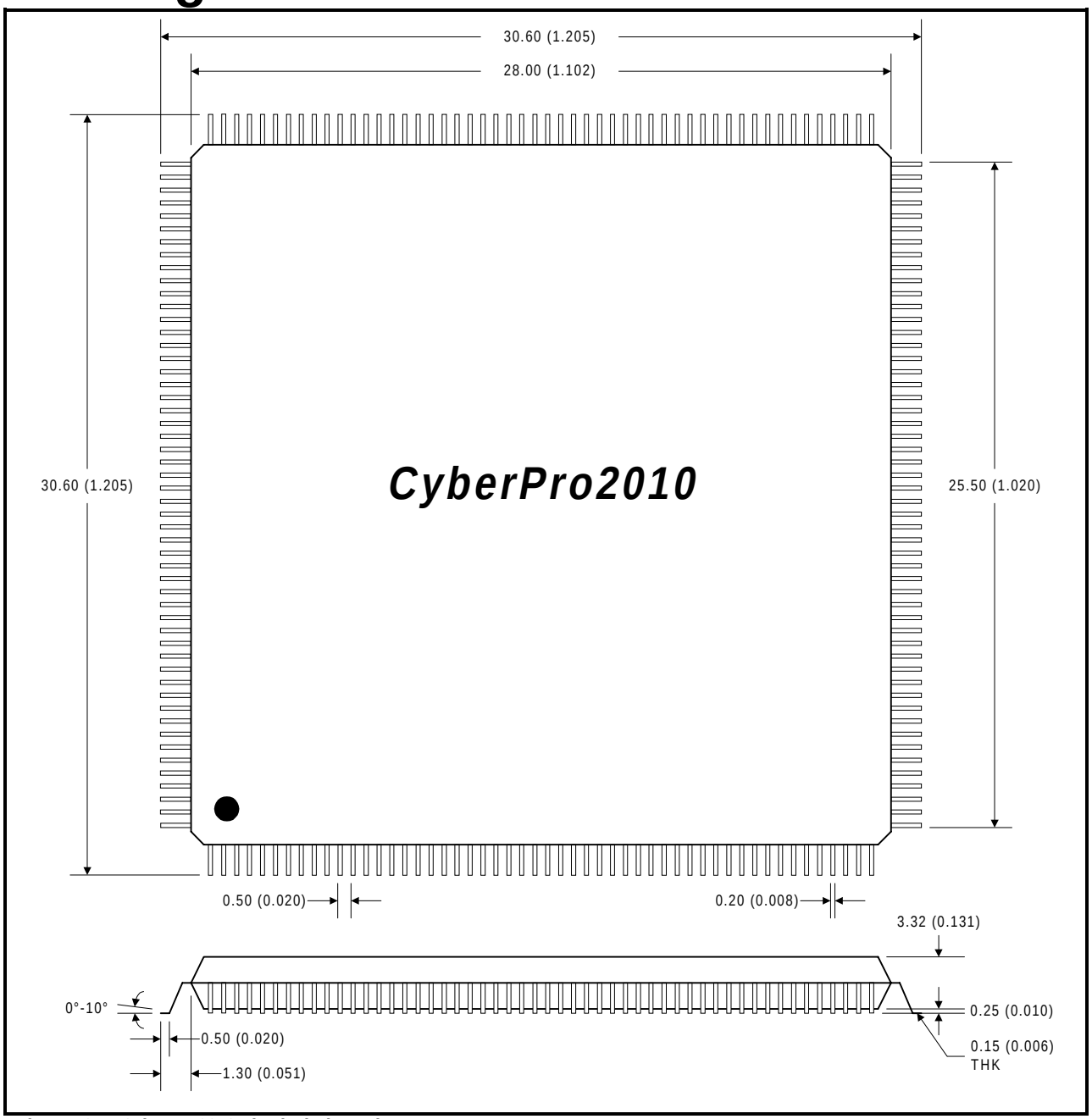


Figure 13-1. CyberPro2010 Physical Dimensions

Application Notes

Application Note IGS001

Power Plane Design

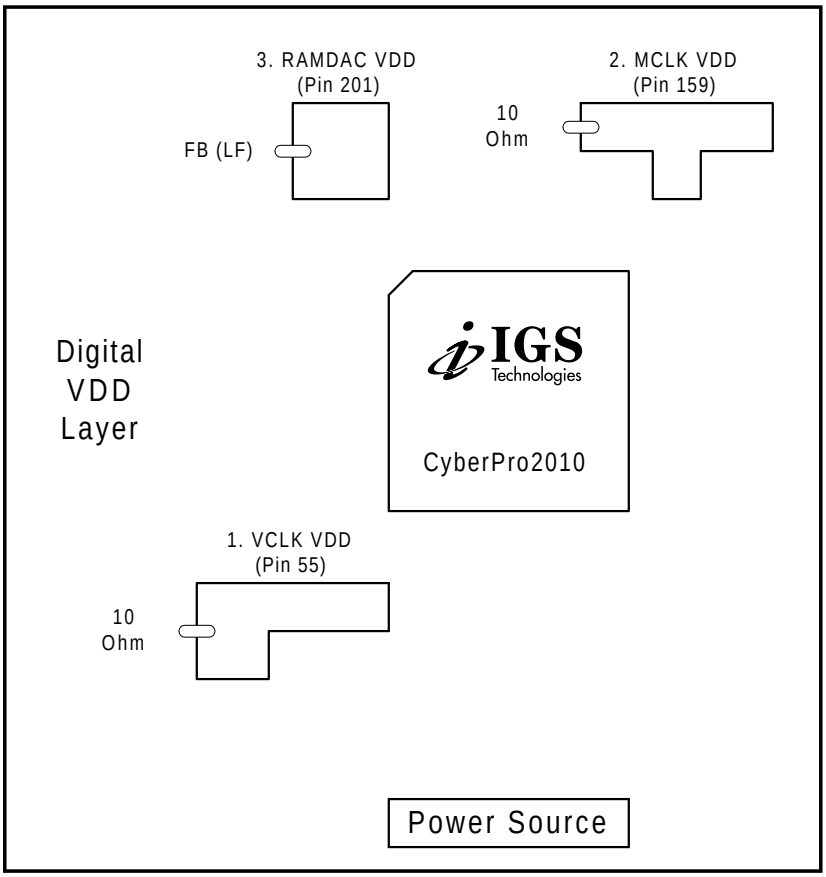
IGS Technologies, Inc. anticipates the use of multi-layer boards for all of its products, in order to assure the high performance designed into them and expected by our customers. The power plane is a separate layer on the PCB than the ground plane, and is intended to have three "islands", each isolated from each other. The following diagrams show the general layout of the CyberPro2010 chip and the power plane islands, as well as the schematics of each island.

Power Plane Island Layout

Figure 1-1 shows the three VDD islands in their general location in relation to the CyberPro2010. Note that the VCLK island (#1) location is of greater importance than the MCLK island (#2) location, as shown in Figure 1-1, because of the VCLK's effect on CRT picture quality. This relationship should be maintained.

The island numbers and their titles relate to the other figures (refer to Figures 1-2 through 1-4) in this application note. The shapes of the island areas shown are not exact and are intended as examples of shapes. However, please note that the VDD island areas that are associated with a GND cut area are the exact same shapes. In other words, the VDD island area and the associated GND cut area are identical. The only difference is the cuts for current flow on the GND cut areas.

Note: It is important that the VDD island areas are not crossed by the trace layer above it.



NOTE: Ensure all components are *inside* each of the island areas.

Figure 1-1: Power Plane Island Layout

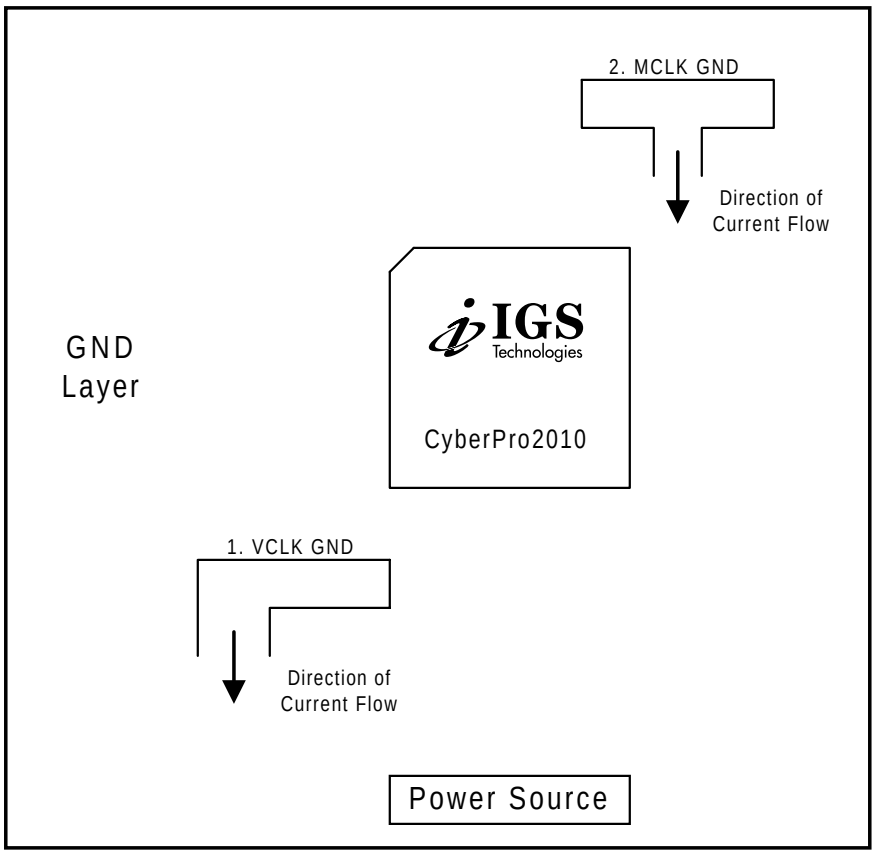
Ground Plane Design

The ground plane is a separate layer on the PCB than the power plane, and is intended to have two “cuts”, each isolated from each other. The ground cuts are designed to suppress currents between all the adjacent areas on the layered PCB.

Ground Plane Cuts Layout

Figure 1-2 shows the two ground plane cuts in their general location in relation to the CyberPro2010. The island numbers and their titles relate to the other figures in this application note.

Note: It is important that the GND cut areas are not crossed by the trace layer below it.



NOTE: Ensure the open side of the ground cuts are facing the power source. The intent is to provide an easy path for current flow.

Figure 1-2: Ground Plane Cut Layout

VCLK Schematic

In Figure 1-3, the power plane island is outlined in dashed lines and the ground plane cut is shown in dark straight lines.

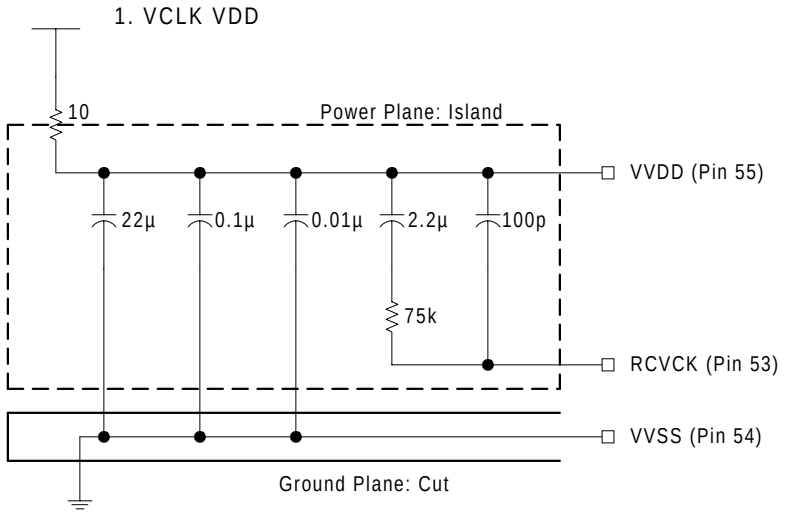


Figure 1-3: VCLK Schematic

MCLK Schematic

In Figure 1-4, the power plane island is outlined in dashed lines and the ground plane cut is shown in dark straight lines.

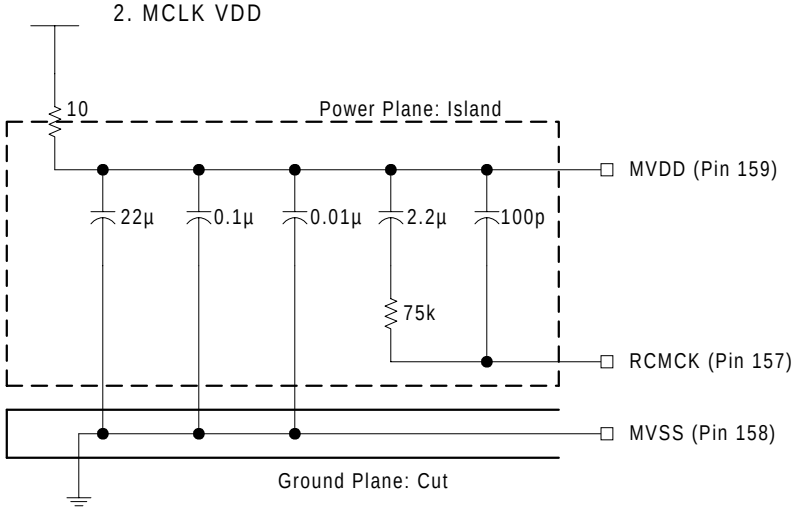


Figure 1-4: MCLK Schematic

RAMDAC Schematic

In Figure 1-5, the power plane island is outlined in dashed lines.

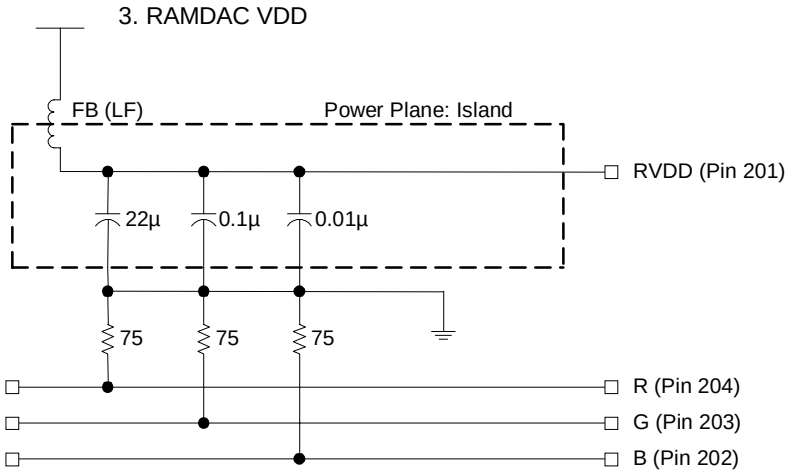


Figure 1-5: RAMDAC Schematic

Analog RGB Output Design

In order to protect the RGB output signals, the CRT connector should be located as close as possible to the CyberPro2010 chip, ensuring that no other signals run parallel with the RGB signals. Each RGB signal should have a protective ground cut on each side, as shown in Figure 1-6.

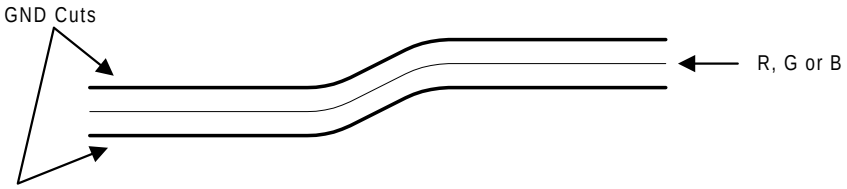


Figure 1-6: Analog RGB Output Design

Power Source Location

In order to reduce cross talk, the power source should be located as close as possible to the CyberPro2010 chip, as indicated in Figure 1-7.

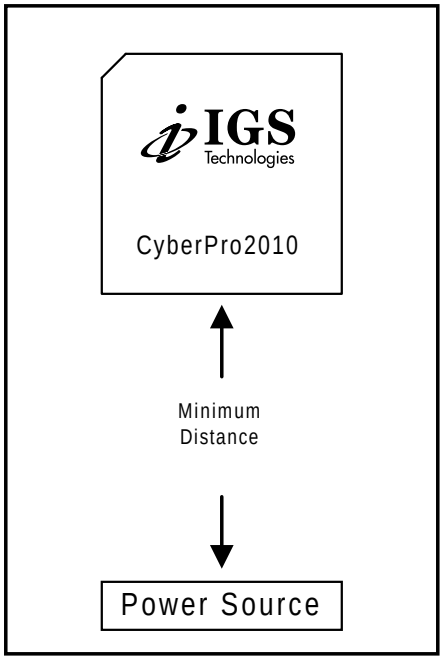


Figure 1-7: Power Source Location

DRAM Isolation

In order to reduce noise in the DRAM area, the DRAM area should be isolated from the CyberPro2010 chip by using a ground cut, as indicated in Figure 1-8.

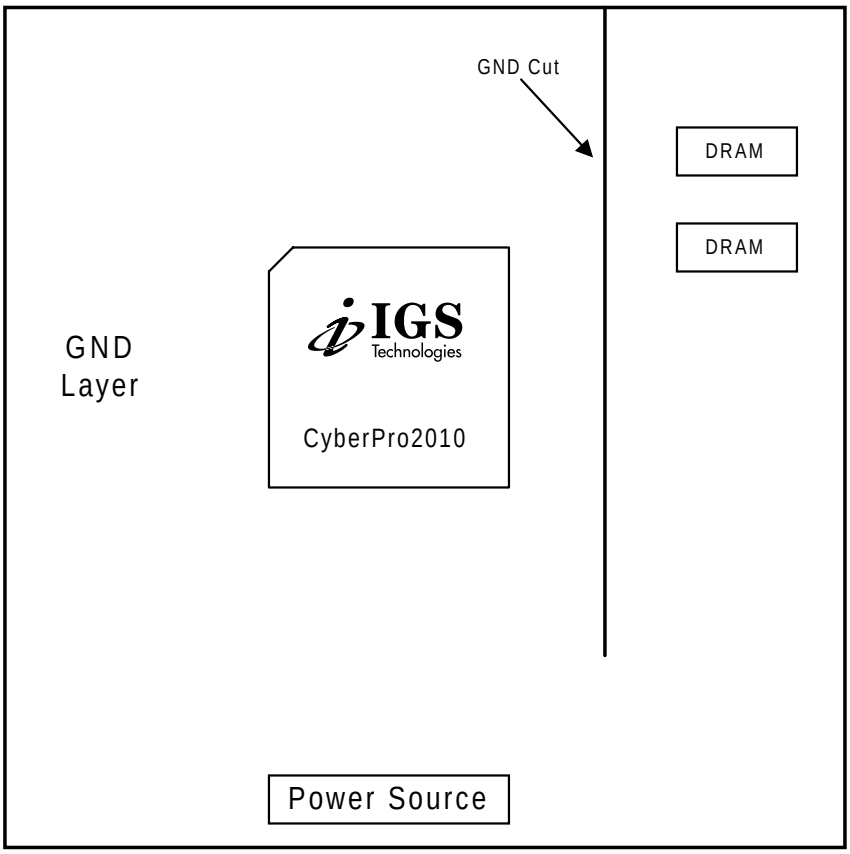


Figure 1-8: DRAM Isolation

Application Note IGS002

Oscillator Component Change

IGS's efforts to make continuous design improvements has led to a decision to use oscillators instead of crystals in our design recommendations. The reason is primarily to provide better performance for TV output. A very accurate frequency is required to prevent unwanted color changes under certain circumstances with various hardware systems.

Oscillator Connection (For TV Out ONLY - Default)

If TV output is provided, then the oscillator solution is the one that must be used. IGS's preferred design requirement is to use a 14.31818 MHz oscillator as shown in Figure 2-1.

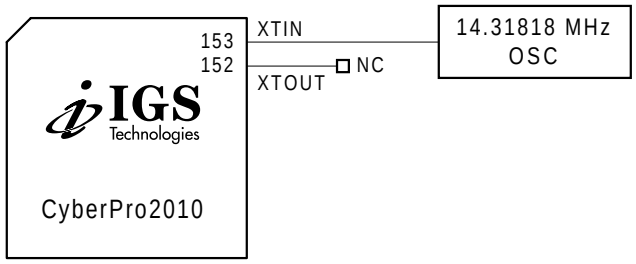


Figure 2-1: Oscillator Schematic (TV Out Only - Default)

Crystal Utilization Option Requirements (For Non-TV Out ONLY)

As long as is it is for a non-TV output design, an OEM can use a crystal if they absolutely must or desire to do so. However, they must follow all of the following design requirements:

1. The crystal circuit must be as shown in Figure 2-2.
2. The crystal must be located as close as possible to the CyberPro2010 chip.
3. DRAM interference must be prevented by using a ground cut between the DRAM and the crystal, as indicated in Figure 1-8.

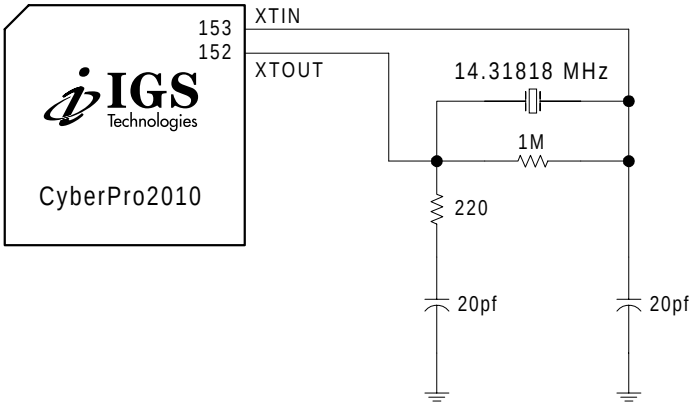


Figure 2-2: Crystal Schematic (Option)

Application Note IGS003

RAMDAC VDD Requirements

In order to reduce noise, the 5.0V source for the RAMDAC should be an independent and clean source, separate from the voltage source for the rest of the PCB components.

RAMDAC VDD Source Input

The following RVDD voltage sources are recommended:

1. The preferred method is to use a 12.0V source coupled with a 7805 voltage regulator for a 5.0V output as shown in Figure 3-1.
2. An optional method, for those situations that lack a 12.0V source, is to use a 5.0V source coupled with an LT1521 low dropout regulator for a 4.5V output as shown in Figure 3-2.

Preferred Method

The circuit for the preferred RAMDAC VDD source input is shown in Figure 3-1.

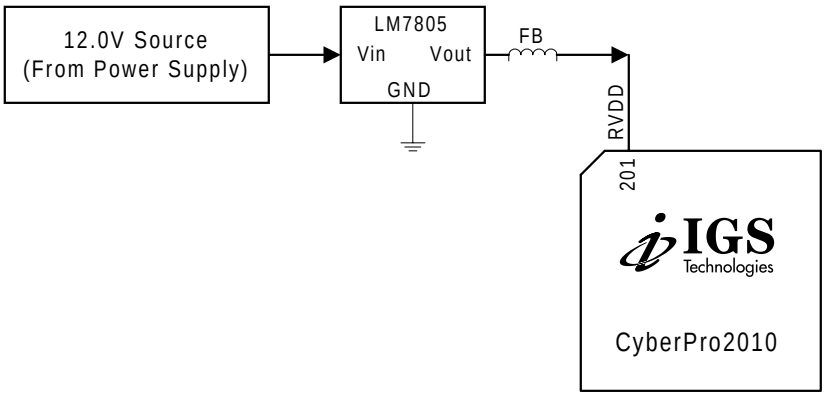


Figure 3-1: Preferred RVDD Voltage Source

Optional Method

The circuit for the optional RAMDAC VDD source input is shown in Figure 3-2.

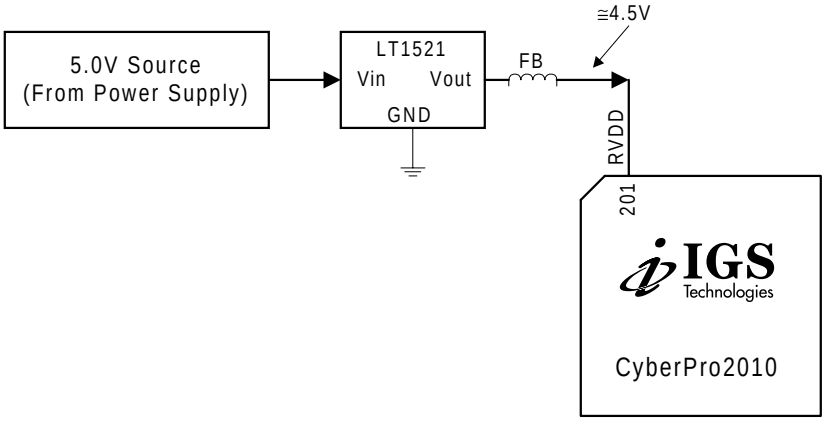


Figure 3-2: Optional RVDD Voltage Source

Application Note IGS004

Video Clock Specifications

Video clock frequency selection is accomplished by CLKSEL1 and CLKSEL2, as defined in the following table.

CLKSEL1	CLKSEL2	Video Output Frequency (MHz)	
0	0	25.175	;IBM mode
0	1	28.322	;IBM mode
1	0	(Not Used)	
1	1	15-260	;Programmable

Video Clock Programmable Frequencies

The following table lists the parameters for the programmable frequencies.

Notes:

VFSEL = 0 (In register B1)

VCO: 115 MHz to 260 MHz

Vout = 14.31818 MHz x (M+1)/((N+1)Q); M = 8-bit counter (From register B0)
N = 5-bit counter (From register B1)

VCO = Vout x Q, where Q=1 if P=0; Q=2 if P=1; Q=4 if P=2; Q=6 if P=3;
P = 2-bit divider (From register B1)

After programming registers B0 and B1, register B9[7] must be toggled from 0 to 1 and then back to 0 in order to enable the video PLL.

Table 4-1: Video Clock Programmable Frequencies

Frequencies (MHz)		Parameters					
Video Output	VCLK VCO	(2B) VP	(1B) VFSEL	(5B) VN	(B0) (8-bit) VM	(B1)	Error Rate
25.175	151.05	3	0	19	210/D2h	D3h	.000046
28.322	169.932	3	0	14	177/B1h	CEh	.00014
31.500	189	3	0	04	65/41h	C4h	.0000001
32.000	192	3	0	16	227/E3h	D0h	.00017
36.000	144	2	0	17	180/B4h	91h	.00016
40.000	160	2	0	16	189/BDh	90h	.00017
44.900	179.6	2	0	12	162/A2h	8Ch	.00041
49.500	198	2	0	05	82/52h	85h	.00035
50.000	200	2	0	17	250/FAh	91h	.0018
50.350	201.4	2	0	14	210/D2h	8Eh	.000046
52.000	208	2	0	16	246/F6h	90h	.00017
56.644	226.576	2	0	10	173/ADh	8Ah	.0004
63.000	126	1	0	04	43/2Bh	44h	.0000001
65.000	130	1	0	24	226/E2h	58h	.00007

Table 4-1: Video Clock Programmable Frequencies (Continued)

Frequencies (MHz)		Parameters					
Video Output	VCLK VCO	(P) 7-6	(B1) 5	(N) 4-0	(B0) (8-bit) VM	(B1)	Error Rate
72.000	144	1	0	17	180/B4h	51h	.00016
75.000	150	1	0	20	219/DBh	54h	.0000001
78.800	157.6	1	0	01	21/15h	41h	.00064
80.000	160	1	0	16	189/BDh	50h	.00017
89.800	179.6	1	0	12	162/A2h	4Ch	.00041
95.000	190	1	0	14	198/C6h	4Eh	.00022
100.000	200	1	0	17	250/FAh	51h	.0018
105.000	210	1	0	02	43/2Bh	42h	.0000002
108.000	216	1	0	11	180/B4h	4Bh	.00016
110.000	220	1	0	10	168/A8h	4Ah	.000095
115.000	230	1	0	14	240/F0h	4Eh	.0002
120.000	240	1	0	12	217/D9h	4Ch	.00044
125.000	250	1	0	12	226/E2h	4Ch	.00007
130.000	130	0	0	24	226/E2h	18h	.00007
135.000	135	0	0	06	65/41h	06h	.0000001
140.000	140	0	0	08	87/57h	08h	.0000001
145.000	145	0	0	07	80/50h	07H	.0002
150.000	150	0	0	20	219/DBh	14h	.0000001
155.000	155	0	0	22	248/F8h	16h	.000064
160.000	160	0	0	16	189/BDh	10h	.000167
182.000	182	0	0	06	88/58h	06h	.00025
206.000	206	0	0	12	186/BAh	0Ch	.00019

Memory Clock Programmable Frequencies

The following table lists the parameters for the programmable frequencies, which range from 15 MHz to 140 MHz.

Notes:

MFSEL = 0 (In register B3)
VCO: 115 MHz to 260 MHz
Mout = 14.31818 MHz x (M+1)/((N+1)Q); M = 8-bit counter (From register B2)
N = 5-bit counter (From register B3)
VCO = Mout x Q, where Q=1 if P=0; Q=2 if P=1; Q=4 if P=2; Q=6 if P=3;
P = 2-bit divider (From register B3)

After programming registers B2 and B3, register B9[7] must be toggled from 0 to 1 and then back to 0 in order to enable the memory PLL.

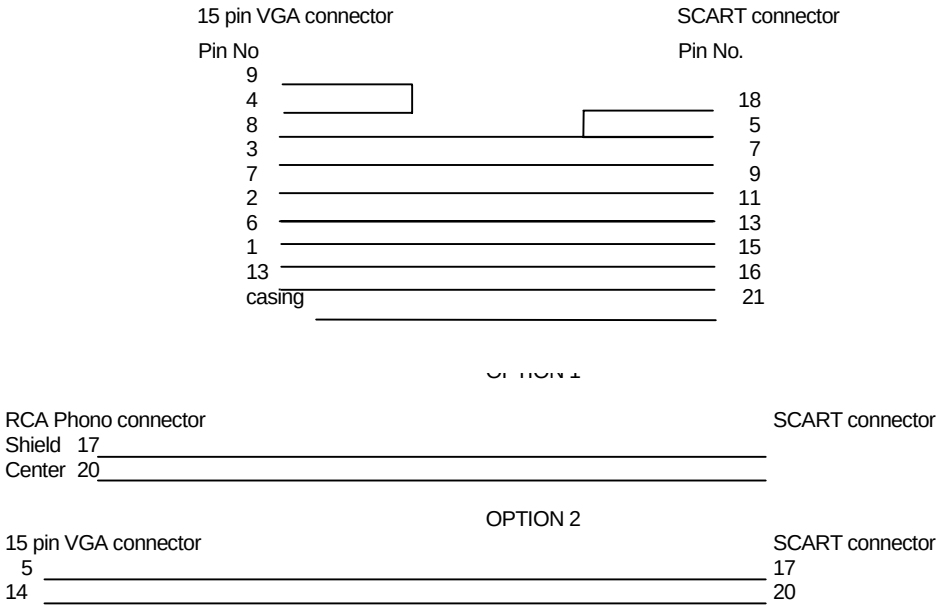
Table 4-2: Memory Clock Programmable Frequencies

Frequencies (MHz)		Parameters					
Video Output	MCLK VCO		(B1)		(B0) (8-bit) MM	(B3)	Error Rate
		(P) 7-6	5	(N) 4-0			
20.000	120	3	0	20	175/AFh	D4h	.0000001
30.000	180	3	0	06	87/57h	C6h	.00000014
40.000	160	2	0	16	189/BDh	90h	.00017
43.000	172	2	0	1	23/17h	81h	.00106
45.000	180	2	0	6	87/57h	86h	.00000014
50.000	200	2	0	17	250/FAh	91h	.0018 (Default)
55.000	220	2	0	10	168/A8h	8Ah	.000095
57.000	228	2	0	12	206/CEh	8Ch	.000047
60.000	120	1	0	20	175/AFh	54h	.0000001
62.000	124	1	0	28	250/FAh	5Ch	.0006
64.000	128	1	0	16	151/97h	50h	.00017
65.000	130	1	0	24	226/E2h	58h	.00007
66.000	132	1	0	22	211/D3h	56h	.00018
67.000	134	1	0	24	233/E9h	58h	.00014
68.000	136	1	0	13	132/84h	4Dh	.00017
70.000	140	1	0	08	87/57h	48h	.00000011
75.000	150	1	0	20	219/DBh	54h	.0000001
80.000	160	1	0	16	189/BDh	50h	.00017
85.000	170	1	0	7	94/5Eh	47h	.00017
90.000	180	1	0	06	87/57h	46h	.00000014
95.000	190	1	0	10	145/91h	4Ah	.00022
100.000	200	1	0	17	250/FAh	51h	.0018

Application Note IGS005

SCART to VGA Connector Cable

The CyberPro 2010 has the ability to output RGB signals at TV frequencies. This feature can be used in conjunction with a TV equipped with a SCART (or Peritel) connector as found on most European televisions. There follows a description of how to make a cable suitable for connecting the output of a card which has a 15 pin VGA connector to a SCART equipped TV.



There are two options for providing SYNC to the TV.

Option 1 allows Composite video to be SYNC. The advantage of this method is that when the RGB output is disabled then video can still be seen on the TV. This allows the user to change channel on the TV with the cable connected. The disadvantage is that a separate 'pigtail' to the RCA connector is required.

Option 2 has SYNC from the Composite Sync pin on the VGA connector. The advantage of this method is that a separate RCA connector is not required. The disadvantage is that if RGB is disabled in order to change channel on the TV the video output is lost until the system is reset.

Auto detection.

There are two options for SCART detection.

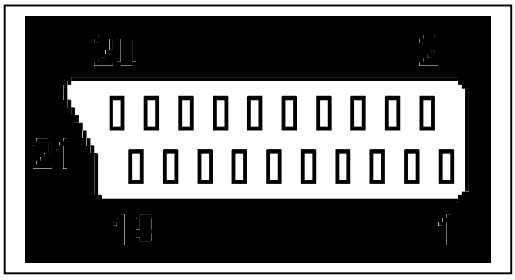
1. If there is no VGA cable connected the software will assume that there is a SCART cable connected. This may cause problems if the system is powered up without a monitor connected and then a VGA monitor is connected after the system boots. The image on the VGA monitor will be in two halves and the system will have to be reset.
2. To force the software to detect the presence of a SCART cable and not just the absence of a VGA cable it is necessary to connect pin 9 of the VGA connector on the PCB to VCC and pin 4 of the VGA connector on the PCB to pin 46 of the CyberPro2010 and pull it down with a 4.7k resistor.

The SCART Connector

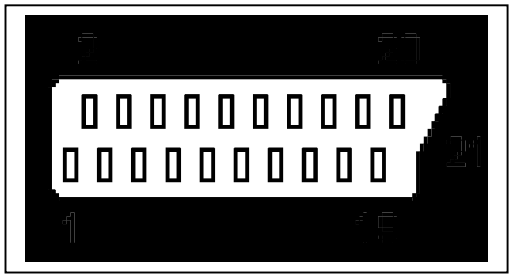
Most European televisions have at least one SCART connector. They are used to connect consumer equipment such as VCRs and Set Top Boxes to the TV. The following signals can be transmitted across the cable

- Composite video; in and out
- Stereo audio; in and out
- RGB; in
- Control; in
- In some cases a second SCART connector can carry S-Video signals

In most cases, when a VCR starts to play a video tape it signals the TV to switch its input to the SCART connector. In other cases the external equipment can signal that the TV should use the RGB input and/or that the incoming video is widescreen. When used in a Set Top Box application with the IGS Technologies CyberPro 2010 the resulting display quality using the CyberPro's SCART RGB output capability with flicker reduction in all modes, is the highest attainable .The video does not have to be bandwidth limited as required by the encoding process.



SCART FEMALE on the equipment



SCART MALE on the Cable.

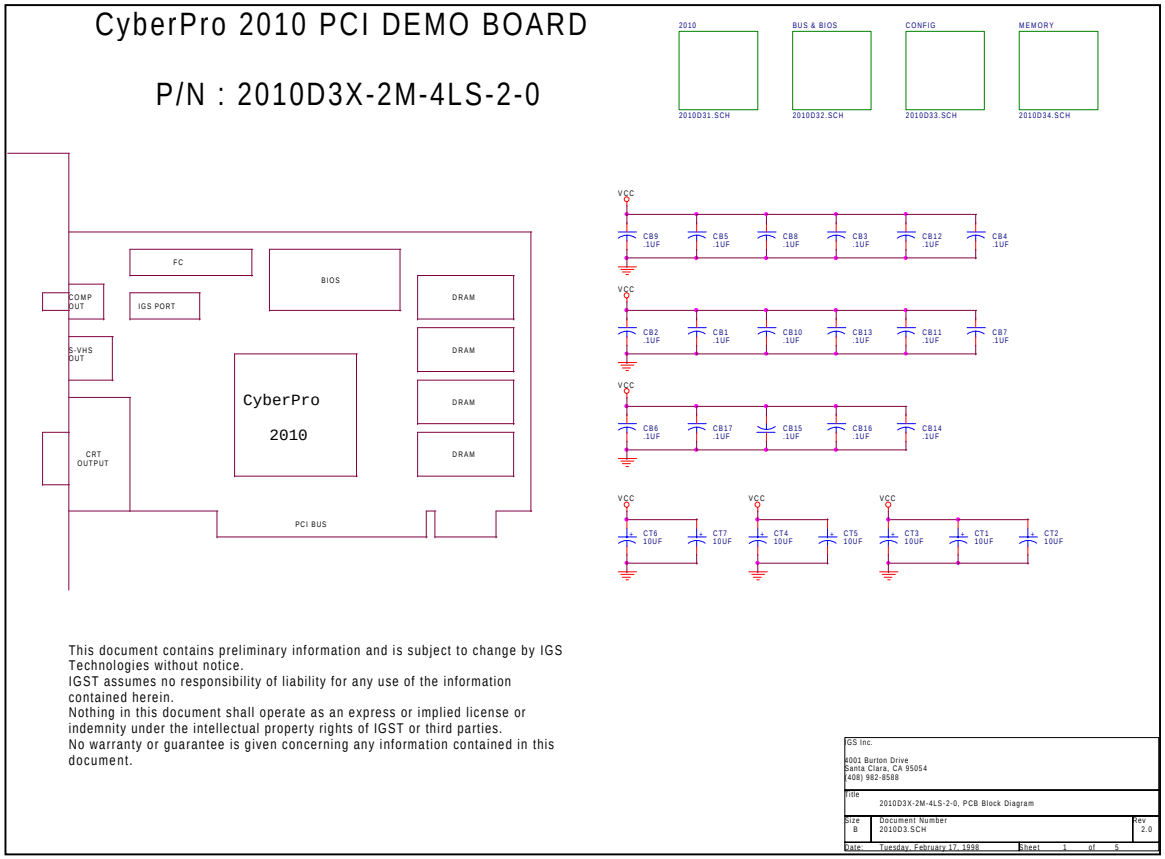
SCART Pin descriptions

Pin	Description	Pin	Description
1	audio output right	12	bus clock
2	audio input right	13	ground red
3	audio output left	14	ground bus
4	ground audio	15	red input
5	ground blue	16	Status RGB
6	audio input left	17	ground CVBS
7	blue input	18	ground Status RGB
8	Status CVBS	19	CVBS output
9	ground green	20	CVBS input
10	bus data	21	common ground (plug, shield)
11	green input		

SCART Signal levels

Signal	Level
Audio input	0.5Vrms, >10kohms
Audio output	0.5Vrms, <1kohm
RGB input	0.7±3dB, 75ohms, positive
Video input	1V±3dB, 75ohms, positive, sync: 0.3V (-3, +10dB)
Video output	1V±3dB, 75ohms, positive, sync: 0.3V (-3, +10dB)
Status CVBS	high: 9.5-12V, low: 0-2V, >10kohms, <2nF
Status RGB	high: 1-3V, low: 0-0.4V, 75ohms

SCHEMATICS


CyberPro 2010 PCI DEMO BOARD
P/N : 2010D3X-2M-4LS-2-0
2010
2010D31.SCH
BUS & BIOS
2010D32.SCH
CONFIG
2010D33.SCH
MEMORY
2010D34.SCH
FC
BIOS
COMP OUT
IGS PORT
S-VHS OUT
CRT OUTPUT
CyberPro
2010
DRAM
DRAM
DRAM
DRAM
PCI BUS
VCC
CB9 .1UF
CB5 .1UF
CB8 .1UF
CB3 .1UF
CB12 .1UF
CB4 .1UF
CB2 .1UF
CB1 .1UF
CB10 .1UF
CB13 .1UF
CB11 .1UF
CB7 .1UF
CB6 .1UF
CB17 .1UF
CB15 .1UF
CB16 .1UF
CB14 .1UF
CT6 10UF
CT7 10UF
CT4 10UF
CT5 10UF
CT3 10UF
CT1 10UF
CT2 10UF
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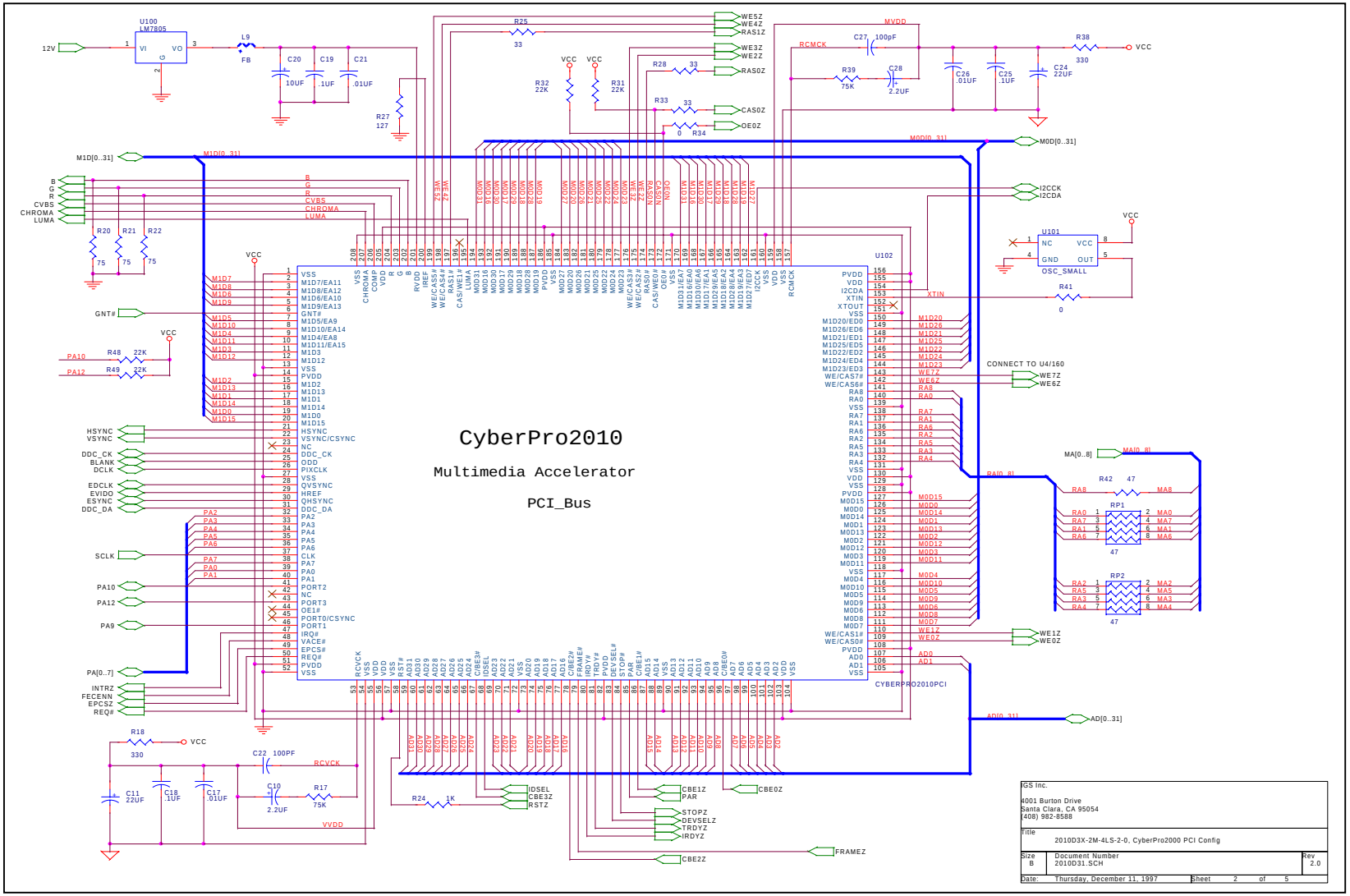
Title
2010D3X-2M-4LS-2-0, PCB Block Diagram
Size B
Document Number 2010D3.SCH
Rev 2.0
Date: Tuesday, February 17, 1998
Sheet 1 of 5


CyberPro2010
Multimedia Accelerator
PCI_Bus
U100
LM7805
U101
OSC_SMALL
U102
CYBERPRO2010PCI
IGS Inc.
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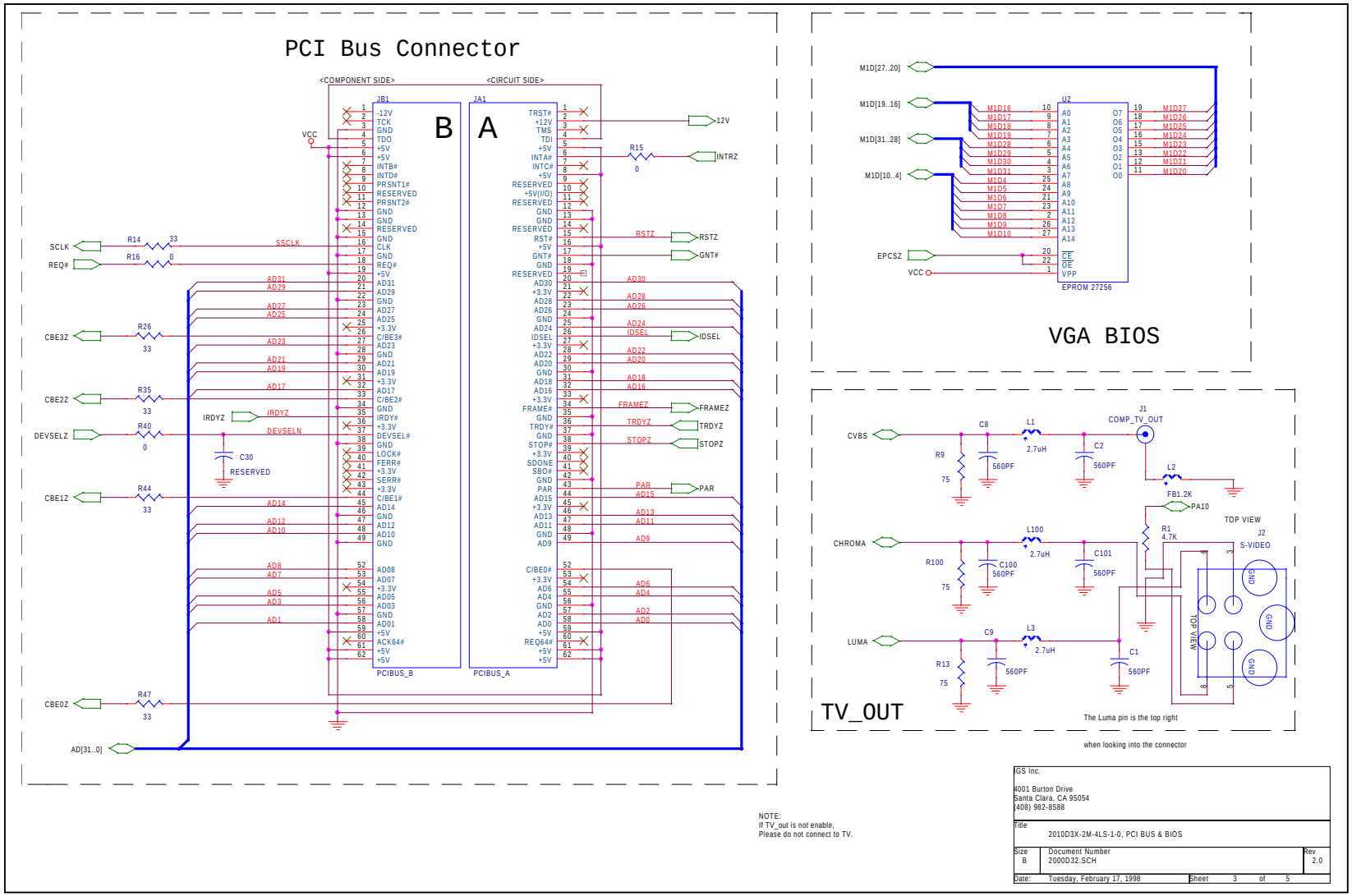
(408) 982-8588
2010D3X-2M-4LS-2-0, CyberPro2000 PCI Config
Document Number 2010D31.SCH
Rev 2.0
Thursday, December 11, 1997
Sheet 2 of 5



NOTE:
If TV_out is not enable,
Please do not connect to TV.

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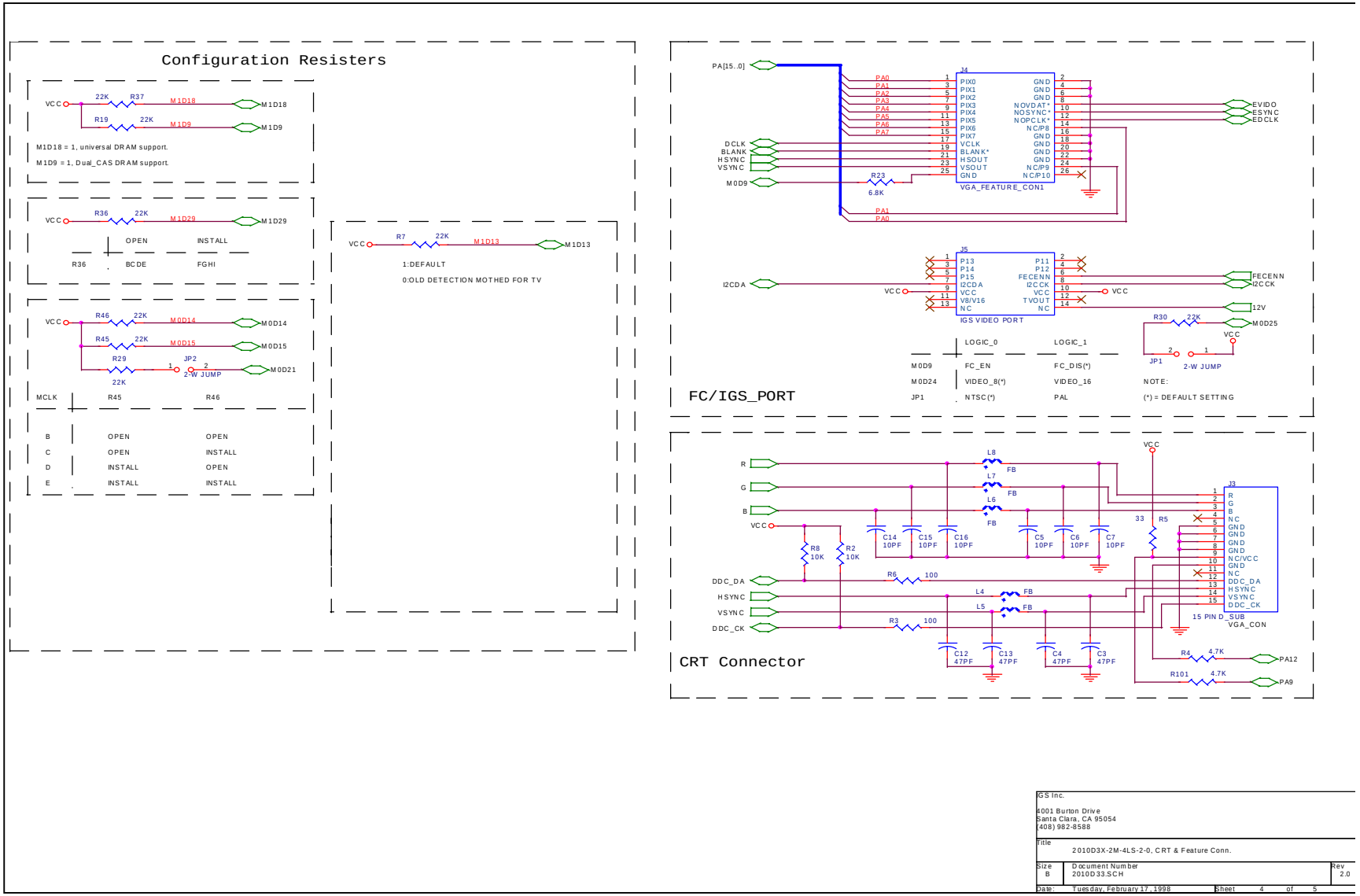
Title: 2010D3X-2M-4LS-1-0, PCI BUS & BIOS

Size	Document Number	Rev
B	2000D32.SCH	2.0

Date: Tuesday, February 17, 1998 Sheet 3 of 5



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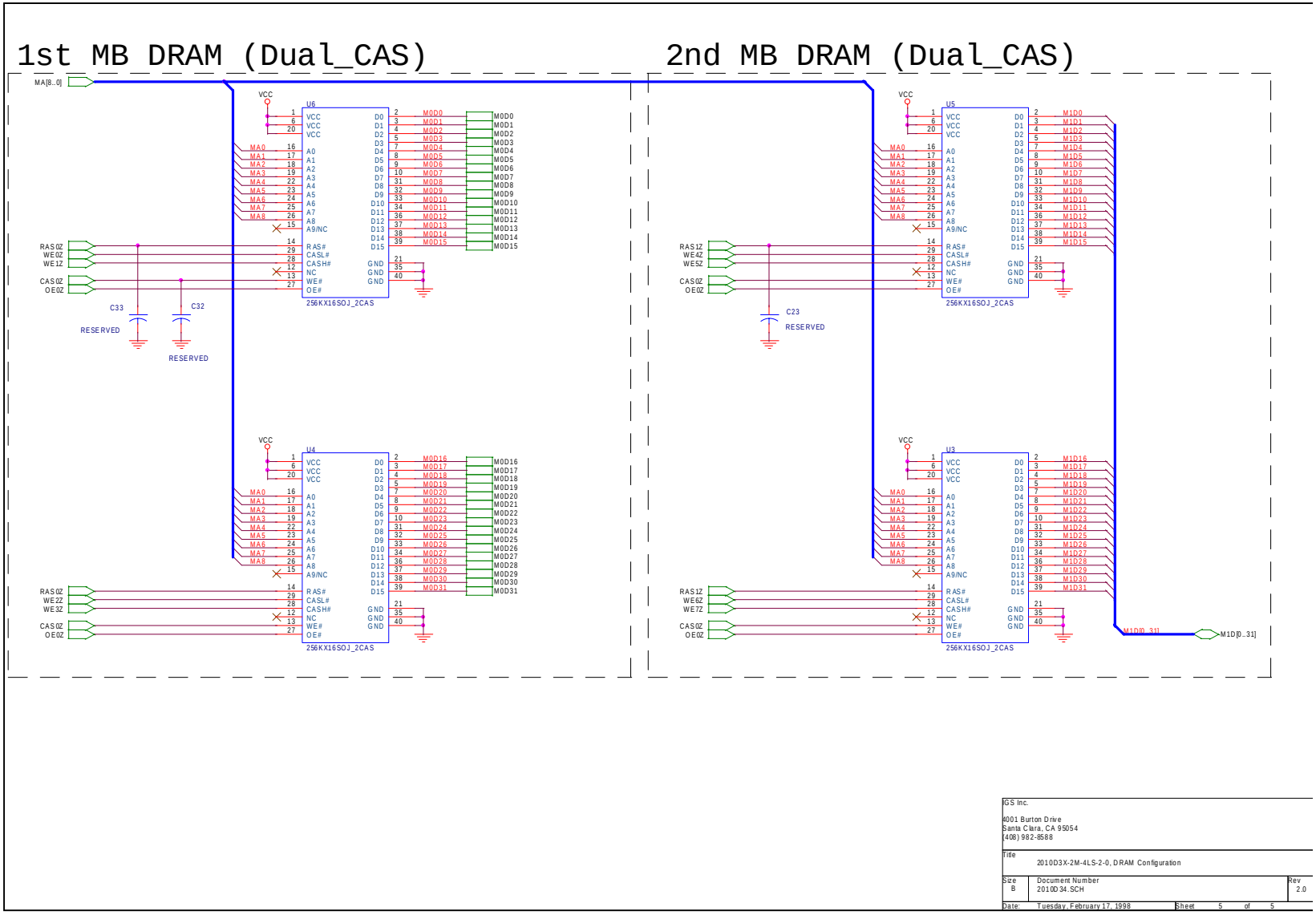
Title: 2010D3X-2M-4LS-2-0, CRT & Feature Conn.

Size: B | Document Number: 2010D33.SCH | Rev: 2.0

Date: Tuesday, February 17, 1998 | Sheet 4 of 5


1st MB DRAM (Dual_CAS)
2nd MB DRAM (Dual_CAS)
MA[8..0]
U6
U4
U5
U3
256KX16SOJ_2CAS
RAS0Z
WE0Z
WE1Z
WE2Z
WE3Z
CAS0Z
OE0Z
RAS1Z
WE4Z
WE5Z
WE6Z
WE7Z
C33
C32
C23
RESERVED
M0D[0..31]
M1D[0..31]
IGS Inc.
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Title
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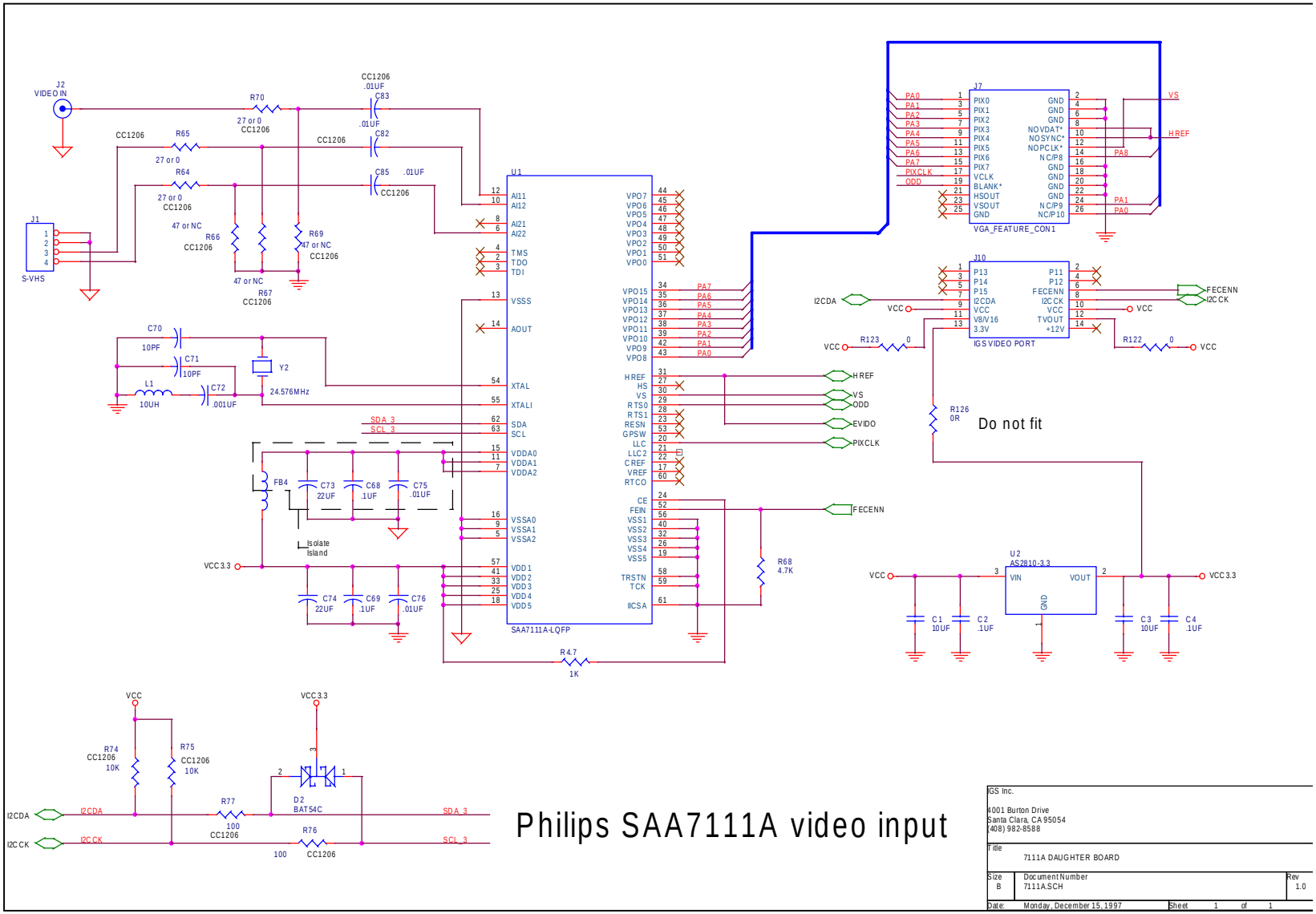
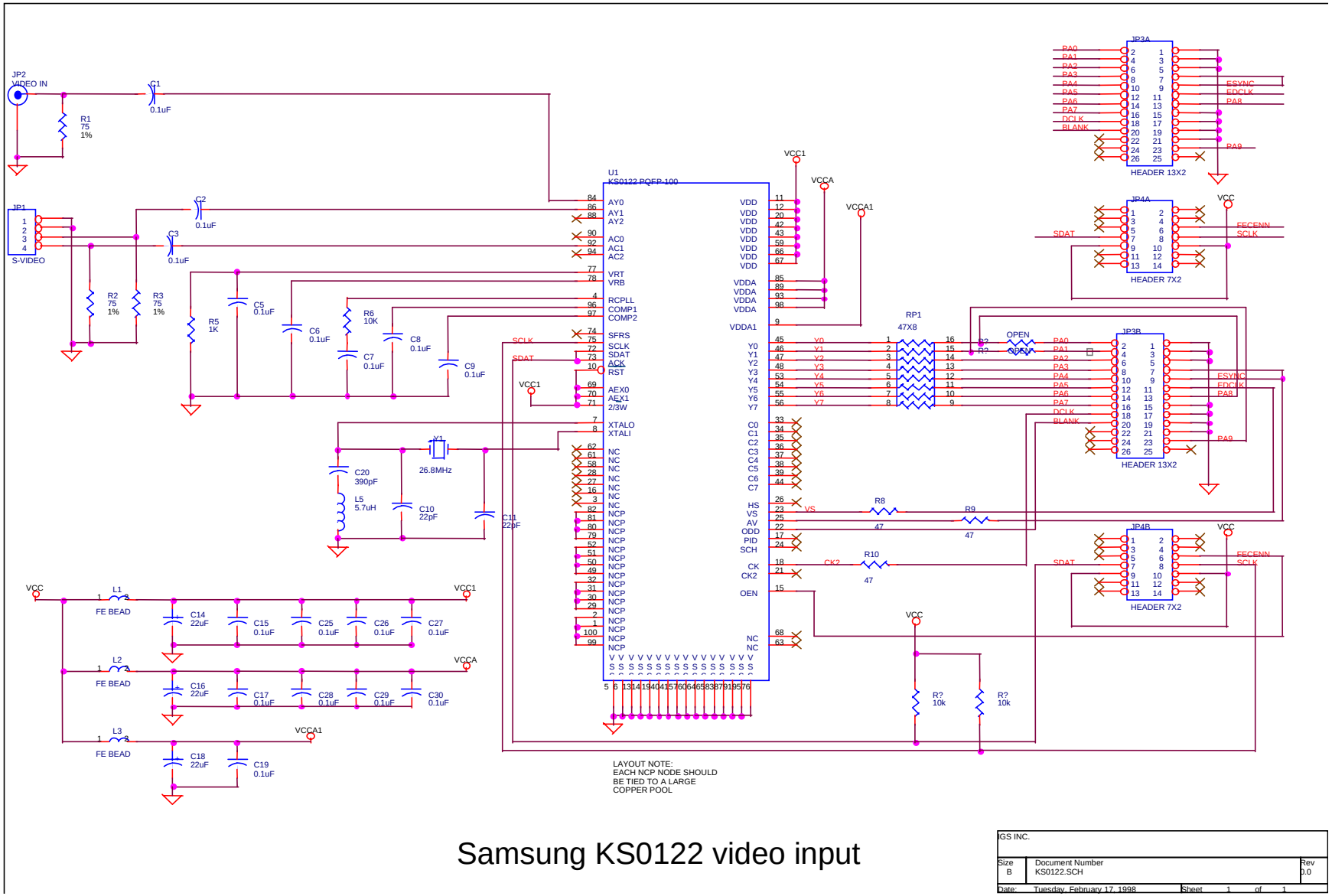
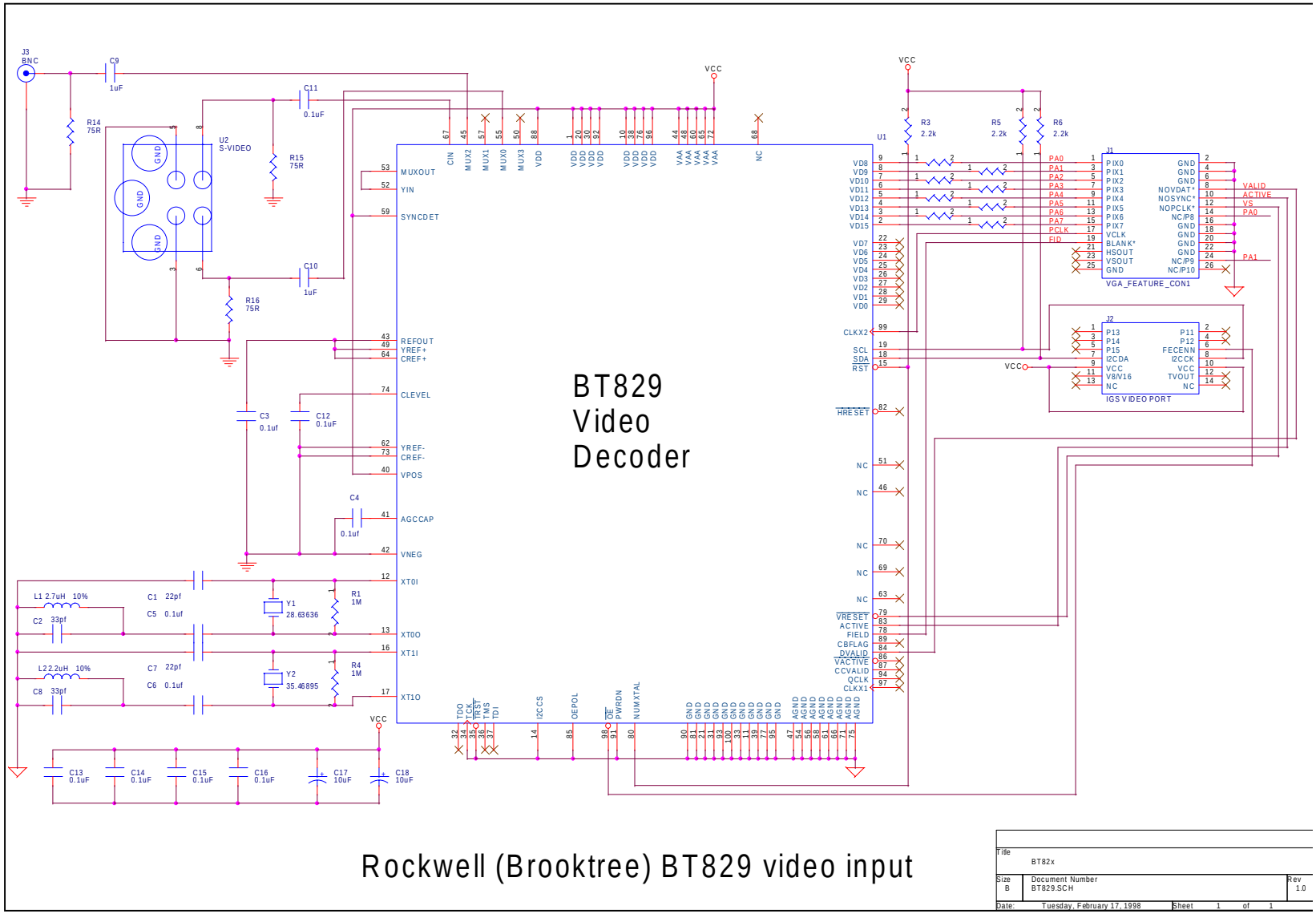
Size B
Document Number 2010D34.SCH
Rev 2.0
Date: Tuesday, February 17, 1998
Sheet 5 of 5

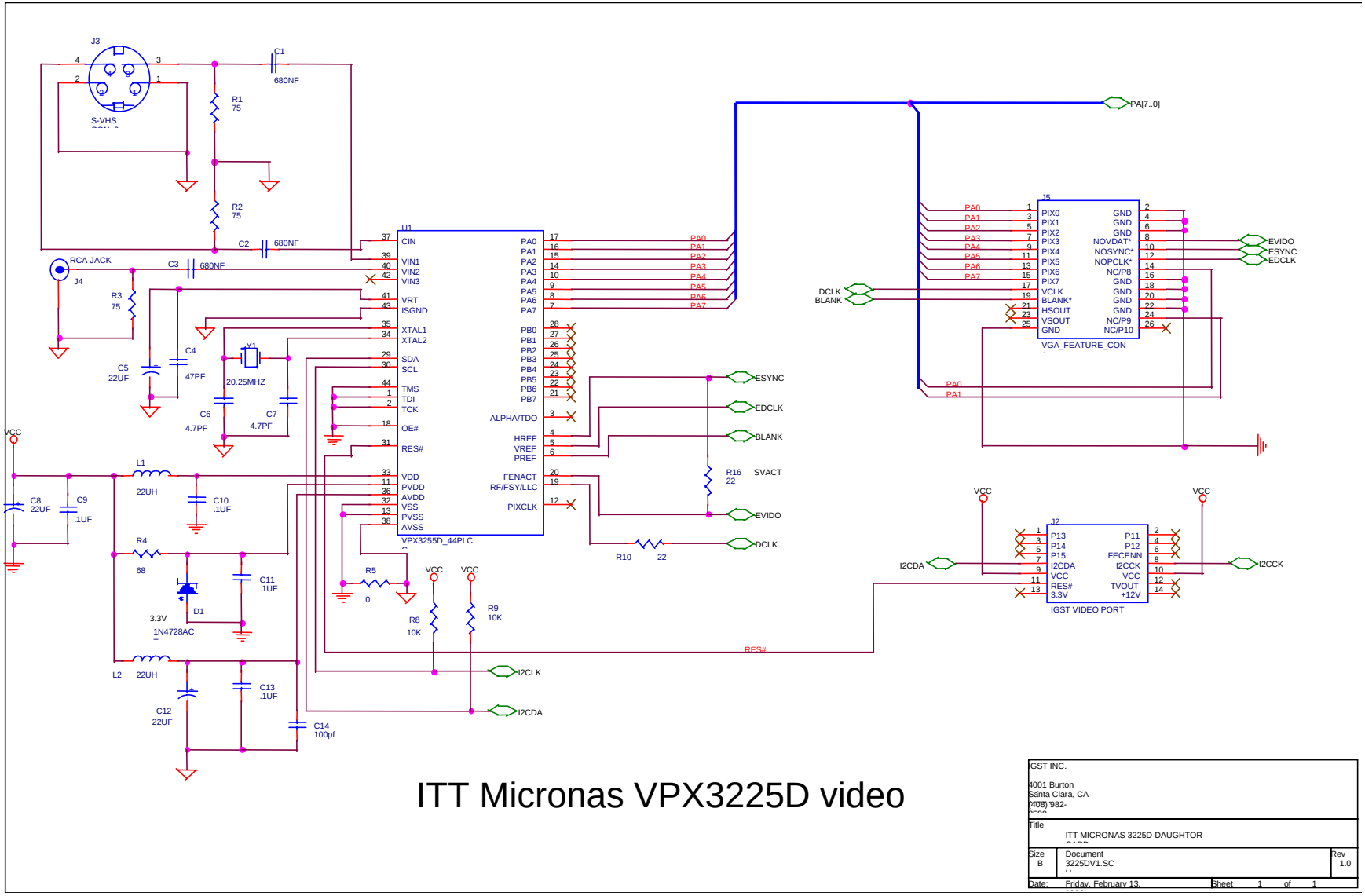

Philips SAA7111A video input
SAA7111A-LQFP
VGA_FEATURE_CON1
IGS VIDEO PORT
Do not fit
Isolate Island
S-VHS
24.576MHz
AS2810-3.3
IGS Inc.
4001 Burton Drive
Santa Clara, CA 95054
(408) 982-8588
Title
7111A DAUGHTER BOARD
Size B
Document Number 7111A.SCH
Rev 1.0
Date: Monday, December 15, 1997
Sheet 1 of 1



Samsung KS0122 video input

IGS INC.		
Size B	Document Number KS0122.SCH	Rev 0.0
Date: Tuesday, February 17, 1998	Sheet 1 of 1	


BT829
Video
Decoder
Rockwell (Brooktree) BT829 video input
BT82x
BT829.SCH
Tuesday, February 17, 1998
VGA_FEATURE_CON1
IGS VIDEO PORT



ITT Micronas VPX3225D video

IGST INC. 4001 Burton Santa Clara, CA (408) 982-		
Title: ITT MICRONAS 3225D DAUGHTOR		
Size: B	Document: 3225DV1.SC	Rev: 1.0
Date: Friday, February 13,	Sheet 1 of 1	

IGS Supported Extended Modes

IGS Mode	VESA Mode	Type	Color	BPP	Alpha Format	Screen Format	Font Type	Buffer Start	V Mem Size	V_Freq (Hz)	H_Freq (KHz)	Dot Clock(MHz)
31	109	Text	16	4	132x25	1056x400	8x16	B8000	256KB	70	31.5	44.9
36	N/A	APA	256	8	N/A	720x540	8x16	A0000	1MB	50	31.25	31
37	N/A	APA	64K	16	N/A	720x540	8x16	A0000	1MB	50	31.25	31
38	N/A	APA	16.8M	24	N/A	720x540	8x16	A0000	2MB	50	31.25	31
39	122	APA	256	8	N/A	640x440	8x16	A0000	1MB	60	31.5	27.19
3A	123	APA	64K	16	N/A	640x440	8x16	A0000	1MB	60	31.5	27.19
3B	124	APA	16.8M	24	N/A	640x440	8x16	A0000	1MB	60	31.5	27.19
43	106	APA	16	4	160x64	1280x1024	8x16	A0000	1MB	60/72/75/87	64.6/78.0/80.0/47.6	108/130/135/80
44	104	APA	16	4	128x48	1024x768	8x16	A0000	512KB	60/72/75/87	48.4/58.5/60.0/35.5	65 /80/78.8/44.9
45	102	APA	16	4	100x75	800x600	8x8	A0000	512KB	60/72/75/56	37.9/47.3/46.9/35.2	40 /50 /49.5/36
46	101	APA	256	8	80x30	640x480	8x16	A0000	512KB	60/72/75	31.5/37.9/37.5	25.177/31.5/31.5
47	103	APA	256	8	100x75	800x600	8x8	A0000	512KB	60/72/75/56	37.9/48.0/46.9/35.2	40 /50 /49.5/36
48	105	APA	256	8	128x48	1024x768	8x16	A0000	1MB	60/72/75/87	48.4/58.5/60.0/35.5	65 /80/78.8/44.9
49	107	APA	256	8	160x64	1280x1024	8x16	A0000	2MB	60/72/75/87	64.0/78.1/80.0/47.6	108/130/135/80
4A	N/A	APA	256	8	200x75	1600x1200	8x16	A0000	2MB	60/72/75/87	76.5/91.0/99.0/55.7	160/182/206/110
4B	100	APA	256	8	80x25	640x400	8x16	A0000	1MB	60	31.5	25.175
4C	120	APA	64K	16	80x25	640x400	8x16	A0000	1MB	60	31.5	25.175
50	111	APA	64K	16	80x30	640x480	8x16	A0000	1MB	60/72/75	31.5/37.9/37.5	25.175/31.5/31.5
51	114	APA	64K	16	100x75	800x600	8x8	A0000	1MB	60/72/75	37.9/48.0/46.9/35.2	40 /50 /49.5/36
52	117	APA	64K	16	128x48	1024x768	8x16	A0000	2MB	60/72/75/87	48.4/58.5/60.0/35.5	65 /80/78.8/44.9
53	11A	APA	64K	16	160x64	1280x1024	8x16	A0000	4MB	60/72/75/87	64.6/78.0/80.0/47.6	108/130/135/80
54	N/A	APA	64K	16	200x75	1600x1200	8x16	A0000	4MB	60/72/75/87	77.0/ / /55.7	160/182/206/110
55	112	APA	16.8M	24	80x30	640x480	8x16	A0000	1MB	60/72/75	31.5/37.9/37.5	25.175/31.5/31.5
56	115	APA	16.8M	24	100x75	800x600	8x8	A0000	2MB	60/72/75	37.9/48.1/46.9/35.2	40 /50 /49.5/36
57	118	APA	16.8M	24	128x48	1024x768	8x16	A0000	4MB	60/72/75/87	48.4/58.5/60.0/35.5	65 /80/78.8/44.9
58	11B	APA	16.8M	24	160x64	1280x1024	8x16	A0000	4MB	60/72/75/87	64.6/78.0/80.0/47.6	108/130/135/80

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